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[54] **LOW VOLTAGE CMOS ANALOG MULTIPLIER WITH EXTENDED INPUT DYNAMIC RANGE**

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[51] **Int. Cl.**⁶ **G05F 3/16; H03F 3/04**

[52] **U.S. Cl.** **323/315; 330/288**

[58] **Field of Search** **323/312, 313, 323/315; 327/538, 539, 543; 330/257, 288**

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[57] **ABSTRACT**

A low voltage CMOS multiplier uses a transconductance stage to generate a dynamic bias current which is used to compensate for non-linear terms in a Gilbert Cell multiplier circuit. Common mode dependence is minimized by using balanced differential input stages for both the transconductance and multiplier stages.

5 Claims, 3 Drawing Sheets

