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Batra et al.

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[54] **THIN FILM TRANSISTORS**

[75] Inventors: **Shubneesh Batra**, Boise; **Monte Manning**, Kuna, both of Id.; **Sanjay Banerjee**; **John Damiano, Jr.**, both of Austin, Tex.

[73] Assignee: **Micron Technology, Inc.**, Boise, Id.

[*] Notice: This patent is subject to a terminal disclaimer.

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Related U.S. Application Data

[60] Continuation of application No. 08/484,979, Jun. 7, 1995, Pat. No. 5,548,132, which is a division of application No. 08/328,096, Oct. 24, 1994, abandoned.

[51] **Int. Cl.**^{6} **H01L 29/04**; H01L 31/036

[52] **U.S. Cl.** **257/66**; 257/327; 257/64; 257/393

[58] **Field of Search** 257/64, 65, 66, 257/67, 69, 70, 327, 390, 391, 392, 393, 401

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,385,937	5/1983	Ohmura	438/162
4,420,870	12/1983	Kimura	438/162
4,498,224	2/1985	Manguchi	438/162
4,528,480	7/1985	Unagami et al.	315/169
5,112,764	5/1992	Mitra et al.	437/41 TFT
5,198,379	3/1993	Adan	437/44
5,208,476	5/1993	Inoue	257/66
5,266,507	11/1993	Wu	437/41
5,286,663	2/1994	Manning	437/46
5,292,675	3/1994	Codama	437/41 TFT
5,308,998	5/1994	Yamazaki et al.	437/41 TFT
5,323,042	6/1994	Matsumoto	437/41 TFT
5,344,790	9/1994	Bryant et al.	437/41 TFT
5,412,493	5/1995	Kunii et al.	437/41 TFT
5,420,055	5/1995	Vu et al.	438/162
5,457,058	10/1995	Yonehara	438/166

FOREIGN PATENT DOCUMENTS

58-56467	4/1983	Japan	437/21
62-76772	4/1987	Japan .	
111369	1/1989	Japan .	
150569	2/1989	Japan .	
1-158775	6/1989	Japan	437/46
1-251668	10/1989	Japan	437/40
3-104210	5/1991	Japan	437/46
4-152639	5/1992	Japan .	
4-162432	6/1992	Japan .	
4-306843	10/1992	Japan .	
5-152329	6/1993	Japan	437/40 TF
6-112223	4/1994	Japan .	
6-163580	6/1994	Japan	437/21
6-232160	8/1994	Japan	437/21

OTHER PUBLICATIONS

Wolf, S., "Silicon Processing For The VLSI Era", vol. II, pp. 354–361 and 436–439.

Hayden et al., A High–Performance Quadruple Well, Quadruple Poly BiCMOS Process For Fast 16Mb SRAMs, IEEE, IEDM 92/819, pp. 819–822, 1992.

(List continued on next page.)

Primary Examiner—Carl Whitehead, Jr.
Attorney, Agent, or Firm—Wells, St. John, Roberts, Gregory & Matkin, P.S.

[57] **ABSTRACT**

A thin film transistor includes: a) a thin film transistor layer comprising a source region, a channel region and a drain region; the thin film transistor layer further comprising a drain offset region positioned between the drain region and the channel region; b) the channel region being substantially polycrystalline and having a first average crystalline grain size; and c) the drain offset region being substantially polycrystalline and having a second average crystalline grain size, the second average crystalline grain size being larger than the first average crystalline grain size. A method for forming such a construction using polycrystalline materials, preferably polysilicon, and an amorphizing silicon implant with subsequent recrystallization is also disclosed.

23 Claims, 5 Drawing Sheets