ABSTRACT

YELTEN, MUSTAFA BERKE. Theoretical Analysis and Design Methodologies for Low Noise Amplifiers based on Tunable Matching Networks. (Under the direction of Dr. Kevin G. Gard.)

The low noise amplifiers (LNAs) have a big importance in the noise performance of the receiver structures for wireless communication devices. Various design procedures and design examples have been suggested for narrowband frequency applications. However, with the increase in the number of different standards in the wireless communication technologies, a rising demand for receiver topologies that will operate at multiple frequencies by preserving the noise, gain and linearity responses reached at a single frequency has been observed. One method to achieve this target is to employ tunable passive components in the circuit. Tunable components give the flexibility of changing the component value for a certain frequency band with a considerable quality factor. Recent studies indicate that various tunable components can be fabricated for radio frequency and microwave integrated circuits with which the design topologies for various building blocks can be converted into their tunable equivalents.

This thesis considers the usage of tunable reactive components in the low noise amplifiers from the theoretical and design perspective. The implemented topologies are based on heterojunction bipolar transistors (HBTs) from the IBM 0.18 μm BICMOS (7HP) design kit. The first part of this thesis considers the theoretical derivation of the quantities, the input impedance and optimum noise impedance, Z_{in} and Z_{OPT}, on which the low noise design principles are built. Subsequently, a design methodology that will be more suitable for tunable low noise amplifier application is developed based on the theoretical calculations presented in the previous part. To demonstrate the design procedure, a LNA operating at 5

GHz will be presented both with ideal and non-ideal reactive components. Then, the tunability aspect of the design procedure is investigated by building two more LNA structures operating at 1 GHz and 10 GHz whereby all passive components are assumed to be tunable. Considering the fact that tunable components actually add noise and nonlinearity to the design structures, a single component, the series matching capacitor is chosen to be the only tunable element in the circuit. The design at 5 GHz is repeated with this constraint and the range for which the noise and input matching characteristics are preserved is determined. It is possible to acquire 3 GHz of bandwidth (3.5 GHz to 6.5 GHz) where the noise figure of the design is very close to the minimum noise figure of the LNA ($NF- NF_{min}<0.5$ dB) and the input matching is sufficient ($S_{11}<-10$ dB). Finally, a feasibility analysis is completed to clarify the issue to what extent the current tunable components can meet the specifications derived from the finished tunable designs.

Theoretical Analysis and Design Methodologies for Low Noise Amplifiers based on Tunable Matching Networks

by
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DEDICATION

To my mother Ufuk, my father Muhammet, and my sister Azade,

for their continuous support, patience and love

To my grandma Suat Berk (1929-2002),

who prepared carrot juices every single morning by her hands when I was a child

so that I can become ‘a clever guy’

BIOGRAPHY

Mustafa Berke Yelten was born on the 10th August 1982, in Istanbul, Turkey. In 2001, he finished his high school education in Istanbul (Erkek) Lisesi. Afterwards, he attended Bogazici University Electrical & Electronics Engineering Department, Istanbul and graduated from there in June 2006, receiving his Bachelor of Science (BS) degree with High Honors. Then, he decided to continue his academic endeavors in North Carolina State University Electrical and Computer Engineering Department (NCSU ECE) and came for this purpose to Raleigh, NC in August 2006. He specialized in analog circuit design and solid state electronics and began researching in the area of radio frequency integrated circuit design (RFIC) under the direction of Dr. Kevin G. Gard in September 2007.

Mustafa Berke Yelten has been a member of Institute of Electrical and Electronics Engineers (IEEE) since 2003 and he has been inducted to the highly selective academic excellence society Phi Kappa Phi in October 2007. Moreover, he completed the newly established certificate program in Teaching Accomplishment (CoAT) of NCSU in April 2008. This program aims to flourish the skills of teaching in academic researchers.

Apart from the engineering career, Mustafa Berke Yelten is a published poet in Turkey and has been awarded with several prizes for his poems and short stories. His first poetry book was published in 2006. A second poetry book mainly inspired by the city of Raleigh will be ready for the publication in couple years.

ACKNOWLEDGMENTS

First of all, I would like to thank Dr. Kevin G. Gard, for providing me this research opportunity with him. His passion in analog circuits and RFIC design also the research perspective composed of both theoretical and practical analysis inspired me deeply. Our conversations with him turned out to be very helpful to bear up novel understanding to our research area and thus, I enjoyed a great advisor-student relationship for the last year.

I would like to express my best feelings to Dr. Wm. Rhett Davis and Dr. Brian Hughes for serving in my committee.

During the time I spent in Raleigh, I had several friends whose existence is important to me. I am very happy to know Namik Kemal Temizer and Nurcan Tezcan. They not only helped me to settle down and enjoy this little though nice city, but also gave hints and suggestions on various problems that I encountered over the time. Besides, I am thankful to Inci Ozdemir, Nazli Dokuzoglu, Ates Dumlupinar, Harun Demircioglu and Attila Altay Yavuz for their kind friendship and their support during the tough periods of research.

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CHAPTER 1

1 THESIS MOTIVATION, TARGET AND OUTLINE

1.1 THESIS MOTIVATION AND TARGET

This thesis concentrates on the operation characteristics of the low noise amplifiers (LNAs). Low noise amplifiers constitute the first stage of a classical receiver structure as can be visualized in Figure 1. The reason for that can be understood with the properties of LNAs. They should have a low noise figure, a reasonable gain and a high dynamic range. Dynamic range refers to the ratio of the highest and lowest input power for which the LNA maintains its linear operation. The first two issues are more dominant compared to the last one in terms of the effect on the general operation. Due to the fact that the transmission medium contaminates the transmitted signal with undesired signals, the received message signal is weak in terms of power. For a perfect processing of the message to occur the receiver hardware should add minimum noise on the message signal. As will be explained in the later sections, the overall noise figure of a multi-stage structure depends heavily on the noise figure and the gain of the first stage.

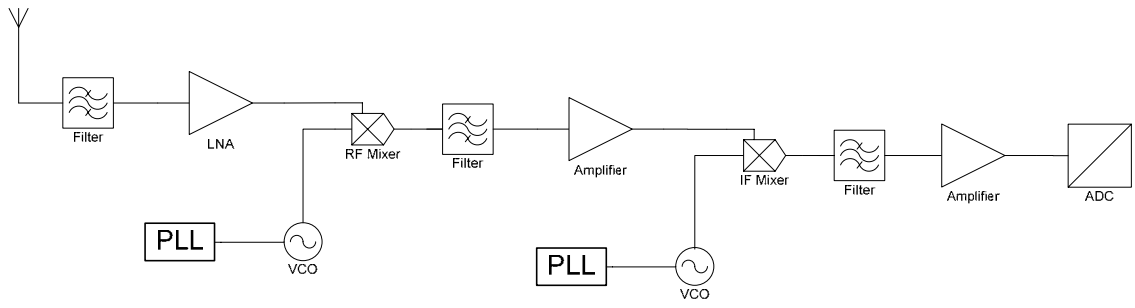

Figure 1: A simplified diagram depicting the common structure of a receiver

So, the low noise amplifier should be designed such that the noise and gain performance can be maximized. This target can be fully achieved for a narrowband operation. Nevertheless, many different communication standards appeared in the recent past so that different frequency bands have been allocated for distinct purposes. This situation necessitated that multiple receiver structures should be utilized in order to fulfill the needs of several frequencies. This means a corresponding increase in the additional hardware to be employed which in turn results in undesirably high power consumption. A practical solution is posed as the wideband design where the design outcomes for the noise, gain and linearity which is a concept directly related with the dynamic range, have been deteriorated up to an acceptable limit such that they can prevail for a larger bandwidth. There are successful examples of this approach [1], [2]. Nevertheless, a better option is to get the characteristics of a narrow-band LNA at each frequency point in a wideband LNA. To realize this scheme, the reactive elements utilized in the circuit topology should be tunable so that the best operation characteristics can be transmitted to other frequencies by making the necessary changes in the component values.

Thus, it is important to understand the theoretical background of the low noise amplifiers related to their noise and gain calculations by analyzing them on the grounds of their small signal circuit diagram. Furthermore, a relatively different perspective to the LNA design procedure based on the theoretical analysis should be derived. The topology of the amplifier has to be modified such that some reactive components can be replaced by their tunable equivalents and with the application of the derived procedure, a tunable low noise amplifier can be accomplished. Finally, the key components which should be tunable have to

be determined and the feasibility of using practical, tunable reactive elements which currently exist should be investigated.

1.2 THESIS OUTLINE

The organization of the thesis can be provided as follows:

Chapter 2 deals with the theoretical discussion of the noise parameters. Concepts in noise theory are defined and their relationships with each other are quantified by the associated formulas.

Chapter 3 introduces the design procedure that has been proposed for the construction of the tunable low noise amplifiers. The design procedure is composed of algorithmic steps that are based on the theoretical background given in Chapter 2. This methodology is validated by two design examples where ideal and realistic reactive components are utilized, respectively. A discussion on linearity aspect of the designs concludes this chapter.

Chapter 4 is the part of the thesis where the tunability aspect of the designs is studied more deeply. Two different frequencies, 1 GHz and 10 GHz, are taken to demonstrate the claim that simultaneous input and noise matching can be managed by changing the values of all the passive elements in the circuit. Then, the key component for the tunable operation of the low noise amplifier is chosen as the series matching capacitor at the base of the heterojunction bipolar transistor (HBT). Both designs given in Chapter 3 are analyzed from this perspective. The chapter is finalized with a comparison of the specifications derived from the tunability study conducted in this thesis and the current standards of practical, tunable capacitors.

CHAPTER 2

2 NOISE ANALYSIS OF HETEROJUNCTION BIPOLAR TRANSISTOR (HBT) LOW NOISE AMPLIFIERS

2.1 CONCEPTS IN NOISE ANALYSIS

To begin with, noise is a random process [3]. Unlike the other electrical quantities such as the current and voltages, which can be represented by a magnitude and the direction or orientation, respectively, noise should be expressed in terms of power spectral density. In order to reach the exact relationship between the noise and power density, one has to consider the fact that noise can be interpreted as a "fluctuation" that can be characterized with a non-periodic change around its mean value [4]. Basically, the origins of noise stem from the physical phenomena which incur these variations on top of the main quantities such as voltages or currents. These mechanisms will be discussed in the forthcoming sections more in detail. Nevertheless, it should be observed that there are sources of voltage and current noise, which can be best described in their power content.

At this point, one can proceed by calculating the mean square value of the noise signal as in (2.1) [4]. A voltage noise source will be assumed for the calculations below, however, similar approach can be adopted for the current noise sources also.

$$\overline{v^2} = \left(V_{RMS}\right)^2 = \frac{1}{T}\int_0^T v^2 dt \qquad (2.1)$$

In all noise calculations, the mean square values of noise sources will be utilized. As mentioned before, this quantity should be in contact with the power content of the noise contributors over the frequency. By considering a narrow-band operation with a finite amount of frequency band (ex. 1Hz) centered on the frequency of operation f_0 one can express the spectral power density as follows [4]:

$$S_V(f) = \frac{V_{RMS}^2}{\Delta f} \qquad (2.2)$$

With these two basic quantities, it is possible to describe the noise sources. Nevertheless, a plethora of different interactions between each noise sources in a physical device can be observed, which necessitate accounting for the overlaps in the frequency. This issue is called the correlation between noise signals and mathematically, the definition of correlation is given below:

$$c = \frac{\overline{v_a v_b}}{\sqrt{\overline{v_a^2}\,\overline{v_b^2}}} \qquad (2.3)$$

In (2.3), c is the correlation factor, that provides the amount of correlation between the two voltage noise sources v_a and v_b. It should be noted that the correlation might exist between voltage and current noise sources, as well. In a detailed noise calculation, each noise source within the investigated physical system and the correlation between them have to be considered in order to assess the low noise operation properties of the particular electronic structure.

2.2 PHYSICAL ORIGINS OF NOISE SOURCES

It is now appropriate to deepen the analysis into the various phenomena that cause the noise sources to come true. There are different types of noise sources in the electronic circuits that might be encountered during analysis stages; however, within this section four of them will be covered due to the nature of the thesis:

2.2.1 Thermal Noise

Thermal noise is a characteristic of the resistors but it also exists in the nonideal reactive elements such as inductors and capacitors. The loss due to the material properties of these electrical components is the main reason for the creation of the thermal noise. It is easy to conceptualize that as the temperature rises, the Brownian motion of the electrons increase as well, yielding higher level of fluctuations which directly influence the spectral power density of the associated noise. Thus, the spectral power density can be given as follows [3]:

$$S_V(f) = 4k_B TR \qquad (2.4)$$

In (2.4), k_B is the Boltzmann constant having a value of 1.38 x 10^{-23} J/K, T is the absolute temperature and R is the resistance of the particular element. In reactive components, R will represent the series parasitic resistance that expresses the non-ideal character. An important feature of the thermal noise can also be observed by its power density. It is constant over the frequency band, thus the available spectral power per bandwidth delivered to the resistive structure is just k_BT, a fixed quantity. This enables to model the thermal noise as a Gaussian noise process at high frequencies [3].

Using these facts, it is straightforward to calculate the associated voltage and current noise sources. By using (2.1) and (2.2), one can find them subsequently:

$$\overline{v_{Th}^2} = 4k_B T \Delta f R \qquad (2.5)$$

$$\overline{i_{Th}^2} = \frac{4k_B T \Delta f}{R} \qquad (2.6)$$

2.2.2 Shot Noise

Shot noise is a typical phenomenon that takes place in semiconductor junctions where the charge carriers have to overcome an energy barrier while crossing the depletion region. During the transit of electrons and holes, their motion causes certain fluctuations that build the specific current noise on top of the junction current, I_J. Shot noise has been observed in various semiconductor devices such as pn-junctions, Schottky diodes and bipolar junction transistors (BJTs) [4]. A simple formula yields the respective current noise source, where q is the unit electronic charge, with the value of 1.6×10^{-19} C.

$$\overline{i_{Sh}^2} = 2qI_J \Delta f \qquad (2.7)$$

Like the thermal noise, shot noise can be assumed to have a flat frequency spectrum resulting in a Gaussian noise process as long as the transit time of the charge carriers is shorter than the inverse of the operating frequency [3]. Another important fact about the shot noise is that it cannot be observed in linear resistors [5].

2.2.3 Flicker Noise

Flicker noise can be easily distinguished from the thermal noise and the shot noise due to the special properties of its spectrum which is strongly depending on the frequency.

Specifically it changes inversely with the frequency, thus it is also often called 1/f noise.

Various studies have shown that the flicker of 1/f noise depends on the structure of the semiconductor surface and the associated problems with that structure experienced by the charge carriers. In that respect, the metal oxide semiconductor transistors (MOSFETs) suffer significantly from the flicker noise. On the other hand, the charge transport happens to be orthogonally to the semiconductor interface in BJTs, that's why, the 1/f noise is effective in their total noise content [3]. A common model quantifies the flicker noise as follows:

$$\overline{i_{1/f}^2} = \frac{k_f I^{\alpha}}{f^{\beta}} \Delta f \qquad (2.8)$$

In (2.8), I represents the current through the device, f is the operation frequency and k_f, α, and β are experimental parameters.

A good measure of this type of noise is the corner frequency at which the total noise due to the thermal and shot noise is equal to the contribution of the flicker noise [5]. As can be expected from the statements above, the corner frequency for MOSFETs is located at much higher frequencies compared to the BJT devices. From a perspective of phase noise that is observed in the vicinity the oscillation frequency (generally defined at 100 kHz or 1 MHz), BJTs suggest better alternatives for oscillator design compared to the MOSFETs. In the context of this thesis, however, flicker noise does not play a crucial role since its impact is restricted to lower frequencies and cannot be extended to GHz levels. Thus, in the upcoming noise analysis of HBTs, the flicker noise will be neglected.

2.2.4 Burst Noise

Burst noise is again a noise source type whose spectrum depends on the operation frequency with a special relation of $1/f^2$. In that respect, its characteristics resemble to the ones of the flicker noise, thus, it is mainly a noise contributor at lower frequency bands. Its origins have not been understood fully but it can be attributed to the metal ion contamination [5]. Again, due to the nature of analysis described in this thesis, burst noise will not be taken into account.

2.3 NOISE SOURCES IN HBT DEVICES

In the previous section, different noise source types have been investigated and characterized. Since within this thesis, the SiGe HBT transistors will be utilized for the device type, the noise sources of HBTs should be analyzed more in detail.

Before continuing with the descriptions of the noise sources, one has to remember the general physical structure of the HBTs. HBT has actually the same structure of BJTs [6]. In a BJT, there exist three terminals, named as collector, base and emitter. The semiconductors used in these terminals can be doped in two distinct fashions. For a NPN BJT, the emitter and the collector are doped with n-type of dopants (Group V elements) whereas the base is doped with p-type of dopants (Group III elements). Conversely, a PNP BJT has p-type doped emitter and collector, also an n-type doped base. As the names of the terminals suggest, there exist two pn-junctions between the base and emitter as well as between the base and the collector in a NPN BJT. For a BJT, both of these junctions are homojunctions, i.e. the same semiconductor is made use of for all the terminal structures. However, this preference causes

some limitations on the hole transport from the base to the emitter and on the transit time through the base in NPN transistors [4]. Especially, the second restriction inhibits the BJT devices to operate at very high frequencies. In HBTs, this problem can be overcome by preparing hetero-junctions where the material for the base is chosen such that the band-gap of the base material is smaller than the emitter material [7]. The abrupt heterojunction will accelerate the charge carriers and thus enable the device to operate at elevated frequencies.

After reviewing the physical background of HBT devices, it is easier to consider the noise sources. There are mainly 4 different noise contributors as it has been indicated in Figure 2. Figure 2 shows the small signal diagram of a HBT in hybrid-π configuration.

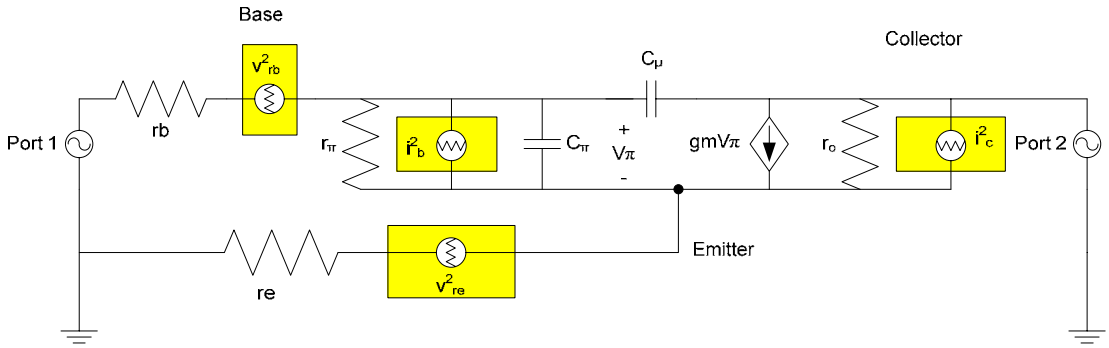

Figure 2: The noise source types within the HBT devices

The first two can be characterized as thermal noise sources which are $\overline{v_{r_b}^2}$ and $\overline{v_{r_e}^2}$. These are created by the parasitic base and emitter resistances. The base resistance is larger than the emitter resistance and for a common-emitter amplifier configuration, it adds up directly to the total input referred noise. Nevertheless, its value is no larger than of several ohms. The base and emitter resistance thermal noise sources can be expressed mathematically as it is provided in (2.9) and (2.10), respectively:

$$\overline{v_{r_b}^2} = 4k_B T \Delta f \; r_b \qquad (2.9)$$

$$\overline{v_{r_e}^2} = 4k_B T \Delta f \; r_e \qquad (2.10)$$

The parasitic emitter resistance is in the order of couple ohms and it becomes specifically important for the common-base topology where the input signal is given from the emitter of the transistor. In this thesis, mainly, cascode BJT structure will be utilized, where the first stage which is in the common emitter topology, basically determines the input referred noise. Thus, during the theoretical analysis emitter resistance will be neglected.

The other two noise sources stem from the physical structure of the HBTs. Each semiconductor junction within the device possesses an associated shot noise with itself. For the base-collector junction, the shot noise can be formulated where I_C is the collector current of the HBT:

$$\overline{i_C^2} = 2qI_C \Delta f \qquad (2.11)$$

Similarly, for the base-emitter junction, same phenomenon can be observed, thus the associated shot noise is given as in (2.12) with I_B representing the base current:

$$\overline{i_B^2} = 2qI_B \Delta f \qquad (2.12)$$

In (2.11) and (2.12), the currents I_B and I_C should be clarified further. There are several different SPICE models for the simulation of the BJTs such as the Gummel-Poon [8], HICUM [9], and VBIC [10] that depend on the physical structure briefly explained above. The IBM design kit, which has been utilized throughout this thesis, has adopted the VBIC model that closely resembles to the Gummel-Poon model [10]. According to the VBIC model, the base and collector currents can be given as in (2.13) and (2.14):

$$I_B = WBE\left\{IBEI\left[\exp\left(\frac{V_{BEi}}{NEI*VT}\right)-1\right]-IBEN\left[\exp\left(\frac{V_{BEi}}{NEN*VT}\right)-1\right]\right\} \qquad (2.13)$$

$$I_C = \frac{I_S}{q_b}\left[\exp\left(\frac{V_{BEi}}{NF*VT}\right)-1\right]-\frac{I_S}{q_b}\left[\exp\left(\frac{V_{BCi}}{NR*VT}\right)-1\right] \qquad (2.14)$$

(2.13) and (2.14) contain various SPICE parameters such as WBE, IBEI, IBEN, NF, NR, and NEN. VBIC distinguish between the intrinsic and extrinsic base-collector and base-emitter voltages by incurring the extrinsic base, emitter and collector resistances. Also, in the equations above, I_S represents the saturation current, q_B is the normalized base resistance and V_T provides the thermal voltage that is by definition equal to k_BT/q. At room temperature, this expression yields a value of approximately 25.9 mV. More information about the derivation and description of VBIC parameters and equations can be found in the original article introducing VBIC model [10].

Before concluding this section, it should also be mentioned that the resistance r_π and r_o are not physical, thus it does not have a thermal noise component. For low frequencies, one can easily compute the value of r_π by using the transconductance g_m and the common emitter current gain β. All relations are provided in (2.15), (2.16) and (2.17) [11]:

$$g_m = \frac{I_C}{V_T} = \frac{qI_C}{k_BT} \qquad (2.15)$$

$$\beta = \frac{I_C}{I_B} \qquad (2.16)$$

$$r_\pi = \frac{\beta}{g_m} = \frac{V_T}{I_B} \qquad (2.17)$$

Similarly, r_o can be calculated with the help of the collector current and the Early Voltage V_A as in (2.18). Finally, it should not be forgotten that C_π and C_μ are ideal components; there fore they do not contribute to the total noise content of the device.

$$r_o = \frac{V_A}{I_C} \qquad (2.18)$$

2.4 CLASSICAL TWO PORT NOISE THEORY

As can be realized in 2.3, several noise sources take place at specific physical locations of the HBT devices. However, if one tries to find the noise content of the device as a whole, it becomes confusing how to regard the contributions of each noise source. To accomplish this analysis, a simple but robust approach should be created. Throughout the research history of the noise in linear circuits [12], a model of two-port network has been developed to get the noise parameters of the device under test (DUT). HBTs are three terminal devices; however depending on the single stage amplifier topologies, one terminal can be taken as 'common', so that the two other terminals constitute two distinct ports with the common terminal. For the single stage common emitter amplifier, the two ports can be built as the base-emitter and collector-emitter port. Since for this topology, the input is applied from the base and the output is taken from the collector, the base-emitter port can be called input port and the collector-emitter port becomes then the output port.

The next step is to express the total noise content that can be measured from one of the ports. For the case of low noise design, circuit designers are interested to find out the noise that is experienced at the input port which is described as the input referred noise, since this noise amount dictates the design specifications for the receiver structure. Thus, the

analysis that will be presented next is targeting to extract the input referred noise based on the discrete noise sources in the transistor.

To accomplish the task provided above, first of all, the necessary transfer functions have to be derived. These transfer functions have to relate the noise source and the contribution of it to the input referred noise. To understand the mechanism better, Figure 3 and Figure 4 could be helpful. As can be observed in Figure 3, noisy two-port network could be the DUT such as the HBT in this case. Afterward, this noisy network should be analyzed such that with the help of transfer functions, a noiseless two port network can be shaped. This noiseless network will be accompanied by the input referred equivalent voltage and current noise sources so that the total noise content of the DUT can be accounted. The resulting scheme can be visualized in Figure 4.

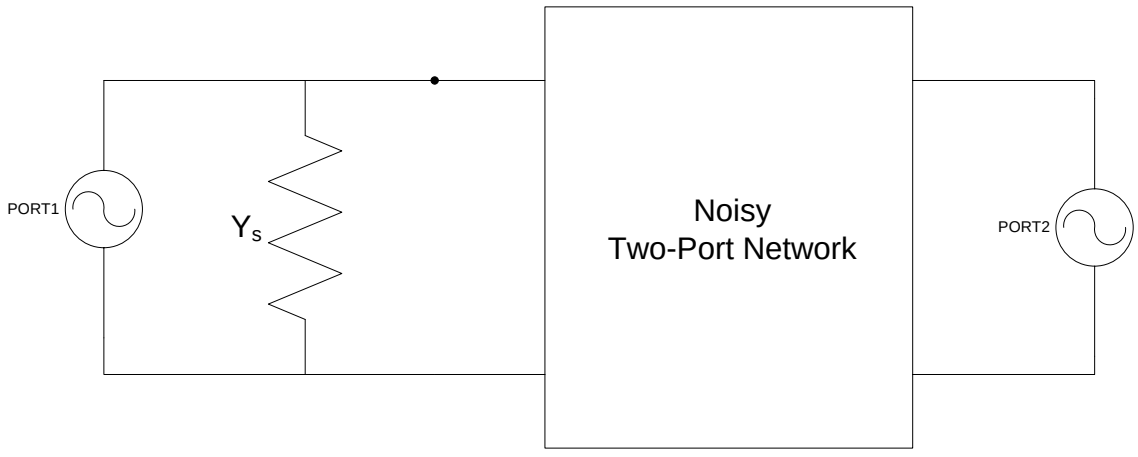

Figure 3: An example of a two-port noisy network

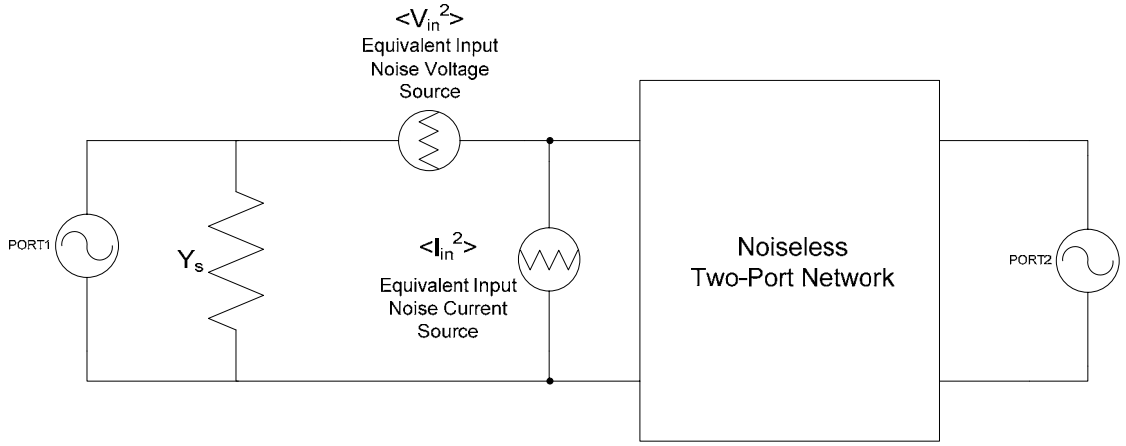

Figure 4: Noiseless two-port network with the equivalent noise sources

After the equivalent input voltage and current noise sources are determined, the possibility of correlation between these two components should be investigated. It is likely since the same noise sources in the output port of the device may be contributing to both the equivalent current and voltage noise sources. The exact nature of correlation can be expressed when a correlation matrix can be established. For this purpose, chain representation of correlation matrix seems the best choice [4]. This selection is actually associated with the two port network selection in Figure 3 above.

The chain representation may be provided as in (2.19):

$$N = \begin{bmatrix} \overline{v_{in}v_{in}^*} & \overline{v_{in}i_{in}^*} \\ \overline{i_{in}v_{in}^*} & \overline{i_{in}i_{in}^*} \end{bmatrix} = \begin{bmatrix} \overline{v_{in}^2} & \overline{v_{in}i_{in}^*} \\ \overline{i_{in}v_{in}^*} & \overline{i_{in}^2} \end{bmatrix} \qquad (2.19)$$

The values in the matrix above can be normalized by dividing them to $4k_BT\Delta f$. The resulting matrix is named as C_A normalized chain correlation matrix.

$$C_A = \begin{bmatrix} \dfrac{\overline{v_{in}^2}}{4k_B T \Delta f} & \dfrac{\overline{v_{in} i_{in}^*}}{4k_B T \Delta f} \\ \dfrac{\overline{i_{in} v_{in}^*}}{4k_B T \Delta f} & \dfrac{\overline{i_{in}^2}}{4k_B T \Delta f} \end{bmatrix} = \begin{bmatrix} C_{A,11} & C_{A,12} \\ C_{A,21} & C_{A,22} \end{bmatrix} \qquad (2.20)$$

These parameters are calculated in order to inquire for the minimum possible noise figure that can be accomplished with the given linear two-port network. In order to manage this special situation, one has to apply certain source admittance (or impedance) so that the source is matched to the admittance required by the linear two-port network that will result in the minimum noise figure. This specific source admittance ($Y_{S,OPT}$) is constituted by the optimum noise source conductance ($G_{S,OPT}$) and the optimum noise source susceptance ($B_{S,OPT}$).

$$Y_{S,OPT} = G_{S,OPT} + j\, B_{S,OPT} \qquad (2.21)$$

Past research enables to find a way with which one can use the normalized chain correlation matrix to compute the optimum source noise conductance and susceptance [13].

$$G_{S,OPT} = \sqrt{\frac{C_{A,22}}{C_{A,11}} - \left[\frac{\mathrm{Im}\left(C_{A,12}\right)}{C_{A,11}}\right]^2} \qquad (2.22)$$

$$B_{S,OPT} = \frac{\mathrm{Im}\left[\left(C_{A,12}\right)\right]}{C_{A,11}} \qquad (2.23)$$

Now, optimum noise source conductance and susceptance can also be expressed regarding the transistor structure. In order to get the minimum noise operation, the device should present an impedance equal to $Z_{OPT}=Z^*_{S,OPT}$. Then, one can write:

$$G_{OPT} = G_{S,OPT} \qquad (2.24)$$

$$B_{OPT} = -B_{S,OPT} \tag{2.25}$$

Since the parameters defined with (2.24) and (2.25) are easier to handle within the procedure, the simulations and theoretical calculations will be based upon them.

The minimum noise factor that will correspond to the values of optimum source conductance and susceptance can be determined as provided in (2.26):

$$F_{\min} = 1 + 2\left[\mathrm{Re}\left(C_{A,12}\right) + C_{A,11} G_{OPT} \right] \tag{2.26}$$

Once the noise factor is found out, it can be converted easily to the noise figure via the simple relationship:

$$NF = 10 \log\left(F\right) \tag{2.27}$$

2.5 DETERMINATION OF INPUT AND OPTIMUM NOISE IMPEDANCE PARAMETERS

The input and optimum noise impedance parameters will be calculated based on the topology depicted in Figure 5.

The derivation of R_{OPT}, X_{OPT}, R_{in} and X_{in} are not straightforward. A variety of calculation and approximation techniques have to be adopted in order to find a compact answer. Appendix A and Appendix C have been devoted for this purpose where detailed mathematical analysis is presented. X_{eqv} is the modified input reactance that can be found after the addition of the bias inductor L_c. L_c should be chosen such that X_{eqv} and X_{OPT} become equal. The exact derivation of X_{eqv} from X_{in} is provided in Appendix B, whereas the importance of L_c and X_{eqv} are shown in Chapter 3. In this section, the results will be given and comparison with the theoretical data is going to be done.

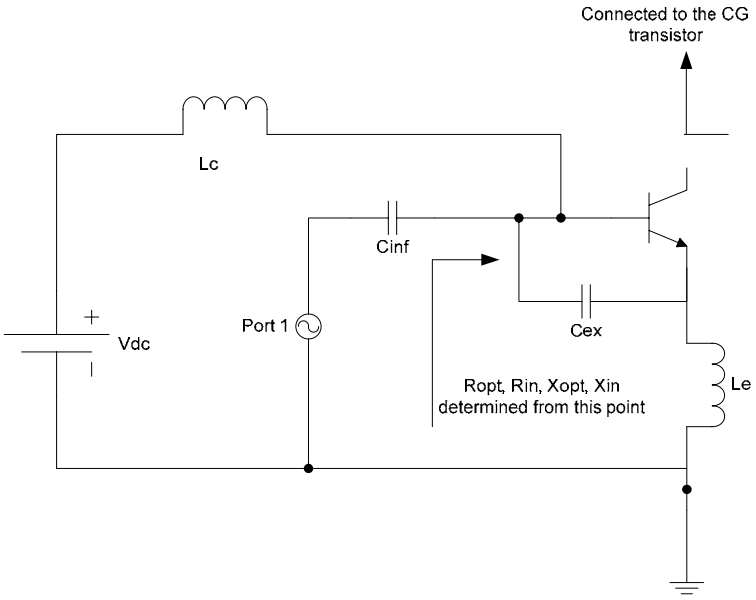

Figure 5: Simplified circuit structure of the input part of the cascode to determine Ropt, Rin, Xin, Xopt

So, R_{in}, X_{in}, X_{OPT}, and R_{OPT} can be given as follows:

$$R_{in} \approx \left\{ \frac{\left[r_\pi - \omega^2 r_\pi^2 C_\mu L_e g_m \left(1 - \omega^2 L_e C_\pi\right) + \omega^2 r_\pi^2 L_e C_\pi g_m \right]}{\left[\left(1 - \omega^2 C_\mu L_e g_m r_\pi\right)^2 + \omega^2 r_\pi^2 C_\pi^2 \right]} \right\} \tag{2.28}$$

$$X_{in} \approx \left\{ \frac{\left\{ \omega L_e \left[\left(1 + g_m r_\pi + \omega^2 r_\pi^2 C_\pi^2\right) - \omega^2 g_m^2 r_\pi^2 L_e C_\mu \right] - \omega C_\pi r_\pi^2 \right\}}{\left[\left(1 - \omega^2 C_\mu L_e g_m r_\pi\right)^2 + \omega^2 r_\pi^2 C_\pi^2 \right]} \right\} \tag{2.29}$$

$$X_{eqv} = \omega \left[\frac{L_c X_{in} \left(X_{in} + \omega L_c \right) + R_{in}^2 L_c}{R_{in}^2 + \left(X_{in} + \omega L_c \right)^2} \right] \tag{2.30}$$

$$X_{OPT} \approx 2 g_m \left(1 + \omega^2 L_e C_\mu\right)^4 \left\{ \begin{array}{l} \left(\frac{1}{r_\pi} + \left(\frac{L_e}{L_c} \right) g_m - \omega^2 L_e C_\mu g_m \right) \omega L_e g_m \left(1 + \omega^2 C_\mu L_e\right)^2 - \\ \left[\omega C_\mu + \omega C_\pi \left(1 + \frac{L_e}{L_c} \right) - \frac{1}{\omega L_c} \right] \left(1 - \omega^2 C_\pi L_e\right) \end{array} \right\}^{-1} \tag{2.31}$$

$$R_{OPT}=\left\{\sqrt{\left\{\frac{\left\{\frac{\left[\left(\frac{1}{r_\pi}-\omega^2L_eC_\mu g_m\right)\left(1+\omega^2C_\mu L_e\right)\right]^2+\left[\omega\left(C_\pi+C_\mu\right)\right]^2}{g_m^2\left(1+\omega^2L_eC_\mu\right)^4}\right\}\times\left\{\left(\frac{g_m}{2}\right)\left[1+\frac{1}{\left(1+\omega^2r_\pi^2C_\pi^2\right)}\right]\right\}}{r_b+\left\{\frac{\left(1-\omega^2L_eC_\pi\right)^2+\left[\omega L_eg_m\left(1+\omega^2C_\mu L_e\right)\right]^2}{g_m^2\left(1+\omega^2C_\mu L_e\right)^4}\right\}\frac{g_m}{2}}-\left(\frac{\frac{1}{2g_m\left(1+\omega^2L_eC_\mu\right)^4}\left\{\begin{array}{l}\omega L_eg_m\left(1+\omega^2C_\mu L_e\right)^2\left(\frac{1}{r_\pi}-\omega^2L_eC_\mu g_m\right)-\\ \omega\left(C_\pi+C_\mu\right)\left(1-\omega^2C_\pi L_e\right)\end{array}\right\}}{r_b+\left\{\frac{\left(1-\omega^2L_eC_\pi\right)^2+\left[\omega L_eg_m\left(1+\omega^2C_\mu L_e\right)\right]^2}{g_m^2\left(1+\omega^2C_\mu L_e\right)^4}\right\}\frac{g_m}{2}}\right)^2\right\}}\right\}^{-1} \tag{2.32}$$

These results can be compared with the simulation outcomes. Figure 6 through Figure 10 are depicting each quantity separately.

It should also be mentioned that the passive components in the simulation are taken ideal since the theoretical analysis does not consider the losses associated with them.

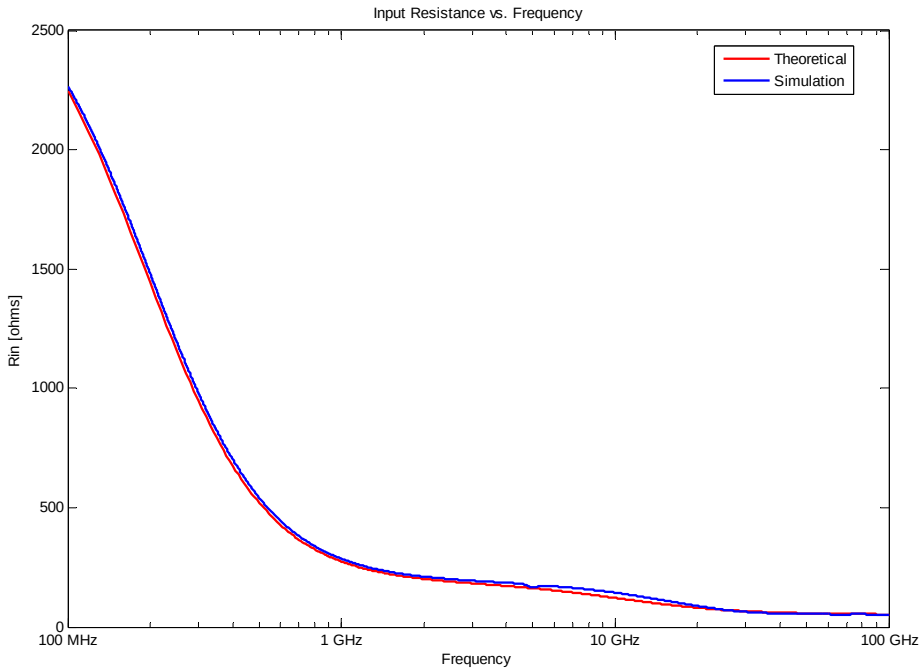

Figure 6: Input Resistance Rin vs. Frequency

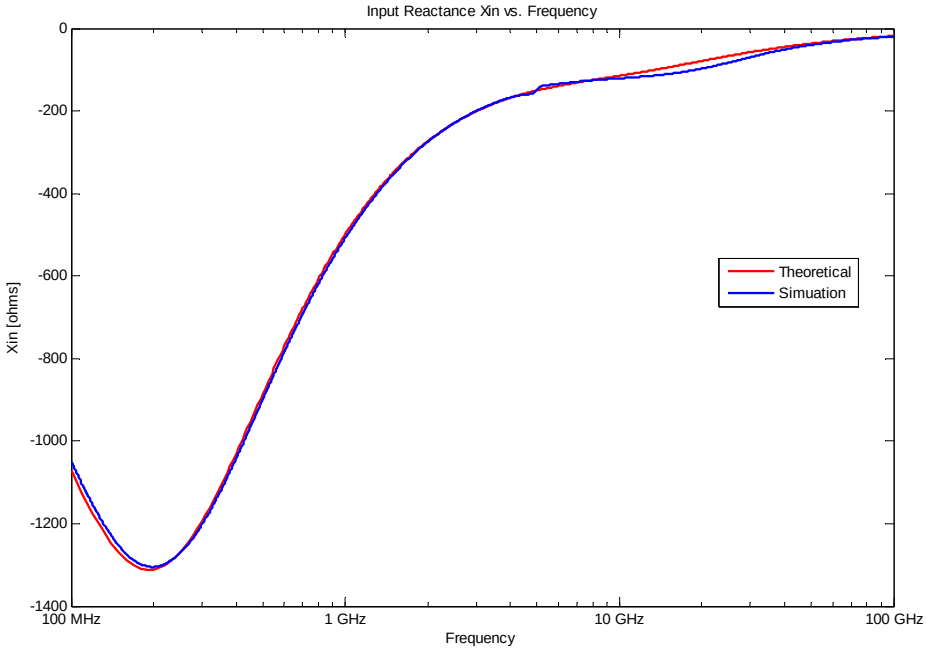

Figure 7: Input Reactance Xin vs. Frequency

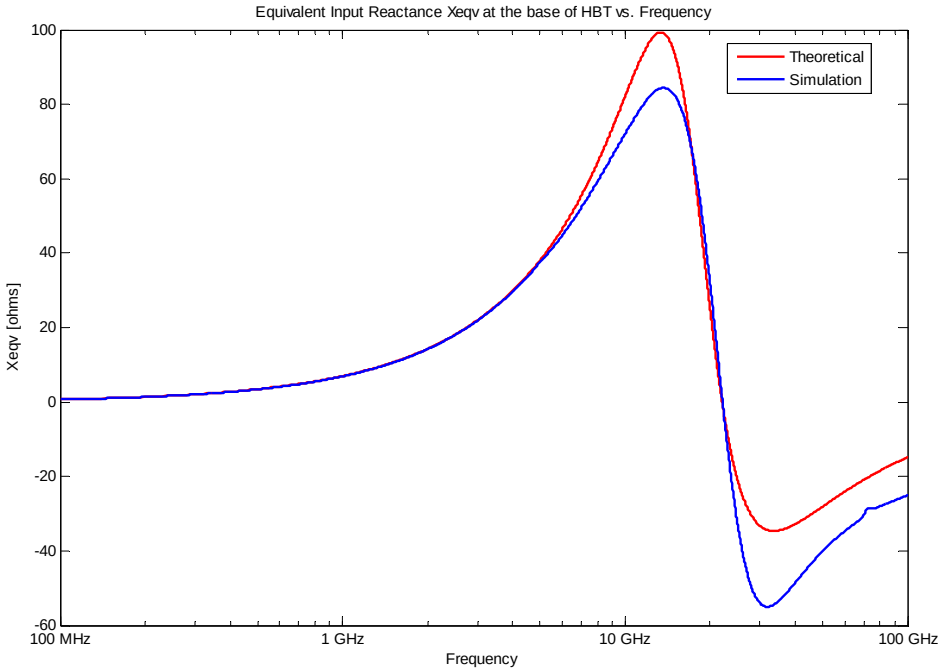

Figure 8: Equivalent Input Reactance Xeqv at the base of HBT vs. Frequency

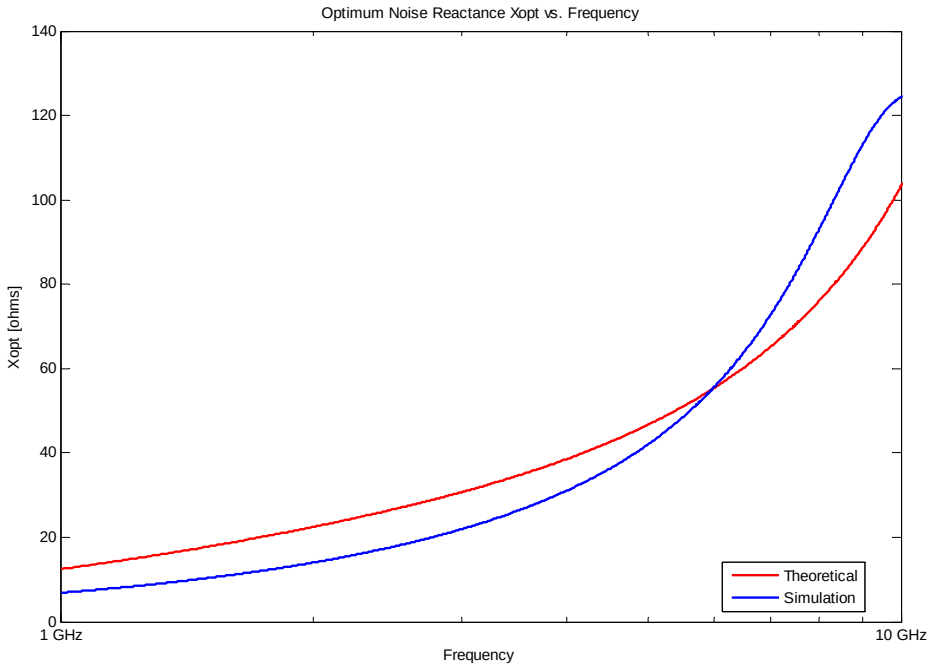

Figure 9: Optimum Noise Reactance Xopt vs. Frequency

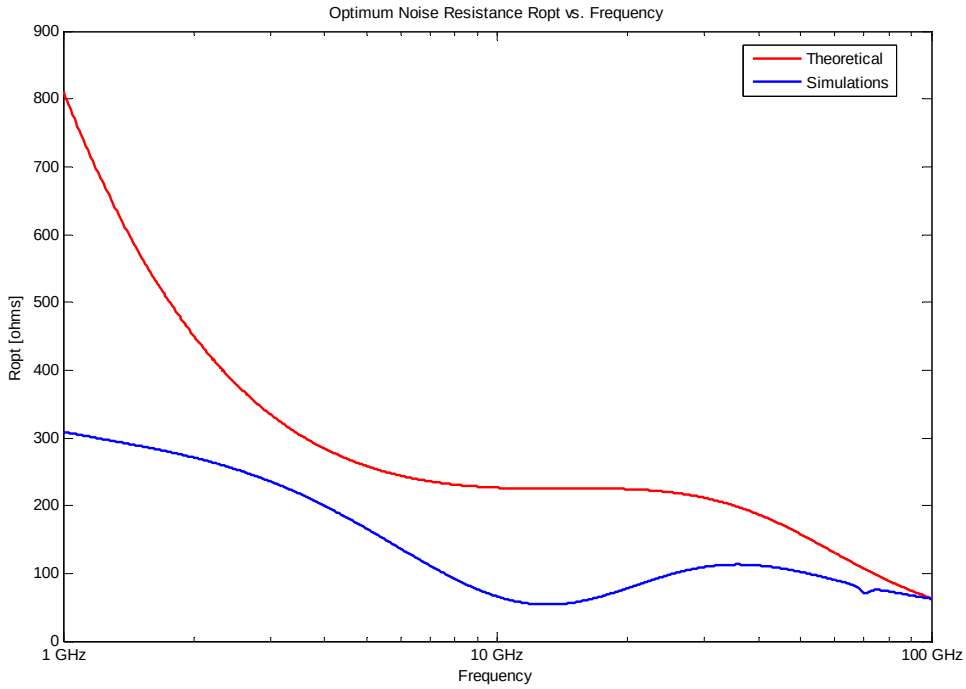

Figure 10: Optimum Noise Resistance Ropt vs. Frequency

Before analyzing the graphs, it should be mentioned, how the various circuit parameters have been determined. The base resistance r_b and the transconductance value of the HBT device g_m are taken from the DC Operation Point (OP) Analysis. L_e and L_c have the values that are going to be used in the design section of next chapter. r_π is calculated using (2.17) where β is taken again from DC OP Analysis. The capacitances are not the same as the values that DC OP Analysis produced. Since the small signal model employed in the analysis is much simpler than the VBIC model used by the simulator, the graphs of the input impedance looking into the base of the HBT are taken and the capacitance values are chosen such that there is a fit with the input impedance curves resulting from the theoretical analysis and the simulation graphs. A summary of these component values are provided in Table 1.

Table 1: Component values used to compare the theoretical results with the simulation outcomes

r_π	$C'_\pi = C_\pi + C_{ex}$	C_μ	L_e	L_c	g_m	r_b
2800 Ω	290 fF	65 fF	750 pH	1.08 nH	0.09S	5 Ω

The graphs give good correspondence except the case of R_{OPT}. Especially, at low frequencies the difference is getting bigger. The reason for this discrepancy is mainly associated with the simplicity of the used small signal model and the approximations which have been done during the analysis. However, the trend in GHz level is anticipated correctly and an approximate and relatively compact equation for R_{OPT} has been derived. In any case, the basic intent with the theoretical analysis is to get a baseline from which the design procedure can be developed. This baseline can be observed clearly in the next chapter.

CHAPTER 3

3 DESIGN PROCEDURE FOR TUNABLE LOW NOISE AMPLIFIERS

After the necessary noise analysis has been performed, now the design stage should take place. Before beginning with the novel approach that has been adopted in this thesis, it is appropriate to look at the general concepts in low noise design.

3.1 CONCEPTS IN LOW NOISE DESIGN

It has been briefly explained in the introduction part, the design of low noise amplifiers plays an important role in the general characteristics of the receiver. As the first component after the antenna where the communication signal has been captured, the low noise amplifier should augment very small amount of noise and possess a high gain. The reason of these choices can be based up on the two port noise theory as well. In section 2.4, expressions for the optimum source conductance and susceptance for noise as well as the minimum noise expressions have been derived. These equations apply well to the single stage systems however for complex electronic structures which consist of multi stages, the noise figure is computed by incorporating all contributions of individual stages. The equation that yields the noise factor for such systems can be provided subsequently:

$$F = F_1 + \frac{F_2 - 1}{G_1^2} + \frac{F_3 - 1}{G_1^2 G_2^2} + \frac{F_4 - 1}{G_1^2 G_2^2 G_3^2} \ldots = F_1 + \sum_{2}^{N} \frac{F_j - 1}{\prod_{1}^{N-1} G_j^2} \qquad (3.1)$$

(3.1) reveals the important knowledge that should be kept throughout the design process: The noise factor of the first stage directly determines the total noise factor of the whole receiver structure. On the other hand, the contributions of subsequent stages are scaled down by the square of the voltage gain of the components before the particular stage. It should be observed that the gain of the first stage repeats itself in the denominator so that the low noise amplifier has to yield not only a minimum possible noise figure but at the same time a respectable gain.

In that sense, the problem includes 3 different sets of impedance values and their relations with each other. The first set is comprised by the port impedance composed of real R_S and imaginary X_S. Traditionally, R_S is set to 50 Ω and X_S is chosen as 0. The next set encompasses the input impedance values looking from the base of the transistor. The input impedance has two distinct components as real (R_{in}) and imaginary (X_{in}), which are evaluated by the Thevenin equivalent impedance when looked at the base of the HBT into the device. The final set is constituted by the optimum noise resistance (R_{OPT}) and reactance (X_{OPT}) of the device which are also evaluated at the base of the HBT. Previously, the optimum noise conductance and susceptance values have been derived. The relation can be established quickly by (3.2) and (3.3).

$$R_{OPT} = \frac{1}{G_{OPT}} \tag{3.2}$$

$$X_{OPT} = \frac{1}{B_{OPT}} \tag{3.3}$$

After mentioning these important quantities, it would be appropriate to set their relations with each other. The first conditions are provided by the minimum noise figure

requirements which can be ensured by the port impedance equal to the optimum noise impedance:

$$R_S = R_{OPT} \tag{3.4}$$

$$X_S = X_{S,OPT} = -X_{OPT} \tag{3.5}$$

The second requirement imposes that the maximum gain should be taken out of the low noise amplifier. This situation is only possible when the input impedance of the amplifier can be matched to the port impedance. In that case, the following mathematical formulation can be performed:

$$R_S = R_{in} \tag{3.6}$$

$$X_S = -X_{in} \tag{3.7}$$

It should be noted why (3.7) differs from (3.5) in terms of sign. As can be realized quickly, the former one builds a relationship between the proposed values for the same quantity which is the source impedance. However, in the latter one, two distinct quantities are set equal by means of a matching network. To achieve the maximum power transfer that in turn guarantees the acquisition of the maximum gain, (3.6) and (3.7) should hold simultaneously by the introduction of a suitable matching topology. This type of matching is also called conjugate matching.

The four conditions characterized above can be summarized by two equations:

$$R_S = R_{OPT} = R_{in} \tag{3.8}$$

$$X_S = -X_{OPT} = -X_{in} \tag{3.9}$$

In case of any mismatches which result due to several design variables, it is possible to quantify the error by using appropriate formulations. If there is a discrepancy between the actual source admittance values G_S and B_S and optimum source noise admittance values $G_{S,OPT}$ and $B_{S,OPT}$, the difference can be reflected to the noise figure via (3.10):

$$F = F_{\min} + \frac{R_n}{G_S}\left[\left(G_S - G_{S,OPT}\right)^2 + \left(B_S - B_{S,OPT}\right)^2\right] \qquad (3.10)$$

Here, R_n is the equivalent noise resistance of the device which can be given as in (3.11):

$$R_n = C_{A,11} \qquad (3.11)$$

Similarly, the success in input and output matching can be determined based on the scattering (S) parameters of the matching network. For this purpose, input and output return loss is used as a metric [14].

$$RL_{in} = 20\log_{10}\left(\left|S_{11}\right|\right) \qquad (3.12)$$

$$RL_{out} = 20\log_{10}\left(\left|S_{22}\right|\right) \qquad (3.13)$$

Generally, it is acceptable to satisfy the input and output matching condition by acquiring an input return loss below -10 dB from the designed matching network.

The concerns mentioned above about the low noise amplifiers are also valid for the bandwidth requirements. In the current design technologies, low noise amplifiers are tuned up to a certain frequency, thus, the circuit operates actually at a narrow band. In that way, superior results can be acquired for particular frequencies. Nevertheless, many applications need to be utilized for a certain bandwidth which is much higher than a single frequency and the associated narrow band. For this case, there exist a variety of solutions such as the

wideband amplifier design techniques by using the noise cancellation topologies or low quality factor (Q) matching networks so that the matching is deliberately deteriorated in return of more bandwidth. Alternatively, the problem can also be handled by producing a plethora of different LNAs each of which is operating at neighboring frequencies. This solution idea requires more devices and the necessary electrical components that increase the dissipated power in the receiver. This work investigates the possibility of using tunable matching networks by introducing variable reactive components such as tunable capacitors so that the designed low noise amplifier can be tuned to different frequencies with the help of these special components by preserving the original noise figure and the gain characteristics.

Before passing to the different ideas on low noise amplifier design methodologies, one other important parameter is the linearity. The concept of linearity indicates to the fact that the input and output should be related to each other via the constant gain that is determined by the topology. However, as the transistor is a device with a non-linear character, this relationship is getting disturbed and critical problems that will degrade the performance of the low noise amplifiers significantly. Generally, these cases include when a strong signal interferes with a desired weak signal so that the weak signal gets lost like in the case of blocking or a transfer of modulation between signals takes place that is called the cross-modulation [5]. The design methodologies that will be discussed in this chapter do not target the linearity directly; however, each of them strives to get a better value of it.

3.2 REVIEW OF DIFFERENT DESIGN PROCEDURES

In this section, a general review of previous work about different design methodologies will be given. The aim is basically is to show how distinct strategies manage to get the desired results and the contribution of this thesis has come about.

3.2.1 Design Procedure of Voinigescu

Voinigescu et al. prepared an extensive analysis of HBT noise models and presented it in 1997 [15]. The model basically includes each noise source in the device that is described before, in Chapter 2. The authors have also suggested that the transistor noise parameters can be extracted via the Y-parameter measurements of the HBT instead of on-wafer noise measurements. After validating their anticipations through their proposed model by successive simulations and measurements, they come up with expressions for R_{OPT}, $X_{S,OPT}$, R_n, and F_{min}. By using these expressions, a design procedure has been derived.

The first step to do is to find the optimum current density J_C which will result in the minimum noise figure. After setting the necessary DC voltages tuned for the desired current density, they inquired how to fulfill the condition of equalizing the R_{OPT} to the port resistance. Based on their expectations from the expression of R_{OPT} they anticipated that the the emitter length of the HBT may help adjusting the optimum noise resistance to the conventional port resistance of 50 Ω. Afterwards, they proposed that the inclusion of an emitter inductance L_e would be changing the value of $X_{S,OPT}$ even though R_{OPT} continues to stay at the same value. Furthermore, according to their view-point L_e also enables the designer to change the value of the input impedance. This fact can be easily verified by the

formulation of basic circuit laws. One key assumption at this point is that not only $X_{S,OPT}$ and X_{in} have been given as their complex conjugates but also their behavior for the addition of the emitter inductance L_e has been forecasted to be identical. These ideas were based on the characteristics of HBT and FET devices. At the final stage of the design a series inductor is inserted to the base of the transistor device so that all the reactance can be resonated out, or more scientifically the condition of $-X_{in}=X_{S,OPT}=X_S$ can be satisfied.

Throughout the formulation of the design procedure, all reactive components are thought to be ideal, i.e. they are fully lossless. They have also provided 4 distinct design examples where the operation frequency varies from 1.9 GHz to 5.8 GHz by using 0.5 μm SiGe HBT transistors. As key observations to be made, the first issue would be the unity-gain frequency f_T of the devices. This quantity basically determines G_{OPT} and $B_{S,OPT}$ in their expressions and its value changes between 10 and 20 GHz. Thus, the operation frequencies are actually a substantial percent of varying 10 to 30 of the unity-gain frequency. In today's technology, even though the operating frequencies have stayed the same, f_T values scaled up significantly. Nevertheless, for that time, they were able to come up with inductor values ranging from 500 pH to 2.3 nH all of which can be produced as on-chip inductors. Moreover, input matching was very successful, resulting in S_{11} values less than -30 dB, and the discrepancy between the actual noise figure of the LNA and the minimum noise figure is negligible. The gains of the low noise amplifiers are also satisfactory changing between 10 and 15 dB. Finally, they assured that finite quality factor (Q) inductors as opposed to ideal counterparts, i.e. infinite Q components, would not change the validity of the design flow.

3.2.2 Design Procedure of Schaeffer and Lee

Schaeffer and Lee based their work on 0.6 μm CMOS process with a supply voltage of 1.5 V [16]. In this design procedure, one more important concept which is the consumed power by the amplifier has been added to the already existing design parameters.

First of all, they introduced a valid noise model for the MOS transistor. Subsequently, they derived an expression for the minimum noise figure which incorporates a constant power P_D and the biasing as well as the device parameters. The biasing is provided by the overdrive voltage that is a specific term for MOS transistor to characterize the difference between the gate-source potential and the threshold voltage ($V_{OV}= V_{GS}-V_T$). To get the minimum noise figure, the derivative of the derived expression has been taken and set to zero. This produced a design value for the overdrive voltage. Furthermore, the limitation on the power dissipation has been quantified by another expression which includes the width of the transistor (W), the overdrive voltage V_{OV}, the oxide capacitance C_{ox} and some other MOSFET parameters. Since the overdrive voltage has been already computed, they achieved to yield a value for the transistor width W. With the acquired value of the overdrive voltage and the predetermined constant power, it is possible to bear up a quality factor for the input matching network. Like in the work of Voinigescu, Schaeffer and Lee also introduced inductive degeneration at the source of their MOS device and a series inductor in the gate, for matching purposes. However, the aim was different in the sense that Scheffer and Lee did not use the matching network to match the port impedance to the optimum noise impedance values. Thus, they found a minimum noise figure for the particular constraint they imposed in

the beginning of the design such as the power. As they also mentioned, the noise figure they come up with is not equal to the minimum noise figure of the device.

They demonstrated their design by an LNA which has a gain of 22 dB and total power dissipation of 7.5 mW (the main amplifier excluding the buffer composed of a source follower). A significant problem with their design was the series gate inductance which cannot be implemented as an on-chip inductor and thus, it was tuned with an off-chip matching network to the desired value.

3.2.3 Design Procedures by Andreani and Nguyen

In this part, two different papers with a related design procedure concept will be discussed. The basic target of both papers is to unify the two design procedures explained in previous sections.

The basic problem of simultaneous input and noise match can be observed when the device sizes are decreased, the dissipated power is restricted to a low value or the frequency of operation is reduced [17]. In these cases, the authors have observed for CMOS devices the real part of the optimum noise impedance gets bigger than the real part of the input impedance for the specific source inductance values. To reconcile these two quantities, one has to boost the source inductance value, for which the minimum noise figure is deteriorated. It can also be understood, the technique developed by Schaeffer and Lee investigate one of these particular situations, i.e. a low level constant power, thus reaching an optimum noise figure which is plausibly higher than the minimum noise figure.

To alleviate that Nguyen et al. referred to a solution proposed earlier by Andreani [18]. Andreani suggested that adding a shunt capacitance between the gate and the source

would decouple the quality factor of the matching circuit from the gate to source capacitance C_{GS} so that a reduction in the noise figure can be enabled. Following this idea, Nguyen et al. added a shunt capacitance across the gate-source junction which made it possible to reduce the values of the source inductance required to make real input impedance equal to the real port impedance.

If these ideas are summed up, their philosophy of design can be rephrased as follows: First they selected a suitable value for the bias voltage that will result in a drain current creating the minimum noise figure. Afterwards, the width is determined by the power requirement as Schaffer and Lee projected. Then, two separate conditions which are the equality of the port resistance to the input resistance and the equality of the port resistance to the optimum noise resistance are fulfilled by selecting suitable values for the inductive degeneration at the source of the transistor L_s and the extra capacitance added to the gate-source junction C_{ex}. Imaginary parts of the input impedance and optimum noise impedance are shown to be approximately the same and they can be resonated out by the matching network of a series inductor at the gate.

Nguyen et al. built also a demonstrative amplifier of 0.25 μm CMOS technology by applying their design strategy. The value of the series inductor and the load inductor at the drains of the transistors in the folded cascode structure are about 33 nH which has been implemented with the off-chip inductors. These components enhance the values of the noise figure and the linearity of the designed structure. So, they were able to come up with an amplifier operating at 900 MHz which has decent outcomes for the noise figure, S_{11} value and the power gain.

3.2.4 Recent Approaches

In this last section of the review of existing design methodologies, two recent approaches will be discussed. The first one considers HBT LNA design with the technology of IBM 0.12 μm SiGe HBT. It actually aims to demonstrate a problem where X_{OPT} and X_{in} do not come out to be the same for the same emitter inductance when the operating frequency is increased to Ka-Band (corresponding to 35 GHz) [19]. For elevated frequencies, it is obvious that the effect of the base-collector junction capacitance C_μ dominates in the transfer functions of the noise sources while their contribution to the input referred noise is computed. Min tries to demonstrate with the help of Miller Theorem that C_μ can be partitioned into two capacitances. The part of C_μ that is reflected back to the input has both real and imaginary components, which means that it also produces a conductance changing the values of real input impedance. Thus, it is concluded that for the value of emitter inductance that makes the real input impedance equal to the real optimum noise impedance does not guarantee anymore the simultaneous match of noise and input power since X_{OPT} differs for that value from X_{in}. An optimization is required to reach a balance with the minimum noise figure and the input match, which is exemplified by a LNA in the paper.

The other approach is developed via the 0.13 μm CMOS technology. The authors warn the readers about three emerging problems related with the design methodologies described in 3.1.1, 3.1.2, and 3.1.3 [20]. The first one is the simplified input impedance expression that does not take into effect the parasitic feedback capacitance C_{GD}, equivalent of C_μ in MOS technology. The second issue is the same topic discussed in Min's paper, namely the differences in X_{OPT} and X_{in}. Finally, the last concern comes from the finite quality factor

of the inductors that are utilized in the low noise amplifier structures. They indicate that the series resistances introduced by the low Q passive components can alter the overall performance significantly. By considering these warnings, they developed a design procedure which closely resembles to other existing methods. The only difference comes from the fact that the width is again chosen for the minimum noise figure like in the way of Voinigescu, and then they tried to match Z_{in} to $Z^*_{S,OPT}$ with a source inductance and an external capacitance added in parallel with the gate-source junction. Finally, with help of a matching network which is composed of not only a single series inductor but also a shunt capacitor to the ground at the gate, they managed to realize $Z^*_{in}= Z_S$. A concrete, algorithmic set of design steps have not been provided. All results are produced by means of successive simulations. However, the contributions of series resistances introduced by the nonideal on-chip inductors have been well quantified. It turns out that the gate inductance deteriorates the noise figure at most, as can be imagined easily.

3.3 THE PROPOSED TOPOLOGY AND DESIGN ESSENTIALS

After completing the review of several different design procedures which are already existing and used in practice, now, the basic design structure that is going to be analyzed in this thesis will be presented. Subsequently, the algorithmic design steps are provided on a theoretical basis. The design steps will be validated and demonstrated by many simulations.

3.3.1 Design Topology

Figure 11 shows the basic structure of the designed circuit. The choices that lead to this topology originate mainly from the fact that the amplifier should be tunable.

A cascode structure has been chosen for the low noise amplifier. For the single stage amplifiers, an inherent problem is the interaction with the input and output port. This leads to a complicated matching problem where not only constraints related to the power and noise matching for the input but also the contributions of the output load should be considered. This makes the problem very difficult to outline on a theoretical basis, thus an easy map for design cannot be provided. With the introduction of the cascode structure, the isolation between the input and output of the amplifier can be accomplished to a large extent.

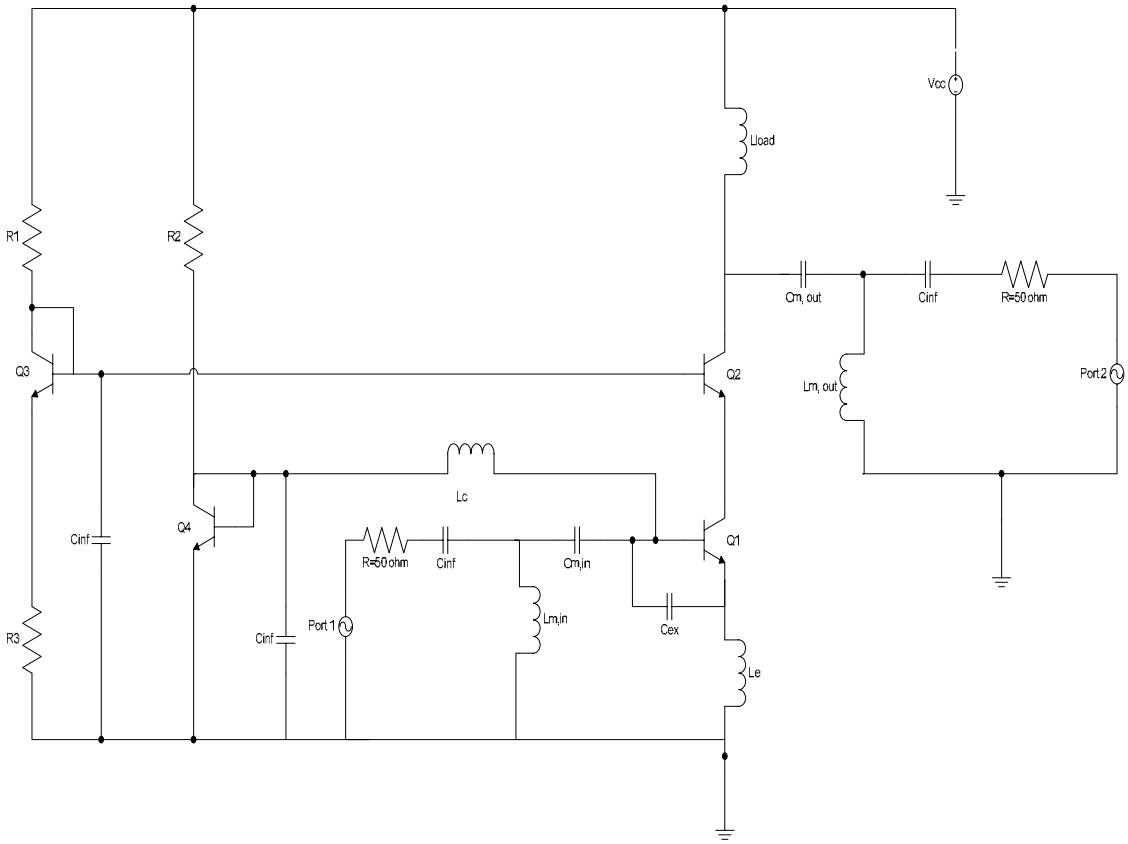

Figure 11: The designed circuit topology

All passive components except L_{load} have been assumed ideal. The reason is basically to verify the validity of the design procedure. It should also be considered that all other

design procedures demonstrated their initial work via ideal passive elements. L_{load} is not a part of the matching network in the total structure thus it has been realistically designed like the resistors in the bias circuitry. At the end of this section, one design example will be implemented via non-ideal passive elements.

The emitter lengths of the transistors in the cascode topology have been an important part of the design procedures in the literature, as summarized in previous sections. The basic aim was to either equalize R_{OPT} to port resistance R_S or to meet a certain power constraint P_D. In this work, R_{OPT} is made the same as R_{in} and then with the help of the matching network converted to R_S. There was also not a power constraint aimed. Moreover, the aim in this procedure is to establish techniques for tunable amplifiers. After fabrication steps, the width of the transistors are finalized, thus, they cannot be a part of the variable structures in the circuit. They will be kept the same for all frequencies. Past research has shown that the change in the emitter length does not create large changes in F_{min} [15]. However, a slight decrease can be observed with large emitter lengths.

The bias network for the amplifier has been established by two distinct potentials at the bases of the two transistors constituting the cascode. The bias circuits are brought to be immune to the noise by the addition of large capacitors at the bases of the transistors providing the DC current for the cascode. As other design methodologies suggested an emitter inductor L_e has been added to the design. Inductive source degeneration helps to change the input resistance significantly and makes it possible to bring the input resistance and optimum noise resistance to the same values as will be discussed in design steps more detailed. Furthermore, as some other procedures suggested, an extra capacitance C_{ex} has been

inserted to the base-emitter junction [17], [18]. L_e and C_{ex} together guarantee that the input resistance R_{in} can be made equal to the optimum noise resistance R_{OPT}.

The bias to the common emitter transistor of the cascode is transferred via the inductor L_c. This inductor is also part of the matching structure of the low noise amplifier which includes a high-pass L network as well. L_C is used to provide the necessary equality between the optimum noise reactance X_{OPT} and X_{eqv}, the total input reactance with the inclusion of L_c. This L network and the bias inductor build together a three element π-network that is used as a whole to match the port resistance R_S to R_{OPT} and R_{in}. Compared to the matching alternative via a single base inductance, this choice significantly reduces the employed inductor values and makes it possible to use high quality on-chip inductors instead of problematic off-chip alternatives. Finally, the output matching structure is built again by a high pass L-type matching network.

3.3.2 Design Steps

Even though the topology is meant to work at several different frequencies, for each frequency, a single method of design should be applied so that it can be called a design procedure. In this section, the design steps that build together the design procedure are going to be algorithmically explained.

Step 1:

Step 1 basically requires the biasing of the cascode structure such that the current density for the minimum noise figure can be determined. The voltage source that will feed Q_1 in Figure 4, has more importance since the characteristics of the minimum noise figure are basically determined by Q_1. For the case of Q_2, conventionally, a diode connected transistor

is utilized so that the biasing problem can be solved automatically where the bias potential becomes the supply voltage V_{CC}. During the design process of this thesis, it has been observed, that this particular choice results in higher emitter inductance values required for $R_{OPT}=R_{in}$. A DC sweep of the voltage at Q_2 indicates that a close value to V_{CC} may significantly reduce the necessary emitter inductance value for the constraint mentioned above, resulting in a very slight increase in the minimum noise figure (around 20 mdB). Considering the integrability issues of the emitter inductance which should be of on-chip type with a low quality factor, a second bias network has been established that will supply a lower voltage than V_{CC}.

Step 2:

After the biasing voltages have been decided, the main aim is to equalize the real part of the input impedance, R_{in} to the real part of the optimum noise impedance R_{OPT}. This can be achieved by the usage of the emitter inductor L_e. In this analysis it is going to be assumed that R_{OPT} is nearly independent of the emitter inductance. This can be shown both by theory and by simulations for small values of emitter inductance [15]. However, as L_e exceeds 1 nH, R_{OPT} rises linearly with the emitter inductance and thus the problems mentioned in the paper of Nguyen et al. are realized.

Now, first of all, the normalized chain matrix elements are computed under the condition stated above. For (3.14)-(3.16), it has been assumed that the effect of C_μ can be neglected and L_e is assumed to be in the range where it does not affect the shape of R_{OPT}. Finally, $\omega r_\pi C_\pi$ is taken to be much greater than 1:

$$C_{A_{11}} \approx r_b + \frac{g_m}{2g_m^2} = r_b + \frac{1}{2g_m} \tag{3.14}$$

$$C_{A_{22}} \approx \left\{ \left\{ \frac{\left(\frac{1}{r_\pi}\right)^2 + \left[\omega\left(C_\pi + C_\mu\right)\right]^2}{g_m^2} \right\} \left(\frac{g_m}{2}\right) \right\} = \frac{\left(\frac{1}{r_\pi}\right)^2 + \omega^2\left(C_\pi + C_\mu\right)^2}{2g_m} \tag{3.15}$$

$$\mathrm{Im}\left(C_{A,12}\right) \approx \mathrm{Im}\left\{ \frac{g_m}{2g_m^2} \left[\left(\frac{1}{r_\pi}\right) - j\omega\left(C_\mu + C_\pi\right) \right] \right\} = -\frac{\omega\left(C_\mu + C_\pi\right)}{2g_m} \tag{3.16}$$

The quantities calculated above should now be put in the associated formulas to yield the noise parameters, G_{OPT} and R_{OPT}.

$$G_{opt} = \sqrt{\frac{C_{A,22}}{C_{A,11}} - \left[\frac{\mathrm{Im}(C_{A,12})}{C_{A,11}}\right]^2} \approx \sqrt{\frac{\left[\left(\frac{1}{r_\pi}\right)^2 + \omega^2\left(C_\pi + C_\mu\right)^2\right]\left(\frac{r_b}{2g_m} + \frac{1}{\left(2g_m\right)^2}\right) - \frac{\omega^2\left(C_\mu + C_\pi\right)^2}{\left(2g_m\right)^2}}{\left(r_b + \frac{1}{2g_m}\right)^2}} \tag{3.17}$$

$$G_{opt} \approx \sqrt{\frac{\left(\frac{1}{r_\pi}\right)^2\left(r_b + \frac{1}{2g_m}\right) + \frac{\omega^2\left(C_\pi + C_\mu\right)^2 r_b}{2g_m}}{\left(r_b + \frac{1}{2g_m}\right)^2}} \approx \frac{\sqrt{\frac{\omega^2\left(C_\pi + C_\mu\right)^2 r_b}{2g_m}}}{\left(r_b + \frac{1}{2g_m}\right)} \tag{3.18}$$

$$R_{OPT} = \frac{1}{G_{opt}} = \frac{\left(r_b + \frac{1}{2g_m}\right)}{\sqrt{\frac{\omega^2\left(C_\pi + C_\mu\right)^2 r_b}{2g_m}}} = \frac{g_m\left(r_b + \frac{1}{2g_m}\right)}{\omega\left(C_\pi + C_\mu\right)\sqrt{\frac{g_m r_b}{2}}} \tag{3.19}$$

Similarly, one can take the input resistance and simplify it in an analogous manner:

$$R_{in} \approx \frac{\left[r_\pi + \omega^2 r_\pi^2 L_e C_\pi g_m\right]}{\omega^2 r_\pi^2 C_\pi^2} \approx \frac{g_m}{C_\pi} L_e \tag{3.20}$$

Now, setting (3.19) and (3.20) equal will yield a crude value for L_e:

$$\frac{g_m}{C_\pi} L_e = \frac{g_m \left(r_b + \frac{1}{2g_m} \right)}{\omega \left(C_\pi + C_\mu \right) \sqrt{\frac{g_m r_b}{2}}} \tag{3.21}$$

$$L_e \approx \frac{\left(r_b + \frac{1}{2g_m} \right)}{\omega \sqrt{\frac{g_m r_b}{2}}} \tag{3.22}$$

(3.22) gives a basic relation to find the emitter inductance that will make the optimum noise resistance R_{OPT} equal to the input resistance R_{in}. This formula has been derived as a result of many approximations, thus, the simulated values for L_e tend to be bigger than the theoretical value. Also, the relation suggests that with decreasing frequency the emitter inductance should increase, which is undesirable since high L_e values degrade the noise figure and reduce the power gain significantly. As a remedy to both of these effects, Andreani and Nguyen suggested to use an extra base-emitter capacitor C_{ex}. C_{ex} increases the effect of the decoupling the quality factor of the matching network from the base-emitter capacitance C_π . This helps to reduce the value of the emitter inductance. So, the realization of R_{OPT} and R_{in} equality depends on the appropriate choices of L_e and C_{ex}.

Step 3:

As it has been discussed in previous sections, many design procedures claimed that X_{in} becomes automatically the same as X_{OPT} for the value of L_e that makes R_S equal to R_{OPT} and $R_{in,}$ however, recent studies suggested that this can diverge from the actual practice when different parameters such as C_μ comes into play. In this thesis, to solve the problem from

another point of view, a shunt inductor, L_c has been suggested that will at the same time carry the bias voltage. This shunt inductor does not change the value of the R_{OPT} but it constitutes a π-network with the remaining reactive components, to match R_{OPT} and R_{in} to the real part of the port impedance, R_S.

To assert the theoretical background for this action, one has to consider X_{in} and X_{OPT}. If the expression for X_{OPT} with L_c investigated, some further approximations can be done. One of them is to neglect the terms containing C_μ. Although, this simplification will cause problems in design calculations above 10 GHz, it is necessary to form a baseline to continue with the computation of the design variables. The expressions for normalized chain matrix elements in Appendix C can be modified to yield:

$$\mathrm{Im}\left(C_{A,12}\right)=\frac{1}{2g_m}\left\{\left(\frac{1}{r_\pi}+\left(\frac{L_e}{L_c}\right)g_m\right)\omega L_e g_m-\left[\omega C_\pi\left(1+\frac{L_e}{L_c}\right)-\frac{1}{\omega L_c}\right]\left(1-\omega^2 C_\pi L_e\right)\right\} \qquad (3.23)$$

Then, one can further assume $\omega^2 L_e C_\pi << 1$, so that (3.23) becomes:

$$\mathrm{Im}\left(C_{A,12}\right)=\frac{1}{2g_m}\left\{\left(\frac{1}{r_\pi}+\left(\frac{L_e}{L_c}\right)g_m\right)\omega L_e g_m-\left[\omega C_\pi\left(1+\frac{L_e}{L_c}\right)-\frac{1}{\omega L_c}\right]\right\} \qquad (3.24)$$

Finally, by choosing a suitable value for L_c such that its impedance is much higher than the modified impedance of the the total base-emitter junction capacitance, one can arrive to (3.25).

$$\mathrm{Im}\left(C_{A,12}\right)=\frac{1}{2g_m}\left\{\left[\left(\frac{L_e}{L_c}\right)g_m\right]\omega L_e g_m-\left(-\frac{1}{\omega L_c}\right)\right\}=\frac{\left(1+g_m^2\omega^2 L_e^2\right)}{2g_m\omega L_c} \qquad (3.25)$$

If similar simplifications could be adopted for $C_{A,11}$ as well, (3.26) can be found.

$$C_{A,11} \approx r_b + \left[\frac{1+\left(\omega L_e g_m\right)^2}{g_m^2}\right]\frac{g_m}{2} = \frac{2g_m r_b + 1 + \left(\omega L_e g_m\right)^2}{2g_m} \tag{3.26}$$

Combining the outcomes of (3.25) and (3.26), it is possible to derive the expression depicted in (3.27) and (3.28).

$$B_{OPT} = -\frac{\mathrm{Im}\left(C_{A,12}\right)}{C_{A,11}} = \frac{\frac{1}{2g_m\omega L_c}\left(1+\omega^2 L_e^2 g_m^2\right)}{\frac{2g_m r_b + 1 + \left(\omega L_e g_m\right)^2}{2g_m}} \approx \frac{\frac{1}{2g_m\omega L_c}\left(\omega^2 L_e^2 g_m^2\right)}{\frac{1}{2g_m}\left(\omega L_e g_m\right)^2} = \frac{1}{\omega L_c} \tag{3.27}$$

$$X_{OPT} = \frac{1}{B_{OPT}} = \omega L_c \tag{3.28}$$

Correspondingly, one has to also analyze the input reactance of the amplifier. X_{in} will be modified with the inclusion of the bias inductor, so based on the expressions derived in Appendix C, (3.29) can be found. As it is done before, all terms including C_μ are neglected.

$$X_{in} \approx \frac{\left\{j\omega L_e\left[\left(1+g_m r_\pi + \omega^2 r_\pi^2 C_\pi^2\right)\right] - \omega C_\pi r_\pi^2\right\}}{\left(\omega^2 r_\pi^2 C_\pi^2\right)} \tag{3.29}$$

Furthermore, it can also be assumed that $\omega^2 r_\pi^2 C_\pi^2 >> 1 + g_m r_\pi$:

$$X_{in} \approx j\omega L_e - \frac{j}{\omega C_\pi} \approx -\frac{j}{\omega C_\pi} \tag{3.30}$$

At GHz frequency level, the second term of (3.30) dominates, and that's why, the input reactance is big. If one chooses L_C such that its impedance is much smaller than the input reactance, it can be shown like in Appendix B of this work:

$$X_{eqv} = \omega\left[\frac{L_c X_{in}\left(X_{in} + \omega L_c\right) + R_{in}^2 L_c}{R_{in}^2 + \left(X_{in} + \omega L_c\right)^2}\right] \approx \frac{\omega L_c\left(R_{in}^2 + X_{in}^2\right)}{R_{in}^2 + X_{in}^2} = \omega L_c \tag{3.31}$$

It is now clear that if the value of L_c can be carefully determined, one can guarantee to get the same imaginary components from the optimum noise impedance and the input impedance. After this step, by selecting proper values for the matching network, these imaginary components will be resonated out so that their contribution to the noise figure can be almost nullified.

Step 4:

One different approach in this work from the already existing procedures is the L-type network. Classically, a single series inductor has been added to the base of the HBT (or gate of the MOSFET) to realize the matching operation. The general aim for the matching is to cancel out the imaginary impedances.

In this work, a shunt inductor and a series capacitance has been chosen instead. The reason for this can be explained on the basis two different reasons. The first one is related with Step 3. As mentioned before, to form a π- network it is necessary to build a high pass L type matching structure. The second reason is the tunability of the low noise amplifier. By the experimentation for the tunability, it has been observed that a series capacitor can easily shift the noise figure curve to different frequencies. It should be remembered that a variable inductor is very difficult to construct. Most of the time, a variable inductor can be produced with the help of a series capacitor. So, this means that in any case, a variable series capacitor should be utilized to acquire a tunable matching structure. The idea is then to have just a single variable single capacitor, C_m. Thus, the third leg of the π- network becomes naturally a shunt inductor, L_m to the input port.

The matching structure in this thesis is assigned to have two distinct missions. The first one is to match the equalized R_{OPT} and R_{in} to the port resistance, R_S. The second duty is like in other methodologies, to resonate out the reactance at the base of the HBT device.

Analytically, the design of the matching network can be performed in several steps. For this purpose, Figure 12 should be considered. Here, all components except one is existing in the low noise amplifier circuit. R_h is, however, a hypothetical resistance and will be used for calculations only.

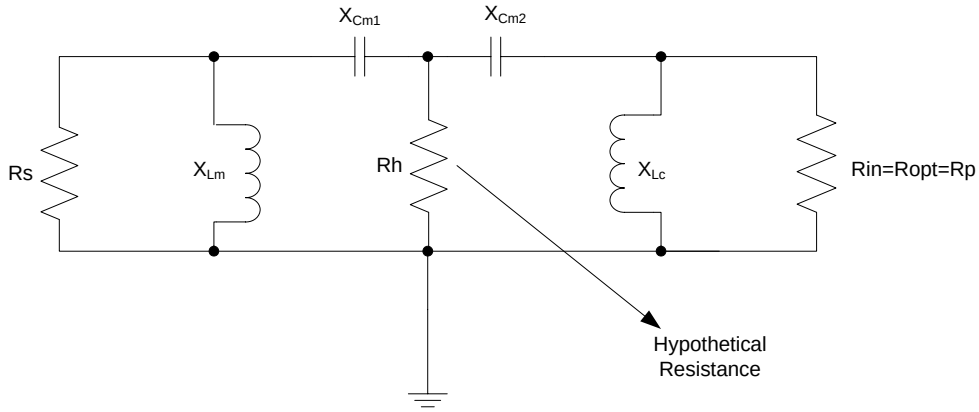

Figure 12: The small signal diagram of the matching network

One can start from the right end of the circuit since the values of R_{in} or R_{OPT} are known. By using the matching network theory, one can define the quality factor of the right-hand part, Q_R as in (3.32) [21].

$$Q_R = \frac{R_p}{X_{Lc}} = \frac{X_{Cm1}}{R_h} \qquad (3.32)$$

R_p is known. Also, since in Step 2, L_c has been chosen, so, X_{Lc} is found out. However, X_{Cm2} and R_h are not determined yet. To find them, another relationship specific to the matching theory can be utilized:

$$R_h = \frac{R_p}{Q_R^2 + 1} \tag{3.33}$$

When, (3.32) and (3.33) are used together, it is easy to find the required value of X_{Cm2}.

$$X_{Cm2} = Q_R R_h \tag{3.34}$$

Now, one can proceed with the left-hand part of the matching network. Using similar relations, it is possible to acquire the quality factor Q_L:

$$Q_L = \sqrt{\frac{R_s}{R_h} - 1} \tag{3.35}$$

$$X_{Cm1} = Q_L R_h \tag{3.36}$$

$$X_{Lm} = \frac{R_S}{Q_L} \tag{3.37}$$

It should be also noted that using a π-network ensures that the total reactance will be resonated out. The exact derivation of this fact is provided in Appendix D. This information clearly indicates the advantage of setting X_{OPT} and X_{eqv} equal to ωL_c.

Now, it is possible to find the remaining component values via simple relations:

$$C_m = \frac{1}{\omega\left(X_{Cm1} + X_{Cm2}\right)} \tag{3.38}$$

$$L_m = \frac{X_{Lm}}{\omega} \tag{3.39}$$

3.4 DESIGN EXAMPLE AT 5 GHZ

In this section, a design example at 5 GHz will be given to exemplify the steps described above. The technology that has been used is the IBM 0.18 µm Design Kit (7HP).

First of all, the emitter lengths are chosen as 19.2 µm for both of the transistors. The emitter widths are the same and 0.2 µm. Then, the optimum biasing voltages are computed. To do this, the common-emitter and the common-base transistors of the cascode topology are analyzed separately. Figure 13 shows the simulation result for the common emitter transistor. The value that results in the lowest minimum noise figure happened to be at 0.83 V. Also, considering the explanation given in Step 1, Q_2 is biased with a supply of 1.4 V.

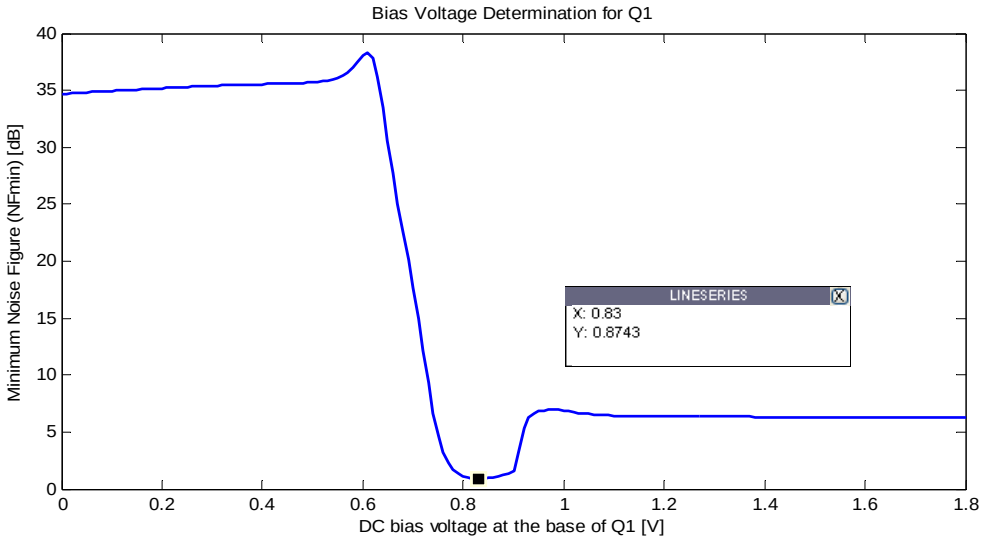

Figure 13: The plot for the bias voltage determination for Q1

Next, the design choices for L_e and C_{ex} should be made. In the previous section, a simple design formula has been derived to give an initial value for the design process.

$$L_e \approx \frac{\left(r_b + \frac{1}{2g_m}\right)}{\omega\sqrt{\frac{g_m r_b}{2}}} \approx \frac{(5+5.6)}{(2\pi)(5GHz)\left(\sqrt{0.225}\right)} = 710\,pH \qquad (3.40)$$

(3.40) poses a good starting point for the design of the L_e, however, throughout the simulations it has been observed that such an emitter inductance value is only possible if an extra base-emitter capacitance C_{ex} is added. So, the next step in design is to find the corresponding C_{ex} value that will justify the given L_e. A sweep of C_{ex} yields sufficient information to decide the necessary design parameter. A good fit can be reached for L_e= 750 pH with C_{ex}=120 fF. The resulting curves of R_{OPT} and R_{in} can be given as in Figure 14. It can be seen that R_{OPT} and R_{in} can be tuned to the value of around 160 Ω.

Subsequently, a suitable value for the bias inductor L_c is chosen. This can be done by looking at the associated analytic values of the X_{OPT} and X_{eqv}. Both predict approximately the same result of ωL_c, if this impedance is sufficiently small compared to X_{in}. It should be also mentioned that the choice for L_c will shape the matching network structure. In the design, an inductance of 1 nH has been set initially, however, after the construction of the bias circuits their values push this inductance to 1.08 nH. In Figure 15, both X_{OPT} and X_{eqv} have been drawn versus the frequency. As can be observed there is a small discrepancy between the two quantities, but this difference is negligible in terms of the net effect to the final results.

At this step, it should be appropriate to begin with the matching network design. From the previous design stages, it has been determined that $R_{OPT} \approx R_{in} \approx 160\ \Omega$. The imaginary parts can be determined from (3.41):

$$X_{OPT} \approx X_{in} \approx \omega L_c = (2\pi)(5GHz)(1.08nH) = 35\Omega \qquad (3.41)$$

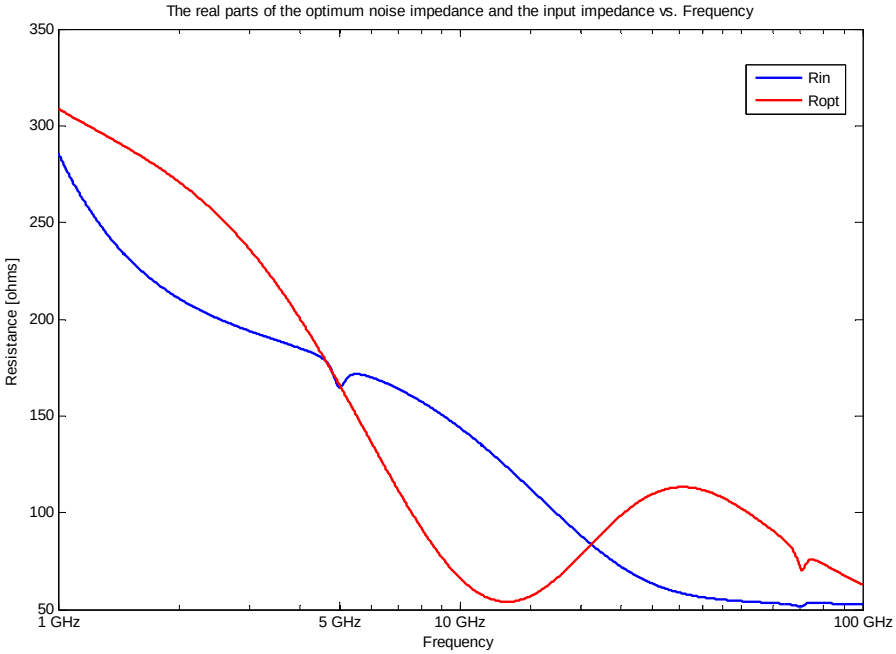

Figure 14: Ropt and Rin vs. Frequency

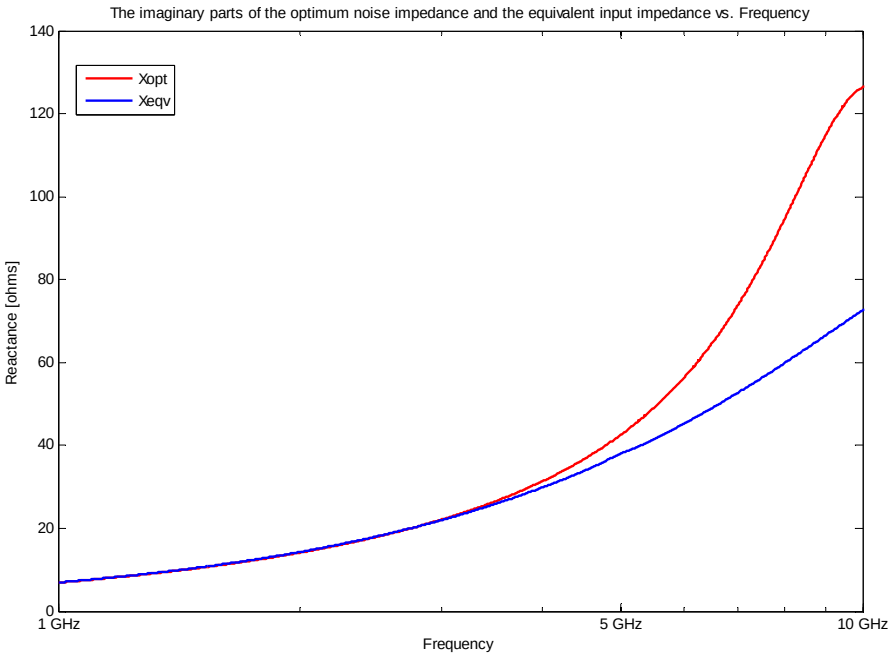

Figure 15: Xopt and Xeqv vs. Frequency

From this knowledge and utilizing the set of equations (3.32)-(3.39) one can derive the matching network components as follows:

$$Q_R = \frac{R_p}{X_{Lc}} = \frac{166}{35} \approx 4.74 \tag{3.42}$$

$$R_h = \frac{R_p}{Q_R^2 + 1} = \frac{166}{(4.74)^2 + 1} \approx 7.1\Omega \tag{3.43}$$

$$X_{Cm2} = Q_R R_h = (4.74)(7.1) = 33.7\Omega \tag{3.44}$$

$$Q_L = \sqrt{\frac{50}{7.1} - 1} = 2.46 \tag{3.45}$$

$$X_{Cm1} = (2.46)(7.1) = 17.5\Omega \tag{3.46}$$

$$X_{Lm} = \frac{50}{2.46} = 20.3\Omega \tag{3.47}$$

$$C_m = \frac{1}{\omega(X_{Cm1} + X_{Cm2})} = \frac{1}{(2\pi)(5GHz)(17.5 + 33.7)} = 622\,fF \tag{3.48}$$

$$L_m = \frac{X_{Lm}}{\omega} = \frac{20.3}{(2\pi)(5GHz)} = 646\,pH \tag{3.49}$$

These values provide an accurate baseline for the design of the matching network. After several simulations, C_m has been optimized to 560 fF and the L_m has been finalized with the value of 670 pH.

In a similar manner, the output matching network has been constructed with the values for $L_{m,o}$=290 pH and $C_{m,o}$=757 fF. As stated before, L_{load} is realistically designed as a spiral inductor with a value of 1 nH.

After these design steps, the biasing network should be built. For this purpose, two more HBT transistors with the same emitter lengths have been made use of. Three resistors from the design kit with the values 134 Ω, 190 Ω, and 365 Ω are chosen for this purpose. Two capacitors each 100 pF are set at the bases of the bias circuit transistors to the ground in order to eliminate the associated noise. By carrying out the final simulations, NF and NF_{min}, the gain, and the input and output matching can be shown as in Figure 16 to Figure 18.

Before concluding this section, the total power dissipation of the design should be discussed. The current that flows over the 1.8 V power supply is 8.15 mA, giving a total power of 14.67 mW power. This is a reasonable power content, however with the addition of the realistic components, due to the additional losses at the parasitic series resistances of the passive components, further increase in the total dissipated power should be expected.

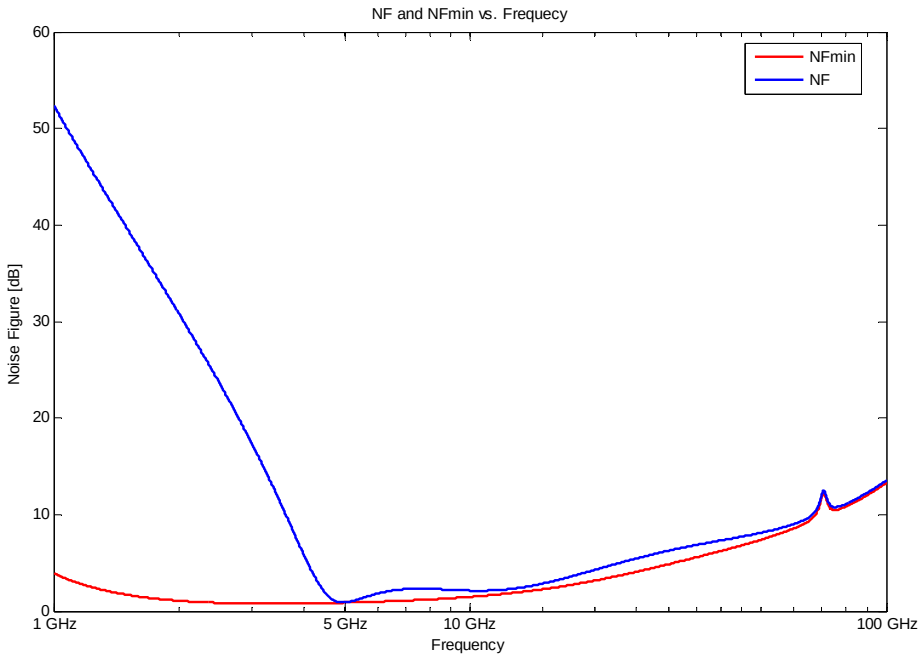

Figure 16: NF and NF_{min} vs. Frequency

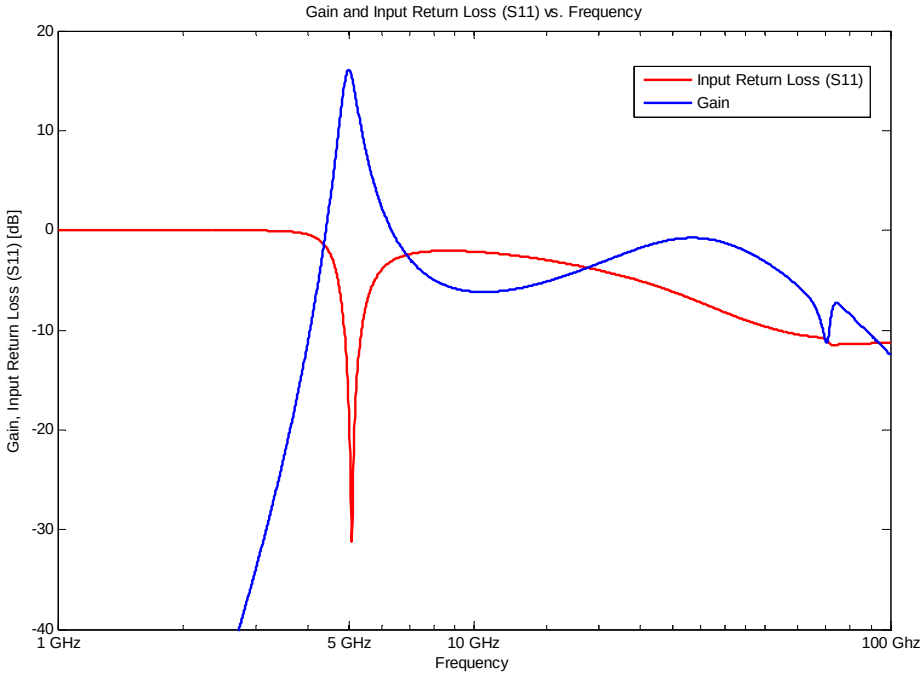

Figure 17: Gain and Input Return Loss vs. Frequency

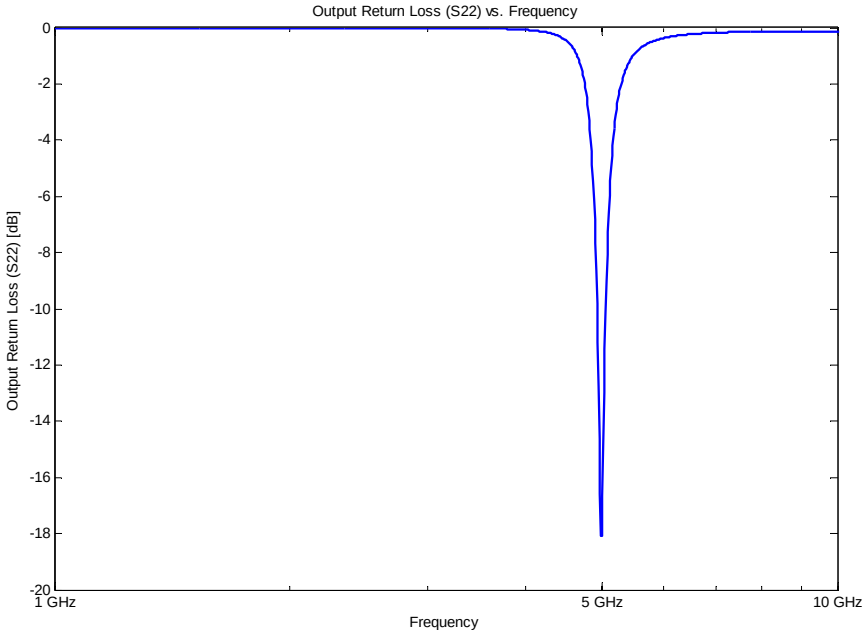

Figure 18: Output Return Loss vs. Frequency

Table 2 provides the summary of the exact outcomes that cannot be observed clearly in the figures.

Table 2: The summary of the achieved results through the design procedure using ideal passive components

	NF	NF_{MIN}	S_{11}	S_{22}	Gain
Results	0.882 dB	0.906 dB	-18 dB	-18.1 dB	16.1 dB

Finally, the finished design schematic is provided in Figure 19.

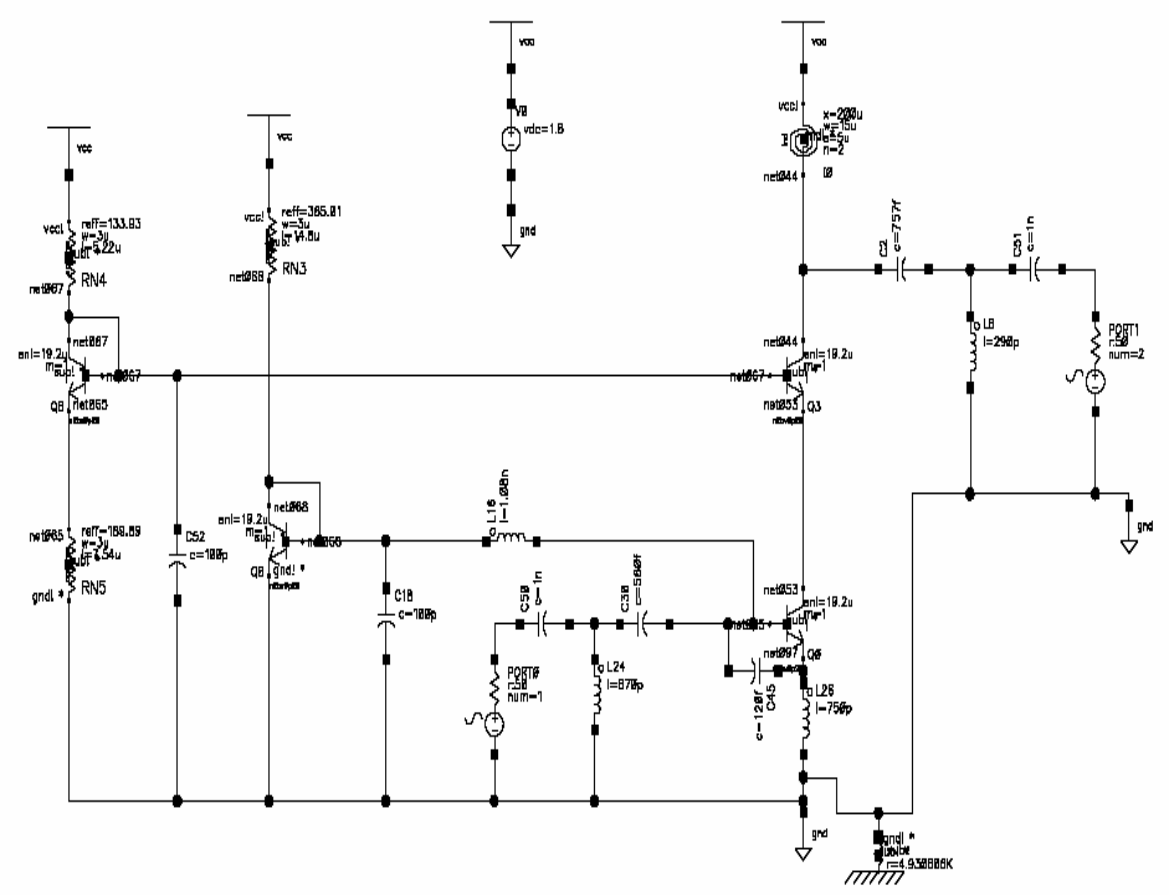

Figure 19: Final schematic of 5 GHz HBT LNA design

3.5 DESIGN EXAMPLE WITH NON-IDEAL PASSIVE COMPONENTS

In section 3.4, a design example of a HBT low noise amplifier operating at 5 GHz has been provided where ideal passive elements for matching network have been used to demonstrate the proposed design procedure. Now, the same low noise amplifier will be implemented with non-ideal components so that more realistic results could be found out.

First of all, it should be mentioned that with the addition of the non-ideal elements, a series resistance with the components should be considered. This series resistance directly determines the quality factor of the components. For an inductor the quality factor can be given as follows:

$$Q_{ind} = \frac{\omega L}{R} \tag{3.50}$$

In (3.50), R is the associated series resistance. With the increase of the series resistance the quality factor drops down so that the performance of the circuit in terms of noise and linearity is degraded. Thus, it is always important to maximize the quality factor at the operating frequency. A similar relation can also be written for the capacitors as well.

$$Q_{cap} = \frac{1}{\omega RC} \tag{3.51}$$

The series resistance creates extra noise sources associated with each passive component so it becomes theoretically harder to identify the noise parameters of the reactive elements thereby increasing the noise figure of the LNA as well. The biggest contribution to the degradation in noise figure comes from the inductors. Generally, on chip inductors are undesired since they consume large space within the chip and the quality factor they present is relatively low (practically below 20). For the design of the 5 GHz HBT LNA, 5 different

inductors should be built. They have been designed as spiral inductors provided by the IBM 7HP design kit. Table 3 shows the characteristics of the constructed inductors.

Table 3: The design parameters and their corresponding values for the spiral inductors

	Outer Dimension	AM Width	n-Turns	Underpass Width	Inductance	Quality Factor at 5 GHz
L_c	450 µm	20 µm	1	15µm	1.031 nH	17.42
L_e	190 µm	20 µm	1	15µm	326 pH	18.46
L_m	270 µm	10 µm	1.5	15µm	1.23 nH	16.82
$L_{m,o}$	200 µm	20 µm	1	15 µm	350 pH	18.74
L_{load}	200 µm	15 µm	2	15 µm	1.05 nH	17.51

As mentioned before, none of the designed inductors can have a quality factor greater 20. Needless to say, this is in contrast with the design concepts assumed in the previous section. The effect of this contrast can be observed in the discrepancies between the values of the same components. The changes originate from the adverse contribution of the series resistances associated with the inductive as well as capacitive elements.

Even though, differences in component values are anticipated, the derived design procedure does not change at all to meet the specifications. This is desired as well as required since the methodology should persist against the variations in the component values. For the 5 GHz HBT LNA design, the same steps described in section 3.3.2 are followed.

As usual, the biasing at the minimum noise figure is ensured by utilizing the same voltage values. Then, a suitable combination of emitter inductance L_e and the extra base-emitter capacitance C_{ex} is searched to maintain the equality between R_{OPT} and R_{in}. This can be accomplished with the values of L_e=326 pH and C_{ex}=220 fF. The associated graph showing the exact behavior of R_{OPT} and R_{in} is provided in Figure 20. At 5 GHz, R_{OPT} is about 83 Ω whereas R_{in} has a value of 79 Ω, which is quite close.

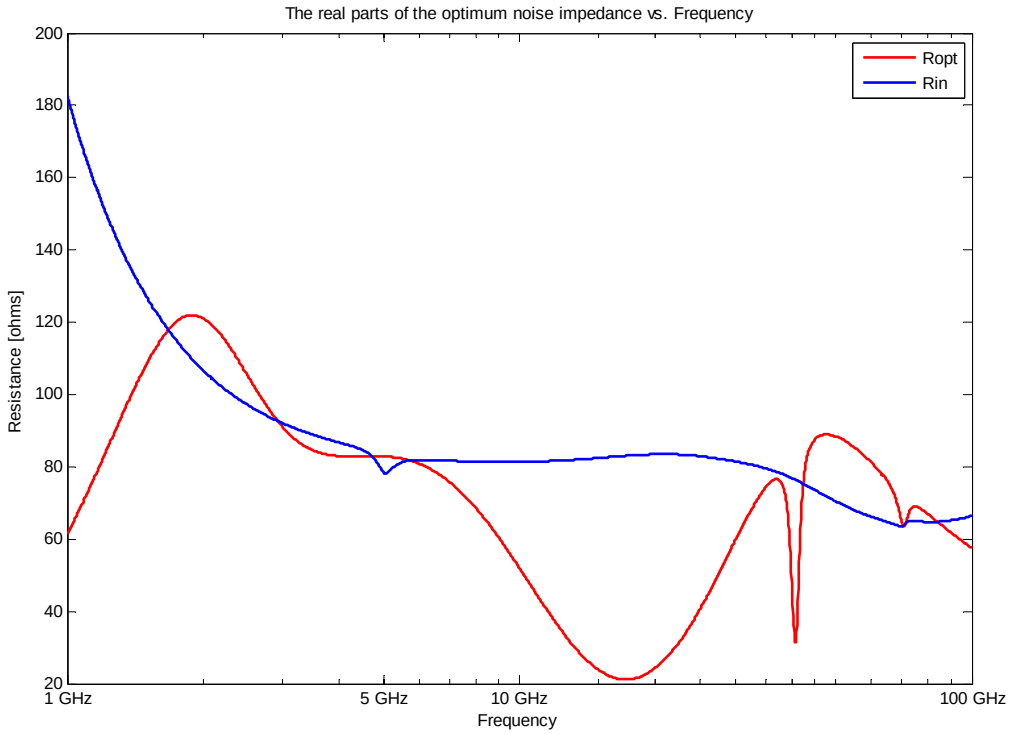

Figure 20: Ropt and Rin vs. Frequency for the design with realistic reactive components

Subsequently, the design continues with the selection of a suitable bias inductor L_c. Earlier, it has been explained that L_c should have a much smaller impedance so that X_{OPT} and X_{eqv} can be approximated to each other for the operating frequency. In the previous design example, the value was 1.08 nH. This value is kept almost the same (1.03 nH in the new

design) and a spiral inductor yielding that value has been constructed. With the introduction of the new inductor, X_{OPT} and X_{eqv} can be drawn like in Figure 21.

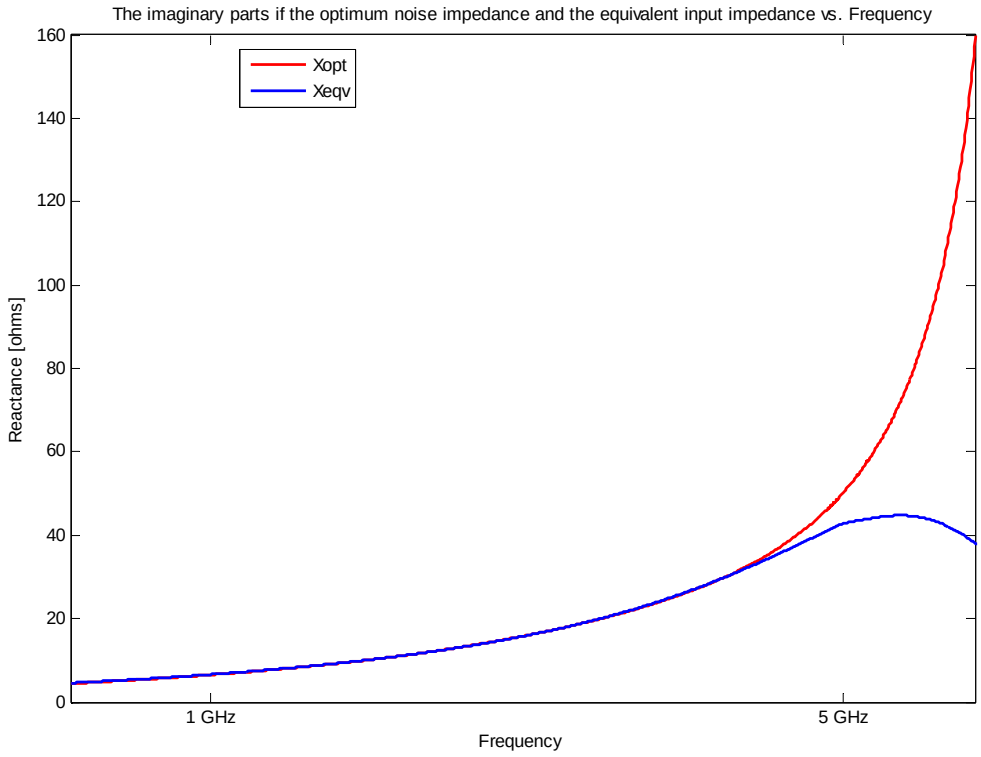

Figure 21: Xopt and Xeqv vs. Frequency for the design with realistic reactive components

Figure 21 suggests that at the operating frequency, X_{OPT} is about 50 Ω and X_{eqv} can be approximated to 43 Ω. Again these two parameters are very close to each other. The minor discrepancy can be tolerated as it will be seen when the final results are presented.

Afterwards, the matching network should be built. The calculations which are given in the theoretical reasoning part can be a base to start the computation; however, the associated series resistances necessitate an optimization process. By the end of the

optimization, the shunt input matching inductance is found to be 1.23 nH whereas the series capacitance at the base of the HBT is finalized with a value of 490 fF.

Using these realistic reactive components, the graphs representing the noise figure characteristics can be given in Figure 22. It suggests a difference between NF and NF_{min} of about 20 mdB. The noise figure is simulated to be around 2.2 dB. Compared to the design example with the ideal reactive components, an increase of 1.3 dB of the noise figure can be observed due to the parasitic resistance with the matching network elements.

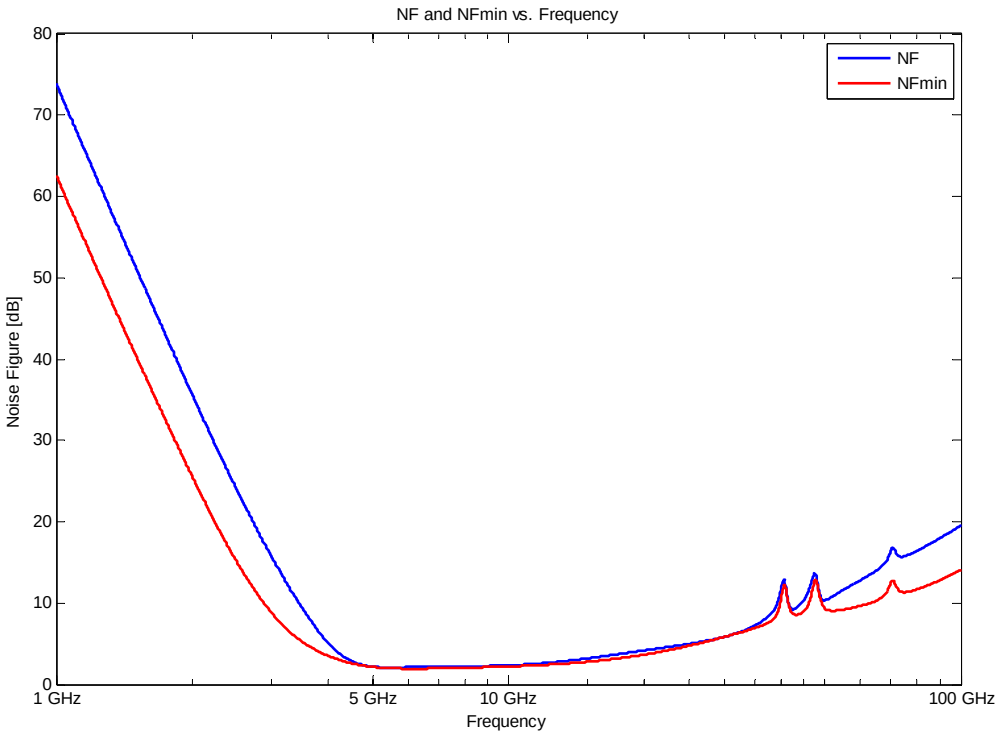

Figure 22: NF and NF_{min} vs. Frequency for the design with realistic reactive components

Next, the input matching and the transducer gain should be analyzed. Figure 23 depict the input matching and gain behavior of the designed low noise amplifier. The response of the circuit with the realistic elements actually exceeded its counterpart with the ideal

components in terms of performance. This can be attributed to the optimization that has been performed to realize the steps explained in the procedure.

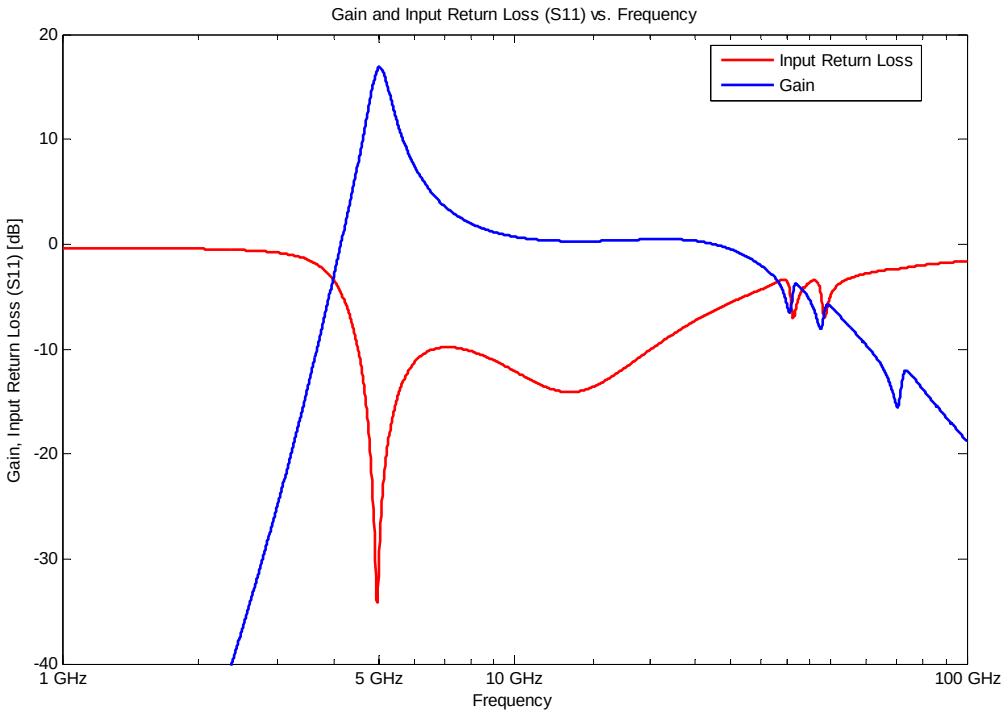

Figure 23: Gain and Input Return Loss vs. Frequency for the design with realistic reactive components

Lastly, the output return loss (S_{22}) has also been provided at this point. An output matching shunt inductor $L_{m,o}$ of 350 pH is made use of with a series capacitor of 730 fF. The outcome of these components can be visualized in Figure 24. The value for S_{22} reached in that diagram is close to its equivalent for the design with ideal components.

Table 2 encompasses the exact values of the critical quantities which constitute the basic design targets. As can be easily realized, the design procedure derived with the ideal reactive components can be safely applied to the design with realistic elements, as well.

Finally, the full design topology that incorporates both the core amplifier structure and the associated bias circuits can be investigated in Figure 25.

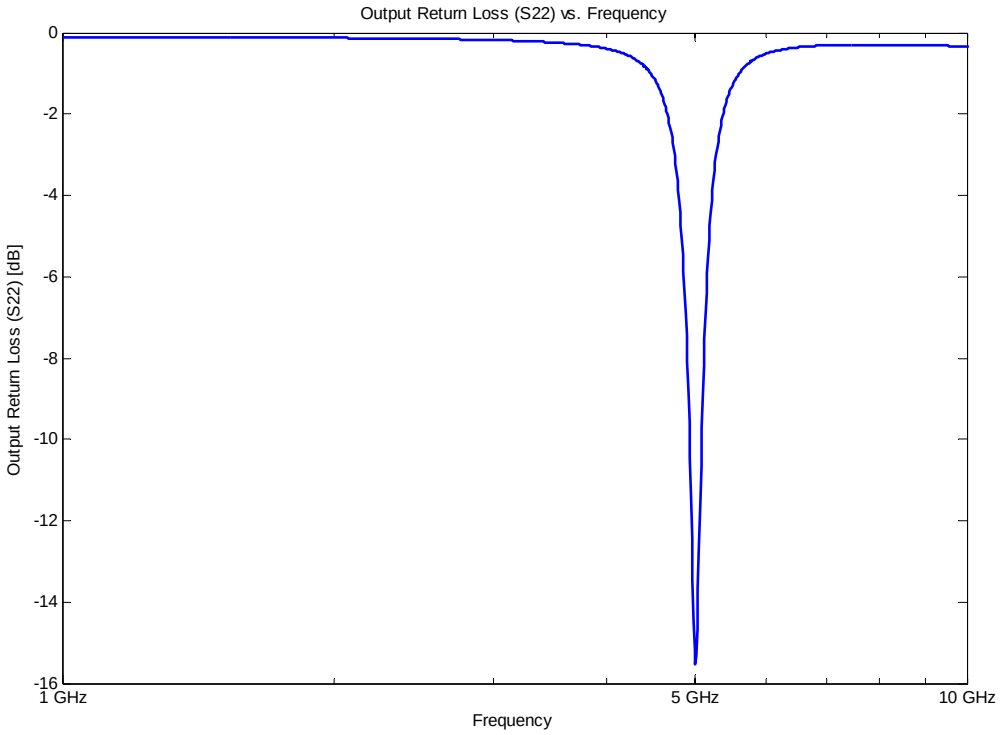

Figure 24: Output return loss (S22) vs. Frequency for the design with realistic reactive components

Table 4: The summary of the achieved results through the design procedure using non-ideal passive components

	NF	NF_{MIN}	S_{11}	S_{22}	Gain
Results	2.181 dB	2.163 dB	-31.6 dB	-15.2 dB	16.8 dB

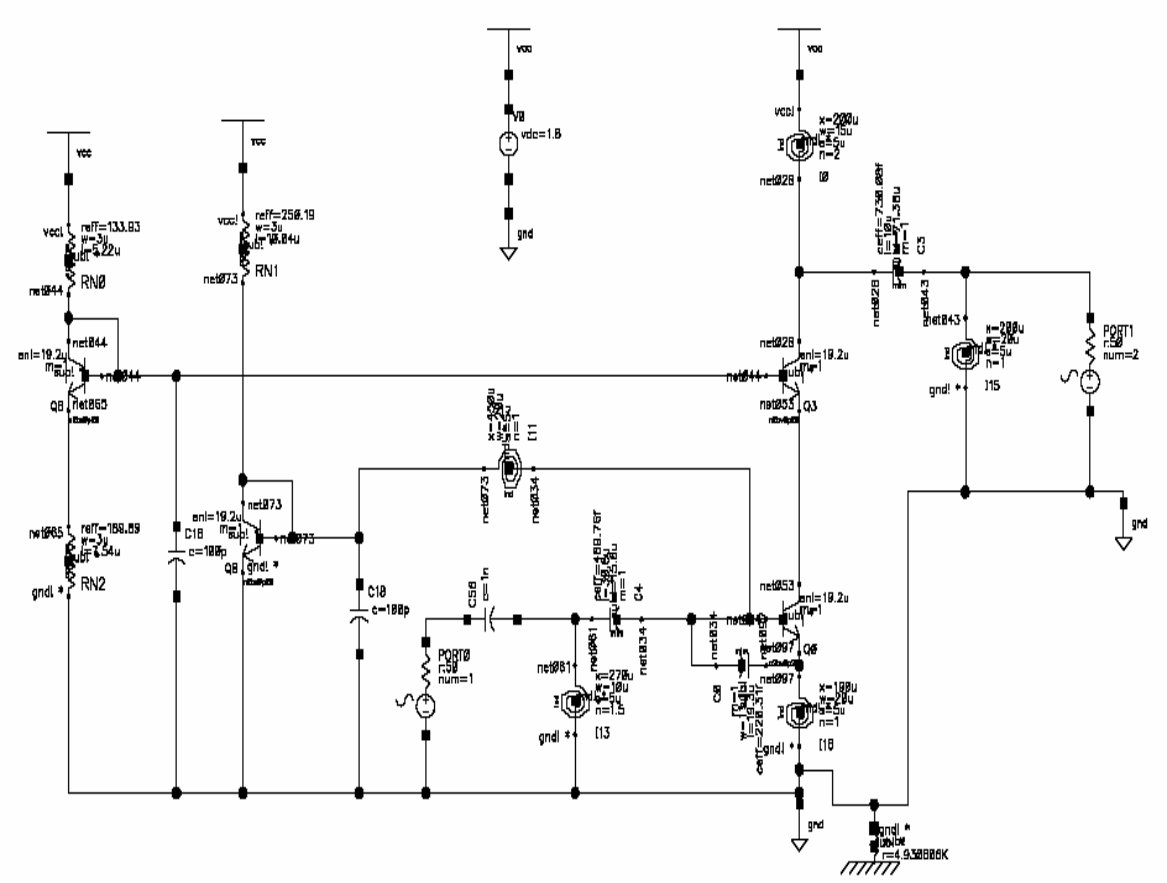

Figure 25: Final schematic of 5 GHz HBT LNA design for the design with realistic reactive components

Like in the previous section, the last issue to investigate is the total dissipated power. As expected before, the total current that passes over the 1.8 V power supply rises to 10.28 mA yielding a total power content of 18.5 mW. This number is also agreeable though as a future work; it should be aimed to reduce it further since generally, high power dissipation is inherently undesired in wireless communication circuits.

3.6 A DISCUSSION ON LINEARITY

The linearity is an important concept for receiver systems. Especially, at large signal level, the deviation from the gain performance that is observed at small signals can be easily characterized by means of linearity concepts. One of these is the input referred third order intercept point (IIP3). When two narrowly spaced sinusoidal tones with frequencies ω_1 and ω_2 applied to the receiver structure, the third order harmonic terms with the frequencies $2\omega_2$-ω_1 and $2\omega_1$-ω_2 take place very close to the original signals. Thus, they cannot be filtered out and add a nonlinear behavior to the power gain response of each component of the receiver [5]. The negative effect due to the existence of these intermodulation (IM) terms can be quantified by determining the intercept point of the first order output with the third order IM terms on an output power vs. input power graph. The simulation results for the design presented in this work with the realistic passive components can be seen in Figure 26. Here, IIP3 can be found as -7 dBm, which indicates that the final design has an acceptable level of linearity.

For LNAs, it should be mentioned that none of the design procedures reviewed before makes a reference to the linearity as a design step. This situation arises mainly due to the fact that the theoretical IIP3 calculations are relatively complex and the results that come out cannot be converted into a simple design step. Besides, the priority in LNA design is always assigned to the noise and gain performance since it can be shown that for a multi-stage receiver structure the latter stages dominate while determining the overall linearity response [22]. Despite these reasons, still, low noise amplifiers are expected to yield satisfactory values for the linearity and the IIP3.

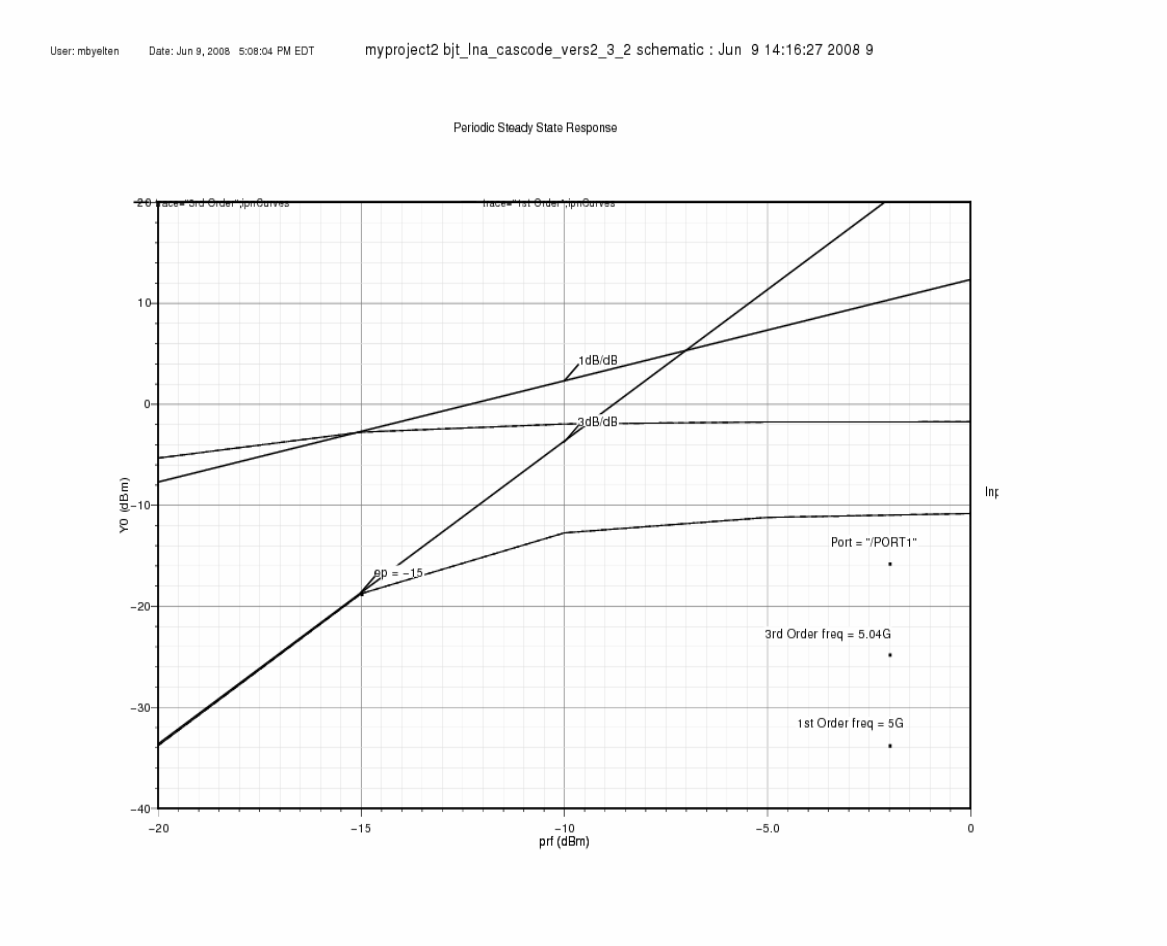

Figure 26: IIP3 of the LNA at 5 GHz with realistic reactive components

The aim of this thesis is to inquire design strategies to achieve simultaneous noise and input power matching by using the tunable reactive components. Thus, the linearity is not considered explicitly based on the reasoning given in the previous paragraph. However, for narrowband structures the relationship between the gain, noise and IIP3 has been investigated. Liang et al. have shown that to operate the LNA at the optimum design point for the noise figure results in acceptable IIP3 values, however, an increase in the bias current and emitter length can improve IIP3 significantly [23]. This observation has also been made by

Shana'a et al. where they claim that an increase of 6 dB in IIP3 can be accomplished when the bias current is doubled [24].

To conclude, the interaction of noise, gain and linearity performances of the low noise amplifiers are relatively obscure and for tunable LNA applications, these should be analyzed in depth which may be viewed as a future work.

CHAPTER 4

4 DESIGN OF TUNABLE LOW NOISE AMPLIFIERS

4.1 THE BACKGROUND KNOWLEDGE ON TUNABLE LNAs

As the wireless communication technology has developed steadily, new standards appeared which are located at different frequency bands. Some examples for these communication standards can be given as WCDMA, WLAN, GPS, etc. [25] The associated hardware that will be used for these standards have been built with the perspective of narrowband IC design techniques. However, it is strongly desired that the designed hardware can receive information simultaneously from several distinct frequency bands [26]. This property is called multi-band operation and the basic aim with that is to unify the circuitry for all wireless communication standards into one single topology.

The first alternative to build a multi-band front end circuit is constructing receiver circuit tracks for each standard, i.e. for all frequency bands, a different LNA, down-converter and other building blocks should be designed. This suggestion consumes high power due to the plethora of the components and the large chip area occupied by them [25]. Another alternative to this problem has been brought by Hashemi and Hajimiri. They built a concurrent multi-band low noise structure so that they introduced an inductor and a capacitor (LC branch) in series, where the LC branch itself is shunted to a parallel combination of an inductor and a capacitor (LC resonator). LC resonator and LC branch have the same task where they create a zero in the transfer function so that the drain load shows high impedance

at the desired frequencies [26]. Their LNA operates at two different frequencies, 2.45 GHz and 5.25 GHz, so that a narrow-band operation can be accomplished with their design proposal. Nevertheless, their work does not allow to arbitrarily increase the number of operation frequencies since for each different band, there is a need for another LC branch, that enforces bigger chip area requirements and degradations in the performance due to the added passive components. Additionally, the noise figure of the low noise amplifier could be optimized for only one operating frequency so the noise performance is exacerbated for elevated frequencies.

A final approach to this problem is using tunable elements so that a reconfigurable LNA can be built. This type of LNA will be able to exhibit minimum noise figure and maximum transducer gain, i.e. narrowband operation characteristics at several distinct frequencies by adjusting the tunable passive components to the required values. Different design proposals have been made in this context. Some notable studies will be provided here briefly.

Some researchers focused on tunable elements in the input matching network. Sugawara et al. built a high pass L-type matching network where a series capacitor with the input port is shunted by a variable inductor at the gate of a NMOS transistor of 0.18 μm CMOS technology [25]. They produced their own tunable inductor with which they built a LNA working over the frequency band of 1.7 to 3.2 GHz. However, the noise figure significantly suffered from the low Q-factor of the inductor and at 1.9 GHz, NF= 7.1 dB has been acquired.

Several researchers investigated the possibilities of using tunable elements in the output load or at the interstage of their topology. The basic reason for this choice originates from the fact that the tunable elements at the input introduce large amount noise and non-linearity. A cascode topology eliminates the interaction between the input and output matching networks so that the degradation due to the passive components at the output can be eliminated via the inherent isolation. Ahsan et al. and Danson et al. used capacitive switches at the load of their LNA [27], [28]. These components enable larger shifts in the frequency domain compared to the tunable capacitors so that a dual band operation can be made possible. Both of the designs target the same frequencies as Hashemi and Hajimiri, namely 2.4 GHz and 5.2 GHz. Ahsan et al. used single-pole double-throw (SPDT) switches based on a specific topology of a set of transistors whereas Danson et al. relied on microelectromechanical systems (MEMS) type capacitive switches. Both design got good results at the desired narrowbands however the operation is limited to the target frequencies, thus the tunability aspect is not satisfied.

Shin and Yoo put a tunable capacitor in the interstage of their LNA design [29]. This preference resulted in a tunability range from 1.8 GHz to 2.4 GHz. Even though the gain and input matching criteria has been met, the noise figure for the whole range is above 4.5 dB which indicates that no special design procedure to minimize the noise figure has been adopted.

Fu et al. has come up with a different design idea [30]. Their design is composed of a broadband input matching structure and a tunable output matching topology where the tunability is achieved by a switched inductor and several varactors. The final LNA can be

tuned from 2.4 GHz to 5.4 GHz and has a good gain ad input matching performance. Nevertheless, the broadband matching does not specifically target the capture of minimum noise figure. Still, the noise figure performance is better compared to similar design examples.

4.2 INITIAL DESIGNS CONSIDERING FULLY TUNABLE CIRCUITS

In this section, the design procedure that has been introduced in Chapter 3, will be tested at two different frequencies, namely at 1 GHz and 10 GHz. The aim here can be summarized as follows. First of all, the design procedure will be tested at two other frequencies so that it can be validated at different bands as well. At the same time, the concepts regarding the tunability should also be considered. For this purpose, the first step of the design procedure which is to find the bias voltage that leads to the minimum noise figure will not be applied here. Instead, the bias voltage that has been chosen for 5 GHz will be preserved. One reason for this preference is to see the effect of the change in the values of the matching network passive components. The other reason comes from a separate analysis that has been applied to see the required bias voltages which will yield the minimum noise figure from the HBT device. This study revealed that a bias voltage of 0.8 V at 1 GHz, and 0.84 V at 10 GHz are required. The results are very close to the assumed value 0.83 V. Considering the hardware difficulties to make the bias voltage variable at that scale, it is more plausible, to equate it to the required value for the near mid-band frequency (exact mid-band is at 5.5 GHz). The biggest change experienced in the noise figure which is at 1 GHz can be approximated as 0.1 dB that can be tolerated.

Another reason to realize two distinct designs is related with the variation in the values of the matching network passive components. These variations directly determine the importance of converting that element to its tunable counterpart. The different elements which are under investigation can be specified as the emitter inductor L_e, input matching inductor L_m, input matching capacitor C_m, bias voltage inductor L_c, the extra base-emitter capacitance C_{ex}, and the output matching capacitor and inductor, $C_{m,o}$ and $L_{m,o}$, respectively.

In the construction of both designs ideal reactive elements have been utilized. Same design steps (except the first one) described in 3.3.2 has been applied exactly. The results for 1 GHz and 10 GHz will be summarized by the subsequent tables and figures.

First, the design values for the individual components in three different designs are presented in Table 5. This table is very good to visualize the trend of the design parameters. As can be easily observed, with the increase of the frequency, the values of L_e and C_{ex} decrease significantly. If one returns to the design equation (3.22), then it can be seen that L_e is anti-proportional with operating frequency. For 1 GHz, (3.22) anticipates an emitter inductance of 3.5 nH. To reduce this value, C_{ex} should be increased so that the decoupling effect can be boosted. From these considerations, the question why L_e and C_{ex} need to have higher values at low frequencies can be clarified.

Another important trend to note is the increase in the values of the L_m, C_m, $L_{m,o}$ and $C_{m,o}$. This also stems from a similar reasoning given above. As the frequency scales down, to reach the necessary reactance values the passive components should be enlarged. L_c complies with this explanation, as well.

Table 5: The design values of the matching network passive components

	1 GHz	**5 GHz**	**10 GHz**
L_e (Emitter Inductance)	880pH	750 pH	500 pH
C_{ex} (Extra Base-Emitter Capacitance)	390 fF	120 fF	50 fF
L_m (Input Matching Inductor)	1.16 nH	670 pH	161 pH
C_m (Input Matching Capacitor)	6.35 pF	560 fF	695 fF
L_c (Bias Voltage Inductor)	2.7 nH	1.08 nH	200 pH
$L_{m,o}$ (Output Matching Inductor)	2.5 nH	290 pH	328 pH
$C_{m,o}$ (Output Matching Capacitor)	2.7 pF	757 fF	150 fF

It should be mentioned that even with ideal components, a large frequency span is very difficult to achieve with tunable elements. The ranges that are projected for tuning the capacitors and inductors are quite large. Furthermore, making every reactive element tunable is not feasible due to the poor quality factors of on-chip tunable elements. Each tunable element enervates the linearity and as well as the noise figure. Thus, the number of them should be minimized and the importance of their contribution should be clearly outlined.

Table 6 summarizes important design outcomes. As the frequency is boosted the noise figure increases proportionally. A good correspondence between the noise figure of the amplifier and the minimum noise performance has been achieved. The return ratios are ensured to be below the predefined limits (i.e. S_{11}, S_{22} <-10). The gain is quite high at 1 GHz, approaching 25 dB whereas at 10 GHz, a gain of 15 dB could be accomplished.

Table 6: Design outcomes of the critical performance quantities

Results	NF	NF_{MIN}	S_{11}	S_{22}	Gain
@ 1 GHz	0.59 dB	0.58 dB	-11 dB	-25.5dB	24.5 dB
@ 10 GHz	1.34 dB	1.33 dB	-12.8 dB	-16.1 dB	14.9 dB

Figure 27 through Figure 32 present the design achievements graphically. The first three figures belong to the LNA operating at 1 GHz; the last three comes from the LNA working at 10 GHz.

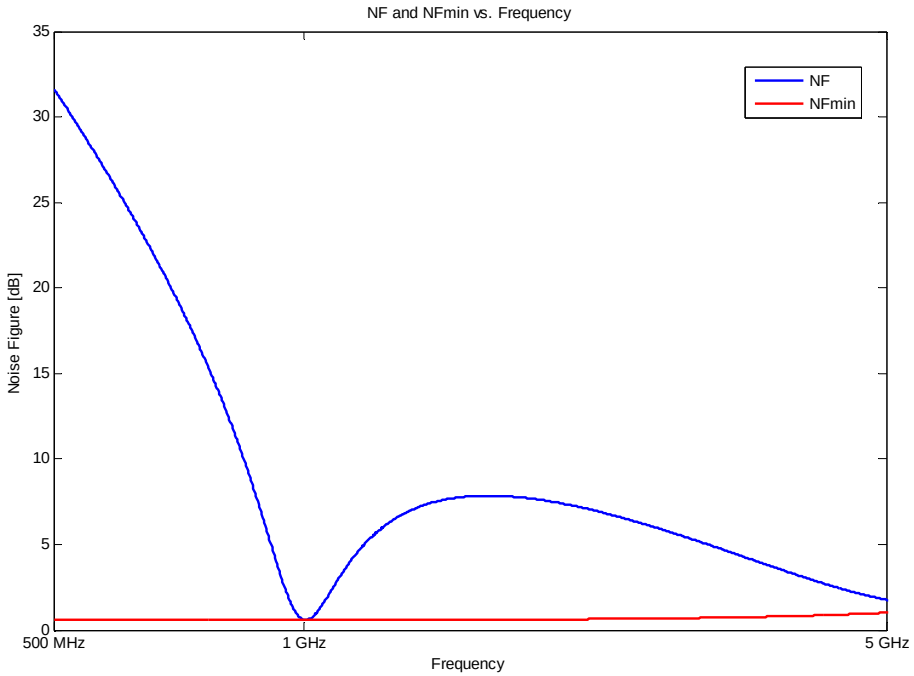

Figure 27: NF and NF_{min} vs. Frequency for the design operating at 1GHz

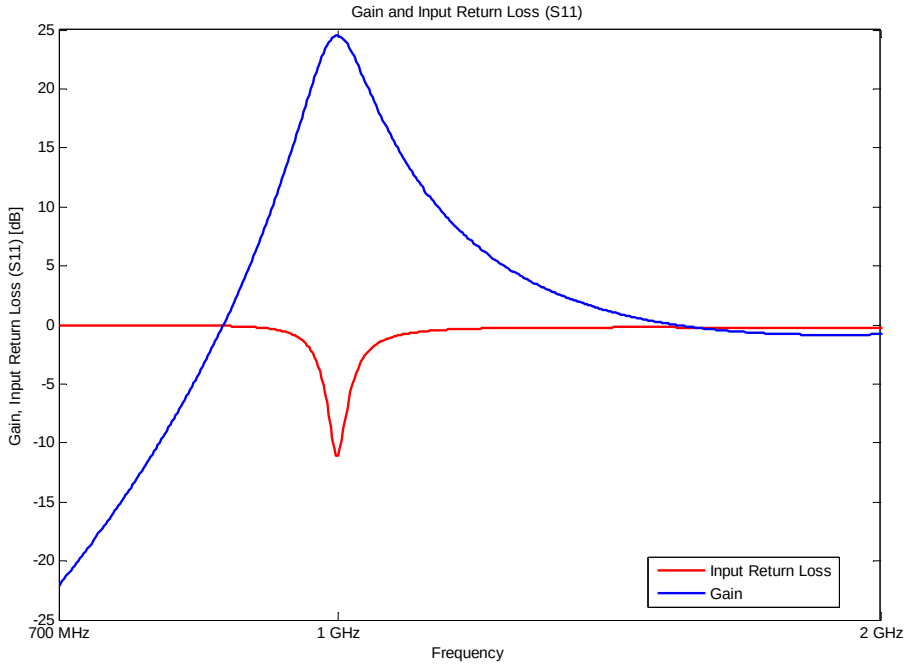

Figure 28: Gain and Input Return Loss vs. Frequency for the design operating at 1 GHz

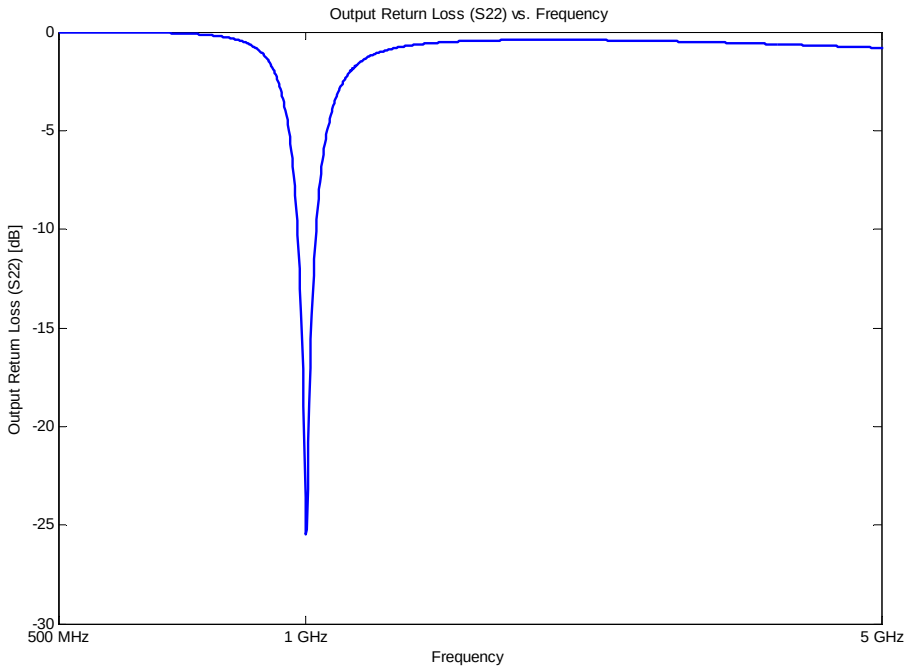

Figure 29: Output Return Loss (S22) vs. Frequency for the design operating at 1 GHz

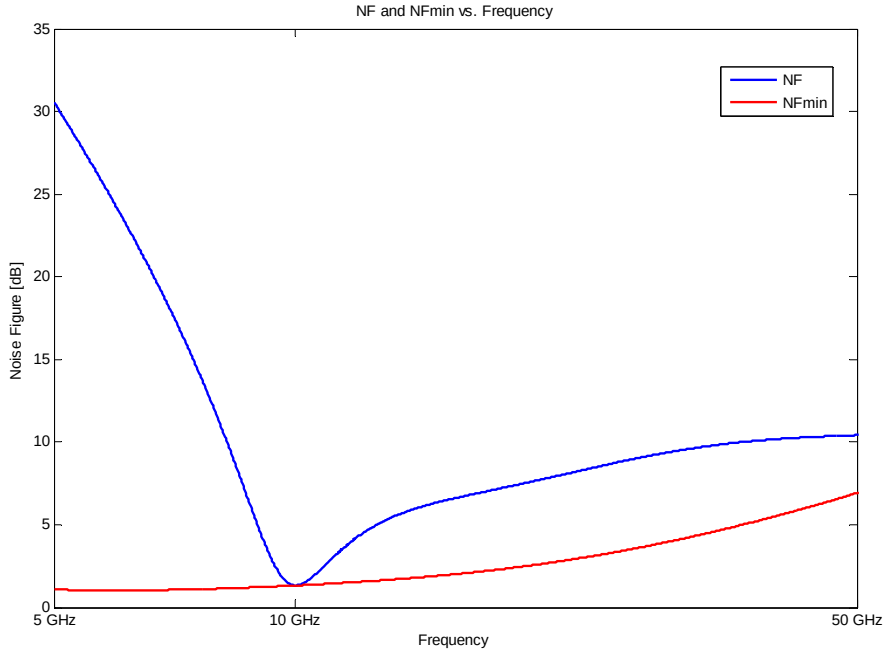

Figure 30: NF and NF_{min} vs. Frequency for the design operating at 10GHz

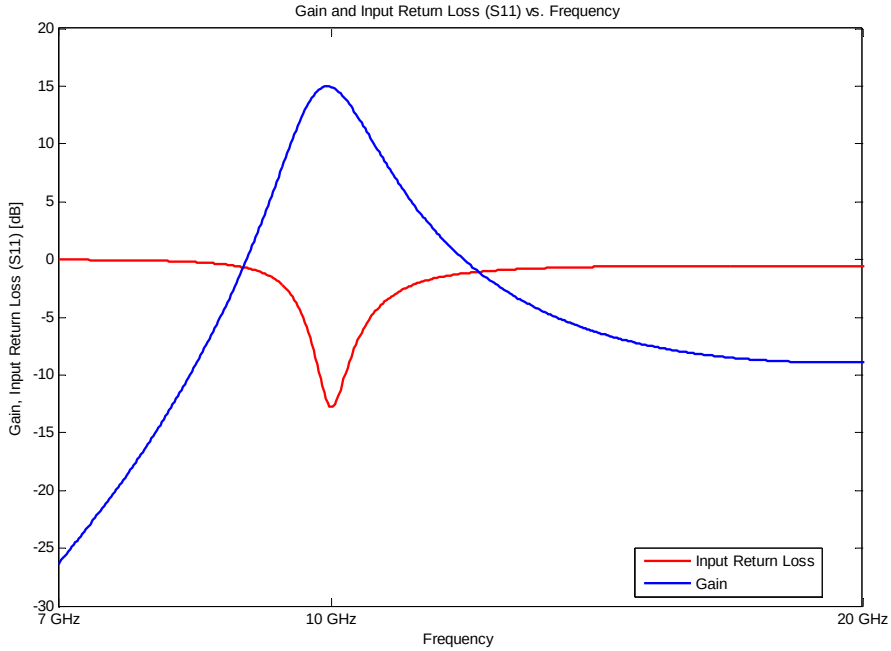

Figure 31: Gain and Input Return Loss (S11) vs. Frequency for the design operating at 10 GHz

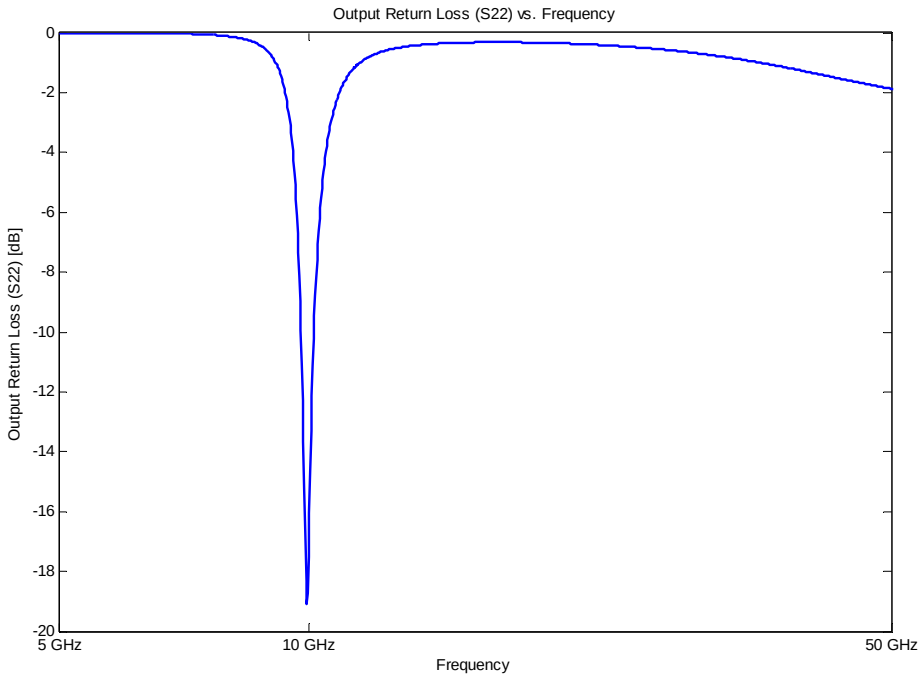

Figure 32: Output Return Loss (S22) vs. Frequency for the design operating at 10 GHz

4.3 PROPOSED TUNABLE LNA ARCHITECTURE

In the previous section, the designed low noise amplifier has been modified so that it can operate at 1 GHz and 10 GHz by changing the values of all reactive components so that the desired performance i.e. a minimized noise figure and a superior input and output matching can be managed. However, as mentioned before, this approach is not practical since multiple tunable elements deteriorate the performance of the low noise amplifier significantly. To prevent this situation, the number of the tunable elements should be held minimum. However, the problem is to find which components pose the most suitable structure for this purpose.

First of all, the reactive elements used in the LNA can be classified into two groups. The first group is constituted by the components which are required to fulfill the minimum noise performance outlined by (3.4)-(3.9). These are L_e, C_{ex}, and L_c. In the previous chapter, these parameters have been adjusted to bring up the best results for the LNA operating at 5 GHz. As can be observed in 4.2, obtaining the same performance at other frequencies requires huge changes in all of these parameters. Thus, at this point, the second group of reactive elements gains importance. These are the elements utilized in the matching network, which are L_m, $L_{m,o}$, C_m and $C_{m,o}$. Actually, the strategy that will be followed next in this chapter can be formulated at this point. Rather than acquiring the best noise and input-output matching performance at all frequencies, an outstanding result will be accomplished near the mid-band of the selected target frequency range and then by using the tunable matching network reactive components, the performance at that particular narrowband operation is translated to the neighboring frequencies.

In this thesis, a design at 5 GHz has already been completed. Thus, the best choice for the investigation of the tunable matching network elements is to modify the architecture proposed for 5 GHz and to extend the satisfactory results managed at the narrowband operation to the maximum range of frequencies.

At this point, however, it has not been determined which matching network components should be converted to their tunable counterparts. In fact, the matching is achieved by the combination of both the shunt inductors L_m and $L_{m,o}$ and the series capacitors C_m and $C_{m,o}$. However, the desired effect of sweeping the noise and minimum noise figure curves over the frequency can be managed by the series capacitors. Shunt inductors are

basically utilized to minimize difference between the noise and minimum noise figure at a certain frequency. However, these comments are valid for the design topology described in this thesis. In other contexts, same outcomes can be brought up by different means of matching network circuit design.

Based on the ideas explained above, Figure 33 has been proposed for a tunable low noise structure. As can be realized easily, the difference between the narrowband topology and this figure is the tunable matching capacitors. It is aimed to keep all other components at their previous values which have been found from the narrowband operation at 5 GHz.

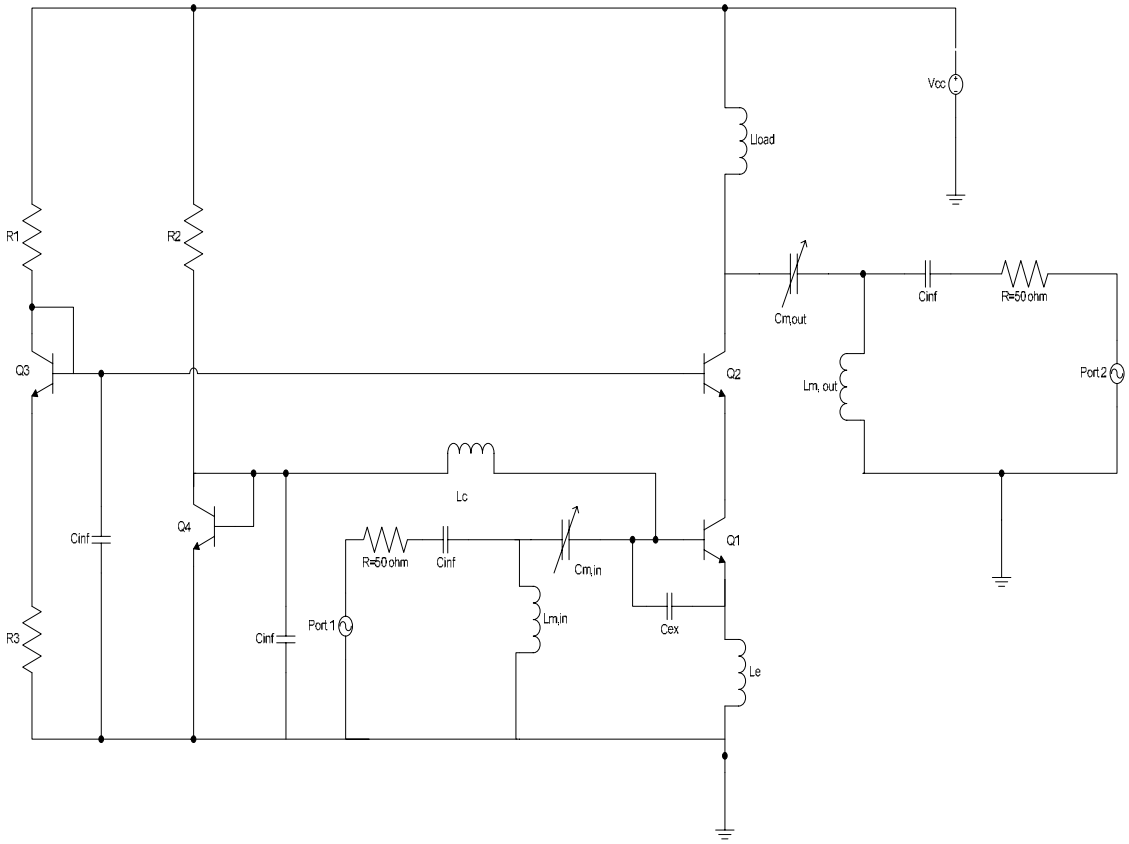

Figure 33: Suggested topology for tunable low noise amplifier

A question may arise why both the input and the output matching capacitors are varied. As it has been mentioned in 4.1, most of the approaches until now were based on a single tunable capacitor at the output of the low noise amplifier and at the input the designers relied on a broadband matching. However, the goal pursued in this thesis is to achieve simultaneous input and noise matching which essentially necessitates employing a variable capacitor in the input matching network, as well.

Next, the ideal and realistic versions of the LNA designs at 5GHz will be analyzed in terms of the tunability. By doing that, the value of the input and output matching capacitors will be varied and the noise and input matching performance are going to be monitored at several other frequencies. This analysis will be conducted both with an ideal capacitor and a realistic capacitor.

4.4 TUNABILITY ANALYSIS OF THE SUGGESTED TOPOLOGY

In this section, the designs regarding the tunability will be presented. In the first step, the LNA design at 5 GHz with ideal reactive components will be considered. This corresponds to the content of the section 3.4. Here, the input and output matching capacitor values are tuned for several different frequencies to get the best results regarding the noise and input matching. Below are the results that have been gathered after simulations at several distinct frequencies. The simulated frequencies are expressed in the x-axis values of the graphs. Figure 34 and Figure 35 depict the behavior of the LNA for various critical quantities for the design procedure whereas Figure 36 reveals the variation in the capacitor values to realize the projected trend in the input matching and noise performance.

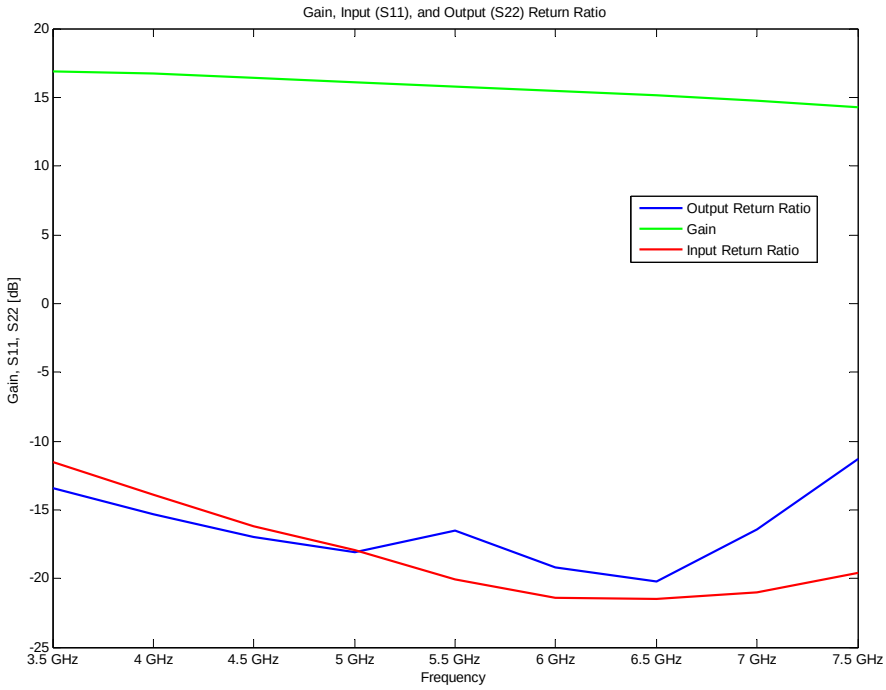

Figure 34: Gain, Input and Output Return Loss vs. Frequency for the tunable LNA with ideal C_m

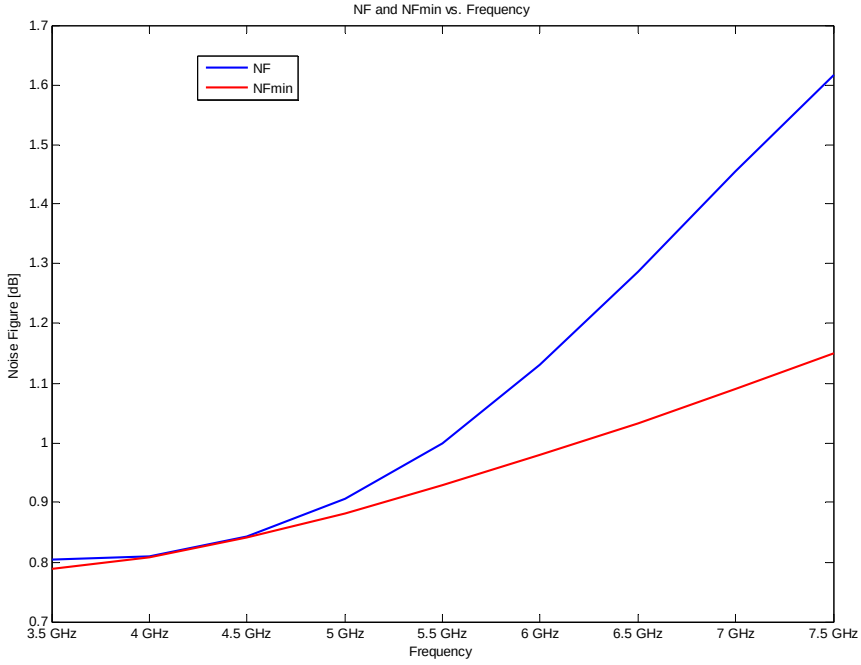

Figure 35: NF and NF_{min} vs. Frequency for the tunable LNA with ideal C_m

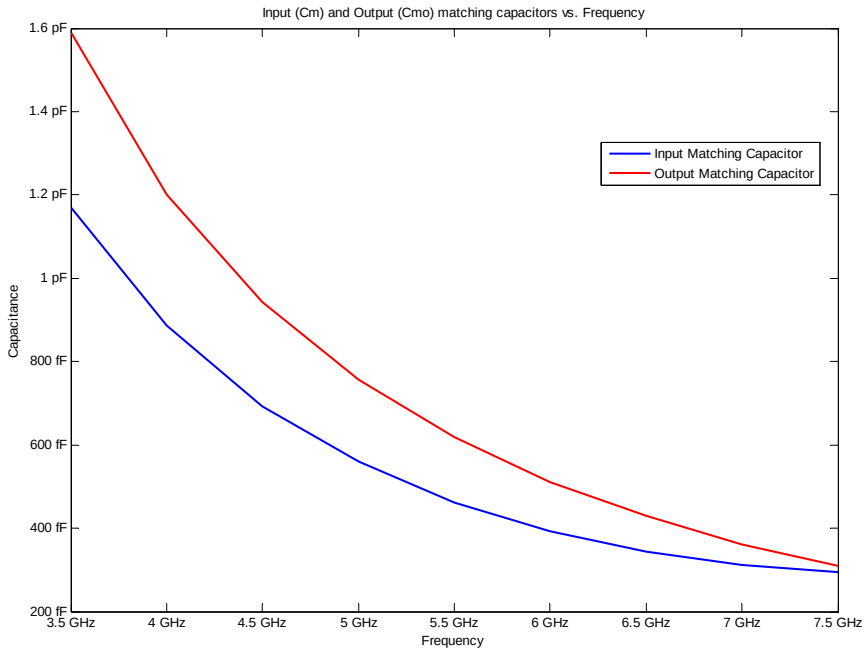

Figure 36: Variation in the values of the Input and Output Matching Capacitor (ideal)

The graphs can be evaluated from various perspectives. First of all, the frequency range over which the design constraints are satisfied is really big, extending from 3.5 GHz to 7.5 GHz. The gain is virtually constant throughout the range and S_{11} and S_{22} values are below the thresholds for appropriate functioning. The noise figure response is almost the same with the minimum noise performance for low frequencies, however as the operation frequencies are increased the difference is enlarged. Typically and practically, a 0.5 dB difference is assumed to be diverging from the equality of NF and NF_{min}, thus the higher limit is basically set by them near 7.5 GHz. The lower limit has been provided by the return ratios where they become lower than -10 dB for smaller frequencies compared to 3.5 GHz. Figure 36 reveals that a moderate range should be expected from the tunable capacitor compared to the large frequency range. The maximum capacitance comes from the output matching capacitor with

1.6 pF at 3.5 GHz, whereas the minimum value is set by the input matching capacitor with 294 fF at 7.5 GHz.

Now, the design discussed in section 3.5 will be taken and modified so that realistic capacitors are used for the variable matching capacitor. The same analysis applied above is adopted. The capacitance value is swept for frequencies from 3 GHz to 7 GHz by a difference of 500 MHz. With the realistic components, the upper limit is reduced from 7.5 GHz to 7 GHz. Figure 37 and Figure 38 represent the combination of the results collected from the various simulations and Figure 39 finalize the values of the input and output matching capacitor values. The outcomes of the simulations indicate that with the realistic capacitors replacing their ideal counterparts, the deterioration of the input return ratio and the divergence of the noise figure from the minimum noise figure performance accelerate.

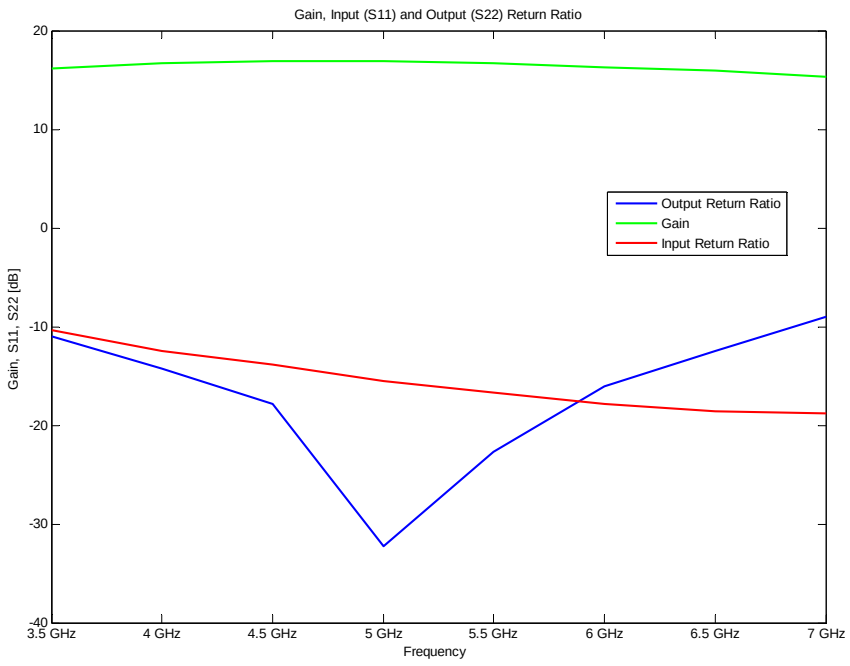

Figure 37: Gain, Input and Output Return Loss vs. Frequency for the tunable LNA with realistic C_m

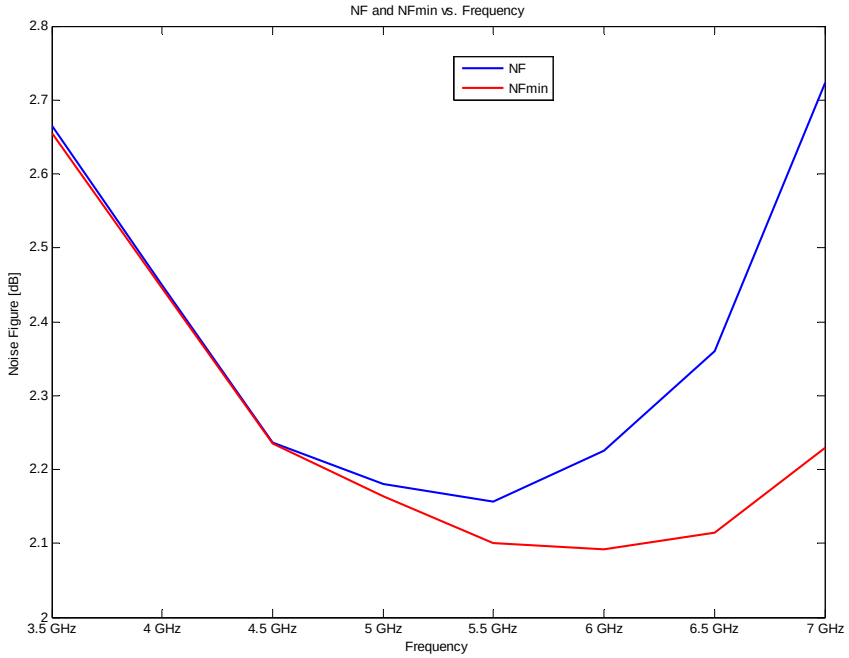

Figure 38: NF and NF_{min} vs. Frequency for the tunable LNA with realistic C_m

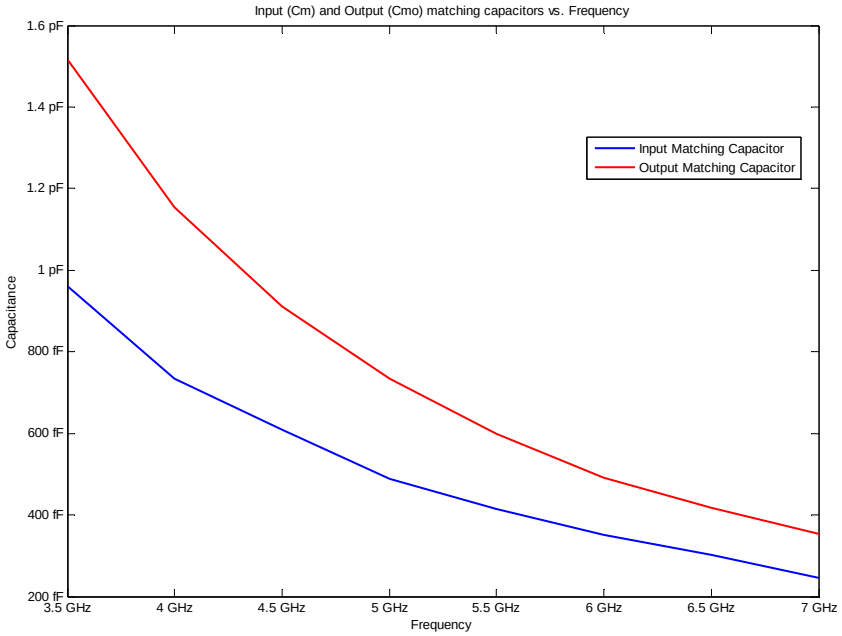

Figure 39: Variation in the values of the Input and Output Matching Capacitor (realistic)

At 7 GHz, the S_{11} parameter drops down to -9 dB exceeding the practical threshold. Same pattern of getting close values for NF and NF_{min} at lower frequencies for ideal matching capacitors continue with realistic components as well. The noise figure changes between 2.2 dB and 2.7 dB, which are relatively low for such a large range. This can be directly attributed to the novel design procedure and the introduction of the tunable input matching capacitor. One further advantage that has been acquired by using the realistic components is the reduction in the necessary capacitance values. This can be observed by comparing Figure 39 with Figure 36. As it will be discussed in the next section, lower capacitance values are favorable from the physical design point of view of the tunable capacitors.

4.5 FEASIBILITY OF PRACTICAL TUNABLE CAPACITORS

In the preceding section it has been assumed that the value of the capacitors can be changed as desired. However, in the real life there are several constraints that restrict the usage of the tunable capacitors. Thus it is a necessity to investigate the feasibility of using the tunable capacitors with the desired characteristics as it has been found out in the previous design examples.

There are several alternatives that can be used as a tunable capacitor. These can be listed as the bipolar diode varactors, gated MOS varactors, Barium Strontium Titanate ($Ba_xSr_{1-x}TiO_3$) varactors (also known as BST varactors) and MEMS tunable capacitors. MEMS type tunable capacitors can be of electrostatic or piezoelectric actuation [31]. Each of

these tunable capacitors has different characteristics which will be explained as these properties are defined.

The first issue to discuss related with the characteristics of the tunable capacitors is the quality factor. Simulation results demonstrate that the realistic capacitors that have been used in the second design reached quality factors between 244 and 127 which are quite high. Nevertheless, practical tunable capacitors can reach that high quality factor only for a narrow frequency range. The low quality factors basically arise due to the series resistance associated with them. Especially, the bipolar diode varactors may yield quality factors of 10 to 20 at 1-2 GHz [31].

The second issue to investigate is the tuning ratio. Tuning ratio for tunable capacitors is defined as follows:

$$R_{tune} = \frac{C_{\max}}{C_{\min}} \qquad (4.1)$$

It is to note that a tunable capacitor should have a maximum tuning ratio to increase the frequency range where it can be used. MEMS type tunable tunable capacitors have been reported to possess a tuning ratio of 15 [32]. However, this quantity may be misleading, since the minimum capacitance can be low (typically less than 100f) thus the highest achievable capacitance might still be less than 1 pF.

Although MEMS type tunable capacitors seem very promising in terms of quality factor and tuning ratio, they require high values of actuation voltages [31]. Similarly BST varactors, which has the tunability property because of the change in their relative dielectric constant ε_r with the application of a DC bias, suffers from a similar issue. The DC voltage

that should be provided for the variation in ε_r is very large [33]. Typical values of the potential that have to be applied to MEMS or BST type tunable capacitors may change between 10 and 50 V. These values pose a great problem because the bias circuitry associated with high voltages produce a big noise content that must be isolated from the low noise amplifier circuit.

Another important feature of the tunable capacitors is the self resonance frequency. The self resonance frequency can be defined as the frequency where the capacitor starts to behave as an inductor yielding negative capacitance values. Just before the self resonance frequency the capacitance begins rising and then it falls sharply to negative values. The self resonance frequency should be pushed outside of the targeted frequency range, so that the possibility of yielding negative capacitances can be avoided. Especially, at high frequencies, the required input and output matching capacitor values decrease as can be observed from the results acquired in the previous sections. This means that the increase due to approaching the self-resonance frequency may lead to higher capacitances though they are undesired. Moreover, near the self-resonance frequencies, the quality factor drops considerably. By building tunable capacitors with self-resonance frequencies occurring at very high frequencies (f_{self}> 10 GHz), this drawback can be overcome as well. Apart from these characteristics, one has to also mention the linearity and power consumption as key concepts. Nonlinear elements will certainly degrade the dynamic range of the low noise amplifier which is strongly discouraged. The power consumption of the tunable elements has to be restricted to smaller values so that dangerous heating can be avoided.

To sum up, the main expectations from a tunable capacitor can be summarized as follows. Series resistance should be minimized so that reasonable quality factors (typically greater than 50) can be acquired. The associated DC bias should be decreased to acceptable values (preferably less than 5 V). Besides, tuning ratios (based on a relatively high C_{min}) has to be increased. Finally, the finished component should yield low power consumption and present a highly linear response.

At this point, some examples of state of the art tunable capacitors will be introduced and their suitability to the specifications determined in this work is going to be analyzed.

Gu and Li have presented a CMOS compatible Metal MEMS tunable capacitor very recently [34]. In this paper, they achieved to develop a variable capacitor which can be varied from about 250 fF to 850 fF by an application of 4 V potential at frequencies lower than 5 GHz. The self resonance frequency of the produced tunable capacitor is at 9.5 GHz, and the quality factor is about 10 to 40 after 2 GHz. Nonetheless, at 1 GHz, the quality factor reaches 169 which is quite good.

Lee et al. also came up with a MEMS type surface micromachined tunable capacitor [35]. Their device can extend from 130 fF to 1.82 pF at 3 GHz by the application of a DC bias ranging from -30 V to 40 V. This result is very promising in terms of the range even though the required DC voltages are very large. Additionally, there was no information about the quality factor, self-resonance frequency and the frequency span in which the projected capacitance range can be covered.

Yoon et al. have developed a MEMS variable capacitor based on a electrically floating plate [36]. At 5 GHz, their T-type spring device yields 600 fF with no bias applied,

and with a 9 V bias, the resulting capacitance increases up to 900 fF. Nevertheless, the quality factor changes between 25 and 7, respectively, for these two conditions.

The most promising results came from Rijks et al. [31]. The self-resonance frequency of their tunable capacitor is 17.6 GHz which is quite high. Additionally, a quality factor greater than 50 has been achieved over the frequency range between 1 GHz and 6 GHz. The minimum capacitance they have is 230 fF. A tuning ratio of about 4.5 can be managed with their design setting so that the maximum capacitance extends to 1 pF. A DC bias of 12 V should be applied for this purpose which is less than the equivalents observed in previous designs.

All on-chip tunable capacitors have different qualifications which are very important considering the specifications needed for the design presented in this work. Nevertheless, none of them fully satisfies all constraints regarding the quality factor, DC bias, self-resonant frequency, tuning ratio and the minimum capacitance. However, the rate of progress is very big so if this trend will continue, the necessary list of qualifications for the design will be met in the near future. Finally, there is always the option employing the off-chip components however their problems with the layout and fabrication makes them undesirable for the radio frequency integrated circuit design (RFIC) that steadily favors the on-chip components.

CHAPTER 5

5 CONCLUSION AND FUTURE WORK

5.1 CONCLUSION

In this thesis, three main issues have been investigated. The first one basically deals with the theoretical analysis of the important design parameters R_{OPT} and X_{OPT}. These quantities are found approximately via a small signal circuit model based method. The capacitance C_μ has been incorporated to the analysis to see its effect on the calculated parameters. The derived equations have been plotted and the trend of the change in the sought quantities has been correctly anticipated over 1 GHz to 10 GHz interval. Nevertheless, the equations are composed of relatively complex expressions and their use will be limited to give an idea which terms of the expression will be dominant in the projected operation frequency. During the design procedure, these equations have been considered and simplified to yield basic formulas for the integrated circuit (IC) designers.

The second problem discussed in this work is the design procedure development for the tunable low noise amplifiers. A different topology has been assumed to satisfy the constraints of the low noise design. This topology consolidated the inductor L_c, which introduces the bias voltage to the core amplifier, with the matching circuit so that a π-network could be built. A π-network significantly reduced the inductor values which can be problematic when implemented with on-chip components. Moreover, a single series capacitor is more suitable for tunability than a series inductor since generally tunable

inductors are very difficult to realize and they incur bigger losses than variable capacitors. Two different LNAs working at 5 GHz have been presented to prove the validity of the proposed methodology one with ideal and the other with the realistic passive elements.

It can be argued that the design procedure is still based on a narrowband perspective. The tunability aspect of the design procedure lies in the easiness to switch to other frequencies by just changing the passive component values. This has been shown by constructing two further designs operating at 1 GHz and 10 GHz. As given in the results, if all reactive elements would be tunable, low noise design criteria can be accomplished without further modification of the device i.e. changing the emitter length as suggested in some other design methodologies.

The third topic handled in this work is the tunability aspect. The critical component for that is determined as the series capacitor in the input and output matching networks. Both designs containing ideal and realistic passive components have been investigated for the extent of the tunability of the noise and input matching. It has been found out that a bandwidth of 3 GHz can be spanned with a difference in NF and NF_{min} less than 0.5 dB and the S_{11} and S_{22} less than -10 dB via tunable capacitors which have quality factors greater than 100. Practical variable capacitors have problems with their quality factor at higher frequencies, need high DC activation voltages and possess low self-resonance frequencies. Nevertheless, the rapid development in MEMS based tunable capacitors forecasts that products that can meet the design specifications as determined in the tunability analysis will be finished with the current progress in near future.

Finally, it should be mentioned that even though the tunability experimentation is realized on a 5 GHz LNA, it could be tried with any narrowband LNA by applying the design procedure and finding the necessary tunable capacitance values for the desired operation frequencies.

5.2 FUTURE WORK

Future work is composed is of different tasks. One of them would be to deepen the theoretical part. Even though complicated expressions that can anticipate the trend in R_{OPT} and X_{OPT} have been are derived, expressions that give exact results should also be found. The possibility of simplifying them so that they become useful for IC design engineers constitutes another part of the possible research.

Like almost any other design procedure, this one does not address directly to the specifications on the linearity of the low noise amplifier. Thus, the simulated IIP3 values are to be improved. This can be achieved by means of cancellation techniques of the harmonics. The key point here is to preserve the input and noise match conditions since for low noise amplifiers these criteria are dominant over the linearity requirements.

Another possible future work might be to simulate tunable capacitors with associated models. This kind of analysis would be good to quantify the extra noise content that will be added by the tunable element. It will also be beneficial from the perspective of how much isolation is required between the core amplifier and the DC activation bias of the variable capacitor. However, to realize such a simulation, a cooperation with other researchers

specialized in MEMS type tunable capacitors and creating an associated SPICE modeling for these components are inevitable.

Finally, like any other electronic design, the circuits and tunable elements described should be manufactured and associated measurement results should be compared with the simulation outcomes.

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APPENDICES

Appendix A: Analysis of Input Impedance of the HBT LNA

The analyzed circuit has the following structure:

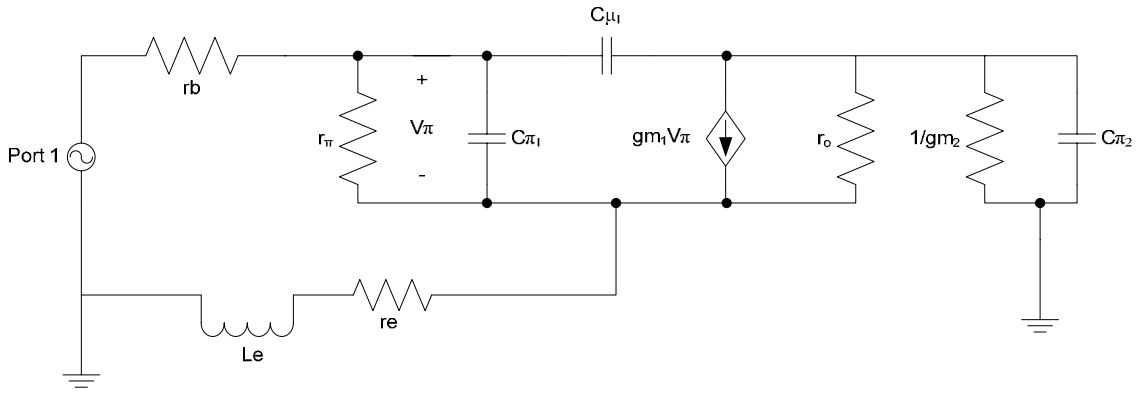

Figure 40: The small signal diagram for the cascode HBT LNA

This structure results in fairly complicated expressions during the mathematical analysis for the calculation of the input impedance. Thus, one has to make logical simplifications on the analyzed circuit to yield reasonable algebraic expressions. The first approach is to eliminate the parasitic resistances r_b and r_e. These are relatively small compared to the other terms, thus they won't affect the general impedance of the system. Another approximation is to eliminate the output resistance r_o. r_o is generally in the range of 5 to 10 kΩ, which reduces the leakage from the collector to the emitter. Thus, its effect is limited in the final expressions for the input impedance. Finally, an important simplification that will alter the nature of the derived expressions is to neglect the load at the collector due to the common gate transistor. The only interaction with these components and the core circuit is through C_μ which itself is very small compared to C_π. Thus, their contribution is scaled down considerably, and it is expected that the final expressions can still reflect the input impedance accurately.

After the approximations, the new circuit to analyze can be drawn as in Figure 41.

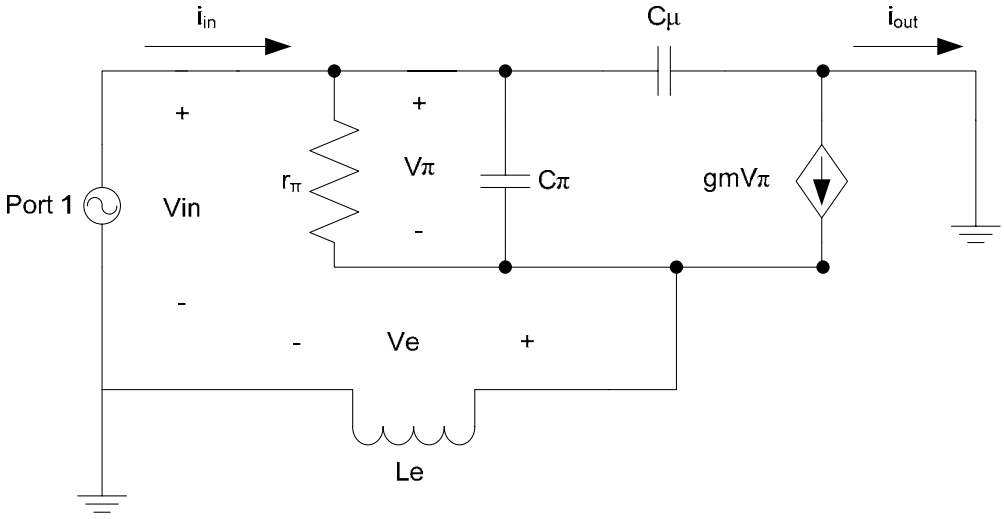

Figure 41: The simplified small signal diagram of the cascode HBT LNA

Based on Figure 41, one can begin to formulate the basic electrical engineering laws:

$$i_{in} = \frac{V_\pi}{r_\pi} + V_\pi j\omega C_\pi + V_{in} j\omega C_\mu \qquad \text{(App-A.1)}$$

$$\frac{V_\pi}{r_\pi} + V_\pi j\omega C_\pi + g_m V_\pi = \frac{V_e}{j\omega L_e} \qquad \text{(App-A.2)}$$

$$V_{in} = V_\pi + V_e \qquad \text{(App-A.3)}$$

From (App-A.2) and (App-A.3) together one can yield:

$$V_\pi j\omega L_e \left(\frac{1}{r_\pi} + j\omega C_\pi + g_m \right) = V_e \qquad \text{(App-A.4)}$$

$$V_{in} = V_\pi \left[j\omega L_e \left(\frac{1}{r_\pi} + j\omega C_\pi + g_m \right) + 1 \right] \qquad \text{(App-A.5)}$$

Using (App-A.5), it is possible to write:

$$i_{in} = \left\{ \frac{\left(\frac{1}{r_\pi} + j\omega C_\pi \right)}{\left[j\omega L_e \left(\frac{1}{r_\pi} + j\omega C_\pi + g_m \right) + 1 \right]} + j\omega C_\mu \right\} V_{in} \qquad \text{(App-A.6)}$$

By assuming $r_\pi << (1/g_m)$:

$$\frac{i_{in}}{V_{in}} \approx \left\{ \frac{\left(\frac{1}{r_\pi} + j\omega C_\pi \right) - \omega^2 C_\mu L_e g_m - j\omega^3 L_e C_\pi C_\mu}{\left[j\omega L_e \left(\frac{1}{r_\pi} + j\omega C_\pi + g_m \right) + 1 \right]} \right\} \qquad \text{(App-A.7)}$$

Furthermore, it can be assumed that $\omega^2 C\mu L_e << 1$:

$$\frac{i_{in}}{V_{in}} \approx \left\{ \frac{\left(\frac{1}{r_\pi} - \omega^2 C_\mu L_e g_m \right) + j\omega C_\pi}{\left[j\omega L_e \left(\frac{1}{r_\pi} + j\omega C_\pi + g_m \right) + 1 \right]} \right\} \qquad \text{(App-A.8)}$$

By some algebraic manipulations, following equations can be acquired:

$$\frac{V_{in}}{i_{in}} \approx \left\{ \frac{\left[j\omega L_e \left(\frac{1}{r_\pi} + j\omega C_\pi + g_m \right) + 1 \right]}{\left[\left(\frac{1}{r_\pi} - \omega^2 C_\mu L_e g_m \right) + j\omega C_\pi \right]} * \frac{\left[\left(\frac{1}{r_\pi} - \omega^2 C_\mu L_e g_m \right) - j\omega C_\pi \right]}{\left[\left(\frac{1}{r_\pi} - \omega^2 C_\mu L_e g_m \right) - j\omega C_\pi \right]} \right\} \qquad \text{(App-A.9)}$$

$$\frac{V_{in}}{i_{in}} \approx \left\{ \frac{\left[\left(1-\omega^2 L_e C_\pi\right)\left(\frac{1}{r_\pi}-\omega^2 C_\mu L_e g_m\right)+\omega^2 L_e C_\pi\left(\frac{1}{r_\pi}+g_m\right)\right] + \left[\left(\frac{1}{r_\pi}-\omega^2 C_\mu L_e g_m\right) j\omega L_e\left(\frac{1}{r_\pi}+g_m\right) - j\omega C_\pi\left(1-\omega^2 C_\pi L_e\right)\right]}{\left[\left(\frac{1}{r_\pi}-\omega^2 C_\mu L_e g_m\right)^2+\omega^2 C_\pi^2\right]} \right\} \quad \text{(App-A.10)}$$

If (App-A.10) can be algebraically analyzed, final results related to the input impedance can be formulated as in (App-A.11) and (App-A.12) which represent the real and imaginary input impedance respectively.

$$R_{in} = \mathrm{Re}\left(\frac{V_{in}}{i_{in}}\right) \approx \left\{ \frac{\left[r_\pi - \omega^2 r_\pi^2 C_\mu L_e g_m\left(1-\omega^2 L_e C_\pi\right)+\omega^2 r_\pi^2 L_e C_\pi g_m\right]}{\left[\left(1-\omega^2 C_\mu L_e g_m r_\pi\right)^2+\omega^2 r_\pi^2 C_\pi^2\right]} \right\} \quad \text{(App-A.11)}$$

$$X_{in} = \mathrm{Im}\left(\frac{V_{in}}{i_{in}}\right) \approx \left\{ \frac{\left\{\omega L_e\left[\left(1+g_m r_\pi+\omega^2 r_\pi^2 C_\pi^2\right)-\omega^2 g_m^2 r_\pi^2 L_e C_\mu\right]-\omega C_\pi r_\pi^2\right\}}{\left[\left(1-\omega^2 C_\mu L_e g_m r_\pi\right)^2+\omega^2 r_\pi^2 C_\pi^2\right]} \right\} \quad \text{(App-A.12)}$$

Appendix B: The Effect of L_c on the imaginary input impedance X_{in}

L_c is used to manipulate the input reactance X_{in} and optimum noise reactance X_{OPT} such that their magnitudes are brought to the same level. With the addition of L_c, the input reactance X_{in}, becomes X_{eqv}. The derivation of X_{eqv} can be quantified as below:

$$X_{eqv} = \mathrm{Im}\left(Z_{in}\right) = \mathrm{Im}\left[\, j\omega L_c \,\|\left(R_{in} + jX_{in}\right)\right] \tag{App-B.1}$$

$$X_{eqv} = \frac{j\omega L_c\left(R_{in} + jX_{in}\right)}{j\omega L_c + \left(R_{in} + jX_{in}\right)} = \frac{-\omega L_c X_{in} + j\omega R_{in} L_c}{R_{in} + j\left(X_{in} + \omega L_c\right)} * \frac{R_{in} - j\left(X_{in} + \omega L_c\right)}{R_{in} - j\left(X_{in} + \omega L_c\right)} \tag{App-B.2}$$

$$X_{eqv} = \mathrm{Im}\left[\frac{-\omega R L_c X + j\omega L_c X\left(X + \omega L_c\right) + j\omega R^2 L_c + \omega R L_c\left(X + \omega L_c\right)}{R^2 + \left(X + \omega L_c\right)^2}\right] \tag{App-B.3}$$

$$X_{eqv} = \mathrm{Im}\left[\frac{\omega^2 R L_c^2}{R^2 + \left(X + \omega L_c\right)^2} + j\frac{\omega L_c X\left(X + \omega L_c\right) + \omega R^2 L_c}{R^2 + \left(X + \omega L_c\right)^2}\right] \tag{App-B.4}$$

$$X_{eqv} = \omega\left[\frac{L_c X\left(X + \omega L_c\right) + R^2 L_c}{R^2 + \left(X + \omega L_c\right)^2}\right] \tag{App-B.5}$$

Appendix C: Detailed Calculation of the Optimum Noise Impedance for the Chosen Design Topology

First of all, the methodology to derive the optimum noise impedance components will be explained. Afterwards, the calculations are going to be provided.

The first step in the analysis would be to identify the noise components of a HBT. One crucial question at this point would be the effect of cascoding on the analyzed small signal model. It has been found out that the cascode transistor ideally does not add up any noise to the total noise content of the low noise amplifier [5]. However, this is not completely true because of the finite output resistance r_o. Still, in this analysis r_o will be neglected so the cascode transistor will be essentially ignored. The calculations here are meant to be an approximation of the trend in R_{OPT} and X_{OPT} rather than exact expressions. Basically, they will be used in the theoretical validation of the design procedure.

Figure 42 will be used as the baseline in the subsequent calculations.

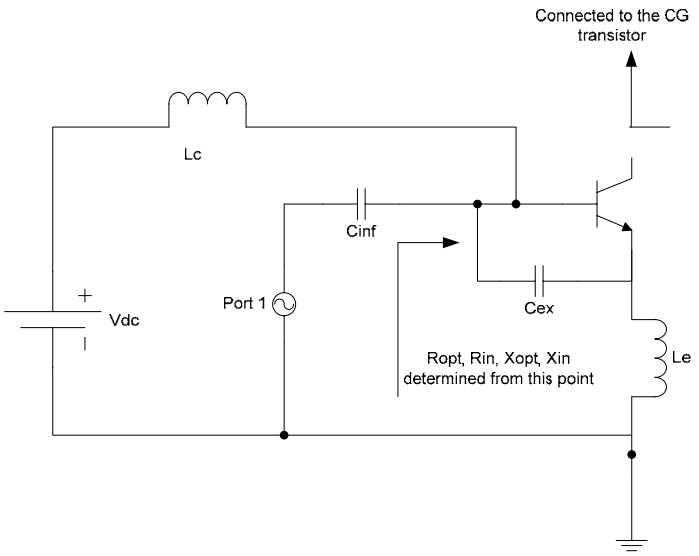

Figure 42: Simplified circuit structure of the input part of the cascode to determine Ropt, Rin, Xin, Xopt

The topology given in Figure 42 shows the basic strategy employed to reach the design targets. The reasons why this particular topology has been adopted is explained in Chapter 3.

Based on Figure 42 one has to modify Figure 2 so that additional components such as L_e and L_c can be introduced to the small signal diagram. The resulting small signal model can be visualized in Figure 43. The current directions determine the nature of the analysis for the optimum noise reactance. Since i_{in} is directed toward the device, the end result will give X_{OPT} rather than $X_{S,OPT}$.

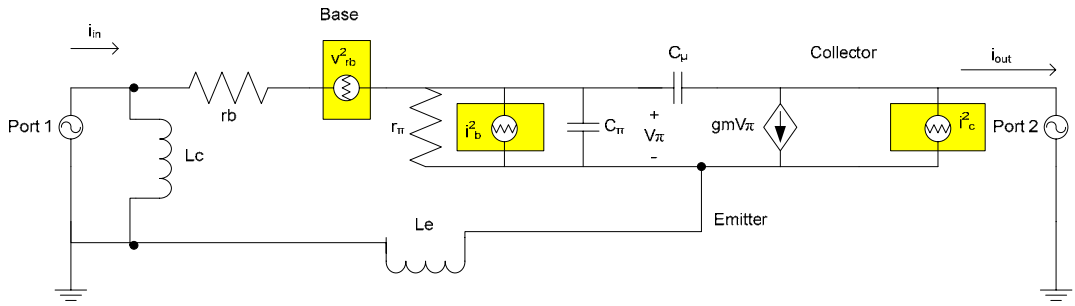

Figure 43: Small signal diagram for the noise analysis

Before beginning with the calculations, one should clarify the role of the bias inductor L_c. As will be discussed more detailed in the sections about the design of the matching network, L_c is a part of the π-network designated to match R_{OPT} to R_{in}. Thus, in the calculations and simulations of R_{OPT}, L_c will not be considered. However, for X_{OPT}, because L_c is a purely reactive component in shunt with the device, it will be incorporated for the calculations and simulations. In a sense, the π-network is broken into two parts for the imaginary components of the impedance matching process. The remaining high pass L-type matching network will resonate out fully X_{eqv} (the modified X_{in} through L_c as derived in Appendix B) and X_{OPT} since X_s is for this case 0 (Port 1 has a purely real resistance of 50 Ω).

The analysis will begin with giving explicit definitions of the noise sources. These are the base shot noise, collector shot noise and the base resistance thermal noise sources:

$$\overline{i_b}^2 = 2qI_b\Delta f \qquad \text{(App-C.1)}$$

$$\overline{i_c}^2 = 2qI_c\Delta f \qquad \text{(App-C.2)}$$

$$\overline{v}_{r_b}^2 = 4k_B T\Delta f\, r_b \qquad \text{(App-C.3)}$$

Afterwards, the output current noise source $\overline{i}_{out}^2$ will be calculated. For this purpose, one has to find the transfer function for the base shot noise source to the collector side.

$$i_{out} \cong g_m\left(\frac{1}{r_\pi} + j\omega C_{gs}\right)^{-1} i_{in} \qquad \text{(App-C.4)}$$

$$i_{out} = \frac{g_m r_\pi}{1 + j\omega r_\pi C_\pi} i_{in} = \left(\frac{g_m r_\pi}{1+\omega^2 r_\pi^2 C_\pi^2}\right)\left(1 - j\omega r_\pi C_\pi\right) i_{in} \qquad \text{(App-C.5)}$$

$$\left|\frac{i_{out}}{i_{in}}\right|^2 = \left(\frac{g_m^2 r_\pi^2}{1+\omega^2 r_\pi^2 C_\pi^2}\right) \qquad \text{(App-C.6)}$$

Next, the output current noise source can be computed using (App-C.6).

$$\overline{i}_{out}^2 = \overline{i}_c^2 + \overline{i}_b^2\left[\left|\frac{g_m r_\pi}{1+\omega^2 r_\pi^2 C_\pi^2} - j\frac{g_m \omega r_\pi^2 C_\pi}{1+\omega^2 r_\pi^2 C_\pi^2}\right|\right]^2 \qquad \text{(App-C.7)}$$

$$\overline{i}_{out}^2 = \overline{i}_c^2 + \overline{i}_b^2\left[\frac{\left(g_m r_\pi\right)^2}{\left(1+\omega^2 r_\pi^2 C_\pi^2\right)}\right] \qquad \text{(App-C.8)}$$

Now, the equivalent input voltage and current noise sources should be found. To achieve that, transfer functions that will connect the output current i_{out} with the input voltage v_{in} and i_{in} have to be derived. For the transfer function connecting i_{out} and v_{in}, the equations

that have been already derived in Appendix A could be utilized. First, by considering Figure 43, one can write:

$$i_{out} = V_{in} j\omega C_{\mu} - g_m V_{\pi} \qquad \text{(App-C.9)}$$

Then, using (App-A.4), (App-A.5) and (App-C.9), one can reach :

$$V_{\pi} = \frac{V_{in} j\omega C_{\mu} - i_{out}}{g_m} \qquad \text{(App-C.10)}$$

$$V_{in} = \frac{\left(V_{in} j\omega C_{\mu} - i_{out}\right)}{g_m}\left[j\omega L_e \left(\frac{1}{r_{\pi}} + j\omega C_{\pi} + g_m \right) + 1 \right] \qquad \text{(App-C.11)}$$

$$i_{out} = V_{in} \left\{ j\omega C_{\mu} - \frac{g_m}{\left[j\omega L_e \left(\frac{1}{r_{\pi}} + j\omega C_{\pi} + g_m \right) + 1 \right]} \right\} \qquad \text{(App-C.12)}$$

$$i_{out} = V_{in} \left\{ \frac{j\omega C_{\mu}\left[j\omega L_e \left(\frac{1}{r_{\pi}} + j\omega C_{\pi} + g_m \right) + 1 \right] - g_m}{\left[j\omega L_e \left(\frac{1}{r_{\pi}} + j\omega C_{\pi} + g_m \right) + 1 \right]} \right\} \qquad \text{(App-C.13)}$$

$$i_{out} = -V_{in} \left\{ \frac{g_m \left(1 + \omega^2 C_{\mu} L_e\right) - j\omega C_{\mu}\left(1 - \omega^2 C_{\pi} L_e\right)}{\left[j\omega L_e \left(\frac{1}{r_{\pi}} + j\omega C_{\pi} + g_m \right) + 1 \right]} \right\} \qquad \text{(App-C.14)}$$

$$\frac{V_{in}}{i_{out}} = -\left\{ \frac{\left(1 - \omega^2 C_{\pi} L_e\right) + j\omega L_e g_m}{g_m \left(1 + \omega^2 C_{\mu} L_e\right) - j\omega C_{\mu}\left(1 - \omega^2 C_{\pi} L_e\right)} \right\} \qquad \text{(App-C.15)}$$

$$\frac{V_{in}}{i_{out}} = -\left\{ \frac{\left[\left(1 - \omega^2 C_{\pi} L_e\right) + j\omega L_e g_m\right]\left[g_m \left(1 + \omega^2 C_{\mu} L_e\right) + j\omega C_{\mu}\left(1 - \omega^2 C_{\pi} L_e\right)\right]}{\left[g_m \left(1 + \omega^2 C_{\mu} L_e\right) - j\omega C_{\mu}\left(1 - \omega^2 C_{\pi} L_e\right)\right]} \right\} \qquad \text{(App-C.16)}$$

$$\frac{V_{in}}{i_{out}} = -\left\{ \begin{array}{l} \left[g_m\left(1+\omega^2 C_\mu L_e\right)\left(1-\omega^2 C_\pi L_e\right) - g_m\omega^2 L_e C_\mu\left(1-\omega^2 C_\pi L_e\right)\right] + \\ \dfrac{j\left[g_m^2\omega L_e\left(1+\omega^2 C_\mu L_e\right) + \omega C_\mu\left(1-\omega^2 C_\pi L_e\right)^2\right]}{\left[g_m\left(1+\omega^2 C_\mu L_e\right)\right]^2 + \left[\omega C_\mu\left(1-\omega^2 C_\pi L_e\right)\right]^2} \end{array} \right\} \quad \text{(App-C.17)}$$

$$\frac{V_{in}}{i_{out}} = -\left\{ \frac{\left[g_m\left(1-\omega^2 C_\pi L_e\right)\right] + j\left[g_m^2\omega L_e\left(1+\omega^2 C_\mu L_e\right) + j\omega C_\mu\left(1-\omega^2 C_\pi L_e\right)^2\right]}{\left[g_m\left(1+\omega^2 C_\mu L_e\right)\right]^2 + \left[\omega C_\mu\left(1-\omega^2 C_\pi L_e\right)\right]^2} \right\} \text{(App-C.18)}$$

The imaginary component of (App-C.18) is composed of two distinct terms however the first term is more dominant than the second one for the practical values of the associated variables. Thus, (App-C.18) can be rewritten as in (App-C.19):

$$\frac{V_{in}}{i_{out}} \approx -\left\{ \frac{\left(1-\omega^2 C_\pi L_e\right)}{g_m\left(1+\omega^2 C_\mu L_e\right)^2} + j\frac{\omega L_e g_m\left(1+\omega^2 C_\mu L_e\right)}{g_m\left(1+\omega^2 C_\mu L_e\right)^2} \right\} \quad \text{(App-C.19)}$$

$$\left|\frac{V_{in}}{i_{out}}\right|^2 \approx \left[\frac{\left(1-\omega^2 L_e C_\pi\right)^2 + \left[\omega L_e g_m\left(1+\omega^2 C_\mu L_e\right)\right]^2}{g_m^2\left(1+\omega^2 C_\mu L_e\right)^4} \right] \quad \text{(App-C.20)}$$

Next, the relation between i_{in} and i_{out} can be explored:

$$i_{in} = \frac{V_\pi}{r_\pi} + V_\pi j\omega C_\pi + V_\pi\left[j\omega L_e\left(\frac{1}{r_\pi} + j\omega C_\pi + g_m\right) + 1\right]\left(j\omega C_\mu + \frac{1}{j\omega L_c}\right) \quad \text{(App-C.21)}$$

$$i_{in} \approx V_\pi\left\{ \begin{array}{l} \left[\dfrac{1}{r_\pi} + g_m\left(\dfrac{L_e}{L_c}\right) - \omega^2 L_e C_\mu g_m\right] + \\ j\left[\omega C_\pi\left(1+\dfrac{L_e}{L_c}\right) - \omega^3 C_\pi C_\mu L_e + \omega C_\mu - \dfrac{1}{\omega L_c}\right] \end{array} \right\} \quad \text{(App-C.22)}$$

$$i_{out} = V_\pi \left[j\omega L_e \left(\frac{1}{r_\pi} + j\omega C_\pi + g_m \right) + 1 \right] j\omega C_\mu - g_m V_\pi \qquad \text{(App-C.23)}$$

$$i_{out} \approx -V_\pi \left[g_m \left(1 + \omega^2 C_\mu L_e \right) - j\omega C_\mu \left(1 - \omega^2 C_\pi L_e \right) \right] \qquad \text{(App-C.24)}$$

$$\frac{i_{in}}{i_{out}} = -\frac{\left[\begin{array}{l} \left(\frac{1}{r_\pi} + \left(\frac{L_e}{L_c} \right) g_m - \omega^2 L_e C_\mu g_m \right) + \\ j \left(\omega C_\pi \left(1 + \frac{L_e}{L_c} \right) + \omega C_\mu \left(1 - \omega^2 C_\pi L_e \right) - \frac{1}{\omega L_c} \right) \end{array} \right]}{\left[g_m \left(1 + \omega^2 C_\mu L_e \right) - j\omega C_\mu \left(1 - \omega^2 C_\pi L_e \right) \right]} \qquad \text{(App-C.25)}$$

$$\frac{i_{in}}{i_{out}} = -\left\{ \begin{array}{l} \left[\frac{\left(\frac{1}{r_\pi} + \left(\frac{L_e}{L_c} \right) g_m - \omega^2 L_e C_\mu g_m \right) \left(1 + \omega^2 C_\mu L_e \right)}{g_m \left(1 + \omega^2 C_\mu L_e \right)^2} \right] + \\ j \left[\frac{\left[\omega C_\mu + \omega C_\pi \left(1 + \frac{L_e}{L_c} \right) - \frac{1}{\omega L_c} \right]}{g_m \left(1 + \omega^2 C_\mu L_e \right)^2} \right] \end{array} \right\} \qquad \text{(App-C.26)}$$

$$\left| \frac{i_{in}}{i_{out}} \right|^2 = \left\{ \begin{array}{l} \left[\frac{\left(\frac{1}{r_\pi} + \left(\frac{L_e}{L_c} \right) g_m - \omega^2 L_e C_\mu g_m \right) \left(1 + \omega^2 C_\mu L_e \right)}{g_m \left(1 + \omega^2 C_\mu L_e \right)^2} \right]^2 + \\ \left[\frac{\left[\omega C_\mu + \omega C_\pi \left(1 + \frac{L_e}{L_c} \right) - \frac{1}{\omega L_c} \right]}{g_m \left(1 + \omega^2 C_\mu L_e \right)^2} \right]^2 \end{array} \right\} \qquad \text{(App-C.27)}$$

For the equivalent input voltage noise source, two different contributors exist. The first one is the thermal noise coming from the base resistance r_b. The other part is constituted

by the output current noise source. One detail should be not overlooked at this point. While calculating the equivalent input noise voltage the input port is shorted so that the base shot noise is eliminated. Thus, for this case, (App-C.8) should be rewritten as in (App-C.28).

$$\overline{i}_{out}^{2} = \overline{i}_{c}^{2} \qquad \text{(App-C.28)}$$

By using (App-C.20), and (App-C.28), the computations can be finalized as below:

$$\overline{v}_{in} = \overline{v}_{r_b} + \left\{ \frac{\left(1-\omega^2 C_\pi L_e\right) + j\omega L_e g_m \left(1+\omega^2 C_\mu L_e\right)}{g_m \left(1+\omega^2 C_\mu L_e\right)^2} \right\} \overline{i}_c \qquad \text{(App-C.29)}$$

$$\overline{v}_{in}^{2} = \overline{v}_{r_b}^{2} + \left\{ \frac{\left(1-\omega^2 L_e C_\pi\right)^2 + \left[\omega L_e g_m \left(1+\omega^2 C_\mu L_e\right)\right]^2}{g_m^2 \left(1+\omega^2 C_\mu L_e\right)^4} \right\} \overline{i}_c^{\,2} \qquad \text{(App-C.30)}$$

The equivalent input current noise source can be derived in an analogous manner. For this case, the input port is left open so that the thermal noise due to the base resistance is zeroed. Taking this fact into consideration, and also utilizing (App-C.8) and (App-C.27), following result can be acquired:

$$\overline{i}_{in} \approx \left\{ \begin{array}{l} \left\{ \dfrac{\left(\dfrac{1}{r_\pi} + \left(\dfrac{L_e}{L_c}\right) g_m - \omega^2 L_e C_\mu g_m\right)\left(1+\omega^2 C_\mu L_e\right) + j\left[\omega C_\mu + \omega C_\pi \left(1+\dfrac{L_e}{L_c}\right) - \dfrac{1}{\omega L_c}\right]}{g_m \left(1+\omega^2 C_\mu L_e\right)^2} \right\} \times \\ \left\{ \overline{i}_c + \overline{i}_b \left[\dfrac{g_m r_\pi \left(1 - j\omega r_\pi C_\pi\right)}{1+\omega^2 r_\pi^2 C_\pi^2} \right] \right\} \end{array} \right\}$$

(App-C.31)

$$\overline{i}_{in}^{2}=\left\{\begin{array}{l}\left\{\dfrac{\left[\left(\dfrac{1}{r_\pi}+\left(\dfrac{L_e}{L_c}\right)g_m-\omega^2L_eC_\mu g_m\right)\left(1+\omega^2C_\mu L_e\right)\right]^2+\left[\omega C_\mu+\omega C_\pi\left(1+\dfrac{L_e}{L_c}\right)-\dfrac{1}{\omega L_c}\right]^2}{g_m^2\left(1+\omega^2L_eC_\mu\right)^4}\right\}\times \\ \left\{\overline{i}_c^{\,2}+\overline{i}_b^{\,2}\left[\dfrac{\left(g_mr_\pi\right)^2}{\left(1+\omega^2r_\pi^2C_\pi^2\right)}\right]\right\}\end{array}\right\}$$

(App-C.32)

At this step, the theory presented in 2.4 will be helpful to determine the noise impedance parameters. Each element of the normalized chain matrix could be calculated with the expressions found in this appendix based on (2.20) and (App-C.1)-(App-C.3):

$$C_{A_{11}}=\frac{\overline{v}_{r_b}^{\,2}}{4k_BT\Delta f}+\left\{\frac{\left(1-\omega^2L_eC_\pi\right)^2+\left[\omega L_eg_m\left(1+\omega^2C_\mu L_e\right)\right]^2}{g_m^2\left(1+\omega^2C_\mu L_e\right)^4}\right\}\frac{\overline{i}_c^{\,2}}{4k_BT\Delta f} \qquad \text{(App-C.33)}$$

$$C_{A_{11}}=\frac{4k_BT\Delta f\,r_b}{4k_BT\Delta f}+\left\{\frac{\left(1-\omega^2L_eC_\pi\right)^2+\left[\omega L_eg_m\left(1+\omega^2C_\mu L_e\right)\right]^2}{g_m^2\left(1+\omega^2C_\mu L_e\right)^4}\right\}\frac{2qI_c\Delta f}{4k_BT\Delta f} \qquad \text{(App-C.34)}$$

$$C_{A_{11}}=r_b+\left\{\frac{\left(1-\omega^2L_eC_\pi\right)^2+\left[\omega L_eg_m\left(1+\omega^2C_\mu L_e\right)\right]^2}{g_m^2\left(1+\omega^2C_\mu L_e\right)^4}\right\}\frac{g_m}{2} \qquad \text{(App-C.35)}$$

$$C_{A_{22}} = \left\{ \begin{array}{l} \left\{ \dfrac{\left[\left(\dfrac{1}{r_\pi} + \left(\dfrac{L_e}{L_c} \right) g_m - \omega^2 L_e C_\mu g_m \right) \left(1 + \omega^2 C_\mu L_e \right) \right]^2 + \left[\omega C_\mu + \omega C_\pi \left(1 + \dfrac{L_e}{L_c} \right) - \dfrac{1}{\omega L_c} \right]^2}{g_m^2 \left(1 + \omega^2 L_e C_\mu \right)^4} \right\} \times \\ \left\{ \dfrac{\overline{i}_c^{\,2}}{4k_B T \Delta f} + \dfrac{\overline{i}_b^{\,2}}{4k_B T \Delta f} \left[\dfrac{\left(g_m r_\pi \right)^2}{\left(1 + \omega^2 r_\pi^2 C_\pi^2 \right)} \right] \right\} \end{array} \right\}$$

(App-C.36)

$$C_{A_{22}} = \left\{ \begin{array}{l} \left\{ \dfrac{\left[\left(\dfrac{1}{r_\pi} + \left(\dfrac{L_e}{L_c} \right) g_m - \omega^2 L_e C_\mu g_m \right) \left(1 + \omega^2 C_\mu L_e \right) \right]^2 + \left[\omega C_\mu + \omega C_\pi \left(1 + \dfrac{L_e}{L_c} \right) - \dfrac{1}{\omega L_c} \right]^2}{g_m^2 \left(1 + \omega^2 L_e C_\mu \right)^4} \right\} \times \\ \left(\dfrac{g_m}{2} \right) \left[1 + \dfrac{1}{\left(1 + \omega^2 r_\pi^2 C_\pi^2 \right)} \right] \end{array} \right\}$$

(App-C.37)

Calculating the correlation term, $C_{A,12}$ should be done with care. First of all, this term represents only the noise sources shared by the equivalent input and current noise sources. This definition indicates only to the collector shot noise source. The other noise sources are involved either in the equivalent input voltage or input current noise sources. Thus, the mathematical analysis for that can be designated as given below:

$$C_{A_{12}} = \frac{\overline{v}_{in}\, \overline{i}_{in}^{\,*}}{4k_B T \Delta f} \qquad \text{(App-C.38)}$$

$$\overline{v}_{in}\,\overline{i}_{in}^{*}=\left\{\begin{array}{l}\left\{\dfrac{\left(\dfrac{1}{r_\pi}+\left(\dfrac{L_e}{L_c}\right)g_m-\omega^2L_eC_\mu g_m\right)\left(1+\omega^2C_\mu L_e\right)-j\left[\omega C_\mu+\omega C_\pi\left(1+\dfrac{L_e}{L_c}\right)-\dfrac{1}{\omega L_c}\right]}{g_m\left(1+\omega^2C_\mu L_e\right)^2}\right\}\times \\ \left\{\left[\dfrac{\left(1-\omega^2C_\pi L_e\right)+j\omega L_e g_m\left(1+\omega^2C_\mu L_e\right)}{g_m\left(1+\omega^2C_\mu L_e\right)^2}\right]\overline{i}_c^{\,2}\right\}\end{array}\right\} \tag{App-C.39}$$

$$\overline{v}_{in}\,\overline{i}_{in}^{*}=\frac{1}{g_m^2\left(1+\omega^2L_eC_\mu\right)^4}\left\{\begin{array}{l}\left\{\left(\dfrac{1}{r_\pi}+\left(\dfrac{L_e}{L_c}\right)g_m-\omega^2L_eC_\mu g_m\right)\left(1+\omega^2C_\mu L_e\right)-\right. \\ \left.j\left[\omega C_\mu+\omega C_\pi\left(1+\dfrac{L_e}{L_c}\right)-\dfrac{1}{\omega L_c}\right]\right\} \\ \left\{\left[\left(1-\omega^2C_\pi L_e\right)+j\omega L_e g_m\left(1+\omega^2C_\mu L_e\right)\right]\overline{i}_c^{\,2}\right\}\end{array}\right. \tag{App-C.40}$$

$$C_{A_{12}}=\frac{1}{2g_m\left(1+\omega^2L_eC_\mu\right)^4}\left\{\begin{array}{l}\left\{\left(\dfrac{1}{r_\pi}+\left(\dfrac{L_e}{L_c}\right)g_m-\omega^2L_eC_\mu g_m\right)\left(1+\omega^2C_\mu L_e\right)-\right. \\ \left.j\left[\omega C_\mu+\omega C_\pi\left(1+\dfrac{L_e}{L_c}\right)-\dfrac{1}{\omega L_c}\right]\right\}\times \\ \left[\left(1-\omega^2C_\pi L_e\right)+j\omega L_e g_m\left(1+\omega^2C_\mu L_e\right)\right]\end{array}\right. \tag{App-C.41}$$

Using (2.23), the optimum noise susceptance B_{OPT} can be found from (App-C.41).

$$B_{OPT}=\frac{1}{2g_m\left(1+\omega^2L_eC_\mu\right)^4}\left\{\begin{array}{l}\left(\dfrac{1}{r_\pi}+\left(\dfrac{L_e}{L_c}\right)g_m-\omega^2L_eC_\mu g_m\right)\omega L_e g_m\left(1+\omega^2C_\mu L_e\right)^2- \\ \left[\omega C_\mu+\omega C_\pi\left(1+\dfrac{L_e}{L_c}\right)-\dfrac{1}{\omega L_c}\right]\left(1-\omega^2C_\pi L_e\right)\end{array}\right\} \tag{App-C.42}$$

So, the optimum noise reactance X_{OPT} could be reached at this point through (3.3). Also, as mentioned before, $B_{S,OPT}$ is the negative of B_{OPT}.

For G_{OPT}, it should be remembered that L_c effectively does not change its value at the base of the transistor. In other words, a pure shunt inductor at the base of the HBT only manipulates the optimum noise susceptance (or equivalently reactance). Thus, (App-C.37) and (App-C.41) should be modified as noted below:

$$C_{A_{22}} = \left\{ \left\{ \frac{\left[\left(\frac{1}{r_\pi} - \omega^2 L_e C_\mu g_m\right)\left(1+\omega^2 C_\mu L_e\right)\right]^2 + \left[\omega\left(C_\pi + C_\mu\right)\right]^2}{g_m^2\left(1+\omega^2 L_e C_\mu\right)^4} \right\} \times \left\{ \left(\frac{g_m}{2}\right)\left[1 + \frac{1}{\left(1+\omega^2 r_\pi^2 C_\pi^2\right)}\right] \right\} \right. \qquad \text{(App-C.43)}$$

$$C_{A_{12}} = \frac{1}{2g_m\left(1+\omega^2 L_e C_\mu\right)^4} \left\{ \left\{ \left(\frac{1}{r_\pi} - \omega^2 L_e C_\mu g_m\right)\left(1+\omega^2 C_\mu L_e\right) - j\left[\omega\left(C_\pi + C_\mu\right)\right] \right\} \times \left[\left(1-\omega^2 C_\pi L_e\right) + j\omega L_e g_m \left(1+\omega^2 C_\mu L_e\right) \right] \right\}$$

(App-C.44)

$$\mathrm{Im}\left(C_{A_{12}}\right) = \frac{1}{2g_m\left(1+\omega^2 L_e C_\mu\right)^4} \left\{ \omega L_e g_m \left(1+\omega^2 C_\mu L_e\right)^2 \left(\frac{1}{r_\pi} - \omega^2 L_e C_\mu g_m\right) - \omega\left(C_\pi + C_\mu\right)\left(1-\omega^2 C_\pi L_e\right) \right\}$$

(App-C.45)

Then, to finalize the analysis, (2.22) can be used:

$$G_{OPT} = \sqrt{\left\{\frac{\left\{\frac{\left[\left(\frac{1}{r_\pi}-\omega^2 L_e C_\mu g_m\right)\left(1+\omega^2 C_\mu L_e\right)\right]^2+\left[\omega\left(C_\pi+C_\mu\right)\right]^2}{g_m^2\left(1+\omega^2 L_e C_\mu\right)^4}\right\}\times\left\{\left(\frac{g_m}{2}\right)\left[1+\frac{1}{\left(1+\omega^2 r_\pi^2 C_\pi^2\right)}\right]\right\}}{r_b+\left\{\frac{\left(1-\omega^2 L_e C_\pi\right)^2+\left[\omega L_e g_m\left(1+\omega^2 C_\mu L_e\right)\right]^2}{g_m^2\left(1+\omega^2 C_\mu L_e\right)^4}\right\}\frac{g_m}{2}}-\left(\frac{\frac{1}{2g_m\left(1+\omega^2 L_e C_\mu\right)^4}\left\{\omega L_e g_m\left(1+\omega^2 C_\mu L_e\right)^2\left(\frac{1}{r_\pi}-\omega^2 L_e C_\mu g_m\right)-\omega\left(C_\pi+C_\mu\right)\left(1-\omega^2 C_\pi L_e\right)\right\}}{r_b+\left\{\frac{\left(1-\omega^2 L_e C_\pi\right)^2+\left[\omega L_e g_m\left(1+\omega^2 C_\mu L_e\right)\right]^2}{g_m^2\left(1+\omega^2 C_\mu L_e\right)^4}\right\}\frac{g_m}{2}}\right)^2\right\}} \quad \text{(App-C.46)}$$

The corresponding optimum noise input resistance R_{OPT} can be derived by making use of (3.4) and (App-C.46).

Appendix D: The reactance calculations in π-type matching network

The matching network in Figure 44 can be analyzed for its input impedance Z_{in} subsequently:

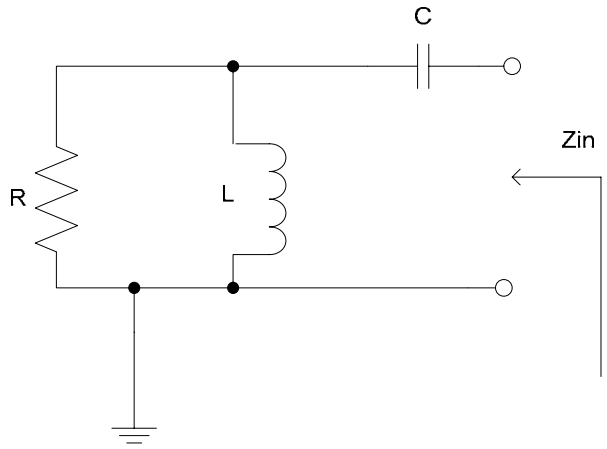

Figure 44: Basic L-type high-pass matching network

$$Z_{in} = \frac{1}{j\omega C} + \left(j\omega L \,||\, R \right) \qquad \text{(App-D.1)}$$

$$Z_{in} = \frac{1}{j\omega C} + \frac{j\omega RL}{R + j\omega L} = -\frac{j}{\omega C} + \frac{j\omega RL\left(R - j\omega L\right)}{R^2 + \omega^2 L^2} \qquad \text{(App-D.2)}$$

$$Z_{in} = j\left(\frac{\omega R^2 L}{R^2 + \omega^2 L^2} - \frac{1}{\omega C} \right) + \frac{\omega^2 L^2 R}{R^2 + \omega^2 L^2} \qquad \text{(App-D.3)}$$

Now using Figure 45 and the input reactance found in (App-D.3) as well as the relations (3.32)-(3.39), one can find the total reactance around R_h in the following manner:

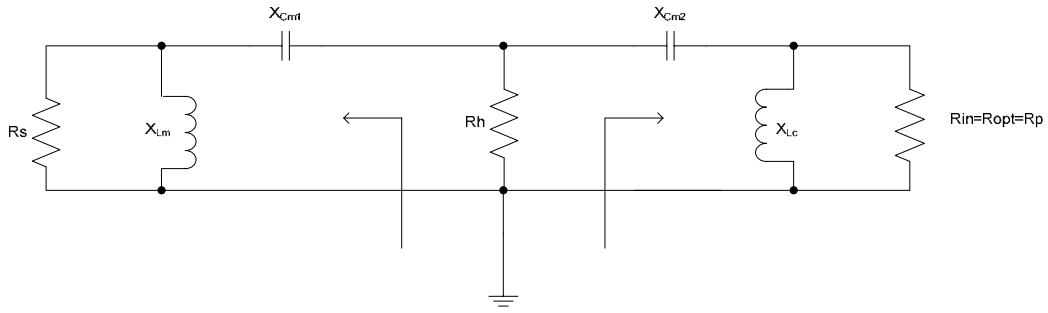

Figure 45: The circuit diagram to calculate the total reactance in a π-type matching network

$$X_{tot} = \frac{\omega R_s^2 L_m}{R_s^2 + \omega^2 L_m^2} - \frac{1}{\omega C_{m,1}} + \frac{\omega R_p^2 L_c}{R_p^2 + \omega^2 L_c^2} - \frac{1}{\omega C_{m,2}} \qquad \text{(App-D.4)}$$

$$X_{tot} = \frac{Q_L^2 X_{Lm}}{1+Q_L^2} - X_{Cm,1} + \frac{Q_R^2 X_{Lc}}{1+Q_R^2} - X_{Cm,2} \qquad \text{(App-D.5)}$$

$$X_{tot} = Q_L \frac{R_s}{1+Q_L^2}\frac{X_{Lm}}{X_{Lm}} - Q_L R_h + Q_R \frac{R_s}{1+Q_R^2}\frac{X_{Lc}}{X_{Lc}} - Q_R R_h \qquad \text{(App-D.6)}$$

$$X_{tot} = Q_L R_h - Q_L R_h + Q_R R_h - Q_R R_h = 0 \qquad \text{(App-D.7)}$$

As can be validated by (App-D.7), in a π-type matching network, all reactances are resonated out.