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(54) **VERSATILE SYSTEM FOR TRIPLE-GATED TRANSISTORS WITH ENGINEERED CORNERS**

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(52) **U.S. Cl.** **257/288; 257/320; 257/510**

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See application file for complete search history.

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(57) **ABSTRACT**

The present invention provides a system for producing a triple-gate transistor segment (300), utilizing a standard semiconductor substrate (302). The substrate has a plurality of isolation regions (304) formed along its upper surface in a distally separate relationship, defining a channel region (306). A form structure (308) is disposed atop the isolation regions, and defines a channel body area (310) over the channel region. A channel body structure (316) is disposed within the channel body area, and is engineered to provide a blunted corner or edge (318) along a perimeter of its upper exposed surface. The form structure is then removed, and subsequent processing is performed.

9 Claims, 2 Drawing Sheets

