ABSTRACT

Suh, YouSeok. ***Fabrication and evaluation of devices containing high K gate dielectrics and metal gate electrodes for the 70 and 50nm technology nodes of ITRS.*** (Under the direction of Dr. Veena Misra.)

This dissertation has focused on fabrication and characterization of alternative gate stacks consisting of high-K dielectrics and metal gates. This work has presented the evaluation of Ta based metals including Ta, TaN_x, and $TaSi_xN_y$ as gate electrodes for their potential use in NMOS devices.

For bulk CMOS devices, gate metals must have work functions that are near the conduction and valence band edges of Si. Although several metal gate electrodes have been identified for SiO_2 dielectrics based on their work function, thermal stability and carrier concentration, their compatibility with high-K dielectrics is not fully understood. The questions that need to be addressed include thermal stability of metals on high-K, work function values, Fermi level pinning and performance. In this work, we report on the characteristics of metal gate electrodes on SiO_2 and HfO_2-based dielectrics with respect to equivalent oxide thickness (EOT), flatband voltage (V_{FB}), leakage, work function and thermal stability.

The research indicated that the workfunction of $TaSi_xN_y$ is compatible with NMOS devices, provided the right composition is achieved. The improved stability of $TaSi_xN_y$ gates is attributed to the presence of Si and N in the gate electrode, which can improve the film microstructure and the diffusion barrier properties at the gate-dielectric interface. This stability of $TaSi_xN_y$ films may enable high-k dielectrics and metallic

electrode to be implemented in advanced CMOS devices. An equivalent oxide thickness of 11.2Å was obtained in $TaSi_xN_y$ /HfO_2/p-Si MOS capacitor, while maintaining low leakage current density of 4.1 x 10^{-2}A/cm^2 at Vg-V_{FB}=-1V in accumulation. A less EOT increase(~3 Å) was observed with $TaSi_xN_y$ gates compared to other gates (Ta, TaN_x, and Ru) due to the excellent oxygen barrier properties of $TaSi_xN_y$ gates, preventing oxygen diffusion into the dielectric through gate electrode and dielectric during annealing. It was observed that trapped charge was increased with nitrogen sputtering ambient and interface charge density was increased due to bombardment damage during gate metal sputtering. Further optimization to reduce oxide charges in the dielectric would be necessary for advanced metal gate/high-k technology.

Electrical characteristics of $TaSi_xN_y$ metal gate electrode on HfSiON/HfO_2 gate dielectrics for N-MOSFET structure were also investigated. Capacitance-voltage results indicated that no evidence of gate-depletion with the introduction of $TaSi_xN_y$ metal gates. Reasonable output MOSFET characteristics such as Ids-Vgs, Ids-Vds, and Subthreshold swing, were obtained. However, degraded mobility characteristics were observed and were attributed to additional scattering mechanisms by trapped charges and interface charges in HfSiON/HfO_2 dielectrics. A reduction in these charges is necessary to understand the intrinsic limitation of carrier mobility at Si-High-K dielectric interfaces.

FABRICATION AND EVALUATION OF DEVICES CONTAINING HIGH K GATE DIELECTRICS AND METAL GATE ELECTRODES FOR THE 70 AND 50NM TECHNOLOGY NODES OF ITRS.

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Biography

YouSeok Suh received the B. S. and M. S. degree in Material Science and Engineering from Korea University, Seoul, Korea in 1995 and 1997 respectively. Form 1997 to 2000, he was with Memory R & D division of Hyundai Electronic Ind. Co. Korea as a research staff. He worked on the gate stack process for 0.13 um DRAM technology. Other research projects included the process development of PVD Ta/TaN barrier metal for Cu interconnections and the process of Ti-Salicide for logic devices. Since 2000, he has been pursuing Ph. D. degree in the Department of Electrical and Computer Engineering at North Carolina State University. Under the guidance of Dr. Veena Misra, he has developed a greater understanding of microelectronics devices and advanced technology. He have developed and optimized TaSiN metal gate electrode for NMOS application. His current research interests are high K gate dielectrics and metal gate electrodes for advanced CMOS process.

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CHAPTER 1

Introduction

1.1 Scaling issues with MOSFET

Aggressive scaling of CMOS devices has enabled high speed operation and high density today's chips. However we are rapidly reaching a fundamental limit with respect to obtaining benefits of transistor scaling. The 2001 edition of the International Technology Roadmap for Semiconductors (ITRS) calls for more rapid scaling than previously anticipated. Semiconductor chips with feature sizes nodes of 0.18 μm (180 nm) with 0.13 μm (130 nm) technologies are just beginning to reach the marketplace and plans are in the place to deliver 90 nm technologies [1]. Table 1 shows the equivalent physical gate oxide thickness for high performance as a function of technology node. There are a number of issues associated with the continued MOSFET scaling for sub 100 nm technology nodes. When the physical thickness of SiO_2 is scaled down below 1.5 nm, gate leakage current increases rapidly due to direct tunneling. Boron penetration effect also becomes significant for PMOSFETs [2]. While the actual scaling limit of SiO_2 is still under debate [3], research on the high-k dielectrics has been expanded significantly and the continued scaling of MOSFET will eventually require replacing the SiO_2 with an alternate high dielectric constant (high-k) material [4-7].

1.2 Alternative high k dielectrics

As the thickness of SiO_2 approaches below 1.5 nm, the leakage current increases significantly due to direct tunneling. The high leakage current degrades the circuit performance such as standby power, reliability, operation speed, and noise margin of CMOS inverter. Therefore, to reduce gate dielectric leakage current while keeping the same equivalent oxide thickness, a thicker film with a high dielectric constant (k) is required.

Alternative high-k dielectrics must have high dielectric constants, high barrier heights for both electrons and holes, low interface state densities and low fixed charges. They should also be thermodynamically stable on Si. Many high dielectric constant materials have recently been reported that could potentially replace SiO_2. Table 2 shows the key properties of alternative high-k dielectric candidates that are currently under investigation.

Dielectrics such as CeO_2, Y_2O_3 and Al_2O_3 do not provide significant advantages over SiO_2 or Si_3N_4 because of their relatively low dielectric constants [8-11]. On the other hand, high-K materials such as $SrTiO_3$ and $BaSrTiO_3$, have very high dielectric constants but also suffer from very small band gaps [12]. Other high-k materials such as Ta_2O_5 and TiO_2 are thermally unstable when directly contact with silicon and also have low barrier heights [13].

Due to their high dielectric constant, large barrier offsets with Si, and thermal-chemical stability with Si, Hf and Zr metal oxides and their silicates are currently considered the most promising candidates for alternative high-k dielectric applications. It was reported that both HfO_2 and ZrO_2 films have promising characteristics such as low leakage current, good interface properties (D_{it} ~10^{11}/eVcm^{-2}), and excellent reliability properties [14-16, 19]. However, it has been shown that most deposition techniques used to deposit ZrO_2 and HfO_2 result in a SiO_2 interfacial layer after high temperature processing due to the well-known fast diffusion of oxygen through ZrO_2 and HfO_2. In this case, oxygen, which diffuses through these metal oxides, reacts with Si substrate at the interface to form an uncontrolled interfacial layer. Under optimized processing conditions, it was reported that the contribution from the interfacial layer is EOT = 5Å, although a significant level of interface states are still apparent in the capacitance-voltage curves at low frequencies. Negligible hysteresis was reported for certain processing conditions, but a relatively high ΔV_{FB} value of + 600 mV was reported in one case [15], and - 300 mV was reported in another [14], with slightly different processing conditions. These significant flatband shifts perhaps arise from a large amount of negative fixed charge (for positive ΔV_{FB}) and positive fixed charge (for negative ΔV_{FB}), respectively, in the films. Both ZrO_2 and HfO_2 tend to crystallize at low temperatures leading to polycrystalline films with high leakage paths along grain boundaries and non-uniformities in ε values and film thickness. Polycrystalline gate dielectric films will most likely have higher leakage current, be less uniform and less reproducible than amorphous films. However, since polycrystalline films have provided reasonable results, the correlation between gate dielectric morphology and device performance requires further investigation.

Gate electrodes combined with these alternative dielectrics have also been investigated. It was reported that polysilicon deposition at higher temperatures (620°C) results in reduction of ZrO_2 to form a Zr-rich layer near the polysilicon-ZrO_2 interface, leading to very high leakage currents [19]. Also, polysilicon gate on HfO_2 have shown formation of interfacial layers (hafnium silicate~5Å) during poly deposition at 625°C [18]. MOSCAP and MOSFET using ZrO_2 and HfO_2 gate dielectric deposited directly on

Si have shown EOT as low as 11.3Å and 12.0Å respectively [18,19]. Capacitors using platinum gate electrode have demonstrated low leakage, negligible frequency dispersion, interface state density less than $10^{11}eV^{-1}cm^{-2}$, and excellent reliability characteristics. However, in both HfO_2 and ZrO_2 dielectric, a significant increase in EOT after the samples underwent a 800°C annealing was observed, which was attributed to the consumption of oxygen coming from the annealing ambient through the oxygen-transparent platinum gate electrode.

1.3 Alternative gate electrodes

As gate oxide thickness decreases, the capacitance associated with the depleted layer at the poly-Si/gate dielectric interface becomes significant, making it necessary to consider alternative gate electrodes [20]. The search for metallic gates faces many challenges since they must have compatible work functions, thermal/chemical interface stability with underlying dielectric and high carrier concentration.

Polysilicon gate has the advantage that it can be doped p-type or n-type, shifting the work function so that it is suitable for NMOS and PMOS devices, thereby simplifying integration. However, many of the new dielectric materials are unstable in direct contact with silicon and the polysilicon material [21]. Metal gate replacements must be chosen based on their workfunction values. Figure 1 shows energy diagrams of threshold voltage for NMOS and PMOS devices using midgap metal gates and dual metal gates. A midgap work function metal gate shifts the threshold voltage higher by half the bandgap (about 0.5 V) compared to a highly doped polysilicon gate electrode. If the channel doping is lowered to provide a suitable lower threshold voltage, then the channel doping is too low to control short-channel effects. For this reason, two different gate metals are required with work functions near E_c and E_v [22]. There are several NMOS candidate metals with work functions near 4 eV such as Al, Ta, Mo, Zr, Hf, V, Ti and several metals with work functions near 5 eV such as Co, Pd, Ni, Re, Ir, Ru, Pt for PMOS. The diagram in Figure 2 shows the work function of the common metals in the silicon band gap. There are also several conducting metal oxides such as In_2O_3, SnO_2, OsO_2, RuO_2, IrO_2, ZnO, MoO_2, ReO_2, and conducting metal nitrides such as WN_x, TiN_x, MoN_x, TaN_x, $TaSi_xN_y$.

Recently, polysilicon gates have shown to suffer from Fermi level pinning on High-K dielectrics [23]. It was reported that Fermi pinning is a fundamental characteristic of the polySi/MeO_x interface and causes high threshold voltages in MOSFET devices. For Hf-based materials, the interfacial Si-Hf bonds are believed to be the main mechanism that creates dipoles. This dipole pins the Fermi level just below the poly-Si conduction band and increases the threshold voltage of p-doped gates. This warrants the investigation of metallic gate electrodes on high-k dielectrics.

Thermal and chemical stability is one of the most important issues for metal gate electrodes. Metal gates should be able to survive device processing temperature and must be stable with respect to the underlying gate dielectric. Unfortunately, most known metal gate electrodes suffer from high temperature instability resulting in a degraded interface with the underlying dielectric [24-25]. Many elemental metals form silicides on dielectrics after high temperature annealing if the dielectrics contain SiO_2. Several thermal and chemical instabilities have been observed when these metals are placed on alternate dielectrics as well as SiO_2. Any reaction or intermixing at electrode/dielectric interface will make the issue more complicated due to the unpredictable modification of work function and equivalent physical oxide thickness (EOT). Several material properties, such as free energy of oxide formation, oxygen solubility, diffusion-barrier properties, and film microstructure, can be used as predictors of stability. Since electronegativity, which is related to free energy of formation, is proportional to work function, elemental metals with lower work functions (*n*-channel MOS-compatible, also called NMOS compatible) have problems with stability due to high electronegativity. Therefore, one of the main challenges lies in finding low-work-function metals with good thermal stability [26]. On the other hand elemental metals with higher work functions provide intrinsic stability due to their low free energy of formation (low electronegativity). However, high work-function metals may suffer from adhesion issues.

1.4 Characterization methods for advanced gate stack

Electrical properties such as dielectric constant, leakage current density, interface trap and oxide trapped charge, dielectric integrity, and reliability are all critical issues for the development of advanced gate stacks. For over 30 years, electrical characterization techniques including capacitance-voltage (C-V) and current-voltage (I-V) have been instrumental in the achievement of high yield and high reliability ICs. C-V and I-V analysis were performed on MOS capacitors and transistors to obtain parameters such as oxide thickness, oxide charges, flatband voltage, threshold voltage, mobility values, sub-threshold properties, average interface trap density, as well as reliability parameters such as charge to breakdown, and time to breakdown. However, the accuracy of C-V measurement for extremely thin dielectric is degraded due to excessive leakage current. The gate electrode can also directly impact these parameters. Analysis of a measured C-V curve needs to be modified to obtain accurate dielectric properties such as EOT. It requires consideration of equivalent circuit model effect such as oxide leakage, series resistance, backside contact, and stray inductance, etc. It also needs correction to account for the impact of quantum mechanical effects. All these issues need to be re-visited for alternative gate stacks [27-30].

In order to measure the workfunction , it is necessary to use varying thicknesses of the dielectric. Figure 3 shows the V_{FB} vs. EOT plot in which the y-intercept indicates the workfunction,Φ_m. ($V_{FB} = \Phi_m - \Phi_s - Q_f\ t_{ox}/\varepsilon_{ox}$). Varying dielectric thicknesses are needed in order to decouple the fixed charge from the work function. Fowler-Nordheim current analysis can also be performed to determine the barrier height at the metal-oxide interface and correlate with C-V measurements. Figure 4 shows the energy band diagram of $TaSi_xN_y/SiO_2$/p-Si capacitor with a negative bias applied to the metal electrode. The current in this structure will be due either to Schottky emission of electrons over the barrier or to Fowler–Nordheim tunneling of electrons through the triangular barrier into the oxide conduction band [31-33]. At room temperature, emission of the electrons is not expected to occur because of the high barrier height and therefore Fowler-Nordheim conduction will dominate. The surface potential of the silicon substrate is neglected under accumulation conditions. The Fowler–Nordheim current is given by $J_{FN} = A\ E_{ox}^2 \exp[-B/E_{ox}]$. The parameter A and B depend on the barrier height (Φ_b) and the effective mass of the tunneling electron m_{ox}. The barrier height values can then be correlated to the work function values extracted from CV analysis. It should be noted that Fowler-Nordheim current method can extract barrier height from one sample with thick dielectric thickness, however, it can produce errors in thin dielectrics since the current may be a critical function of process damage, defects, and metal diffusion.

1.5 Recent research on metal gate electrodes

For sub-100nm gate length, Al/TiN or W/TiN metal gate nMOSFETs with 1.5-3 nm SiO_2 and Si_3N_4 was demonstrated using a replacement gate process [34]. This process allows the temperatures following metal gate definition to be limited to 450°C. It also demonstrated the feasibility of using W/TiN as a metal-electrode on SiO_2 and Si_3N_4 (<33 Å) [35]. Capacitance –voltage (C-V) characteristics indicated good Si/SiO_2 interface quality without any gate depletion. The flat band voltage of the TiN indicated a work function value near 4.7 ~ 4.8 eV. Nakajima et al. reported the deviation of the crystal orientation of the metal electrode can cause a deviation of flat band voltage [36]. They found CVD-TiN film displayed better MOS characteristics due to lower metal penetration and extremely uniform flat band voltage due to highly preferred orientation of TiN film. Yamada et al. investigated the effect of surface nitridation in W/WN_x/SiON/Si gate MOS capacitor [37]. It was reported the termination of the dangling bonds in the gate dielectric due to surface nitridation improved the dielectric reliability. It also confirmed the WN_x gate electrodes have the nearly mid-gap work function values. Metal gates such as TiN and Pt have been most commonly used with the high- k gate dielectrics to prevent reactions at the gate interface.

As has mentioned before, the workfunction of gate electrodes is a very critical parameter. A significant advantage of employing a midgap metal arises from a symmetrical V_T value for both NMOS and PMOS, because by definition the same energy difference exists between the metal Fermi level and the conduction and valence bands of Si. This can afford a simpler CMOS processing scheme, since only one mask and one metal would be required for the gate electrode. However, for scaled CMOS devices, a major drawback of midgap metals is that since the band gap of Si is fixed at 1.1 eV, the threshold voltage for any midgap metal on Si will be 0.5 V for both NMOS and PMOS. Since voltage supplies are expected to be <1.0 V for sub-0.13 μm CMOS technology, a V_T of 0.5V is much too large, as it would be difficult to turn on the device. Lowering of the V_T would require a lowering of the doping concentration, which would degrade the short channel characteristics. Therefore, ideal situation calls for two metals with dual workfunction: 4eV for NMOS and 5eV for PMOS. This will enable low threshold voltages without degraded short channel effects. For example, the work function value of Al could produce a V_T of 0.2V for NMOS, while the higher work function value of Pt could achieve V_T (0.2V) for PMOS.

For NMOS gate electrodes, Al is not a feasible electrode metal because it will reduce nearly any oxide gate dielectric to form an Al_2O_3-containing interface layer and also has a low melting temperature. Hf and Zr gate electrodes on SiO_2, $ZrSi_xO_y$, and ZrO_2 have also been evaluated as alternative gate electrodes [38]. A large reduction in the SiO_2 equivalent oxide thickness accompanied by an increase in the leakage current was observed with Hf and Zr electrodes when subjected to anneal temperatures as low as 400°C due to the combination of physical thinning of the SiO_2 and formation of a high-k layer. A severe instability of Zr and Hf electrodes was also observed on $ZrSi_xO_y$ and ZrO_2 dielectrics. It was attributed to thermal instability owing to their high affinity for metal oxide formation, resulting in the reduction of the gate dielectric and subsequent oxygen diffusion to the gate electrode.

The characteristics of MOSFET using TaN gate electrode and HfO_2 dielectric were investigated by Lee et al. [39]. Using TaN electrodes, the gate dielectric thickness of MOSFET with HfO_2 was scaled down to 11 Å with very low leakage current even after conventional high temperature CMOS process. The resistivity of stoichiometric TaN was low (~200 μΩcm) and the reported work function was 4.15 eV. However, it should be pointed out that there is a large discrepancy in the reported value of TaN work function values.

We have recently reported that $TaSi_xN_y$ films on SiO_2 provide work function (4.2 ~ 4.4eV) compatible with NMOS devices and good thermal stability up to 1000ºC resulting in minimal change of EOT, while demonstrating low leakage current [40]. The improved stability of $TaSi_xN_y$ gates is attributed to the presence of Si and N in the gate electrode, which can improve the film microstructure and the diffusion barrier properties at the gate-dielectric interface. Park et al. studied ternary metal nitride gates such as $Ti_{1-x}Al_xN_y$ (TiAlN) on high-k gate dielectrics (ZrO_2, HfO_2) annealed up to 950°C [41]. They found that stoichiometric TiAlN (y~1) exhibited highly robust p-type gate electrode (p-TiAlN) properties, demonstrating the work function of ~5.1 eV and excellent gate oxide integrity against the thermal budget of conventional Si CMOS process. The N-deficient TiAlN (y < 1) had work function compatible with n-type electrodes (n-TiAlN), however with limited thermal stability.

For PMOS gate electrodes, Pt is not a practical choice for the gate metal since it (a) conducts oxygen, (b) does not adhere well to most dielectrics, (c) is difficult to etch, and (d) is expensive. Other elemental metals with high work function values such as Au are also not practical, for the same reasons as for Pt. Lu et al. investigated Mo metal gate with high-k gate dielectrics [42]. They reported a suitable PMOSFET work function with good device characteristics. It was also reported that with nitrogen implantation, the work function of Mo could be lowered so as to be suitable for NMOSFETs. This was attributed to the dependence of the gate work function on the bulk metal microstructure, metal/dielectric interface chemistry, and even gate–dielectric properties. Consequently, the metal work function value will depend on deposition and anneal conditions, as well as the dielectric underneath. They also fabricated dual metal gate CMOS devices on Si_3N_4 (EOT=9Å) dielectric using Ti and Mo for the N- and P- MOSFET respectively [43]. They reported the work function was 4.72 eV for Mo and 4.56 eV for Ti. The higher work function of Ti was attributed to the formation of TiN layer from Ti and Si_3N_4 during high temperature annealing. Zhong et al. studied the electrical and thermal stability of Ru and RuO_2 electrodes on ZrO_2 and Zr-silicate dielectrics [44-45]. Their low resistivity of 65 μΩcm, excellent thermal stability of EOT, and a work function of 5.1 eV, make them suitable candidates for P-MOS devices. Kim et al. reported the physical and electrical properties of CVD TaN as a gate material for sub 100nm MOS devices [46]. Compared to PVD TaN, CVD TaN gate electrode showed higher work functions (~5 eV) for PMOS devices, excellent stability of gate oxide thickness, leakage current, and interface properties during high temperature annealing and reliability. They reported that the difference in work function between PVD TaN and CVD TaN may be attributed to the crystal orientation, the concentration of impurities such as oxygen and carbon in the film, and plasma induced oxide charges in PVD films. The metal-dielectric compatibility and thermal stability of Ir and IrO on HfO_2 as candidate metals for PMOS is currently under investigation [47].

Polishchuk et al. proposed a new metal-gate CMOS technology that is depositing a stack consisting of two metals, followed by metal interdiffusion to achieve low threshold voltages for both n- and p-MOSFET's. It was demonstrated that interdiffusion of Ti-Ni metal stacks produces gate electrodes with 3.9 eV and 5.3 eV work functions for n-MOS and p-MOS devices respectively [48].

Binary metal alloys of Ru and Ta as candidates for CMOS gate electrodes have also been recently reported [49]. It was reported that Ru-Ta alloys are excellent NMOS gate electrode candidates since they exhibit low work functions and demonstrate superior thermal stability compared to Ta. These metal alloys also offer workfunction tuning capability. Moreover, by increasing the Ru concentration of this alloy, excellent PMOS gate characteristics were achieved. Intermixed stack of Ru and Ta have been investigated as a route to obtaining ease of integration [50]

Metal gates promise to solve several issues such as poly gate electrode depletion effects, boron penetration, stability with alternate high-K dielectrics, and decreased gate resistance as devices are scaled down further. For alternative metal gate electrode, in addition to the work-function requirements, the metal gate and the high-k gate dielectric should be mutually compatible and not inter-diffuse or react at the MOSFET thermal budget.

1.6 Overview of dissertation

The focus of this dissertation is on the fabrication and characterization of alternative gate stacks consisting of high-K dielectrics and metal gates. This work will provide evaluation of Ta based metals, such as Ta, TaN_x, and $TaSi_xN_y$ as gate electrodes for their potential use in NMOS devices. Then metal gates will be evaluated on HfO2 dielectrics. Following the introduction chapter, chapter 2 provides a literature review of $TaSi_xN_y$ films and material characterization of $TaSi_xN_y$ films. Chapter 3 presents an in-depth study about characteristics of $TaSi_xN_y$/ SiO_2/ Si structures. Specifically, the role of the Si and N content on the electrical properties will be discussed in chapter 4. Chapter 5 describes electrical characteristics of metal gate electrode, including Ru and Ta-based metal gates, on HfO_2 dielectrics. Finally, device characteristics in NMOSFET devices of $TaSi_xN_y$ on Hf based based dielectrics stacks will be described in chapter 6. A summary and suggestion for future work will be presented in Chapter 7.

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Year	2001	2002	2003	2004	2005	2006	2007
Technology node (nm)	130	115	110	90	80	70	65
T_{ox} (nm)	**1.3-1.6**	**1.2-1.5**	**1.1-1.6**	**0.9-1.4**	**0.8-1.3**	**0.7-1.2**	**0.6-1.1**

Table 1. Equivalent physical gate oxide thickness with technology node for high performance (HP) in 2001 ITRS road map

Material	SiO_2	Si_3N_4	Ta_2O_5	TiO_2	Al_2O_3	Zr–Al–Si–O	ZrO_2	$ZrO_2 : Y_2O_3$	HfO_2	$ZrSiO_4$	$HfSiO_4$
κ	3.9	7	26	80	9	3–29	25	29.7	18–40	12.6	13
Band gap (eV)	8.9	5.1	4.5	3.5	8.7		7.8		5.7	6	6
ΔE_c/Si(eV)	3.3	2	1–1.5	1.2	2.8^a		1.4^a		1.5^a	1.5^a	
Notice								Epitaxy			

Material	La_2O_3	CeO_2	Pr_2O_3	Gd_2O_3	Y_2O_3	$SrTiO_3$	$PbTiO_3$	$PbZrO_3$	$CoTiO_3$	$BaSrTiO_3$	$LaAlO_3$
κ	30	26–16.6	14.9	13.6	15–18	150–250	1000		40–45	300	25.1
Band gap (eV)	4.3				5.6	3.3	3.4	3.7			
ΔE_c/Si(eV)	2.3				1.3^a	-0.1^a				-0.1	
Notice		Epi.		Epi.	Epi.	Epi.					

ΔE_c/Si (eV): energy offset between the dielectric and silicon conduction bands.
[a] Calculated by Robertson [9].

Table 2. Properties of alternative high-k materials

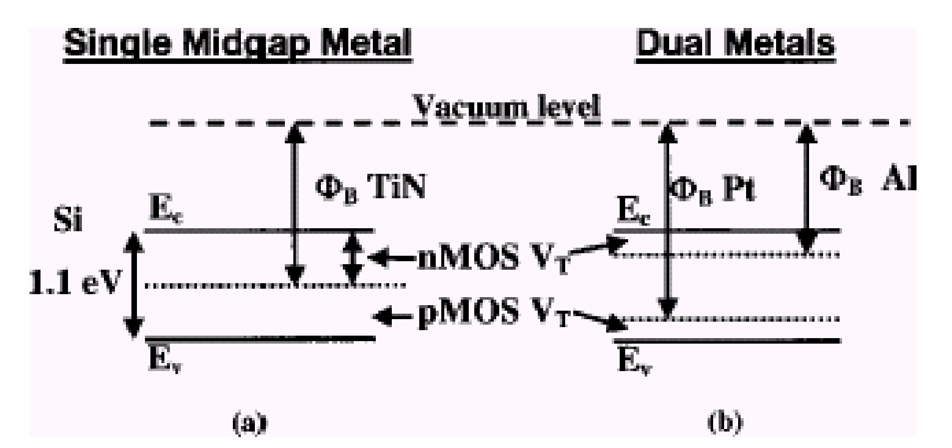

Figure 1. Energy diagrams of threshold voltage for NMOS and PMOS devices using midgap metal gates and dual metal gates.

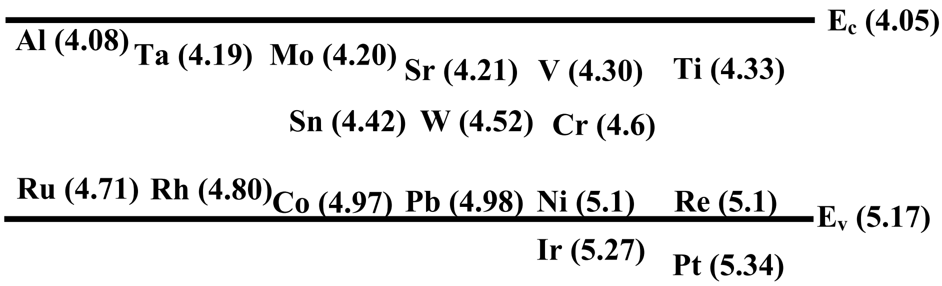

Figure 2. Work function of possible metal gates

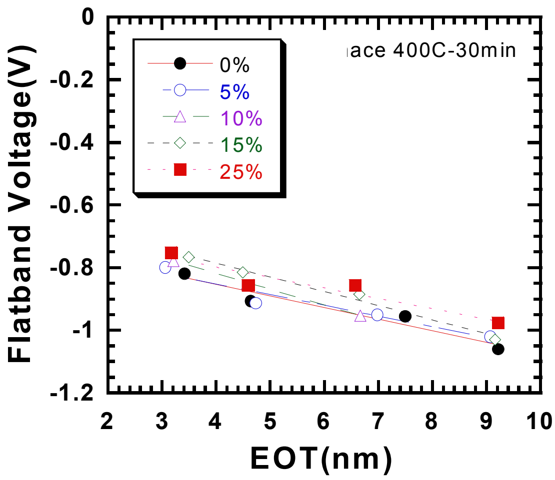

Figure 3. The Flat band voltage as a function of equivalent oxide thickness at the various $TaSi_xN_y$ electrodes.

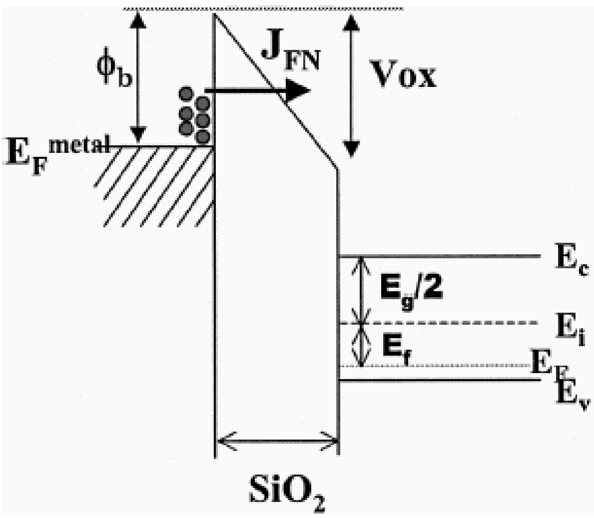

Figure 4. Energy diagram of $TaSi_xN_y$ /SiO2/p-Si structures for Fowler-Nordheim tunneling.

CHAPTER 2

Material Properties of $TaSi_xN_y$ thin films

This two-part chapter will discuss the material properties of $TaSi_xN_y$ in terms of bonding, diffusion barrier properties and microstructure. These properties will then be correlated to the feasibility of using $TaSi_xN_y$ as a gate metal electrode. The first part of this chapter will review the literature on the material properties of $TaSi_xN_y$. The second part of this chapter will present our experimental results on $TaSi_xN_y$ films as NMOS compatible gate electrodes.

2.1 Literature review: Properties of $TaSi_xN_y$ thin films

$TaSi_xN_y$ films have been studied both as barrier layers for Cu interconnection and bottom electrodes for DRAM capacitors [1-9]. They have shown low resistivity and excellent thermal/chemical stability against high temperature processing. It has also been reported that $TaSi_xN_y$ is an excellent oxygen diffusion barrier up to 900°C, due to Si-N bonds which results in an amorphous structure and suppresses grain boundaries as diffusion paths [4-5]. For these reasons, it is worthwhile to investigate $TaSi_xN_y$ as metal gate electrodes [10].

Nicolet et al. have performed in-depth analysis of the barrier properties and failure mechanisms of $Ta_{30}Si_{14}N_{50}$ thin film for applications in Cu interconnection [1]. They reported that $Ta_{30}Si_{14}N_{50}$ thin film has a resistivity of 625 $\mu\Omega$cm and crystallizes at 1100°C into Ta_2N, Ta_5Si_3 and $Ta_{4.5}Si$. It was reported that the excellent diffusion properties of amorphous $Ta_{30}Si_{14}N_{50}$ are attributed to the lack of grain boundaries that can act as fast diffusion paths. Wang et al. reported that the $TaSi_xN_y$ thin films (resisitivity ~ 180 μΩcm) have Ta-Si, Ta-N and Si-N bonding as obtained from XPS analysis [5]. XRD analysis showed that $TaSi_xN_y$ film contained both $TaSi_2$ and Ta_5Si_3 phases. It was also reported that the grain size of the $TaSi_xN_y$ film was smaller than that of the $TaSi_x$ film due to suppression of the grain growth of $TaSi_2$ and Ta_5Si_3. Nah et al. studied the chemical state of $TaSi_xN_y$ films deposited via reactively sputtering from a Ta_5Si_3 target. Kim et al. reported the $TaSi_xN_y$ film with N content higher than 40 at. % contains Ta-Si, Ta-N, and Si-N bonding. Furthermore, Ta-Si-N film remains in a nanostructured state even after annealing at 1100°C owing to the fact that the N in the film suppresses the TaSi phase [6]. Olowolafe et al. reported that $Ta_{28}Si_7N_{65}$ film with the lowest Si to Ta ratio start crystallizing at ~ 900°C and resulted in the formation of Ta_2N, Ta_5Si and Ta_5Si_3 intermetallic phases. Films with higher Si to Ta ratios, $Ta_{24}Si_{10}N_{66}$ and $Ta_{24}Si_{12}N_{64}$, showed no evidence of recrystallization for anneals up to 1100°C [7].

Hara et al. investigated the barrier properties of the O diffusion in TaSiN film with different Si compositions [3]. They found the depth of oxygen diffusion decreased with increasing Si composition ($Ta_{22}Si_{35}N_{43}$). Grill et al. reported that the Si content controlled the oxidation resistance of the $TaSi_xN_y$ films [2]. They found $TaSi_xN_y$ film with more than 28 at.% Si had no identifiable oxidation in RBS spectra for anneals up to 700°C. Table 1 summarizes the prior research activities on $TaSi_xN_y$ thin films as a barrier layer for Cu interconnection and a bottom electrode for DRAM capacitors.

$Ta_{30}Si_{14}N_{50}$	625 μΩcm, Ta_2N, Ta_5Si_3 and $Ta_{4.5}Si$ at 1100°C as-deposited $Ta_{30}Si_{14}N_{50} \rightarrow$ amorphous
$TaSi_xN_y$	180 μΩcm, $TaSi_2$ and Ta_5Si_3 phases Ta-Si, Ta-N and Si-N bonding suppression of the grain growth of $TaSi_2$ and Ta_5Si_3
$TaSi_xN_y$	bonding structures of Ta-Si, Ta-N, and Si-N (> N 40 at. %) nanostructure up to 1100°C
$Ta_{28}Si_7N_{65}$	(low Si/Ta) Ta_2N, Ta_5Si and Ta_5Si_3 crystallizing at 900°C
$Ta_{24}Si_{10}N_{66}$, $Ta_{24}Si_{12}N_{64}$	(higher Si/Ta) no recrystallization up to 1100°C
$Ta_{22}Si_{35}N_{43}$	oxygen diffusion decreased with increasing Si
$TaSi_xN_y$	(> 28 at.% Si) no identifiable oxidation up to 700°C

Table 1. summarizes the previous research on $TaSi_xN_y$ thin films

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2.2 Material Properties of $TaSi_xN_y$ thin films

$TaSi_xN_y$ thin films with several compositions have been investigated as gate electrodes for dual gate Si-CMOS devices. We have investigated the structural properties of the $TaSi_xN_y$ for various annealing conditions with respect to the microstructure, resistivity, and bonding structure.

2.2.1 Experimental

$TaSi_xN_y$ thin films were deposited by reactive DC sputtering from a $TaSi_2$ target in argon and nitrogen ambient. The target was 1.3 inches in diameter with 99.9% purity. The flow ratio of $N_2/(N_2+Ar)$ was varied from 0% to 25%. The deposition pressure was 8 – 10 mTorr. The base pressure of the chamber was < $5x10^{-8}$ Torr. No intentional heating was applied to the substrate. The DC power was 50W and the thickness of the $TaSi_xN_y$ films was 1000 Å. The blanket SiO_2 32Å/p-Si substrates were used to characterize the material properties of $TaSi_xN_y$ thin films. Field oxide (3000Å) isolated overlap capacitors were fabricated on p-type wafers using lift-off to define the gate electrodes for electrical characterization. Thermally grown SiO_2 32-100Å was used as dielectrics. A sputtered tungsten-capping layer was deposited on $TaSi_xN_y$ film. To evaluate the thermal stability, all samples were rapid thermal annealed in Ar ambient at 600°C, 700°C, 900°C, and 1000°C for 15s. All samples were subjected to forming gas annealing at 400°C for 30min.

To correlate the composition of the film to the process conditions, we obtained Rutherford backscattering spectroscopy (RBS) spectra of $TaSi_xN_y$ films as a function of percent N_2 flow. Electrical resistivity was measured by 4pt probe method. In order to investigate the crystal structure of the films and interfacial reaction between $TaSi_xN_y$ film and SiO_2, X-ray diffraction (XRD) and transmission electron microscopy (TEM) analysis were performed. X-ray photoelectron spectroscopy (XPS) analysis was performed to get the bonding information in the $TaSi_xN_y$ thin films.

2.2.2 Composition

Figure 1 shows the RBS spectra of the $TaSi_xN_y$ films deposited on SiO_2 /p-type Si substrate with different N_2 percent flow rates (f_N). In case of f_N = 0%, no nitrogen peak can be identified. As the N_2 flow increases, the nitrogen peak emerged and the intensity of N peak increased. The RBS spectra also revealed that 2 at. % argon and 5 at. % of oxygen were incorporated in the $TaSi_xN_y$ films as impurities. It is attributed to argon and residual oxygen in the sputtering chamber.

Figure 2 shows the composition of $TaSi_xN_y$ films as a function of f_N. It indicates that increasing f_N results in higher incorporation of N in the films. It has been reported that N in $TaSi_xN_y$ films can suppress the growth of Ta_5Si_3 and $TaSi_2$ microcrystallites resulting in an amorphous film. This amorphous film is expected to have good thermal/chemical stability. In our films, the N concentration in the films increases from 5% to 59% as f_N increases from 0% to 25%. The measurement of the nitrogen in the film by RBS has a 7% uncertainty due to the resolution limitation of MeV $^4He^{2+}$ backscattering spectroscopy and statistical error. The RBS data showed higher nitrogen contents compared to the corresponding XPS data. It was reported that preferential removal of light elements can occur during Ar depth profiling of XPS analysis.[1] The Si/Ta ratio was found to vary with the various N flows. It is attributed to differences in sputtering yields of the Ta and Si component with changing sputtering conditions. The

Si/Ta ratio in the films increased with N_2 flow for a given Ar flow. A steady state condition at the target surface was not reached since the difference of Ta (180.95) and Si atomic weight (28.09) is large enough to cause a preferential sputtering of the film. As f_N increases, both the Si/Ta ratio and the N/Ta ratio increase.

Figure 3 shows the isothermal ternary Ta-Si-N phase diagram indicating the $TaSi_xN_y$ compositions studied here. There is no change of stable tie lines at temperature range between 300K and 1700K.[2] The $TaSi_xN_y$ composition can be optimized for barrier properties, oxidation barrier, low resistance, or thermal stability. Increasing nitrogen content cause oxidation resistance but also increases the resistivity. Also, excessive N content results in nitrogen diffusion and higher work function of $TaSi_xN_y$ gate electrode. Increasing Si content improves oxidation resistance but also causes an increase in resistivity and promotes $TaSi_2$ formation. The presence of both Si and N is deemed necessary and their content is critical in obtaining optimized $TaSi_xN_y$ gate electrodes suitable for NMOS devices.

2.2.3. Resistivity

The resistivity of the films as a function of f_N is plotted in figure 4. The resistivity of the film increases sharply, when f_N exceeds 10%. The sharp increase in resistivity with increased N content can be attributed to the amorphous structure of the film. At higher f_N, significant decrease in the deposition rates was observed due to the target poisoning, where nitrides are formed directly on the target surface. The resistivity of as deposited $TaSi_xN_y$ film (f_N = 0%) was 220μΩcm and it decreased to ~122 μΩcm after annealing at 1000^{o}C. The resistivity of the $TaSi_xN_y$ film reduces by the subsequent RTA process. It is attributed to reduction of the defect concentration in the film after high temperature annealing. Table 1 summarizes compositions, resistivity, and crystal structures of $TaSi_xN_y$ thin films as a function of f_N.

2.2.4 Crystal structures

In order to investigate the crystal structures and formation of phases in the film after annealing, XRD analysis was performed. No crystalline peak was observed in the as-deposited $TaSi_xN_y$ films for all values of f_N.(not shown here). Figure 5 shows the XRD patterns of $TaSi_xN_y$ films as a function of f_N after 1000°C anneals. For $TaSi_xN_y$ film (f_N = 0%), all the peaks correspond to the $TaSi_2$ and Ta_5Si_3 phases, where the Ta_5Si_3 phase dominates. The intensity of the peaks increases after annealing. The $TaSi_xN_y$ film (f_N = 0%) did not show any change in phase and structure during the annealing in the range of 400 - 1000°C. When f_N was 10% and higher, the $TaSi_xN_y$ remained amorphous (or microcrystalline) as detected by XRD analysis. No crystalline peaks were observed even after anneals up to 1000°C.

2.2.5 Bonding structure

Figure 6 (a), (b), and (c) show the XPS core-level spectra of the Si 2p, Ta 4f, and N 1s region for the as-deposited $TaSi_xN_y$ film with different nitrogen flow rate. As shown in fig. 6(a), the binding energy of Si for f_N = 0 % is 99.3eV, indicating Si bonding with Ta.[3] For f_N = 15%, the Si 2p peak at 101.8eV indicates Si-N bond formation.[4] It shows a significant increase of Si-N bonding with increasing N flow. Figure 6(b) shows that the binding energy of Ta $4f_{7/2}$ and Ta $4f_{5/2}$ for $TaSi_xN_y$ film with f_N = 0 % flow are 22.1 eV and 23.8 eV, indicating Ta 4f binding with Si.[5] It was reported that a doublet of Ta 4f peak is due to spin-orbit coupling.[6] In case of 5% and 15% N flow, the peaks of Ta $4f_{7/2}$ shifted to higher energy of 23.0 eV, suggesting Ta-N bonds.[7] In fig. 6(c), the Si-N bonding (397.4 eV) [8] is also observed in the N 1s spectrum of $TaSi_xN_y$ film with f_N = 15 %. XPS analysis shows that the $TaSi_xN_y$ film with f_N = 0 % consisted of Ta-Si bonds, while $TaSi_xN_y$ film with f_N = 5 % composed of Ta-Si and Ta-N bonds and $TaSi_xN_y$ film with f_N = 15% consisted of a combination Ta-Si, Ta-N and Si-N bonds. The presence of Si-N bonds is attributed to cause the amorphous nature of the high N containing films.

2.3 Summary

We have investigated reactively sputtered $TaSi_xN_y$ films as gate electrodes for dual gate Si-CMOS devices. The as-deposited $TaSi_xN_y$ films remained amorphous over a wide range of compositions and temperatures. $Ta_{30}Si_{33}N_{37}$ film changed to crystalline, however $Ta_{26}Si_{28}N_{52}$ film remains amorphous after 1000^{o}C anneal. In XPS analysis, the $TaSi_xN_y$ (f_N = 0%) film consisted of Ta-Si bonds, the $TaSi_xN_y$ (f_N = 5%) consisted of Ta-Si and Ta-N bonds and the $TaSi_xN_y$ (f_N = 25%) consisted of a combination Ta-Si, Ta-N and Si-N bonds. The presence of Si-N bonds is attributed to cause the amorphous nature of the high N containing $TaSi_xN_y$ films, but at the cost of higher resistivity.

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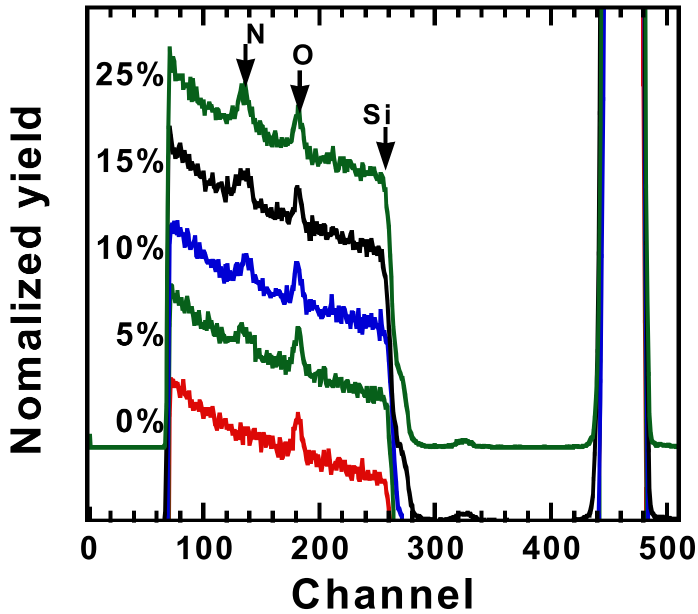

Fig. 1. RBS spectra of the $TaSi_xN_y$ films deposited on SiO_2 /p-type Si substrate with different percent N_2 flow rates.

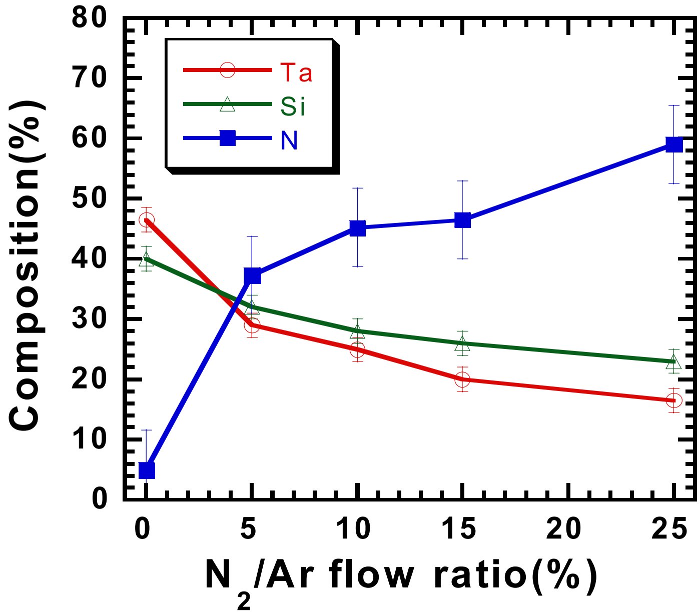

Fig. 2. Compositions of Ta, Si, and N in the $TaSi_xN_y$ films reactively sputtered from $TaSi_2$ targets as a function of percent N_2 flow rates.

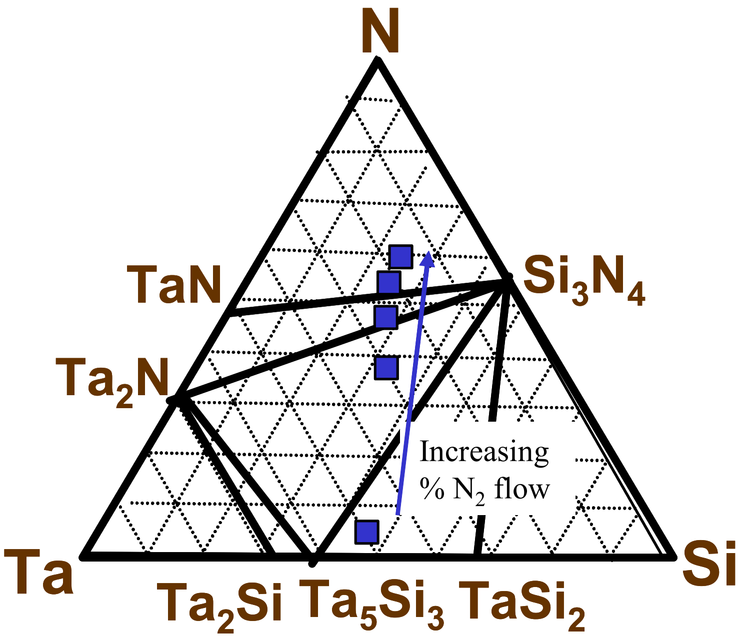

Fig. 3. The isothermal ternary phase diagram of Ta-Si-N at 1000^{o}C

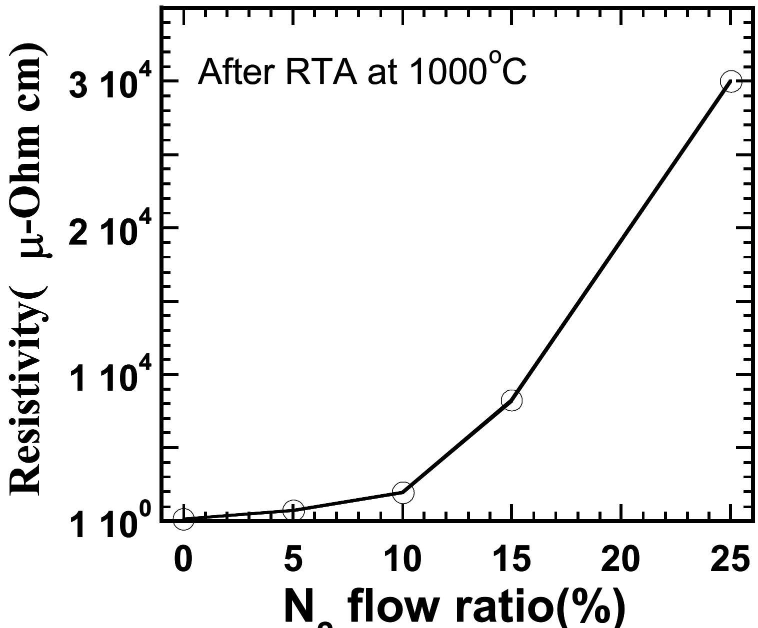

Fig. 4. Resistivity of 1000^{o}C annealed $TaSi_xN_y$ films as a function of percent N_2 flow rates.

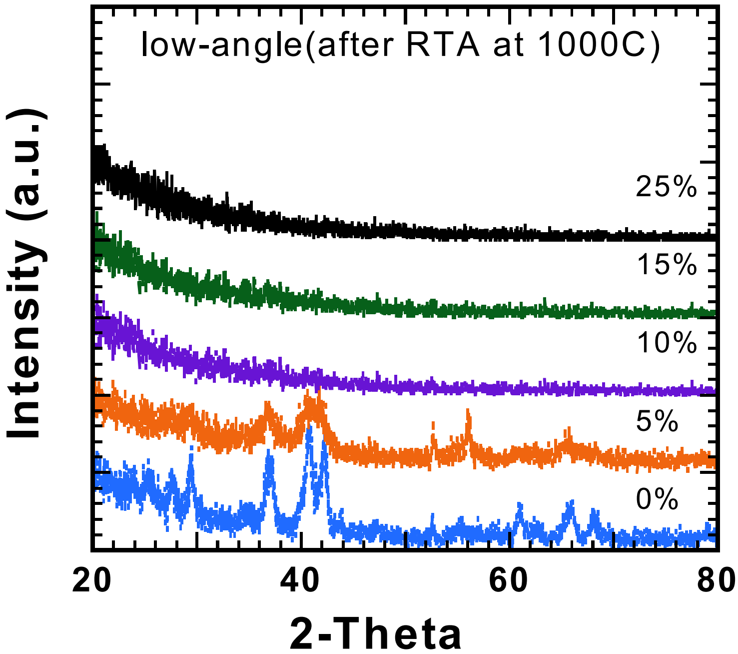

Fig. 5. The XRD spectra of the $TaSi_xN_y$ films with different nitrogen flows after 1000°C anneals.

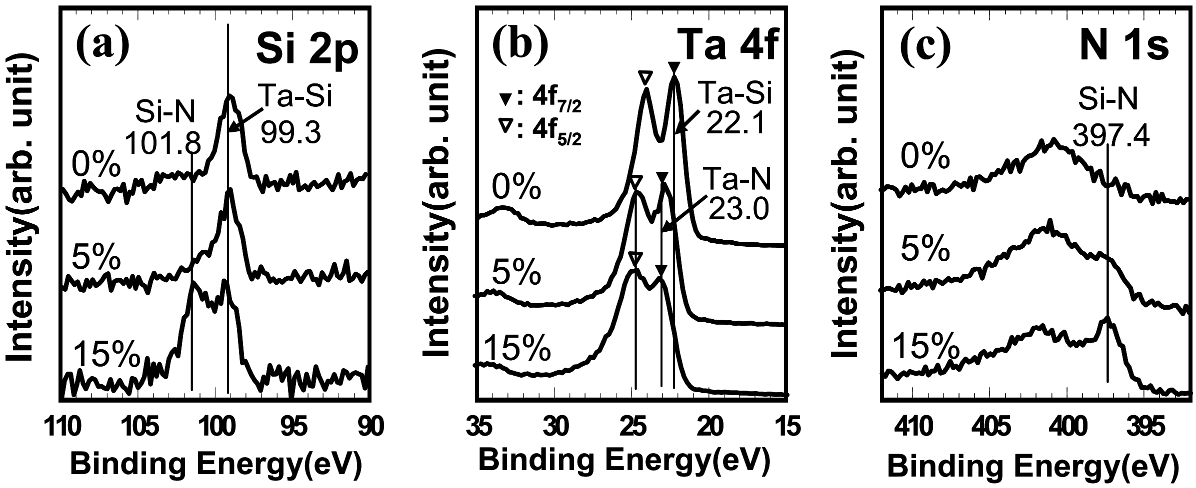

Fig. 6. The XPS spectra of as-deposited $TaSi_xN_y$ films with different nitrogen flows.

(a) the Si 2p region (b) the Ta 4f region, and (c) the N 1s region

N_2/Ar flow rate	Composition	Resistivity ($\mu\Omega$cm)	Crystal structure
0%	$Ta_{51}Si_{44}N_5$	**122**	Ta_5Si_3+$TaSi_2$
5%	$Ta_{30}Si_{33}N_{37}$	**707**	**mixture***
10%	$Ta_{26}Si_{28}N_{46}$	**1941**	**amorphous**
15%	$Ta_{22}Si_{26}N_{52}$	**8222**	**amorphous**
25%	$Ta_{17}Si_{24}N_{59}$	**-**	**amorphous**

*** mixture = Ta_5Si_3+$TaSi_2$+amorphous**

Table 1. Compositions, resistivity, and crystal structures of Ta-Si-N thin films

CHAPTER 3

Characteristics of $TaSi_xN_y$/ SiO_2/ Si structures

In this chapter, characteristics of $TaSi_xN_y$/ SiO_2/ Si structures will be discussed in detail. This chapter consists of three papers and will cover the materials and electrical analysis of $TaSi_xN_y$ films.

In the first paper, the properties of $TaSi_xN_y$ films were evaluated for gate electrode applications for the first time. The $TaSi_xN_y$ films in this chapter were deposited by reactively sputtering from a $TaSi_2$ target. The workfunction of $TaSi_xN_y$ was investigated from capacitance-voltage analysis. Also, the thermal stability of gate oxide thickness and gate current is discussed.

In the second paper, Fowler-Nordheim tunneling in $TaSi_xN_y/SiO_2$/p-Si structures was used to analyze the work function behavior of $TaSi_xN_y$ films. The barrier height, extracted by Fowler-Nordheim current analysis, was correlated with the extracted workfunction from capacitance-voltage analysis. The mechanisms that describe the workfunction behavior with high temperature annealing are discussed.

In the third paper, the thermal stability of $TaSi_xN_y/SiO_2$/p-type Si metal-insulator-semiconductor (MOS) structure is discussed with respect to electrical and physical properties in detail. To investigate the composition of $TaSi_xN_y$ films and the bonding structures of Ta, Si, and N in the film, X-ray photoelectron spectroscopy (XPS) analysis was performed. In order to investigate the crystal structure of the films and the interfacial reaction between $TaSi_xN_y$ film and SiO_2, X-ray diffraction (XRD) and Transmission electron microscopy (TEM) analyses were performed.

3.1 Electrical Characteristics of $TaSi_xN_y$ Gate Electrodes

For Dual Gate Si-CMOS Devices

You-Seok Suh, Greg Heuss, Huicai Zhong, Shin-Nam Hong and Veena Misra

VLSI Tech. Dig. 01, 47 (2001).

Electrical Characteristics of $TaSi_xN_y$ Gate Electrodes For Dual Gate Si-CMOS Devices

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Abstract

In this work, the physical and electrical properties of $TaSi_xN_y$ films are evaluated for gate electrode applications. MOS capacitors with $TaSi_xN_y$ gates of varying N concentrations were fabricated. The stability of $TaSi_xN_y/SiO_2$/p-type Si stacks was studied at annealing temperatures of 700°C, 900°C, and 1000°C in Ar. When the nitrogen content exceeds 35 at.%, excellent stability of oxide thickness and gate current is observed for anneals up to 1000°C. The results also indicate that the workfunction of $TaSi_xN_y$ is compatible with NMOS devices.

Introduction

As gate oxide thickness decreases, the capacitance associated with the depleted layer at the poly-Si/gate dielectric interface becomes significant, making it necessary to consider alternative gate electrodes[1]. The search for metallic gates faces many challenges since they must have compatible work functions, process compatibility and thermal/chemical interface stability with underlying dielectric. To replace n^+ and p^+ poly-Si and maintain scaled performance, it is necessary to identify pairs of metals with workfunctions that are respectively within 0.2 eV of the conduction and valence band edges of Si [2]. Most metal gate electrodes studied to date suffer from high temperature instability resulting in a degraded interface with the underlying dielectric [3]. $TaSi_xN_y$ films have been studied as barrier layers for Cu interconnection and have shown superior diffusion barrier properties[4]. In this work, we have investigated the electrical properties of $TaSi_xN_y$ metals and evaluated them as gate electrodes for their potential use in NMOS devices. This paper presents the workfunction and thermal stability of $TaSi_xN_y$ gate electrodes.

Experimental

Table 1 summarizes the fabrication process of MOS capacitor structures with $W/TaSi_xN_y/SiO_2$/p-type Si stack. $TaSi_xN_y$ films were deposited on the thermally grown SiO_2 gate oxides using reactive DC magnetron sputtering from a $TaSi_2$ target, varying the N_2 flow rate. A W capping layer was sputtered on the $TaSi_xN_y$ films. The $TaSi_xN_y$ gate electrodes were patterned using lift-off lithography. All samples were annealed in 10% H_2/N_2 at 400°C for 30 min. The samples were then annealed in Ar at 700°C, 900°C and 1000°C for 15sec. C-V and I-V characteristics were obtained using HP4184 and HP4155B, respectively. The capacitance was measured at various frequencies on an area of $2.5x10^{-5}cm^2$. The V_{FB} and equivalent oxide thickness (EOT) for the capacitors were obtained using the NCSU CV program.

Results and Discussion

Fig. 1. shows the RBS spectra of $TaSi_xN_y$ films with different N_2 flow rates. Fig. 2 displays the N concentration in the $TaSi_xN_y$ film as a function of N_2/Ar flow ratio. The resistivity of $TaSi_2$ was ~260 μΩ-cm and ~180 μΩ-cm after annealing at 400ºC and 900ºC, respectively. The XRD analysis indicated that the $TaSi_2$ films were crystalline in the as-deposited state. In contrast, the $TaSi_xN_y$ films with N_2 flow ratio of 25%, did not exhibit any peaks even after anneals up to 1000ºC, as shown in Fig. 3, indicating a nanocrystalline or amorphous microstructure. The resistivity of 25% N_2 flow ratio $TaSi_xN_y$ films was similar to heavily doped polysilicon films.

The C-V curves of the capacitors with $TaSi_xN_y$ gate electrodes after annealing at 400ºC are shown in Fig. 4. In order to decouple the fixed charge from the workfunction, several oxide thicknesses were used. The V_{FB} vs. EOT plot is shown in Fig. 5 in which the y-intercept indicates the workfunction, Φ_m. As shown in Fig. 6, the Φ_m values of $TaSi_xN_y$ with varying N contents ranges from 4.19-4.27 eV, suggesting that $TaSi_xN_y$ films have workfunctions appropriate for NMOS devices. Diffusion of nitrogen from the gate to the Si-SiO_2 interface, which typically occurs with TaN_x gates, was not observed with $TaSi_xN_y$ gates since there was no change in the slope of V_{FB} vs T_{ox} curves for $SiO_2 <$ 4nm, as shown in Fig. 7. Thermal stability was evaluated by annealing the gates at 700°C, 900°C, and 1000°C in Ar for 15sec. As shown in Fig. 8, the $TaSi_xN_y$ gates display good stability on SiO_2 even up to 1000ºC with no degradation of the CV curves. A slight change in V_{FB} (<150mV) is observed after annealing and is attributed to fixed and interface charges that are created in the dielectric upon annealing. This charge may be reduced using a forming gas anneal. As shown in Fig 9, the negligible change in EOT of the $TaSi_xN_y/SiO_2$ stack after high temperature anneals demonstrates the excellent thermal stability of these gates, In order to evaluate the effect of nitrogen in $TaSi_xN_y$ films, the I-V characteristics were obtained for both $TaSi_x$ and $TaSi_xN_y$ and are shown in Figs. 10 (a) and (b) for anneals of 400ºC and 1000ºC, respectively. The I-V characteristics of the capacitors with $TaSi_xN_y$ gates displayed lower gate leakage compared to the $TaSi_x$ gates for both 400ºC and 1000ºC anneals. It is believed that the microstructure of the film and the presence of nitrogen retards reaction rates and improves the chemical stability of the gate-dielectric interface.

Conclusion

We have shown that $TaSi_xN_y$ films on SiO_2 provide good thermal stability up to 1000ºC resulting in minimal change of EOT and V_{FB}, while demonstrating low leakage current. The improved stability of $TaSi_xN_y$ gates is attributed to the presence of Si and N in the gate electrode, which can improve the film microstructure and the diffusion barrier properties at the gate-dielectric interface.

Acknowledgement: This work is supported by SRC and SEMATECH.

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- Isolation(Fox = 3500Å)
- Gate oxidation Tox 3-10nm
- $TaSi_xN_y$ deposition(1000 Å)
- W deposition(500 Å)
- Electrode patterning by wet etch
- Annealing at 400°C for 30min
- RTA: 700°C, 900°C,1000°C, 15sec

Table 1 Fabrication process of MOS capacitor.

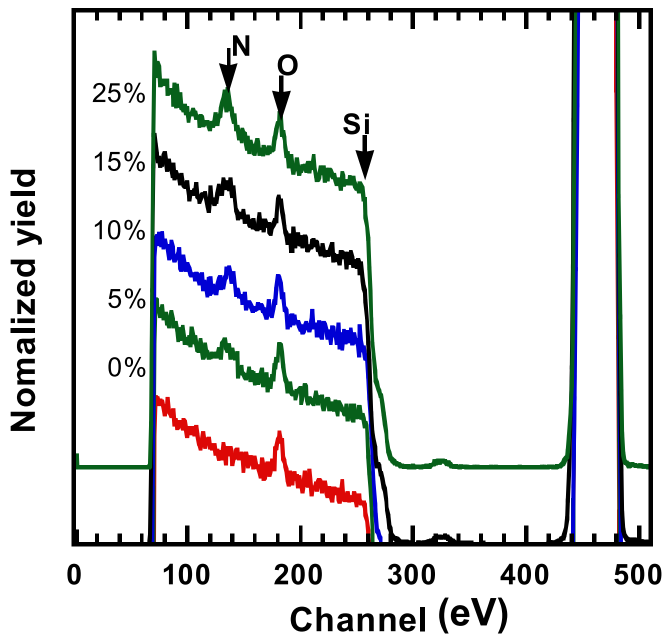

Fig. 1. RBS spectra of as-deposited $TaSi_xN_y$ film as a function of the N_2 flow rate.

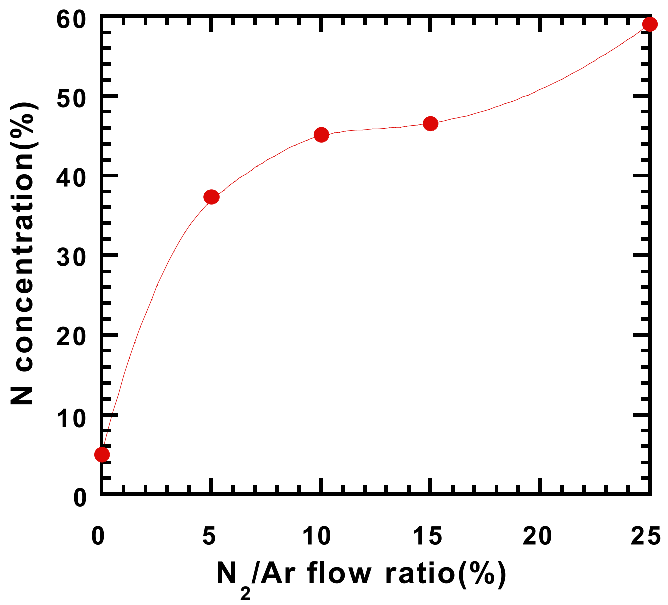

Fig. 2. The variation of N concentration vs N_2 flow rate.

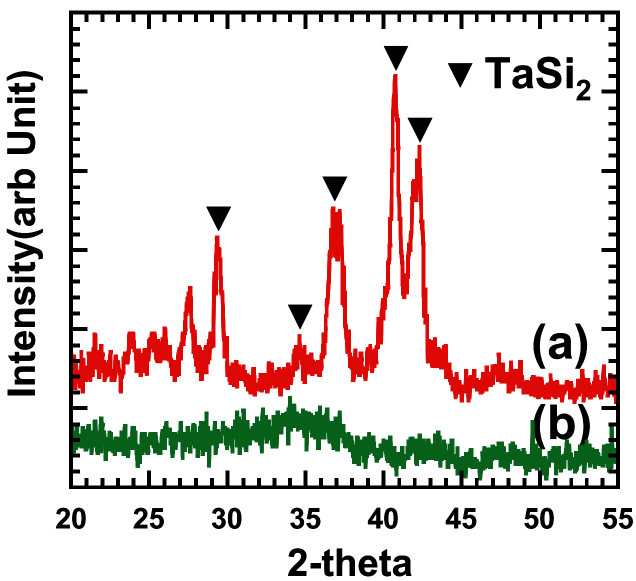

Fig. 3. The XRD patterns for $TaSi_xN_y$ film after the annealing at 1000 ºC for 30sec.
(a) TaSix (N_2 flow: 0%) and (b) $TaSi_xN_y$ (N_2 flow: 25%)

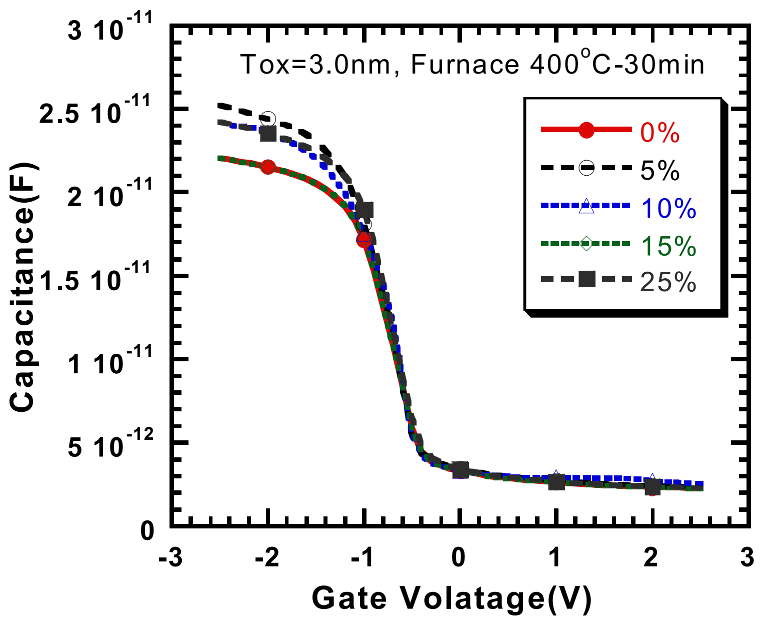

Fig. 4. Typical C-V curves of $TaSi_xN_y$ electrode capacitor with the N_2 flow rate, after annealing at 400ºC for 30min. Capacitor area =2.5E-5cm^2.

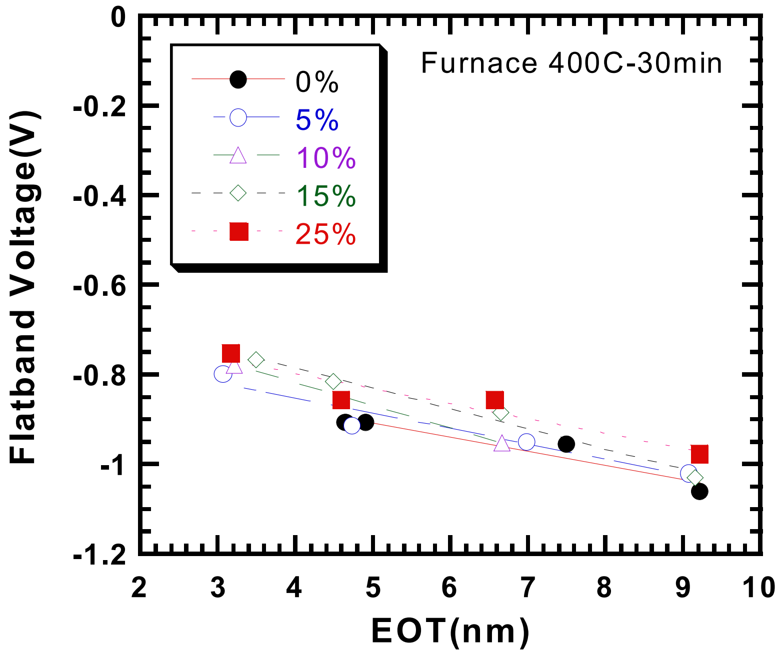

Fig. 5. V_{FB} vs. EOT at the various $TaSi_xN_y$ electrodes.

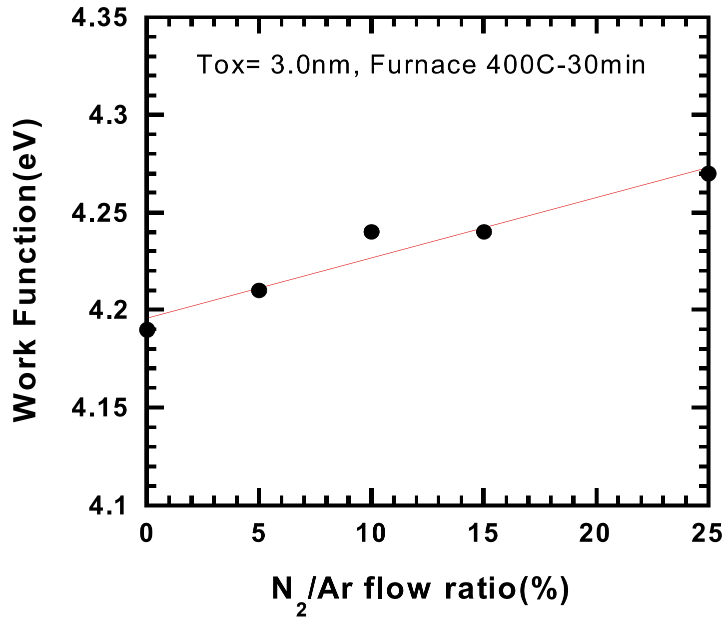

Fig. 6. Effect of N_2 flow rate on the work function of $TaSi_xN_y$ electrodes.

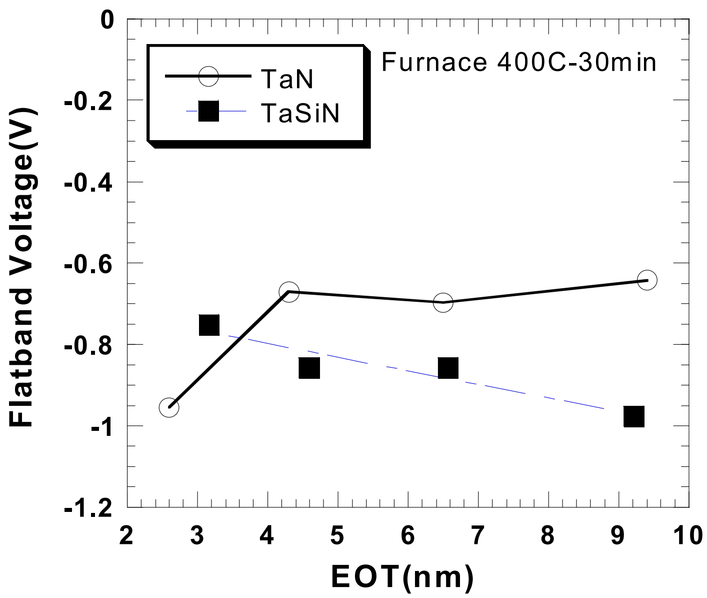

Fig. 7. Comparison of V_{FB} vs EOT between TaN and of $TaSi_xN_y$.

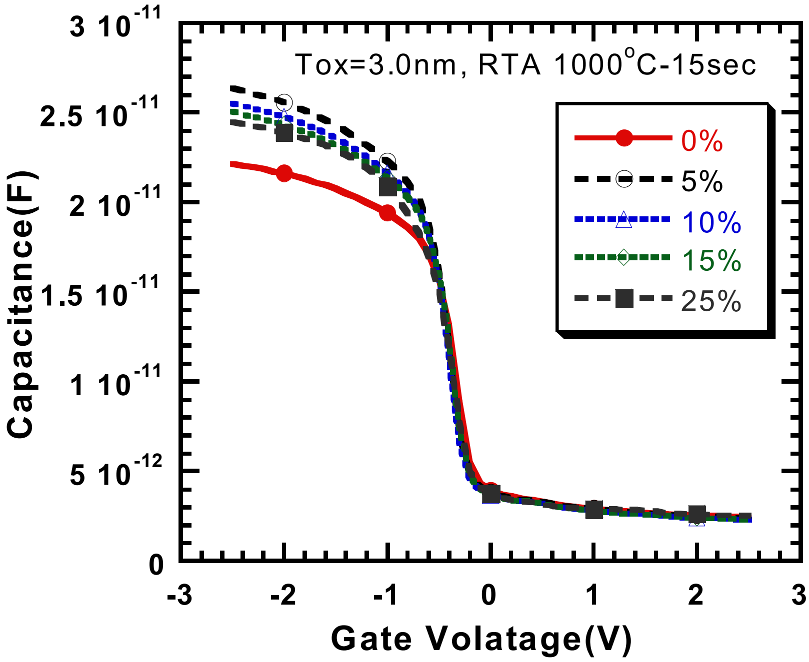

Fig. 8. Typical C-V curves of $TaSi_xN_y$ electrode capacitor with the N_2 flow rate, after annealing at 1000ºC for 30min. Capacitor area =2.5E-5cm^2

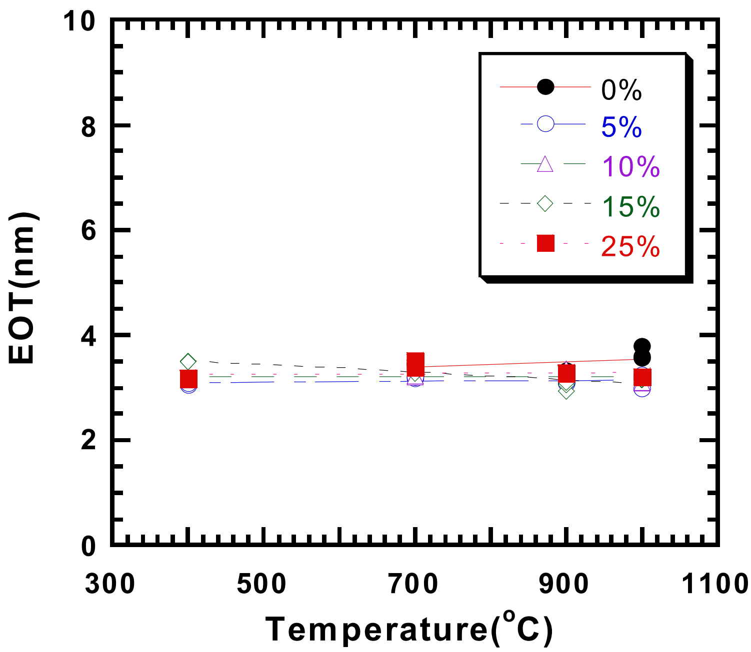

Fig. 9. EOT vs. annealing conditions at the various $TaSi_xN_y$ electrodes.

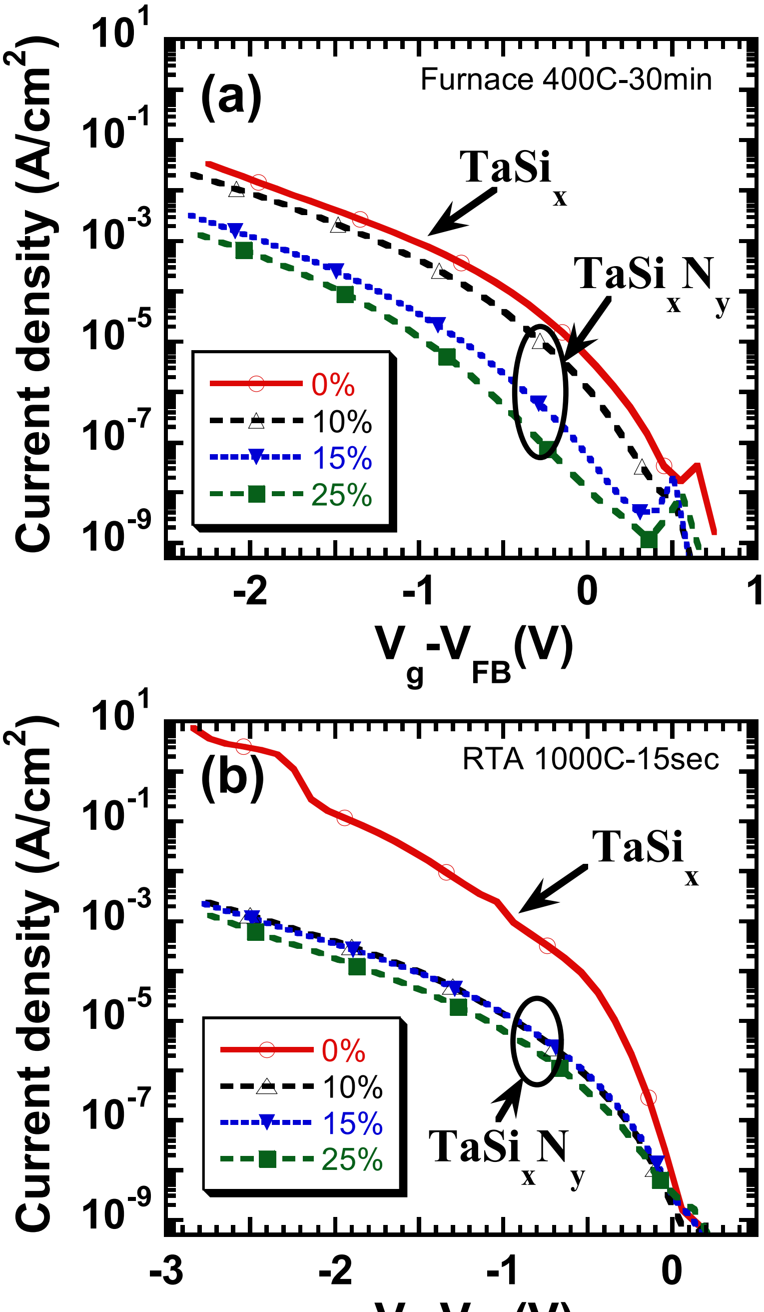

Fig. 10. Typical I-V curves of $TaSi_xN_y$ electrode capacitor with the N_2 flow rate. (a) Furnace annealing at 400ºC for 30min and (b) RTA at 1000 ºC for 30sec.

3.2 Electrical characteristics of $TaSi_xN_y$/ SiO_2/Si structures by Fowler-Nordheim current analysis

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Appl. Phys. Lett., 80(8), 1403 (2002).

Electrical characteristics of $TaSi_xN_y$/ SiO_2/Si structures by Fowler-Nordheim current analysis

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Abstract

In this paper, the Fowler-Nordheim tunneling in $TaSi_xN_y/SiO_2$/p-Si structures has been analyzed. The effective barrier height at the metal-oxide interface was extracted by Fowler-Nordheim current analysis. The barrier height was found to increase with increased annealing temperature. The barrier height was correlated with the extracted workfunction from Capacitance-Voltage (CV) analysis. This indicated that the workfunction of $TaSi_xN_y$ films changes under high temperature annealing from 4.2 ~ 4.3eV after 400ºC anneals to ~4.8eV after 900ºC anneals. We believe that the mechanism that causes the workfunction to increase is the formation of a Ta-disilicide layer at the interface of the electrode and the dielectric.

$TaSi_xN_y$ films have been studied both as a barrier layer for Cu interconnection and a bottom electrode for DRAM capacitors.[1-5] They have shown low resistivity and excellent thermal/chemical stability against high temperature processing. It has also been reported that $TaSi_xN_y$ is an excellent oxygen diffusion barrier up to 900^oC.[6,7] Recently, $TaSi_xN_y$ films have been investigated as a metal gate electrode due to good thermal stability and appropriate workfunctions for NMOS devices.[8] In the previous paper, we evaluated the electrical properties of the $TaSi_xN_y$ films for gate electrode applications.[8] We have shown that $TaSi_xN_y$ films on SiO_2 provide good thermal stability up to 1000^oC resulting in minimal change of oxide thickness and demonstrating low leakage currents.

In this paper, we have evaluated the work function of $TaSi_xN_y$ thin films with various $TaSi_xN_y$ compositions, subjected to high temperature anneals. We have analyzed the workfunction of the stack by using Fowler-Nordheim tunneling analysis to extract the effective barrier height at the metal-oxide interface. This barrier height was then correlated with the extracted workfunction from CV analysis.

$TaSi_xN_y$ thin films were deposited by reactive DC sputtering from a $TaSi_2$ target in an argon and nitrogen ambient. The target was 1.3 inches in diameter with 99.9% purity. The flow ratio of $N_2/(N_2+Ar)$ was varied from 0% to 25%. The deposition pressure was 8 – 10 mTorr. No intentional heating was applied to the substrate. The DC power was 50W and the thickness of the $TaSi_xN_y$ films was 1000 Å. Field oxide (3000Å) isolated overlap capacitors were fabricated on p-type wafers using lift-off to define the gate electrodes. Thermally grown SiO_2 with thicknesses of 32 – 100 Å were used as dielectrics. A sputtered tungsten-capping layer was deposited on $TaSi_xN_y$ film. The base pressure of the chamber was < $5x10^{-8}$ Torr. To evaluate the thermal stability, the samples were rapid thermal annealed in Ar ambient at 600^{o}C, 700^{o}C, 900^{o}C, and 1000^{o}C for 15seconds. All samples were subjected to forming gas annealing at 400^{o}C for 30min. Rutherford backscattering spectroscopy (RBS) and Auger electron spectroscopy (AES) analysis were performed to investigate the compositions of the films. Capacitance-voltage and current-voltage characteristics were obtained using HP4284 and HP4155B, respectively. Fowler-Nordheim current analysis was performed to determine the barrier height at the metal-oxide interface in $TaSi_xN_y/SiO_2$/p-Si structures. The barrier height values were then correlated to the workfunction values extracted from CV analysis by taking the y-intercept of V_{FB} vs. T_{ox} curves

Figure 1 shows the energy band diagram of a $TaSi_xN_y/SiO_2$/p-Si structure with negative bias applied to the metal electrode. The current in this structure will be due either to Schottky emission of electrons over the barrier or to Fowler–Nordheim tunneling of electrons through the triangular barrier into the oxide conduction band.[9] At room temperature, emission of the electrons is not expected to occur because of the high barrier height and Fowler-Nordheim will dominate. The surface potential of the silicon substrate is neglected under accumulation conditions. The Fowler–Nordheim current is given by $J_{FN} = A\ E_{ox}^2 \exp[-B/E_{ox}]$.[9-11] The parameter A and B depend on the barrier height (Φ_b) and the effective mass of the tunneling electron m_{ox}. The Fowler–Nordheim current is the dominant conduction mechanism in SiO_2 for thicknesses above 70 Å, while the direct tunneling current is dominant for thicknesses below 32 Å SiO_2.

Figure 2 shows the shift of the CV curves for $TaSi_xN_y$ (15% N_2 flow) gate electrodes after high temperature annealing. The extracted EOT values are 32.0 ±0.5 Å for 400^{o}C and 31.6 ±0.5Å nm for 1000^{o}C anneals indicating the excellent stability of the

$TaSi_xN_y$ gate electrodes up to 1000°C. However, a positive shift of flatband voltage was observed after high temperature annealing. This V_{FB} change can be attributed to either the fixed charges (Q_f) created in the dielectric or a change in workfunction (Φ_m). In order to understand the origin of the increase in flatband voltage under high temperature annealing, the barrier height(Φ_b) using Fowler-Nordheim analysis was extracted and compared to the workfunction obtained from CV analysis. An effective mass of 0.5 (m_{ox}/m) was chosen for the tunneling electron. The barrier heights of $TaSi_xN_y$ with varying N contents ranged from 3.36 – 3.53eV at 400°C and 4.03 – 4.07eV for 1000°C. This indicated that the barrier height increased with annealing temperatures. The deivations for the workfunction and barrier height measurements were ± 0.05(eV). Table 1 summarized the compositions of the $TaSi_xN_y$ films, workfunction (Φ_m) from CV measurement and barrier height (Φ_b) from Fowler-Nordheim tunneling as a function of different temperature and various N flow rates.

In Fig. 3, the extracted barrier height was correlated with the extracted workfunction from CV analysis. A linear relationship was found between the workfunction and barrier height. The increase of the barrier height was attributed to the increase of workfunction during the annealing. The above analysis indicated that the V_{FB} increase is attributed to a change in workfunction and not to charge contained within the dielectric.

Figure 4 shows the behavior of worfunction as a function of different temperature and various N flow rates. As reported,[8] the workfunction of the $TaSi_xN_y$ gate was determined using the flatband voltage ($V_{FB} = \Phi_m - \Phi_s - Q_f\ t_{ox}/\varepsilon_{ox}$). The Φm values for $TaSi_xN_y$ with varying N contents range from 4.2-4.4eV just after FGA at 400°C for

30min and increased after high temperature annealing. As shown in Fig. 4, the change in workfunction was affected by the N content. For example, the $TaSi_xN_y$ films deposited with 15% N flow produced a smaller change in workfunction at 700ºC compared to the $TaSi_xN_y$ film 0% N flow. However, after 1000ºC annealing, the value of Φ_m for all films was near 4.8eV, regardless of N content. The reported Φ_m values of Ta di-silicide ($TaSi_2$) are near 4.7eV,[12] similar to the value observed here after high temperature annealing. It is believed that the mechanism that causes the workfunction to increase is the formation of a Ta-disilicide layer at the interface of the electrode and the dielectric. The Si content in the $TaSi_xN_y$ films and the underlying SiO_2 dielectric may be related to the formation of the di-silicide layer at the interface. In addition, it is also believed that only the interface region is involved since the bulk film did not show any change in phase and structure as determined by X-ray analysis. The N content in the $TaSi_xN_y$ film can retard the formation of this interface layer to some degree as was observed in our data at 700ºC.

In summary, we have investigated the work function of $TaSi_xN_y$ thin films with the various N contents, as a function of annealing temperature. We analyzed the C-V curves and Fowler-Nordheim tunneling current in $TaSi_xN_y/SiO_2$/p-Si structures. The positive shift of the CV curves was observed after high temperature annealing, indicating the change in flatband voltage. The barrier height from Fowler-Nordheim analysis was correlated with the extracted workfunction from CV analysis. We found the V_{FB} change is attributed to a change in workfunction (Φ_m) and not the fixed charges (Q_f) but We believe the mechanism that causes the workfunction to increase is the formation of a Ta-disilicide (Φ_m = 4.7eV) layer at the interface of the electrode and the dielectric.

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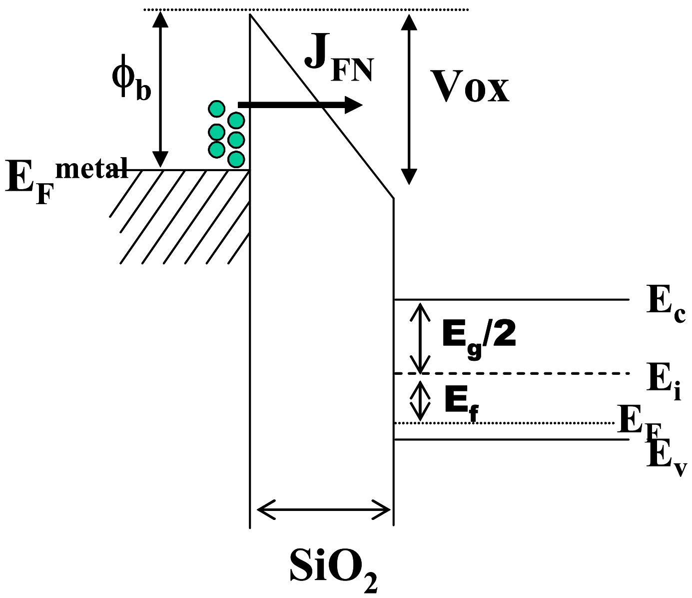

Fig. 1. Energy diagram of $TaSi_xN_y/SiO_2$/p-Si structures for Fowler-Nordheim tunneling

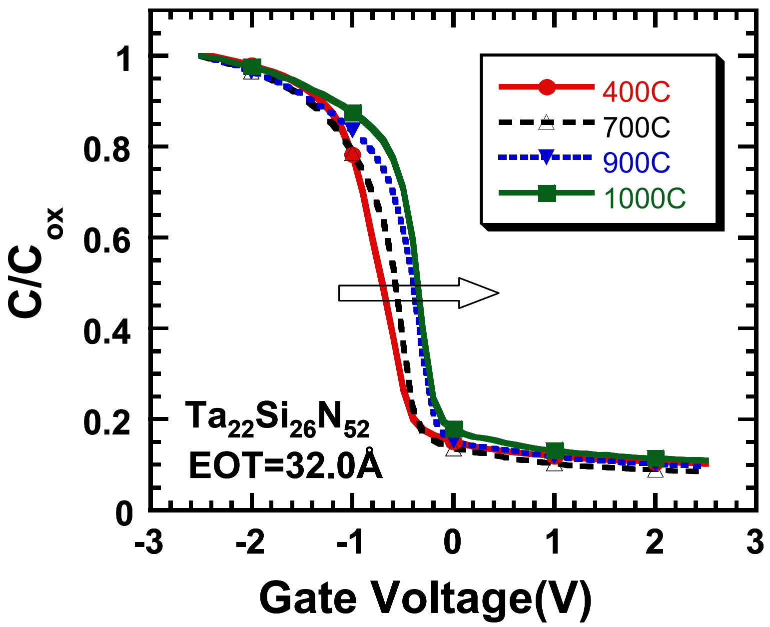

Fig. 2. C-V characteristics of $TaSi_xN_y$ (15% N_2 flow) gate electrodes with EOT=3.2nm as a function of annealing temperatures.

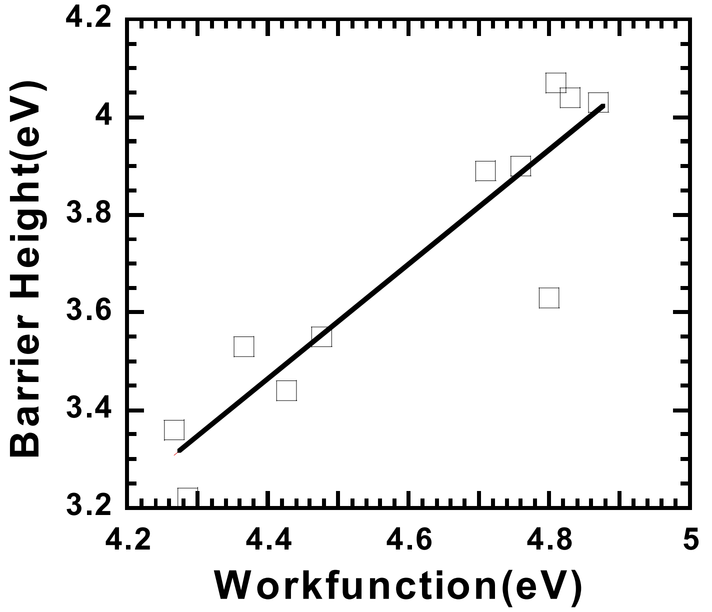

Fig. 3. Workfunction versus barrier height for $TaSi_xN_y$ films. The extracted barrier height from Fowler-Nordheim tunneling correlated with the extracted workfunction from CV analysis.

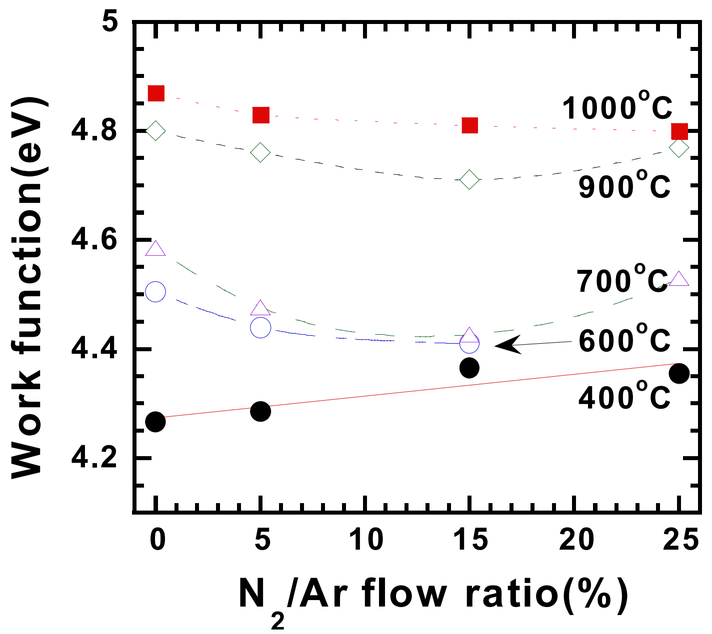

Fig. 4. The worfunction change of $TaSi_xN_y$ gate electrode at different temperatures for various N_2 flow rates.

N_2/Ar flow rate	Composition(at.%) Ta	Si	N	Workfunction(eV) 400°C	700°C	900°C	Barrier Height(eV) 400°C	700°C	900°C
0%	**46.5**	**40.0**	**–**	**4.26**	**4.58**	**4.80**	**3.36**	**3.28**	**3.63**
5%	**29.0**	**32.0**	**37.3**	**4.28**	**4.44**	**4.76**	**3.22**	**3.55**	**3.90**
15%	**21.9**	**25.5**	**51.7**	**4.36**	**4.41**	**4.71**	**3.53**	**3.44**	**3.89**
25%	**16.5**	**23.0**	**59.1**	**4.35**	**4.53**	**4.77**			

Table. 1. The compositions of the $TaSi_xN_y$ films, workfunction (Φ_m) from CV measurement and barrier height (Φ_b) from Fowler-Nordheim tunneling as a function of different temperature and various N flow rates.

3.3 Thermal stability of $TaSi_xN_y$ films deposited by reactive sputtering on SiO_2

You-Seok Suh, Greg P. Heuss, Dae-Gyu Park, Kwan-Yong Lim, and Veena Misra

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Thermal stability of $TaSi_xN_y$ films deposited by reactive sputtering on SiO_2

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Abstract

The thermal stability of $TaSi_xN_y/SiO_2$/p-type Si metal-insulator-semiconductor (MOS) structure has been evaluated by measuring equivalent oxide thickness (EOT) from capacitance–voltage curves and gate leakage current as a function of annealing temperatures. $TaSi_xN_y$ films were deposited using reactive sputtering from a $TaSi_2$ target, varying the nitrogen/argon flow ratio. A reaction between $Ta_{53}Si_{47}$ and SiO_2 was observed after a 1000°C anneal, resulting in the increase of interfacial roughness and oxide thickness in the $TaSi_xN_y/SiO_2$/p-Si structures. Cross-sectional transmission electron microscopy shows no indication of an interfacial reaction or crystallization in $Ta_{22}Si_{29}N_{49}$ on SiO_2 up to 1000°C as manifested by the negligible change in EOT and the stable leakage currents density (2.0×10^{-6} A/cm^2 at V_g= -1V). The presence of Si-N bonds is attributed to cause the amorphous nature of the high N containing $TaSi_xN_y$ films. This may retard the formation of an interface layer and improve the chemical-thermal stability of the gate electrode/dielectric interface and oxygen diffusion barrier properties under high temperature annealing.

I. INTRODUCTION

$TaSi_xN_y$ films have been studied both as a barrier layer for Cu interconnection and as a bottom electrode for DRAM capacitors.[1-3] They have shown low resistivity and excellent thermal/chemical stability against high temperature processing. It has also been reported that $TaSi_xN_y$ has excellent oxygen diffusion barrier properties up to 900^{o}C.[4-6] Recently, $TaSi_xN_y$ films have been investigated as metal gate electrodes owing to their good thermal stability and N-type metal-oxide-semiconductor (MOS) compatible workfunctions.[7] As gate oxide thickness decreases, the poly-Si gate depletion problem becomes significant, making it necessary to consider alternative gate electrodes.[8] The search for metallic gates faces many challenges since they must have compatible work functions, process compatibility and thermal/chemical interface stability with underlying dielectric.[9] Most metal gate electrodes studied to date suffer from high temperature instability, resulting in a degraded interface with the underlying dielectric.[10]

In this work, we report the thermal and chemical stability of $TaSi_xN_y$ thin films with various compositions of x and y in the $TaSi_xN_y/SiO_2$/p-Si structures under high temperature anneal. We have evaluated the thermal stability of $TaSi_xN_y$ /SiO_2/p-type Si stacks by measuring equivalent oxide thickness from capacitance–voltage (C-V) curves and gate leakage current as a function of annealing temperatures. We have analyzed physical oxide thickness and interfacial reaction between the $TaSi_xN_y$ film and SiO_2 by transmission electron microscopy (TEM) and x-ray photoelectron spectroscopy (XPS).

II. EXPERIMENTAL

$TaSi_xN_y$ thin films were deposited by reactive DC sputtering from a $TaSi_2$ target in an argon and nitrogen ambient. The target was 1.3 inches in diameter with 99.9% purity. The ratio of $N_2/(N_2+Ar)$ flow rate, f_N, was varied from 0% to 25%. The deposition pressure was 8 – 10 mTorr, while the base pressure of the chamber was < $5x10^{-8}$ Torr. No intentional heating was applied to the substrate. The dc power was 50W and the thickness of the $TaSi_xN_y$ film was 1000 Å. Field oxide (3000Å) isolated overlap capacitors were fabricated on p-type wafers and the gate electrodes were prepared by lift-off method. Thermally grown SiO_2 (32 - 35Å) was used as gate dielectrics. A sputtered tungsten-capping layer was deposited on the $TaSi_xN_y$ film. The unpatterned SiO_2/p-Si substrate was used to characterize the thin films. To evaluate the thermal stability, the samples were exposed to rapid thermal anneal (RTA) in Ar ambient at 700°C, 900°C, and 1000°C for 15 seconds. All samples were subjected to forming gas annealing at 400°C for 30min. To investigate the composition of $TaSi_xN_y$ films and the bonding structures of Ta, Si, and N in the film, X-ray photoelectron spectroscopy (XPS) analysis was performed. Electrical resistivity was measured by 4-point probe method. In order to investigate the crystal structure of the films and the interfacial reaction between $TaSi_xN_y$ film and SiO_2, X-ray diffraction (XRD) and Transmission electron microscopy (TEM) analyses were performed. Capacitance-voltage and current-voltage (I-V) characteristics were obtained using HP4284 and HP4155B, respectively. The capacitance was measured at 1MHz frequency on an area of $2.5x10^{-5}$ cm^2. Equivalent oxide thickness (EOT) for the capacitors was obtained using the NCSU CV program.[11,12] Physical oxide thickness was then correlated with EOT extracted from C-V curves. We have also evaluated Ta and TaN_x films to compare their stability on SiO_2 to that of $TaSi_xN_y$.

III. Results and Discussion

Figure 1 shows the XPS core-level spectra of the Si 2p, Ta 4f, and N 1s region for the as-deposited $TaSi_xN_y$ films with different nitrogen flow rates. As shown in fig. 1(a), the binding energy of Si for f_N = 0 % is 99.3eV, indicating Si bonding with Ta.[13] For f_N = 15%, the Si 2p peak at 101.8eV indicates Si-N bond formation.[14] It shows a significant increase of Si-N bonding with increasing N flow. Figure 1(b) shows that the binding energy of Ta $4f_{7/2}$ and Ta $4f_{5/2}$ for $TaSi_xN_y$ films with f_N = 0 % flow are 22.1 eV and 23.8 eV, indicating Ta 4f binding with Si.[15] It was reported that a doublet of Ta 4f peak is due to spin-orbit coupling.[16] In case of 5% and 15% N flow, the peaks of Ta $4f_{7/2}$ shifted to higher energy of 23.0 eV, suggesting Ta-N bonds.[17] In fig. 1(c), the Si-N bonding (397.4 eV)[18] is also observed in the N 1s spectrum of $TaSi_xN_y$ film with f_N = 15 %. XPS analysis shows that the $TaSi_x$ films with f_N = 0 % consisted of Ta-Si bonds, while $TaSi_xN_y$ films with f_N = 5 % are composed of Ta-Si and Ta-N bonds and $TaSi_xN_y$ films with f_N = 15% consisted of a combination of Ta-Si, Ta-N and Si-N bonds. The presence of Si-N bonds is attributed to cause the amorphous nature of the high N containing films.

Table 1 summarizes the composition, resistivity, and crystal structure of $TaSi_xN_y$ film annealed at 1000°C and the equivalent oxide thickness (EOT) in $TaSi_xN_y/SiO_2$/p-Si with annealing temperatures. Increasing the nitrogen flow rate resulted in higher incorporation of N in the film. The nitrogen content in the films increases from 0% to 53% as the percent N_2 flow increases from 0% to 25%. The Si/Ta ratio in $TaSi_xN_y$ films was found to vary for the various N flows for a given Ar flow, which is thought to be due to the differences in sputtering yields of the Ta and Si component with changing sputtering conditions. A steady state condition at the target surface was not reached since the difference of Ta (180.95) and Si atomic weight (28.09) is large enough to cause preferential sputtering of the film. The resistivity of as deposited $Ta_{53}Si_{47}$ film was 220μΩcm and it decreased to ~122 μΩcm after annealing at 1000°C. The resistivity of the film increases sharply, when the f_N exceeds 10%. The sharp increase in resistivity with increased N content can be attributed to the increased Si-N bonding in the film. The resistivity of the films reduces by the subsequent RTA process. As shown in figure 2, an XRD study revealed that the crystal structure of the as-deposited $Ta_{53}Si_{47}$ film was amorphous and the $Ta_{53}Si_{47}$ film transformed to the Ta_5Si_3 phase and $TaSi_2$ phase after annealing at 1000°C. The $Ta_{34}Si_{37}N_{29}$ film (f_N = 5%) has a mixture of crystalline Ta_5Si_3, $TaSi_2$, and amorphous phases. When N flow rates were 10% and higher, the $TaSi_xN_y$ remained amorphous and did not show any crystalline peaks even after anneals up to 1000°C. It has been reported that N in $TaSi_xN_y$ films can suppress the growth of Ta_5Si_3 and $TaSi_2$ microcrystallites, resulting in an amorphous film.[19]

Figure 3 shows the EOT of $TaSi_xN_y/SiO_2/Si$ MOS structure with N flow rate as a function of annealing temperature. $TaSi_xN_y$ ($y > 0$) gates show good stability on SiO_2 even up to 1000°C with negligible change in EOT and no degradation of the CV curves (not shown). On the other hand, $TaSi_x$ (f_N = 0 %) gate showed negligible EOT change up to 900°C and ~ 3Å of EOT increase after 1000°C anneal. It matches the physical thickness of the SiO_2 layer as observed by TEM. We have also investigated the thermal stability of Ta and TaN_x (x=0.86) on SiO_2 after 400 ~1000 °C anneals. The inset of figure

3 shows EOT change of Ta and TaN_x gate as a function of annealing temperature. A large reduction in SiO_2 EOT was observed with Ta thin film on SiO_2 with annealing temperature, indicating serious instability of Ta on SiO_2. The reduction in electrical thickness is attributed to the formation of a high-k layer (TaO_x) and/or the reduction of SiO_2 physical thickness. It was reported that metals such as Ta, Ti, Hf, and V, are very unstable on SiO_2 and are able to reduce it.[20] The instability of Ta on SiO_2 can be understood from thermodynamic consideration, which predicts that Ta on SiO_2 reacts to form Ta_2O_5 and $TaSi_2$.[21] It has been reported that N presence at the grain boundary of TaN can retard the diffusion of species.[22] However, TaN_x gates on SiO_2 show an increase of 4.6Å in EOT after 1000°C anneal. This could be attributed to the oxygen coming from the annealing ambient through TaN_x gate. It was reported that oxygen diffusion decreased with increasing Si composition in $TaSi_xN_y$ film.[9] It was also found to suffer from N diffusion for very thin dielectrics and under high temperature annealing, as indicated by negative shift of the flatband voltage, owing to the positive donor-like charge arising from nitrogen. By adding Si, TaN film can be stabilized further. The improved stability of $TaSi_xN_y$ gates is attributed to the presence of Si and N in the gate electrode, which can improve the film microstructure and the diffusion barrier properties at the gate-dielectric interface.

Figure 4 shows high-resolution TEM of $TaSi_xN_y/SiO_2$ (32Å)/Si stacks after RTA at 1000°C for (a) $TaSi_x$ gate (f_N = 0%) and (b) $TaSi_xN_y$ (f_N = 25%) gate electrodes. The physical thickness of the SiO_2 layer is 36Å (Fig. 1a) and it matches the oxide thickness as obtained from the CV curves. The interface of the $TaSi_x$ and SiO_2 was found to be rough after the annealing. The higher SiO_2 thickness with local SiO_2 bulge indicates a reaction at the $TaSi_x/SiO_2$ interface, which may cause electrical degradation. However, the thinner SiO_2 thickness and smooth $TaSi_xN_y/SiO_2$ interface were observed up to 1000°C, consistent with the results of negligible change in EOT (Fig. 3).

Shown in figure 5 are I-V characteristics obtained for various $TaSi_xN_y$ gates on SiO_2 with anneals at (a) 400ºC and (b) 1000ºC, respectively. The I-V characteristics of capacitors with $TaSi_xN_y$ gates displayed lower gate leakage compared to $TaSi_x$ gates for both 400ºC and 1000ºC anneals. In the case of the $TaSi_xN_y$ gate, no significant increase of J_g (2.0×10^{-6} A/cm^2 at V_g= -1V) was observed after 1000°C anneals. On the other hand, the leakage current density of the $TaSi_x$ gate increased to 5.2×10^{-4} A/cm^2 at V_g= -1V after RTA at 1000°C. It is believed that presence of Si and N improved the chemical-thermal stability of the gate electrode/dielectric interface and retarded the reaction rates and the oxygen diffusion.

IV. CONCLUSION

We have demonstrated that $TaSi_xN_y$ films on SiO_2 provide good thermal stability and results in a minimal change of equivalent oxide thickness and stable leakage current. After an 1000°C anneal, the reaction of $Ta_{53}Si_{47}$ with SiO_2 resulted in the increase of interfacial roughness and oxide thickness in the $TaSi_x/SiO_2$/p-Si structures. The chemical structure of $Ta_{22}Si_{29}N_{49}$ was stable up to 1000°C, exhibiting lower leakage current compared to $TaSi_x$ gate. The presence of Si-N bonds is attributed to the amorphous nature of the high N containing $TaSi_xN_y$ films, which retarded the formation of the interface layer under high temperature annealing. The stability of $TaSi_xN_y$ films may enable high-k dielectrics and metallic electrode to be implemented in advanced CMOS devices.

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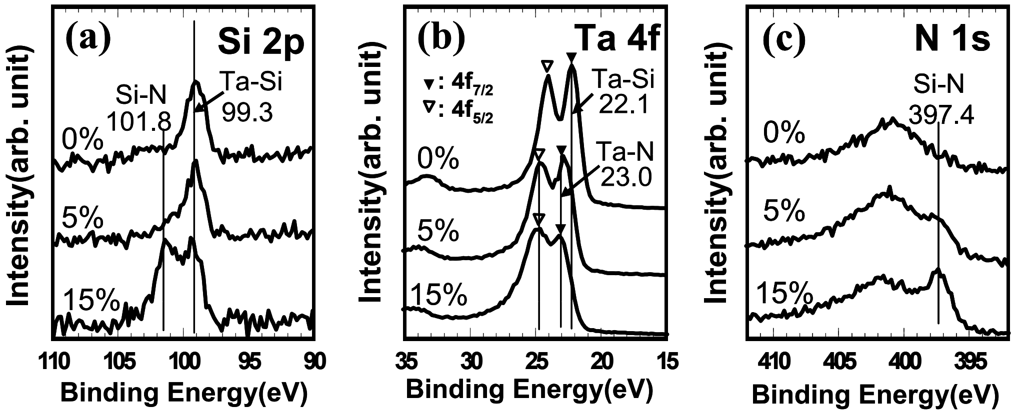

Fig. 1. The XPS spectra of the as-deposited $TaSi_xN_y$ film with different nitrogen flow.

(a) the Si 2p region, (b) the Ta 4f region, and (c) N 1s region

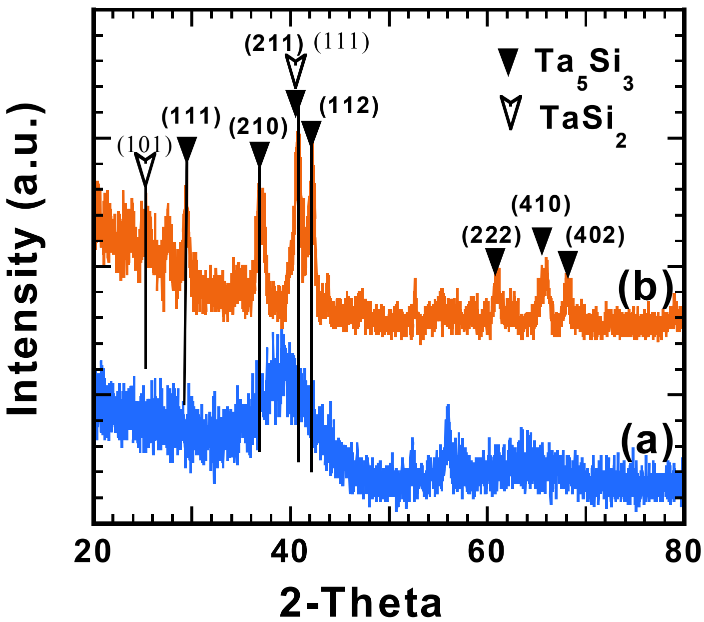

Fig. 2. The XRD pattern for $Ta_{53}Si_{47}$ films

(a) as-deposited and (b) after 1000°C anneals for 15second.

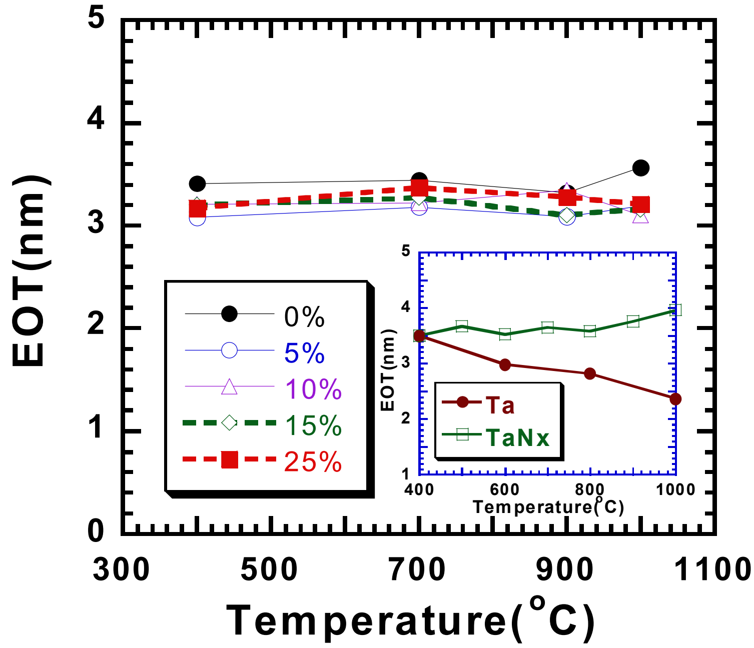

Fig. 3. Equivalent oxide thickness of the various $TaSi_xN_y$ films as a function of annealing temperature.

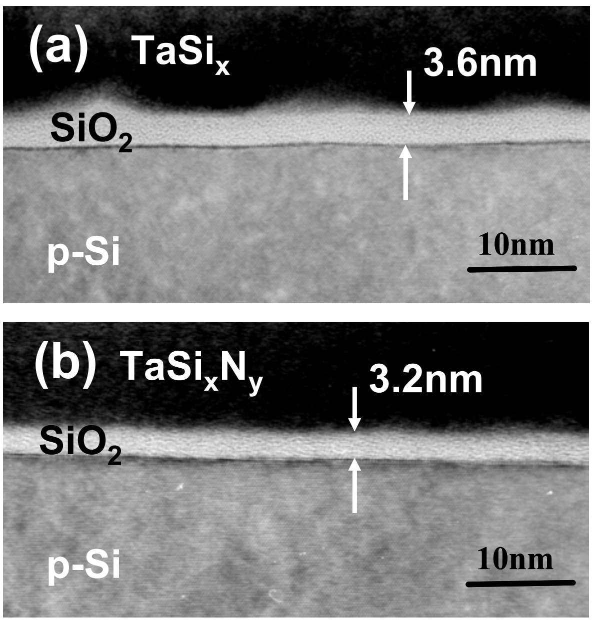

Fig. 4. The HR-TEM of $TaSi_xN_y/SiO_2/Si$ stacks after 1000°C anneals

(a)$TaSi_x$ gate and (b)$TaSi_xN_y$ (N_2 flow 25%) gate electrodes

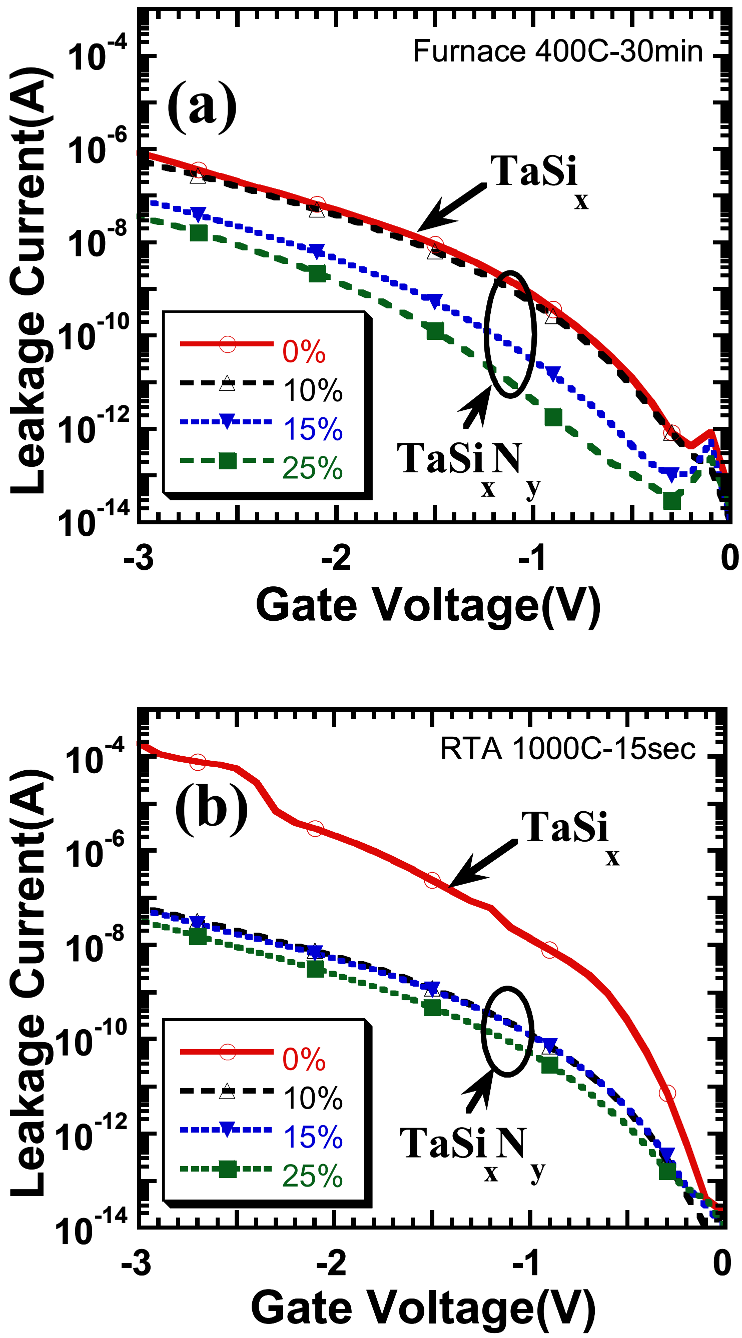

Fig. 5. Typical I-V curves of $TaSi_xN_y$ electrode capacitor with the N_2 flow rate.

(a) Furnace annealing at 400ºC for 30min and (b) RTA at 1000 ºC for 30sec.

N_2/Ar flow rate	Composition	Resistivity ($\mu\Omega$cm)	Crystal structure	$T_{ox\text{-}eq}$(nm) 400°C	900°C	1000°C
0%	$Ta_{53}Si_{47}$	122	Ta_5Si_3+$TaSi_2$	3.41	3.32	3.57
5%	$Ta_{34}Si_{37}N_{29}$	707	mixture*	3.08	3.09	3.19
10%	$Ta_{28}Si_{31}N_{41}$	1941	amorphous	3.21	3.35	3.10
15%	$Ta_{22}Si_{29}N_{49}$	8222	amorphous	3.20	3.10	3.16
25%	$Ta_{19}Si_{28}N_{53}$	-	amorphous	3.17	3.28	3.21

*** mixture = Ta_5Si_3+$TaSi_2$+amorphous**

Table. 1. Properties of Ta-Si-N thin films and equivalent oxide thickness with annealing temperatures for $TaSi_xN_y$ capacitors on SiO_2.

3.4 Summary

We have shown that $TaSi_xN_y$ films on SiO_2 provide good thermal stability up to 1000ºC resulting in minimal change of EOT and V_{FB}, while demonstrating low leakage current. The improved stability of $TaSi_xN_y$ gates is attributed to the presence of Si and N in the gate electrode, which can improve the film microstructure and the diffusion barrier properties at the gate-dielectric interface. The presence of Si-N bonds is attributed to the amorphous nature, which retarded the formation of the interface layer under high temperature annealing.

CHAPTER 4

Optimizing the composition of $TaSi_xN_y$ gate electrode on SiO_2

In this chapter, the role of N and Si on the electrical properties will be discussed. In the first paper, the effects of nitrogen on electrical and structural properties in $TaSi_xN_y$ /SiO_2/p-Si MOS capacitor are presented. $TaSi_xN_y$ films with various compositions were characterized by Rutherford backscattering spectroscopy, Auger electron spectroscopy and transmission electron microscopy. Capacitance-voltage and current-voltage characteristics were also investigated.

In the second paper, the effects of silicon and nitrogen on the electrical properties of $TaSi_xN_y$ gate electrode were investigated. The thermal stability of $TaSi_xN_y$/SiO_2/p-type Si stacks was evaluated by measuring the flatband voltage and equivalent oxide thickness at 400°C and 900°C in Ar. the role of the Si and N content in the films on the electrical and physical properties are presented. Finally, an optimized composition of $TaSi_xN_y$ gates suitable for NMOS gates is presented.

4.1 The Effects of Nitrogen on Electrical and Structural Properties in $TaSi_xN_y$ /SiO_2/p-Si MOS Capacitors

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ABSRACT

In this work, we report the effects of nitrogen on electrical and structural properties in $TaSi_xN_y$ /SiO_2/p-Si MOS capacitors. $TaSi_xN_y$ films with various compositions were deposited by reactive sputtering of $TaSi_2$ or by co-sputtering of Ta and Si targets in argon and nitrogen ambient. $TaSi_xN_y$ films were characterized by Rutherford backscattering spectroscopy and Auger electron spectroscopy. It was found that the workfunction of $TaSi_xN_y$ (Si>Ta) with varying N contents ranges from 4.2 to 4.3 eV. Cross-sectional transmission electron microscopy shows no indication of interfacial reaction or crystallization in $TaSi_xN_y$ on SiO_2, resulting in no significant increase of leakage current in the capacitor during annealing. It is believed that nitrogen retards reaction rates and improves the chemical-thermal stability of the gate-dielectric interface and oxygen diffusion barrier properties.

INTRODUCTION

As gate oxide thickness decreases, the capacitance associated with the depleted layer at the poly-Si/gate dielectric interface becomes significant, making it necessary to consider alternative gate electrodes [1]. The search for metallic gates faces many challenges since they must have compatible work functions, process compatibility and thermal/chemical interface stability with underlying dielectric [2]. Most metal gate electrodes studied to date suffer from high temperature instability resulting in a degraded interface with the underlying dielectric [3]. $TaSi_xN_y$ films have been studied both as a barrier layer for Cu interconnection and as a bottom electrode for DRAM capacitors [4-6]. They have shown low resistivity and excellent thermal/chemical stability against high temperature processing. It has also been reported that $TaSi_xN_y$ have excellent oxygen diffusion barrier properties up to 900^{o}C [7-9]. Recently, $TaSi_xN_y$ films have been investigated as a metal gate electrode owing to their good thermal stability and NMOS compatible workfunctions [10]. In a previous paper, we evaluated the electrical properties of the $TaSi_xN_y$ films for gate electrode applications [10]. We have shown that $TaSi_xN_y$ films on SiO_2 provide good thermal stability up to 1000^{o}C resulting in minimal change of oxide thickness and demonstrating low leakage currents.

In this work, we report the effects of the nitrogen in the $TaSi_xN_y$ gate on the electrical and structural properties. We have also evaluated the thermal and chemical stability of $TaSi_xN_y$ thin films with various compositions under high temperature treatments.

EXPERIMENTAL

$TaSi_xN_y$ films were deposited on the SiO_2 gate oxides using reactive sputtering of $TaSi_2$ or reactive co-sputtering of Ta and Si target in argon and nitrogen ambient. The target was 2 inches in diameter with 99.9% purity. The flow ratio of $N_2/(N_2+Ar)$ was varied from 0% to 15%. The deposition pressure was 5.5 mTorr. No intentional heating was applied to the substrate. In order to change the composition of $TaSi_xN_y$ films, the RF sputtering power was varied from 70W to 100W. Field oxide (3000Å) isolated overlap capacitors were fabricated on p-type wafers using lift-off to define the gate electrodes. Thermally grown SiO_2 with several oxide thicknesses were used as dielectrics. A sputtered tungsten-capping layer was deposited on $TaSi_xN_y$ film. The base pressure of the chamber was < $5x10^{-8}$ Torr. To evaluate the thermal stability, the samples were subjected to a rapid thermal anneal in Ar ambient at 900^{o}C for 15seconds. All samples were then subjected to a forming gas annealing at 400^{o}C for 30min. The composition of the $TaSi_xN_y$ film was obtained by Rutherford backscattering spectroscopy (RBS) and Auger electron spectroscopy (AES) analysis. X-ray photoelectron spectroscopy (XPS) and transmission electron spectroscopy (TEM) analysis were performed to get the bonding information in the films and interfacial reaction between $TaSi_xN_y$ film and SiO_2. Capacitance-voltage and current-voltage characteristics were obtained using HP4284 and HP4155B, respectively. The capacitance was measured at various frequencies on an area of $2.5x10^{-5}cm^2$. The flat band voltage (V_{FB}) and equivalent oxide thickness (EOT) for the capacitors were obtained using the NCSU CV program.

RESULTS AND DISCUSSION

Composition of the films

To correlate the composition of the $TaSi_xN_y$ film to the process conditions, we obtained Rutherford backscattering spectroscopy (RBS) and Auger electron spectroscopy (AES) Spectra. Table. 1 summarizes the compositions of the $TaSi_xN_y$ films as a function of N_2 flow rates. It indicates that increasing N_2 flow rate results in increasing N concentration in the films. In the case of $TaSi_x$ film without N_2 flow, the Si/Ta ratio was < 1 and this film had a predominance of the Ta_5Si_3 phase as measured by X-ray diffraction. The resistivity of the as-deposited $TaSi_x$ film was 220μΩcm which decreased to ~122 μΩcm after annealing at 1000°C. It has been reported that N in $TaSi_xN_y$ films can suppress the growth of Ta_5Si_3 and $TaSi_2$ microcrystallites resulting in an amorphous film [11]. This amorphous film is expected to have good thermal/chemical stability.

Work function

In order to decouple the fixed charges from the workfunction, several SiO_2 thicknesses were used. The flatband voltage as a function of equivalent oxide thickness (EOT) is shown in figure 1, in which the y-intercept indicates the workfunction difference (Φ_{ms}). As shown in figure 1 (a), only a slight increase in workfunction was observed for the Si rich $TaSi_xN_y$ gate capacitors as nitrogen increase. The workfunction values of $TaSi_xN_y$ with varying N contents ranges from 4.2 to 4.3eV, suggesting that $TaSi_xN_y$ films have workfunctions appropriate for NMOS devices. Diffusion of nitrogen from the gate to the Si-SiO_2 interface, which typically occurs with TaN_x gates, was not observed with Si-rich $TaSi_xN_y$ gates since there was no change in the slope of V_{FB} vs T_{ox} curves for SiO_2 <

4nm. As shown in figure 1 (b), the workfunction values of Ta-rich $TaSi_x$ gate are similar to the Si-rich $TaSi_x$ gate (~ 4.2eV). When N (flows between 5 and 15%) is added to Ta-rich $TaSi_x$ films, the work function increases up to ~ 0.3eV. The work function value of $TaSi_xN_y$ with N 15%, which was obtained from V_{FB} is ~ 4.6eV, similar to the reported value of TaN_x [12]. Moreover, the change in slope of the V_{FB} vs T_{ox} curves for the Ta-rich $TaSi_xN_y$ gate with N 15%, indicated nitrogen diffusion from the gate to the Si-SiO_2 interface.

C-V characteristics

Figures 2 (a), (b) and (c) display the CV characteristics of Ta-rich $TaSi_xN_y$ gate after annealing at 400°C and 900°C as a function of N_2 flow. As seen in figure (a), a negligible change in V_{FB} (-0.66V → -0.69V) and EOT (24.9A → 25.2A) was observed. In the case of 5% N_2 flow, a positive shift in V_{FB} (-0.68V → -0.41V) was observed, indicating the increase in work function due to $TaSi_2$ formation at the gate-dielectric interface after high temperature annealing. In the case of 15% N_2 flow, a negative shift in V_{FB} (-0.64V → -0.84V) was observed, indicating increase of fixed charges in the dielectric. Therefore, 10% N_2 resulted in a $TaSi_xN_y$ gate condition that provided stability of EOT and V_{FB}. For Si-rich $TaSi_xN_y$ gate, a positive shift of the C-V curves was observed under high temperature annealing. It was reported that the V_{FB} change is attributed to a change in workfunction due to a Ta-disilicide layer at the interface between the electrode and the dielectric [13].

I-V characteristics

I-V characteristics were obtained for both $TaSi_x$ and $TaSi_xN_y$ gate on SiO_2 and are shown in figure 3 (a) and (b) for anneals of 400ºC and 1000ºC, respectively. The I-V characteristics of capacitors with $TaSi_xN_y$ gates displayed lower gate leakage compared to $TaSi_x$ gates for both 400ºC and 1000ºC anneals. It is believed that the microstructure of the film and the presence of nitrogen retards reaction rates and improves the chemical stability of the gate-dielectric interface. In the case of the $TaSi_xN_y$ gate, no significant increase of J_g ($2.0x10^{-6}$ A/cm^2 @ at V_g= -1V) was observed after 1000^{o}C anneals. On the other hand, leakage current density of the $TaSi_x$ gate increased to $5.2x10^{-4}$ A/cm^2 @ at V_g= -1V after a 1000^{o}C anneal.

Microstructure

Figure 4 shows the HR-TEM of $TaSi_xN_y/SiO_2/Si$ stacks after a 1000^{o}C anneal for $TaSi_x$ gate and $TaSi_xN_y$ (N_2 flow 25%) gate electrodes. In a previous paper, we reported that $TaSi_xN_y$ gates showed good stability on SiO_2 even up to 1000^{o}C with no degradation of the CV curves and negligible change in equivalent oxide thickness (EOT) [10]. However, $TaSi_x$ gate showed up to a ~ 3Å EOT change after 1000^{o}C anneal. As shown in figure 4, the physical thickness of the SiO_2 layer is 36Å and it matches the oxide thickness as obtained from the CV curves. The interface of the $TaSi_x$ and SiO_2 was found to be rough after the annealing. The rough interface can cause the increase of leakage currents and a decrease of EOT. On the other hand, the interface of the $TaSi_xN_y/SiO_2$ remained smooth up to 1000^{o}C. The smooth interface is correlated with the stable leakage current density even after a 1000^{o}C anneal. The XPS analysis indicated that a) $TaSi_x$ films consisted of

Ta-Si bonds, b) $TaSi_xN_y$ (N_2 flow = 5%) consisted of Ta-Si and Ta-N bonds and c) $TaSi_xN_y$ (N_2 flow = 25%) consisted of a combination of Ta-Si, Ta-N and Si-N bonds. The presence of Si-N bonds is attributed as the cause of the amorphous nature of the high N containing films [11]. These amorphous films are expected to have good thermal and chemical stability. It is believed that nitrogen retards reaction rates and improves the chemical-thermal stability of the gate-dielectric interface and the oxygen diffusion barrier properties.

CONCLUSION

We investigated the effects of the nitrogen on the electrical and structural properties in $TaSi_xN_y$ /SiO_2/p-Si MOS capacitors. We found the workfunction of $TaSi_xN_y$ (Si>Ta) with varying N contents ranges from 4.2 ~ 4.3 eV. However, the workfunction of $TaSi_xN_y$ (Ta>>Si) were higher and close to those observed with TaN_x. Stability of leakage currents was observed in $TaSi_xN_y$ gates even after 1000°C. This was attributed to the lack of interface reactions and amorphous microstructure of these films. It is believed that nitrogen retards reaction rates and improves the chemical-thermal stability of the gate-dielectric interface and the barrier properties of oxygen diffusion.

ACKNOWLEDGEMENTS

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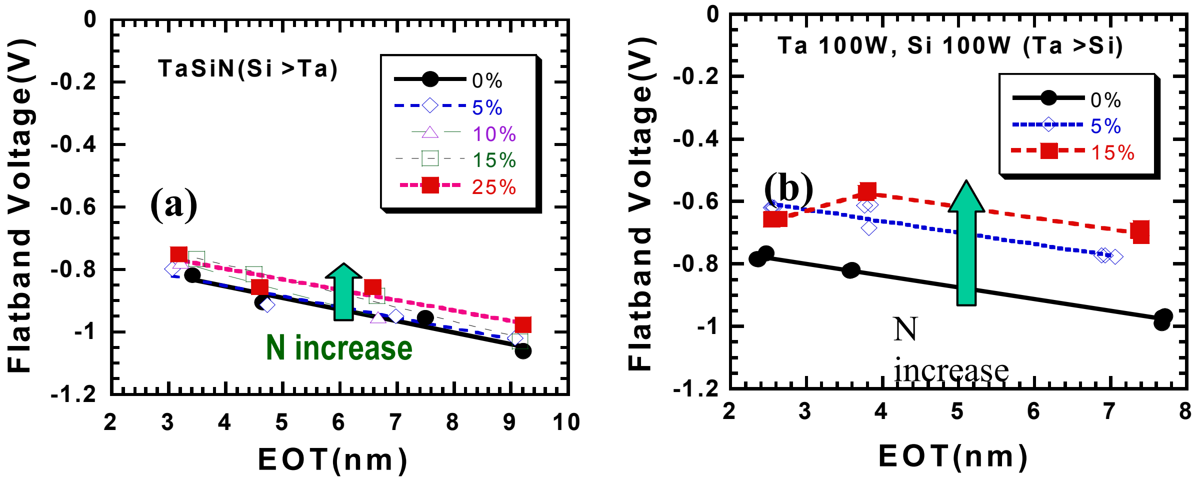

Figure 1. V_{FB} vs. EOT at the various $TaSi_xN_y$ electrodes after forming gas annealing at 400°C. (a) reactive sputtering of $TaSi_2$, (b) reactive co-sputtering of Ta and Si in Ar and N_2 ambient.

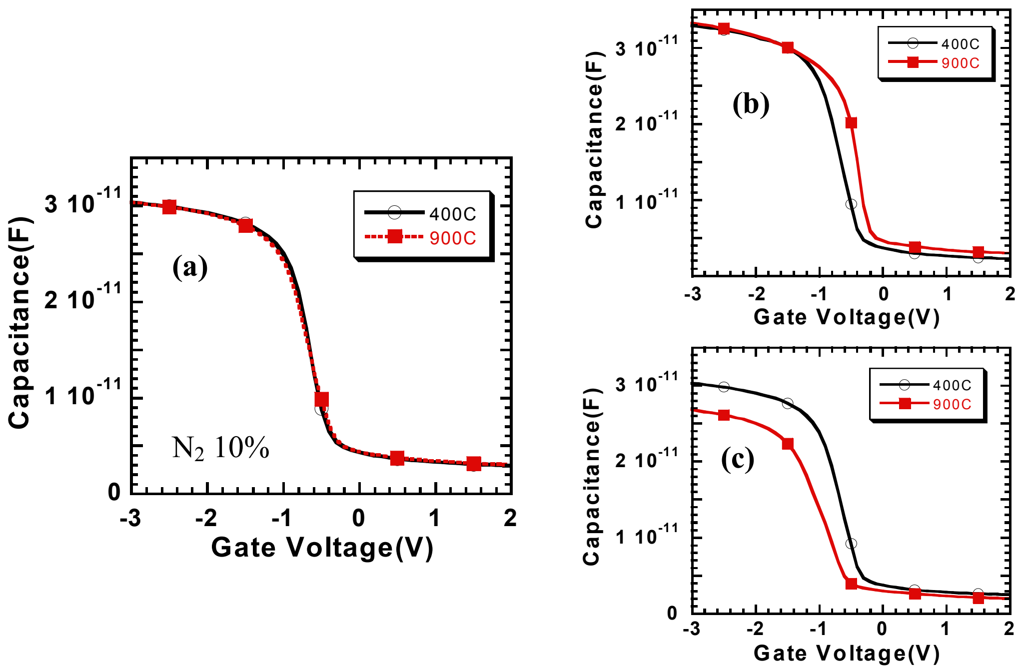

Figure. 2. The C-V curves of $TaSi_xN_y$ electrode capacitor with the N_2 flow rate, after annealing at 400ºC and 900ºC. Capacitor area =2.5E-5cm^2 (a) 10 %, (b) 5%, (c) 15% N_2 flow.

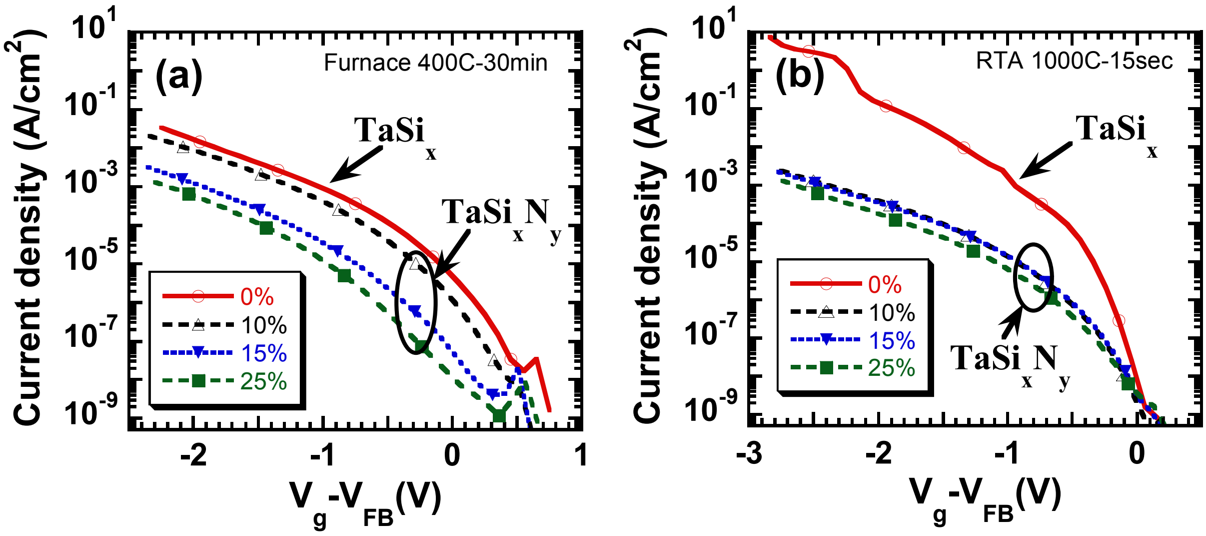

Figure 3. Typical I-V curves of $TaSi_xN_y$ electrode capacitor with the N_2 flow rate. (a) Furnace annealing at 400ºC for 30min and (b) RTA at 1000 ºC for 30sec.

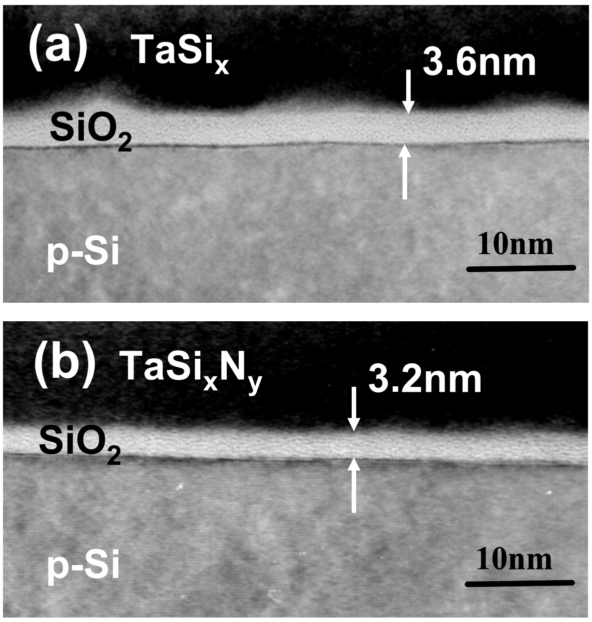

Figure. 4. The HR-TEM of $TaSi_xN_y/SiO_2/Si$ stacks after 1000°C anneals. (a)$TaSi_x$ gate., (b)$TaSi_xN_y$ (N_2 flow 25%) gate electrodes.

N_2/Ar Flow rate (%)	Compositions (at.%)					
	(a)$TaSi_xN_y$			**(b)$TaSi_xN_y$**		
	Ta	Si	N	Ta	Si	N
0	46.5	40.0				
5	29.0	32.0	37.3	48.7	10.5	40.8
10	25.0	28.0	45.2	41.8	9.8	48.4
15	21.9	25.5	51.7	39.9	9.6	50.5
25	16.5	23.0	59.1			

Table. 1. The compositions of the $TaSi_xN_y$ films as a function of N_2 flow rates. (a) by reactive sputtering of $TaSi_2$, (b) by reactive co-sputtering of Ta and Si target in Ar and N_2 ambient.

4.2 Effect of the Composition on the Electrical Properties of $TaSi_xN_y$ Metal Gate Electrodes

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Elec. Dev. Lett., 24(7), 439 (2003).

Effect of the Composition on the Electrical Properties of $TaSi_xN_y$ Metal Gate Electrodes

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Abstract

In this work, the effect of silicon and nitrogen on the electrical properties of $TaSi_xN_y$ gate electrode was investigated. The $TaSi_xN_y$ films were deposited on the SiO_2 using reactive co-sputtering of Ta and Si target in Ar and N_2 ambient. The thermal stability of $TaSi_xN_y/SiO_2$/p-type Si stacks was evaluated by measuring the flatband voltage and equivalent oxide thickness at 400°C and 900°C in Ar. It was found that under high temperature anneals, Si-rich $TaSi_xN_y$ films resulted in $TaSi_2$ formation at the electrode-dielectric interface, which increased the work function. Reducing the Si content alone did not prevent the $TaSi_2$ formation while removing Si completely by utilizing TaN resulted in work functions that were too high. The presence of both Si and N was deemed necessary and their content was critical in obtaining optimized $TaSi_xN_y$ gates that are suitable for NMOS devices.

I. INTRODUCTION

$TaSi_xN_y$ films have been studied both as a barrier layer for Cu interconnection and a bottom electrode for DRAM capacitors [1-3]. It has also been reported that $TaSi_xN_y$ is an excellent oxygen diffusion barrier up to 900^{o}C [4-6]. We have reported that the work function of $TaSi_xN_y$ films changes from 4.2~4.3eV after 400ºC anneal to ~4.8eV after 900ºC anneal due to the formation of a Ta-disilicide layer at the interface of the electrode and the dielectric [7]. In this work, we have investigated the role of N and Si in $TaSi_xN_y$ gates. By optimizing the Si and N content in the $TaSi_xN_y$ films, we have stabilized the flat band voltage and the equivalent oxide thickness of the $TaSi_xN_y$ gate electrode on SiO_2.

II. EXPERIMENTAL

$TaSi_xN_y$ films were deposited on the SiO_2 gate oxides using reactive co-sputtering of Ta and Si target in argon and nitrogen ambient. The ratio of $N_2/(N_2+Ar)$ flow rate, f_N, was varied from 0% to 15%. In order to change the composition of $TaSi_xN_y$ films, RF sputtering power was varied from 70W to 100W. Field oxide isolated overlap capacitors were fabricated on p-type wafers using lift-off to define the gate electrodes. To evaluate the thermal stability, the samples were annealed in Ar ambient at 700^{o}C and 900^{o}C for 15sec. All samples were annealed in 10% H_2/N_2 at 400^{o}C for 30min. The composition of the film was obtained by Auger electron spectroscopy (AES). In order to measure the diffusion of N through dielectric, Secondary ion mass spectroscopy (SIMS) analysis was performed. Capacitance-voltage (C-V) and current-voltage (I-V) characteristics were obtained using HP4284 and HP4155B, respectively. The flat band voltage (V_{FB}) and equivalent oxide thickness (EOT) for the capacitors were obtained using the NCSU CV program.

III. RESULTS AND DISCUSSION

Fig. 1 shows the effect of adding nitrogen (N) on the V_{FB} of Ta, Ta-rich $TaSi_x$ and Si-rich $TaSi_x$ gate electrodes on SiO_2 (25~30 Å). As shown, the V_{FB} for Ta gate is -0.90V, which translates to Φ_m value of 4.2eV and agrees with reported values [8]. When N_2 (5~10% flow rate) is added to Ta, the V_{FB} increases to -0.61V. A V_{FB} vs. EOT extraction of various thicknesses indicated that these films resulted in Φ_m increase of up to 0.3eV. The Φ_m value for TaN_x gates as obtained from V_{FB} is ~4.5eV, similar to reported values [9]. As the N_2 flow rate was increased, a negative shift of V_{FB} was observed. This shift was found to occur at lower N_2 flow rates as the SiO_2 thickness decreased. This shift is attributed to the presence of fixed positive charge caused by N incorporation in the dielectric film. It was found that in poly-Si/Si_3N_4/SiO_2/Si structures, the V_{FB} becomes more negative with increasing nitride thickness owing to the additional charge arising from N diffusion from the bulk nitride [10]. To confirm the presence of N in the dielectric, Secondary Ion Mass Spectroscopy (SIMS) analysis was performed. Fig. 2(a) shows the nitrogen profile in TaN_x/SiO_2/Si structures after annealing at 1000ºC for 15sec. As shown, a large nitrogen peak at the SiO_2/Si interface is observed and attributed to N diffusion from TaN_x gate through the dielectric. In comparison to TaN_x, the addition of N to Ta-rich $TaSi_xN_y$ (Ta/Si =4) films resulted in only slight increases of the Φ_m values. In addition, the $TaSi_xN_y$ films did not show a negative V_{FB} shift at high N flow rates suggesting that N diffusion into the dielectric was suppressed. Fig. 2(b) shows the nitrogen profile in $TaSi_xN_y/SiO_2/Si$ structures after annealing at 1000ºC for 15sec, analyzed by SIMS. No nitrogen peak at the SiO_2/Si interface was observed for $TaSi_xN_y$ gates. It demonstrates the Si content in $TaSi_xN_y$ gate indeed retards the diffusion of nitrogen. The suppression of N incorporation for $TaSi_xN_y$ gates was attributed to the presence of Si in the gate electrode, which can act as a diffusion barrier. The effect of increased N incorporation in Si-rich $TaSi_xN_y$ (Si/Ta=1.3) films resulted in complete suppression of N diffusion while resulting only in a minimal increase of Φ_m. . Therefore, the presence of Si in the $TaSi_xN_y$ gates acts as a diffusion barrier for N and also produces a non-varying Φ_m dependence on N. Although, Ta-rich $TaSi_xN_y$ films also suppress N diffusion, their work functions were slightly larger than Si rich $TaSi_xN_y$. Although both the Ta-rich and Si-rich $TaSi_xN_y$ films provided NMOS compatible Φ_m values after a 400°C anneal, their high temperature behavior must also be evaluated. In our previous work, we have reported that Φ_m values of Si-rich $TaSi_xN_y$ dramatically increase after a 900°C anneal. Barrier height extrapolations using Fowler-Nordheim analysis as a function of temperature also confirmed that the V_{FB} increase was indeed due to a change in Φ_m [7]. It is believed that the $TaSi_2$ formation at the gate-dielectric interface causes the Φ_m to increase. Under high temperature anneals, the presence of Si in the $TaSi_xN_y$ gate results in the formation of $TaSi_2$ at the dielectric-electrode interface regardless of the N content. Therefore to suppress $TaSi_2$ formation it is necessary to understand and optimize the role of Si and N in $TaSi_xN_y$ films. To this end, we have evaluated the effect of reducing the Si content in the $TaSi_xN_y$ film while optimizing the N content concurrently.

Fig. 3 shows the V_{FB} of various $TaSi_xN_y$ gate capacitors as a function of EOT before and after high temperature annealing at 900ºC. The y-intercept indicates the work function difference (Φ_{ms}), which is decoupled from the effect of fixed charges. As shown in fig. 3(a), the Φ_{ms} of $TaSi_x$ films without nitrogen is ~ -0.69 ± 0.02eV. However, an increase in Φ_m after annealing at 900°C is observed and is attributed to the formation of $TaSi_2$. Furthermore, these gates also indicated further instability as is evident by the increase of accumulation capacitance, which is attributed to the reduction in SiO_2 accompanied by the formation of an interfacial high-k layer (TaO_x) during annealing. The instability of Ta rich gates on SiO_2 can be understood from the thermodynamics which predict that Ta on SiO_2 react to form both Ta_2O_5 and $TaSi_2$ [11]. Fig. 3(b) shows that when N is added to the film (f_N= 5%), the increase in Φ_m at higher temperatures is minimized indicating the retardation of reaction rates at the interface. When the N content is further increased (f_N= 10%), the thermal stability of the gate drastically improves and a minimal change in Φ_m is observed with annealing temperature in Fig. 3(c). However, too much N in the gate (f_N= 15%) results in diffusion of N as is seen by the change of slope and linearity of V_{FB} vs. EOT in fig. 3(d).

Fig. 4 shows C-V curves of the optimized $Ta_{39}Si_{12}N_{49}$ gate electrodes on 25Å SiO_2 before and after annealing at 900°C in Ar for 15sec. The extracted V_{FB} translates to Φ_m value of 4.33 ~ 4.36eV, which is compatible with NMOS devices. The inset figure shows gate leakage current (J_g) characteristics of $Ta_{39}Si_{12}N_{49}$ gate electrodes after 400°C and 900°C annealing. No significant change of (J_g) was observed after 900°C anneals. The V_{FB} and EOT trends of Ta-rich $TaSi_xN_y$ gate at 400°C and 900°C as a function of N flow are summarized in Table 1. A shift of C-V curves for Ta-rich $TaSi_xN_y$ gate was observed after annealing and was related to the N content. For the case of 5% N_2 flow, a positive shift in V_{FB} (-0.64V → -0.41V) was observed, indicating a change in work function. For the case of 15% N_2 flow, a negative shift in V_{FB} (-0.65V → -0.86V) was observed, indicating positive fixed charges arising from N diffusion. For 10 % N_2 flow, a negligible shift in V_{FB} (-0.64V → -0.68V) and EOT (2.4nm → 2.5nm) was observed under high temperature annealing. Therefore, by understanding and controlling the Si and N content in the $TaSi_xN_y$ films, we have achieved a NMOS compatible metal alloy that is stable with regards to EOT and V_{FB} under high temperature processing and is therefore an excellent candidate for scaled CMOS devices.

IV. CONCLUSION

The role of Si and N was investigated in $TaSi_xN_y$ gate electrodes. It was found that the presence of excess Si resulted in an increase of Φ_m due to $TaSi_2$ formation at the gate-dielectric interface. This effect was prevented by reducing the Si content and adding N to the film. The N content was optimized since too little did not prevent the $TaSi_2$ formation and too much resulted in N diffusion. Also, the lack of Si (i.e. TaN_x) resulted in undesirable Φ_m values. $Ta_{39}Si_{12}N_{49}$ composition was considered optimum for NMOS gates based on the excellent stability of EOT and V_{FB} at high temperatures. It is believed that the presence of Si-N bonds in the film improves the thermal stability of the gate-dielectric interface while maintaining appropriate work function.

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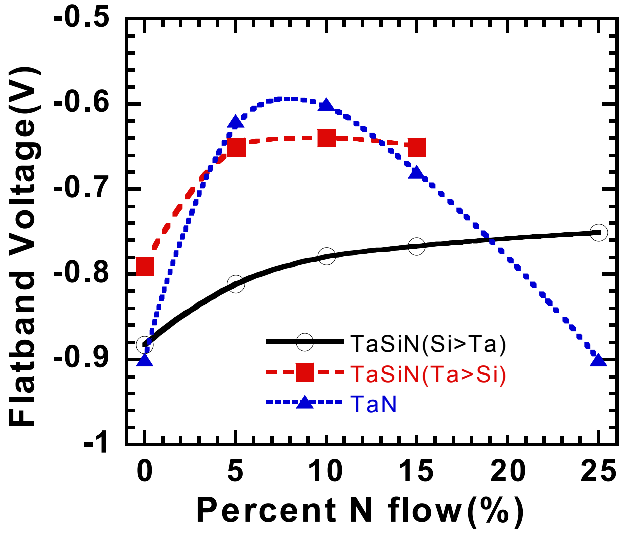

Fig. 1. The flat band voltage (V_{FB}) of the Ta, Ta-rich $TaSi_x$ and Si-rich $TaSi_x$ capacitors on SiO_2 with oxide thickness (T_{ox}) of 25 ~ 30 Å as a function of percent N_2 flow at 400 °C. The capacitance was measured at a frequency of 1MHz on an area of $2.5x10^{-5}cm^2$.

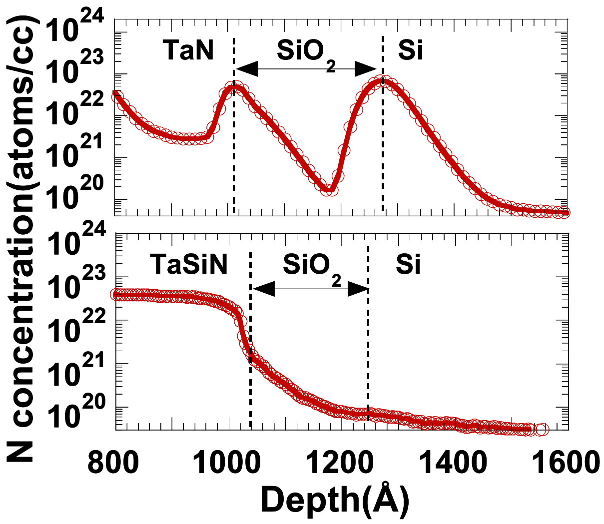

Fig. 2. The nitrogen profile for nitrogen diffusion from gate electrode through SiO_2 at 1000°C for 15sec. (a) $TaN_x/SiO_2/Si$ and (b) $TaSi_xN_y/SiO_2/Si$ structures.

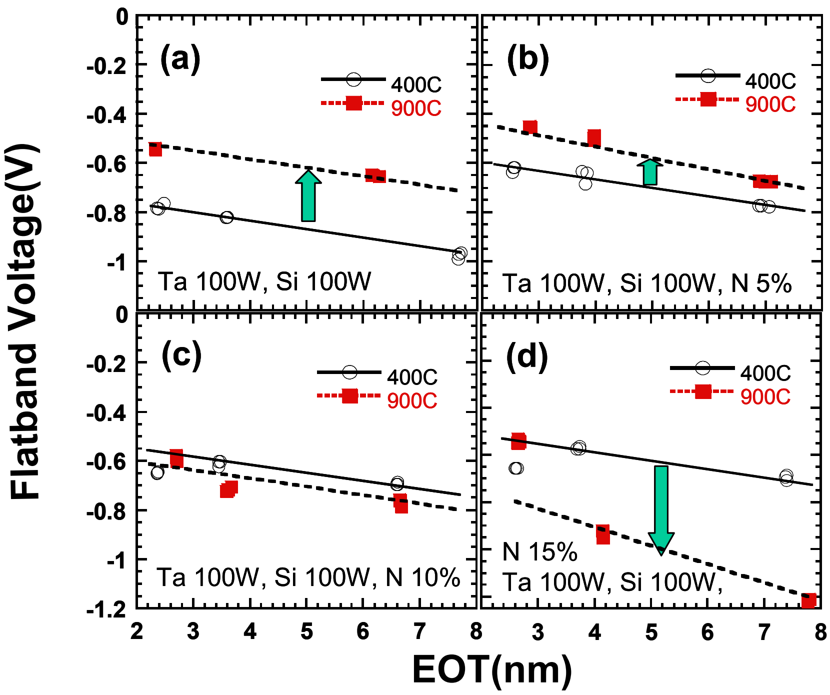

Fig. 3. The flat band voltage (V_{FB}) of $TaSi_xN_y$ gate capacitors as a function of equivalent oxide thickness (EOT) before and after the high temperature annealing at 900ºC. Ta 100W and Si 100W rf power were used. (a) Without N flow, (b) N 5% flow, (c) N 10% flow, and (d) N 15% flow.

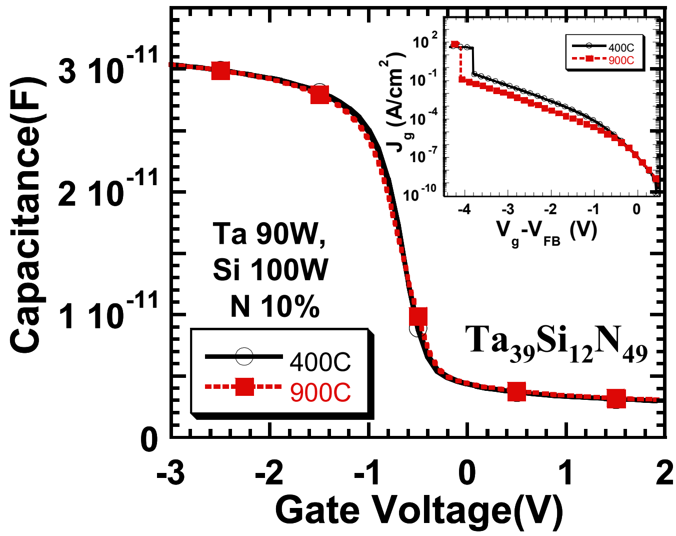

Fig. 4. The C-V curves of $Ta_{39}Si_{12}N_{49}$ capacitors with optimized composition after anneals at 400°C and 900°C. Ta 90W and Si 100W rf power were used with f_N=10%. The inset figure shows gate leakage current (J_g) – gate voltage (V_g-V_{FB}) of $Ta_{39}Si_{12}N_{49}$ gate electrodes at 400°C and 900°C annealing.

Percent N2 flow	V_{FB} (V)		EOT(Å)	
	400°C	900°C	400°C	900°C
N 5%	-0.68	-0.41	24.2	25.6
N10%	-0.66	-0.69	24.9	25.2
N15%	-0.64	-0.84	27.1	30.0

Table 1. V_{FB} and EOT of $TaSi_xN_y$ capacitor as a function of N_2 flow at different temperatures. Ta 90W and Si 100W RF power were used.

4.3 Summary

The physical and electrical properties of $TaSi_xN_y$ films were evaluated for NMOSFET gate electrode applications. The results indicated that the workfunction of $TaSi_xN_y$ is compatible with NMOS devices. We found the workfunction of $TaSi_xN_y$ (Si>Ta) with varying N contents ranges from 4.2 ~ 4.3 eV. However, the workfunction of $TaSi_xN_y$ (Ta>>Si) were higher and close to those observed with TaN_x. The role of Si and N was investigated in $TaSi_xN_y$ gate electrodes with annealing. It was found that the presence of excess Si resulted in an increase of Φ_m due to $TaSi_2$ formation at the gate-dielectric interface under high temperature anneals. This effect was prevented by reducing the Si content and adding N to the film. The N content was optimized since too little did not prevent the $TaSi_2$ formation and too much resulted in N diffusion. Also, the lack of Si (i.e. TaN_x) resulted in undesirable Φ_m values. It is believed that the presence of Si-N bonds in the film improves the thermal stability of the gate-dielectric interface while maintaining appropriate work function.

In summary, we have shown that $TaSi_XN_Y$ films on SiO_2 provide good thermal stability up to 1000ºC resulting in minimal change of EOT and V_{FB}, while demonstrating low leakage current. The improved stability of $TaSi_xN_y$ gates is attributed to the presence of Si and N in the gate electrode, which can improve the film microstructure and the diffusion barrier properties at the gate-dielectric interface. Furthermore, this increased stability does not come at the cost of the carrier concentration. Although the work function value is slightly higher than the desired 4.2eV, it still provides a reasonable compromise since to date not other gate with a lower work function and an equivalent stability has been reported. This stability of $TaSi_xN_y$ films may enable high-k dielectrics and metallic electrode to be implemented in advanced CMOS devices.

CHAPTER 5

Electrical characteristics metal gate electrodes on HfO_2 dielectrics

In this chapter, we have evaluated the properties of metal gate electrodes on high-K dielectrics. To this end, a HfO_2 gate dielectric process was developed and evaluated with Ru and Ta based metals (Ta, TaN_x, and $TaSi_xN_y$). Furthermore, the interface charges and oxide fixed charges were obtained using conductance method and C-V analysis and then correlated with sputtering damage encountered during gate metal sputtering. The discussion will be presented in two papers that have been submitted for publication.

In the first paper, we investigated the electrical characteristics of HfO_2 thin films prepared by RF magnetron sputtering of thin hafnium layers, followed by an oxidation process. An equivalent oxide thickness of 12.5Å was obtained in Ru/HfO_2/n-Si MOS capacitors, with a low leakage current density of 1.7 x 10^{-2}A/cm^2 at Vg-V_{FB}=1V in accumulation. The work function of Ru gate extracted from C-V analysis was 5.02 eV, suggesting Ru has the appropriate work function for P-MOSFETs on HfO_2. The electrical characteristics of Ru/HfO_2/n-Si MOS capacitor are discussed in detail with post metal annealing temperatures.

In the second paper, we investigated the electrical characteristics of $TaSi_xN_y$/HfO_2/p-Si MOS capacitor. An equivalent oxide thickness of 11.2Å and the flatband voltage of -0.78V were obtained with a low leakage current density of 4.1x10^{-2}A/cm^2 at V_g-V_{FB}= -1V in accumulation. The electrical characteristics of Ta-based metals/HfO_2/p-Si MOS capacitor are discussed in detail and related with post metal annealing temperature.

5.1 Electrical characteristics of HfO_2 dielectrics with Ru metal gate electrodes

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Electrical characteristics of HfO_2 dielectrics with Ru metal gate electrodes

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Abstract

Hafnium dioxide, HfO_2, thin films were prepared by RF magnetron sputtering of thin hafnium layers, followed by an oxidation process. Ru was deposited on the HfO_2 as the gate electrode. An equivalent oxide thickness of 12.5Å was obtained in Ru/HfO_2/n-Si MOS capacitor with a low leakage current density of 1.7 x 10^{-2}A/cm^2 at Vg-V_{FB}=1V in accumulation. The work function of Ru gate extracted from C-V analysis was 5.02 eV, suggesting Ru has the appropriate work function for P-MOSFETs. Using the conductance method, a high interface state density of 1.3 x 10^{13} eV^{-1}cm^{-2} from the conduction band edge to the near midgap of Si was obtained in Ru/HfO_2/n-Si MOS, compared to low interface density level of ~ 10^{11} eV^{-1}cm^{-2} in p+ poly Si/SiO_2/n-Si MOS. To evaluate the thermal stability, the samples were subjected to a rapid thermal anneal in an argon ambient up to 900°C. The electrical characteristics of Ru/HfO_2/n-Si MOS capacitor are discussed in detail with post metal annealing temperatures.

As the minimum VLSI feature size continues to scale down below the 100nm regime, the need for alternative high dielectric constant (high-k) material and metal gate electrode becomes increasingly critical. Metal gates will eliminate the poly depletion effect and improve other issues such as increased gate resistance and boron penetration.[1,2]

Due to their appropriate work functions, Ru and RuO_2 films have been studied as promising gate electrodes for PMOSFETs.[3,4] These gates have also been investigated as bottom electrodes for dynamic random access memory (DRAM) capacitors. The search for metallic gates faces many challenges since they must have compatible work functions, process compatibility and thermal/chemical interface stability with the underlying dielectric.[5] Most metal gate electrodes studied to date suffer from high temperature instability resulting in a degraded interface with the underlying dielectric.[6] Although there have been studies on the electrical properties of metal gates (Pt, TaN) on HfO_2,[7,8] the electrical characteristics of Ru gate electrode on HfO_2 dielectric has not been investigated in detail.

In this paper, we report the electrical characteristics of HfO_2 dielectrics with Ru gate electrodes. We also present the dielectric charges such as interface trapped and oxide trapped charges in HfO_2 dielectrics and compare them with those in thermally grown SiO_2. The electrical characteristics and thermal stability of Ru/HfO_2/n-Si MOS capacitors are discussed in detail with post metal annealing (PMA) temperatures.

Experimental

HfO_2 thin films were formed via RF sputtering of a Hafnium target in an argon ambient followed by subsequent oxidation. The substrates used in this work were n-type

Si with field oxide defined active regions. The active surfaces were H-terminated by subjecting them to a 1%HF clean prior to hafnium deposition. The RF power density and deposition pressure were 2.47 W/cm^2 and 5.5 mTorr, respectively. After deposition, the hafnium layers were oxidized by rapid thermal annealing (RTA) at 600°C for 30 seconds or furnace annealing at 600°C for 30min in nitrogen (N_2) or oxygen (O_2) ambients. Ru gate electrodes were then deposited using rf power density of 4.93 W/cm^2. Lift-off lithography was used to define the gate electrodes patterns. To evaluate the post-gate thermal stability, the samples were annealed in argon (Ar) ambient at 700°C, 800°C, and 900°C for 15sec. Forming gas annealing (FGA) was performed in 10% H_2/N_2 at 400^{o}C for 30min prior to electrical and material characterization. Capacitance-voltage (C-V) and current-voltage (I-V) characteristics were obtained using HP4284 and HP4155B, respectively. To investigate interface charge density, conductance method measurement were performed.[9-11] The flatband voltage (V_{FB}) and equivalent oxide thickness (EOT) for the capacitors were obtained using the NCSU CV program.[12]

Results and Discussion

Figure 1 shows the C-V curves of Ru/HfO_2/n-Si MOS capacitors after a FGA at 400°C for 30min. The capacitance was measured at a frequency of 1MHz on an area of 2.5x10^{-5} cm^2. In order to get the lowest EOT while maintaining low leakage current, we optimized the process conditions including oxidation time, oxidation ambient, and initial metal (Hf) thickness (Fig. 2). As shown in inset of figures 2, the oxygen ambient yielded a thicker EOT than the nitrogen ambient. Using an RTA oxidation process at 600°C for

30 sec in nitrogen ambient, an EOT of 12.5Å and a V_{FB} of 1.01V for Ru gate was obtained. The oxidation of hafnium films in N_2 ambient is attributed to high background of O_2 and H_2O on the Hf surface or in the nitrogen gas. The inset of figure 1 shows leakage current density of Ru/HfO_2/n-Si for equivalent oxide thickness of 12.5 Å. The leakage current at Vg-V_{FB}=1V in accumulation for 12.5 Å equivalent oxide thickness is about 1.7 x 10^{-2}A/cm^2, which is several orders of magnitude lower than that of SiO_2 for the same EOT. It is attributed to an increase of the physical thickness of HfO_2 with high dielectric constant, which reduces the tunneling current significantly.

Figure 3 (a) and (b) show XPS spectra of Hf 4f and Si 2p in HfO_2 films. As shown in figure 3 (a), hafnium was identified as mainly HfO_2. This is because the Hf $4f_{7/2}$ peak was at 16.3eV and was close to the reported value for HfO_2.[13] Two different silicon species were present on the surface. The silicon binding energy at approximately ~99eV was consistent with Si^o,[13] while the silicon peak at approximately ~102eV was assigned as an oxide (SiO_x) or a silicate (Fig. 3b). Based on the reported Hf 4f and Si 2p peak positions, hafnium silicate might be present but cannot be unambiguously determined. Hf-Silicide was not detected on the surface, since no Hf 4f peak was observed at binding energy ~14.3 eV which was the reported peak position for $HfSi_x$.[14, 15] From the outermost surface into the substrate, both the Hf 4f and the Si 2p peaks appeared at the similar binding energies of 16.2-16.3eV and 101.6-102eV, as shown in Fig. 3(a) and (b). This indicates that there are no obvious interfacial reactions between Hf and Si occurring at the HfO_2 and Si interface.

Figure 4 shows the V_{FB} of Ru/HfO_2/n-Si MOS capacitor as a function of EOT after FGA at 400ºC. The y-intercept indicates the work function difference (Φ_{ms}= Φ_m-

Φ_s), which is decoupled from the effect of fixed charges. The work function of the Ru gate was determined using the flatband voltage ($V_{FB} = \Phi_{ms} - Q_f\, t_{ox}/\varepsilon_{ox}$). As shown in figure 4, the Φ_{ms} of Ru gate electrode is found to be ~ 0.88± 0.05eV, which translates to work function (Φ_m) value of 5.02eV, an appropriate work function for PMOS gates. It should be noted that the EOT range for HfO_2 is small. The Φ_m value also agrees with the work function of Ru on SiO_2.[16] Table 1. summarizes the V_{FB}, EOT, and D_{it} of p+ poly Si and Ru gate electrode with several dielectrics. The V_{FB} for p+ poly Si and Ru gate on SiO_2 / n-type Si was 1.1 V, suggesting Ru has the appropriate work function for P-MOSFETs on HfO_2. The V_{FB} for Ru gate on SiO_2, ZrO_2, and HfO_2 was 1.10 V, 1.00V, and 1.01V, respectively. The density of negative fixed oxide charges ($N_f = Q_f/q$) is estimated to be ~4 x $10^{12}cm^{-2}$ from the slope in V_{FB} vs. EOT plot. Interface state density (D_{it}) was extracted from the conductance method, which is considered to be one of the most sensitive methods to determine D_{it}. We performed conductance measurements with frequency for a given surface potential to determine an accurate D_{it}. The D_{it} values obtained from the conductance measurement for Ru gates on HfO_2 were near $1.0x10^{13}$ ~ $3.0x10^{13}eV^{-1}cm^{-2}$ from the conduction band edge to the midgap of Si. For SiO_2, the D_{it} values near $0.2x10^{12}$ ~ $1.0x10^{12}$ $eV^{-1}cm^{-2}$ were observed for Ru gates while lower D_{it} values of $0.3x10^{11}$ ~ $1.1x10^{11}$ $eV^{-1}cm^{-2}$ were observed for p+ poly Si gate. The large D_{it} for Ru gate electrode may be related to sputtering damage resulting from deposition of Ru. It was reported that the physical bombardment of energetic ion and metal penetration results in damage the gate dielectrics, generating interface and oxide trapped charges in the gate dielectrics during the physical vapor deposition (PVD).[17,18] This damage can be optimized by the process conditions or reduced using a chemical vapor deposition (CVD) or atomic layer chemical vapor deposition (ALCVD) for gate process.[19,20] Also the Ru/HfO_2 system showed a higher D_{it} (1.3 x 10^{13} $eV^{-1}cm^{-2}$) value than that of the Ru/SiO_2 system(0.2x10^{12} ~ 1.0x10^{12} $eV^{-1}cm^{-2}$). It is known that bonding constraints at a intrinsically heterovalent interface between metal oxide and Si cause constrained Si-dielectric interface, resulting in high density of electrical defects.[21] Therefore further optimization of the dielectric may be required to reduce oxide charges.

Figure 5 shows the variation of EOT and current density of Ru/HfO_2/n-Si MOS capacitors as a function of PMA temperatures. As shown, the EOT increases with PMA temperature and is attributed to lower-k interfacial layer growth. It was reported that interfacial layer growth results from the excessive oxygen diffusion into the dielectric through gate electrode and dielectric during annealing.[8] It is also attributed to the excess oxygen and absorbed water embedded in the dielectric prior to gate electrode deposition. It should be noted that that a larger EOT increase has been observed with RuO_2 gates compared to Ru gate due to the oxygen present in the RuO_2 deposition.[3] It is therefore critical to study in situ gate stack deposition to prevent oxygen and water in the dielectric from ambient exposure. The leakage current density decreased after high temperature annealing due to the growth of the interfacial layer, resulting in EOT increase.

Figure 6 shows hysteresis of Ru/HfO_2/n-Si MOS capacitors as a function of annealing temperatures. When the gate voltage was swept from –1 V to 2.5 V, the hysteresis (ΔV_H) of C-V curves was about 50~60 mV, due to the charge trapping and detrapping at the gate dielectrics. The large ΔV_H indicates high level of oxide trapped charge ($Q_{ot}= -\Delta V_H \cdot C_{ox}$) in the gate dielectrics. However, the ΔV_H could be reduced (< 30mV) with high temperature anneals (~900°C).

Conclusion

We have investigated the electrical characteristics of Ru/HfO_2/n-Si MOS capacitor. An equivalent oxide thickness of 12.5Å was obtained with a low leakage current density of 1.7 x 10^{-2}A/cm^2 at Vg-V_{FB}=1V in accumulation. The work function of Ru gate extracted from C-V analysis was 5.02 eV, suggesting Ru has the appropriate work function for P-MOSFETs. However, a high level of interface charge density of 1.3 x 10^{13} $eV^{-1}cm^{-2}$ was obtained in Ru/HfO_2/n-Si MOS due to intrinsic heterovalent HfO_2-Si interface and sputtering damage on the dielectric. Further optimization in the dielectric and gate electrode deposition process would be necessary for advanced metal gate/high-k technology.

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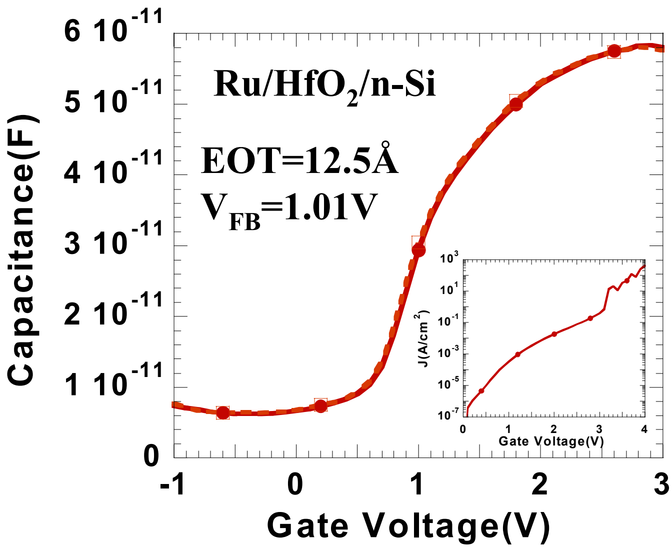

Fig. 1. The C-V curves of HfO_2 dielectrics with Ru gate electrode after forming gas annealing at 400 °C-30min. The capacitance was measured at a frequency of 1MHz on an area of $2.5x10^{-5}cm^2$. The inset figure shows I-V characteristics of HfO_2 dielectrics with Ru gate electrode.

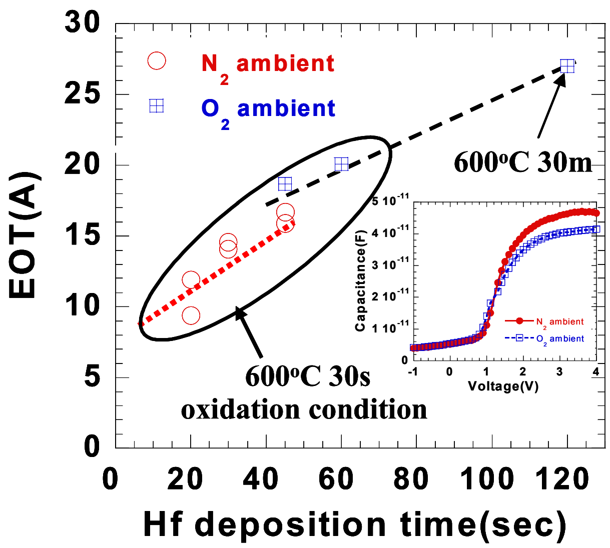

Fig. 2. Equivalent oxide thickness (EOT) as a function of process conditions including oxidation time, oxidation ambient, and initial metal (Hf) thickness

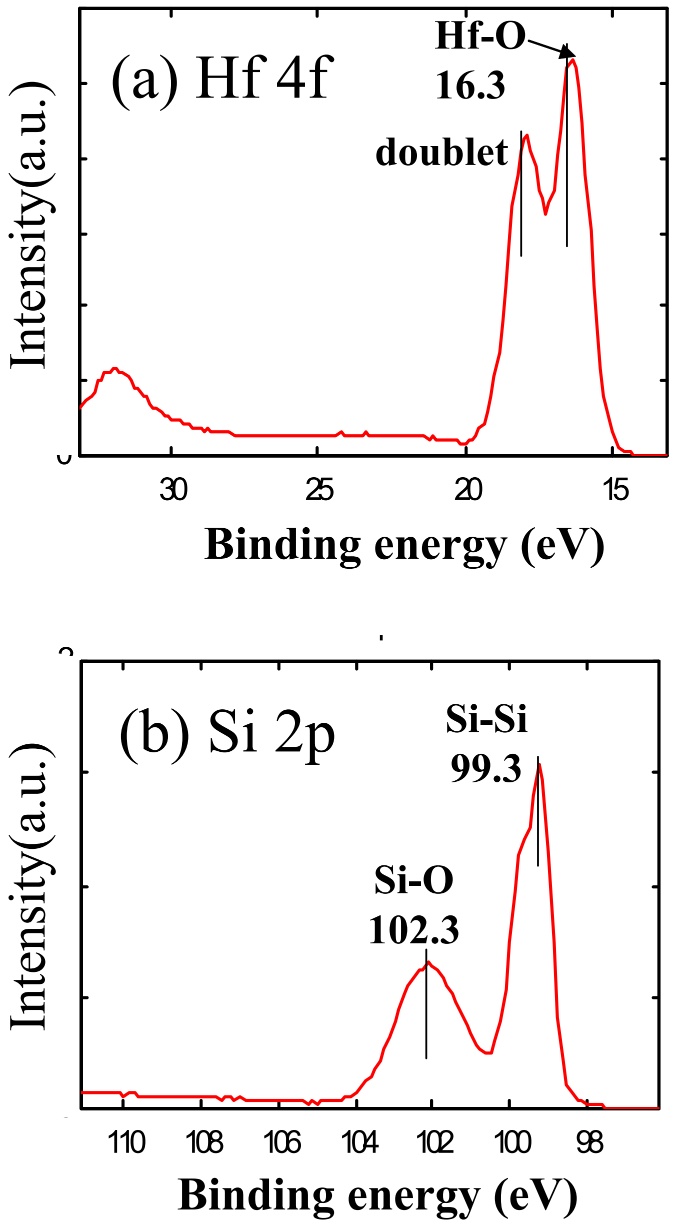

Fig. 3. XPS spectra of HfO_2 films annealed at 600°C in N_2 ambient (a) Hf 4f and (b) Si 2p

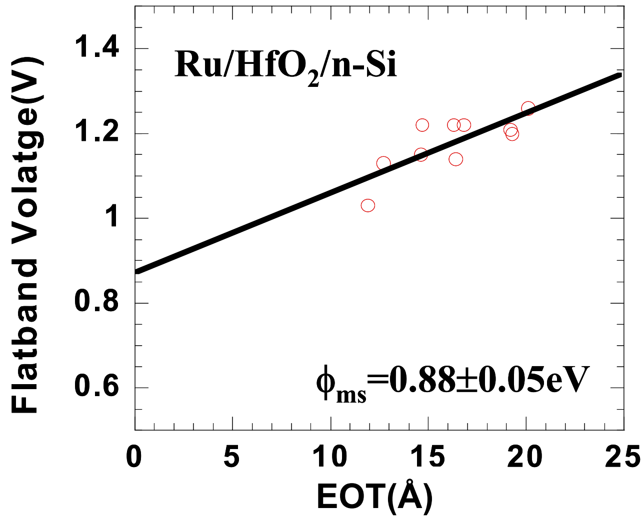

Fig. 4. The flat band voltage (V_{FB}) of Ru gate electrode on HfO_2 as a function of equivalent oxide thickness (EOT) after forming gas annealing at 400 °C for 30min.

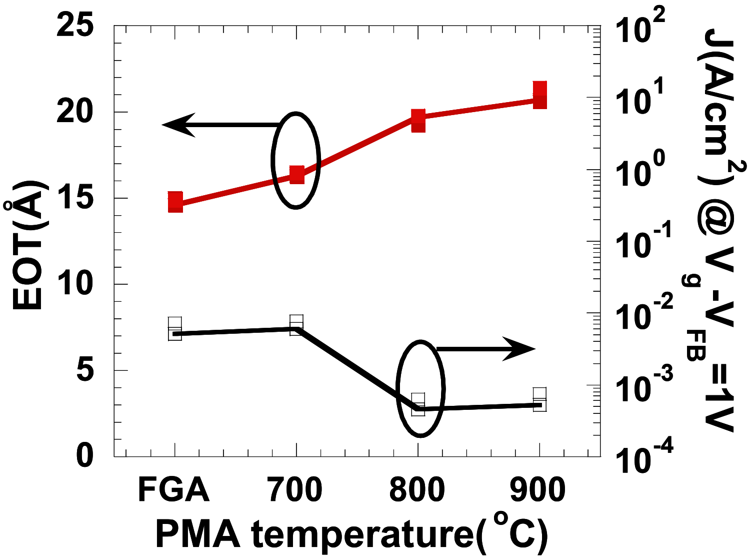

Fig. 5. Effect of post metal annealing (PMA) temperatures on equivalent oxide thickness (EOT) and gate leakage current density (J_g) @ V_g-V_{FB} =1V. Rapid thermal annealing (RTA) was performed in Ar ambient for 15 second.

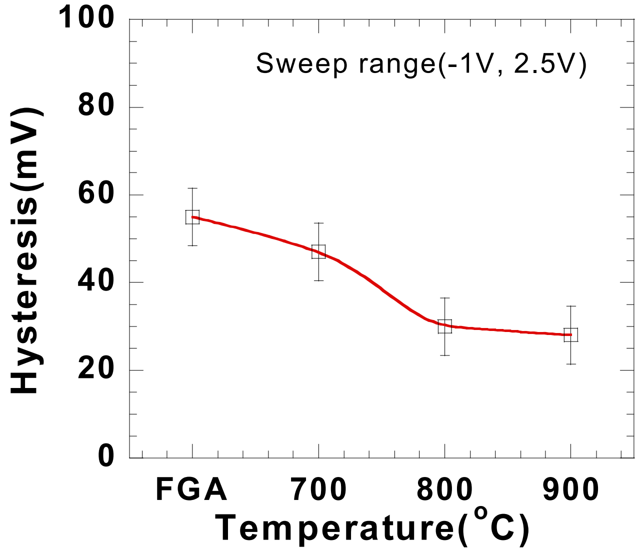

Fig. 6. Hysteresis (ΔV_H) of Ru gate MOSCAP as a function of PMA temperatures.

	p+ poly Si	Ru gate electrode		
	a)SiO_2	a)SiO_2	b)ZrO_2	b)HfO_2
V_{FB}	1.1V	1.1V	1.00V	1.01V
EOT	31.0Å	32.7Å	26.8Å	12.5Å
*D_{it}	~10^{11}	~10^{12}	—	~10^{13}

a)Thermally grown SiO_2, b) ZrO_2 & HfO_2 prepared by PVD, *D_{it} in unit of $eV^{-1}cm^{-2}$,

Table 1. The V_{FB}, EOT, and D_{it} of p+ poly Si and Ru gate electrode with several dielectrics (SiO_2, ZrO_2, and HfO_2).

5.2 Evaluation of Ta-based metal gates on HfO_2 dielectrics for Dual metal gate Si-CMOS Devices

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Abstract

In this letter, we have evaluated the electrical properties of Ta-based metals (Ta, TaN_x, and $TaSi_xN_y$) on HfO_2 dielectrics as advanced alternative gate stacks. Ta-based metals were deposited by reactive sputtering with varying N_2 flows to investigate the effect of N content on the electrical properties. An equivalent oxide thickness of 11.2Å and the flatband voltage of -0.78V were obtained in $TaSi_xN_y/HfO_2$/p-Si MOS capacitor, while maintaining low leakage current density of 4.1×10^{-2}A/cm^2 at V_g-V_{FB}= -1V in accumulation. It was observed that trapped charge increased with increasing nitrogen content and interface charge density levels were higher with all metal gates. To evaluate the thermal stability, the samples were subjected to a rapid thermal anneal in an argon ambient up to 900°C. The electrical characteristics of Ta-based metals/HfO_2/p-Si MOS capacitor are discussed in detail with post metal annealing temperature.

As the minimum VLSI feature size continues to scale down below the 100nm regime, the need for alternative high dielectric constant (high-k) material and metal gate electrode becomes increasingly critical. Metal gate will eliminate the poly depletion effect and improve other issues such as increased gate resistance and boron penetration.[1,2] The search for metallic gates faces many challenges since they must have compatible work functions, process compatibility and thermal/chemical interface stability with the underlying dielectric.[5] Most metal gate electrodes studied to date suffer from high temperature instability resulting in a degraded interface with the underlying dielectric.[6]

In this paper, we compare the electrical characteristics of Ta-based metals (Ta, TaN_x, and $TaSi_xN_y$) gate electrodes on HfO_2 dielectrics. The properties of Ta-based metals are also compared with those of Ru gates. We investigated the dielectric charges such as interface trapped and oxide trapped charges in HfO_2 dielectrics as a function of N content in the films. The electrical characteristics and thermal stability of Ta-based metals/ HfO_2/n-Si MOS capacitors are discussed in detail with post metal annealing (PMA) temperatures.

HfO_2 thin films were prepared by RF magnetron sputtering of thin hafnium layers followed by an oxidation process. The substrates used in this work were p-type Si with field oxide defined active regions. The active surfaces were H-terminated by subjecting them to a 1%HF clean prior to hafnium deposition. The RF power density and deposition pressure were 2.47 W/cm^2 and 5.5 mTorr, respectively. For subsequent oxidation of the hafnium layers, rapid thermal annealing (RTA) at 600°C for 30 seconds in nitrogen (N_2) or oxygen (O_2) ambient was performed. Ta-based metals were deposited by reactive sputtering at rf power density of 4.93 W/cm^2 and varying N_2 flow to investigate the effect of N content in the films on the electrical properties were used. Lift-off lithography was used to define the gate electrodes patterns. To evaluate the thermal stability, the samples were annealed in argon (Ar) ambient at 700°C, and 900°C for 15sec. Forming gas annealing (FGA) was performed in 10% H_2/N_2 at 400^{o}C for 30min prior to electrical and material characterization. Capacitance-voltage (C-V) and current-voltage (I-V) characteristics were obtained using HP4284 and HP4155B, respectively. The capacitance was measured at a frequency of 1MHz on an area of $2.5x10^{-5}cm^2$. To investigate interface charge density, conductance method measurement were performed.[9-11] The flatband voltage (V_{FB}) and equivalent oxide thickness (EOT) for the capacitors were obtained using the NCSU CV program.[12]

Figure 1 shows the leakage current density at Vg-V_{FB} = -1V as a function of EOT after a FGA at 400°C for 30min. Using an RTA oxidation process at 600°C for 30 sec in nitrogen ambient, an EOT of 11.2Å and a V_{FB} voltage of -0.78V for $TaSi_xN_y$ gate was obtained. The oxidation occurred due to background concentration of O_2 in the nitrogen gas and in the vented RTA chamber. The leakage current at Vg-V_{FB}=-1V in accumulation for 11.2 Å equivalent oxide thickness is about 4.1 x $10^{-2}A/cm^2$, which is several orders of magnitude lower than that of SiO_2 for the same EOT. This is attributed to an increase of the physical thickness of HfO_2 accompanied by a high dielectric constant, which reduces the direct tunneling significantly.

Figure 2 shows comparison of the hysteresis (ΔV_H) for several kinds of metal gate electrodes on HfO_2 dielectrics after FGA at 400ºC. The hysteresis due to the charge trapping and detrapping at the gate dielectrics were measured in voltage range of -2.5 V to 1 V. As shown, Ta and Ru gate have smaller hysteresis (50 ~ 60mV) than the N-contained metal gates. This hysteresis shift is attributed to charges, Q_{ot}, generated in the HfO_2 dielectric and potential sputter damage during gate electrode sputtering. For TaN_x and $TaSi_xN_y$ gate, the hysteresis was increased to >200mV with higher N flow rate (f_N). Higher Q_{ot} is attributed to the nitrogen-related traps for high N content films, which result from excessive N during reactive sputtering in N_2 ambient. The large ΔV_H indicates high level of oxide trapped charge (Q_{ot}= $-\Delta V_H \cdot C_{ox}$) in the gate dielectrics, resulting in the threshold voltage instability. This hysteresis was reduced to less than 30mV after high temperature annealing (Fig. 3).

Figure 4 shows the variation of EOT for several metal gates on HfO_2 as a function of PMA temperatures. As shown, EOT increases with PMA temperature and is attributed to lower-k interfacial layer growth. It has been reported that interfacial layer growth results from the excessive oxygen diffusion into the dielectric through gate electrode and dielectric during annealing.[8] It is also attributed to the excess oxygen and absorbed water embedded in the dielectric during dielectric preparation and prior to gate electrode deposition. It should be noted that that a smaller EOT increase (~3 Å) was observed with $TaSi_xN_y$ gates compared to other gates (Ta, TaN_x, and Ru). This is attributed to the excellent oxygen barrier properties of $TaSi_xN_y$ gates, preventing oxygen diffusion into the dielectric through gate electrode and dielectric during annealing, whereas other gates, such TaNx, are vulnerable to oxygen diffusion through gate stacks. However, even with excellent gate diffusion barriers, the exposure of the dielectric o ambient conditions must be avoided to prevent EOT increases after subsequent anneals. This warrants the investigation of in-situ deposition of gate electrodes and high-K dielectrics. The EOT increase was accompanied by a corresponding decrease in the leakage current density and is correlated to the growth of an interfacial layer which increases the EOT.

Table 1 summarizes the V_{FB} and EOT for Ta-based metal gates on HfO_2 as a function of annealing temperatures. The V_{FB} for $TaSi_xN_y$ (f_N =5%) gate on HfO_2 / p-type Si was -0.78 V, suggesting $TaSi_xN_y$ has the appropriate work function for N-MOSFETs. The V_{FB} for Ta, TaN_x (f_N =5%), and $TaSi_xN_y$ (f_N = 5%) gate on HfO_2 was -1.083 V, -0.782V, and -0.780V, respectively. As annealing temperature increased, the V_{FB} of the Ta-based metal gates shifted positively. This increase could be attributed to either a) the variation of effective oxide charges and b) modification of the work function at the gate-dielectric interface. A single thickness of HfO_2 does not allow the decoupling of these two components. Varying thicknesses of HfO_2 are needed to separate out the contribution of these two effects, howver, PVD technique of depositing Hf layer and oxidizing it cannot be used to obtain a range of thicknesses.

Figure 5 shows interface state density (D_{it}) for Ru and $TaSi_xN_y$ gate with annealing temperature. Interface state density (D_{it}) was extracted from the conductance method, which is considered to be one of the most sensitive methods to determine D_{it}. We performed conductance measurements with frequency for a given surface potential to determine an accurate D_{it}. For 400°C, the D_{it} values near ~ $1.0x10^{12}$ $eV^{-1}cm^{-2}$ from the conduction band edge to the midgap of Si were observed for $TaSi_xN_y$ gates while higher D_{it} values of $1.0x10^{13}$ ~ $3.0x10^{13}eV^{-1}cm^{-2}$ were observed for Ru gate. The lower D_{it} for $TaSi_xN_y$ gate is attributed to the low deposition rate during the reactive sputtering, resulting in less bombardment damage into the dielectrics. The large D_{it} for Ru gate electrode may be related to sputtering damage resulting from higher deposition rate of

Ru. It was reported that the physical bombardment of energetic ion and metal penetration results in damage the gate dielectrics, generating interface and oxide trapped charges in the gate dielectrics during the physical vapor deposition (PVD).[14,15] Also, it is known that bonding constraints at a intrinsically heterovalent interface between metal oxide and Si cause constrained Si-dielectric interface, resulting in high density of electrical defects.[18] The high D_{it} values shown above were successfully reduced upon high temperature annealing.

In summary, we investigated the electrical characteristics of HfO_2 dielectrics with Ta-based metals (Ta, TaN_x, and $TaSi_xN_y$) gate electrodes. An equivalent oxide thickness of 11.2Å was obtained in $TaSi_xN_y$ /HfO_2/p-Si MOS capacitor, while maintaining low leakage current density of 4.1 x 10^{-2}A/cm^2 at Vg-V_{FB}=-1V in accumulation. A small increase (~3 Å) in EOT increase was observed with $TaSi_xN_y$ gates compared to a much larger EOT increase with other gates (Ta, TaN_x, and Ru). This is attributed to the excellent oxygen barrier properties of $TaSi_xN_y$ gates, preventing oxygen diffusion into the dielectric through gate electrode and dielectric during annealing. The V_{FB} for $TaSi_xN_y$ (f_N= 5%) gate on HfO_2 / p-type Si was -0.78 V, suggesting $TaSi_xN_y$ has the appropriate work function for N-MOSFETs. However, as annealing temperature increases, the V_{FB} of the Ta-based metal gates shifted positively either due to charge generation in the dielectric and/or work function change at the electrode-dielectric interface. It was observed that trapped charge was increased with nitrogen sputtering ambient and interface charge density was increased due to bombardment damage during gate metal sputtering. Further optimization to reduce oxide charges in the dielectric would be necessary for advanced metal gate/high-k technology.

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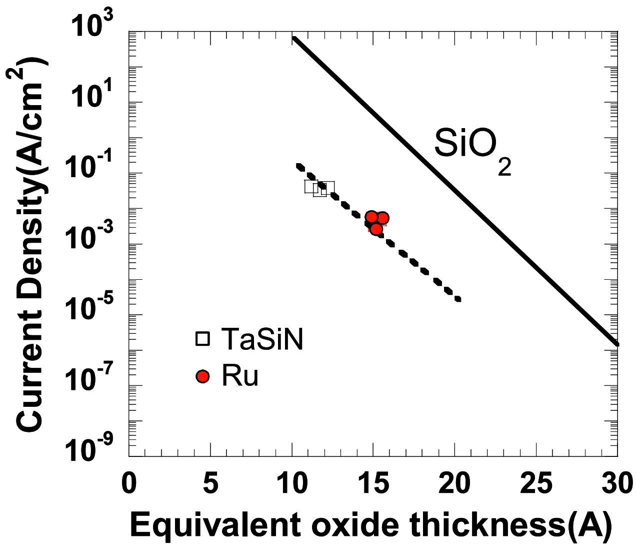

Fig. 1. The leakage current density at $V_g\text{-}V_{FB}$ = -1V as a function of EOT after a FGA at 400°C for 30min

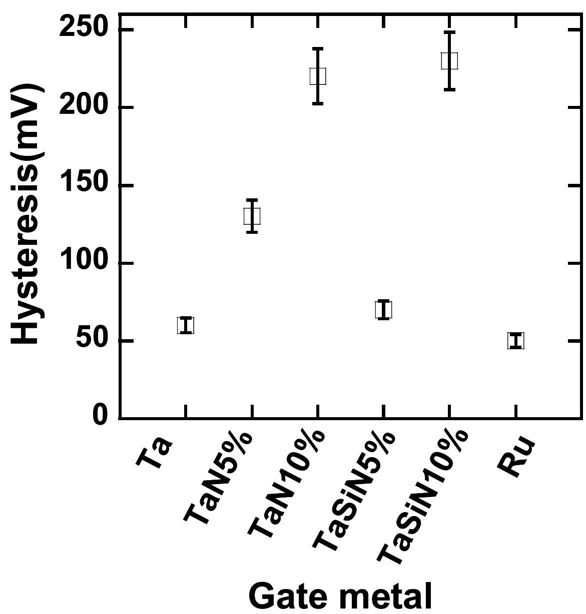

Fig. 2. Comparison of the hysteresis (ΔV_H) for several kinds of metal gate electrodes on HfO_2 dielectrics after FGA at 400ºC

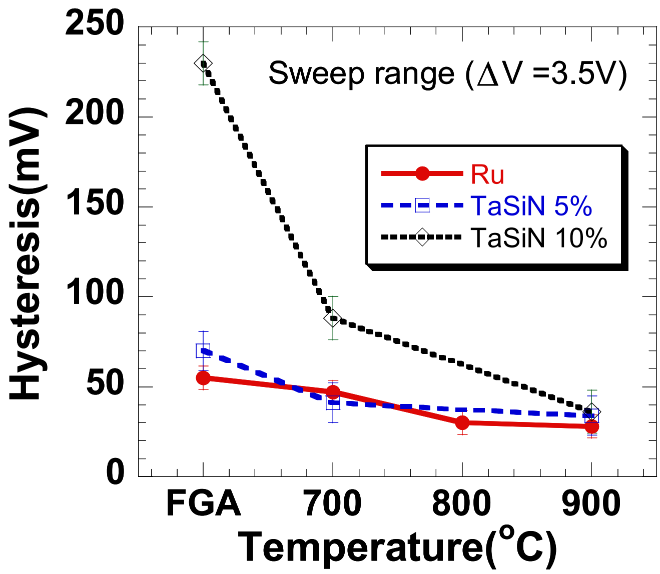

Fig. 3. Hysteresis (ΔV_H) of several kinds of metal gate electrodes MOSCAP as a function of post metal annealing (PMA) temperatures. Rapid thermal annealing (RTA) was performed in Ar ambient for 15 second.

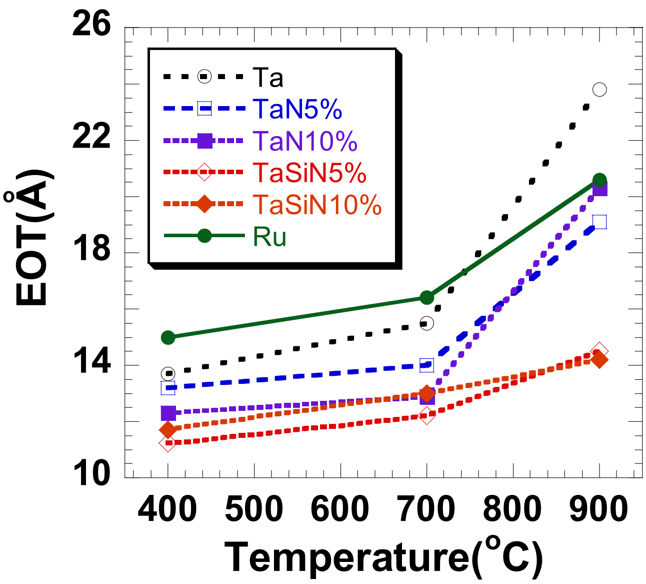

Fig. 4. Effect of PMA temperatures on equivalent oxide thickness (EOT) for several kinds of metal gates.

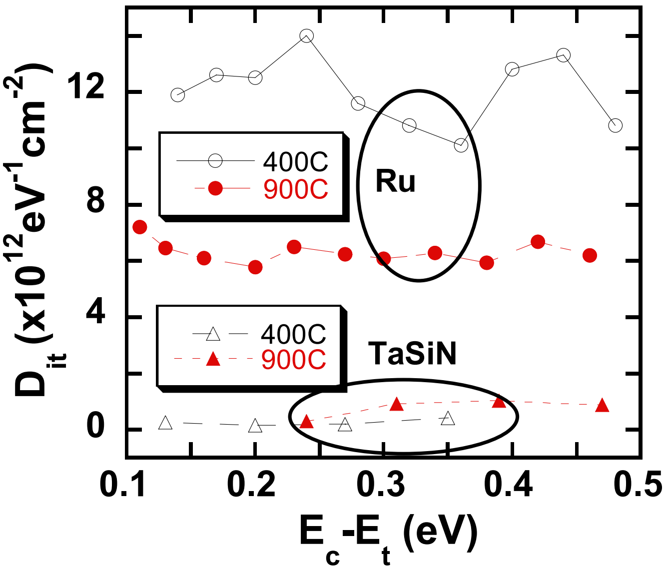

Fig. 5. The interface state density (D_{it}) for Ru and $TaSi_xN_y$ gate with annealing temperature.

	400C		700C		900C	
	V_{FB}(V)	EOT(nm)	V_{FB}(V)	EOT(nm)	V_{FB}(V)	EOT(nm)
Ta	-1.083	1.37	-0.690	1.55	-0.626	2.38
TaN 5%	-0.782	1.32	-0.618	1.40	-0.423	1.91
TaN 10%	-0.773	1.23	-0.449	1.31	-0.497	2.03
TaSiN 5%	-0.780	1.12	-0.600	1.22	-0.420	1.45
TaSiN 10%	-0.736	1.17	-0.564	1.33	-0.450	1.42

Table 1. The V_{FB} and EOT of Ta-based metal gate electrode on HfO_2 dielectrics as a function of PMA temperature.

5.3 Summary

We investigated the electrical characteristics of HfO_2 dielectrics with Ta-based metals (Ta, TaN_x, and $TaSi_xN_y$) and Ru gate electrodes. An equivalent oxide thickness of 11.2Å was obtained in $TaSi_xN_y$ /HfO_2/p-Si MOS capacitor, while maintaining low leakage current density of 4.1 x 10^{-2}A/cm^2 at Vg-V_{FB}=-1V in accumulation. A less increase (~3 Å) in EOT increase was observed with $TaSi_xN_y$ gates compared to other gates (Ta, TaN_x, and Ru) due to the excellent oxygen barrier properties of $TaSi_xN_y$ gates, preventing oxygen diffusion into the dielectric through gate electrode and dielectric during annealing. The work function of Ru gate extracted from C-V analysis was 5.02 eV, suggesting Ru has the appropriate work function for P-MOSFETs. The V_{FB} for $TaSi_xN_y$ (f_N= 5%) gate on HfO_2 / p-type Si was -0.78 V, suggesting $TaSi_xN_y$ has the appropriate work function for N-MOSFETs. It was observed that trapped charge was increased with nitrogen sputtering ambient and interface charge density was increased due to bombardment damage during gate metal sputtering. Further optimization to reduce oxide charges in the dielectric would be necessary for advanced metal gate/high-k technology.

CHAPTER 6

Characteristics of $TaSi_xN_y$/ $HfSiO_xN_y/HfO_2$ MOSFETs

I. Introduction

In this chapter, electrical characteristics of $TaSi_xN_y$ metal gate electrodes on Hf based based dielectrics for NMOSFET structures will be discussed. NMOSFETs were fabricated using a conventional process flow. Measurements on MOSFETs with $TaSi_xN_y$ metal gate electrodes did not indicate any evidence of gate depletion effects. The output MOSFET characteristics such as I_{DS}-V_{GS}, I_{DS}-V_{DS} and mobility, will be discussed.

II. Experimental

The substrates used for MOSFET fabrication consisted of p-type (100) Si wafers, with doping concentration of $3x10^{17}cm^{-3}$. A field oxide (3500 Å) was grown and patterned to form the active areas. The device fabrication was carried out in collaboration with Jack Lee's group at UT-Austin. The dielectric deposition and some processing steps were done at UT-Austin where as the gate electrode and other process steps were performed at NCSU. The high-K dielectric stack consisted of HfO_2 on the Si substrate followed by top surface nitridation on top of the HfO_2 to make $HfSiO_xN_y$. Next, $Ta_{45}Si_{14}N_{41}$ gate electrode was patterned using lift-off lithography. Phosphorus was then implanted to form the source/drain (S/D). Low-temperature oxide (LTO 1500 Å) was deposited and etched to form the contact openings. The S/D implant was activated using an RTP at 950°C for 30 s in N_2. Aluminum/Titanium stacks were deposited and patterned to form the contacts; Al was also deposited on the wafer backside, and the wafers were then sintered in forming gas (N_2/ H_2=95%/5%) at 400°C for 30 min.

Capacitance-voltage (C-V) and current-voltage characteristics were obtained using HP4284 LCR meter and HP4155, respectively. The flat-band voltage (V_{FB}) and the equivalent oxide thickness (EOT) for the capacitors were obtained by using the NCSU CV program that includes the quantum mechanical deduction. Mobility was extracted using NCSU 2D mobility program, which also gave information regarding the individual contributions to mobility from charged interface scattering and surface roughness. A nonlinear least squares technique for experimental and theoretical fits is used to determine the optimum mobility parameters [1].

III. Results and Discussion

Figure 1 shows the C-V characteristics of N-MOSFET with $TaSi_xN_y$ gate electrode (W/L=150 m/10 m). The equivalent oxide thickness (EOT) of device is 16.6Å. Negligible gate depletion was observed for transistors with $TaSi_xN_y$ gate electrodes. This suggests that the use of metal gates can effectively eliminate gate depletion due to their high carrier concentration. The poly Si gate depletion width is given by $W_{poly} = \varepsilon_{ox}E_{ox}/qN_{poly}$ (where $E_{ox} = V_{ox}/t_{ox}$). It depends on the poly Si gate active dopant concentration (N_{poly}) and the oxide thickness (t_{ox}). The carrier concentrations, via Hall measurement, was found to be $> 10^{22}cm^{-3}$ for $TaSi_xN_y$ films, which is significantly higher than the heaviest doped poly-Si films (~ $10^{20}cm^{-3}$). For the heavily doped poly-Si films, there are practical limits to the electrically active dopant concentration due to solubility limits and defects. The flatband voltage(V_{FB}) extracted from C-V curve is –

0.54V and is ~105mV more positive than the expected value if the work function of 4.4eV is used and no oxide charges are assumed. However, there are two possibilities that could change the flatband voltage a) a different work function value of $TaSi_xN_y$ on high-K dielectrics, and b) presence of charge in the high-K dielectric. It should be noted that for $TaSi_xN_y$ /HfO_2 capacitors, a V_{FB} shift of ~380mV (-0.78V → -0.42) was observed with annealing temperature (400°C → 900°C) as shown in the previous chapter. It is possible that the charge evolution in the Si-N bonds containing $HfSiO_xN_y$/HfO_2 stacked films is quite different from HfO_2 dielectrics.

Figure 2 (a) and (b) show the transistor characteristics of $HfSiO_xN_y$/HfO_2 stacked dielectrics with $TaSi_xN_y$ gate electrode devices (W/L=150 m/10 m). As shown in fig. 2 (a), well-behaved Ids-Vds characteristics were obtained. Figure 2 (b) shows Id-Vgs characteristics. The subthreshold swing of ~100mV/dec was observed after forming gas annealing (FGA) at 400^{o}C. It was reported that high temperature FGA reduces the interface charges in TaN/ ZrO_xN_y, which improved the subthreshold swing [2]. The threshold voltage V_{TH} extracted from the Ids-Vgs plot at Vds=50mV is ~ 0.86V, which is much higher than the extracted V_{TH} =0.67V using NCSU CVC program [1]. It is attributed to the low mobility and high gate leakage current which reduces the drain current and complicates extracting V_{TH} from the Id-Vgs plot. Further characterization to understand the role of trapped charges, interface charges and gate leakage currents is necessary.

Carrier mobility of the above devices was extracted by the NCSU 2D mobility program [2]. Figure 3 compares the extracted electron mobility of $TaSi_xN_y$ on high-K dielectrics with the universal curve. The electron mobility values of $TaSi_xN_y$/

$HfSiO_xN_y/HfO_2$ stacks were lower than the ideal mobility values for SiO_2 [1]. The peak electron mobility of NMOSFET is approximately 133cm^2/Vs at 0.8 MV/cm. This is about a factor of two lower than the values commonly obtained from poly-Si based MOSFETs on SiO_2. The low electron mobility of NMOSFET with $TaSi_xN_y$ on $HfSiO_xN_y/HfO_2$ can be attributed to additional scattering due to fixed charges, trapping charges, and interface charges. The origin of the interface charges and surface roughness may be attributed to the sputtering process for the gate and the dielectric which may impact damage to the Si-HfO_2 interface. Other mechanisms that are believed to contribute to reduction in mobility are related to remote phonon but these are still based only on theoretical predictions. The interface scattering of 1.48×10^{11} /cm^2 and surface roughness of 30.5 Å^2 were obtained from NCSU 2D mobility program. Further optimization of gate stack processing and optimized high temperature anneals will be required to improve carrier mobility.

IV. Conclusion

Electrical characteristics of $TaSi_xN_y$ metal gate electrode on $HfSiO_xN_y/HfO_2$ gate dielectrics for N-MOSFET structure was investigated. Capacitance-voltage results indicated that no evidence of gate-depletion with the introduction of $TaSi_xN_y$ metal gates. Reasonable output MOSFET characteristics such as Ids-Vgs and Ids-Vds were obtained. However, degraded mobility characteristics were observed and were attributed to additional scattering mechanisms by trapped charges trapping charges, and interface charges in HfSiON/HfO_2 dielectrics. A reduction in these charges is necessary to understand the intrinsic limitation of carrier mobility at Si-High-K dielectric interfaces.

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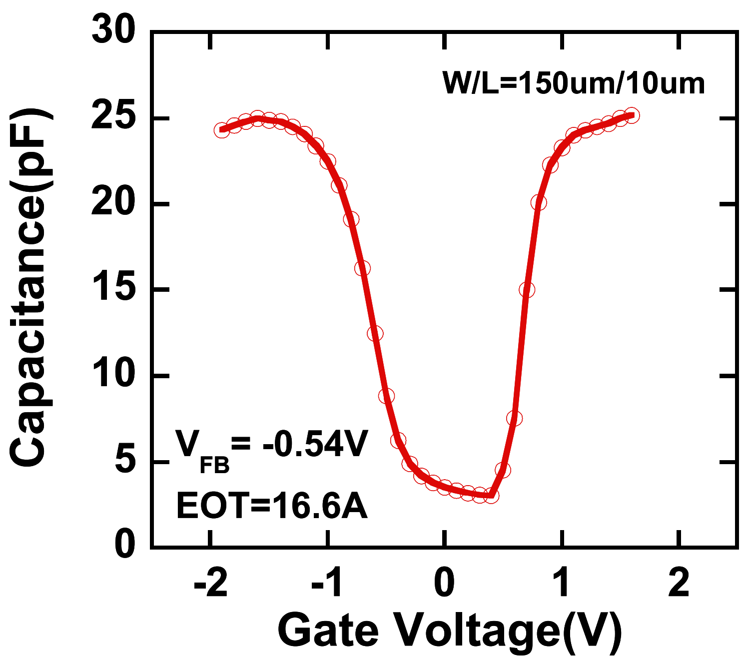

Figure 1 shows the C-V characteristics of N-MOSFET with $TaSi_xN_y$ gate electrode. No gate depletion was observed for the transistor with $TaSi_xN_y$ gate electrode.

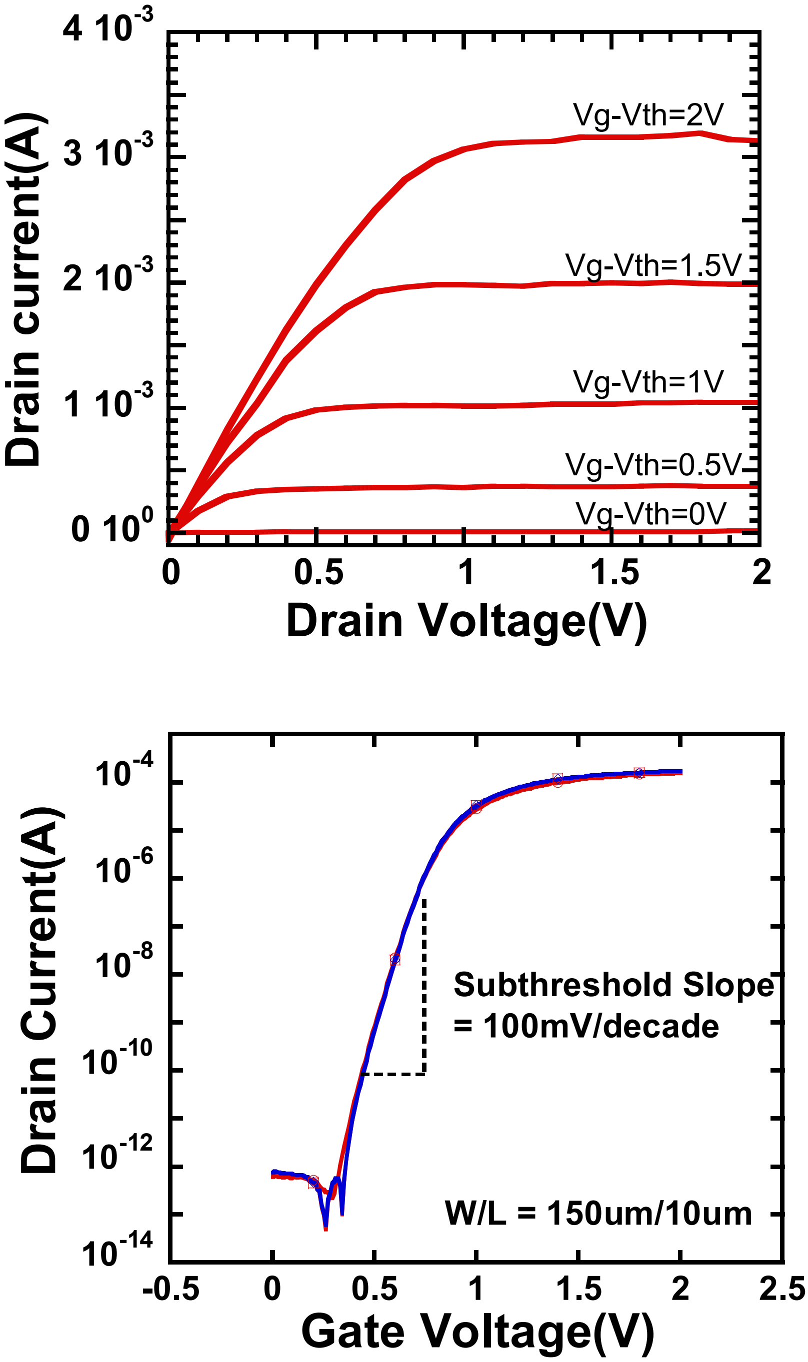

Figure 2 (a), Ids-Vds characteristics for NMOSFET (W/L=150 um/10 um) with $TaSi_xN_y$ on $HfSiO_xN_y/HfO_2$ (b) Ids-Vgs curves and transconductance at Vds=50mV.

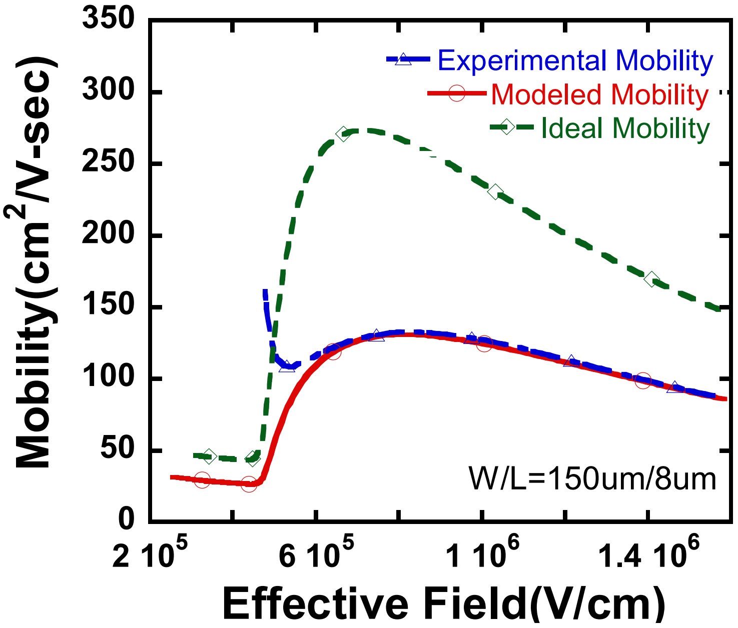

Figure 3 Comparison the experimentally measured electron mobility of $TaSi_xN_y$ / $HfSiO_xN_y$ / HfO_2 NMOSFET with the ideal mobility curve.

CHAPTER 7

Conclusion and Future research

This dissertation has focused on fabrication and characterization of alternative gate stacks consisting of high-K dielectrics and metal gates. This work has presented the evaluation of Ta based metals including Ta, TaN_x, and $TaSi_xN_y$ as gate electrodes for their potential use in NMOS devices.

7.1 Characteristics of $TaSi_xN_y$/ SiO_2/ Si structures

The research indicated that the workfunction of $TaSi_xN_y$ is compatible with NMOS devices, provided the right composition is achieved. We found the workfunction of $TaSi_xN_y$ (Si>Ta) with varying N contents ranges from 4.2 ~ 4.3 eV. However, the workfunction of $TaSi_xN_y$ (Ta>>Si) were higher and close to those observed with TaN_x. The role of Si and N was investigated in $TaSi_xN_y$ gate electrodes with annealing. It was found that the presence of excess Si resulted in an increase of Φ_m under high temperature anneals and was attributed to $TaSi_2$ formation at the gate-dielectric interface. This effect was prevented by reducing the Si content and adding N to the film. The N content was optimized since too little did not prevent the $TaSi_2$ formation and too much resulted in N diffusion. Also, the lack of Si (i.e. TaN_x) resulted in undesirably high Φ_m values. It is believed that the presence of Si-N bonds in the film improves the thermal stability of the gate-dielectric interface while maintaining appropriate work functions.

The improved stability of $TaSi_xN_y$ gates is attributed to the presence of Si and N in the gate electrode, which can improve the film microstructure and the diffusion barrier properties at the gate-dielectric interface. Furthermore, this increased stability does not come at the cost of the carrier concentration. Although the work function value is slightly higher than the desired 4.2eV, it still provides a reasonable compromise since to date not other gate with a lower work function and an equivalent thermal stability has been reported. This stability of $TaSi_xN_y$ films may enable high-k dielectrics and metallic electrode to be implemented in advanced CMOS devices.

7.2 Characteristics of metal gate electrode on HfO_2 dielectrics

The electrical characteristics of HfO_2 dielectrics with Ta-based metals (Ta, TaN_x, and $TaSi_xN_y$) and Ru gate electrodes are also summarized here. An equivalent oxide thickness of 11.2Å was obtained in $TaSi_xN_y$ /HfO_2/p-Si MOS capacitor, while maintaining low leakage current density of 4.1 x 10^{-2}A/cm^2 at V_g-V_{FB}=-1V in accumulation. A ~3 Å EOT increase was observed with $TaSi_xN_y$ gates compared to other gates (Ta, TaN_x, and Ru) due to the excellent oxygen barrier properties of $TaSi_xN_y$ gates, preventing oxygen diffusion into the dielectric through gate electrode and dielectric during annealing. The work function of Ru gate extracted from C-V analysis was 5.02 eV, suggesting Ru has the appropriate work function for P-MOSFETs. The V_{FB} for $TaSi_xN_y$ (f_N= 5%) gate on HfO_2 / p-type Si was -0.78 V, suggesting $TaSi_xN_y$ has the appropriate work function for N-MOSFETs. It was observed that trapped charge was increased with nitrogen sputtering ambient and interface charge density was increased due to bombardment damage during gate metal sputtering. Further optimization to reduce oxide charges in the dielectric would be necessary for advanced metal gate/high-k technology.

7.3 Characteristics of $TaSi_xN_y$/ $HfSiON/HfO_2$ MOSFETs

Electrical characteristics of $TaSi_xN_y$ metal gate electrode on $HfSiON/HfO_2$ gate dielectrics for N-MOSFET structure were also investigated. Capacitance-voltage results indicated that no evidence of gate-depletion with the introduction of $TaSi_xN_y$ metal gates. Reasonable output MOSFET characteristics such as Ids-Vgs, Ids-Vds, and Subthreshold swing, were obtained. However, degraded mobility characteristics were observed and were attributed to additional scattering mechanisms by trapped charges in $HfSiON/HfO_2$ dielectrics. A reduction in these charges is necessary to understand the intrinsic limitation of carrier mobility at Si-High-K dielectric interfaces.

7.4 Future Works

There are several areas of research that need further investigation. First, optimization of the transistor fabrication process is needed to minimize the damage at gate electrode/ dielectric and dielectric/Si interface. This damage can be optimized by the process conditions or reduced using a chemical vapor deposition (CVD) or atomic layer chemical vapor deposition (ALCVD) for gate process. Comparisons between ALCVD and PVD processes are necessary. Additional study on the H_2 or D_2 forming gas annealing at high temperature will be required to improve interface states. Though it is still controversial, it will be able to improve the channel carrier mobility. Second, the thermal stability of high K gate dielectrics needs to be improved. Further optimization of surface and interfacial nitridation is needed and other techniques, such as alloying with Al_2O_3 have to be studied. Third, in order to investigate the positive shift of V_{FB} with temperature, which is attributed to either the variation of effective oxide charges or the modification of Φ_m at the gate-dielectric interface, varying thicknesses of HfO_2 are needed to separate out the contribution of these two effects.