ABSTRACT

KOHLER, WILLIAM LEAVELL. Failure Analysis of AlGaN/GaN HEMTs in a Commercial Production Environment. (Under the direction of Dr. Spyridon Pavlidis).

AlGaN/GaN HEMTs are inherently well suited for RF and high-power applications. These devices are now commercially available and are produced by companies all over the globe. During production, tests are run on the devices to determine device health and wafer yield. This makes it possible to identify and isolate failed devices. These failed devices are candidates for failure analysis which is performed to determine and remedy the root cause of failure, in turn improving production. However, by utilizing the DC electrical measurements performed during initial screening, one can get a hypothesis into how any AlGaN/GaN HEMT failed before failure analysis is performed. The objective of this thesis, therefore, is to establish a basic framework of electrical measurements and analysis to isolate the source of failure in AlGaN/GaN HEMTs on silicon produced in a commercial foundry.

This study demonstrates how four different DC tests give a different insight into device performance and can be used as symptoms for determining the root cause of failure for a failed device. These tests are the gate-source diode test, the gate and drain three-terminal current leakage tests, imbalance current tests, and pinch off voltage test. Each of these four tests offers a different insight into the failure mode for both on-wafer and packaged AlGaN/GaN HEMTs. It is shown that careful inspection of the imbalance current can help attribute sources of failure to either the gate or source/drain regions, thereby accelerating the process of subsequently inspecting devices microscopically. These tests offer symptoms for how a device fails and is reinforced by microscopic, spectroscopic, and physical failure analysis techniques.

Failure Analysis of AlGaN/GaN HEMTs in a Commercial Production Environment

by
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DEDICATION

To my family and friends who supported me along the way.

BIOGRAPHY

William Kohler was born in Albuquerque, New Mexico on July 23, 1996. He earned his Bachelor of Science degree from Florida State University in May of 2018. In August of 2018 he enrolled into the masters program in the Department of Electrical and Computer Engineering at North Carolina State University.

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CHAPTER 1

Overview of AlGaN/GaN HEMTs

1.1 Introduction

Semiconductor technology has been evolving since the first patent on controlling current utilizing semiconductor properties by Julius Lileinfeld [1]. Today, there are a multitude of materials used to fabricate transistors as well as many transistor types. This paper will focus on one particular type of transistor fabricated with a particular material, that is AlGaN/GaN on Si HEMTs. A HEMT is a high electron mobility transistor whose advantageous properties are based on the formation of a heterostructure, in this case between aluminum gallium nitride (AlGaN) and gallium nitride (GaN). GaN and AlGaN are wide bandgap materials that are particularly promising for high voltage applications. GaN is a material that has been the focus of extensive study and is used as a material for device fabrication by many companies. This chapter will explain what wide bandgap materials are and why they are necessary. Furthermore, it will compare the material properties of AlGaN/GaN with other common semiconductor materials. The process flow of how AlGaN/GaN is grown on silicon as well as how devices are fabricated will be explained. Lastly the expected operation of a good device will be outlined and compared to a failed device. Performing failure analysis on failed devices is necessary in order to determine why the device failed and remedy that cause of failure to increase wafer yield and device performance. The primary objective of this thesis is to use DC electrical characterization methods for failure analysis (FA) of AlGaN/GaN HEMTs to identify manufacturing and processing issues.

1.2 Wide Bandgap Semiconductors

Wide bandgap semiconductors are a category of semiconducting material that have a large bandgap compared to other semiconducting materials. The bandgap, or energy gap, is the amount of energy needed to excite an electron from the valence band to the conduction band of a given material. This energy gap is an important material property because materials with a higher bandgap will be able to operate at higher voltage and power levels. The wide bandgap material that is the focus of this paper is Gallium Nitride or GaN. GaN is the material of choice for high power and radio frequency applications because of its wide bandgap energy, high electron mobility, high breakdown field, and performance at high frequencies of operation. A comparison of the material properties of GaN and other semiconducting materials is shown in Table 1.1.

Table 1.1: Material properties of GaN compared to other semiconducting materials used in industry.

Material	Band Gap (eV) **[2]**	Mobility (cm^2/Vs) **[3]**	Critical Breakdown Field (MV/cm) **[4]**	Saturation Electron Velocity (x10^7 cm/s) **[4]**
Si	1.1	1360	0.3	1
AlGaAs/GaAs [1]	1.4	8000	0.4	1.3
SiC	2.9	1140	3	2
AlGaN/GaN [1]	3.4	1590	3.3	2.5

As seen from Table 1.1, GaN has a higher bandgap than the other semiconductors meaning that it can be used for higher power applications than Si or GaAs. AlGaN/GaN also has a high critical breakdown field as well as a high saturation velocity when compared to other wide bandgap semiconductors. Furthermore, GaN has a higher mobility than that of SiC meaning that for high power applications where high mobility is needed, GaN is the best material to be used. Huang et al. was able to demonstrate a mobility of 1676 $cm^2/V^{-1}s^{-1}$ based on room temperature hall

[1] Mobility in the channel layer when a channel is formed within a heterostructure.

measurements of GaN on SiC [5]. The reason GaN has a high mobility is due to the formation of a 2-dimensional electron gas, or 2DEG, at the interface between the GaN and AlGaN layers. The 2DEG is right below the AlGaN layer and is shown in Figure 1.1. The 2DEG consists of electrons that are free to conduct; these free electrons allow GaN to have such a high lateral mobility. The formation of the 2DEG is due to the piezoelectric polarization of charge that is the product of the lattice mismatch between the AlGaN and GaN layers [6].

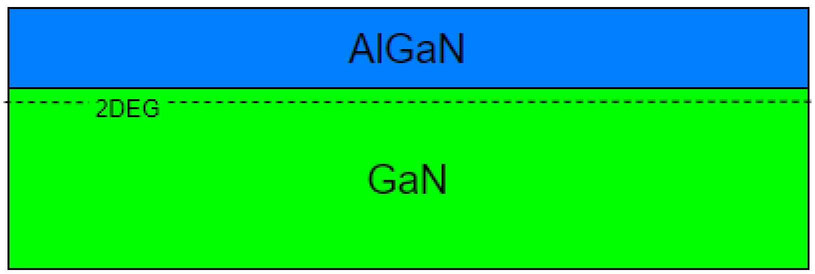


Figure 1.1: Schematic showing the location of the 2DEG at the AlGaN/GaN interface.

GaN is also a very desirable material for fabrication of radio frequency (RF) devices due to its ability to make heterostructures with AlGaN. When compared to a similar material like SiC, GaN shows a high power density of 12 W/mm while SiC shows a power density of 5.2W/mm at 3.5GHz [7]. The combination of power and frequency response of GaN HEMTs make them good for power amplifier applications.

Typical AlGaN/GaN HEMTs fabricated in industrial environments are not on a native substrate. This means that the AlGaN/GaN layers are grown on a substrate that is not GaN. SiC and Si are the most common grown substrates in industry. There are advantages and disadvantages to using either material as the growth substrate; however, in terms of cost and substrate size Si outperforms SiC. Si substrates are low cost, have larger size compared to SiC substrates, and can potentially be integrated with Si technology [8].

1.3 Growth of AlGaN/GaN on Si and Device Fabrication

In industry, AlGaN and GaN are grown on various substrates by metalorganic chemical vapor deposition (MOCVD) [9]. MOCVD utilizes a metal organic as one of the precursors for epitaxial growth. The process starts with a bare Si (111) substrate. The structure of the epitaxial stack is shown in Figure 1.2.

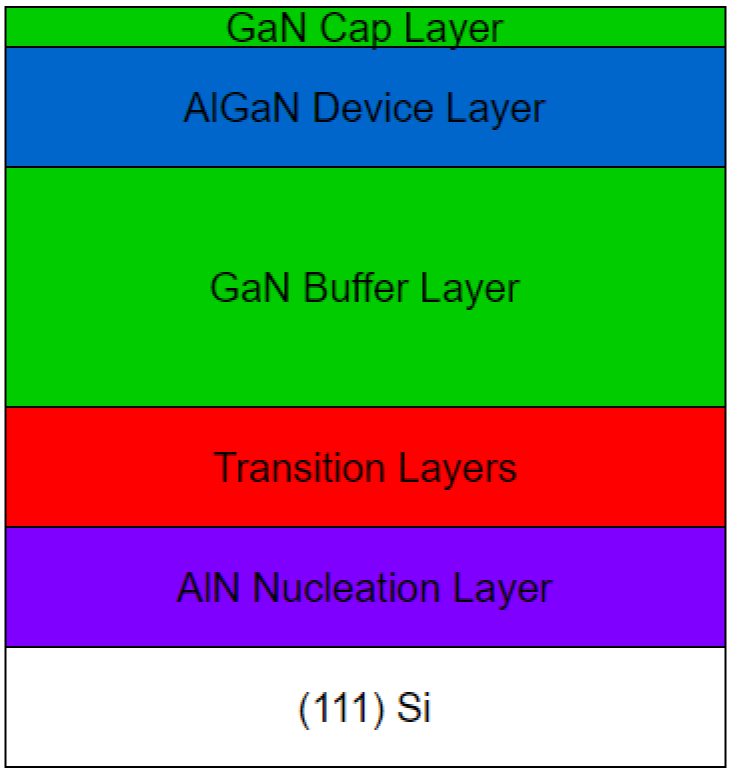


Figure 1.2: Schematic showing the layers of the epitaxial stack in order. The size of each layer is not to scale.

The substrate is loaded into the MOCVD chamber and an aluminum nitride nucleation layer is grown. GaN has difficulty nucleating directly on a Si substrate due to a large lattice mismatch, so AlN is used as a nucleation layer to promote future growth [9]. After the nucleation layer is grown, a series of transition layers are grown. These transition layers are used for stress balance and compensation that arise due to a difference in lattice constant [10]. Si has a lattice constant in the (111) plane of 5.3354Å while GaN has a lattice constant of 3.214Å.[11] This is done to reduce defects in the epitaxial films that could obstruct or damage the device channel. If the GaN layer were to be grown directly on the Si substrate, the lattice mismatch would be too great and the GaN layer would have too many defects to be useable. After the transition layers have been grown, a thick GaN buffer layer is grown. The GaN buffer layer not only promotes the formation of the 2DEG at the AlGaN/GaN interface, but the thickness of the GaN buffer layer impacts the maximum breakdown voltage [3]. On top of the GaN buffer layer is the AlGaN device layer, also called the AlGaN barrier layer. The AlGaN device layer consists of a low percentage of Al, around 22-26% [12]. This AlGaN layer is necessary for the formation of the 2DEG which makes us the device channel. Finally, the epitaxial stack is completed by the growth of a thin GaN cap layer.

Once the epitaxial stack has been grown, the devices can be fabricated. The devices fabricated are multi-finger lateral devices. The devices are lateral to take advantage of the high mobility of the 2DEG that is formed at the AlGaN/GaN interface. The fabrication process begins with the deposition of Ti-Al-Ni-Au ohmic contacts and a rapid thermal anneal [12]. Next the devices are passivated using a layer of SiN_x and device isolation is accomplished by a multiple energy N^+ implantation which significantly disorders the lattice in the AlGaN/GaN heterostructure. This implantation damages and destroys the 2DEG outside of the device region to assure the current is flowing only within the active region of the device [12]. Next, Schottky gate contacts were formed by selectively etching the SiN_x passivation down to the semiconductor surface with a dry fluorine based etch chemistry with a subsequent deposition of the gate metal stack. The gate metal generally consists of a Ni-Au stack, but the exact metal stack is usually proprietary information [12]. The multiple fingers were interconnected through the use of air bridges. A schematic of the fabrication process is found in Figure 1.3.

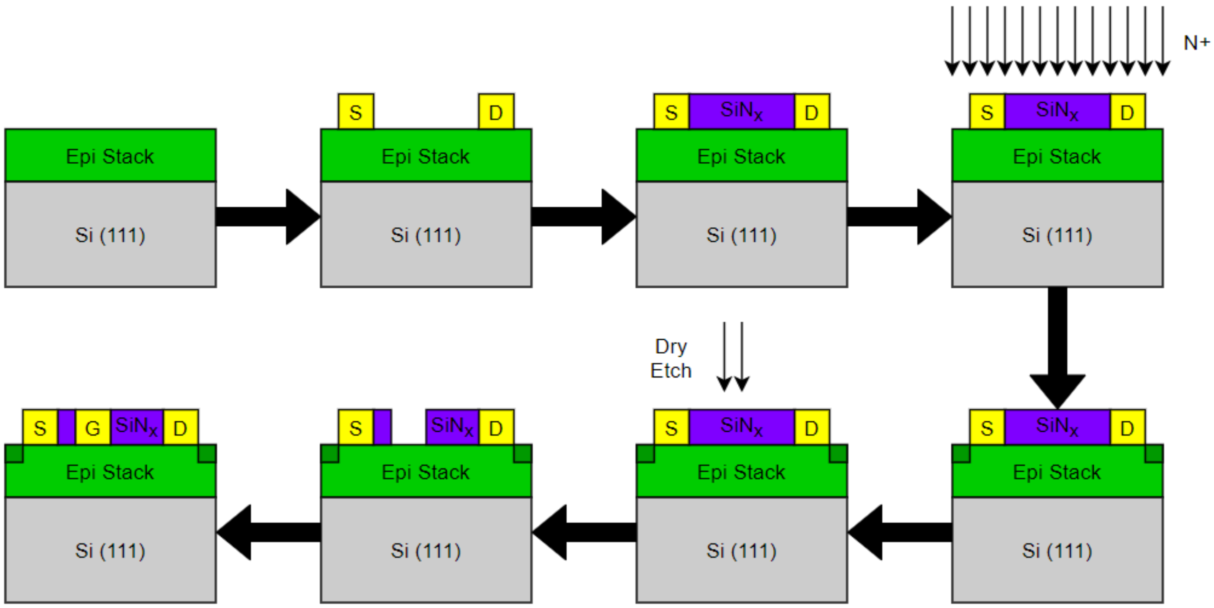


Figure 1.3: Schematic outlining the fabrication process of an AlGaN/GaN HEMT.

After the completion of front side processing, the back side of the wafer is processed. The Si substrate is ground down and vias are etched through the substrate and epitaxial stack to the source busses on the front of the wafer [13]. Then Au is deposited on the back side of the wafer to finalize backside processing. The process for backside processing is shown in Figure 1.4. All devices are then tested electrically, and devices with satisfactory performance can be diced and packaged to be sent to customers.

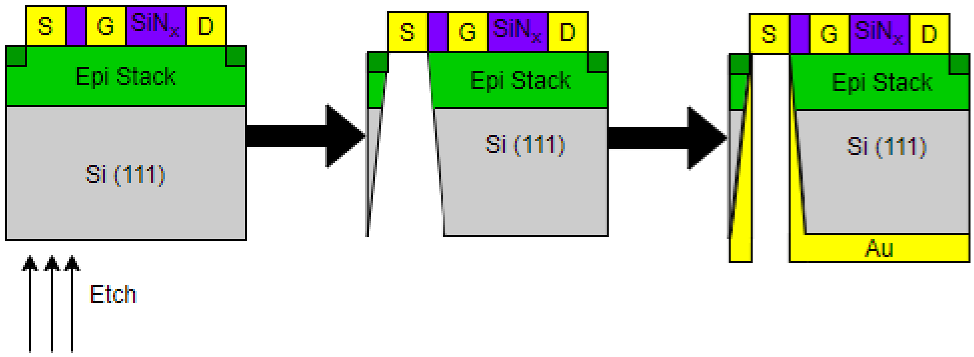


Figure 1.4: Backside processing of an AlGaN/GaN HEMT.

1.4 Device Operation

The formation of the 2DEG at the AlGaN/GaN heterojunction constitutes an electron channel that must be depleted to turn the device off; therefore, to date, most AlGaN/GAN HEMTs are usually considered "depletion mode" devices. A depletion mode device is a device that is normally on at 0V gate bias and needs a negative bias to deplete the channel and turn the device off. All devices outlined in this thesis are depletion mode (normally on) devices. In order to test these devices in an off state, a negative bias must be applied to the gate to deplete the electrons in the channel. In this so-called "off state" there will still be a small amount of current leakage between the source, gate, and drain pads.

For a good device, the gate-source diode leakage at negative gate voltages is on the order of nanoamps to microamps. A failed device, however, can have a gate-source diode leakage at negative gate voltages on the order of hundreds of microamps to milliamps for soft fails and hard fails respectively. The three terminal drain and gate leakages for a good device is expected to be on the order of microamps and the magnitude of each should be about the same. This magnitude is important for determining the so called "leakage imbalance" of a device. Failed devices can show large leakage imbalance, meaning that the magnitude of the three terminal gate and drain leakage currents will not be the same and will often be orders of magnitude different. A failed device can also have the gate three terminal leakage, drain three terminal leakage, or both three terminal leakage currents on the order of milliamps. Lastly, for a good device the pinch off voltage will be slightly negative. As mentioned before, a negative bias is needed to deplete the channel and turn the device off. A bad device, however, can have a pinch off voltage that is much more negative than the desired pinch off voltage meaning that the gate is not controlling the channel properly. A table depicting the expected values of a good and bad device is shown in Table 1.2.

Table 1.2: Table depicting the expected characteristics of a good device and a bad device by parameter.

Parameter	Good Device	Bad Device
Gate-Source Diode Leakage Current	Can be on the order of nA to low μA	Can be hundreds of μA to mA
Three Terminal Drain Leakage Current	On the order of μA	On the order of mA
Three Terminal Gate Leakage Current	On the order of μA	On the order of mA
Magnitude of Three Terminal Leakage Currents	Balanced with the magnitude of the gate current being slightly higher than the magnitude of the drain current	Imbalanced, the magnitude of one three terminal leakage current dwarfs the other
Pinch Off Voltage	Slightly negative	Extremely negative

1.5 Conclusion

In conclusion, wide bandgap semiconducting materials are an important technology for high power applications due to their large bandgap. GaN is a wide bandgap material with beneficial properties such as a high electron mobility from the 2DEG, large bandgap, and high breakdown field. GaN on Si is especially useful for industry because Si is a low cost, large area substrate. Knowing the difference between a good device and a bad device from DC measurements is important in assessing the quality of devices that have been fabricated. These DC measurements are the first step in failure analysis of AlGaN/GaN HEMTs and can be used as symptoms to determine the overall failure mode of any failed device.

CHAPTER 2:

In Line Testing of AlGaN/GaN HEMTs

2.1 Introduction

During the fabrication of AlGaN/GaN HEMTs it is necessary to perform certain tests to make sure that the fabrication is being done correctly and that all devices are as high quality as possible. The two main test suites are the wafer characterization tests and the finished device tests. The wafer characterization testing is a suite of DC and RF tests done on the test structures in the process control monitoring (PCM) coupon and give feedback on the electrical properties of the wafer as a whole; finished device testing is a suite of DC tests that is performed on all devices once fabrication is completed and is used to determine wafer yield by screening failed and weak devices. This chapter will explain the different current leakage paths as well as the different tests and what insights they might give to device health and performance. Also, the general pass/fail criteria will be outlined along with what is considered a good device at each test.

2.2 Current Leakage Paths

In a transistor there are a number of leakage paths between the three terminals. However, these leakage paths are hard to quantify through testing so an “ideal device” model is used to visualize the leakage paths. When an ideal device is biased in the off state, the current I_{ds} is equal to zero and all leakage flows from the drain to the gate and from the source to the gate, with the contribution from the source to gate being much smaller than that of the drain to gate due to the difference in voltage between the contacts. With this model the “balance” of the device can be defined. A balanced device is indicative of a healthy device and an imbalance device is indicative of a failed or weak device. The term balanced means that the three terminal gate and drain leakage have similar magnitude and therefore, balance each other. An imbalanced device means that one three-terminal leakage current has a magnitude much higher than the other. A schematic of a balanced and an imbalance device is shown in Figure 2.1.

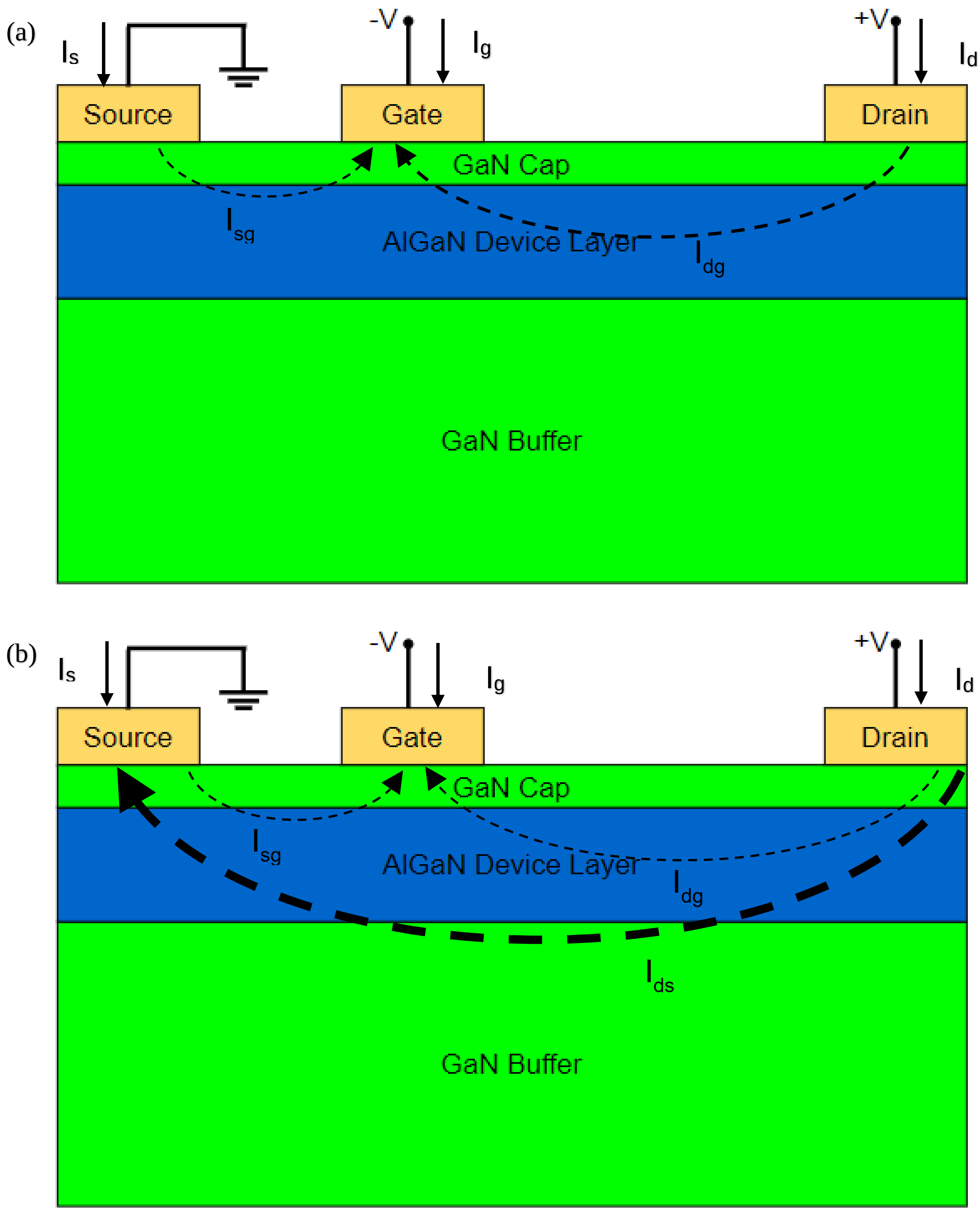


Figure 2.1: Schematic of the leakage paths of (a) an ideal AlGaN/GaN HEMT, and (b) of an imbalanced AlGaN/GaN HEMT. The thickness of the arrows denotes the magnitude of the leakage with thin arrows having a very small amount of leakage.

The three terminal leakage currents as well as the imbalance current of an ideal device is outlined in the equations below:

$$I_g = -I_{sg} + -I_{dg} \tag{1}$$

$$I_d = I_{ds} + I_{dg} \tag{2}$$

$$I_{imbalance} = I_g + I_d \tag{3}$$

Since, in a balanced device, all of the drain leakage current flows from drain to gate, the magnitude of the drain leakage and gate leakage currents should be very similar. However, the magnitude of the gate leakage will be slightly higher due to the leakage from the source contact to the gate. An imbalanced device is one where the magnitude of either the gate or drain leakage currents is much higher than the other. The imbalance parameter can be determined by summing the three-terminal gate and drain currents measured during DC testing. Leakage imbalance is an important parameter to determine for device quality and failure analysis because it is a symptom of a weak or failed device and gives insight into the possible failure mode for any failed devices.

2.3 Wafer Characterization Tests

Wafer characterization tests are a set of DC and RF measurements that are performed on the test structures in the PCM coupon. This testing gives information about the electrical and RF properties of the entire wafer and is an important step in determining quality and yield because it eliminates wafers whose electrical and RF properties are considered out of specifications. A list of all measurements done during wafer characterization testing is shown in Table 2.1.

Table 2.1: Wafer Characterization tests and corresponding measurements.

Test	Explanation
Active Device Parameter Test	Measures multiple resistance, voltage, current, and transconductance parameters
Breakdown Voltage Test	Measures breakdown voltage at multiple bias conditions
Leakage Tests	Measures current leakage at multiple bias conditions
MIM Capacitor Tests	Zero DC bias capacitance MIM Leakage current at 48V MIM leakage current at 100V
DC Parameters	Pinch off voltage Drain and gate three-terminal leakage at 10V Current imbalance at 10V Drain and gate three-terminal leakage at 30V Current imbalance at 30V Drain and gate three-terminal leakage at 65V Current imbalance at 65V On resistance
Small-Signal S-Parameters Test	S-parameter test at varying bias points
Large Signal Gain Test	Measures multiple gain parameters

The wafer characterization test is performed on many test structures across the wafer. Each test listed above gives insight into the quality of the wafer. The DC tests are extremely important for failure analysis because a failure of one or more of the DC tests suggests different failure modes for a given wafer. A wafer must pass every measurement listed in the table above on 5 different PCM coupons to pass the wafer characterization testing phase. Any wafer that does not pass these tests is considered bad and is scrapped. Scrapped wafers do not complete fabrication and are a loss because no devices on a scrapped wafer can be distributed to customers. A wafer that passes all testing is considered good and completes fabrication. Devices that complete fabrication are then sent to device characterization testing.

2.4 Device Characterization Tests

Device characterization tests are a suite of DC measurements done on every device on a wafer after fabrication has been completed. These tests are used to determine wafer yield and identify weak and failed devices so these devices cannot be sent to packaging. The measurements performed during device characterization testing are shown in Table 2.2.

Table 2.2: Device characterization tests, bias conditions, and an explanation of what each test measures or calculates.

Test	Bias Conditions	Explanation
Gate-Source Diode	Measured at one voltage bias: V_g=-8V	Provides information on the health of the gate Schottky contact as well as barrier height
Three-Terminal Gate and Drain Leakage	Measured at four different voltage bias: V_g=-3V, V_d=10V V_g=-8V, V_d=50V V_g=-8V, V_d=100V V_g=-8V, V_d=130V	Gives information on the magnitude of leakage from each metal contact as well as how this leakage evolves at higher voltages
Imbalance Current	Calculated at four different voltage bias: V_g=-3V, V_d=10V V_g=-8V, V_d=50V V_g=-8V, V_d=100V V_g=-8V, V_d=130V	Gives information on the leakage balance between the metal contacts
On Resistance	Measured at two different current bias: I=5mA/mm I=10mA/mm	Measures the on resistance of the device
Pinch Off Voltage	Determined via interpolation from a voltage sweep from a negative voltage to 0V.	Measures the voltage needed to deplete the channel and turn the device off and gives information on how well the gate controls the channel
Three-Terminal Gate and Drain Leakage	Measured at one voltage bias: V_g=-8V, V_d=50V	A second three-terminal test used to determine the magnitude of the leakage current from each metal contact after high voltage tests have been performed
Imbalance Current	Calculated at one voltage bias: V_g=-8V, V_d=50V	A second imbalance current calculation used to determine the balance of the leakage current between each metal contact after high voltage tests have been performed

For a device to pass device characterization testing it must pass every test in the test suite. The pass or fail criteria for each test is device dependent meaning the limits depend on the gate length and channel width of the device. Device characterization testing is extremely important because it determines wafer yield and differentiates good and bad devices. Furthermore, the DC tests performed during this testing give insights into how the device operates and the health of the device. These measurement results can be analyzed and used during failure analysis in order to speculate the cause of failure for any given device. Therefore, these electrical device measurements will be used in this thesis for failure analysis of AlGaN/GaN HEMTs on silicon.

2.5 Insights Given by DC Measurements

As mentioned before, DC measurements are very helpful in determining the health of devices, and each measurement sheds insight into any potential problems a device might have. The measurements that will be explained will come from the device characterization test because both device and wafer characterization testing share similar DC measurements. The first measurement done in device characterization testing is a gate-source diode. This test shows the health of the gate Schottky contact. If the plot of the gate-source diode is not rectifying, then that suggests a short between the gate and source or a damaged gate metal. A graph of a good gate-source diode and a non-rectifying gate-source diode is shown in Figure 2.2. Furthermore, the magnitude of the reverse gate leakage current shows the health of the gate metal's Schottky contact. It should be noted that a compliance level of 21.6 mA was used in these measurements, which causes artifical clipping of the I-V behavior.

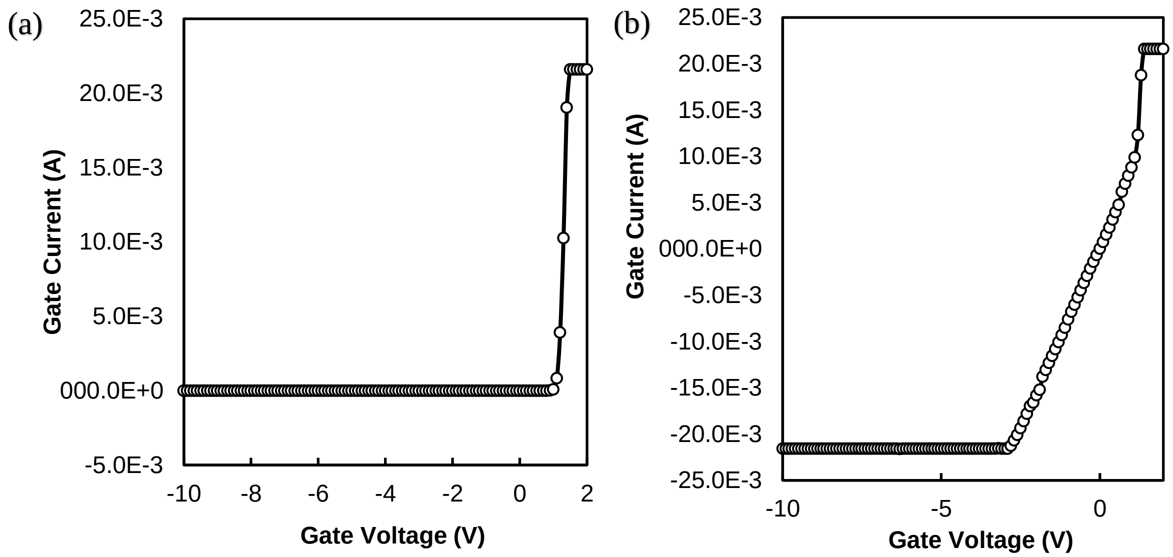


Figure 2.2: (a) Gate-source diode sweep of (a) a good device, and (b) a bad non-rectifying device. The reverse gate leakage current at -10V is on the order of nanoamps in (a), which is expected from a good device. The reverse gate leakage current at -10V is on the order of mA on (b), which is orders of magnitude higher than that of a good device. Also, the bad device does not show rectifying behavior that is expected from a diode shown by a linear curve between -3V and 1V.

The next measurement is the gate and drain three-terminal leakage measurement. This test measures the leakage current of the gate and the drain at any given drain voltage. A good device will have a small amount of gate and drain leakage while a bad device will have a much higher magnitude of gate and drain leakage. The imbalance current calculation is associated with the gate and drain three-terminal leakage measurement because imbalance current is the sum of the two leakage currents. A good device will have balanced leakage meaning the magnitude of the gate and drain three-terminal leakage measurements are almost the same, but the gate will have a slightly higher magnitude because of a contribution from the source. A bad device, however, will not be balanced and either the magnitude of the gate or drain leakage current will be orders of magnitude higher than the other. If the drain leakage is orders of magnitude higher than the gate leakage, it suggests an issue with the channel and gate control. If the gate leakage is orders of magnitude higher than the drain leakage, then that suggests an issue with the gate metal or Schottky contact. This test is done from low to high voltage to determine how the three-terminal leakage currents and the imbalance current evolve with varying drain bias. Plots of a good device's three-terminal leakage and imbalance current as well as a bad device's three-terminal leakage and imbalance current ranging from 0V to 10V is shown in Figure 2.3.

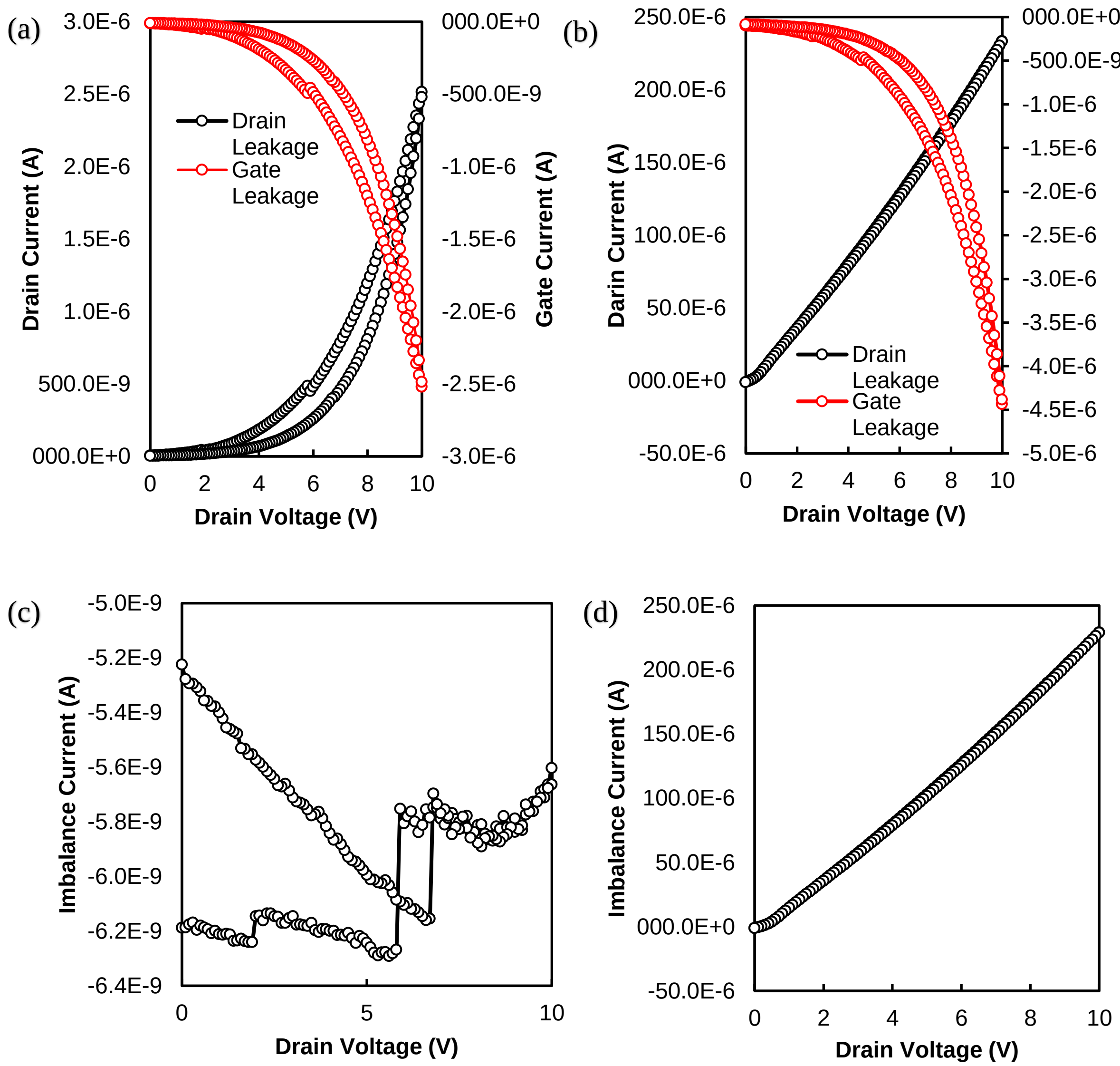


Figure 2.3: Off-state three-terminal leakage current sweep of (a) a good device, and (b) a bad device. The gate and drain leakage current of a good device has a low magnitude at all voltages and are similar in magnitude at 10V with a value around 2.5µA which is expected of a good device. For a bad device, the drain current increases linearly at low voltages instead of staying at a relatively low magnitude, and at 10V the drain leakage dwarfs the gate leakage by roughly 2 orders of magnitude which indicates that this is a bad device. Imbalance parameter of (c) a good device, and (d) a bad device. Since a good device has balanced three-terminal gate and drain leakage currents, the imbalance current is very small and slightly negative, around -6nA at 10V. Since the drain leakage dwarfs the gate leakage in a bad device, the imbalance current is very large and positive, about 250µA at 10V, suggesting that current is flowing from drain to source when the channel device should be pinched off.

Due to limited instrument capabilities, measurements to calculate the on resistance were not performed on any devices for assisting in failure analysis. Therefore, the next and last DC measurement performed is a pinch off voltage test. The pinch off voltage test is done to determine what voltage needs to be applied to the gate to deplete the channel and turn off the device. The target for pinch off voltage varies depending on device parameters such as gate length and channel width. A good device will have a pinch off voltage at or very near the target, while a bad device will have a pinch off voltage that is much more negative. The existence of the 2DEG makes these devices depletion mode so a negative bias is needed to turn them off. A graph of a good device and a graph of a bad device is shown in Figure 2.4.

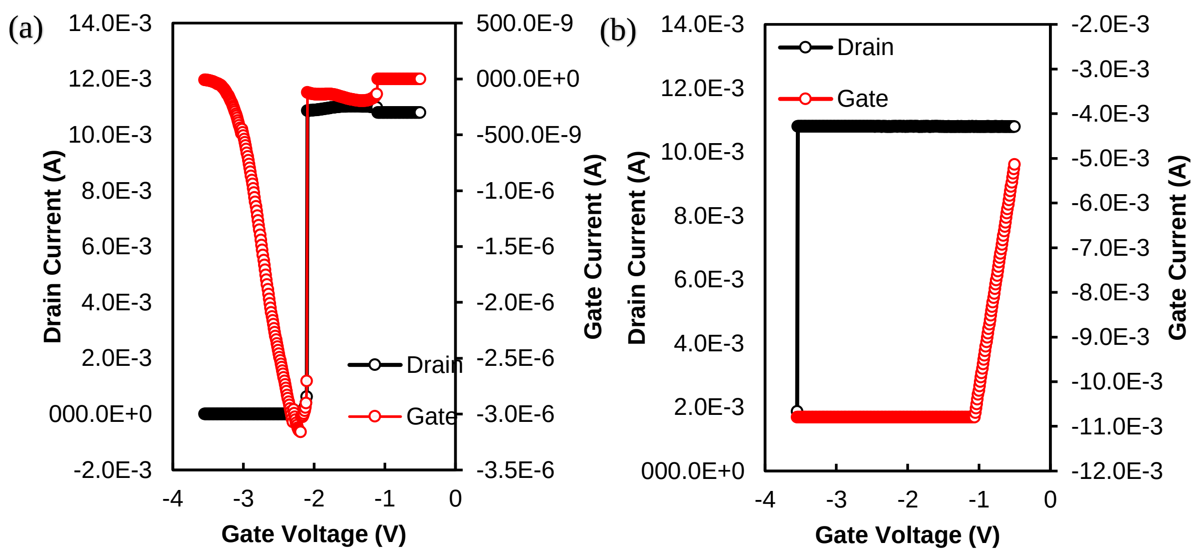


Figure 2.4: (a) Pinch off voltage sweep for (a) a good device, and (b) a bad device. The pinch off voltage is around -2.15V for a good device which is expected. Prior to -2.15V the drain and gate current are both in the nanoamp to low microamp range, and after -2.15V the drain current moves to milliamps suggesting that is the point where the device turns on. The bad device in (b) does not pinch off the channel and the drain current is in the milliamp range from -3.5V to -0.5V suggesting that the gate cannot control the channel and turn the device off.

2.6 Conclusion

In conclusion DC measurement tests are not only important during and after fabrication for differentiating between good and bad devices, but also for use in failure analysis as a symptom for what could be wrong in a device. A very important parameter from DC testing is imbalance current.

Imbalance current is the sum of the three-terminal gate and drain leakage currents and gives an idea of device health. A healthy device will be balanced but slightly negative and a bad device will be very imbalanced. The wafer characterization tests utilize RF and DC measurements to determine the electrical properties of a wafer and make sure the wafer properties are within specifications. Once a wafer finishes fabrication, then the device characterization tests are performed. These tests determine wafer yield by identifying weak and failed devices. The wafers and devices that fail characterization tests can then be inspected using failure analysis techniques, as will be demonstrated in the proceeding chapters.

CHAPTER 3:

Failure Analysis of On-Wafer Devices

3.1 Introduction

Within a commercial production environment, one of the major yield concerns surround the impact of fabrication processes on device performance. Especially when gate length dimensions become very small; as is the case in RF applications, care must be taken to reduce failures. Throughout the fabrication process, devices are tested to confirm whether they align with the target specifications. It is important to determine and remedy the cause of failure for any devices that fail these tests to keep device quality high and improve yield. Maintaining high yield and device quality improves customer relations and saves cost since material does not need to be scrapped. This chapter will present four examples of devices that have failed on wafer testing as well as the symptoms for the failure, how the failure symptom impacts device performance, and what these symptoms can possibly mean in terms of failure mechanism. Furthermore, this chapter will explain the spectroscopic and microscopic methods behind the identification of the root cause of failure.

3.2 Current Imbalance Failures

One of the main test parameters that was developed to give insight into failure mode is imbalance current. As previously mentioned, imbalance current is the sum of the off-state three-terminal gate and drain leakage currents. This test parameter is a good indicator of any issues with the gate contact or of any potential vertical leakage paths to ground. Three separate failure modes, all of which exhibited an anomalously high leakage imbalance, have been identified during the course of this work and will be discussed in the following sections.

3.2.1 Ni Gate Metal Degradation

One device that failed imbalance current is device A. Device A is a GaN on Si RF device with a 10.8mm channel periphery and 0.4μm gate length. For every wafer that has completed the full fabrication sequence, imbalance currents are calculated from a subset of the final DC probe measurements (sometimes referred to as "known good die" [KGD] testing) and imbalance current levels are scrutinized for out of family values. For any device, there are as many as 4 imbalance currents that are considered: imbalance current at low voltage when the gate is kept at -3V and the drain voltage is swept to 10V, and imbalance current at high voltage when the gate is kept at -8V and the drain is swept to 50V, 100V, and 130V. This device failed the imbalance current parameters at 10V and 50V, as shown in Figure 3.1. The very high slope of the imbalance current plot and the three-terminal drain leakage plot at low voltages are an indication that the drain current of the device is increasing at an unacceptably high rate compared to the gate current - a typical signature of many imbalance current failures. This kind of parametric failure indicates that there is a problem with the gate metal stack somewhere along the channel of the device.

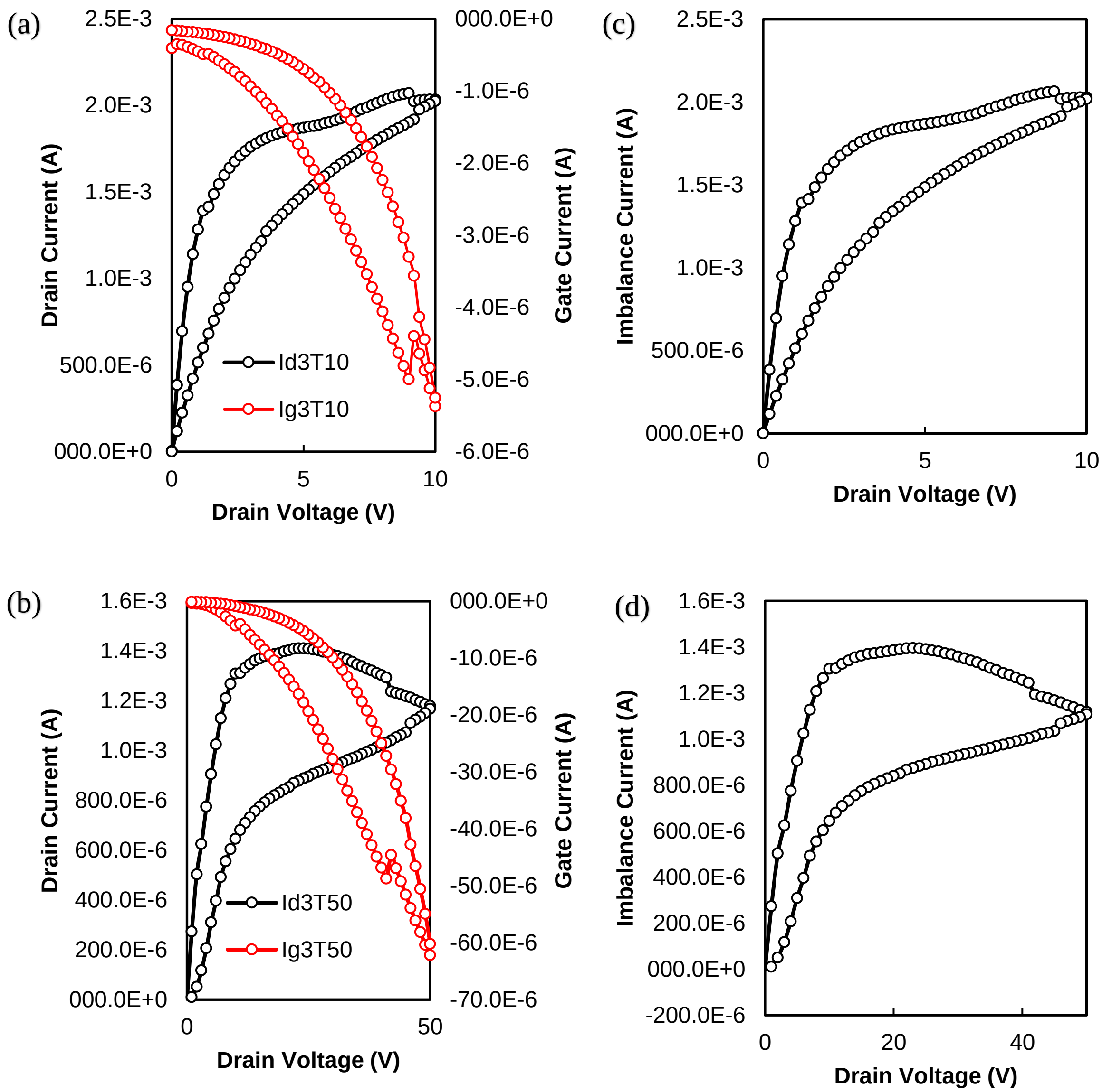


Figure 3.1: Three terminal gate and drain leakage tests for device A sweeping (a) from 0 to 10V and back again, (b) from 0 to 50V and back again. Imbalance current parameter for device A sweeping (c) from 0 to 10V and back again, (d) from 0 to 50V and back again. For the three three-terminal leakage tests, the drain leakage increases very rapidly at low voltages and is the indication that there is a problem with the device.

The failure signature of device A illustrates some interesting points. First, the failure was not catastrophic – the device did not suffer intense electrical over-stress (EOS) and "catastrophically fail". Secondly, device A also did not fail the specification limits of drain current and gate current at the particular off state voltages applied (V_g=-3V/V_d=10V & V_g=-8V/V_d=50V respectively). For these off-state conditions, the upper specification limit (USL) of gate and drain current are 1mA/mm of gate periphery (i.e., 10.8mA total current) and I_d and I_g are clearly within those limits. Device A exhibits a "soft" failure mode of leakage imbalance, where the device failed for having much higher off-state three-terminal drain leakage than gate leakage; meaning the channel of the device does not entirely pinch off when the device is biased into the off state. Thus, not all the drain leakage is flowing from the positively biased drain to the negatively biased gate, most of the drain current is flowing elsewhere to ground. If this device were delivered to customers, when the device is supposed to be off it could still allow a small amount of current to flow. Furthermore, having such high drain current as fabricated is indicative of a weak device; if all of the excess drain leakage is being conducted under a relatively small gate defect, where pinch off is being inhibited by some mechanism, the local current density and power dissipation could be excessive and eventually lead to a catastrophic failure. Such a device would have a much shorter life span than other "good" devices.

As stated before, an imbalance current failure points to a potential problem with the gate metal stack. This is the case because if a device fails for imbalance it means that the gate is not properly pinching off the channel and turning the device off. There are many theories as to what the issue could be including: deformed gate metal, missing gate metal, gate metal not being in intimate contact with the semiconductor, gate obstructions, etc. Since this device failed for all imbalance current screens that it underwent, any issue with the gate metal could be the root cause of failure for device A. Thus, spectroscopic and microscopic analysis is needed to prove the cause of the high imbalance current.

The first thing that must be done is an inspection of the device under a high-magnification microscope. Since the device was covered in gel coat (a surface protective layer typically applied to a device during the assembly process), scanning electron microscopy (SEM) could not be performed as the gel coat charges uncontrollably and inhibits SEM imaging. Therefore, an optical microscope must be used. This allows one to see the details of the device and the channel and look for any abnormalities. A high resolution stitched optical image of device A is shown in Figure 3.2. Acquisition of stitched high resolution optical images of devices is a useful first step in most FA activity as this allows the entirety of the device area to be archived and guarantees the ability to come back later to re-examine the “as delivered" device surface if necessary.

Figure 3.2: Optical image of device A captured by high-magnification optical microscopy.

If no obvious fabrication abnormalities can be seen, then the next thing to do is to perform emission microscopy (EMMI) analysis on the device. The device was loaded into an EMMI system and biased so that the channel was pinched off. The drain voltage was then increased until an emission signature was identified using a camera that is sensitive to the emitted light. The EMMI map that is obtained is laid over the optical image of the device to show where on the device the emission emanates. EMMI analysis monitors the emission of photons from the device over a specific wavelength. These photons are emitted by the recombination of energetic electrons and holes within the device. If the device is biased in the off state and EMMI emission is observed in an area of the channel, this is potential evidence that the EMMI emission is directly associated with a localized area of leakage and therefore would potentially be where the root cause of device failure is located. The EMMI analysis for device A is shown in Figure 3.3. An EMMI "hotspot" can clearly be seen and is the focus for further failure analysis.

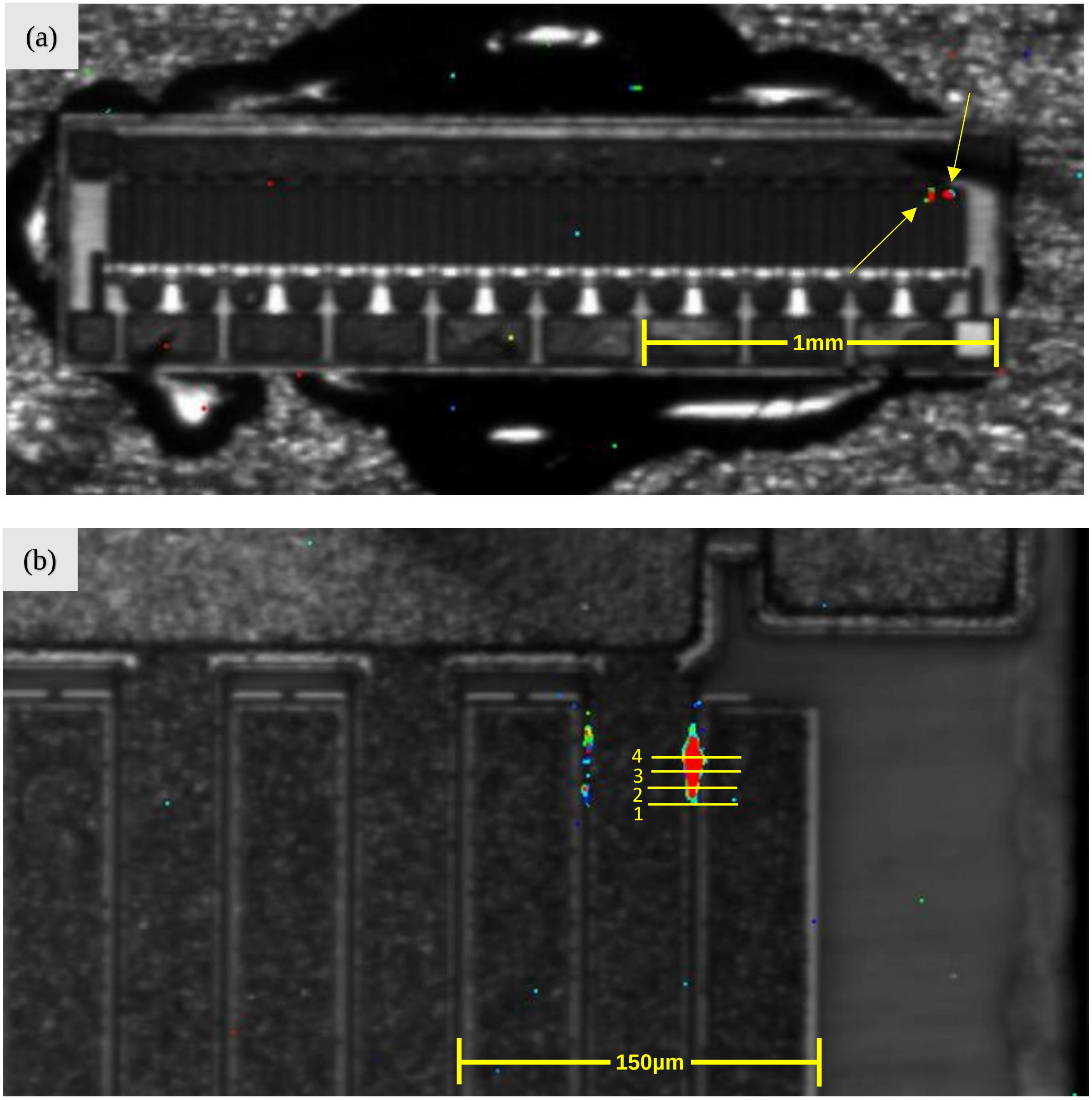


Figure 3.3: (a) EEMI emission spectroscopy results from device A taken with the lowest magnitude objective. (b) EMMI analysis results of the emission site and FIB cut locations taken at 20x objective.

Once EMMI analysis was completed and a region of interest had been identified, then a series of Focused Ion Beam (FIB) cuts followed by SEM imaging of the cross-section was performed to give insight into how the channel looked at that region of interest. Three FIB cuts were proposed, one as a control that is outside the region of interest, and two within the region of interest to see how the gate metal might be changing over distance. The first FIB cut shown in Figure 3.4 shows a cross-section of the gate metal and can be considered the control FIB cut. The gate metal stack is as expected, and the metal to semiconductor interface looks normal with expected symmetric gate metal placement over the gate stem.

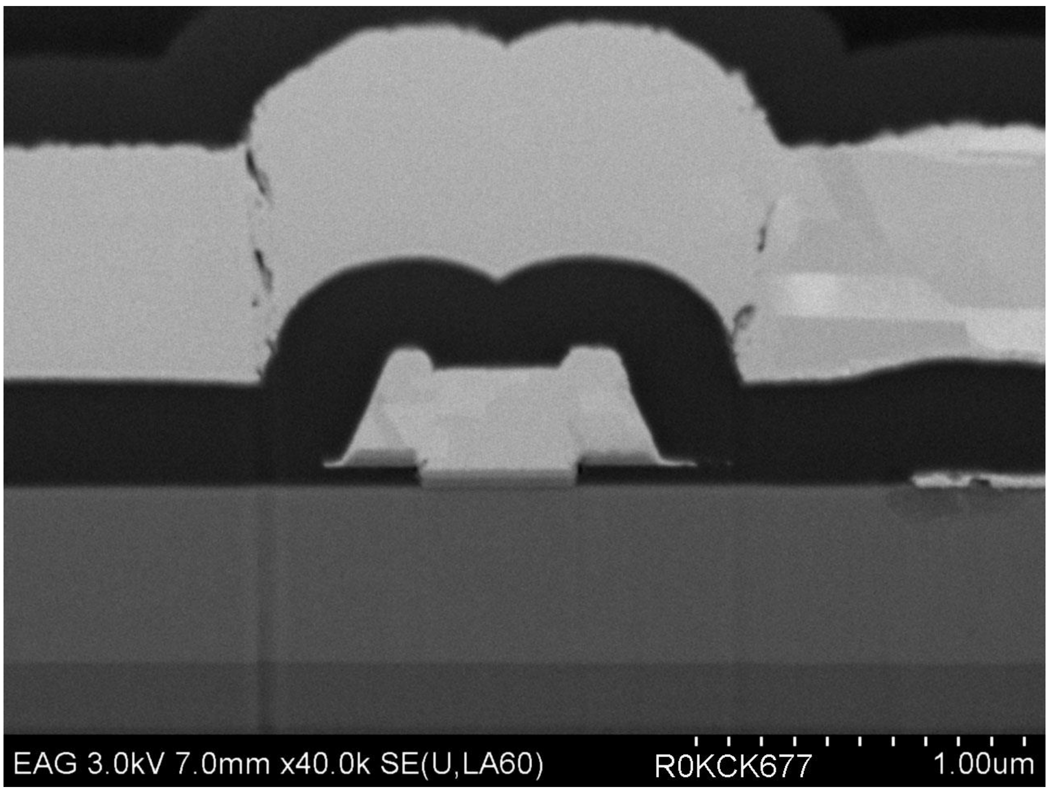


Figure 3.4: FIB cut 1 (control) focused on the gate metal stack. The metal-semiconductor interface is seen, as well as the source field plate.

A second FIB cut was performed at the very edge of the region of interest. The cross-section SEM image of FIB cut 2 is shown in Figure 3.5. The gate metal is clearly seen, and the metal stack looks as expected. There are what looks like voids at the corners of the gate stem between the metal and Silicon Nitride layers. However, these voids are not the cause of this failure. Furthermore, the metal is shown to be in intimate contact with the semiconductor interface.

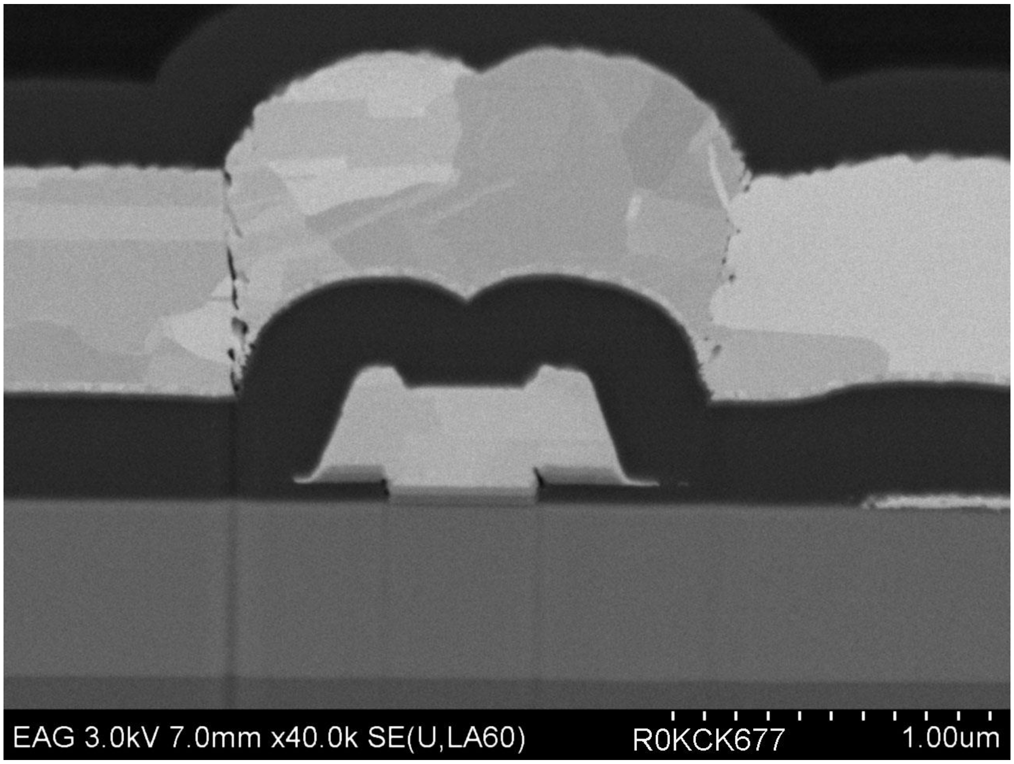


Figure 3.5: Second FIB cut focused on the gate metal stack. The gate-semiconductor interface is clearly seen as well as the source field plate. What appears to be voids are seen at the corner of the gate stem between the metal and Silicon Nitride layers.

Finally, a third FIB cut was performed deeper into the region of interest. This FIB cut cross-section can be seen in Figure 3.6. This cross-section clearly shows the cause of failure. The gate metal at the metal-semiconductor interface has degraded leading to loss of local gate control and resulted in high localized leakage as seen from DC testing. The first metal deposited was nickel; so, at some point in the fabrication sequence, the Ni was exposed to some agent that resulted in the Ni corrosion.

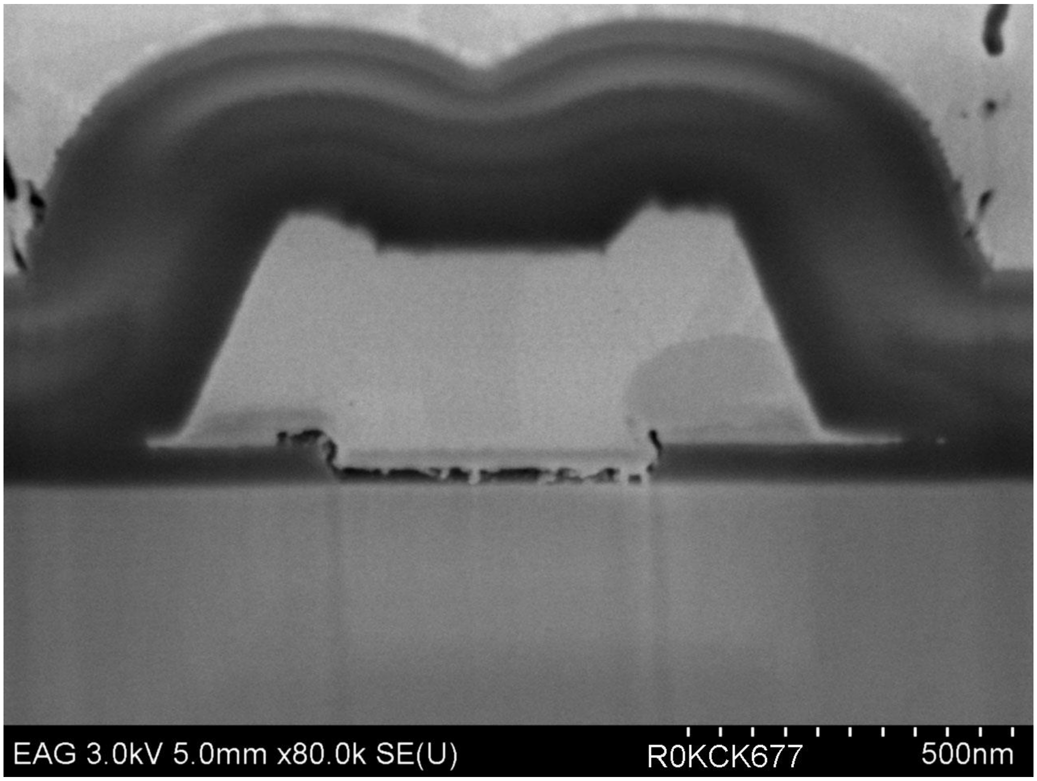


Figure 3.6: FIB cut 3 showing the cause of failure for device A. The gate-semiconductor interface has been compromised due to degradation of the Ni metal layer.

After DC measurements were taken and a symptom of the failure was seen, optical inspection was done using a high-resolution optical microscope. Since nothing was seen in the channel that would point to a cause of failure under an optical microscope, EMMI analysis was performed to determine the failure area. Using EMMI emission as a guide to the suspect failure area, FIB cuts followed by SEM imaging was done to determine the root cause of failure. The results of this failure analysis clearly show the cause of failure for this device is a degradation of the Ni metal at the gate-semiconductor interface. This degradation is believed to be due to HCl attacking the Ni metal during fabrication. HCl is not used in the processing of this device; however, since the device was fabricated in a foundry that also works on Si devices and HCl is used in their processes, contamination could have taken place if a workstation was not properly cleaned. An investigation by Subramanian et al. shows the selectivity of HCl to Ni as an etchant[14]. After learning why the device failed, precautions can be taken to reduce similar failures in the future. Reducing these failures ultimately improves device performance and yield which directly translate to a reduction in cost.

3.2.2 Foreign Body Gate Obstruction

Another device that had failed the imbalance screen was device B. Device B is another GaN on Si RF device with a 10.8mm channel periphery and 0.4μm gate length. This device passed every three-terminal leakage test as well as the gate-source diode test; however, it failed every imbalance screen in the test suite. The current imbalance sweeps are shown in Figure 3.7. As stated in the previous example, an imbalance failure is a symptom of a weak device. Both this device and the previous device passed all DC measurements but failed the imbalance screen. A failure of the imbalance screen is indicative of a device that is too leaky or failing to pinch off completely. A leaky device would still allow current to flow has and would be at the risk of having a shorter lifetime than a “good” device. If this device were to be sent to a customer, then it could potentially fail in the field, costing the customer and supplier considerably.

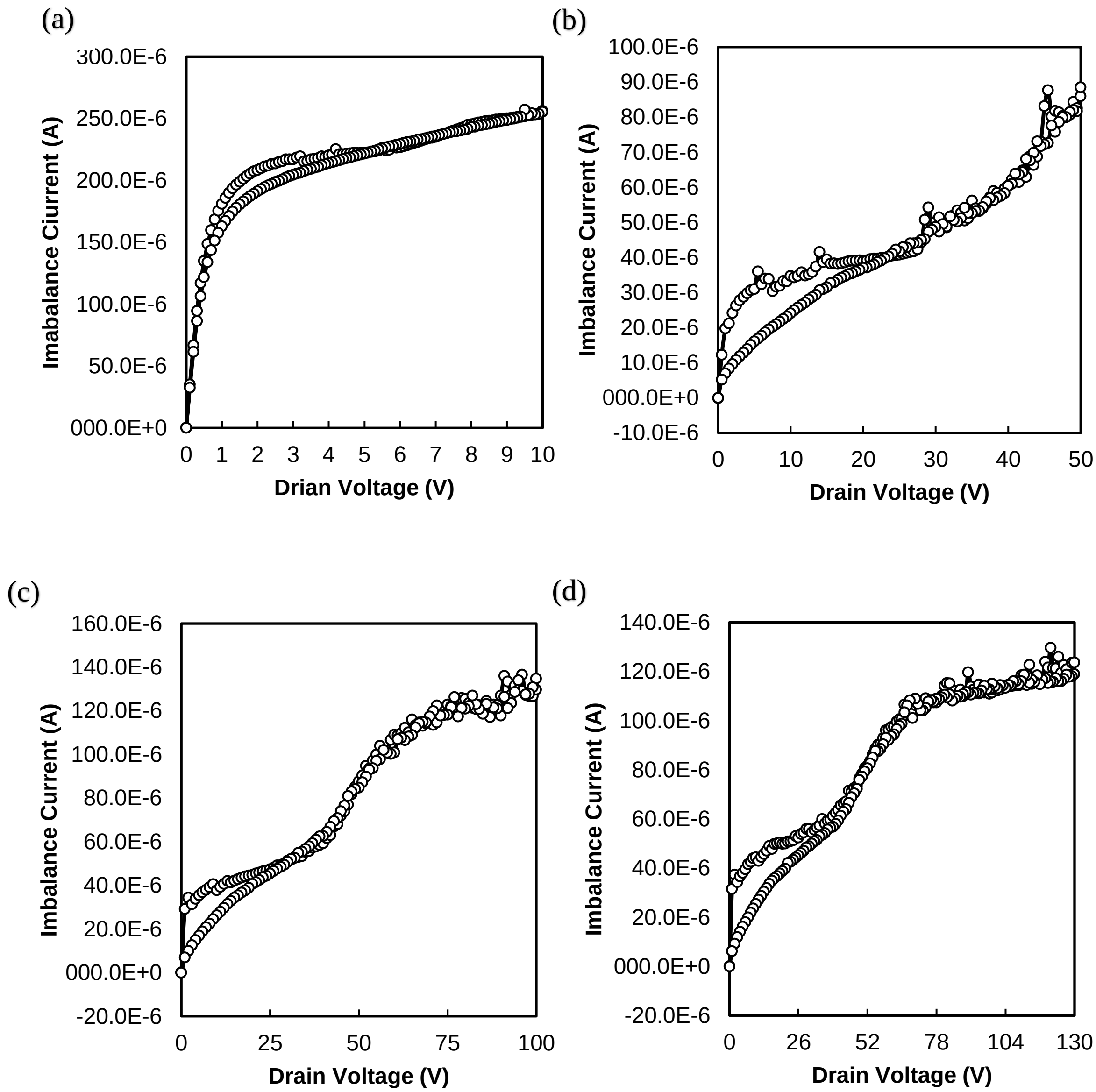


Figure 3.7: Imbalance current sweep for the off-state three-terminal gate and drain leakage for device B sweeping (a) from 0 to 10V and back again, (b) from 0 to 50V and back again. (c) from 0 to 100V and back again. (d) from 0 to 130V and back again. In every plot the imbalance current is roughly hundreds of microamps at its highest voltage bias meaning this device failed every imbalance current sweep, a good device would not have such a large amount of imbalance current.

As in the previous example, a device which fails for imbalance current at all tests points to an issue where the drain current is leaking to somewhere other than the gate. An extraordinarily high amount of drain leakage compared to gate leakage while in the off state means that the gate is not properly pinching off the channel and potentially keeping the device on in an isolated area causing high drain leakage currents.

After using the DC measurement suite to identify a symptom of failure; an optical inspection of the device using a high magnification microscope was once again employed to check for any visible fabrication defects. The device was inspected under high magnification, but no anomalous features were observed that would point to a specific cause of failure. An optical image of the device is shown in Figure 3.8 below.

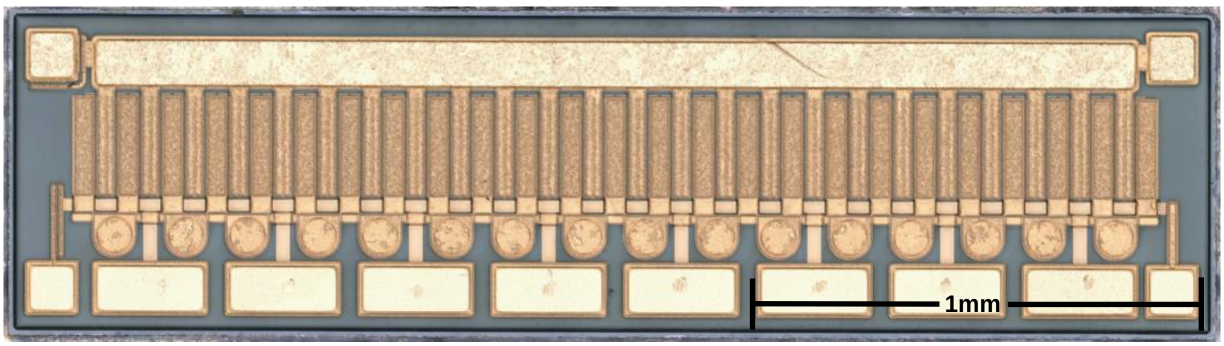


Figure 3.8: Optical image of device B taken with a high magnification optical microscope.

Since nothing could be gleaned from an optical inspection, the next step was to perform EMMI analysis. The device was loaded into an SEM and biased in the off state. The high amount of leakage due to a short showed an EMMI hot spot in the channel of the device. The EMMI spectrum is shown in Figure 3.9. This hot spot is believed to be the point of failure for this device.

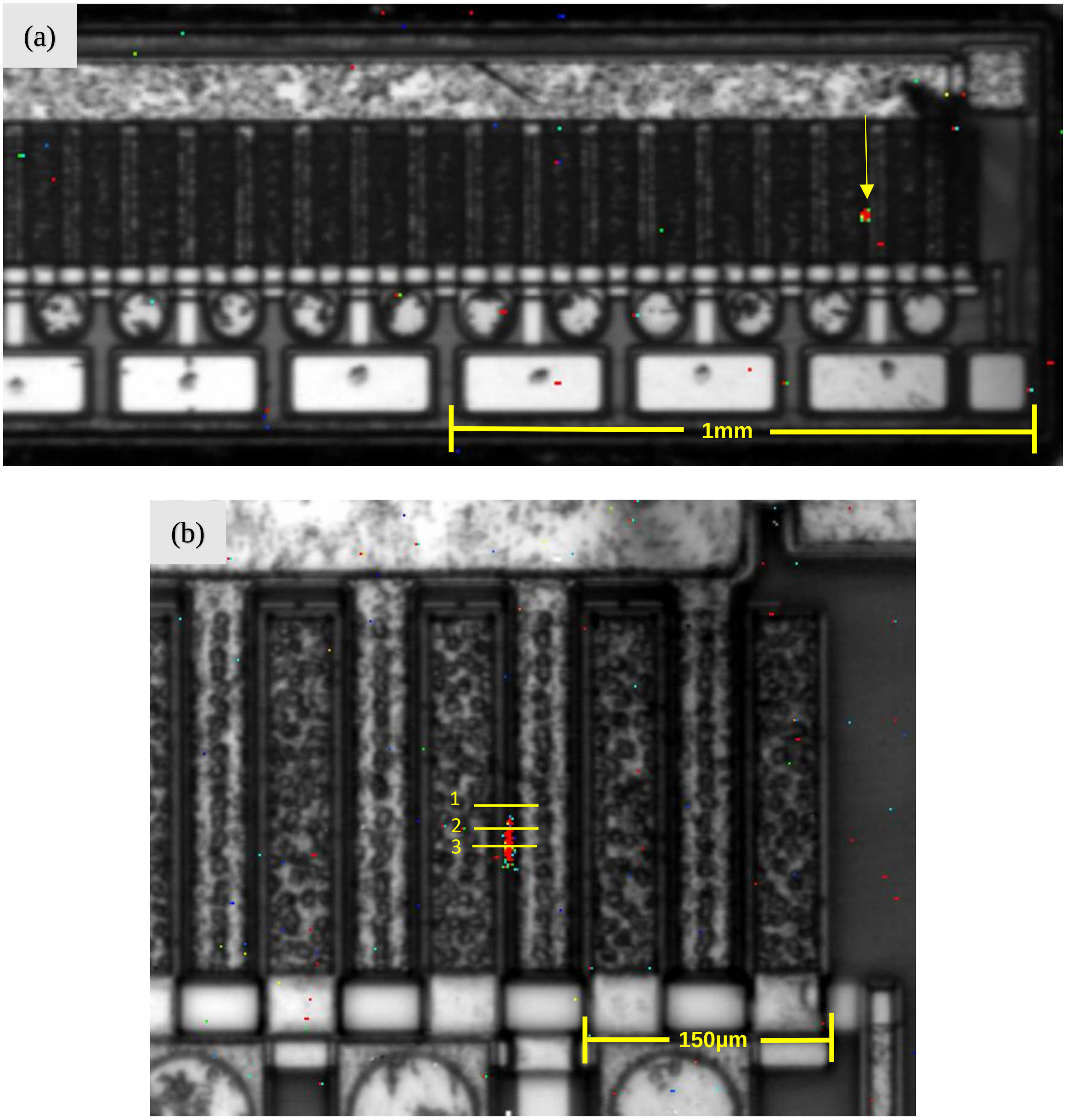


Figure 3.9: (a) EMMI Spectrum of device B showing the EMMI emission location. (b) Magnified image of the EMMI emission location showing exactly where it is in the channel as well as the proposed FIB cut locations.

A series of FIB cuts were planned at the EMMI location to determine the root cause of failure for the device. One FIB cut would be the control while the other two FIB cuts would be in the area of EMMI emission. The first FIB cut, and SEM cross-section is shown in Figure 3.10. This cut is the control and is expected to have no abnormalities. From the SEM image one can see that the gate metal stack alignment to the etched gate stem is asymmetric but still intact, and the metal is in intimate contact with the semiconductor interface. This asymmetry is not desired and would impact RF performance; however, it is not the root cause of failure for this device.

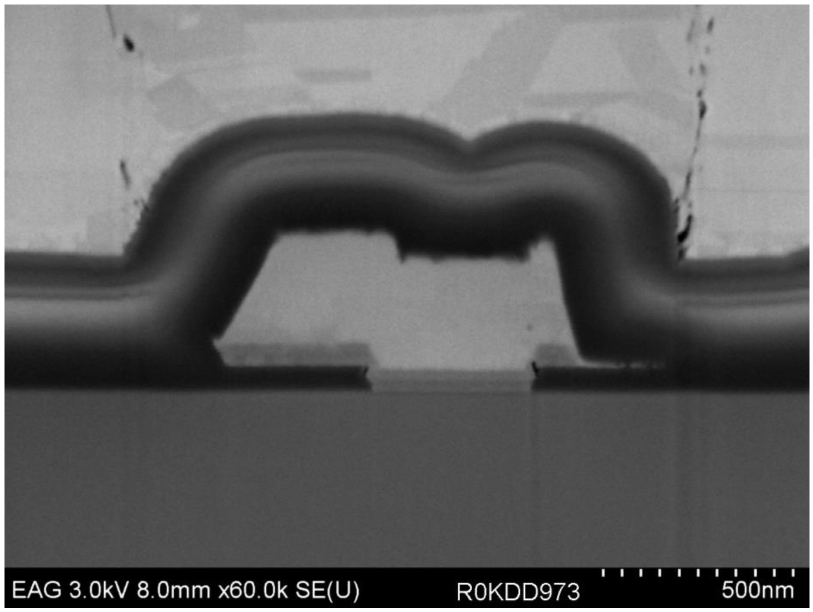


Figure 3.10: SEM cross-section of FIB cut 1 which is the control cut. The gate metal is in contact with the semiconductor and is intact. Asymmetry can be seen with the gate metal, but this is not the cause of failure for this device.

A second FIB cut was performed at the edge of the EMMI emission site and is shown in Figure 3.11. This FIB cut was at the edge of the EMMI emission and might show some sign of the reason for failure. The asymmetry of the gate metal stack is similar to the asymmetry seen in FIB cut 1, but the metal stack is intact and the metal to semiconductor interface appears unobstructed.

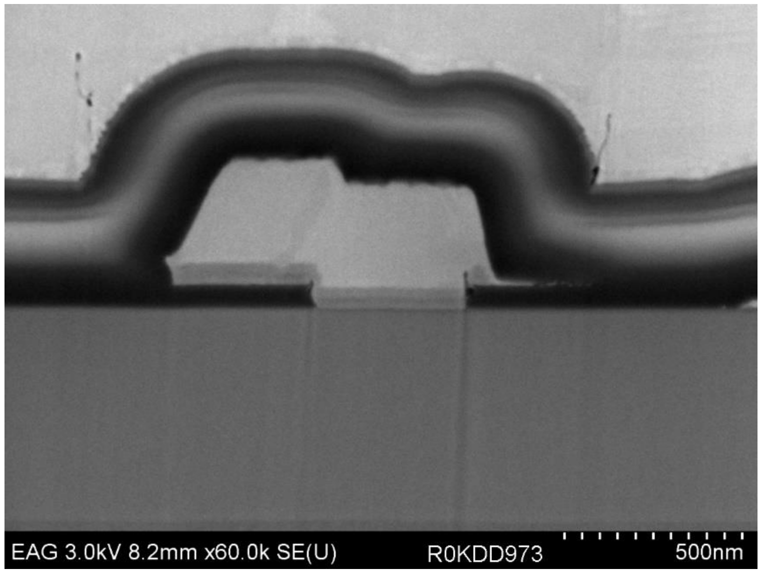


Figure 3.11: FIB cut 2 SEM cross-section. This cut was at the edge of the EMMI emission site. The metal stack is asymmetric but otherwise looks as expected.

A third FIB cut was performed deeper into the emission hotspot. This cut was expected to yield the cause of failure for the device and is shown in Figure 3.12. The cross-section shows that the gate metal is severely compromised. There is very little metal contacting the semiconductor, there are what look like voids throughout the metal stack, and the metals seem to have mixed at some point during fabrication. To understand what happened to the gate of this device; the cross section was thinned, and a foil was extracted for STEM analysis.

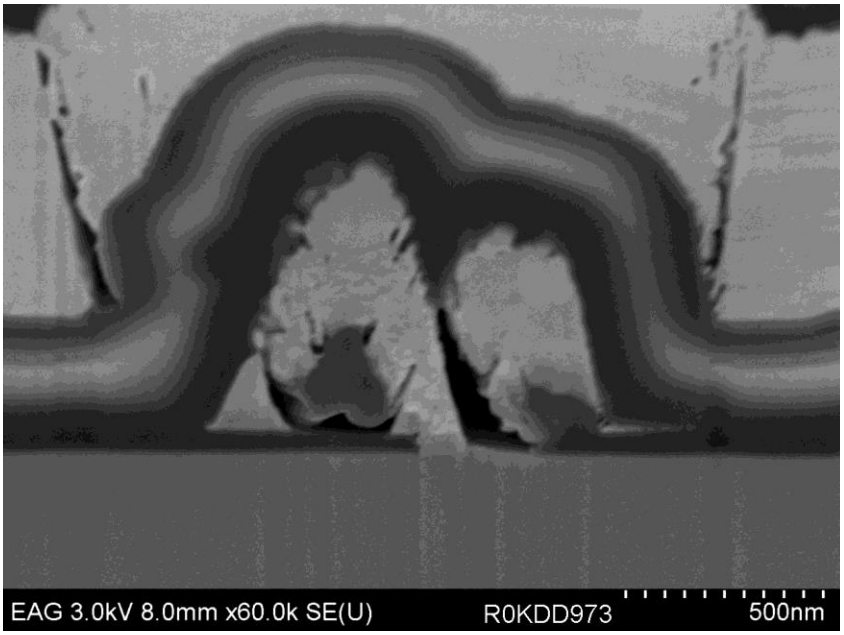


Figure 3.12: Cross-section from FIB cut 3 showing a highly compromised gate metal. Further microscopic and spectroscopic techniques are needed to understand the cause of failure for this device.

Scanning Transmission Electron Microscopy (STEM), was used to see how the gate developed over distance. STEM utilizes a rasterized beam of electrons to image not only the surface of the sample, but also into the sample. STEM images are shown in Figure 3.13 and give further insight into how the gate developed during fabrication. The STEM image shows a deformed gate metal and what looks like a particle on the right side of the gate. The transmission electron image shows how the gate metal looks through the foil, and confirms that the gate metal is deformed, compromised and has limited contact with the semiconductor surface throughout the foil thickness. This local region of the device would therefore be significantly compromised in terms of its ability to modulate current through the channel at this area of the device.

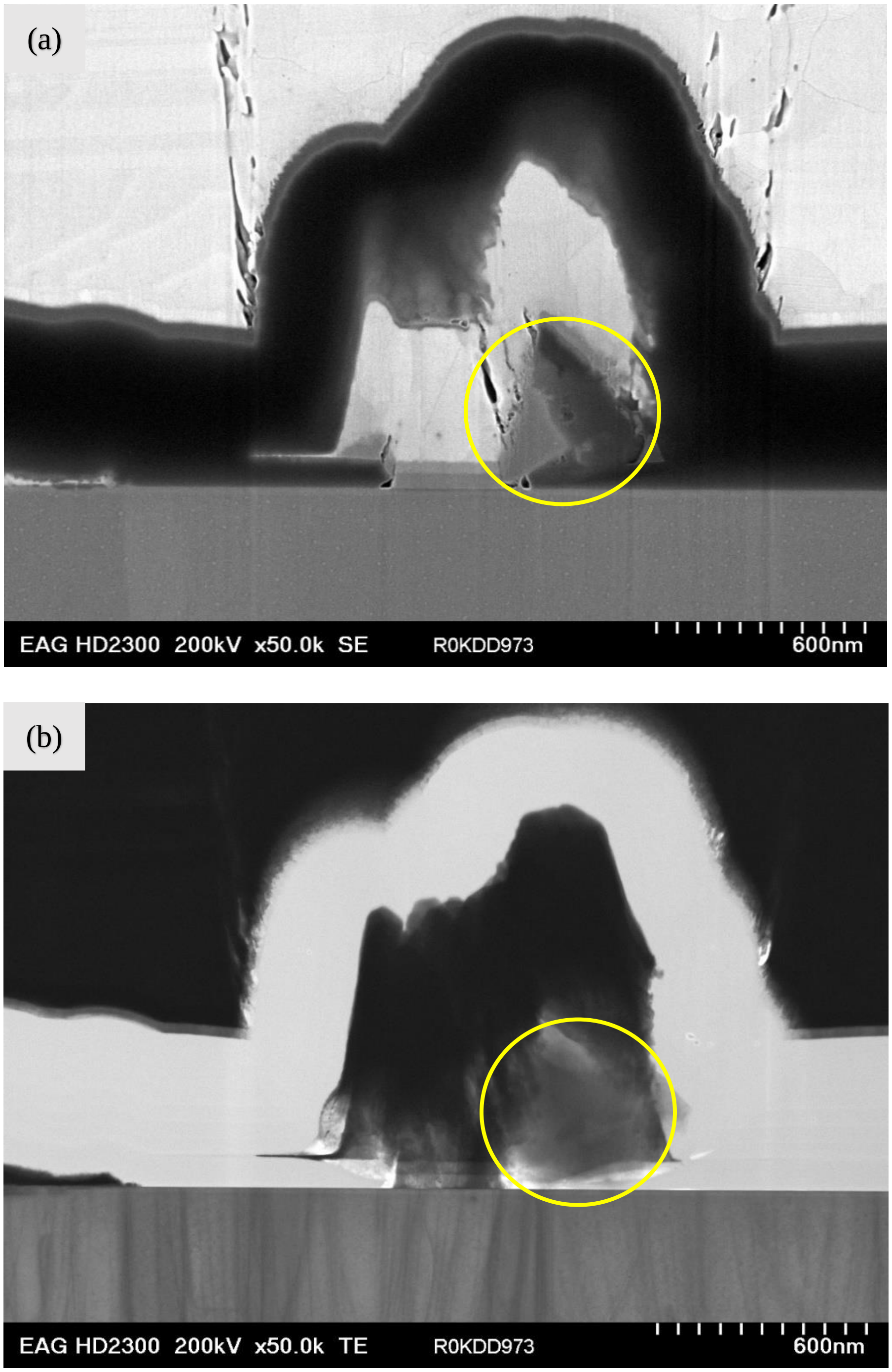


Figure 3.13: (a) STEM image of the thinned cross-section taken from device B. The gate metal is highly compromised, and a particle seems to be blocking the right part of the gate as shown by a yellow circle. (b) Transmission electron image of the same thinned cross-section. This image shows that the gate metal is deformed throughout the entire foil.

After STEM analysis showed what looked like a particle obstructing the gate, EDS was performed to determine the chemical composition of the obstruction. EDS, or Energy Dispersive

X-ray Spectroscopy, is a spectroscopic technique that gives elemental composition of a sample. EDS uses an energetic electron beam to excite the sample; the sample then emits characteristic radiation associated with each excited element in the sample which is collected by a detector which outputs the data as an energy spectrum. The location of the peaks of the spectrum give insight into the elemental composition of the sample. The location of the peaks of the spectrum gives insight into the chemical composition of the sample. The EDS spectrum of the particle that has interfered with the gate formation is shown in Figure 3.14. The peaks of the spectrum correspond to gallium; meaning that the particle is most likely GaN debris that was deposited on the surface at some point during processing, possibly during the etch of the silicon nitride prior to gate metal deposition.

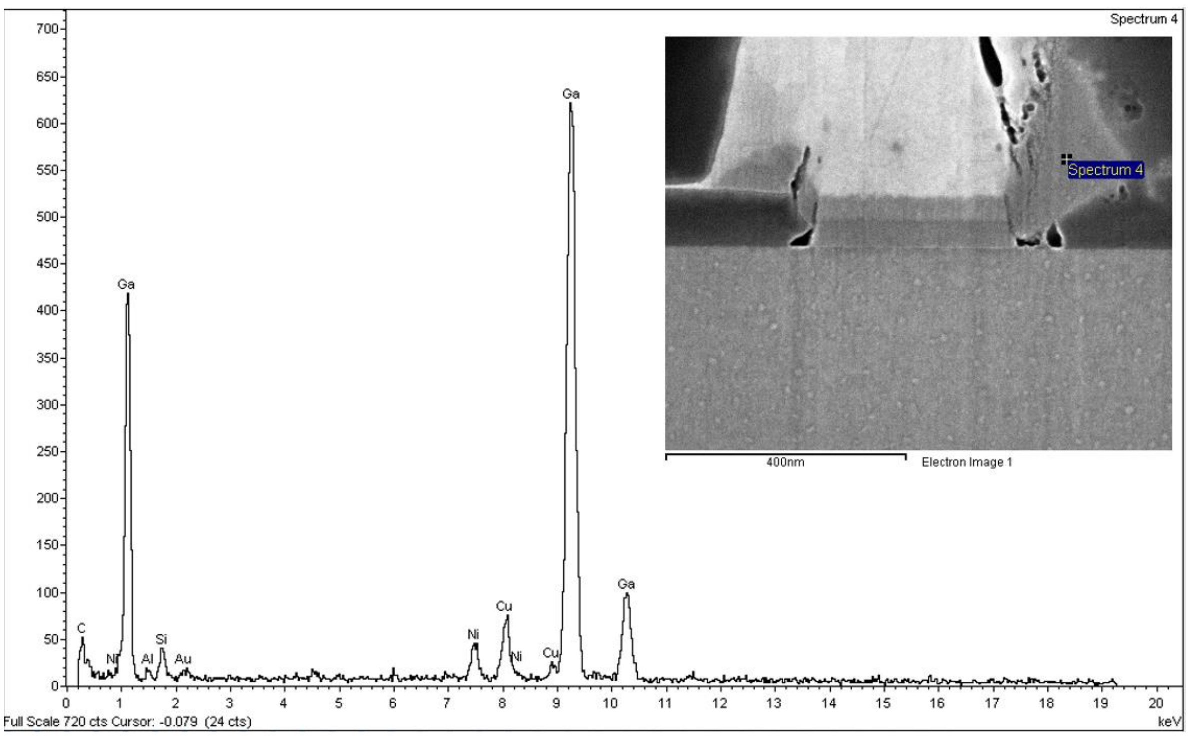


Figure 3.14: EDS spectrum of the obstructed gate from the STEM foil. The spectrum shows that the object consists of Gallium and is most likely GaN.

In conclusion the cause of the high amount of imbalance current in this device was an obstructed gate. The gate metal was partially obstructed by a particle of GaN that had deposited on the surface of the wafer during fabrication and interfered with the deposition of the gate metal stack. Since the gate metal stack was compromised, the device was not pinching off the channel at this region of the device and high amounts of leakage current resulted even when the device was supposed to be off. Imbalance current was the symptom of the failure; through the use of microscopic and spectroscopic techniques, gate obstruction was determined to be the root cause of failure. Remedying this root cause of failure increases fabrication yield, device quality and reliability thus saving the manufacturer and customer money.

3.2.3 Vertical Leakage Path Due to an Epitaxial Defect

The device that was focused on in this section is device C. Device C is a 10.8mm channel periphery 0.4μm gate length GaN on Si RF device. Device C failed for imbalance at all voltage tests, but in contrast to the other devices, the magnitude of the leakage increased with an increased drain bias. The root cause of failure for the previous devices was related to the gate metal stack being deformed or damaged in some way. A study of Device C is performed to see if the difference in imbalance current behavior can be attributed to a different location of failure within the device. The Imbalance current sweeps for this device are shown in Figure 3.15.

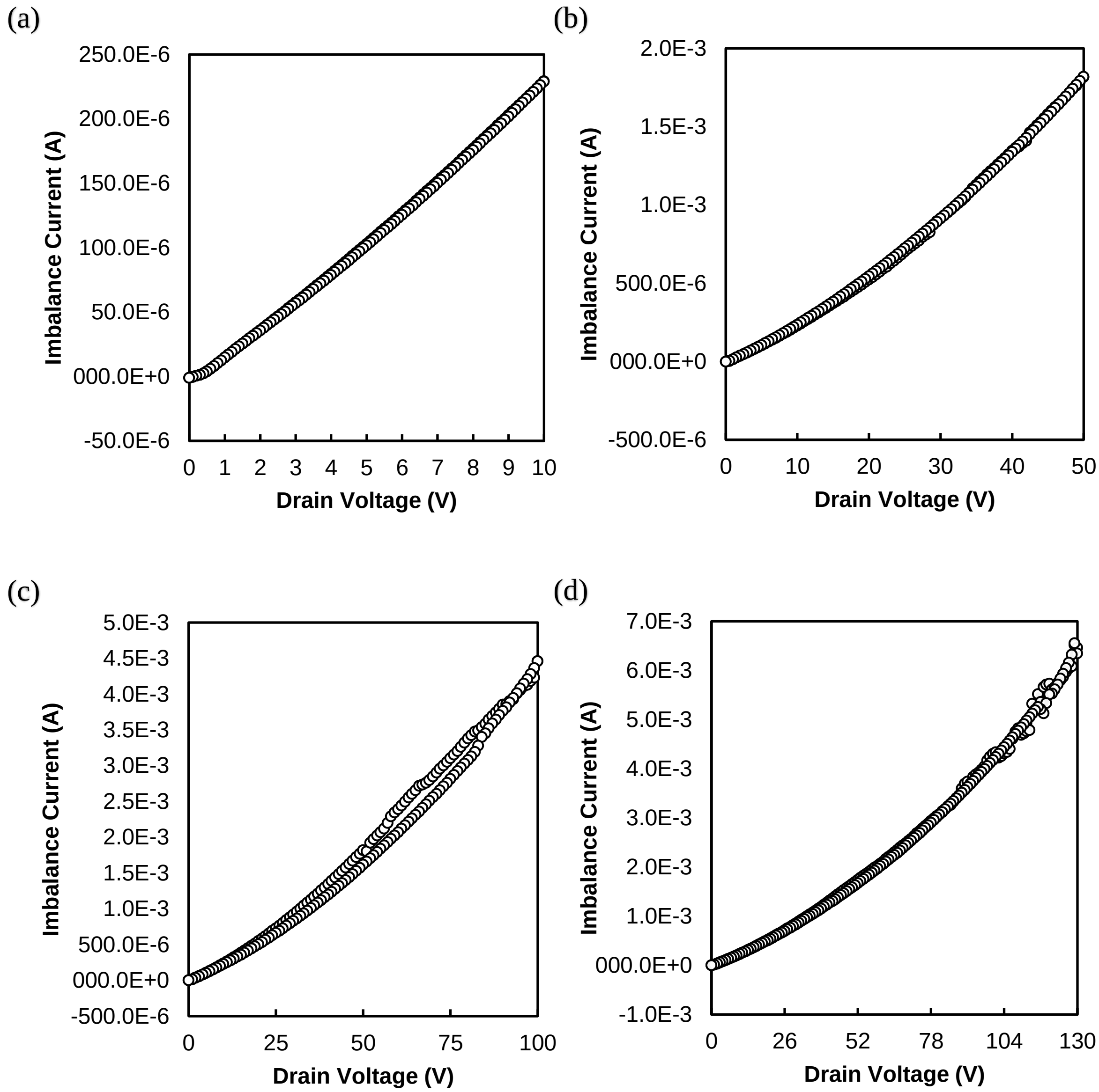


Figure 3.15: Imbalance current measurements of device C sweeping drain voltage from (a) 0 to 10V and back again, (b) 0 to 50V and back again, (c) 0 to 100V and back again, (d) 0 to 130V and back again. The imbalance current of interest is the point at the max drain voltage for each test. In these figures with an increased drain bias the magnitude of the imbalance current also increases contrary to the behavior of the previous devices.

The imbalance current at each drain bias for this device was much higher than expected, and an increase in the drain voltage resulted in an increase in imbalance current. This failure symptom means that the device is leaking more when the drain is biased with a higher voltage. If there were to be an issue with the gate metal, the imbalance current at the three high voltage tests

(50V, 100V, and 130V) would be similar but they are not. So, this suggests that the root cause of failure is not with the gate metal, but with some other leakage path that is exacerbated at higher drain voltage.

The first thing that needs to be done in order to determine the root cause of failure is an optical inspection with a high-resolution optical microscope. The optical image for device C is shown in Figure 3.16. Nothing can be seen on the device that would indicate a point of failure, so other microscopic and spectroscopic techniques are needed to determine the point of interest for this device.

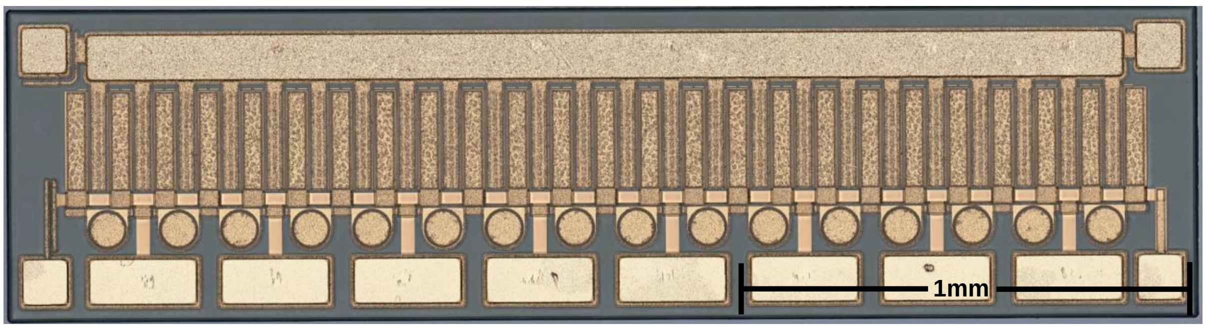


Figure 3.16: Optical image of device C taken using a high-resolution optical microscope at 1000x.

Since nothing could be seen via optical inspection of the device, EMMI analysis was performed to help determine the failure point for device C. The Device showed a strong EMMI emission site in the channel, and the EMMI emission is shown in Figure 3.17. The emission site is a part of the channel where current is still flowing and is the point of interest for further failure analysis.

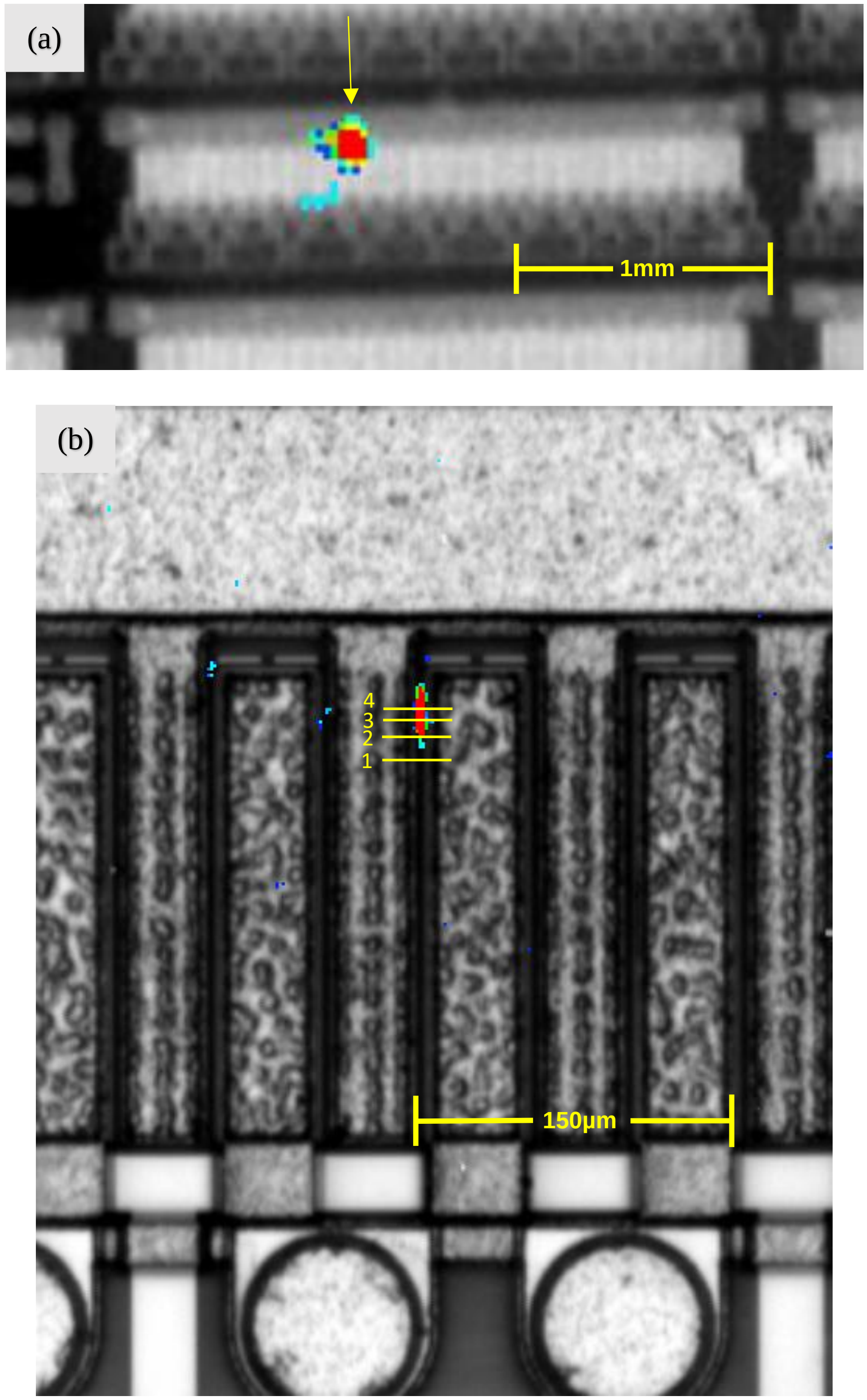
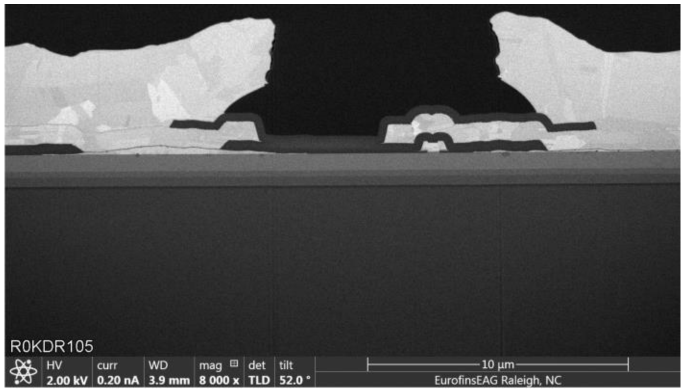


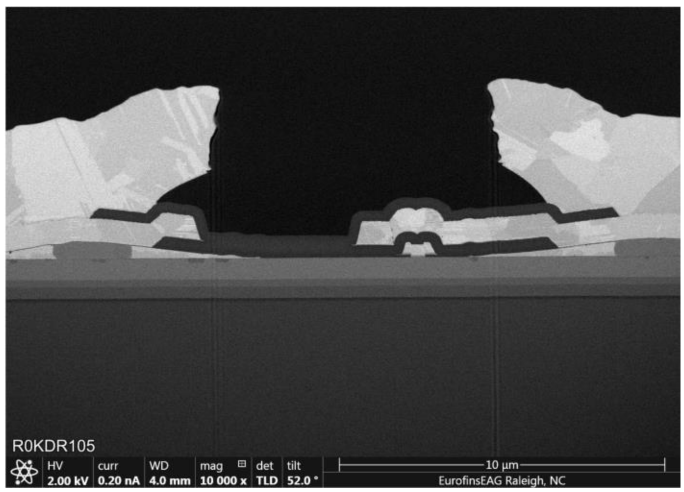
Figure 3.17: (a) EMMI emission site on device C. (b) high magnification image of the EMMI emission site showing its location in the channel of the device and the proposed FIB cuts.

After determining a point of interest for physical failure analysis, a series of four FIB cuts were performed. The first FIB cut was a control cut that is used to make sure the device looks normal outside of the emission site. The next three FIB cuts are inside the EMMI emission site and are expected to show the root cause of failure for device C. The first three cross-sectional SEM images from FIB cuts one through three are shown in Figure 3.18. The gate metal as well as the ohmic contacts do not look damaged, have proper dimensions, and are all in contact with the semiconductor surface, which is expected from the control FIB cut. The area of dark contrast in the ohmic contacts in FIB cuts 2 and 3 is alloying of the metal during ohmic annealing and is not a cause for alarm.

(a)



(b)



(c)

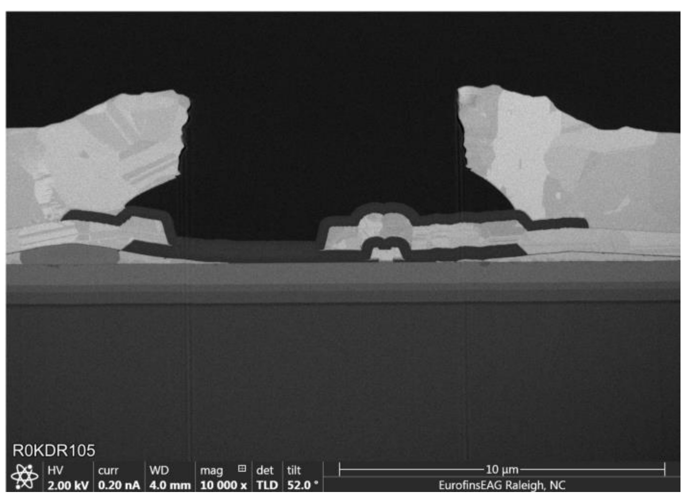
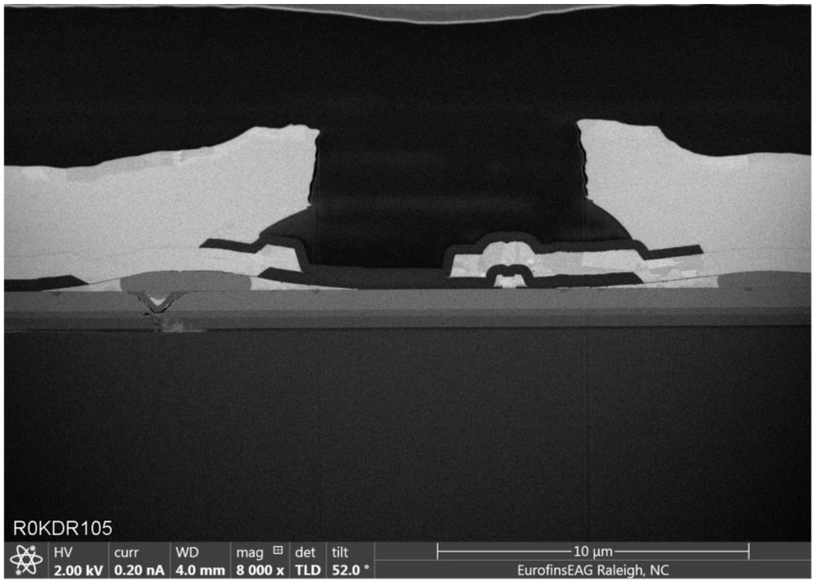


Figure 3.18: (a) Cross-sectional SEM image of FIB cut 1 (control cut). (b) Cross-sectional SEM image of FIB cut 2. (c) Cross-sectional SEM image of FIB cut 3. Nothing can be seen in any of these three cuts that would be the cause of failure for this device.

The next FIB cut was in the heart of the EMMI emission region and is shown in Figure 3.19. This image shows a defect beneath the drain ohmic contact that appears to penetrate into the GaN epi and all the way down into the Si substrate. Furthermore, the difference in contrast shows what looks like metal at the bottom of the defect. Discoloration at the bottom of the epi stack suggests that this is a vertical leakage path between the drain ohmic and the source on the back side of the device.

(a)

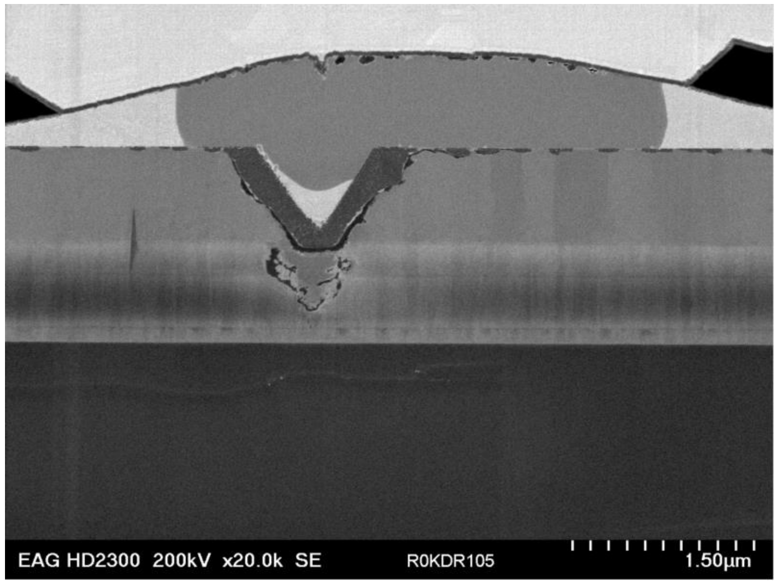


(b)

Figure 3.19: (a) Cross-sectional SEM image of FIB cut 4 showing a defect penetrating the epi beneath the drain contact. (b) Magnified image showing the defect beneath the drain contact.

The defect beneath the drain contact is presumed to be a pit that formed during epitaxial growth. To confirm that this defect is an epi pit and that it goes deeper into the cross-sectional image, a STEM foil was removed from this region of the device and examined. The secondary electron image and transmission electron image is shown in Figure 3.20. The secondary electron image shows the defect and a path of damage leading through the epi stack to the Si substrate. The transmission electron image shows the defect as well as a large area of damage within the Si substrate which supports the assertation that this was a vertical leakage path from drain to source.

(a)



(b)

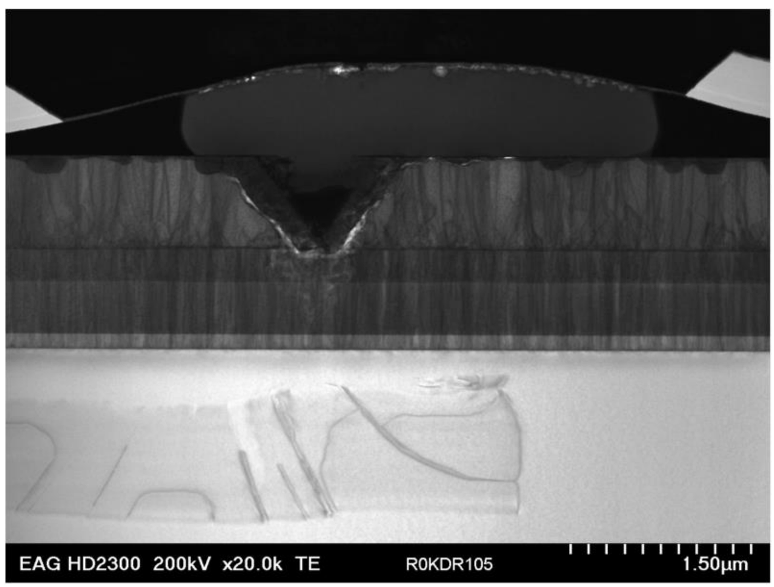


Figure 3.20: (a) secondary electron image from the stem foil lifted from device C. (b) Transmission electron image of the STEM foil lifted from device C.

Finally, if this pit had been on the surface of the wafer during fabrication, metal would be expected at the bottom and along the sides of it. This metal would allow for current to move downward and would be a part of forming that vertical leakage path from drain to source. To investigate this aspect, an EDS map of the defect area was performed and is shown in Figure 3.21. From the EDS map it shows that all four contact metals were deposited in the pit, and the gold that is usually the last contact had diffused during processing to the bottom of the pit. The proximity of the bottom of the pit to the Si (111) substrate is a much shorter distance than the top of the epi stack to the Si (111) substrate. When a high drain voltage is applied to the drain contact, this implies that the field strength from the bottom of the pit will be significantly higher than from the epitaxial surface. One explanation for the device failure is that the increased field strength along with the deformation within the pit, led to the breakdown at this region of the device.

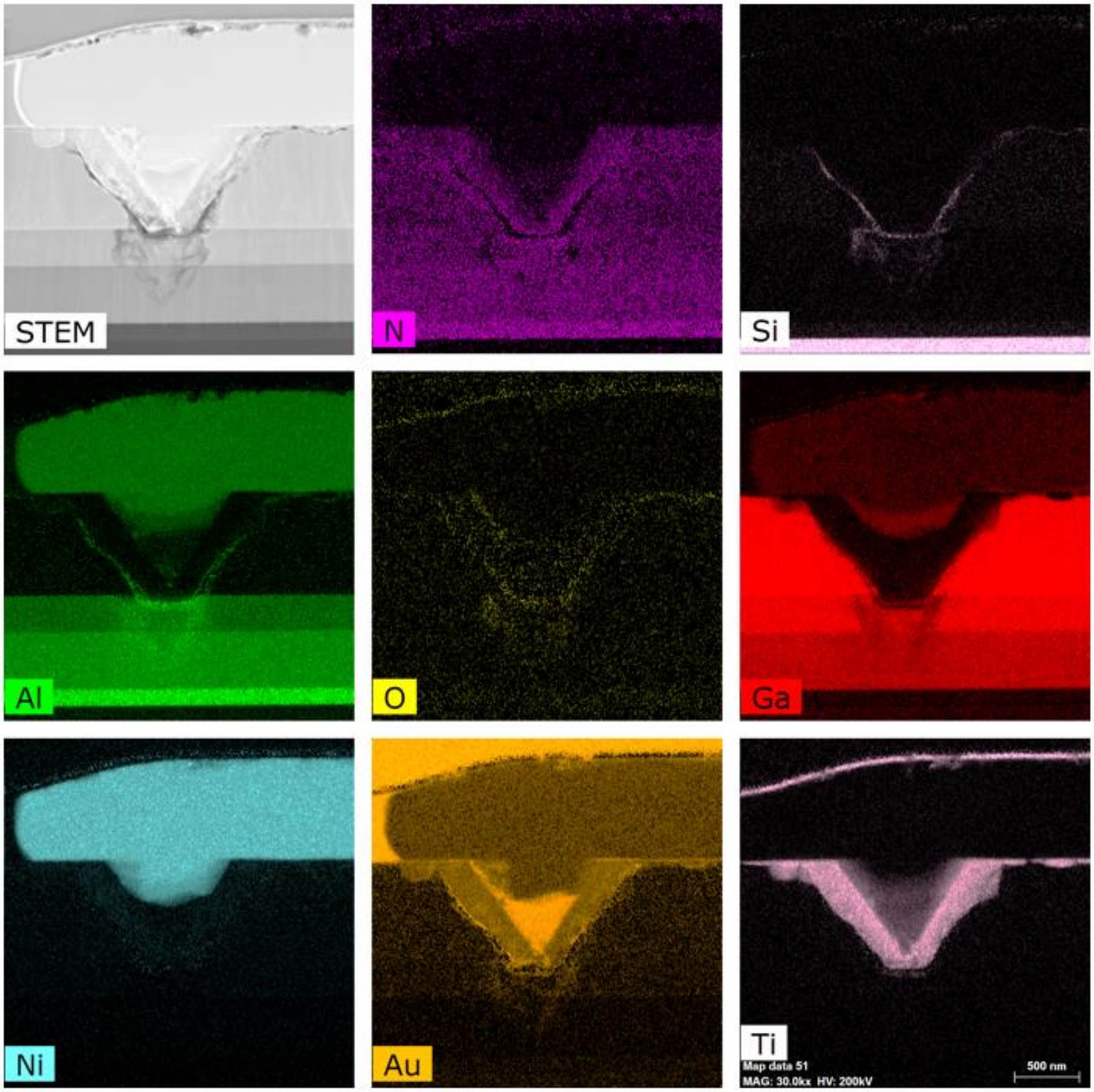


Figure 3.21: STEM map of the defect beneath the drain contact of device C. This map shows that the defect was filled with metal that was deposited as the contact for the drain.

In conclusion, device C failed for imbalance current at high voltages and not at all voltages like previous devices. This suggests that the gate was not the source of the defect since the gate voltage changing did not change the leakage current. However, it was the changing of the drain voltage that contributed to the imbalance current leading to the hypothesis that the failure was associated with the drain. An optical inspection and EMMI analysis was performed to determine the failure point for the device. After determining a point of interest, four FIB cuts followed by SEM imaging was done to find the root cause of failure. A defect was found beneath the drain contact and a STEM foil was removed to see how that defect developed deeper into the device channel. The STEM foil showed that it penetrated not only vertically into the epi and substrate, but also laterally into the channel. This kind of formation is indicative of an epitaxial pit. This pit was believed to have promoted a vertical leakage path from the drain contact to the source on the back side of the wafer. An EDS map was performed to determine if the pit was a void or if it was filled with metal. The map showed that it was filled with metal reinforcing that this pit along with the metal promoted a vertical leakage path between the drain and source.

3.3 Pinch Off Voltage Failure

The fourth device that was examined was a 2mm channel periphery 0.25µm gate length test structure that had failed for high leakage at the wafer characterization tests, device D. While this device had failed for high leakage and imbalance current at low voltages, it passed for leakage and imbalance current at high voltages, leading to a hypothesis that the device had failed to pinch off the channel. This was confirmed when the device failed for an out of spec V_p, meaning the main symptom was failing the pinch off voltage test. The device has a pinch off voltage that is much more negative than the target for that test, the pinch off voltage for device D is shown in Figure 3.22. The device had a more negative pinch off voltage than the spec limits would allow. This means that the device had to be biased with a negative voltage twice that of a normal device in order to deplete the channel and turn the device off. This symptom means that if the device were to be used in a customer's circuit, assuming the circuit was designed for a "good" device, then the device would always be on. This would be disastrous if delivered to a customer and sent to the field. Catching these failures early and changing the fabrication steps in order to eliminate these failures ultimately saves the customer and the manufacturer money.

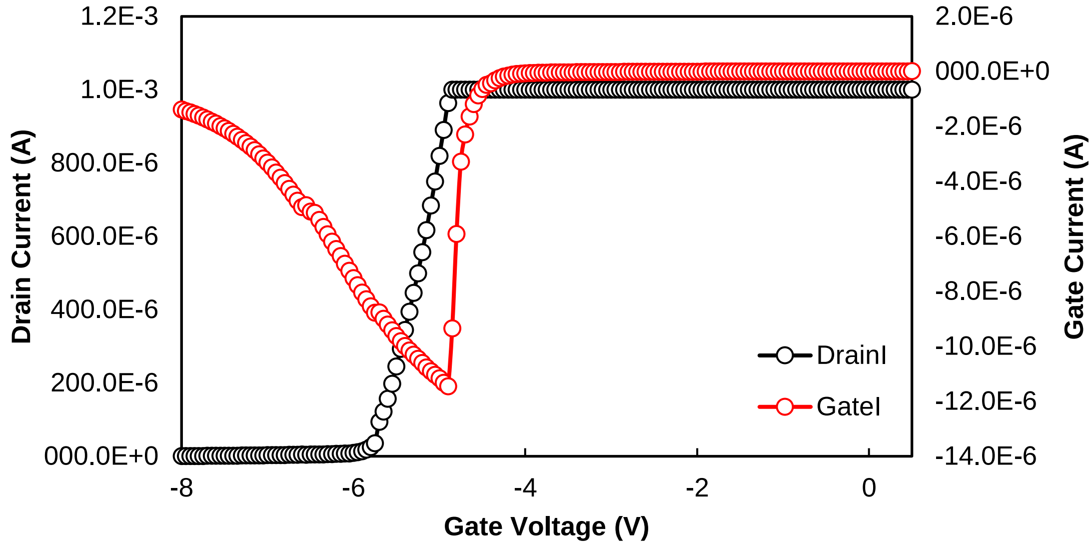


Figure 3.22: Graph of the pinch off voltage test showing that the device has a Vp around -6V which is roughly double the target for this test.

Since no passivation layer is used between the gate and semiconductor for any of these devices, the metal and semiconductor should be in contact with each other. A failure of pinch off voltage is a symptom of having some obstruction between the gate metal and the semiconductor surface. If there is anything between the metal and semiconductor, then a more negative voltage will have to be used in order to turn the device off because the obstruction causes the electric field to be weaker at the channel than normal. To deplete the channel with an obstruction, a higher magnitude of voltage is needed to apply the same field intensity at the channel. The pinch off voltage being twice that of a normal device is the symptom for the failure determined from DC testing.

The first thing that needs to be done is an optical inspection on the device which is shown in Figure 3.23. Nothing of interest can be seen from optical inspection, the device looks normal and no area of interest can be determined. The next step is to perform EMMI analysis to look for the failure site for the device.

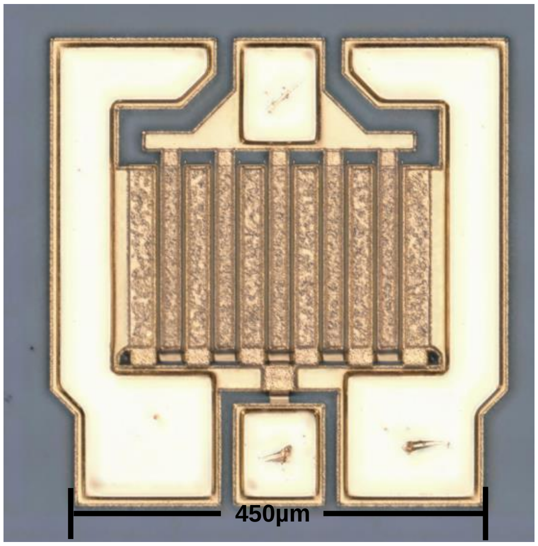


Figure 3.23: Device D imaged using a high magnification optical microscope. Nothing of interest is seen that would point to an area of failure for this device.

EMMI analysis was performed on device D and an emission site was found. This emission site is shown in Figure 3.24, and is believed to be the failure site. This emission site is the target for further physical failure analysis techniques.

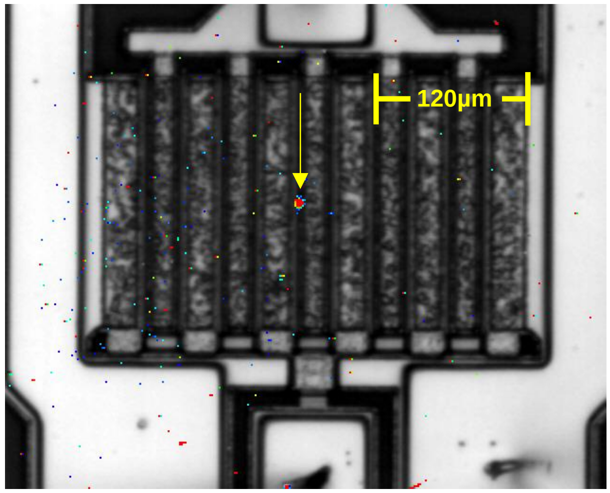


Figure 3.24: EMMI spectrum of device D. An emission site can be seen in the channel of the device, which is the target for further failure analysis.

Two FIB cuts were proposed for this device, one control cut outside of the emission zone and a second cut that is expected to show the cause of failure for the device. Since the emission site is relatively small, only one cut would fit within the emission area. The first control cut is shown in Figure 3.25. The gate metal stack is intact, and the metal is in contact with the semiconductor surface. There is slight asymmetry and a particle on the left side of the gate metal but neither of these would cause the device to fail for pinch off voltage.

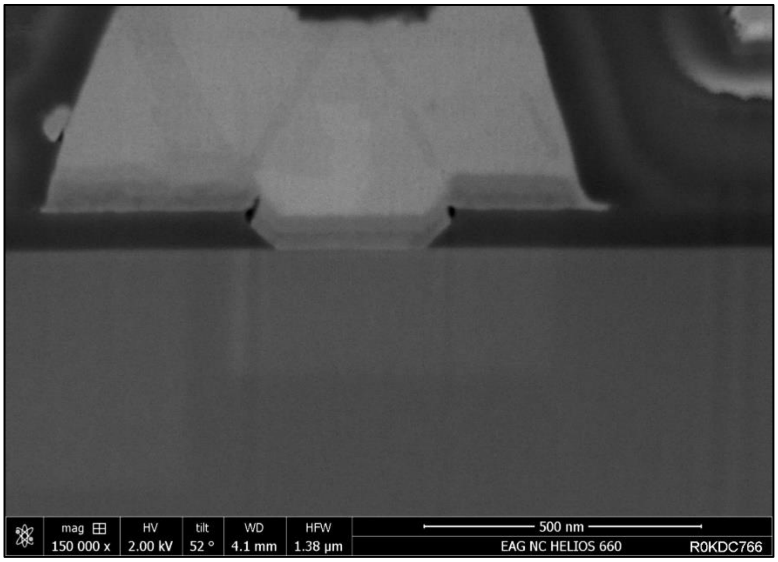


Figure 3.25: Cross section of FIB cut 1 for device D. The gate metal is intact and in contact with the semiconductor. Asymmetry is seen as well as a particle on the left side of the gate metal; neither of these are the cause of failure.

FIB cut 2, which was positioned in the middle of the emission site, is shown in Figure 3.26. The gate metal is intact; however, a small amount of Silicon Nitride is seen between the gate metal and the semiconductor surface. The SiN_x is obstructing the gate and forcing the pinch off voltage to be more negative, thus causing then device to fail.

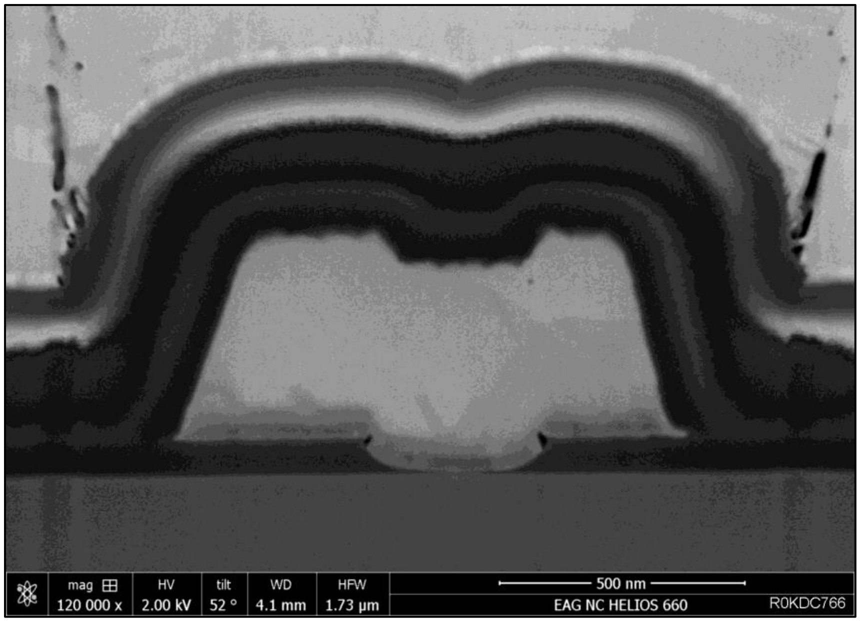


Figure 3.26: SEM cross-section of FIB cut 2. A small amount of Silicon Nitride can be seen between the gate metal and the semiconductor causing the device to fail for pinch off voltage.

In conclusion, a small amount of residual Silicon Nitride dielectric was seen between the gate metal and the semiconductor in the channel of device D. The SiN_x layer was not fully etched before the gate metal was deposited, causing a failure to pinch off the channel of the device. This was determined by the device failing for pinch off voltage, EMMI analysis found an emission site, and with the use of FIB cuts and SEM images the root cause of failure was found. This investigation supports a need to adjust the etch recipe for these devices in order to reduce failures in the future.

3.4 Discussion

The imbalance current screen is a powerful way of determining the symptom of failure for any device during failure analysis. An imbalanced device means that current is leaking from one terminal of the device mor so than others. Depending on how a device fails for imbalance, a certain terminal of the device can be pinpointed as the problem area. A change in imbalance current of hundreds of microamps to milliamps with a change in gate bias is important because it means the gate affects the magnitude of leakage in the device more so than the drain terminal. A change in imbalance current of hundreds of microamps to milliamps with a change in drain bias while the gate bias remains constant is important because it means the drain affects the magnitude of leakage in the device more so than the gate. This means that how a device performs in the 4 imbalance current tests can give insight into the potential failure mode of a device. A flowchart for the different outcomes from the imbalance current tests is shown in Figure 3.27.

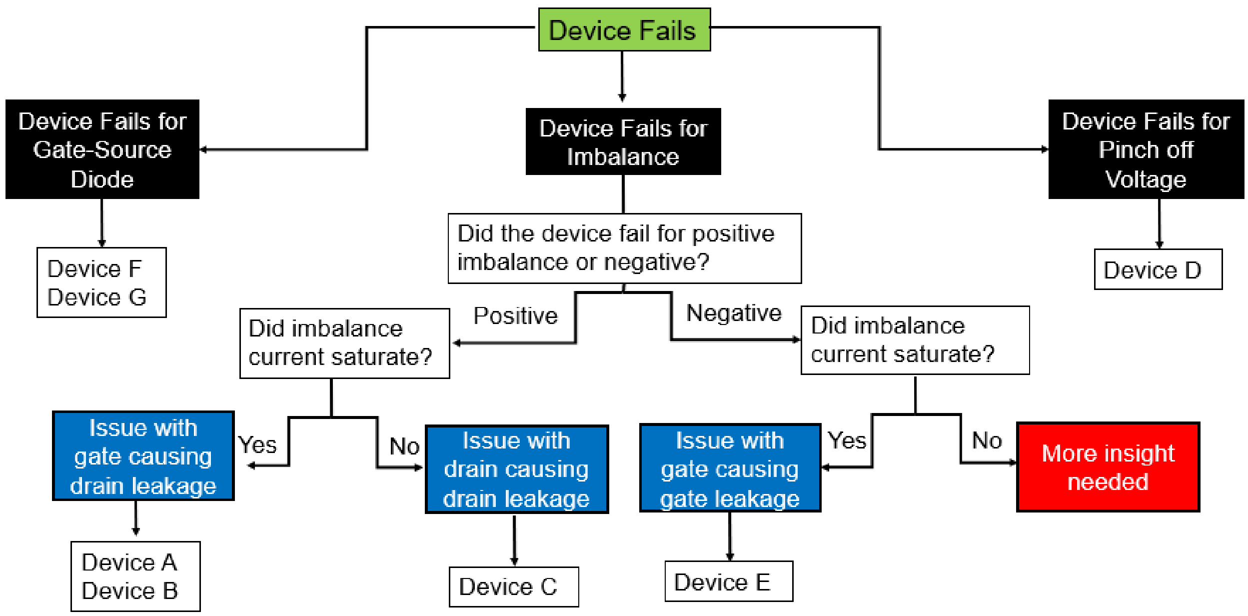


Figure 3.27: The different outcomes of the imbalance current tests and what insights they might give when determining a terminal of interest during failure analysis.

Furthermore, the magnitude of the imbalance current also is important in determining device health. The upper limit for imbalance current for these tests is 5µA/mm, this means that the upper limit for imbalance current changes depending on device periphery. For instance, a 10.8mm periphery device will have a 54µA upper limit for imbalance current. A device could fail just above this limit or it could have imbalance current orders of magnitude higher. The more the imbalance current is above the upper limit, the weaker the device is because it is leaking more current between the terminals.

3.5 Conclusion

In conclusion four examples of on wafer failure analysis were examined. Three devices had failed for imbalance current, while one had failed for an out of spec pinch off voltage. Each device underwent a suite of DC testing to determine the symptom for failure. A failure of the imbalance current screen means that there is a leakage path between either the gate and source or the drain and source. Devices that fail the imbalance screen have a shorter life span than other “good” devices and fail earlier when stressed due to their high leakage. A failure of pinch off voltage means that the gate is not pinching off the channel at all and the device stays on when it should be off. Next A series of microscopic and spectroscopic techniques were employed, mainly optical inspection, EMMI, and FIB cuts followed by cross-sectional SEM. After SEM imaging of each cross-section the failure mode was determined. Screening these weak devices and determining the cause of failure helps reduce the amount of field failures by eliminating these devices from final assembly. Successful determination of root cause of the failed devices can also lead to higher manufacturing yields as the semiconductor processing foundries can target process improvements to eliminate manufacturing defects levels associated with the root causes identified.

CHAPTER 4:

Failure Analysis of Packaged Devices

4.1 Introduction

Another concern in a production environment is device reliability which is determined after the device is packaged. Devices that have passed on wafer testing get diced and packaged for distribution for customers and for in house reliability testing. It is necessary to determine the root cause of failure for devices that fail these package tests so that the manufacturer is certain that the devices will not fail in the field. This chapter will go over three examples of failure analysis of packaged devices including the symptom of the failure, how the symptom affects device performance, and what this symptom could mean in terms of failure mode. Additionally, the spectroscopic and microscopic techniques used to determine the root cause of failure for these devices will be given for each failure analysis example.

4.2 Schottky Degradation Identified by Two DC Tests

The previous chapter outlined four devices that had failed for imbalance current. However, those devices were dominated by drain leakage due to the channel not being pinched off or a short between drain and source contacts. Gate dominated imbalance current and drain dominated imbalance current are a symptom of different failure modes and are identified in the imbalance current test. An imbalance current that is in the negative milliamp range is considered gate dominate while an imbalance current in the positive milliamp range is considered drain dominated. For instance, device E failed for imbalance current that was extremely gate dominated identified by an extremely negative imbalance current. Device E is a 4.14mm channel periphery and 0.25μm gate length device. An early insight into this extremely negative imbalance current can be seen in the gate-source diode sweep shown in Figure 4.1.

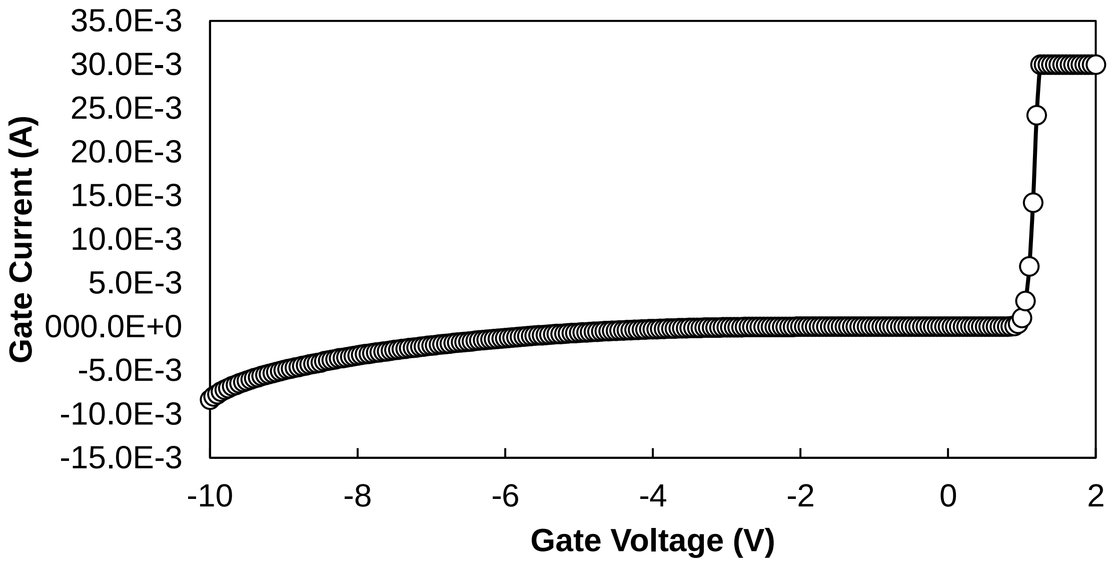


Figure 4.1: Gate-source diode sweep showing extremely high amounts of reverse leakage. The reverse leakage is in the mA range at the start of the test, which is very high.

This device did not fail for gate-source diode leakage; however, it gives insight into how the device might perform in the imbalance screen. A device that has a gate current of milliamps at -10V on the gate is indicative of a poor metal to semiconductor contact and is one of two symptoms for this device. A better look into the health of the gate metal is shown by looking at the imbalance current. The imbalance screen is ultimately what the device failed for and is shown in Figure 4.2. Having an extremely negative imbalance current means that the gate leakage dwarfs the drain leakage. If the gate is extremely leaky that could result in a lower lifetime for the device and increased power consumption while the device is supposed to be off due to leakage currents. This kind of behavior points to an issue with the device's gate metal to semiconductor contact. The gate is allowing milliamps of current to flow into it rather than the expected microamps suggesting that the Schottky contact had degraded in some way.

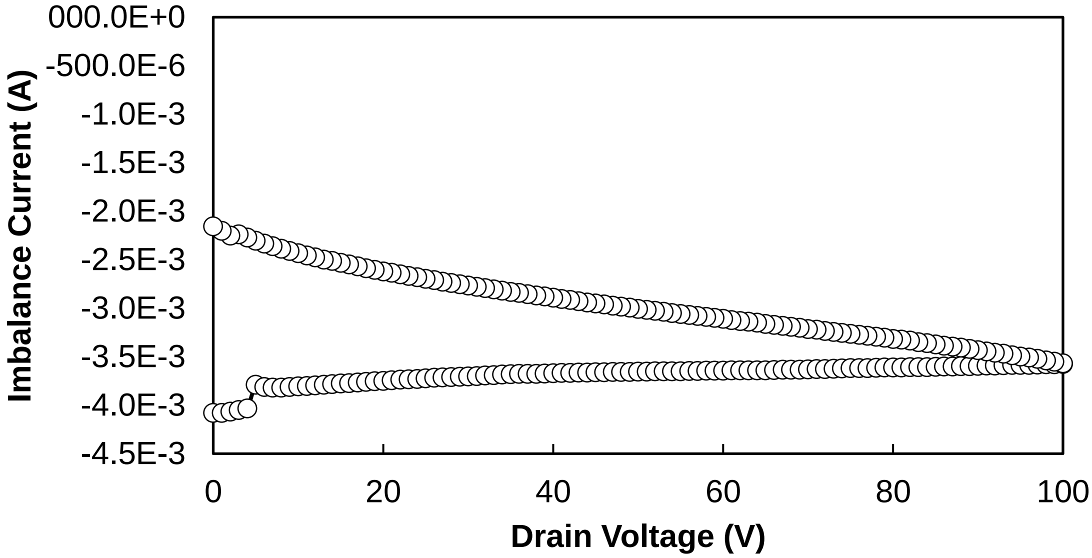


Figure 4.2: Imbalance current sweep for device E biased at -8V on the gate and being swept to 100V on the drain. The imbalance current is extremely negative, and in the milliamp range, implying that it is gate dominated in nature.

After determining the symptom of the failure, the first thing to do is an optical inspection. The device has a coating of BCB which will charge in an SEM and obstruct the image, so a high magnification optical microscope was used for imaging. An optical image of the device is shown in Figure 4.3. Discoloration is seen on the surface of the device in areas where the electric field was very high during reliability testing. The discoloration of the BCB is seen across all similarly stressed devices and would not result in failure.

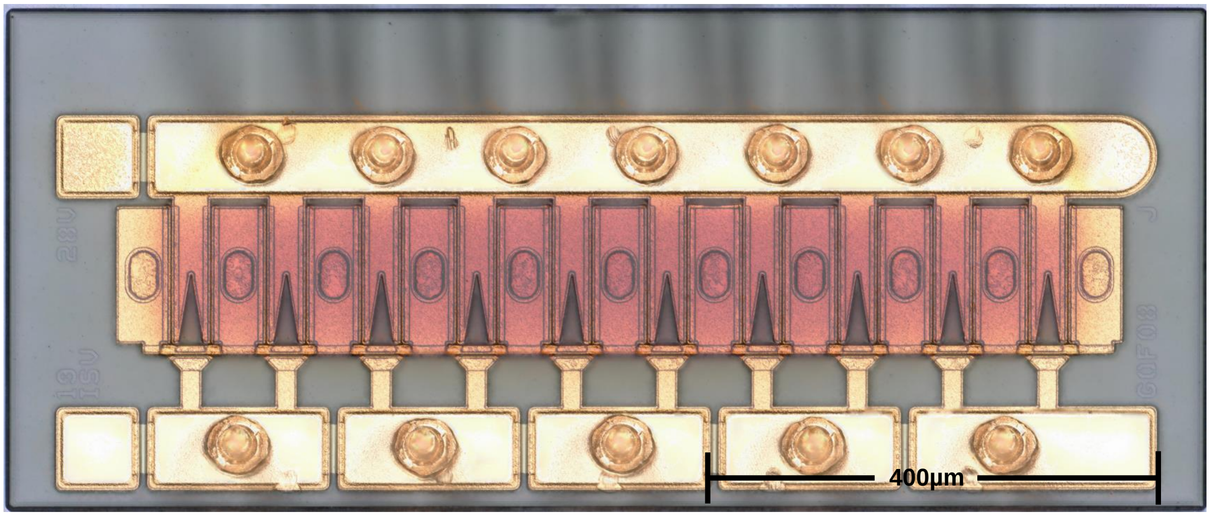


Figure 4.3: Optical image of device E taken using a high magnification optical microscope. The device has been packaged and underwent reliability testing which resulted in the discoloration of the gel goat covering the device. This discoloration is commonly seen in all devices following reliability testing.

Nothing can be seen from the optical image that would point to the cause of failure, so EMMI analysis was done on the device. The device was loaded into an SEM and biased in the off state, the drain voltage was increased until emission was seen. EMMI is used to determine a point of interest for further failure analysis; the emission spectrum for this device is shown in Figure 4.4. The EMMI analysis showed large amounts of emission; however, the emission was not located at a single point and was constant throughout most of the channel. As opposed to previous EMMI spectra, an emission spectrum that spans most of the channel points to there being an issue throughout the device instead of at specific points.

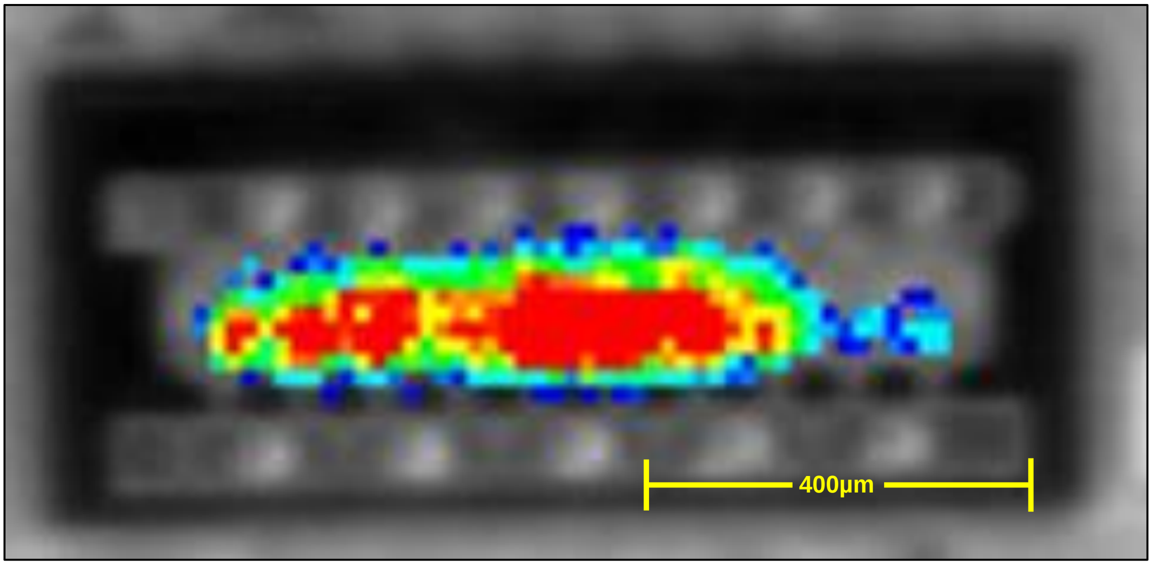


Figure 4.4: EMMI emission spectrum of device E showing EMMI emission throughout most of the channel of the device.

Since the EMMI emission was seen throughout the channel a point of interest was not needed to proceed further. A STEM foil of the channel was taken out of the device and analyzed to see how the gate metal looks after the stress from the reliability test. This STEM image is shown in Figure 4.5. The device's gate length is within specifications; however, just by looking at the contrast of color between the layers of the gate metal it looks as if the metal had diffused and moved along the sides of the gate. Areas at the corners of the gate metal seem to be voids that have been filled by metal that migrated during stress testing. Further spectroscopic techniques are required to determine what had moved.

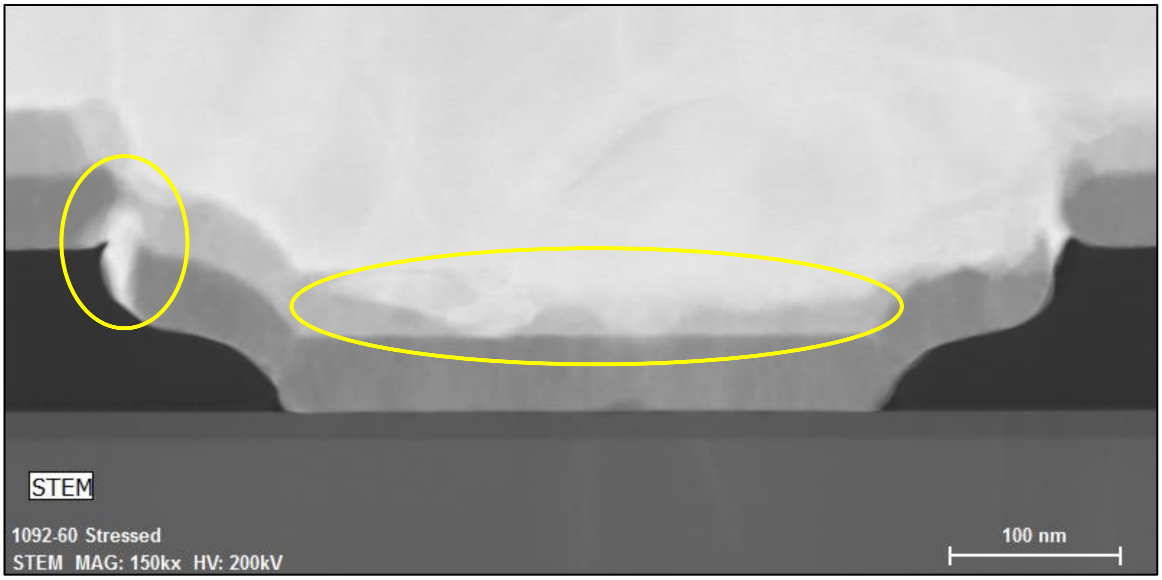


Figure 4.5: STEM cross-sectional image of the gate metal of device E. Contrast differences along the gate metal stack, identified by a yellow circle, indicate that some of the metal might have moved during reliability testing.

EDS was used to determine the chemical composition of the materials in the cross-section. This was done as a map of the STEM foil instead of at specific points and is shown in Figure 4.6. A map was performed on the entirety of the sample because it was important to see the elemental composition of the entire region as opposed to specific points. The EDS map shows that gold metal did indeed move through the voids at the corner of the gate metal and down onto the semiconductor surface, and the other metals diffused upwards. Furthermore, the EDS map indicates that Gallium diffused away from the gate metal during the stress from the reliability test.

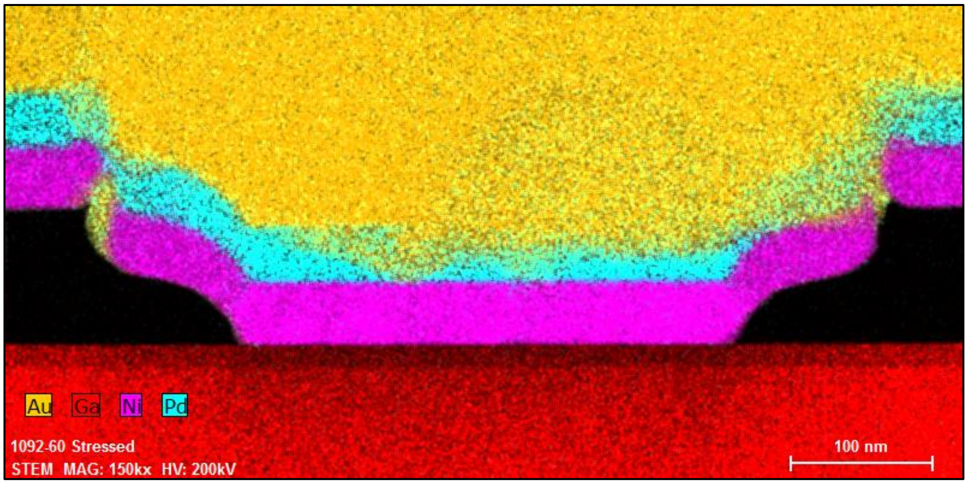


Figure 4.6: EDS map of the STEM foil that was taken from device E. The EDS map shows that gold diffused through voids to the semiconductor surface.

The diffusion of gold metal along the gate stem was determined to be the cause of the Schottky degradation of the gate metal; a study by Chen et al. showed how the diffusion of gold along the gate stem degrades the Schottky contact[15]. This Schottky degradation resulted in the device to fail for an extremely negative imbalance current, as well as exhibit a very negative reverse leakage in the gate-source diode sweep. The device's very negative imbalance current is considered to be gate dominated and could result in a shorter lifetime for the device and could cause the device to fail in the field if it is not screened early. By screening this device and determining the cause of failure future devices will benefit because they will not show a similar failure mode. This increases device quality and reduces costs incurred if a device like this one was to fail on the customer's end.

4.3 Gate-Source Diode Failures

A failure of the gate-source diode sweep points to a gate that is shorted to the source and shows no rectifying behavior. A failure of such a test is not generally explored when the tested device is on wafer; because this failure is highly catastrophic and is accompanied by a burn mark on the device which would visually obscure anything of interest. However, when a packaged device fails for the gate-source diode, failure analysis is done to determine if it failed because of a fabrication issue or a packaging issue.

4.3.1 Crushed Air Bridge During Assembly

Device F is a packaged device that is mature and does very well in its DC and reliability tests. Device F is a packaged device that consists of two GaN on Si FETs and some capacitors. However, a group of these devices failed all of the DC tests that it was put through, with the first test in the suite being the gate-source diode check. The gate-source diode sweep for device F is shown in Figure 4.7. The graph shows that the gate is shorted to the source somewhere on the device since the gate current is at compliance in both the forward and backward portions of the sweep. Furthermore, the graph shows no rectifying behavior that is expected of a diode and shows a more resistor like characteristics.

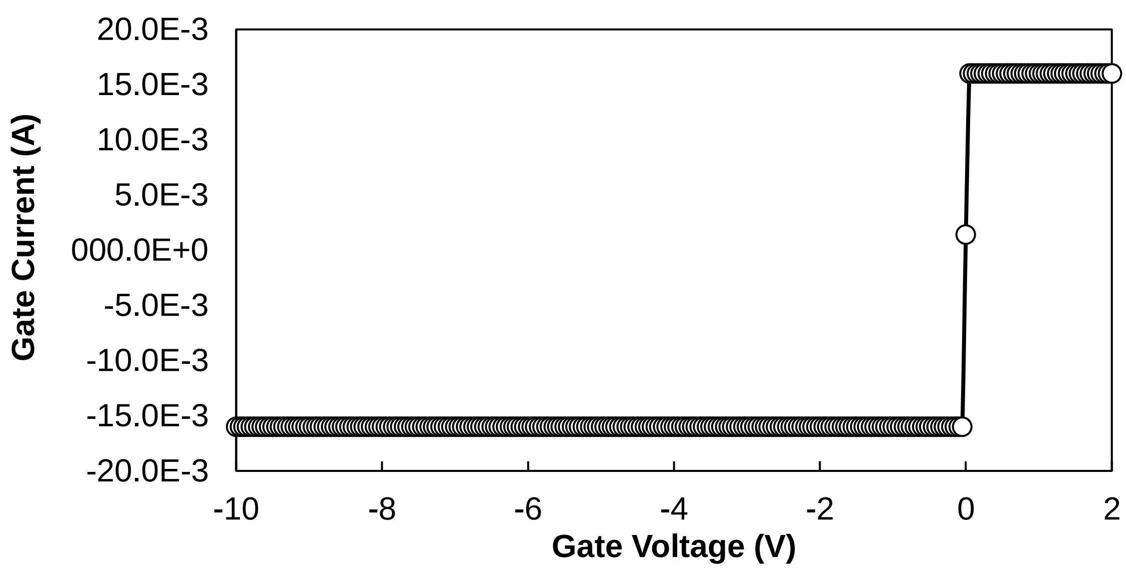


Figure 4.7: Gate-source diode sweep for device F which shows no rectifying behavior and therefore, no characteristics of a diode.

The resistor like characteristics of the gate-source diode curve is the symptom for why this device failed. A resistor like curve means that there is a short between the gate and the source of the device. A short between the gate and the source would make it impossible for the device to function. The device would never be able to pinch off the channel and would constantly be conducting current. This would be disastrous if delivered to a customer and it is necessary for it to be screened early. Failure analysis for failures of this type is not often needed; however, since this technology is mature and performs well and since it was a large group that all failed for the same test, failure analysis was performed.

The first step in failure analysis is to remove the lid of the device and inspect it with a high magnification optical microscope. The devices are coated in a very thick layer of gel coat which obscures the image in areas. An optical image of the entire device after the lid was removed is shown in Figure 4.8. The two FETs and all of the capacitors are clearly seen. None of the wire bonds seem to be touching one another and nothing can be seen that would cause a short between the gate and the source of the devices. A closer inspection of the FETs themselves is needed to determine the root cause of failure.

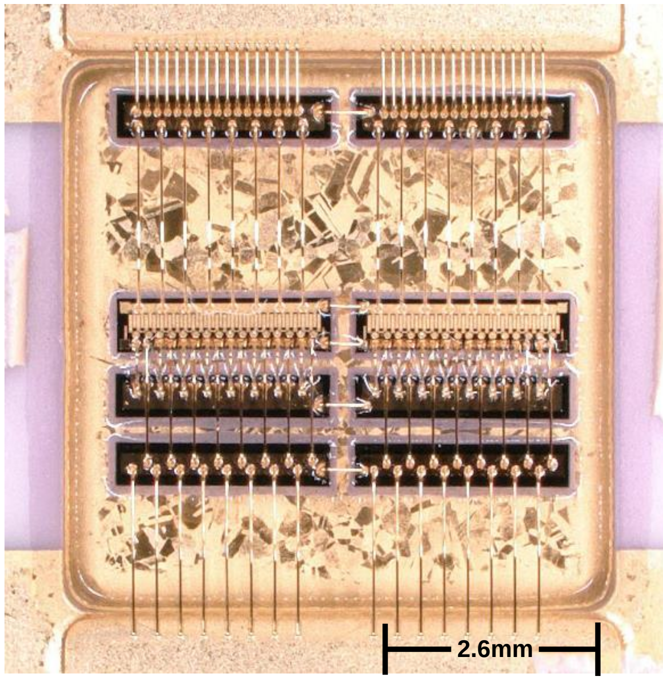


Figure 4.8: Optical image of the entirety of device F after the lid was removed. Two FETs and 6 capacitors are clearly visible, but a short between the gate and source cannot be seen on this image.

As previously stated, a closer inspection of the devices themselves was needed to determine how the gate had shorted to the source. Images of the right and left transistors are shown in Figure 4.9 respectively. These images have an extreme amount of distortion due to the gel coat refracting the light from the microscope.

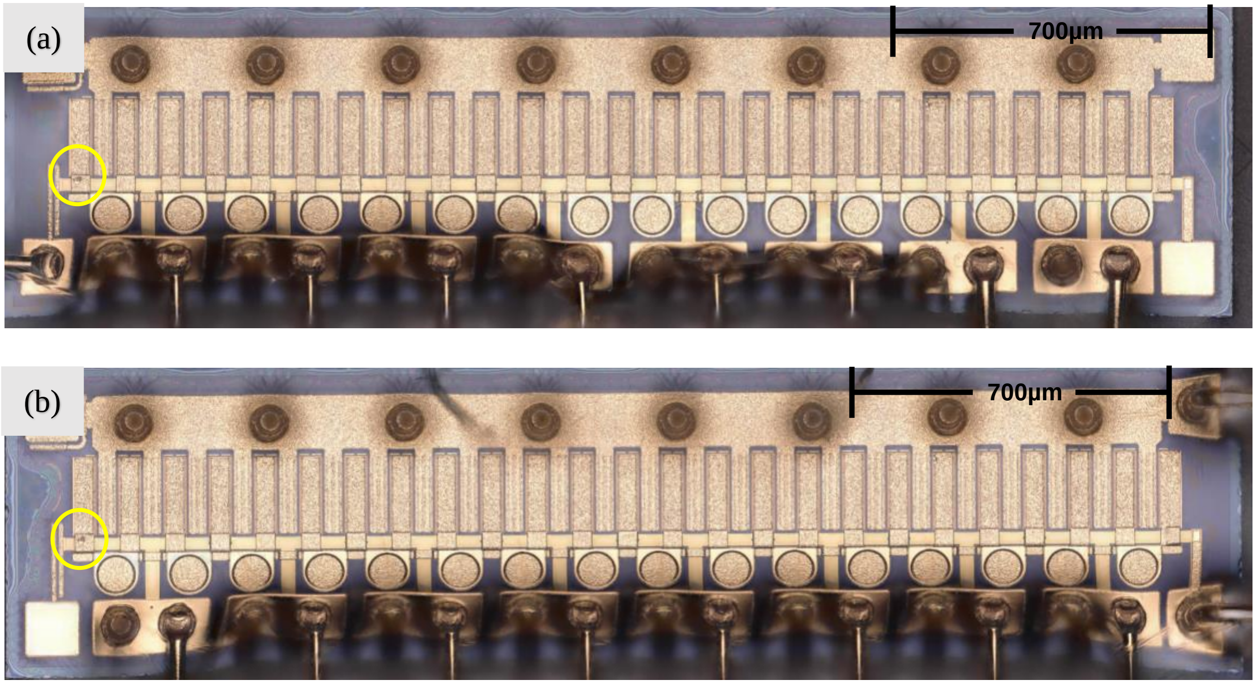


Figure 4.9: High magnification image of the FET on (a) the right side of device F, and (b) the left side of device F. Yellow circles indicate the air bridge of interest that shows a defect on its surface.

A defect on the surface of both transistors is seen on the first airbridge from the left. A closer look at each air bridge is shown in Figure 4.10. The surface defect is a mark from something hitting and crushing the air bridge during assembly. This crushed air bridge shorts the gate and the source and is the ultimate cause of failure for this device.

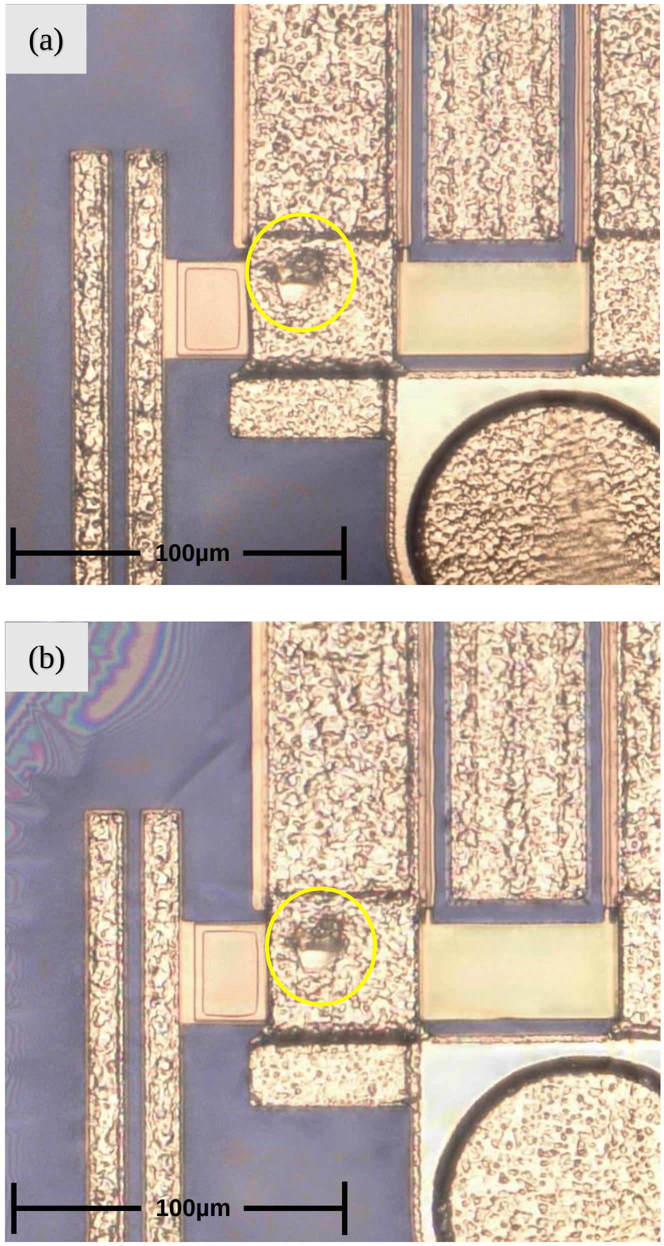


Figure 4.10: Surface defect on the air bridge of (a) the right FET on device F, and (b) the left FET on device F. These defects, identified by yellow circles, are crushed air bridges that are shorting the gate and source.

The root cause of failure for device F was an air bridge that was crushed during assembly and shorted the gate metal to the source metal. This could have happened when a tool was misaligned and accidently pressed down on the airbridge. An inspection of all the other devices that failed in a similar manner showed that they all had crushed air bridges. The symptom for this failure was failing the gate-source diode and having a resistor-like curve. A resistor-like curve is indicative of a short between the gate and source, which was found to be the cause of failure by high magnification optical microscopy.

4.3.2 Migration of Silver Shorting the Gate and Source

The last packaged device that was tested was device G. Device G is a 2mm channel periphery 0.25μm gate length GaN on Si RF device. This device was put through a Highly Accelerated Stress Tests (HAST) reliability test and was considered a "hard fail" since it failed every test but the imbalance screen. The reason device G failed every DC test was because it failed the gate source diode sweep. The gate-source diode sweep for this device I shown in Figure 4.11. The device was at compliance in the reverse part of the graph, which is considered a failure. Also, the sweep shows that this device has a short between the gate and source because the curve looks like a resistor instead of the expected diode characteristic.

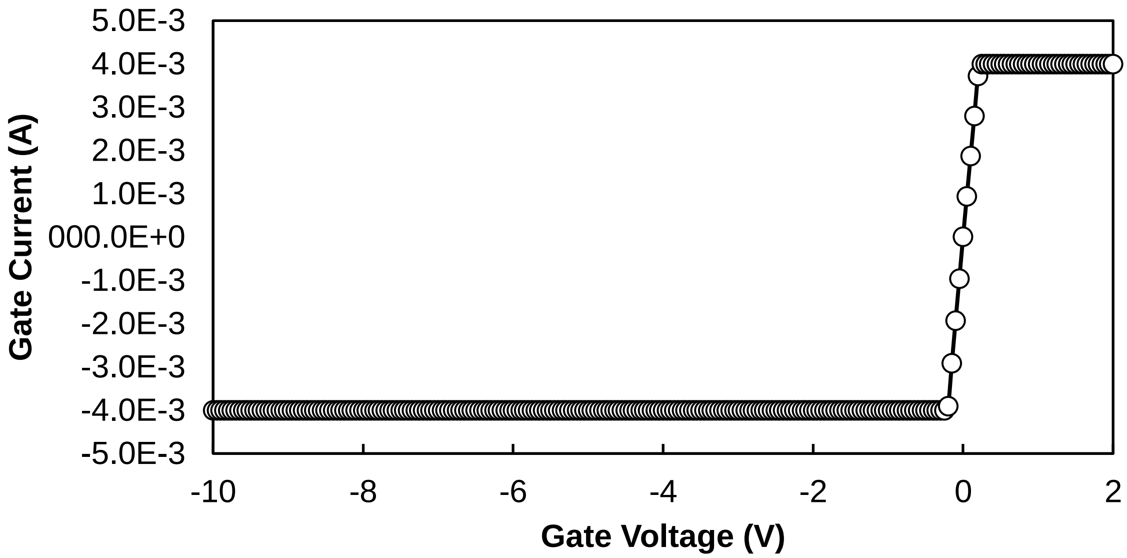


Figure 4.11: Gate-source diode sweep for device G. The device failed this test because it reached compliance in the reverse area of the graph.

The failure of the gate-source diode sweep is the symptom for this device. As previously stated, the sweep suggests that there is a sort between the gate and source of device G. This short means that the gate will never be able to pinch off the channel of the device so it will always be on. This is not beneficial at all and results in the transistor being completely useless since the channel cannot be controlled. This device failed the reliability test and was screened out early so there is no way it could be sent to a customer.

The first step in the failure analysis for this device is to remove the lid and perform an optical inspection using a high-resolution optical microscope. An image of device G is shown in Figure 4.12. The image shows the root cause of failure for this device. The silver epoxy, which is the dark material at the bottom right of the image, that was used to attach the die to the package has migrated during reliability testing and shorted the gate to the package. Silver, when in a humid environment and under the influence of an electric field can ionize, migrate, and redeposit somewhere else on the device[16]. Since the backside contact of the die is the source contact, the gate is shorted to the source through the package.

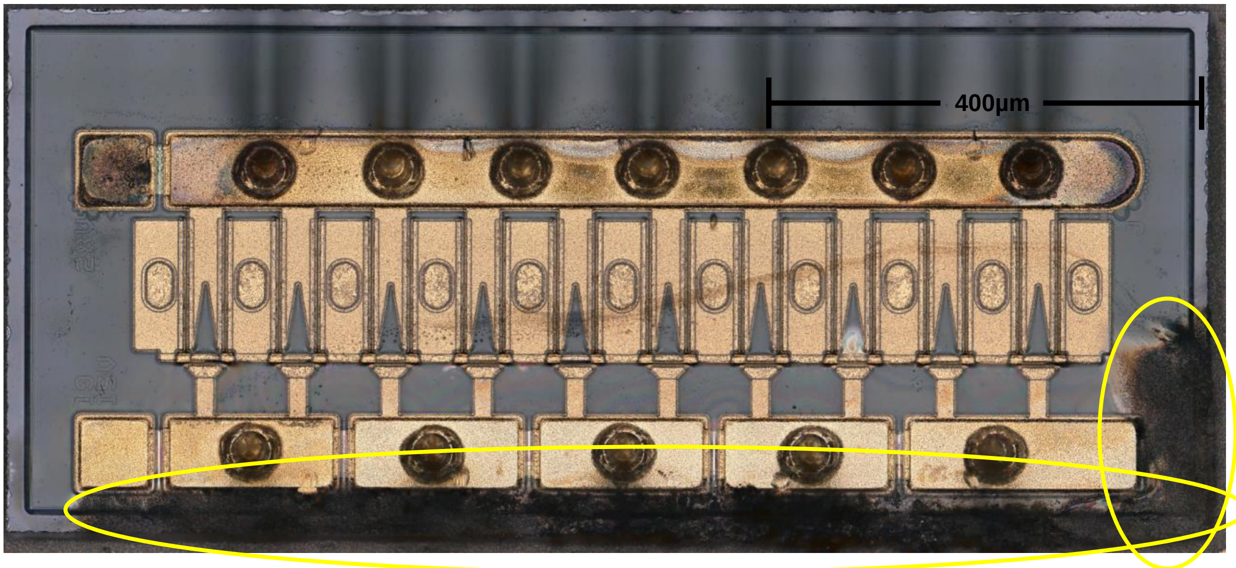


Figure 4.12: Optical image of device G showing Ag migration, identified by yellow circles, to be the cause of the gate to source short.

In conclusion, device G failed reliability testing for every parameter besides imbalance current. The main symptom for the device was the fact that it failed the gate-source diode sweep. A failure of the gate to source diode sweep suggests that there is a short between the two contacts. This was proven after removing the lid of the device and taking an optical image. The image showed that the silver epoxy that was used to attach the die to the package had migrated and shorted the source to the gate.

4.4 Conclusion

In conclusion, three different packaged devices failed their respective reliability screen and were subjected to failure analysis to determine what caused the failure. One device failed for an extremely gate dominated imbalance current and the other two failed for the gate-source diode test. An extremely gate dominated imbalance current failure means that the device has very high leakage when it should be off. A negative imbalance suggests that the Schottky barrier between the gate and the semiconductor had degraded in some way causing current to leak to the gate contact. To prove this hypothesis, a series of microscopic and spectroscopic techniques were employed. These techniques showed that gold metal had diffused along the side of the gate stem and to the semiconductor surface degrading the Schottky barrier[15]. The other two devices failed for the gate-source diode test. These devices did not show any rectifying behavior in their graphs. A curve that does not rectify and shows “resistor like” characteristics means that the gate and source are shorted to each other in some way. Optical inspection showed that for device F the cause of failure was an assembly issue that crushed an air bridge and shorted the gate to the source, and for device G optical inspection showed that the silver in the die attach had migrated during testing and shorted the gate and the source. Determining the cause of failure for packaged devices is just as important as determining the cause of failure for devices on wafer. Any mechanism of failure that can be pin-pointed and remedied improves yield and device quality. Improving yield and device quality saves money and improves customer relations.

CHAPTER 5:

Conclusions and Future Work

5.1 Conclusion

In conclusion, GaN is a wide bandgap semiconductor that is ideal for high power and RF applications due to its material properties. AlGaN/GaN HEMTs are commercially produced by several companies and adoption of this technology for next generation wireless communication infrastructure continues to increase. When these HEMTs fail testing in a commercial production environment, failure analysis is performed to determine the root cause of failure. One very important step in failure analysis is the use of electrical characterization, which is a powerful method that is used to help identify manufacturing and processing issues in a failed AlGaN/GaN HEMT.

Chapter 1 was an overview of AlGaN/GaN HEMTs which highlighted the material properties that make GaN a material system well suited from which high power and high frequency electronic devices can be fabricated. GaN is a wide bandgap semiconducting material having an energy gap about 3 times greater than traditional semiconductors such as silicon and GaAs. The wide bandgap allows GaN to operate at higher power than lower bandgap semiconductors. Also, the AlGaN/GaN heterostructure forms a two-dimensional electron gas (2DEG) that allows for high lateral electron mobilities, and the combination of power and frequency response of GaN HEMTs make them good for power amplifier applications. The AlGaN/GaN epitaxial stack is grown using MOCVD and is usually grown on nonnative substrates such as Si or SiC. However, Si offers an advantage in both wafer diameter scalability and wafer cost.

Chapter 2 outlined the different tests that are done during the device fabrication process as well as how to differentiate a good and bad device at each test. The focus of the thesis is in the DC measurements and both the wafer and device characterization tests utilize a suite of DC measurements for characterization. The first test is the gate-source diode test which can be used to identify any shorts between the gate and source as well as the health of the gate Schottky contact. The second test is the gate and drain three terminal leakage tests. These tests monitor the amount of off-state leakage current from the gate and drain contacts. Also, the three terminal leakage tests are used to determine the imbalance current parameter for a device. The imbalance current parameter is the sum of the gate and drain three terminal tests and is a very important parameter when identifying weak or failing devices. Furthermore, imbalance current gives insight into any possible causes of failure for an AlGaN/GaN HEMT. Depending on how the imbalance current parameter changes with changes in bias conditions, one can determine what might be wrong in a failed device. Lastly the pinch off voltage test is a way to monitor how well the gate can control the channel. These tests can be used to help identify a symptom for the cause of failure for any AlGaN/GaN HEMT.

Chapter 3 outlined four separate cases of on-wafer devices that underwent failure analysis. Three of the devices failed for imbalance current. Devices A and B failed for imbalance current that was affected by a change in gate voltage. This was a symptom of an issue with the gate metal that lead to an increase in drain leakage. These symptoms and the cause of failure were confirmed via the use of microscopic, spectroscopic, and destructive failure analysis techniques. Device A failed because of Ni degradation at the gate metal to semiconductor interface, while device B failed due to damaged gate metal caused by a particle obstructing the deposition of metal during fabrication. Device C also failed for imbalance current, but the imbalance current was affected by a change in drain voltage. This is a symptom that there is an issue with the drain metal that causes an increase in drain leakage. The cause of failure for device C was determined to be a vertical leakage path created by an epitaxial pit that was on the surface of the semiconductor and just below the drain contact. Finally, device D failed for a pinch off voltage measurement meaning that the gate was not able to control the channel at a target voltage. The cause of failure for device D was determined to be a small amount if silicon nitride obstructing the gate metal causing the pinch off voltage to be more negative than that of an ideal device. The DC measurements and the symptoms of failure for each device correlated with the root cause of failure for all devices demonstrating how important DC measurements are for use in failure analysis.

Chapter 4 outlined three different cases of failure analysis performed on packaged devices. Device E failed for an imbalance current that was in the negative milliamps range, meaning that the imbalance was gate dominated. A gate dominated imbalance current is a symptom of an issue with the gate metal that causes an increase of gate leakage current. The cause of failure for device E was determined to be a degradation of the gate Schottky contact due to a migration of gold to the metal to semiconductor interface which aligned with the information taken from the DC measurements. Devices F and G both failed for the gate-source diode test which is a symptom for a short between the gate and source contacts. Device F failed because an air bridge was crushed shorting the gate and source together due to mechanical error during packaging. Furthermore, device G failed because silver metal from the silver epoxy used as a die attach migrated shorting the source and gate contacts after being in the presence of an electric field during reliability testing. The root cause of failure for all three devices aligned with the symptom determined through DC testing.

The DC measurements taken on all devices lead to a symptom for failure for any device that failed. With the use of microscopic, spectroscopic, and destructing failure analysis techniques, the root cause of failure for each device was determined. The root cause of failure aligned with the symptoms from DC measurements in all cases demonstrating how powerful DC measurements are when performing failure analysis.

The future work for this project would be to apply these techniques to more failed devices that fail either on wafer or after packaging. Furthermore, imbalance current does not have a one-to-one correlation to failure mode. An imbalance failure gives an idea as to the culprit leading to device failure, but physical failure analysis is still needed to be certain as to the root cause of failure. For instance, there is not yet a way using imbalance current to determine the difference between an obstructed gate metal or a damaged gate metal as both perform similarly during imbalance current measurements. A separate parameter would be needed to differentiate the two failure modes. Further experiments are needed to develop a DC test that can differentiate between these two failure modes. Experiments are also needed to determine a correlation between these DC tests and a devices' RF performance. More tests are needed to determine if performance during RF testing correlates to a specific failure mode. However, imbalance current and other DC measurements are still a very important and powerful tool when performing failure analysis on AlGaN/GaN HEMTs, as it gives insight into the possible failure mode of a filed device.

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