

## ABSTRACT

JIANG, JUNNING. Peripheral Circuits Design of a Double Floating Gate Memory. (Under the direction of Dr. Paul D. Franzon).

Together with the fast development of the semiconductor technologies, storage memory technologies had been going through extremely fast changes day-by-day. The volatile and non-volatile memories take up the main part of the contemporary storage memory market shares. Due to the different working states of volatile and non-volatile memories, they are used as main memory and secondary memory respectively. A new storage memory device called double floating gate FET has the potential of functioning as volatile and non-volatile devices simultaneously. It may change the storage memory market by combining volatile and non-volatile devices into one device. In the future, a new storage memory chip functions as volatile and non-volatile devices will replace traditional storage memory chips like DRAM and flash memory.

The working mechanisms of the double floating gate FET is similar to traditional flash memory, so it's important to control the changings of threshold voltages of this device. Based on previous work of building double floating gate FETs, this thesis focused on building a complete storage memory based on double floating gate FETs. This thesis included a SPICE compatible model of double floating gate FET and a complete peripheral circuit. The performances of desired storage memory composed of double floating gate FETs were tested.

Based on the master's thesis of V. Kotipalli, the double floating gate FET is with macro-level and micro-level process variations, which leads to the variations of threshold voltages across the complete storage array. In order to solve this problem, a piece-wise linear write circuit, also called small write circuit, was designed and verified to give accurate

controls over the double floating gate FET. This circuit increased the robustness of reading the value stored in the device and reduced the error rate in face of huge micro-level process variations.

In conclusion, accurate threshold voltage control over the device was developed. The read energy is between 1.03 and 1.63pJ on a four-by-four array and a dynamic write takes 0.7pJ.

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Peripheral Circuits Design of a Double Floating Gate Memory

by  
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## **DEDICATION**

This thesis is dedicated to my parents, professors and friends.

For their understandings and supports.

## **BIOGRAPHY**

Junning Jiang received his Bachelor of Science in School of Information Engineering from Southeast University, Nanjing, China. He was a graduate student of North Carolina State University under Dr. Paul D Franzon's guidance.

## **ACKNOWLEDGMENTS**

First of all, I wish to express my gratitude to Dr. Franzon, for this valuable chance into studying the state-of-art devices and circuits. This work contained his time and concentration into the electrical engineering area.

Secondly, I would like to thank Dr. Neil Di Spigna and Dr. Veena Misra. Their approvals of becoming my master's thesis committee member are important to me. Their experience, suggestions are priceless in this thesis work.

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## CHAPTER 1 INTRODUCTION

This chapter describes the background and motivations of developing the double floating gate and its peripheral circuits. Also a brief outline of latter chapters in this thesis will be presented.

### 1.1 Background and Motivation

In the PhD dissertation of Dr. Daniel Schinke [1], *Computing with Novel Floating Gates*, a universal memory device with volatile and non-volatile working modes was proposed, which was also called double floating gate FET. Floating gate device is the traditional device used in non-volatile memory, which has a stack of control gate and floating gate over the substrate. The double floating gate has a similar stack of two floating gates between the control gate and substrate. This means it has multiple operational modes due to different charge transitions and distributions on its two floating gates. By observing and comparing its threshold voltage with a locally generated reference cell, its operational mode could be decided and the volatile and non-volatile bit stored inside the device could be read out. The double floating gate FET has strong potentials to be applied in “just in time” (JIT) switches, FPGAs and etc. Due to its ability to hibernate when the computer is idle, it’s also applicable for instant-on applications. Dr. Schinke’s dissertation also applied this device into field programmable gate arrays (FPGA). Comparisons were made with state-of-the-art FPGAs on reading speed and directions. Its performance over transistor-based designs was also demonstrated.

Dr. Schinke's work also concentrated on the scalability of decreasing the traditional size of the device from 45nm to 16nm. There are several advantages such as faster speed, less power consumption and denser layout, when 16nm technology is applied to peripheral circuits design. However 16nm technology is with high threshold voltage, e.g. 0.7V, which makes it difficult to design analog circuits with current mirrors in presence of  $V_{dd}$  of 1V. Some low threshold voltage 16nm technology did not have a complete leakage current control mechanism, which can heat up the whole part. Moreover, different doping concentrations has a great impact on the surface potential, which is essential in deciding the tunneling current between different layers like control gate and top floating gate. On the other hand, the designed barrier can maintain and classify the different states. The non-volatile mode of the double floating gate FET has a huge threshold voltage shift from uncharged state. Thus, the decoding strategy in designing peripheral circuits and applying proper voltage envelopes are crucial to decide the functionality of the device, improve performance and reduce power consumption.

## **1.2 Problem Statements and Objectives**

A. Bhattacharyya's work [2] included a sense amplifier and a refresh strategy which requires frequent refreshments and large power consumption. V. Kotipalli's thesis [3] mentioned the macro and micro variations of the double floating gate FET, which would lead to variations in threshold voltage of double floating gate FET and errors during read process.

One main objective is to use 16nm, 45nm, 0.18um technology to build an optimized system with better performances. A better sense amplifier and read strategy is also one of the main

objectives of this work. Another main objective lies in building new circuits and strategies to accurately control the threshold voltage of the double floating gate FET. This greatly reduced the effects of macro and micro variations on system performances.

### **1.3 Thesis Outline**

Chapter 2 gives literature review of current solid-state memories. A brief introduction of structures and operating modes of SRAM, DRAM, flash gate and double floating is shown. The SPICE compatible model based on Schinke's work is discussed in Chapter 3. The double floating gate is modeled using a Verilog-A module and a Predictive Technology Model [6]. Verilog-A model is used to model the threshold voltage variations of double floating gate FET. Chapter 4 touches on the peripheral circuit design of the double floating gate array. A piece-wise linear write circuit is developed to accurately control the threshold shifts among states and drifts due to process variations. The simulation result is analyzed and described in Chapter 5 and a faster and more power hungry topology is verified. In Chapter 6, conclusions and future work for the double floating gate FET are presented.

### **1.4 Contributions**

A complete peripheral circuit of the double floating gate FET array over 16nm, 45nm and 0.18um technologies is designed in this thesis. The performance of the system is improved in comparison with [2]. Although the read and write power consumption increase respectively, a faster and stable system is achieved. Also the increase in refresh period greatly reduces the power consumption for refresh process. Meanwhile fewer power supplies are implemented, i.e. only 1V and power supply for level shifter network are needed. A newly designed sense

amplifier is capable of dealing with small threshold voltage changes. On the other hand, this system has a larger refresh period and less power consumption.

The piece-wise write circuit and strategy is also designed to give accurate control over the threshold voltage of double floating gate FET. By working jointly with the high-resolution sense amplifier and locally generated current references, errors from macro and micro level process variations mentioned in [3] could be reduced in write or read process.

## CHAPTER 2 LITERATURE REVIEW

Basic structures and operation modes of current mainstream volatile and nonvolatile memories are reviewed in this chapter.

### 2.1 Current Solid-State Semiconductor Memory Technologies

Solid-state semiconductor memories are designed to store and handle data efficiently, which take an indispensable part in modern semiconductor market. According to recent survey, they occupy 20-25% of semiconductor market share, which is equivalent to 12-15 billion dollar. This drives universities, research institutes and companies to pay more in building memories with better structures, faster speeds, higher densities and less power consumptions.

Normally, mainstream memories are divided into two categories, volatile and non-volatile. For volatile memories, data is stored on capacitors (DRAM) or states of transistors (SRAM). Without power supply, no transistor can be controlled and capacitors will gradually discharge itself, so the data is lost. As to non-volatile memories, such as the floating gate, charges are absorbed and stored on the floating gate. If there is no power supply, it's also difficult for the charges to go through the barrier to the substrate. Thus the data is maintained. A prevailing application of floating gate is the flash memory used as read-only memory (ROM). Important and reused bits are stored in an ROM of a computer. The next section will present a brief overview of operating modes volatile and non-volatile memories.

### 2.2 Volatile Memories

SRAM and DRAM are two kinds of widely used volatile memories in modern semiconductor technologies. Both of them will lose data when power is off. However, in comparison with

non-volatile memories, volatile memories are faster in read and write process. This property makes them suitable for applications with fast data changes and switches, such as cache and main memories in computers.

### 2.2.1 DRAM

Traditional DRAM is composed of a transistor and a capacitor (CS), shown in figure below.

The transistor acts as switches to access the data stored on the capacitor Cs.

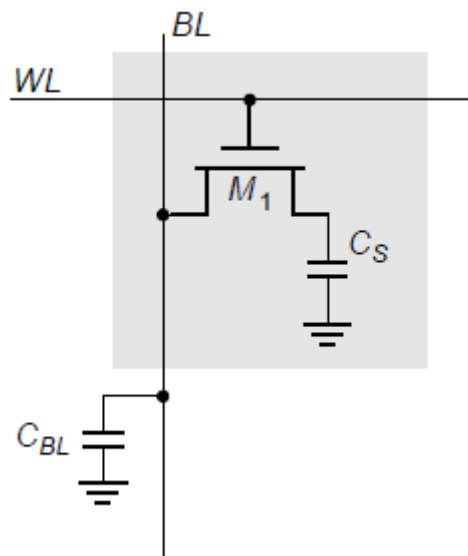


Figure 2-1 Traditional 1T DRAM from [4]

Traditional 1T (one transistor) DRAM is shown in Figure 2-1. In addition to the transistor and capacitor, word line (WL) and bit line (BL) are connected to the gate and drain of the transistor respectively. Also the capacitor on the BL is labeled  $C_{BL}$ . The word line controls

the access to the voltage level stored on the  $C_S$ . Usually the  $C_{BL}$  is smaller than  $C_S$  to reduce the error during read and write process.

In read process, the bit line is pre-charged to certain level, for example,  $V_{dd}/2$ . Then the word line is asserted the  $C_S$  starts to interact with  $C_{BL}$ . If “0” is stored on  $C_S$ , the voltage level on  $C_{BL}$  starts to drop. If “1” is stored on  $C_S$ , the  $C_{BL}$  starts to rise. The change on the voltage level of  $C_{BL}$  could be sensed and amplified by carefully designed sense amplifiers. The sense amplifier is required to be resistant to noise and sensitive to small voltage change. The output of sense amplifier is the value read from the selected DRAM cell. The read process will cause change on the amount of charges on the  $C_S$ . Thus this process is called destructive read. To maintain the correct value on the  $C_S$ , refresh is needed periodically. On the other hand, if one bit line is connected to many DRAM cells,  $C_{BL}$  tends to be large. This requires a more accurate sense amplifier with strong ability to fight against all kinds of noises. The cross-coupled pair is not suitable for the situations here in presence of large noise.

For a write process, the word line is asserted. If “0” needs to be written, the bit line is pulled down to ground and certain time is needed to make sure that  $C_S$  is fully discharged. If “1” is needs to be written, bit line is pulled up to  $V_{dd}$  and it keeps charging  $C_S$  until the voltage on  $C_S$  reaches  $V_{dd}-V_{th}$ . At this point, the transistor is turned off in a second order model. It can be assumed that the write process is finished.

To avoid the destructive read, certain modifications such as the 3T-DRAM, which avoids direct access to  $C_S$  during read process by splitting the shared word line and bit line into word line for read, word line for write, bit line for read and bit line for write respectively.

Due to its high density and low cost per bit in comparison with SRAM, DRAM is mainly used as main memory in computers.

### 2.2.2 SRAM

SRAM usually consists of six transistors (6T) as in Figure 2-2. M2, M4 are PMOS transistors and M1, M3, M5, M6 are NMOS transistors.

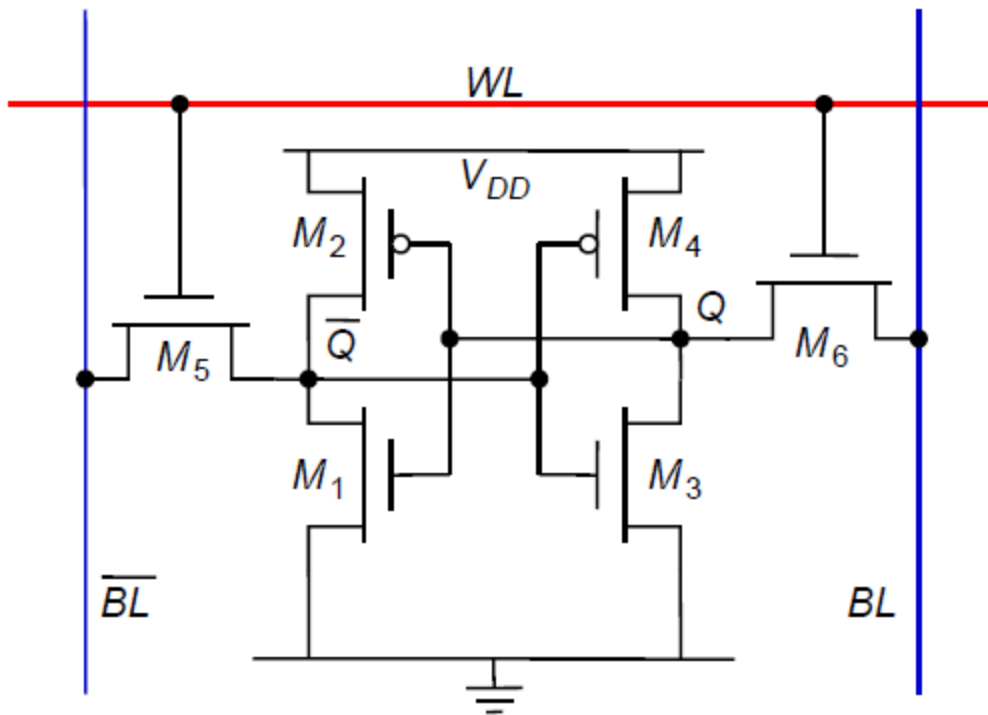


Figure 2-2 6T SRAM [4]

M1, M2, M3 and M4 form a loop-forcing latch that it only has two stable states:

$Q=1, \bar{Q}=0$  and  $Q=0, \bar{Q}=1$ . Any intermediate states will be unstable until it reaches any one of the stable states due to the positive feedback in 6T SRAM when all of these transistors are in

linear or saturations region. M5 and M6 are controlled by the write line and with their drains connected to bit line and bit line bar. When the cell is selected for read or write, both of the word line and bit line must be asserted. Similar to DRAM, SRAM also have three working modes: write, read and standby. There are two robust definitions of the cell's abilities: read static noise margin and write static noise margin. These noise margins identify the ability of the cell to maintain the data in standby or read process, to be written (flip the value in Q). It's not easy to keep reading static noise margin during the process of scaling down transistor size and reducing power supply, due to the threshold variation over the transistors.

In standby mode, write line should not be asserted so that the value is not affected by outside voltage envelopes. In read mode, both the bit line and bit line bar are precharged to  $V_{dd}$ . After finishing precharging, word line is asserted. If "1" is stored in Q, the bit line will remain  $V_{dd}$  voltage. The "0" stored in  $\bar{Q}$  will discharge bit line bar to make sure bit line bar is pulled down. All of these are based on the assumption that  $\bar{Q}$  is pulled down low enough so that it could not turn on M3 to flip the values stored in Q and  $\bar{Q}$ . Usually,  $\bar{Q}$  is assumed to be lower than the threshold voltage of M3. The value of  $\bar{Q}$  is decided upon the size of M5 and M1. Usually the width over length ratio of M1 to M5 should be over certain value to ensure the proper operation of the cell, i.e. M1 is wider than M5.

The write process is quite different from the read process. It needs to flip the value, under the assumption that the data inside the cell is changed. It should have the ability to overcome the original positive feedback loop and build another feedback loop. Suppose "1" is stored in Q, if "0" is required to be written into Q, bit line should be pulled down to ground. M6 will fight

with M4 to pull Q down. If M6 is strong enough to pull Q below the threshold voltage of M1, a successful “0” is written inside. So M6 should be wider than M4, or it has a large width length ratio in order to have a successful write.

In comparison with DRAM, SRAM writes faster and consumes less energy. This means it’s applicable for high throughput applications like cache in a CPU. However, it’s not as dense as a DRAM array.

### **2.3 Non-Volatile Memories**

In contrast to volatile memories, non-volatile memories are capable of storing data when the power supply is removed. According to J. Hutchby and M. Garner’s presentation [11], NAND and NOR flash array are mature on the market. PCM, MRAM and FeRAM are within prototypical demonstration. And other kinds of arrays, for example Nano-Mechm, Polymer including the desired double floating gate FETs are emerging. Phase Change Memory (PCM) exploits the material properties of changing resistivity over structural order. By applying heat, the Chalcogenides could alternate between crystalline and amorphous, which has low and high resistance respectively. Magnetic Tunnel Junction RAM (MRAM) also has alternations among high and low resistance states depending on the polarity of the magnetic layers in between. Ferroelectric RAM (FeRAM) uses the non-volatile electric polarity stored in the ferroelectric layer. This makes it similar to 1T-DRAM structure. Among these devices, only NAND and NOR flash arrays are put into batch production and widely used in the semiconductor market. Dr. Schinke’s PhD dissertation gave a comprehensive comparison table of current non-volatile devices.

Table 2-1 Comparison between the Flash memory and Emerging Nonvolatile Memory Alternatives [1]

Attribute	Flash NOR	Flash NAND	FeRAM	MRAM	PCM
Cell Size	10F <sup>2</sup>	4-5F <sup>2</sup>	15-100F <sup>2</sup>	15-30F <sup>2</sup>	8-20F <sup>2</sup>
Endurance	10 <sup>5-6</sup> cycles	10 <sup>5-6</sup> cycles	10 <sup>8-12</sup> cycles	10 <sup>9-16</sup> cycles	10 <sup>9-12</sup> cycles
Write Time	1μs	200μs/page	30-200ns	10-30ns	10-100ns
Erase Time	1s/sector	2ms/block	30-200ns	30ns	100-120ns
Read Time	20-60ns	60ns/serial	20-80ns	10-30ns	20-100ns
Scalability	Fair	Fair	Poor	Poor	Good
Multi-Bit	Possible	Possible	No	No	Difficult
Cost/Bit	Medium	Low	High	High	Medium
Maturity	High	High	Medium	Medium	Medium
Process	Full custom or +10 masks	Full custom or +10 masks	+2-3 masks back-end process	+4-6 masks back-end process	+2-3 masks back-end process

### 2.3.1 Flash Memory

Dr. Fujio Masuka presented the floating gate at IEDM in 1987 [10]. Its compatibility with current CMOS technology made it very prevailing. Since the double floating gate FET is based on the traditional floating gate, it is worthwhile to introduce the working modes of traditional floating gate.

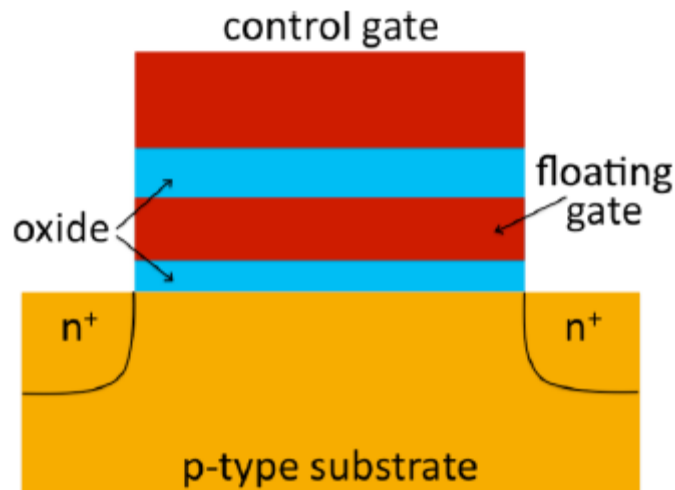


Figure 2-3 Schematic Cross-Section of a Continuous Floating Gate Device [1]

Traditional metal-oxide-semiconductor field-effect-transistor (MOSFET) has a control gate to control the formation of inversion layer to control the “conduction” and “stop” state of the transistor. The oxide between the control gate and the substrate blocks current injection from inversion layer to the gate. Floating gate exploits the similar structure by adding another floating gate between the control gate and substrate. Hence it forms a four-layer stack over the substrate: control gate, blocking oxide, floating gate, and tunneling oxide as illustrated in Figure 2-3. The floating gate is used to store the charges and change the threshold voltage of the transistor. The oxides between control gate, floating gate and control gate are called blocking oxide and tunneling oxide respectively. To write “0” in the device, a high programming voltage is applied to the control gate to form the inversion layer as in most of the MOSFET devices. Meanwhile, the drain is also applied with a moderate voltage to generate high energy carriers. The high energy carriers can go through the barrier of the

tunneling oxide to the floating gate. This process is called channel hot electron injection (CHEI). Since negative charges injected from inversion layer are stored on the floating gate, the threshold voltage increases comparing with the original state. To write “1” in the device or to erase the device into uncharged state, by applying a high positive voltage on the source or a negative voltage with high amplitude to the control gate, the electrons on the floating are pushed to source or substrate via Fowler-Nordheim (FN) tunneling. The main disadvantage of the flash gate is that the erase process will be applied to the block without being applied to a single device. And the programming and erasing processes are not self-limiting, which means the control over writing envelopes is needed. Certain products use the multi-level cells (MLC) by giving accurate control over the threshold voltage shift. Although non-volatile memory needs a higher voltage envelope compared to volatile memory, it’s less power-consuming and many state-of-the-art solid state drivers (SSD) have benefitted a lot from this.

### **2.3.2 NOR Flash Memory**

Two kinds of mature flash memories dominate the semiconductor market, the NOR flash and NAND flash. NOR flash is more like many devices arrayed in parallel, selecting one device out of the block does not need the cooperation of other devices.

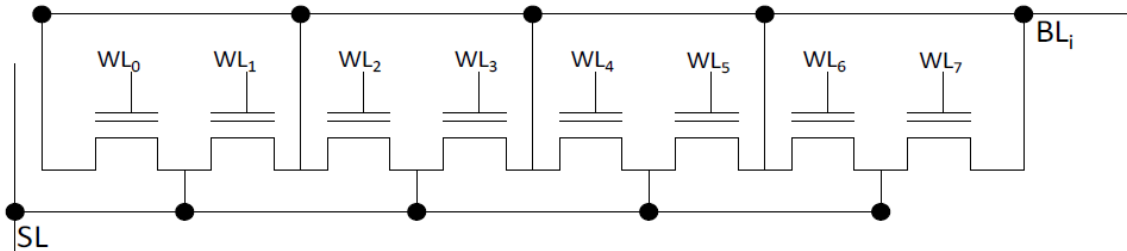


Figure 2-4 NOR Flash Column Schematics

In Figure 2-4, the column of NOR flash shares the same bit line (BL). By applying appropriate voltage envelope to control gate through word line (WL), any data stored inside the device of the column could be read out. The typical programming and erasing process of NOR flash are CHEI and FN tunneling respectively. And each erase process happens within each block of the NOR flash in most commercial NOR flash chips. NOR flash chips usually have a hierarchy to control each device, namely the pages, the block and etc. Since only one device need to be driven to read one bit out, the NOR flash has a faster read speed compared with NAND flash gate. NOR flash memories are widely used to store important system information of embedded applications.

### 2.3.3 NAND Flash

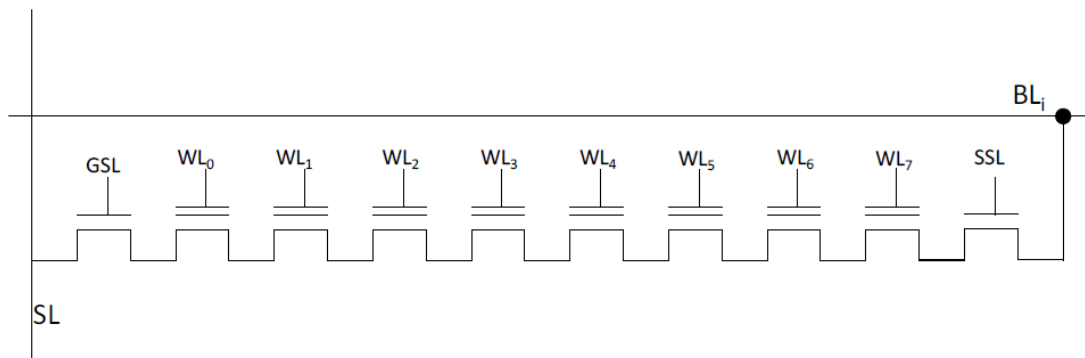


Figure 2-5 NAND Flash Column Schematics

The NAND flash column has several floating gates in series with the source selecting line (SSL) and ground selecting line (GSL) controlling the column. When a specific device is selected, to read its state out, GSL and SSL must be asserted. Also the other devices in a line must be applied with a proper voltage to move into working state, so state of the selected device could be read out by observing the values on the bit line and the output of the sense amplifier. Since the other devices in a column need to be pulled high to read a single device, its read speed is slower than NOR type counterpart. However, only FN tunneling is used in programming and erasing a single device and the NAND flash has a longer life span over NOR flash. Also it has a more compact layout to reduce the cost per bit. All of these make NAND flash suitable for SSD applications.

### 2.4 Double Floating Gate

The 16-nm double floating gate FET (DFGFET) proposed in Dr. Schinke’s PhD dissertation [1] has two floating gates in comparison with traditional single floating gate. The double floating gate FET shown in Figure 2-6 has two floating gates with a back gate.

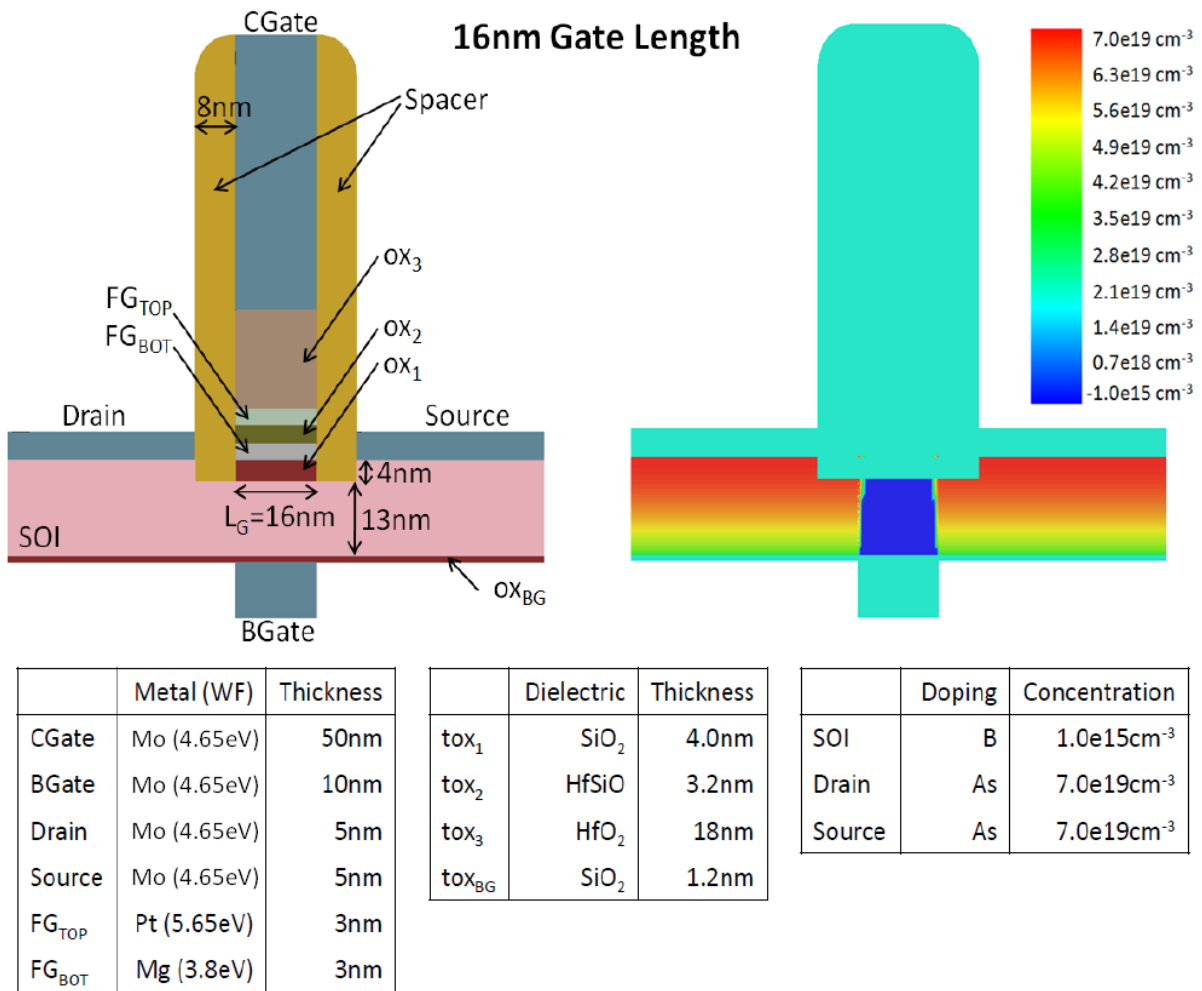


Figure 2-6 Cross-Selection of 16nm Double Floating Gate [1]

The back gate enables multiple selections for voltage envelopes to program and erase the device. Without too many considerations about the reliability of device, the voltage envelope of 7V and -2V applied to control gate and back gate respectively is assumed to be equivalent to 9V and 0V to control gate and back gate. The usage of back gate will help to reduce inter cell interferences.

Among the stack on the substrate, there are three gates: control gate, top floating gate and bottom floating gate. There are also three layers of oxides. Similar to floating gate device, the blocking oxide lies between the control gate and top floating gate, the tunneling oxide lies between substrate and bottom floating gate. The additional oxide decides the tunneling properties between bottom floating gate and top floating gate. In Figure 2-6, the blocking oxide, inter-floating gate and tunneling oxide are  $OX_3$ ,  $OX_2$ , and  $OX_1$  respectively.  $OX_3$  and  $OX_2$  exploit the high- $\kappa$  material  $HfSiO$  and  $HfO_2$  to decrease the size of the device and increase the capacitance among different gates. The thickness of  $OX_3$ ,  $OX_2$ , and  $OX_1$  is 18nm, 3.2nm and 4nm. Silicon on insulator (SOI) is used to reduce the parasitic components and facilitates more accurate control of the device. The SOI is doped with Boron of  $1.0 \times 10^{15} \text{cm}^{-3}$  and Arsenic is used to dope the source and drain with  $7.0 \times 10^{19} \text{cm}^{-3}$ .

The double floating gate FET has similar operating modes as traditional floating gate. It requires voltage envelopes to apply to the control gate and back gate to program and erase. Charges are tunneled and trapped on top floating gate and bottom floating gate. The threshold voltage of double floating gate FET is decided by net charge and distributions of the charge on the top and bottom floating gate. As previously described, double floating gate

FET is called universal memory because it has dynamic and non-volatile modes simultaneously. These two modes are introduced below.

### **2.4.1 Volatile Mode**

When the control gate of double floating gate FET is applied with a positive voltage envelope, which is large enough to redistribute charges among top and bottom floating gates but not strong enough to make large FN tunneling from the substrate to the bottom floating gate, the device works in volatile or dynamic mode. In this thesis, a 65ns of 6.2V voltage envelope is used between the control gate and back gate to achieve dynamic programming. During this process, more negative charges are absorbed onto the top floating gate and more positive charges are pulled onto the bottom floating gate. The net charge on the two floating gates remains nearly constant. Since the bottom floating gate is closer to the substrate, the negative shift of threshold voltage is achieved. After dynamic programming, more current can be conducted through the device when applied with same gate voltage.

When the programming voltage envelope is removed, the charges with opposite polarities on the top and bottom floating gate will recombine to the previous state of the device and the threshold voltage will start to increase. Also to erase the dynamic programming, a negative voltage envelope needs to be applied to the control gate and the back gate to facilitate the recombination of charges to uncharged state. The oxide between the top floating gate and the inter-floating gate oxide prevents the floating gates from leakage. The programming and retention properties are similar to a DRAM cell. The charge stored in one DRAM cell can leak so that a periodic refresh is needed. As in the dynamic working mode of double floating

gate FET, a periodic refresh is also needed to ensure the threshold voltage shift is discernible. In the double floating gate FET, the time length of applying programming voltage is 30ns to 65ns, erase voltage is 20us. The data retention time is nearly 100ms and the data refresh period mainly depends on this. The data refresh period is also dependent on the ability of sense amplifier to distinguish between two small threshold voltage shifts. If the sense amplifier is not able to distinguish between two states with small threshold voltage shift, a smaller refresh period is needed.

#### **2.4.2 Non-Volatile Mode**

The non-volatile mode needs a high positive voltage envelope to be applied to the control gate and the back gate. Usually the voltage and length are 9V and 35 $\mu$ s, which ensures that the charges could tunnel from the substrate through the tunneling oxide to the bottom floating gate. And the programming time depends on devices and applications. The idea of traditional floating gate is applied to double floating gate FET that the tunneled negative charge on the floating gate will make a positive shift of threshold voltage. However, during programming process, most of the negative charges are tunneled to the top floating gate. A wait time of 1s is required to let the charges redistribute among the top and bottom floating gates. A larger positive threshold voltage shift takes place due to more negative charges on the bottom floating gate, which has larger contribution to the shift of threshold voltage.

## **2.5 Applications and Challenges for Double Floating Gate FET**

The most prominent feature of the double floating gate is its ability to carry out volatile and non-volatile programming simultaneously. Consider a computer needs to be switched between idle and working modes, the data stored on the double floating gate FET could alternate between volatile mode and non-volatile mode locally. This greatly saves energy and shortens the read access time. This is also called fast check-pointing, which significantly improves the ability of computers to fight against bit flips due to noise, heat or other undesired cases.

The “just in time” (JIT) network is also proposed in Dr. Schinke’s dissertation. The JIT network only builds paths for the incoming packet and the path will be removed if there is no following packet. The unused path could be switched to non-volatile mode to save energy by double floating gate FET and the desired path uses the volatile mode to ensure fast switching. Although double floating gate FET has many advantages, Dr. Schinke also pointed out some potential challenges. For example, the endurance problems, tradeoffs between dynamic erase speed and refresh rate and layout considerations are within future work.

### CHAPTER 3 SPICE COMPATIBLE MODEL OF FLOATING GATE DEVICES

Figure 3.1 illustrates the SPICE compatible model of the double floating gate FET. The Verilog-A module is designed to model the behavior of the floating gate stack, include control gate, top floating gate, bottom floating gate and the oxides between them.

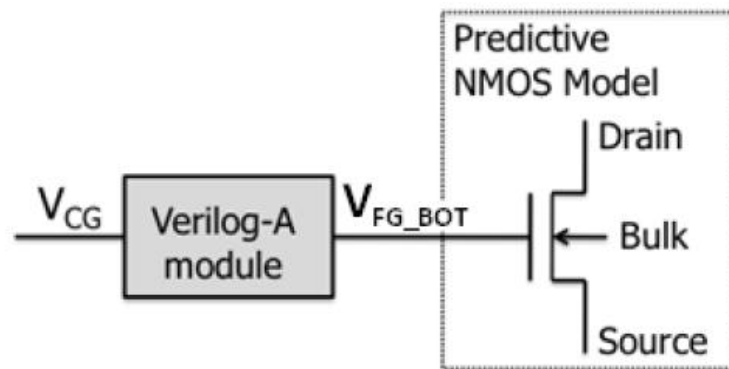


Figure 3.1 SPICE Compatible Physical Model [1]

The Verilog-A module includes the bottom floating gate, top floating gate, control gate, inter-gate oxide and blocking oxide. Schinke assumed the floating gate could only affect the threshold of a traditional MOS device, so the Verilog-A module containing the structure of double floating gate FET was enough to describe the threshold voltage change. Thus this model could be used to describe the behavior of the double floating gate FET.

The bottom of Verilog-A module is connected to the gate of a NMOS to constitute the SPICE compatible physical model. The NMOS used in this model is from Predictive Technology Model [6]. In this thesis, multiple combinations of the voltage envelopes are applied to the control gate. This model could be used to describe the behavior of programming, erasing and

data retention. Also charge leakage and unintended writing are included. The selected Predictive NMOS model has the same oxide thickness with  $t_{ox1}$ . And the charge stored on the bottom and top floating gates are calculated over each time step.

### 3.1 Computing Algorithms

To decide the state of the double floating gate FET, it's important to know the threshold voltage at every time step. So calculating the voltages of the bottom floating gate and the top floating gate is essential.

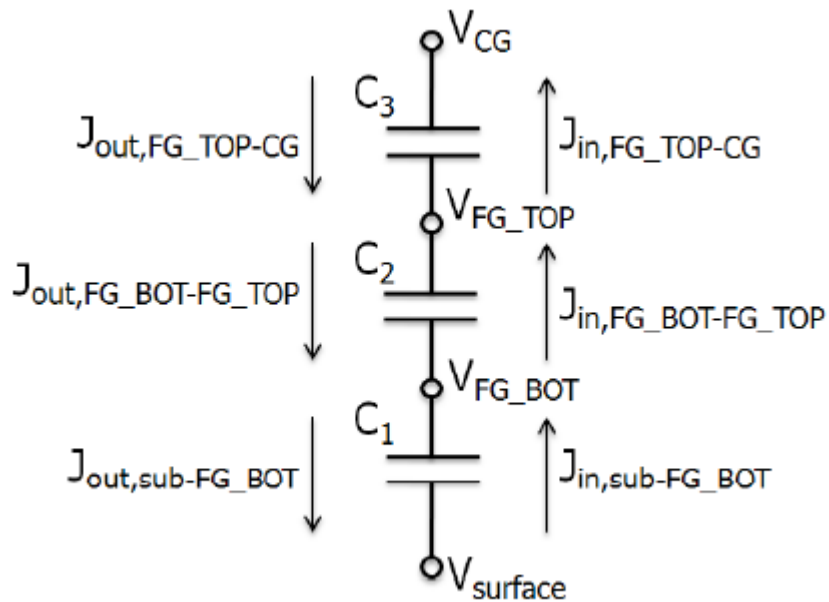


Figure 3.2 Capacitor Model of Double Floating Gate FET [1]

The capacitor model from previous work was used in building the Verilog-A model. To accurately model the internal steps of double floating gate FET, only direct tunneling and FN

tunneling are included. The current density flow over each capacitor is decided by the relationship between voltages applied to the two plates of the capacitors.

$$J_{FGTOP} = J_{out,FG\_TOP-CG} + J_{in,FG\_BOT-FG\_TOP} - J_{in,FG\_TOP-CG} - J_{out,FG\_BOT-FG\_TOP} \quad (3.1)$$

$$J_{FGBOT} = J_{out,FG\_BOT-FG\_TOP} + J_{in,sub-FG\_BOT} - J_{in,FG\_BOT-FG\_TOP} - J_{out,sub-FG\_BOT} \quad (3.2)$$

These current densities only contain FN tunneling and direct tunneling. FN tunneling always exists and direct tunneling is overlooked if the voltage drop between two plates is lower than certain barriers.

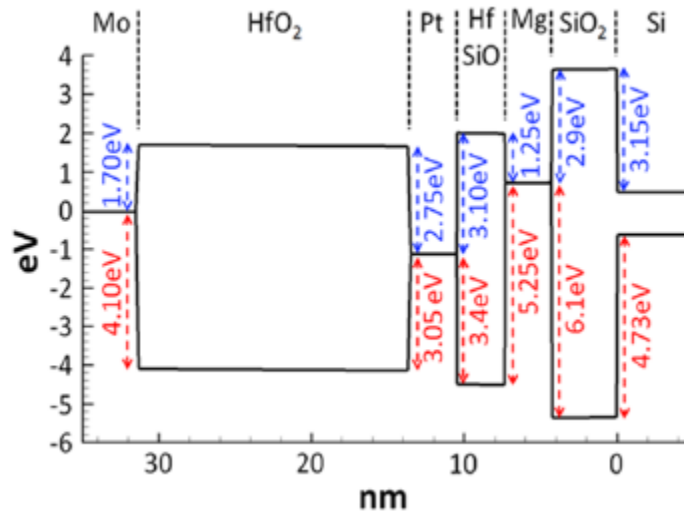


Figure 3.3 Band Diagram of Proposed Gate Stack [1]

Figure 3.3 shows the band diagram of the proposed gate stack when flat-band condition is assumed. For a write process, the control gate is applied with a high voltage, the barrier heights are Pt and HfO<sub>2</sub>, HfSiO and Mg, SiO<sub>2</sub> and Si barriers. Their heights are 2.75 eV, 1.25 eV and 3.15 eV respectively. For an erasing process, Mo and HfO<sub>2</sub>, Pt and HfSiO, Mg and SiO<sub>2</sub> barriers are 1.70 eV, 3.10 eV and 2.9 eV respectively. In our calculation of current

densities, direct tunneling happens when the voltage drop among two plates of a capacitor is lower than the barriers listed above.

### 3.2 Iteration Steps and Results

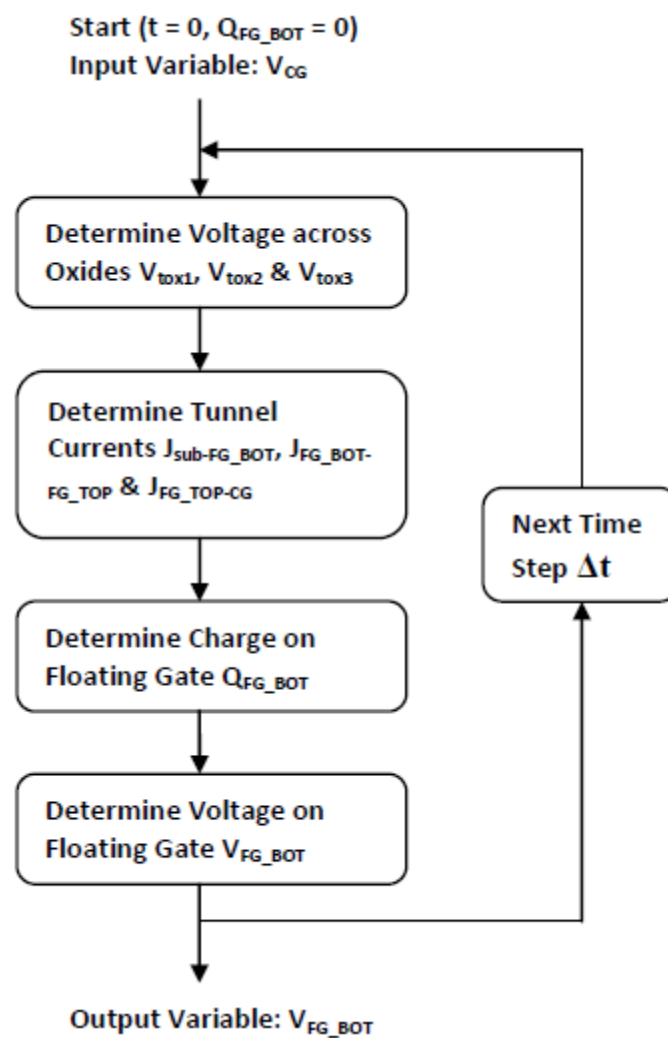


Figure 3.4 Flowchart for Physical Model Computation [1]

In Figure 3-4, the flowchart for calculating the voltage of the bottom floating gate is shown over each step. Four steps are carried out within each time step. First of all, the voltages across each oxide are decided. Secondly, FN and direct tunneling for the four currents are calculated from the voltages derived in first step. On the third, changes of charge on each floating gate are reflected. Finally, the voltage on the bottom and top floating gate are updated for this time step.

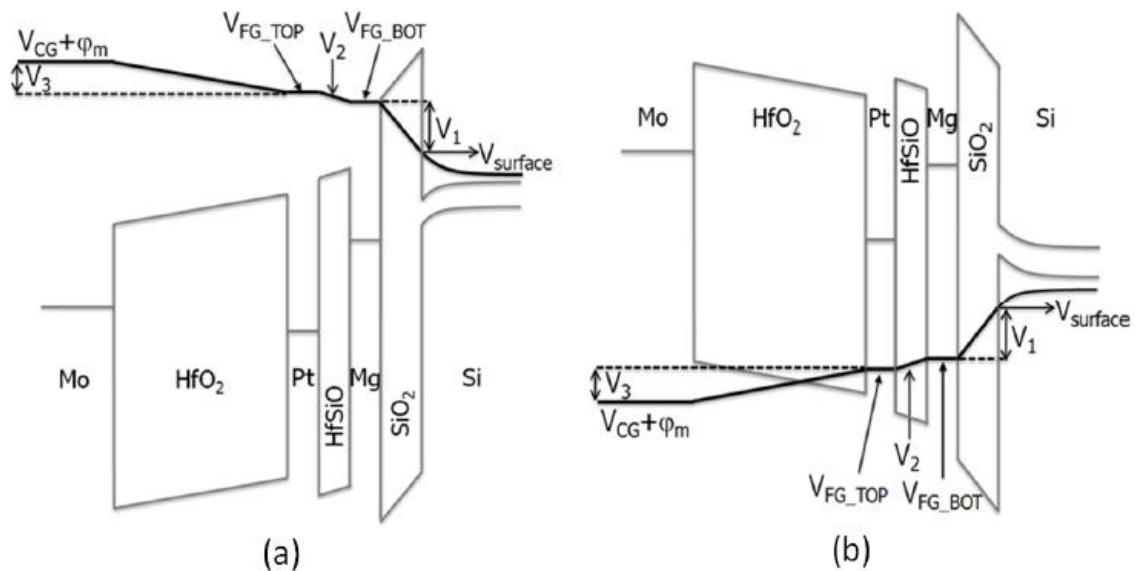


Figure 3.5 Band diagram of universal memory device in (a) program mode, (b) erase mode [1]

The voltage over the  $OX_3$ ,  $OX_2$  and  $OX_1$  are  $V_3$ ,  $V_2$  and  $V_1$  respectively. They are derived from the voltage difference between the oxides as shown in Figure 3.5. Such as  $V_3$  equals  $V_{CG} + \phi_m - V_{FG\_TOP}$ . After each step of calculating the charge changes on each floating gate, the voltages of the bottom and top floating gates are decided.

$$V_{FG\_TOP} = ((V_{CG} + \phi_m)C_3 + V_{FG\_BOT}C_2)/(C_2 + C_3) + Q_{FG\_TOP}/(C_2 + C_3) \quad (3.3)$$

$$V_{FG\_BOT} = (V_{FG\_BOT}C_2 + V_{surface}C_1)/(C_2 + C_1) + Q_{FG\_BOT}/(C_2 + C_1) \quad (3.4)$$

Using equations 3.3 and 3.4, the voltage of the bottom floating gate is decided. Thus the threshold voltage and working mode is decided.

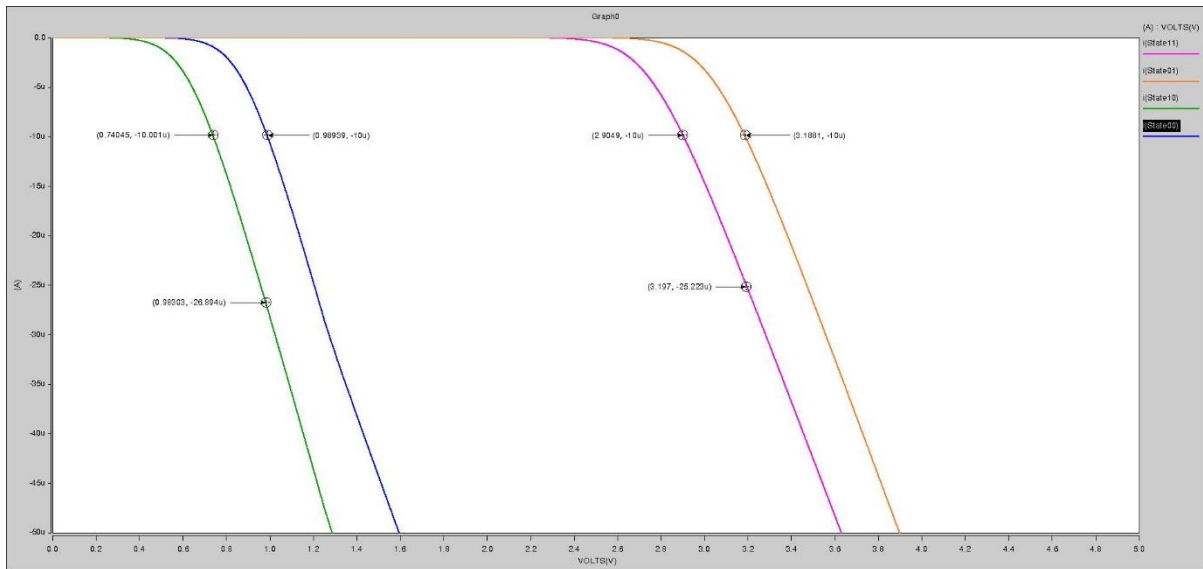


Figure 3.6 I<sub>d</sub>-V<sub>gs</sub> Curve of Four States of double floating gate FET (V<sub>ds</sub> = 1V)

Figure 3-6 is the I<sub>d</sub>-V<sub>g</sub> curve of four states of proposed double floating gate FET based on previous described Verilog-A model. S00, S01, S10 and S11 are the four states of the proposed double floating gate FET. The following table summarizes all the four states:

Table 3-1 Descriptions of Four States of Double Floating Gate

State	Description	$V_{th}$	$V_{th}$ Shift from S00
S00	Uncharged State	0.71V	0.00
S10	Volatile Programmed	0.46V	-0.25V
S01	Non-volatile Programmed	2.61V	1.90V
S11	Volatile and non-volatile programmed	2.36V	1.65V

The threshold voltages of all four states are 460mV, 710mV, 2.36V and 2.61V for S10, S00, S11 and S01 respectively. The threshold shift of non-volatile programming to original state is 1.9V. This value is larger than the previous research results and mainly due to the inaccuracy of the Verilog-A model. However, this does not affect the main body of this thesis, in which building the peripheral circuits of the double floating gate FET array to reach certain functionalities is achieved.

## **CHAPTER 4 PERIPHERAL CIRCUITS DESIGN AND PERFORMANCE OPTIMIZATION**

Based on previous work [2] [3], this thesis improved the performances of the peripheral circuits of the double floating gate FET array. The proposed peripheral circuits can access the memory faster. Also a strategy is developed to give accurate control over the threshold voltage of the double floating gate. This not only reduces the errors and in read processes but also increase the efficiency of the system. Macro and micro variations mentioned in [3] can also be relieved by this strategy.

It's not easy to scale down from 45nm peripheral circuits design into 16nm. The 16nm Predictive Technology Model has a large initial threshold voltage of 0.68V, which is very unsuitable for analog design with power supply of 1V. If current mirror structure is applied using this 16nm Technology, it will be very hard to drive them to work and the slew rate can be very small. However, higher threshold voltage reduces the subthreshold voltage leakage. High threshold 16nm Technology is suitable for digital circuits design due to its faster speed and lower power consumption.

This thesis achieves the “small write circuit”, which has a very accurate control over the threshold voltages of double floating gate FET. It is designed to get over the macro level variations by applying local references and micro level variable by using specially designed sense amplifiers and writing strategies.

#### 4.1 Systematic Diagrams of Double Floating Gate FET Array

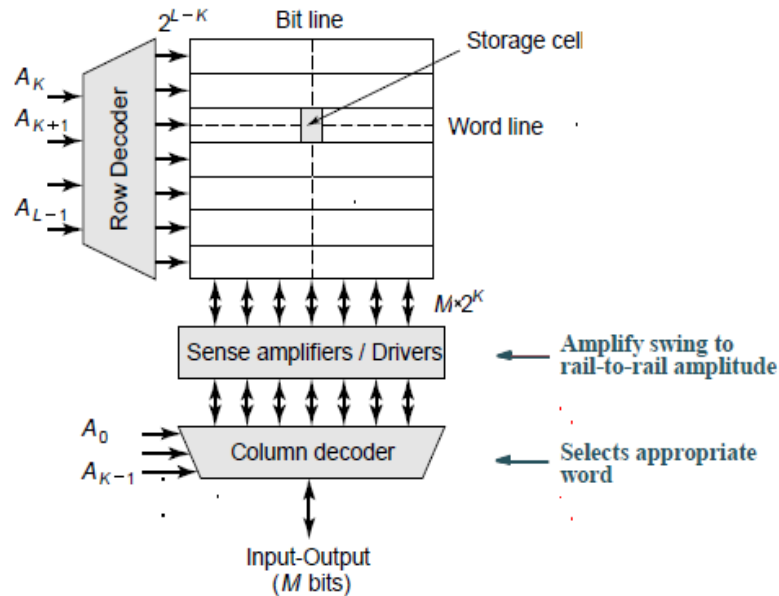


Figure 4.1 Traditional Array-Structured Memory Architecture [4]

The traditional array-structured memory is widely used among SRAM and DRAM arrays. It builds a “standard” template to design peripheral circuits of memories. The row decoder and column decoder jointly select out the desired cell in the memory. The column decoder also connects sense amplifiers for read and drivers for write in this scheme.

When it comes to non-volatile memories like a traditional floating gate array, it’s not easy to solely apply single voltage envelope to the cell to perform read and write. For the double floating gate FET array, the row and column decoder functions a little bit different from traditional decoders in array-structured memory. Since the word line is connected to the gate of double floating gate FET, the column decoder may go through the level shifter network before it accesses the double floating gate FET. The column decoder also needs to drive the

back gate of the double floating gate FET, so a new systematic diagram is proposed, shown in Figure 4.2.

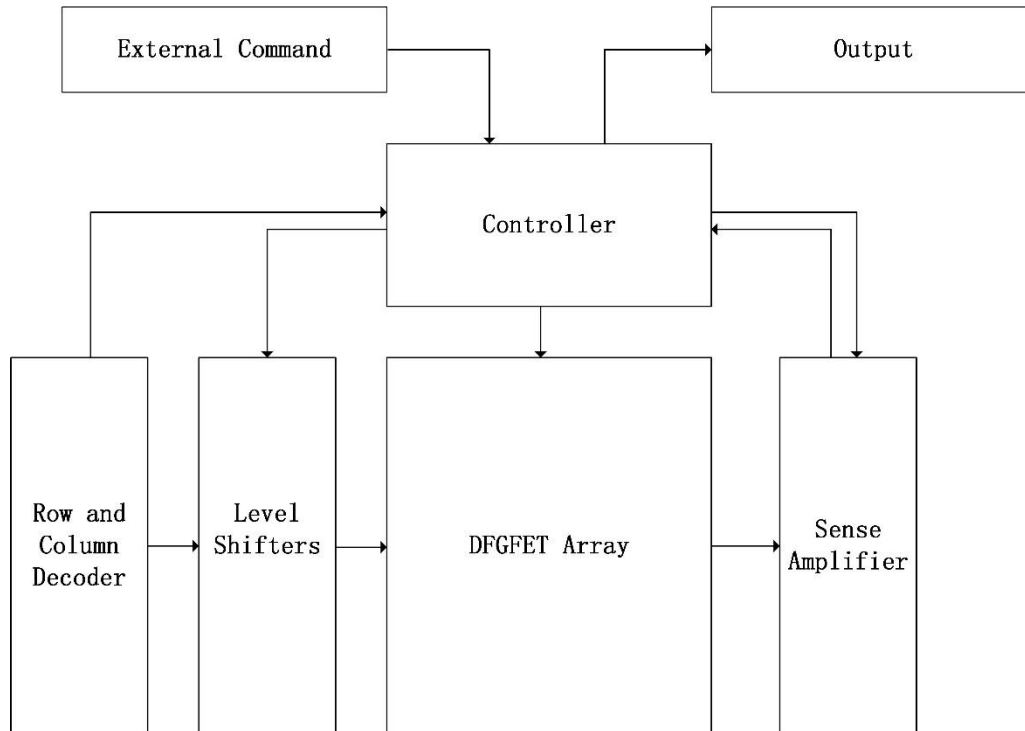


Figure 4.2 Systematic Diagram of double floating gate FET Memory

There is a controller that controls the working status of the double floating gate FET Array. A five stage ring oscillator in the controller can be digitally controlled to generate pulses with width of 5ns. This ring oscillator can be used to drive the level shift network to generate desired voltage envelopes with fixed pulse width. External command could access the controller and let it send out a series of read or write commands. Row and column decoder are receiving the commands from the controller, and going through level shifters to drive the

double floating gate FET array. Both the read and write process need the sense amplifier to sense the output. In read cycle, sense amplifier senses the output of the selected cell. In write cycle, sense amplifier is used to carry out “small write” after huge write voltage envelopes. The sense amplifier can distinguish between very small current changes and amplifies it. So it could be exploited to get very accurate threshold voltage control.

#### 4.2 Row and Column Decoder

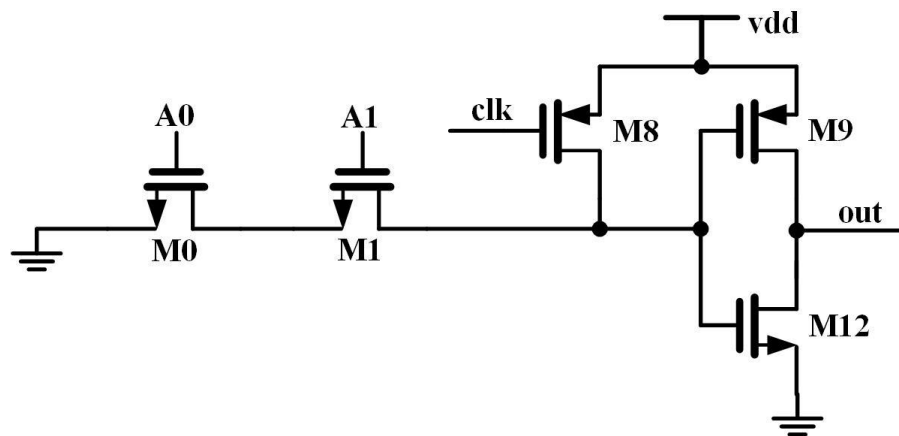


Figure 4.3 2 Bit NAND Decoder

Table 4-1 MOSFET Sizes and Technologies of Two Input Decoder

Name	Size (nm)	Technology
M0, M1, M12	16/16	Predictive Technology Model 16nm NMOS
M8, M9	32/16	Predictive Technology Model 16nm PMOS

Figure 4.3 shows a typical type of 2 input NAND decoder. Since 16nm Technology is used, NAND type is fast enough to satisfy our needs to access the double floating gate FET array. The double floating gate FET array tested in this thesis exploited a NOR type structure. For 16nm technology, NAND type decoder can be switching within nanoseconds and is fast enough to drive the NOR double floating gate FET array. In Figure 4.3, This 2 bit NAND decoder drives the column when A0 and A1 are asserted. During precharge phase, clock (clk) signal turns on M8, which in turn get the drain of M1 charged to  $V_{dd}$ . During decoding phase, M8 is turned off and the drain of M1 is pulled down close to ground and the inverter has a high output to drive the word line. These two phases are controlled by the controller.

For a very large double floating gate FET array with many devices, it will lead to errors if the number of NMOS in series in a NAND decoder is too large. So many NMOS in series will have a huge equivalent RC network Such as in Figure 4.3, if M1 is followed by many NMOSs to the ground on the left side, the RC time constant will be prominently larger than the frequency of the clock signal and the drain of M1 could not discharge completely. Thus the output of the decoder will not have a proper result.

A strategy called pre-decoding scheme which builds a hierarchical level of decoding sequence. For example, A0, A1, A2, A3, A4 and A5 are six bits needed to be decoded. To avoid a long NAND decoder, the six bits are partitioned into two groups. Each group contains three bits, and a 3 bit NAND decoder is used within each group and has 8 outputs. The 8 outputs of each group are combined together by a multiplier to generate 64 outputs, usually NAND s and inverters are used here. Thus the six bit decoding is finished. We could

also apply other strategies like multiple cycles to decode many input bits. However, there is a tradeoff between decoding speed, power consumption and circuitry complexity. The pre-decoding scheme is reconfigurable and easy to implement. It's fit for usage in verification of large double floating gate FET array. In this thesis, a  $4 \times 4$  double floating gate FET array is suggested, so 2 bit NAND decoder is enough. The NAND decoder applies for row and column decoder simultaneously.

### 4.3 Internal Clock Source

An internal clock source is designed to generate pulses of specific width and drive the controller.

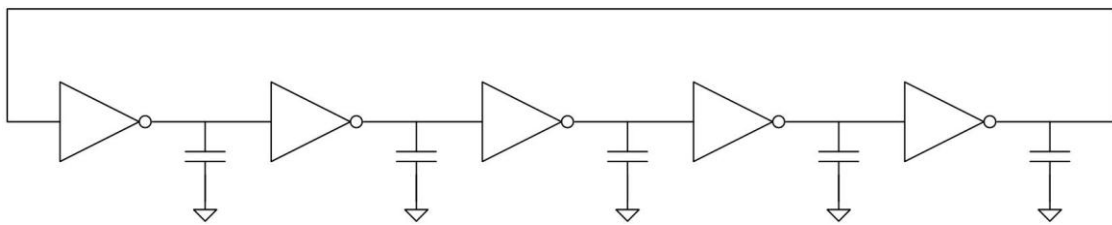


Figure 4.4 5 Stage Ring Oscillator

Figure 4.4 shows a 5 stage ring oscillator. Odd number of inverters in series with output of last stage connected to the input of first stage builds up a positive feedback system. This chain of inverters, also called ring oscillators, has its own advantages. In comparison with cross-coupled pair style, or Colpitts style (positive feedback with single transistor), cross-coupled pair style usually needs on-chip spiral inductor and are much more power hungry. Colpitts style is harder to be driven and also needs an on-chip or off-chip inductor. Although

susceptible to negative-bias temperature instability (NBTI), the ring oscillator consumes less power and is easier to apply.

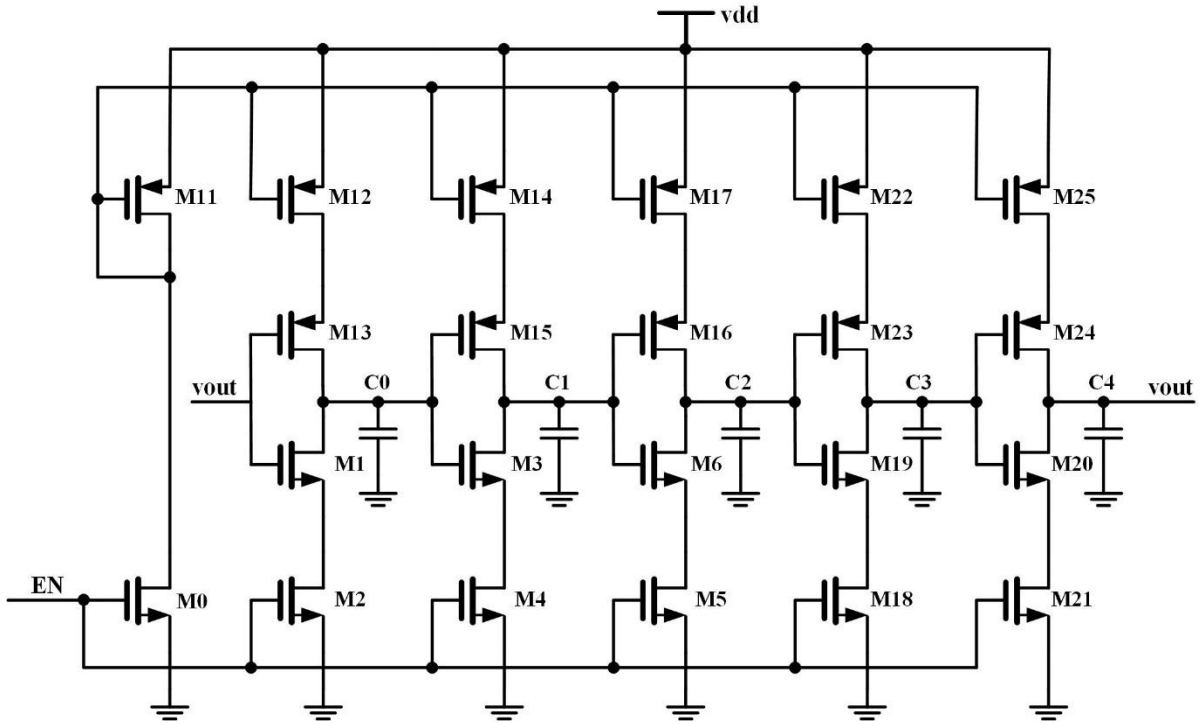


Figure 4.5 Schematic of 5 Stage Ring Oscillator

Table 4-2 MOSFET Sizes and Technologies of VCO

Name	Size (nm)	Technology
M0	90/50	NMOS_VTL of FreePDK45
M11	250/50	PMOS_VTL of FreePDK45
M2, M4, M5, M18, M21	90/50	NMOS_VTL of FreePDK45

Table 4-2 continued

M1, M3, M6, M19, M20	110/50	NMOS_VTL of FreePDK45
M13, M15, M16, M23, M24	222.5/50	PMOS_VTL of FreePDK45
M12, M14, M17, M22, M25	250/50	PMOS_VTL of FreePDK45

The 5 stage ring oscillator is built with an enable control. The oscillation frequency of an N stage ring oscillator is

$$f = 1/(5 \times (t_{pth} + t_{phl}))$$

$t_{plh}$  and  $t_{phl}$  are the propagation delay of an inverter. It's decided by the size, gate voltage and loading capacitor. After tuning, the loading capacitor is chosen to be 50fF and the simulation result is quite close to 200MHz.

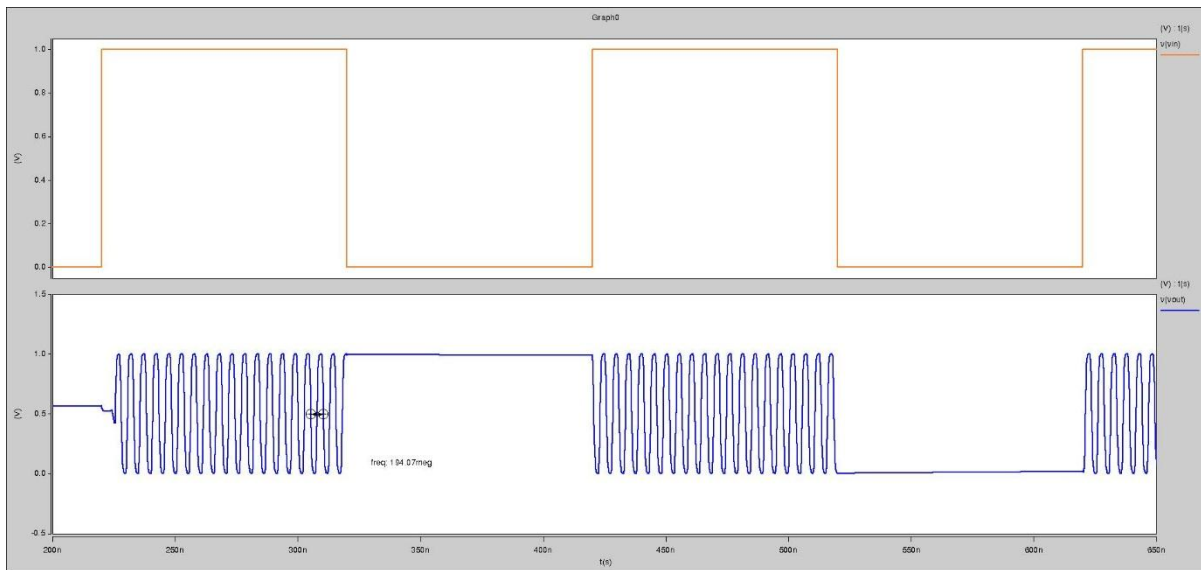


Figure 4.6 Ring Oscillator Simulation Result

It could be seen that when the enable is high, the oscillator starts to work. And it stops working when the enable is pulled down to low. This is more power efficient than a free running clock source.

#### 4.4 Level Shifters

There are many kinds of level shifters, the simplest ones are implemented in this thesis. Almost all the level shifters use cross coupled pair to drive one end to  $V_{dd}$  and another end to ground.

#### 4.4.1 Positive Level Shifter

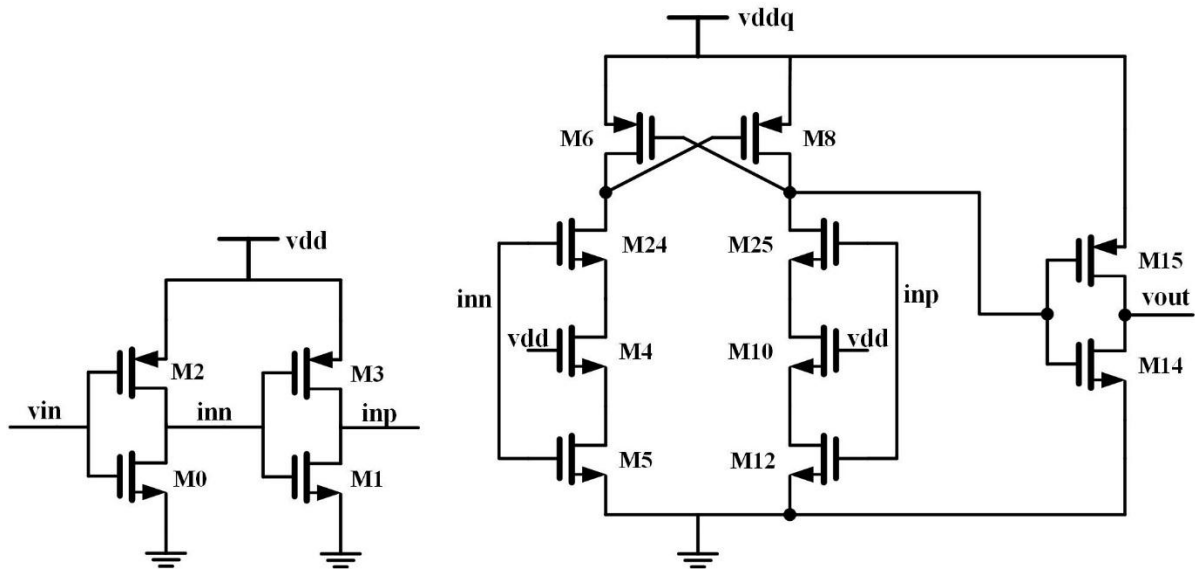


Figure 4.7 Positive Level Shifter

Table 4-3 MOSFET Sizes and Technologies of Positive Level Shifter

Name	Size (nm)	Technology
M0, M1	720/50	NMOS_VTL of FreePDK45
M2, M3	1440/50	PMOS_VTL of FreePDK45
M4, M5, M10, M12	2000/50	NMOS_VTL of FreePDK45
M24, M25	10000/450	Predictive Technology Model 180nm NMOS
M6, M8	2000/450	Predictive Technology Model 180nm PMOS

Table 4-3 continued

M14	1000/450	Predictive Technology Model 180nm NMOS
M15	5000/450	Predictive Technology Model 180nm PMOS

The positive level shifter uses 45nm and 180nm technology. To increase its driving ability, input buffer M0 to M3 are selected wide enough. No zero threshold voltage transistor is used. When  $V_{in}$  is high,  $V_{inp}$  is high. And the gate of M6 and drain of M8 is pulled down. M6 starts work, which further stops M8 to work by pulling up M8 gate to be high.  $V_{O2}$  is low and the output is high. It's the same case when  $V_{in}$  is low. The speed of the positive level shifter mainly depends on the driving ability of the input buffer and the driving ability of the cross coupled pair. It's fast enough to generate a 7V pulse with a delay smaller than 1ns.

#### 4.4.2 Negative Level Shifter

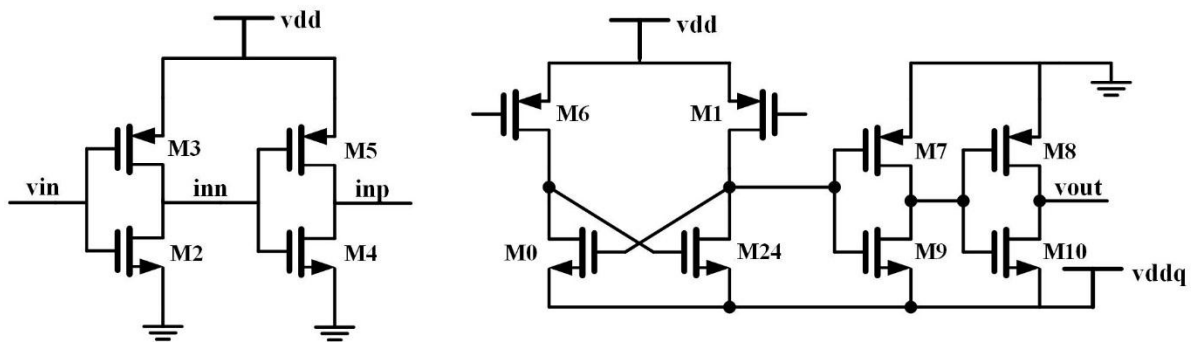


Figure 4.8 Negative Level Shifter

Table 4-4 MOSFET Sizes and Technologies of Negative Level Shifter

Name	Size (nm)	Technology
M2, M4	720/50	NMOS_VTL of FreePDK45
M3, M5	1440/50	PMOS_VTL of FreePDK45
M6, M1	50000/180	Predictive Technology Model 180nm PMOS
M0, M24	10000/450	Predictive Technology Model 180nm NMOS
M9, M10	10000/450	Predictive Technology Model 180nm NMOS
M7, M8	50000/450	Predictive Technology Model 180nm NMOS

Similar to positive level shifter, input buffer is also selected strong. When  $V_{in}$  is high and  $V_{inn}$  is low, M1 starts to pull up B. B is connected to the gate of M0. So M0 is driven to work by pulling  $V_{O2}$  to  $V_{ss}$  (-7V in the schematic).  $V_{out}$  is -7V after a buffer. The negative level shifter also responds quickly and has a delay of less than 1ns.

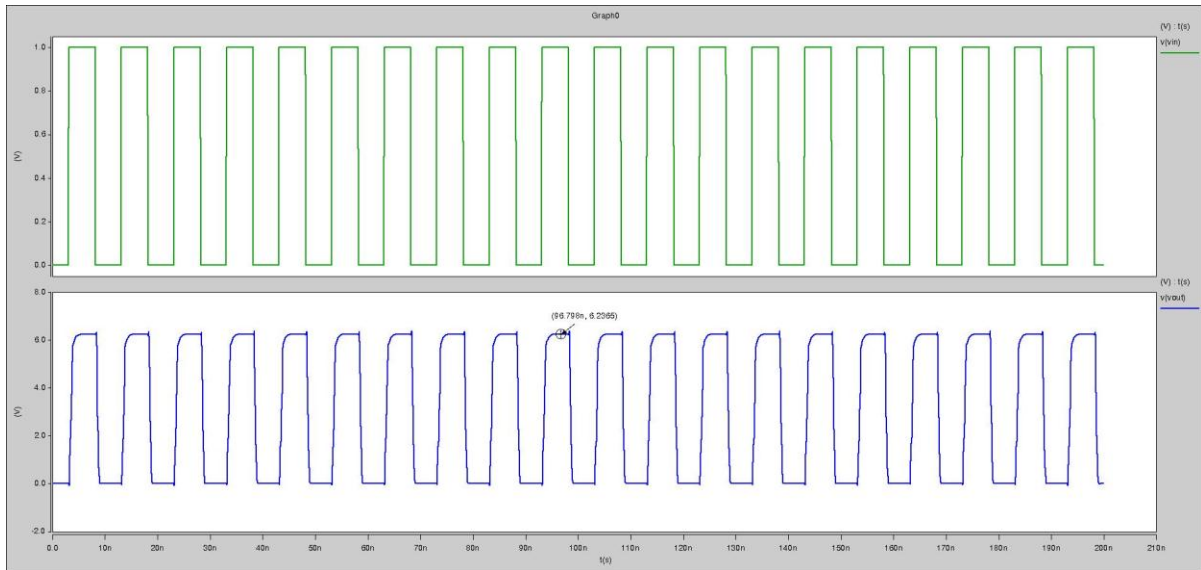


Figure 4.9 Ring Oscillator Driving Positive Level Shifter

Figure 4.9 shows the simulation results of the proposed ring oscillator driving the positive level shifter, which has a high power supply of 6.2V. The 6.2V, 5ns pulse is crucial in building the small write circuit. It shows that the level shifters are very fast.

#### 4.4.3 Multiple Level Shifter Considerations

Since the control gate of double floating gate FET needs to be driven by multiple voltage envelopes, it is nature to consider using multiple levels, i.e. 4.2V, 6.2V, 7V, 9V and -2V to the double floating gate FET array. However, this will lead to driving issues. Consider two identical positive level shifters with  $V_{out}$  connected together, at most one of them works in any moment. If one positive level shifter works, its output buffer needs to drive the pull down NMOS of another shift. One compensation is to increase the pull up ability of the output buffer. However, this will lead to the variation of duty cycle since the propagation delay of

the inverter changes. Another compensation is to increase the supply voltage, like changing the power supply from 6.5V to 7.5V to drive a 4.2V pull down device of the positive level shifter.

Since the proposed level shifters function well among these power supplies, it's suggested to use the controller to control the duty cycle of off-chip boost converter. This is the most power efficient method and the multiple level shifter could be avoided. This increases the design complexity of the controller and requires an accurate time control.

## 4.5 Sense Amplifier

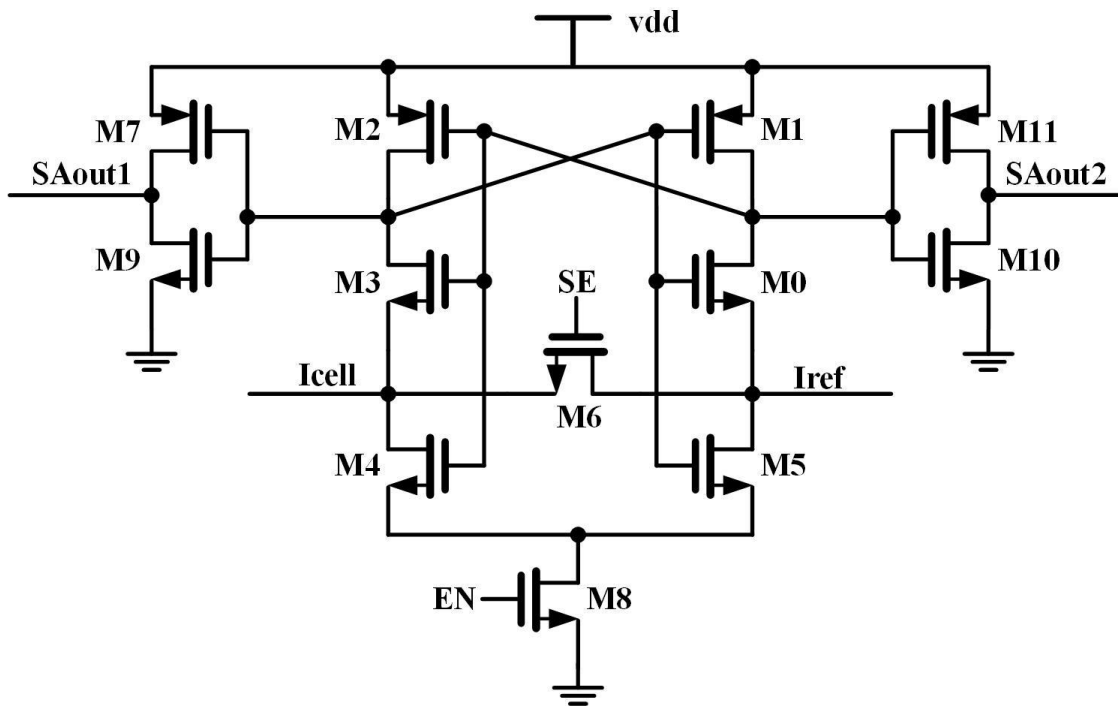


Figure 4.10 Current Mode Sense Amplifier

Table 4-5 MOSFET Sizes and Technologies of Sense Amplifier

Name	Size (nm)	Technology
M0, M3, M6	64/16	Predictive Technology Model 16nm NMOS Low $V_{th}$
M1, M2	128/16	Predictive Technology Model 16nm PMOS Low $V_{th}$
M4, M5	128/16	Predictive Technology Model 16nm NMOS Low $V_{th}$
M8	256/16	Predictive Technology Model 16nm NMOS Low $V_{th}$
M9, M10	32/16	Predictive Technology Model 16nm NMOS Low $V_{th}$
M7, M11	64/16	Predictive Technology Model 16nm PMOS Low $V_{th}$

This is a current mode sense amplifier and is very sensitive to the current gap among two inputs. When SE is enabled to drive the equalizer (M6), the source of M0 and M3 will be pulled low enough to inject current. If  $I_{\text{cell}}$  is larger than  $I_{\text{ref}}$ , the cross-coupled pair will give more drive on M5 to maintain the current balance among the equalizer, thus the sense amplifier has low output on SA<sub>out1</sub> and high output on SA<sub>out2</sub>.

This sense amplifier is sensitive to overshoot thus careful control of the rising and falling time of SE and EN signals is crucial. And its ability to distinguish between small current differences greatly affects the refresh time and design strategy of the double floating gate memory.

## 4.6 Piecewise Linear Write Circuit

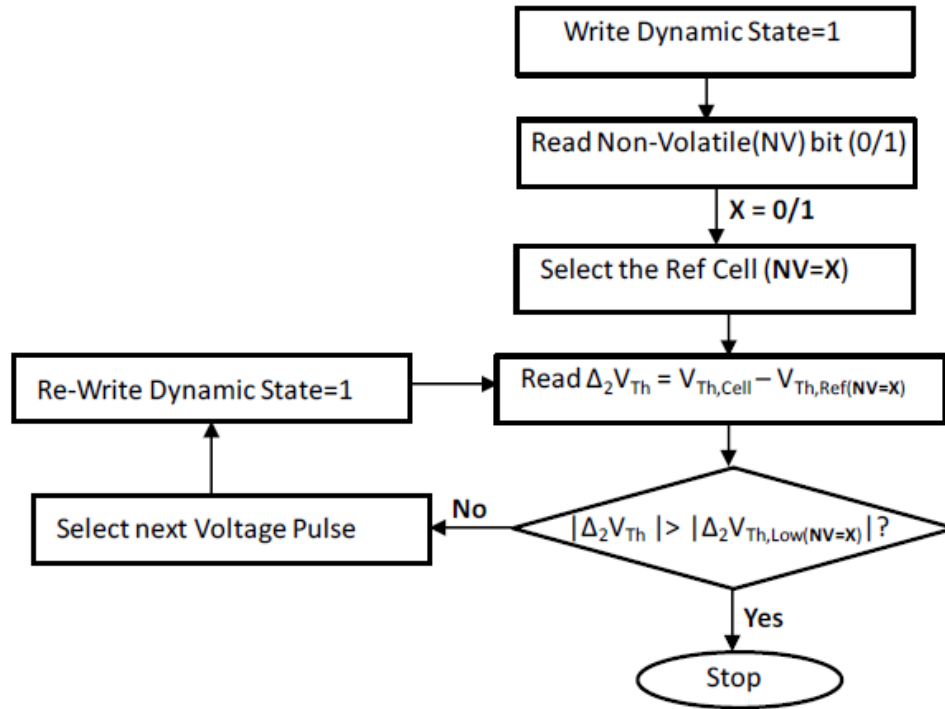


Figure 4.11 Precise Write Algorithm [3]

In Figure 4.11, there is an accurate control algorithm of the threshold voltage [3]. It is required to compare the threshold voltage with a standard cell to decide if the threshold voltage difference satisfies our needs, like 250mV to distinguish the volatile state and uncharged state.

### 4.6.1 Basic Ideas

It's not easy to read out the threshold voltage, since the device may switch among deep linear region, linear region and saturation region. The cell, which is needed to read the data out, is called the target cell. The standard cell is locally selected double floating gate FET, which is



Table 4-6 MOSFET Sizes and Technologies of Piecewise Linear Write Circuit

Name	Size (nm)	Technology
M0, M3, M6	64/16	Predictive Technology Model 16nm NMOS Low $V_{th}$
M1, M2	128/16	Predictive Technology Model 16nm PMOS Low $V_{th}$
M4, M5	128/16	Predictive Technology Model 16nm NMOS Low $V_{th}$
M8	256/16	Predictive Technology Model 16nm NMOS Low $V_{th}$
M9, M10	32/16	Predictive Technology Model 16nm NMOS Low $V_{th}$
M7, M11	64/16	Predictive Technology Model 16nm PMOS Low $V_{th}$
M12, M15, M16, M19	90/50	NMOS_VTL of FreePDK45
M13, M14, M17, M17	90/50	NMOS_VTL of FreePDK45
DFG_1, DFG_Ref	NA	Double Floating Gate FET Model

As in Figure 4.12, if the currents injected into the sense amplifier are pretty close, it can be concluded that the threshold voltage could be defined by the current differences of external current source 1 (CS1) and current source 2 (CS2). The resolution of the bias current decides the accuracy of the piecewise linear write circuit. Thus the threshold voltage shift is transformed into the current difference between two current reference cells.



M4 will remain in triode region after start-up. The out2 is defined by the R0 and their relationship could be found in textbooks and journals.

### 4.6.3 Auxiliary Network in Generating Current

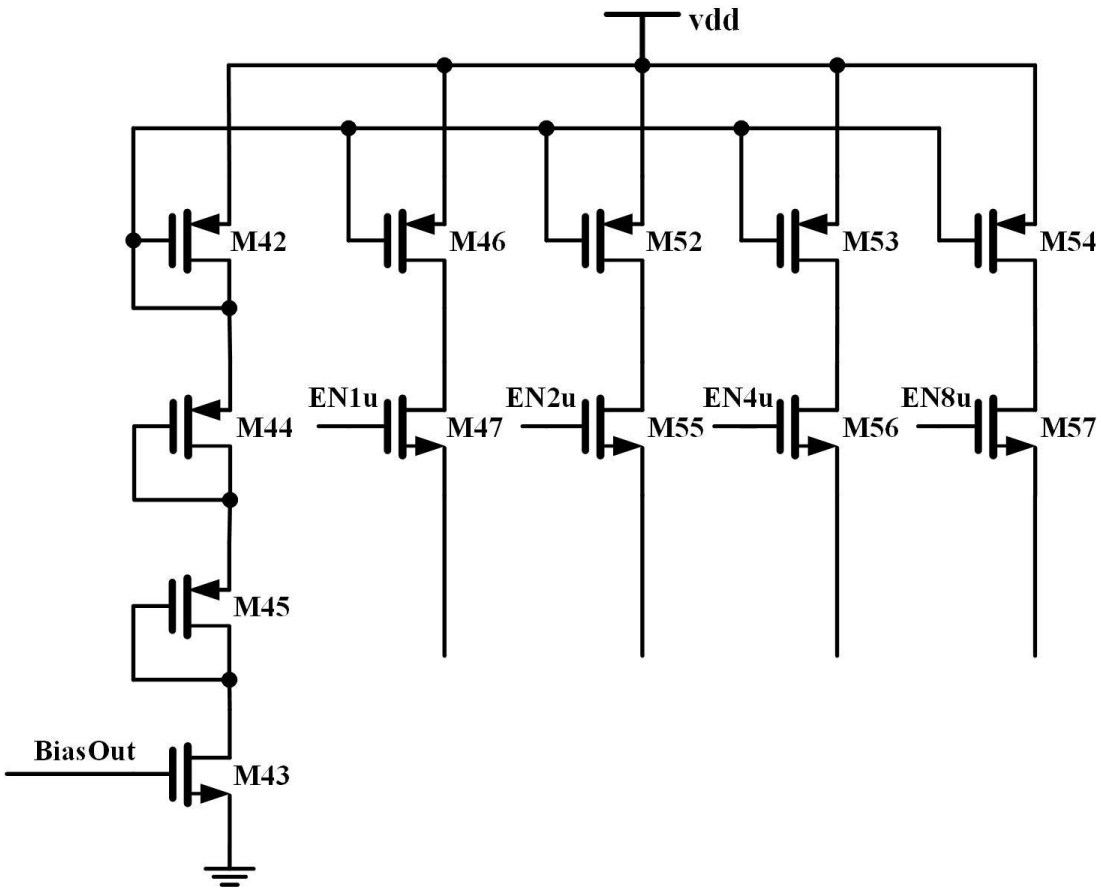


Figure 4.14 Auxiliary Network

Table 4-8 MOSFET Sizes and Technologies of Auxiliary Network

Name	Size (nm)	Technology
M43	90/50	NMOS_VTL of FreePDK45

Table 4-8 continued

M42, M44, M45	90/50	PMOS_VTL of FreePDK45
M45, M55, M56, M57	90/50	NMOS_VTL of FreePDK45
M46	90/50	PMOS_VTL of FreePDK45
M52	180/50	PMOS_VTL of FreePDK45
M53	360/50	PMOS_VTL of FreePDK45
M54	720/50	PMOS_VTL of FreePDK45

The node ConstantGmOut2 is from the Out2 node of Constant Gm Bias. It's nearly 0.6V.

The three triode-connected M45 M44 and M42 are used to define 1uA. Transistors of 45nm and 16nm technologies suffer from the drain induced barriers lowering (DIBL). So the  $V_{ds}$  over the transistor has larger impact over the  $I_{ds}$  than 180nm and other long channel technologies. This network defines 1uA, 2uA, 4uA and 8uA. They can be used to generate from 1uA to 15uA with any values among them and a resolution of 1uA. M47, M55, M56 and M57 are specially chosen NMOS. Not only these four transistor can be controlled by the controller to select desired current, they will also protect M46, M52, M54 and M53 from too large  $V_{ds}$  variations. Thus making the current definitions as accurate as possible is crucial.

#### 4.6.4 Piecewise-Write Demonstration

V. Kotipalli's thesis proposed use of 5ns 6.2V small write envelope to accurate write the threshold voltage of double floating gate FET.

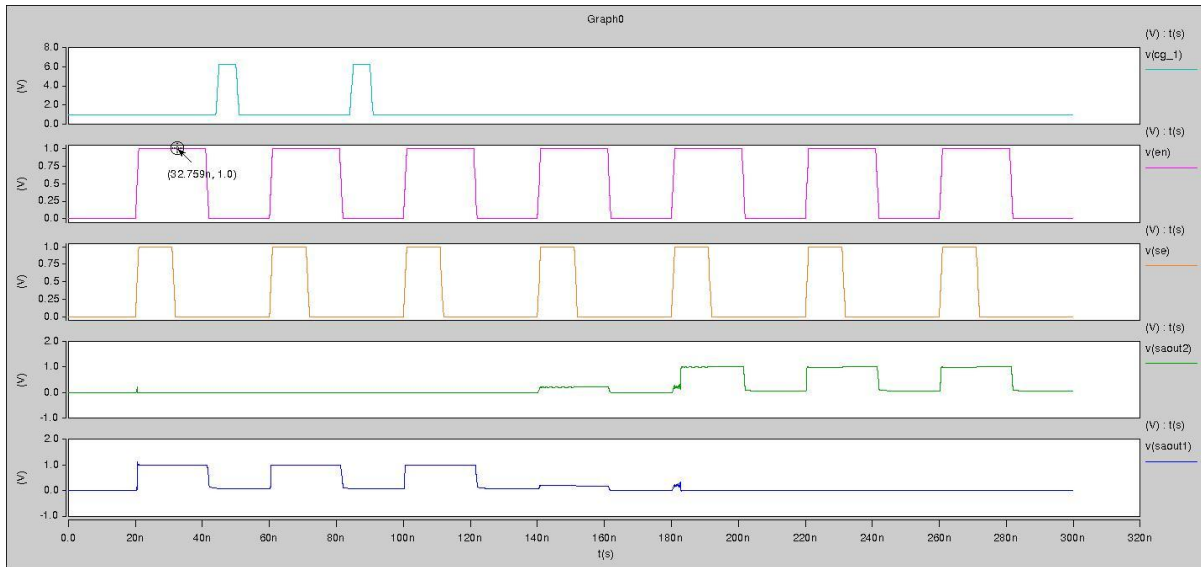


Figure 4.15 Simulation of Piecewise Linear Write Circuit

Due to previous error-and-trail results,  $I_{Bias1}$  and  $I_{Bias2}$  are  $1\mu A$  and  $8\mu A$  respectively. Thus the cell will have threshold voltage of  $-300mV$  when the flip of the output of sense amplifier happens. To demonstrate the piece-wise linear write strategy, an uncharged double floating gate FET is applied  $6.2V$   $60ns$  voltage envelope initially. And two  $6.2V$   $5ns$  envelope is applied between  $40ns$ - $60ns$  and  $80ns$ - $100ns$  respectively. The flip of the sense amplifier is observed. Since the write envelope is so small, the relative error is within controllable range.

#### 4.6.5 Increased Read Noise Margin from Piecewise Linear Write Circuit

It's easy to distinguish between dynamic programmed device and the not programmed device. However, it's easy to make errors in deciding when the device is not programmed. Benefitting from the piecewise linear write circuit, a hard threshold could be added to ensure

the proper read by applying higher current to reference end. If the current from the bias circuit into the reference end is 1uA higher than the cell end, it's more likely the sense amplifier have SAout1 high and SAout2 low. This means the "0" is stored inside the cell. The noise must be large enough to overcome the "1uA" barrier. Many more selections like 2uA, 3uA could also be used. The proper operation to building the 1uA barrier is to inject 2uA to the reference end and 1uA to the cell end. This will keep symmetry of the topology and ensure its accuracy.

#### **4.6.6 Reducing the Micro-Level Variation**

Micro-level variation mentioned in V. Kotipalli's thesis will cause about 47mV threshold voltage shift. Consider a cell with 0.757V threshold voltage and waits to be dynamically programmed. The 6.2V 65nm voltage envelope is applied and it has the threshold voltage shift of 300mV. It's still 77mV from the desired threshold voltage. After applying piecewise linear write circuit, its threshold voltage disparity is defined by the external current sources. If will have threshold voltage close to 380mV or the circuit will not stop programming it. If the cell leaks faster than standard cell, a faster refresh time is need. If the cell leaks slower, another piece-wise linear write will be applied to make sure its threshold voltage is close to zero when the controller want this device to be erased. Thus, the piece-wise write circuit redefines the most important threshold voltage by using external current sources. This achieves the desired small write circuit and makes the programming and erasing devices easier. And over-write can be avoided. The nearly exact control over the threshold voltage is achieved.

#### **4.7 Controller Design**

As discussed in the thesis before, the running of the whole peripheral circuits are controlled by a controller. A finite state machine (FSM) is assumed. It is able of communicating with other chips like MCUs or some others. First, it should be able to generate pulse with modulation (PWM) wave. The PWM wave is used to tune the supply voltage of the positive level shifter and negative level shifter, since the output voltage of a Boost Converter is decided by the duty cycle of the PWM wave.

From Figure 4-15, precise control over the threshold voltage of the double floating gate FET is achieved. Multiple cycles of “small write” can be used to ensure the threshold voltage is close to certain conditions. For a write process, the controller will keep on programming the double floating gate device, until the flip of the output of sense amplifier is achieved. The refresh and erase process is similar to this process, because the essence is to control the threshold voltage.

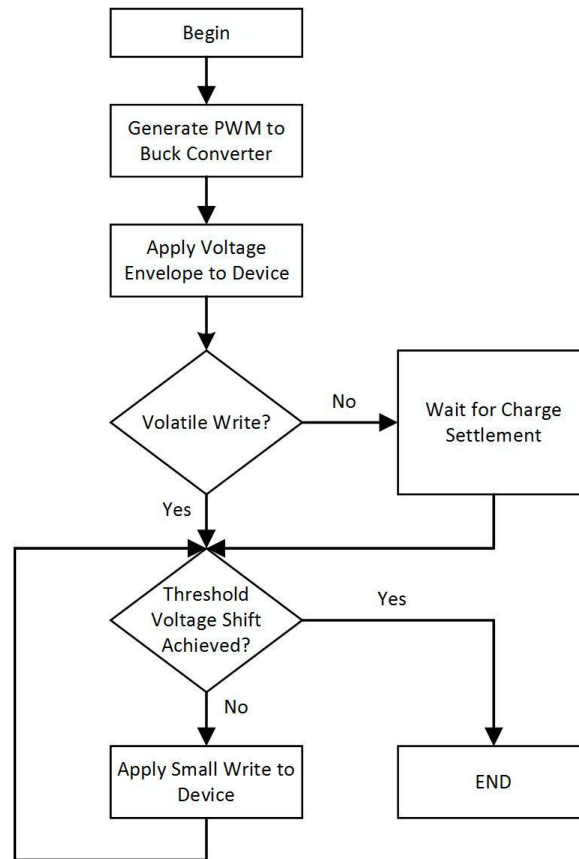


Figure 4.16 Flow Chart of a Write Process



two reference cells are locally selected to get over the macro level process variations. And one of it is not programmed and the other one is non-volatile programmed.

### **5.1 Operations of Double Floating Gate FET Array**

For a read process, at first the non-volatile programmed cell is picked out and applied 1.4V to control gate together with the target cell. If the target cell end has larger current, this means the target cell is not non-volatile programmed. And if the reference cell end has larger current, this means the cell is non-volatile programmed. Here we used the piecewise linear write strategy to overcome the noise. For a non-volatile programmed device, a 3.2V is applied to the control gate to compare with the non-volatile reference cell. For a device without non-volatile programming, 1V is applied to the control gate. There many reading methods and they depend on different circuits. Like the current multi0-level cell (MLC) used in flash memory, there is a tradeoff between accuracy and storage capability. If a single cycle read is preferred for double floating gate FET, 3.0V to the control gate is desired since the  $I_{ds}$  clearly differentiate each other of the four states.

For a write process, the non-volatile will overthrow the dynamic state is assumed. Dynamic writing requires 6.2V 65ns envelope applied to the control gate. Also the 4.2V on control gate and -2V on back gate is nearly equivalent. If the micro level threshold voltage shift is considered, piecewise linear writing strategy will be used to achieve accurate threshold voltage control. The non-volatile write requires 9V 30us to program and 1s to wait for charge redistribution among two floating gates. Since the high voltage programming needs settle

time, when piece-wise linear write strategy is applied, certain settle time should be scheduled by the controller.

## 5.2 Simulation Process and Results

The Verilog-A model simulation takes up huge amount of disk spaces. For 2 Gigabytes space from NC State University, it's not possible to wait for 1s with proper time step and no convergence problems of 18 double floating gate FETs. A possible substitution is to write down the charge on the top and bottom floating gate of four states and simulate the crucial transitions.

The extracted wire resistance and capacitance from Bhattacharyya's work are included in simulations. After random tests of 16 cells with reads and dynamic writes, it takes 1.03pJ to 1.63pJ to read and 0.7pJ to dynamic write. For the read, 5ns is needed from assert the bit line to the output of the sense amplifier over the SR latch. The refresh time is close to Kotipalli's work of 180ms. In comparison with Bhattacharyya's work, higher power consumptions, faster read and smaller refresh rate are reached. It's not to say this design is superior to his design. Because the change in topologies and design ideas, like this thesis proposed a very sensitive current mode amplifier, which takes higher power consumption and have higher resolution. The double floating gate FET's source are connected to ground and the current are mirrored through current mirrors into the sense amplifier, which is fundamentally different from Bhattacharyya's work. Future work needs to apply real library from manufactures instead of Predictive Technology Model to give real design and verification work instead of demonstration work.

## CHAPTER 6 CONCLUSIONS AND FUTURE WORK

### 6.1 Conclusion

A complete, fast and stable peripheral circuits design is finished in this thesis. Macro and micro variations aforementioned [3] are reduced by applying locally generated reference and piece-wise linear write circuits. The core of this thesis is building the piece-wise linear write circuits, which controls the threshold voltage difference between two cells by using externally defined current source. This method achieves the small write circuit and has an accurate control over the threshold voltage shifts in micro process variation. Also the possibilities of the read error are lowered by setting a hard threshold using this circuit. However, the Verilog-A model used in this thesis is not identical enough to other Verilog-A models, like in Bhattacharyya's work.

The thesis uses the FreePDK 45nm and Predictive 180nm, 16nm technology to give predictively demonstrative work for the peripheral circuits design. The improvement in technology is avoiding zero threshold voltage transistors by tuning the size of transistors. Faster and accurate read is achieved at the cost of consuming higher power.

### 6.2 Future work

Future researchers need to keep on finding the best tradeoff between spend and power consumption. If 16nm technology with multiple threshold voltage is accessible, it's advisable to change all the transistors in this work into 16nm technology, and power consumption tends to reduce more. This also avoids using multiple technology libraries. Careful layout of the 16nm technology is needed to withstand high voltage between the control gate and substrate.

And a controller internally designed or externally used with an ARM or FPGA should be done to give control of every phase of the double floating gate FET array.

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**APPENDICES**

## Appendix A Verilog-A module

```
// FUNCTION: Physical Model of Charging/Discharging Nanocrystal Floating Gate
// VERSION: $Revision: 2.7 $
// AUTHOR: Cadence Design Systems, Inc.
// GENERATED BY: Cadence Modelwriter 2.31
// ON: Tue May 05 13:09:59 EDT 2015
//
`include "discipline.h"
`include "constants.h"

module NanocrystalFloatingGate_NCFG_45nm_RefNV (vin, vout);
inout vin, vout;

voltage vin, vout;

real psi_weak, Qfg_top, Qfg_bottom, n, delta_phi, psi_strong, Vsurface, Vgb_acc, psi_acc,
psi_sacc, Vfg_top, Vfg_bottom, VSiO2, ESiO2, phibn, A, B,
J_FN, J_DT, psi_SiO2, Jfg_bottom_to_sub, phibn2, A2, B2, Jsub_to_fg_bottom, VHfO2,
EHfO2, phibn3, A3, B3, psi_HfO2, Jcg_to_fg_top, phibn4, A4, B4,
Jfg_top_to_cg, VHfSiO, EHfSiO, phibn5, A5, B5, psi_HfSiO, Jfg_top_to_fg_bottom, phibn6,
A6, B6, Jfg_bottom_to_fg_top;

// Physical Constants
parameter real Eo = 8.85419e-12; //Permittivity of free space [F/m]
```

```
parameter real Epi_Si = 11.8*Eo;//Permittivity of silicon [F/m]
parameter real Epi_SiO2 = 3.9*Eo; //Permittivity of SiO2 [F/m]
parameter real Epi_HfO2 = 17*Eo; //Permittivity of Hfo2 [F/m]
parameter real Epi_HfSiO = 25*Eo; //Permittivity of HfSio [F/m]
parameter real Mo = 9.10938188e-31; //Free electron mass [kg]
parameter real h = 6.62606876e-34; //Planck's constant [m^2*kg/s]
parameter real k = 1.38066e-23; //Boltzmann constant [C*V/K]
parameter real e = 1.60219e-19; //Electron charge [C]
parameter real pi = 3.141592654; //Mathematical Pi
parameter real kappa = 0.1; //(important for surface potential computation in the
accumulation region)

//Device Parameters for calculating direct tunneling and F-N tunneling

//For Programming Model
parameter real phi_HfO2_Pt = 2.75; //Maybe I will type in them in the later cases
parameter real phi_HfSiO_Mg = 1.25;
parameter real phi_SiO2_Si = 3.15;

//For Erasing Model
parameter real phi_HfO2_Mo = 1.7;
parameter real phi_HfSiO_Pt = 3.1;
parameter real phi_SiO2_Mg = 2.9;

//Parameter for Surface Potential
```

```

parameter real Ni = 1.45e16; //Intrinsic carrier concentration of silicon [1/m^-3]
parameter real Nbulk = 5e22; //Acceptor concentration in the bulk [1/m^-3]
parameter real Nchannel = 4e24; //Acceptor concentration in the channel [1/m^-3]
parameter real channel_depth = 0.02e-6; //Channel junction depth [m]
parameter real T = 300; //Temperature
parameter real doxHfO2 = 18n; //Control Gate to Top Floating Gate Oxide Thickness
parameter real doxHfSiO = 3.2n; //Top Floating Gate to Bottom Floating Gate Oxide
Thickness
parameter real doxSiO2 = 4n; //Bottom Floating Gate to Channel Oxide Thickness
parameter real phi_m = 0.1; //Contact potential of control gate to intrinsic silicon
parameter real phi_t=k*T/e; //Thermal Voltage [V]
parameter real Qo = 0; //Effective interface charge
parameter real gate_length = 45n; //Device gate length
parameter real gate_depth = 100n; //Device gate width
parameter real Area = gate_length*gate_depth; //Device gate area
//Nanocrystal Parameters (spherical NCs considered)
parameter real nc_diameter = 3.0n; //Diameter of the nanocrystal
parameter real nc_area = pi*(nc_diameter/2)*(nc_diameter/2); //Surface area of the
//nanocrystal
parameter real Nnc = (1/nc_diameter)*(1/nc_diameter)/4; //Nanocrystal density [1/m^-2]
parameter real Rnc = nc_area*Nnc; //Nanocrystal fill factor in the floating gate layer

```

parameter real C3 = Epi\_HfO2\*nc\_area/doxHfO2; //Capacitance between the control gate  
and top floating gate

parameter real C2 = Epi\_HfSiO\*nc\_area/doxHfSiO; //Capacitance between the  
top floating gate and bottom floating gate

parameter real C1 = Epi\_SiO2\*nc\_area/doxSiO2; //Capactance between the  
bottom floating gate and the substrate

//Process Parameters

parameter real const = channel\_depth/sqrt(2\*(-ln(Nbulk/Nchannel)));/(important for  
effective channel doping in next line)

parameter real Neff = Nchannel\*const\*sqrt(2\*pi)/(2\*channel\_depth);

//Effective channel doping ( here is from discussing with Dr. Di Spigna)

parameter real gamma = doxSiO2\*sqrt(2\*Epi\_Si\*e\*(Nbulk+Neff))/Epi\_SiO2;//Body effect  
coefficient I strongly doubt it here

parameter real phi\_f = phi\_t\*ln(Neff/Ni);//Fermi-level

parameter real Vfb = -phi\_f-phi\_m-Qo\*doxSiO2/Epi\_SiO2;//Flatband voltage [V]

parameter real GAMMA1 = 1/(1+gamma/sqrt(2\*phi\_t));/(important for band bending  
computation in accumulation region)

parameter real Eg=1.12; //Silicon bandgap [eV]

//Electron Mass in Silicon and SiO2

parameter real msin = (1.045+4.5e-4\*T)\*Mo;

```

parameter real moxn = 0.4*Mo;

parameter real mHfO2 = 0.17*Mo;

parameter real mHfSiO = 0.2*Mo;

parameter real time_step = 1n;

analog begin

    bound_step(time_step);

    @(timer(0,0)) begin

        Qfg_bottom = 0;          //Initial Charge on Bottom Floating Gate

        Qfg_top = 0;           //Initial Charge on Top Floating Gate

        //Computation of the initial surface potential and floating gate voltage at time = 0 seconds
        using equations for the accumulation region from

        //Pregaldiny et al, "Accounting for quantum mechanical effects from accumulation to
        inversion, in a fully analytical surface-potential-based

        //MOSFET model," Solid State Electronics, vol 48, pp 781-787, 2004

        if (V(vin)+Qfg_top/(C3+C2)+Qfg_bottom/(C2+C1) >= Vfb) begin

```

```

psi_week=      (-gamma/2+sqrt(gamma*gamma/4+V(vin)+Qfg_top/(C3+C2)      +
Qfg_bottom/(C2+C1)-Vfb))*(-gamma/2+sqrt(gamma*gamma/4+V(vin)+Qfg_top/(C3+C2)
+ Qfg_bottom/(C2+C1)-Vfb));
n=1+gamma/(2*sqrt(psi_week));
delta_phi = 2*phi_t/n*ln(1+(psi_week-2*phi_f)/(2*phi_t));
psi_strong= 2*phi_f+delta_phi;
if (psi_week <= 2*phi_f) begin                                     //weak inversion region
    Vsurface = psi_week-phi_f;
end
else begin                                                         //strong inversion region
    Vsurface = psi_strong-phi_f;
end
end
else begin                                                         //accumulation region
    Vgb_acc      =      0.5*(V(vin)+Qfg_top/(C3+C2)+Qfg_bottom/(C2+C1)-
Vfb+sqrt((V(vin)+Qfg_top/(C3+C2)+Qfg_bottom/(C2+C1)-
Vfb)*(V(vin)+Qfg_top/(C3+C2)+Qfg_bottom/(C2+C1)-Vfb)+4*kappa*kappa));
    psi_acc      =      GAMMA1*(V(vin)+Qfg_top/(C3+C2)+Qfg_bottom/(C2+C1)-Vfb-
Vgb_acc)/(sqrt(1+GAMMA1*(V(vin)+Qfg_top/(C3+C2)+Qfg_bottom/(C2+C1)-Vfb-
Vgb_acc)/(4*phi_t)*GAMMA1*(V(vin)+Qfg_top/(C3+C2)+Qfg_bottom/(C2+C1)-Vfb-
Vgb_acc)/(4*phi_t)));

```

```

psi_sacc = -phi_t*ln(1-psi_acc/phi_t+(V(vin)+Qfg_top/(C3+C2)+Qfg_bottom/(C2+C1)-
Vfb-Vgb_acc-
psi_acc)/(gamma*sqrt(phi_t))*(V(vin)+Qfg_top/(C3+C2)+Qfg_bottom/(C2+C1)-Vfb-
Vgb_acc-psi_acc)/(gamma*sqrt(phi_t)));
Vsurface = psi_sacc-phi_f;
end
Vfg_top = ((V(vin)+phi_m)*C3+Vfg_bottom*C2)/(C3+C2)+Qfg_top/(C3+C2);
Vfg_bottom = (Vfg_top*C2+Vsurface*C1)/(C2+C1)+Qfg_bottom/(C2+C1);
end

//Computation of electron tunneling through the tunnel oxide
if (Vfg_bottom >= Vsurface) begin // This is the current from Mg to Si
    VSiO2 = Vfg_bottom-Vsurface;
    ESiO2 = VSiO2/doxSiO2;
    phibn = 3.15*e;
    //Barrier height between SiO2 and the channel surface in the conduction band
    A = e*e*e*(msin/moxn)/(8*pi*h*phibn);
    B = (8*pi*pow(phibn, 1.5)*sqrt(2*moxn))/(3*e*h);
    J_FN = A*ESiO2*ESiO2*exp(-B/ESiO2); //Fowler-Nordheim tunneling equation
    if (e*VSiO2 < phibn) begin

```

```

psi_SiO2 = exp(-8*pi*sqrt(2*moxn)*(pow(phibn,1.5)-pow(phibn-
e*VSiO2,1.5)))/(3*h*e*ESiO2));
J_DT=e*e*e*(msin/moxn)/(8*pi*h*phibn)*ESiO2*ESiO2*psi_SiO2;
//Direct tunneling equation
end
else begin
J_DT=0;
end
Jfg_bottom_to_sub=J_FN+J_DT;
end
else begin
VSiO2=Vsurface-Vfg_bottom;
ESiO2=VSiO2/doxSiO2;
phibn2=2.9*e; //Electron affinity of SiO2 is assumed to be
0.9eV
A2=e*e*e*(msin/moxn)/(8*pi*h*phibn2);
B2=(8*pi*pow(phibn2, 1.5)*sqrt(2*moxn))/(3*e*h);
J_FN = A2*ESiO2*ESiO2*exp(-B2/ESiO2);
if (e*VSiO2 < phibn2) begin

```

```

    psi_SiO2      =      exp(-8*pi*sqrt(2*moxn)*(pow(phibn2,1.5)-pow(phibn2-
e*VSiO2,1.5)))/(3*h*e*ESiO2));
J_DT=e*e*e*(msin/moxn)/(8*pi*h*phibn2)*ESiO2*ESiO2*psi_SiO2;
end
else begin
    J_DT=0;
end
Jsub_to_fg_bottom=J_FN+J_DT;
end
//Computation of electron tunneling through the control gate oxide and floating gate top
if (Vfg_top <= V(vin)+phi_m) begin          // current from Mo to Pt
    VHfO2=V(vin)+phi_m-Vfg_top;
    EHfO2=VHfO2/doxHfO2;
    phibn3=2.9*e;
    A3=e*e*e*(msin/mHfO2)/(8*pi*h*phibn3);
    B3=(8*pi*pow(phibn3, 1.5)*sqrt(2*mHfO2))/(3*e*h);
    J_FN = A3*EHfO2*EHfO2*exp(-B3/EHfO2);
    if (e*VHfO2 < phibn3) begin
        psi_HfO2      =      exp(-8*pi*sqrt(2*mHfO2)*(pow(phibn3,1.5)-pow(phibn3-
e*VHfO2,1.5)))/(3*h*e*EHfO2));
        J_DT=e*e*e*(msin/mHfO2)/(8*pi*h*phibn3)*EHfO2*EHfO2*psi_HfO2;

```

```

end

else begin

    J_DT=0;

end

Jcg_to_fg_top=J_FN+J_DT;

end

else begin

    VHfO2=Vfg_top-(V(vin)+phi_m);           // curren from Pt to Mo

    EHfO2=VHfO2/doxHfO2;

    phibn4=1.7*e;

    A4=e*e*e*(msin/mHfO2)/(8*pi*h*phibn4);

    B4=(8*pi*pow(phibn4, 1.5)*sqrt(2*mHfO2))/(3*e*h);

    J_FN = A4*EHfO2*EHfO2*exp(-B4/EHfO2);

    if (e*VHfO2 < phibn4) begin

        psi_HfO2          =          exp(-8*pi*sqrt(2*mHfO2)*(pow(phibn4,1.5)-pow(phibn4-
e*VHfO2,1.5)))/(3*h*e*EHfO2));

        J_DT=e*e*e*(msin/mHfO2)/(8*pi*h*phibn4)*EHfO2*EHfO2*psi_HfO2;

    end

else begin

    J_DT=0;

end

```

```

Jfg_top_to_cg=J_FN+J_DT;

end

// Computing of electron tunneling through the floating gate top and floating gate bottom

if (Vfg_bottom <= Vfg_top) begin          // current from Mo to Pt

    VHfSiO=Vfg_top - Vfg_bottom;

    EHfSiO=VHfSiO/doxHfSiO;

    phibn5=1.25*e;

    A5=e*e*e*(msin/mHfSiO)/(8*pi*h*phibn5);

    B5=(8*pi*pow(phibn5, 1.5)*sqrt(2*mHfSiO))/(3*e*h);

    J_FN = A5*EHfSiO*EHfSiO*exp(-B3/EHfSiO);

    if (e*VHfSiO < phibn5) begin

        psi_HfSiO          =          exp(-8*pi*sqrt(2*mHfSiO)*(pow(phibn5,1.5)-pow(phibn5-
e*VHfSiO,1.5)))/(3*h*e*EHfSiO));

        J_DT=e*e*e*(msin/mHfSiO)/(8*pi*h*phibn5)*EHfSiO*EHfSiO*psi_HfSiO;

    end

else begin

    J_DT=0;

end

Jfg_top_to_fg_bottom = J_FN + J_DT;

end

```

```

else begin

    VHfSiO=Vfg_bottom - Vfg_top;

    EHfSiO=VHfSiO/doxHfSiO;

    phibn6=3.10*e;

    A6=e*e*e*(msin/mHfSiO)/(8*pi*h*phibn6);

    B6=(8*pi*pow(phibn6, 1.5)*sqrt(2*mHfSiO))/(3*e*h);

    J_FN = A6*EHfSiO*EHfSiO*exp(-B3/EHfSiO);

    if (e*VHfSiO < phibn6) begin

        psi_HfSiO      =      exp(-8*pi*sqrt(2*mHfSiO)*(pow(phibn6,1.5)-pow(phibn6-
e*VHfSiO,1.5)))/(3*h*e*EHfSiO));

        J_DT=e*e*e*(msin/mHfSiO)/(8*pi*h*phibn6)*EHfSiO*EHfSiO*psi_HfSiO;

    end

else begin

    J_DT=0;

end

Jfg_bottom_to_fg_top = J_FN + J_DT;

end

//Computing of the new surface potential after every iteration

if (Vfg_bottom >= -phi_f) begin

```

```

psi_week=          (-gamma/2+sqrt(gamma*gamma/4+Vfg_bottom+phi_f))*(-
gamma/2+sqrt(gamma*gamma/4+Vfg_bottom+phi_f));
n=1+gamma/(2*sqrt(psi_week));
delta_phi = 2*phi_t/n*ln(1+(psi_week-2*phi_f)/(2*phi_t));
psi_strong= 2*phi_f+delta_phi;
if (psi_week <= 2*phi_f) begin
    Vsurface = psi_week-phi_f;
end
else begin
    Vsurface = psi_strong-phi_f;
end
end
else begin
    Vgb_acc =
0.5*(Vfg_bottom+phi_f+sqrt((Vfg_bottom+phi_f)*(Vfg_bottom+phi_f)+4*kappa*kappa));
    psi_acc =          GAMMA1*(Vfg_bottom+phi_f-
Vgb_acc)/(sqrt(1+GAMMA1*(Vfg_bottom+phi_f-
Vgb_acc)/(4*phi_t)*GAMMA1*(Vfg_bottom+phi_f-Vgb_acc)/(4*phi_t)));
    psi_sacc =          -phi_t*ln(1-psi_acc/phi_t+(Vfg_bottom+phi_f-Vgb_acc-
psi_acc)/(gamma*sqrt(phi_t))*(Vfg_bottom+phi_f-Vgb_acc-psi_acc)/(gamma*sqrt(phi_t)));
    Vsurface = psi_sacc-phi_f;

```

end

//Computing of the new floating gate charge and voltage after each iteration

// Qfg=Qfg-(Jin\_sub+Jin\_cgate-Jout\_sub - Jout\_cgate)\*nc\_area\*Rnc\*time\_step;

// Vfg=((V(vin)+phi\_m)\*Ccgox+Vsurface\*Ctox)/(Ctox+Ccgox)+Qfg/(Ctox+Ccgox);

Qfg\_bottom = Qfg\_bottom-(Jfg\_bottom\_to\_sub-  
Jsub\_to\_fg\_bottom+Jfg\_bottom\_to\_fg\_top-Jfg\_top\_to\_fg\_bottom)\*3\*Area\*time\_step;

Qfg\_top = Qfg\_top-(Jfg\_top\_to\_fg\_bottom-Jfg\_bottom\_to\_fg\_top+Jfg\_top\_to\_cg-  
Jcg\_to\_fg\_top)\*3\*Area\*time\_step;

Vfg\_top = ((V(vin)+phi\_m)\*C3+Vfg\_bottom\*C2)/(C3+C2)+Qfg\_top/(C2+C3);

Vfg\_bottom = (Vfg\_top\*C2+Vsurface\*C1)/(C1+C2)+Qfg\_bottom/(C1+C2);

V(vout) <+ Vfg\_bottom; //The output of this Verilog-A model is the  
floating gate voltage, which is then connected to the gate terminal of a MOSFET to complete  
the physical model

@(final\_step)

```
begin  
  
  $strobe("Number Ref NV Charge per Nanocrystal Bottom Floating Gate = %e, time is %e",  
  Qfg_bottom, $realtime);  
  
  $strobe("Number Ref NV Charge per Nanocrystal Top Floating Gate= %e", Qfg_top);  
  
end  
  
end  
  
endmodule
```

**Appendix B VCO**

```
// this is the voltage controlled oscillator
```

```
** Generated for: hspiceD
```

```
** Generated on: May 5 22:18:40 2015
```

```
** Design library name: Tutorial
```

```
** Design cell name: VCO
```

```
** Design view name: schematic
```

```
////v3 net05 0 PULSE 0 1.0 20e-9 10e-12 10e-12 5e-9 10e-9
```

```
.GLOBAL vdd!
```

```
.tran 1p 1000n
```

```
.include '$PDK_DIR/ncsu_basekit/models/hspice/hspice_nom.include'
```

```
.TEMP 25.0
```

```
.OPTION
```

```
+ ARTIST=2
```

```
+ INGOLD=2
```

```
+ PARHIER=LOCAL
```

```
+ PSF=2
```

```
+ POST
```

\*\* Library name: Tutorial

\*\* Cell name: VCO

\*\* View name: schematic

\*\* Library name: Tutorial

\*\* Cell name: VCO

\*\* View name: schematic

m23 net023 net019 net036 vdd! PMOS\_VTL L=50e-9 W=222.5e-9 AD=23.3625e-15  
AS=23.3625e-15 PD=432.5e-9 PS=432.5e-9 M=1

m22 net036 net6 vdd! vdd! PMOS\_VTL L=50e-9 W=250e-9 AD=26.25e-15 AS=26.25e-15  
PD=460e-9 PS=460e-9 M=1

m15 net14 net8 net42 vdd! PMOS\_VTL L=50e-9 W=222.5e-9 AD=23.3625e-15  
AS=23.3625e-15 PD=432.5e-9 PS=432.5e-9 M=1

m25 net035 net6 vdd! vdd! PMOS\_VTL L=50e-9 W=250e-9 AD=26.25e-15 AS=26.25e-15  
PD=460e-9 PS=460e-9 M=1

m11 net6 net6 vdd! vdd! PMOS\_VTL L=50e-9 W=250e-9 AD=26.25e-15 AS=26.25e-15  
PD=460e-9 PS=460e-9 M=1

m13 net8 vout net43 vdd! PMOS\_VTL L=50e-9 W=222.5e-9 AD=23.3625e-15  
AS=23.3625e-15 PD=432.5e-9 PS=432.5e-9 M=1

m24 vout net023 net035 vdd! PMOS\_VTL L=50e-9 W=222.5e-9 AD=23.3625e-15  
AS=23.3625e-15 PD=432.5e-9 PS=432.5e-9 M=1

m14 net42 net6 vdd! vdd! PMOS\_VTL L=50e-9 W=250e-9 AD=26.25e-15 AS=26.25e-15  
PD=460e-9 PS=460e-9 M=1

m12 net43 net6 vdd! vdd! PMOS\_VTL L=50e-9 W=250e-9 AD=26.25e-15 AS=26.25e-15  
PD=460e-9 PS=460e-9 M=1

m16 net019 net14 net41 vdd! PMOS\_VTL L=50e-9 W=222.5e-9 AD=23.3625e-15  
AS=23.3625e-15 PD=432.5e-9 PS=432.5e-9 M=1

m17 net41 net6 vdd! vdd! PMOS\_VTL L=50e-9 W=250e-9 AD=26.25e-15 AS=26.25e-15  
PD=460e-9 PS=460e-9 M=1

m19 net023 net019 net037 0 NMOS\_VTL L=50e-9 W=110e-9 AD=11.55e-15 AS=11.55e-  
15 PD=320e-9 PS=320e-9 M=1

m18 net037 net05 0 0 NMOS\_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15  
PD=300e-9 PS=300e-9 M=1

m2 net38 net05 0 0 NMOS\_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9  
PS=300e-9 M=1

m21 net034 net05 0 0 NMOS\_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15  
PD=300e-9 PS=300e-9 M=1

m1 net8 vout net38 0 NMOS\_VTL L=50e-9 W=110e-9 AD=11.55e-15 AS=11.55e-15  
PD=320e-9 PS=320e-9 M=1

m5 net36 net05 0 0 NMOS\_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9  
PS=300e-9 M=1

```
m6 net019 net14 net36 0 NMOS_VTL L=50e-9 W=110e-9 AD=11.55e-15 AS=11.55e-15
PD=320e-9 PS=320e-9 M=1

m4 net37 net05 0 0 NMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1

m0 net6 net05 0 0 NMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1

m20 vout net023 net034 0 NMOS_VTL L=50e-9 W=110e-9 AD=11.55e-15 AS=11.55e-15
PD=320e-9 PS=320e-9 M=1

m3 net14 net8 net37 0 NMOS_VTL L=50e-9 W=110e-9 AD=11.55e-15 AS=11.55e-15
PD=320e-9 PS=320e-9 M=1

v3 net05 0 PULSE 0 1.0 20e-9 10e-12 10e-12 100e-9 200e-9

v0 vdd! 0 DC=1

c4 vout 0 50e-15

c3 net023 0 50e-15

c2 net019 0 50e-15

c1 net14 0 50e-15

c0 net8 0 50e-15

.END
```

**Appendix C Positive Level Shifter**

\*\* Generated for: hspiceD

\*\* Generated on: Mar 18 17:29:26 2015

\*\* Design library name: Tutorial

\*\* Design cell name: levelshiftpos

\*\* Design view name: schematic

.GLOBAL vdd!

.include '\$PDK\_DIR/ncsu\_basekit/models/hspice/hspice\_nom.include'

.include "/afs/unity.ncsu.edu/users/j/jjiang11/thesis/Predictive180NMOS.scs"

.include "/afs/unity.ncsu.edu/users/j/jjiang11/thesis/Predictive180PMOS.scs"

.include "/afs/unity.ncsu.edu/users/j/jjiang11/thesis/Predictive180NMOSZeroVt.scs"

.include "/afs/unity.ncsu.edu/users/j/jjiang11/thesis/Predictive180PMOSZeroVt.scs"

.TEMP 25.0

.OPTION

+ ARTIST=2

+ INGOLD=2

+ PARHIER=LOCAL

+ PSF=2

+ POST

.tran 1p 200n

\*\* Library name: Tutorial

\*\* Cell name: levelshiftpos

\*\* View name: schematic

m25 o2 inp net027 vddq Predictive180NMOS L=450e-9 W=10e-6

m24 o1 inn net028 vddq Predictive180NMOS L=450e-9 W=10e-6

m14 vout o2 0 0 Predictive180NMOS L=180e-9 W=1e-6

m15 vout o2 vddq vddq Predictive180PMOS L=180e-9 W=5e-6

m8 o2 o1 vddq vddq Predictive180PMOS L=450e-9 W=2e-6

m6 o1 o2 vddq vddq Predictive180PMOS L=450e-9 W=2e-6

v0 vdd! 0 DC=1

v1 vddq 0 DC=7

m3 inp inn vdd! vdd! PMOS\_VTL L=50e-9 W=1.44e-6 AD=151.2e-15 AS=151.2e-15  
PD=1.65e-6 PS=1.65e-6 M=1

m2 inn vin vdd! vdd! PMOS\_VTL L=50e-9 W=1.44e-6 AD=151.2e-15 AS=151.2e-15  
PD=1.65e-6 PS=1.65e-6 M=1

m12 net029 inp 0 0 NMOS\_VTL L=50e-9 W=2e-6 AD=210e-15 AS=210e-15 PD=2.21e-6  
PS=2.21e-6 M=1

m10 net027 vdd! net029 0 NMOS\_VTL L=50e-9 W=2e-6 AD=210e-15 AS=210e-15  
PD=2.21e-6 PS=2.21e-6 M=1

m5 net030 inn 0 0 NMOS\_VTL L=50e-9 W=2e-6 AD=210e-15 AS=210e-15 PD=2.21e-6  
PS=2.21e-6 M=1

m4 net028 vdd! net030 0 NMOS\_VTL L=50e-9 W=2e-6 AD=210e-15 AS=210e-15  
PD=2.21e-6 PS=2.21e-6 M=1

m1 inp inn 0 0 NMOS\_VTL L=50e-9 W=720e-9 AD=75.6e-15 AS=75.6e-15 PD=930e-9  
PS=930e-9 M=1

m0 inn vin 0 0 NMOS\_VTL L=50e-9 W=720e-9 AD=75.6e-15 AS=75.6e-15 PD=930e-9  
PS=930e-9 M=1

v2 vin 0 PULSE 0 1.0 3e-9 10e-11 10e-11 65e-9 100e-9

.END



## Appendix D Negative Level Shifter

\*\* Generated for: hspiceD

\*\* Generated on: Mar 19 16:42:48 2015

\*\* Design library name: Tutorial

\*\* Design cell name: levelshiftneg

\*\* Design view name: schematic

.GLOBAL vdd!

.include '\$PDK\_DIR/ncsu\_basekit/models/hspice/hspice\_nom.include'

.include "/afs/unity.ncsu.edu/users/j/jjiang11/thesis/Predictive180NMOS.scs"

.include "/afs/unity.ncsu.edu/users/j/jjiang11/thesis/Predictive180PMOS.scs"

.include "/afs/unity.ncsu.edu/users/j/jjiang11/thesis/Predictive180NMOSZeroVt.scs"

.include "/afs/unity.ncsu.edu/users/j/jjiang11/thesis/Predictive180PMOSZeroVt.scs"

.TEMP 25.0

.OPTION

+ ARTIST=2

+ INGOLD=2

+ PARHIER=LOCAL

+ PSF=2

+ POST

.tran 1p 400n

\*\* Library name: Tutorial

\*\* Cell name: levelshiftneg

\*\* View name: schematic

m4 inp inn 0 0 NMOS\_VTL L=50e-9 W=720e-9 AD=75.6e-15 AS=75.6e-15 PD=930e-9

PS=930e-9 M=1

m2 inn vin 0 0 NMOS\_VTL L=50e-9 W=720e-9 AD=75.6e-15 AS=75.6e-15 PD=930e-9

PS=930e-9 M=1

m10 vout net020 vn vn Predictive180NMOS L=450e-9 W=10e-6

m9 net020 o2 vn vn Predictive180NMOS L=450e-9 W=10e-6

```
m0 o2 b vn vn Predictive180NMOS L=450e-9 W=10e-6

m24 b o2 vn vn Predictive180NMOS L=450e-9 W=10e-6

m5 inp inn vdd! vdd! PMOS_VTL L=50e-9 W=1.44e-6 AD=151.2e-15 AS=151.2e-15
PD=1.65e-6 PS=1.65e-6 M=1

m3 inn vin vdd! vdd! PMOS_VTL L=50e-9 W=1.44e-6 AD=151.2e-15 AS=151.2e-15
PD=1.65e-6 PS=1.65e-6 M=1

v1 vn 0 DC=-7

v0 vdd! 0 DC=1

m8 vout net020 0 0 Predictive180PMOS L=450e-9 W=50e-6

m7 net020 o2 0 0 Predictive180PMOS L=450e-9 W=50e-6

m1 b inn vdd! vdd! Predictive180PMOS L=180e-9 W=50e-6

m6 o2 inp vdd! vdd! Predictive180PMOS L=180e-9 W=50e-6

v2 vin 0 PULSE 0 1.0 3e-9 10e-11 10e-11 5e-9 100e-9

.END
```

## Appendix E Constant-gm Bias Network

\*\* Generated for: hspiceD

\*\* Generated on: Jun 20 13:41:11 2015

\*\* Design library name: FinalTest

\*\* Design cell name: ConstantGmBias\_Drawing

\*\* Design view name: schematic

.GLOBAL vdd!

.TEMP 25.0

.OPTION

+ ARTIST=2

+ INGOLD=2

+ PARHIER=LOCAL

+ PSF=2

\*\* Library name: FinalTest

\*\* Cell name: ConstantGmBias\_Drawing

\*\* View name: schematic

m1 out1 out2 net6 net6 NMOS\_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15  
PD=570e-9 PS=570e-9 M=1

m0 out2 out2 0 0 NMOS\_VTH L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9  
PS=300e-9 M=1

m2 feedback out2 0 0 NMOS\_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15  
PD=300e-9 PS=300e-9 M=1

m4 out1 feedback 0 0 NMOS\_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15  
PD=300e-9 PS=300e-9 M=1

m7 feedback out2 vdd! vdd! PMOS\_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15  
PD=390e-9 PS=390e-9 M=1

m5 out1 out1 vdd! vdd! PMOS\_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15  
PD=300e-9 PS=300e-9 M=1

m6 out2 out1 vdd! vdd! PMOS\_VTH L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15  
PD=300e-9 PS=300e-9 M=1

r0 net6 0 3e3

.END

**Appendix F Auxiliary Network**

\*\* Generated for: hspiceD

\*\* Generated on: Jun 20 13:42:07 2015

\*\* Design library name: FinalTest

\*\* Design cell name: ConstantGmBias

\*\* Design view name: schematic

.GLOBAL vdd!

.TEMP 25.0

.OPTION

+ ARTIST=2

+ INGOLD=2

+ PARHIER=LOCAL

+ PSF=2

\*\* Library name: FinalTest

\*\* Cell name: ConstantGmBias

\*\* View name: schematic

v2 net025 net020

m17 net029 en\_8ua out\_8ua 0 NMOS\_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15  
PD=300e-9 PS=300e-9 M=1

m15 net028 en\_2ua out\_2ua 0 NMOS\_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15  
PD=300e-9 PS=300e-9 M=1

m8 net040 en\_1ua out\_1ua 0 NMOS\_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15  
PD=300e-9 PS=300e-9 M=1

m16 net030 en\_4ua out\_4ua 0 NMOS\_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15  
PD=300e-9 PS=300e-9 M=1

m3 net020 gmbias2 0 0 NMOS\_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15  
PD=300e-9 PS=300e-9 M=1

m18 net029 bias1 vdd! vdd! PMOS\_VTL L=50e-9 W=720e-9 AD=75.6e-15 AS=75.6e-15  
PD=930e-9 PS=930e-9 M=1

m13 net028 bias1 vdd! vdd! PMOS\_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15  
PD=390e-9 PS=390e-9 M=1

m14 net030 bias1 vdd! vdd! PMOS\_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15  
PD=570e-9 PS=570e-9 M=1

m12 net040 bias1 vdd! vdd! PMOS\_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15  
PD=300e-9 PS=300e-9 M=1

m11 net025 net025 net022 vdd! PMOS\_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15  
PD=300e-9 PS=300e-9 M=1

m10 net022 net022 bias1 vdd! PMOS\_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15  
PD=300e-9 PS=300e-9 M=1

m9 bias1 bias1 vdd! vdd! PMOS\_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15  
PD=300e-9 PS=300e-9 M=1

.END

**Appendix G Double Floating Gate FET Array**

\*\* Generated for: hspiceD

\*\* Generated on: Jun 20 13:08:18 2015

\*\* Design library name: FinalTest

\*\* Design cell name: TestAll

\*\* Design view name: config

.PARAM eo k t e gate\_length gate\_depth pi nc\_diameter nc\_area nnc epi\_hfo2

+ doxhfo2 epi\_hfsio doxhfsio epi\_sio2 doxsio2 channel\_depth nbulk nchannel

+ epi\_si neff phi\_t ni phi\_f phi\_m qo gamma mo

.TEMP 25.0

.OPTION

+ ARTIST=2

+ INGOLD=2

+ PARHIER=LOCAL

+ PSF=2

\*\* Library name: NCFG\_45nm\_1

\*\* Cell name: NCFG\_45nm\_1

\*\* View name: schematic

\*\* Inherited view list: hspiceD spice cmos\_sch cmos.sch schematic

.subckt NCFG\_45nm\_1 b cg d s

m0 d net9 s b PredictiveNMOS L=45e-9 W=100e-9

xi0 cg net9 NanocrystalFloatingGate\_45nm\_1 Eo=8.85419e-12 Epi\_Si='11.8\*eo'

Epi\_SiO2='3.9\*eo' Epi\_HfO2='17\*eo' Epi\_HfSiO='25\*eo' Mo=910.938e-33 h=662.607e-36

k=13.8066e-24 e=160.219e-21 pi=3.14159 kappa=100e-3 time\_step=10e-9

phi\_HfO2\_Pt=2.75 phi\_HfSiO\_Mg=1.25 phi\_SiO2\_Si=3.15 phi\_HfO2\_Mo=1.7

phi\_HfSiO\_Pt=3.1 phi\_SiO2\_Mg=2.9 Ni=14.5e15 Nbulk=50e21 Nchannel=4e24

channel\_depth=20e-9 T=300 doxHfO2=18e-9 doxHfSiO=3.2e-9 doxSiO2=4e-9

phi\_m=100e-3 phi\_t='(k\*t)/e' Qo=0 gate\_length=45e-9 gate\_depth=100e-9

Area='gate\_length\*gate\_depth' nc\_diameter=3e-9

nc\_area='(pi\*(nc\_diameter/2))\*(nc\_diameter/2)' Nnc='((1/nc\_diameter)\*(1/nc\_diameter))/4'

Rnc='nc\_area\*nnc' C3='(epi\_hfo2\*nc\_area)/doxhfo2' C2='(epi\_hfsio\*nc\_area)/doxhfsio'

C1='(epi\_sio2\*nc\_area)/doxsio2' const='channel\_depth/sqrt(2\*(-ln(nbulk/nchannel)))'

```

Neff=nchannel gamma='(doxsio2*sqrt(((2*epi_si)*e)*(nbulk+neff)))/epi_sio2'
phi_f='phi_t*ln(neff/ni)' Vfb='(-phi_f-phi_m)-(qo*doxsio2)/epi_sio2'
GAMMA1='1/(1+gamma/sqrt(2*phi_t))' Eg=1.12 msin='(1.045+450e-6*t)*mo'
+moxn='400e-3*mo' mHfO2='170e-3*mo' mHfSiO='200e-3*mo'

```

```
.ends NCFG_45nm_1
```

```
** End of subcircuit definition.
```

```
** Library name: NCFG_45nm_2
```

```
** Cell name: NCFG_45nm_2
```

```
** View name: schematic
```

```
** Inherited view list: hspiceD spice cmos_sch cmos.sch schematic
```

```
.subckt NCFG_45nm_2 b cg d s
```

```

xi0 cg net11 NanocrystalFloatingGate_45nm_2 Eo=8.85419e-12 Epi_Si='11.8*eo'
Epi_SiO2='3.9*eo' Epi_HfO2='17*eo' Epi_HfSiO='25*eo' Mo=910.938e-33 h=662.607e-36
k=13.8066e-24 e=160.219e-21 pi=3.14159 kappa=100e-3 time_step=10e-9
phi_HfO2_Pt=2.75 phi_HfSiO_Mg=1.25 phi_SiO2_Si=3.15 phi_HfO2_Mo=1.7
phi_HfSiO_Pt=3.1 phi_SiO2_Mg=2.9 Ni=14.5e15 Nbulk=50e21 Nchannel=4e24
channel_depth=20e-9 T=300 doxHfO2=18e-9 doxHfSiO=3.2e-9 doxSiO2=4e-9

```

```

phi_m=100e-3 phi_t=(k*t)/e' Qo=0 gate_length=45e-9 gate_depth=100e-9
Area='gate_length*gate_depth' nc_diameter=3e-9
nc_area=(pi*(nc_diameter/2))*(nc_diameter/2)' Nnc='((1/nc_diameter)*(1/nc_diameter))/4'
Rnc='nc_area*nnc' C3=(epi_hfo2*nc_area)/doxhfo2' C2=(epi_hfsio*nc_area)/doxhfsio'
C1=(epi_sio2*nc_area)/doxsio2' const='channel_depth/sqrt(2*(-ln(nbulk/nchannel)))'
Neff=nchannel gamma=(doxsio2*sqrt(((2*epi_si)*e)*(nbulk+neff)))/epi_sio2'
phi_f='phi_t*ln(neff/ni)' Vfb=(-phi_f-phi_m)-(qo*doxsio2)/epi_sio2'
GAMMA1='1/(1+gamma/sqrt(2*phi_t))' Eg=1.12 msin=(1.045+450e-6*t)*mo'
+moxn='400e-3*mo' mHfO2='170e-3*mo' mHfSiO='200e-3*mo'

m0 d net11 s b PredictiveNMOS L=45e-9 W=100e-9

.ends NCFG_45nm_2

** End of subcircuit definition.

** Library name: NCFG_45nm_3

** Cell name: NCFG_45nm_3

** View name: schematic

** Inherited view list: hspiceD spice cmos_sch cmos.sch schematic

.subckt NCFG_45nm_3 b cg d s

```

```

xi1 cg net5 NanocrystalFloatingGate_45nm_3 Eo=8.85419e-12 Epi_Si='11.8*eo'
Epi_SiO2='3.9*eo' Epi_HfO2='17*eo' Epi_HfSiO='25*eo' Mo=910.938e-33 h=662.607e-36
k=13.8066e-24 e=160.219e-21 pi=3.14159 kappa=100e-3 time_step=10e-9
phi_HfO2_Pt=2.75 phi_HfSiO_Mg=1.25 phi_SiO2_Si=3.15 phi_HfO2_Mo=1.7
phi_HfSiO_Pt=3.1 phi_SiO2_Mg=2.9 Ni=14.5e15 Nbulk=50e21 Nchannel=4e24
channel_depth=20e-9 T=300 doxHfO2=18e-9 doxHfSiO=3.2e-9 doxSiO2=4e-9
phi_m=100e-3 phi_t='(k*t)/e' Qo=0 gate_length=45e-9 gate_depth=100e-9
Area='gate_length*gate_depth' nc_diameter=3e-9
nc_area='(pi*(nc_diameter/2))*(nc_diameter/2)' Nnc='((1/nc_diameter)*(1/nc_diameter))/4'
Rnc='nc_area*nnc' C3='(epi_hfo2*nc_area)/doxhfo2' C2='(epi_hfsio*nc_area)/doxhfsio'
C1='(epi_sio2*nc_area)/doxsio2' const='channel_depth/sqrt(2*(-ln(nbulk/nchannel)))'
Neff=nchannel gamma='(doxsio2*sqrt(((2*epi_si)*e)*(nbulk+neff)))/epi_sio2'
phi_f='phi_t*ln(neff/ni)' Vfb='(-phi_f-phi_m)-(qo*doxsio2)/epi_sio2'
GAMMA1='1/(1+gamma/sqrt(2*phi_t))' Eg=1.12 msin='(1.045+450e-6*t)*mo'
+moxn='400e-3*mo' mHfO2='170e-3*mo' mHfSiO='200e-3*mo'

m0 d net5 s b PredictiveNMOS L=45e-9 W=100e-9

.ends NCFG_45nm_3

** End of subcircuit definition.

```

\*\* Library name: NCFG\_45nm\_4

\*\* Cell name: NCFG\_45nm\_4

\*\* View name: schematic

\*\* Inherited view list: hspiceD spice cmos\_sch cmos.sch schematic

.subckt NCFG\_45nm\_4 b cg d s

m0 d net11 s b PredictiveNMOS L=45e-9 W=100e-9

xi0 cg net11 NanocrystalFloatingGate\_45nm\_4 Eo=8.85419e-12 Epi\_Si='11.8\*eo'

Epi\_SiO2='3.9\*eo' Epi\_HfO2='17\*eo' Epi\_HfSiO='25\*eo' Mo=910.938e-33 h=662.607e-36

k=13.8066e-24 e=160.219e-21 pi=3.14159 kappa=100e-3 time\_step=10e-9

phi\_HfO2\_Pt=2.75 phi\_HfSiO\_Mg=1.25 phi\_SiO2\_Si=3.15 phi\_HfO2\_Mo=1.7

phi\_HfSiO\_Pt=3.1 phi\_SiO2\_Mg=2.9 Ni=14.5e15 Nbulk=50e21 Nchannel=4e24

channel\_depth=20e-9 T=300 doxHfO2=18e-9 doxHfSiO=3.2e-9 doxSiO2=4e-9

phi\_m=100e-3 phi\_t='(k\*t)/e' Qo=0 gate\_length=45e-9 gate\_depth=100e-9

Area='gate\_length\*gate\_depth' nc\_diameter=3e-9

nc\_area='(pi\*(nc\_diameter/2))\*(nc\_diameter/2)' Nnc='((1/nc\_diameter)\*(1/nc\_diameter))/4'

Rnc='nc\_area\*nnc' C3='(epi\_hfo2\*nc\_area)/doxhfo2' C2='(epi\_hfsio\*nc\_area)/doxhfsio'

C1='(epi\_sio2\*nc\_area)/doxsio2' const='channel\_depth/sqrt(2\*(-ln(nbulk/nchannel)))'

Neff=nchannel gamma='(doxsio2\*sqrt(((2\*epi\_si)\*e)\*(nbulk+neff)))/epi\_sio2'

```

phi_f='phi_t*ln(neff/ni)' Vfb='(-phi_f-phi_m)-(qo*doxsio2)/epi_sio2'
GAMMA1='1/(1+gamma/sqrt(2*phi_t))' Eg=1.12 msin='(1.045+450e-6*t)*mo'
+moxn='400e-3*mo' mHfO2='170e-3*mo' mHfSiO='200e-3*mo'

```

```
.ends NCFG_45nm_4
```

```
** End of subcircuit definition.
```

```
** Library name: NCFG_45nm_5
```

```
** Cell name: NCFG_45nm_5
```

```
** View name: schematic
```

```
** Inherited view list: hspiceD spice cmos_sch cmos.sch schematic
```

```
.subckt NCFG_45nm_5 b cg d s
```

```
xi0 cg net9 NanocrystalFloatingGate_45nm_5 Eo=8.85419e-12 Epi_Si='11.8*eo'
```

```
Epi_SiO2='3.9*eo' Epi_HfO2='17*eo' Epi_HfSiO='25*eo' Mo=910.938e-33 h=662.607e-36
```

```
k=13.8066e-24 e=160.219e-21 pi=3.14159 kappa=100e-3 time_step=10e-9
```

```
phi_HfO2_Pt=2.75 phi_HfSiO_Mg=1.25 phi_SiO2_Si=3.15 phi_HfO2_Mo=1.7
```

```
phi_HfSiO_Pt=3.1 phi_SiO2_Mg=2.9 Ni=14.5e15 Nbulk=50e21 Nchannel=4e24
```

```
channel_depth=20e-9 T=300 doxHfO2=18e-9 doxHfSiO=3.2e-9 doxSiO2=4e-9
```

```
phi_m=100e-3 phi_t='(k*t)/e' Qo=0 gate_length=45e-9 gate_depth=100e-9
```

```

Area='gate_length*gate_depth' nc_diameter=3e-9
nc_area='(pi*(nc_diameter/2))*(nc_diameter/2)' Nnc='((1/nc_diameter)*(1/nc_diameter))/4'
Rnc='nc_area*nnc' C3='(epi_hfo2*nc_area)/doxhfo2' C2='(epi_hfsio*nc_area)/doxhfsio'
C1='(epi_sio2*nc_area)/doxsio2' const='channel_depth/sqrt(2*(-ln(nbulk/nchannel)))'
Neff=nchannel gamma='(doxsio2*sqrt(((2*epi_si)*e)*(nbulk+neff)))/epi_sio2'
phi_f='phi_t*ln(neff/ni)' Vfb='(-phi_f-phi_m)-(qo*doxsio2)/epi_sio2'
GAMMA1='1/(1+gamma/sqrt(2*phi_t))' Eg=1.12 msin='(1.045+450e-6*t)*mo'
+moxn='400e-3*mo' mHfO2='170e-3*mo' mHfSiO='200e-3*mo'

m0 d net9 s b PredictiveNMOS L=45e-9 W=100e-9

.ends NCFG_45nm_5

** End of subcircuit definition.

** Library name: NCFG_45nm_6

** Cell name: NCFG_45nm_6

** View name: schematic

** Inherited view list: hspiceD spice cmos_sch cmos.sch schematic

.subckt NCFG_45nm_6 b cg d s

```

```

m0 d net11 s b PredictiveNMOS L=45e-9 W=100e-9

xi0 cg net11 NanocrystalFloatingGate_45nm_6 Eo=8.85419e-12 Epi_Si='11.8*eo'
Epi_SiO2='3.9*eo' Epi_HfO2='17*eo' Epi_HfSiO='25*eo' Mo=910.938e-33 h=662.607e-36
k=13.8066e-24 e=160.219e-21 pi=3.14159 kappa=100e-3 time_step=10e-9
phi_HfO2_Pt=2.75 phi_HfSiO_Mg=1.25 phi_SiO2_Si=3.15 phi_HfO2_Mo=1.7
phi_HfSiO_Pt=3.1 phi_SiO2_Mg=2.9 Ni=14.5e15 Nbulk=50e21 Nchannel=4e24
channel_depth=20e-9 T=300 doxHfO2=18e-9 doxHfSiO=3.2e-9 doxSiO2=4e-9
phi_m=100e-3 phi_t='(k*t)/e' Qo=0 gate_length=45e-9 gate_depth=100e-9
Area='gate_length*gate_depth' nc_diameter=3e-9
nc_area='(pi*(nc_diameter/2))*(nc_diameter/2)' Nnc='((1/nc_diameter)*(1/nc_diameter))/4'
Rnc='nc_area*nnc' C3='(epi_hfo2*nc_area)/doxhfo2' C2='(epi_hfsio*nc_area)/doxhfsio'
C1='(epi_sio2*nc_area)/doxsio2' const='channel_depth/sqrt(2*(-ln(nbulk/nchannel)))'
Neff=nchannel gamma='(doxsio2*sqrt(((2*epi_si)*e)*(nbulk+neff)))/epi_sio2'
phi_f='phi_t*ln(neff/ni)' Vfb='(-phi_f-phi_m)-(qo*doxsio2)/epi_sio2'
GAMMA1='1/(1+gamma/sqrt(2*phi_t))' Eg=1.12 msin='(1.045+450e-6*t)*mo'
+moxn='400e-3*mo' mHfO2='170e-3*mo' mHfSiO='200e-3*mo'

.ends NCFG_45nm_6

** End of subcircuit definition.

```

\*\* Library name: NCFG\_45nm\_7

\*\* Cell name: NCFG\_45nm\_7

\*\* View name: schematic

\*\* Inherited view list: hspiceD spice cmos\_sch cmos.sch schematic

.subckt NCFG\_45nm\_7 b cg d s

xi0 cg net10 NanocrystalFloatingGate\_45nm\_7 Eo=8.85419e-12 Epi\_Si='11.8\*eo'  
 Epi\_SiO2='3.9\*eo' Epi\_HfO2='17\*eo' Epi\_HfSiO='25\*eo' Mo=910.938e-33 h=662.607e-36  
 k=13.8066e-24 e=160.219e-21 pi=3.14159 kappa=100e-3 time\_step=10e-9  
 phi\_HfO2\_Pt=2.75 phi\_HfSiO\_Mg=1.25 phi\_SiO2\_Si=3.15 phi\_HfO2\_Mo=1.7  
 phi\_HfSiO\_Pt=3.1 phi\_SiO2\_Mg=2.9 Ni=14.5e15 Nbulk=50e21 Nchannel=4e24  
 channel\_depth=20e-9 T=300 doxHfO2=18e-9 doxHfSiO=3.2e-9 doxSiO2=4e-9  
 phi\_m=100e-3 phi\_t='(k\*t)/e' Qo=0 gate\_length=45e-9 gate\_depth=100e-9  
 Area='gate\_length\*gate\_depth' nc\_diameter=3e-9  
 nc\_area='(pi\*(nc\_diameter/2))\*(nc\_diameter/2)' Nnc='((1/nc\_diameter)\*(1/nc\_diameter))/4'  
 Rnc='nc\_area\*nnc' C3='(epi\_hfo2\*nc\_area)/doxhfo2' C2='(epi\_hfsio\*nc\_area)/doxhfsio'  
 C1='(epi\_sio2\*nc\_area)/doxsio2' const='channel\_depth/sqrt(2\*(-ln(nbulk/nchannel)))'  
 Neff=nchannel gamma='(doxsio2\*sqrt(((2\*epi\_si)\*e)\*(nbulk+neff)))/epi\_sio2'  
 phi\_f='phi\_t\*ln(neff/ni)' Vfb='(-phi\_f-phi\_m)-(qo\*doxsio2)/epi\_sio2'  
 GAMMA1='1/(1+gamma/sqrt(2\*phi\_t))' Eg=1.12 msin='(1.045+450e-6\*t)\*mo'

+moxn='400e-3\*mo' mHfO2='170e-3\*mo' mHfSiO='200e-3\*mo'

m0 d net10 s b PredictiveNMOS L=45e-9 W=100e-9

.ends NCFG\_45nm\_7

\*\* End of subcircuit definition.

\*\* Library name: NCFG\_45nm\_8

\*\* Cell name: NCFG\_45nm\_8

\*\* View name: schematic

\*\* Inherited view list: hspiceD spice cmos\_sch cmos.sch schematic

.subckt NCFG\_45nm\_8 b cg d s

m0 d net10 s b PredictiveNMOS L=45e-9 W=100e-9

xi0 cg net10 NanocrystalFloatingGate\_45nm\_8 Eo=8.85419e-12 Epi\_Si='11.8\*eo'

Epi\_SiO2='3.9\*eo' Epi\_HfO2='17\*eo' Epi\_HfSiO='25\*eo' Mo=910.938e-33 h=662.607e-36

k=13.8066e-24 e=160.219e-21 pi=3.14159 kappa=100e-3 time\_step=10e-9

phi\_HfO2\_Pt=2.75 phi\_HfSiO\_Mg=1.25 phi\_SiO2\_Si=3.15 phi\_HfO2\_Mo=1.7

phi\_HfSiO\_Pt=3.1 phi\_SiO2\_Mg=2.9 Ni=14.5e15 Nbulk=50e21 Nchannel=4e24

channel\_depth=20e-9 T=300 doxHfO2=18e-9 doxHfSiO=3.2e-9 doxSiO2=4e-9

```

phi_m=100e-3 phi_t='(k*t)/e' Qo=0 gate_length=45e-9 gate_depth=100e-9
Area='gate_length*gate_depth' nc_diameter=3e-9
nc_area='(pi*(nc_diameter/2))*(nc_diameter/2)' Nnc='((1/nc_diameter)*(1/nc_diameter))/4'
Rnc='nc_area*nnc' C3='(epi_hfo2*nc_area)/doxhfo2' C2='(epi_hfsio*nc_area)/doxhfsio'
C1='(epi_sio2*nc_area)/doxsio2' const='channel_depth/sqrt(2*(-ln(nbulk/nchannel)))'
Neff=nchannel gamma='(doxsio2*sqrt(((2*epi_si)*e)*(nbulk+neff)))/epi_sio2'
phi_f='phi_t*ln(neff/ni)' Vfb='(-phi_f-phi_m)-(qo*doxsio2)/epi_sio2'
GAMMA1='1/(1+gamma/sqrt(2*phi_t))' Eg=1.12 msin='(1.045+450e-6*t)*mo'
+moxn='400e-3*mo' mHfO2='170e-3*mo' mHfSiO='200e-3*mo'

.ends NCFG_45nm_8

** End of subcircuit definition.

** Library name: NCFG_45nm_9

** Cell name: NCFG_45nm_9

** View name: schematic

** Inherited view list: hspiceD spice cmos_sch cmos.sch schematic

.subckt NCFG_45nm_9 b cg d s

```

```

xi0 cg net9 NanocrystalFloatingGate_45nm_9 Eo=8.85419e-12 Epi_Si='11.8*eo'
Epi_SiO2='3.9*eo' Epi_HfO2='17*eo' Epi_HfSiO='25*eo' Mo=910.938e-33 h=662.607e-36
k=13.8066e-24 e=160.219e-21 pi=3.14159 kappa=100e-3 time_step=10e-9
phi_HfO2_Pt=2.75 phi_HfSiO_Mg=1.25 phi_SiO2_Si=3.15 phi_HfO2_Mo=1.7
phi_HfSiO_Pt=3.1 phi_SiO2_Mg=2.9 Ni=14.5e15 Nbulk=50e21 Nchannel=4e24
channel_depth=20e-9 T=300 doxHfO2=18e-9 doxHfSiO=3.2e-9 doxSiO2=4e-9
phi_m=100e-3 phi_t='(k*t)/e' Qo=0 gate_length=45e-9 gate_depth=100e-9
Area='gate_length*gate_depth' nc_diameter=3e-9
nc_area='(pi*(nc_diameter/2))*(nc_diameter/2)' Nnc='((1/nc_diameter)*(1/nc_diameter))/4'
Rnc='nc_area*nnc' C3='(epi_hfo2*nc_area)/doxhfo2' C2='(epi_hfsio*nc_area)/doxhfsio'
C1='(epi_sio2*nc_area)/doxsio2' const='channel_depth/sqrt(2*(-ln(nbulk/nchannel)))'
Neff=nchannel gamma='(doxsio2*sqrt(((2*epi_si)*e)*(nbulk+neff)))/epi_sio2'
phi_f='phi_t*ln(neff/ni)' Vfb='(-phi_f-phi_m)-(qo*doxsio2)/epi_sio2'
GAMMA1='1/(1+gamma/sqrt(2*phi_t))' Eg=1.12 msin='(1.045+450e-6*t)*mo'
+moxn='400e-3*mo' mHfO2='170e-3*mo' mHfSiO='200e-3*mo'

m0 d net9 s b PredictiveNMOS L=45e-9 W=100e-9

.ends NCFG_45nm_9

** End of subcircuit definition.

```

\*\* Library name: NCFG\_45nm\_10

\*\* Cell name: NCFG\_45nm\_10

\*\* View name: schematic

\*\* Inherited view list: hspiceD spice cmos\_sch cmos.sch schematic

.subckt NCFG\_45nm\_10 b cg d s

xi0 cg net9 NanocrystalFloatingGate\_45nm\_10 Eo=8.85419e-12 Epi\_Si='11.8\*eo'  
 Epi\_SiO2='3.9\*eo' Epi\_HfO2='17\*eo' Epi\_HfSiO='25\*eo' Mo=910.938e-33 h=662.607e-36  
 k=13.8066e-24 e=160.219e-21 pi=3.14159 kappa=100e-3 time\_step=10e-9  
 phi\_HfO2\_Pt=2.75 phi\_HfSiO\_Mg=1.25 phi\_SiO2\_Si=3.15 phi\_HfO2\_Mo=1.7  
 phi\_HfSiO\_Pt=3.1 phi\_SiO2\_Mg=2.9 Ni=14.5e15 Nbulk=50e21 Nchannel=4e24  
 channel\_depth=20e-9 T=300 doxHfO2=18e-9 doxHfSiO=3.2e-9 doxSiO2=4e-9  
 phi\_m=100e-3 phi\_t='(k\*t)/e' Qo=0 gate\_length=45e-9 gate\_depth=100e-9  
 Area='gate\_length\*gate\_depth' nc\_diameter=3e-9  
 nc\_area='(pi\*(nc\_diameter/2))\*(nc\_diameter/2)' Nnc='((1/nc\_diameter)\*(1/nc\_diameter))/4'  
 Rnc='nc\_area\*nnc' C3='(epi\_hfo2\*nc\_area)/doxhfo2' C2='(epi\_hfsio\*nc\_area)/doxhfsio'  
 C1='(epi\_sio2\*nc\_area)/doxsio2' const='channel\_depth/sqrt(2\*(-ln(nbulk/nchannel)))'  
 Neff=nchannel gamma='(doxsio2\*sqrt(((2\*epi\_si)\*e)\*(nbulk+neff)))/epi\_sio2'  
 phi\_f='phi\_t\*ln(neff/ni)' Vfb='(-phi\_f-phi\_m)-(qo\*doxsio2)/epi\_sio2'  
 GAMMA1='1/(1+gamma/sqrt(2\*phi\_t))' Eg=1.12 msin='(1.045+450e-6\*t)\*mo'

+moxn='400e-3\*mo' mHfO2='170e-3\*mo' mHfSiO='200e-3\*mo'

m0 d net9 s b PredictiveNMOS L=45e-9 W=100e-9

.ends NCFG\_45nm\_10

\*\* End of subcircuit definition.

\*\* Library name: NCFG\_45nm\_11

\*\* Cell name: NCFG\_45nm\_11

\*\* View name: schematic

\*\* Inherited view list: hspiceD spice cmos\_sch cmos.sch schematic

.subckt NCFG\_45nm\_11 b cg d s

m0 d net9 s b PredictiveNMOS L=45e-9 W=100e-9

xi0 cg net9 NanocrystalFloatingGate\_45nm\_11 Eo=8.85419e-12 Epi\_Si='11.8\*eo'

Epi\_SiO2='3.9\*eo' Epi\_HfO2='17\*eo' Epi\_HfSiO='25\*eo' Mo=910.938e-33 h=662.607e-36

k=13.8066e-24 e=160.219e-21 pi=3.14159 kappa=100e-3 time\_step=10e-9

phi\_HfO2\_Pt=2.75 phi\_HfSiO\_Mg=1.25 phi\_SiO2\_Si=3.15 phi\_HfO2\_Mo=1.7

phi\_HfSiO\_Pt=3.1 phi\_SiO2\_Mg=2.9 Ni=14.5e15 Nbulk=50e21 Nchannel=4e24

channel\_depth=20e-9 T=300 doxHfO2=18e-9 doxHfSiO=3.2e-9 doxSiO2=4e-9

```

phi_m=100e-3 phi_t=(k*t)/e' Qo=0 gate_length=45e-9 gate_depth=100e-9
Area='gate_length*gate_depth' nc_diameter=3e-9
nc_area=(pi*(nc_diameter/2))*(nc_diameter/2)' Nnc='((1/nc_diameter)*(1/nc_diameter))/4'
Rnc='nc_area*nnc' C3=(epi_hfo2*nc_area)/doxhfo2' C2=(epi_hfsio*nc_area)/doxhfsio'
C1=(epi_sio2*nc_area)/doxsio2' const='channel_depth/sqrt(2*(-ln(nbulk/nchannel)))'
Neff=nchannel gamma=(doxsio2*sqrt(((2*epi_si)*e)*(nbulk+neff)))/epi_sio2'
phi_f='phi_t*ln(neff/ni)' Vfb=(-phi_f-phi_m)-(qo*doxsio2)/epi_sio2'
GAMMA1='1/(1+gamma/sqrt(2*phi_t))' Eg=1.12 msin=(1.045+450e-6*t)*mo'
+moxn='400e-3*mo' mHfO2='170e-3*mo' mHfSiO='200e-3*mo'

.ends NCFG_45nm_11

** End of subcircuit definition.

** Library name: NCFG_45nm_12

** Cell name: NCFG_45nm_12

** View name: schematic

** Inherited view list: hspiceD spice cmos_sch cmos.sch schematic

.subckt NCFG_45nm_12 b cg d s

```

```

xi0 cg net10 NanocrystalFloatingGate_45nm_12 Eo=8.85419e-12 Epi_Si='11.8*eo'
Epi_SiO2='3.9*eo' Epi_HfO2='17*eo' Epi_HfSiO='25*eo' Mo=910.938e-33 h=662.607e-36
k=13.8066e-24 e=160.219e-21 pi=3.14159 kappa=100e-3 time_step=10e-9
phi_HfO2_Pt=2.75 phi_HfSiO_Mg=1.25 phi_SiO2_Si=3.15 phi_HfO2_Mo=1.7
phi_HfSiO_Pt=3.1 phi_SiO2_Mg=2.9 Ni=14.5e15 Nbulk=50e21 Nchannel=4e24
channel_depth=20e-9 T=300 doxHfO2=18e-9 doxHfSiO=3.2e-9 doxSiO2=4e-9
phi_m=100e-3 phi_t='(k*t)/e' Qo=0 gate_length=45e-9 gate_depth=100e-9
Area='gate_length*gate_depth' nc_diameter=3e-9
nc_area='(pi*(nc_diameter/2))*(nc_diameter/2)' Nnc='((1/nc_diameter)*(1/nc_diameter))/4'
Rnc='nc_area*nnc' C3='(epi_hfo2*nc_area)/doxhfo2' C2='(epi_hfsio*nc_area)/doxhfsio'
C1='(epi_sio2*nc_area)/doxsio2' const='channel_depth/sqrt(2*(-ln(nbulk/nchannel)))'
Neff=nchannel gamma='(doxsio2*sqrt(((2*epi_si)*e)*(nbulk+neff)))/epi_sio2'
phi_f='phi_t*ln(neff/ni)' Vfb='(-phi_f-phi_m)-(qo*doxsio2)/epi_sio2'
GAMMA1='1/(1+gamma/sqrt(2*phi_t))' Eg=1.12 msin='(1.045+450e-6*t)*mo'
+moxn='400e-3*mo' mHfO2='170e-3*mo' mHfSiO='200e-3*mo'

m0 d net10 s b PredictiveNMOS L=45e-9 W=100e-9

.ends NCFG_45nm_12

** End of subcircuit definition.

```

\*\* Library name: NCFG\_45nm\_13

\*\* Cell name: NCFG\_45nm\_13

\*\* View name: schematic

\*\* Inherited view list: hspiceD spice cmos\_sch cmos.sch schematic

.subckt NCFG\_45nm\_13 b cg d s

m0 d net10 s b PredictiveNMOS L=45e-9 W=100e-9

xi0 cg net10 NanocrystalFloatingGate\_45nm\_13 Eo=8.85419e-12 Epi\_Si='11.8\*eo'

Epi\_SiO2='3.9\*eo' Epi\_HfO2='17\*eo' Epi\_HfSiO='25\*eo' Mo=910.938e-33 h=662.607e-36

k=13.8066e-24 e=160.219e-21 pi=3.14159 kappa=100e-3 time\_step=10e-9

phi\_HfO2\_Pt=2.75 phi\_HfSiO\_Mg=1.25 phi\_SiO2\_Si=3.15 phi\_HfO2\_Mo=1.7

phi\_HfSiO\_Pt=3.1 phi\_SiO2\_Mg=2.9 Ni=14.5e15 Nbulk=50e21 Nchannel=4e24

channel\_depth=20e-9 T=300 doxHfO2=18e-9 doxHfSiO=3.2e-9 doxSiO2=4e-9

phi\_m=100e-3 phi\_t='(k\*t)/e' Qo=0 gate\_length=45e-9 gate\_depth=100e-9

Area='gate\_length\*gate\_depth' nc\_diameter=3e-9

nc\_area='(pi\*(nc\_diameter/2))\*(nc\_diameter/2)' Nnc='((1/nc\_diameter)\*(1/nc\_diameter))/4'

Rnc='nc\_area\*nnc' C3='(epi\_hfo2\*nc\_area)/doxhfo2' C2='(epi\_hfsio\*nc\_area)/doxhfsio'

C1='(epi\_sio2\*nc\_area)/doxsio2' const='channel\_depth/sqrt(2\*(-ln(nbulk/nchannel)))'

Neff=nchannel gamma='(doxsio2\*sqrt(((2\*epi\_si)\*e)\*(nbulk+neff)))/epi\_sio2'

```

phi_f='phi_t*ln(neff/ni)' Vfb='(-phi_f-phi_m)-(qo*doxsio2)/epi_sio2'
GAMMA1='1/(1+gamma/sqrt(2*phi_t))' Eg=1.12 msin='(1.045+450e-6*t)*mo'
+moxn='400e-3*mo' mHfO2='170e-3*mo' mHfSiO='200e-3*mo'

```

```
.ends NCFG_45nm_13
```

```
** End of subcircuit definition.
```

```
** Library name: NCFG_45nm_14
```

```
** Cell name: NCFG_45nm_14
```

```
** View name: schematic
```

```
** Inherited view list: hspiceD spice cmos_sch cmos.sch schematic
```

```
.subckt NCFG_45nm_14 b cg d s
```

```

xi0 cg net9 NanocrystalFloatingGate_45nm_14 Eo=8.85419e-12 Epi_Si='11.8*eo'
Epi_SiO2='3.9*eo' Epi_HfO2='17*eo' Epi_HfSiO='25*eo' Mo=910.938e-33 h=662.607e-36
k=13.8066e-24 e=160.219e-21 pi=3.14159 kappa=100e-3 time_step=10e-9
phi_HfO2_Pt=2.75 phi_HfSiO_Mg=1.25 phi_SiO2_Si=3.15 phi_HfO2_Mo=1.7
phi_HfSiO_Pt=3.1 phi_SiO2_Mg=2.9 Ni=14.5e15 Nbulk=50e21 Nchannel=4e24
channel_depth=20e-9 T=300 doxHfO2=18e-9 doxHfSiO=3.2e-9 doxSiO2=4e-9
phi_m=100e-3 phi_t='(k*t)/e' Qo=0 gate_length=45e-9 gate_depth=100e-9

```

```

Area='gate_length*gate_depth' nc_diameter=3e-9
nc_area='(pi*(nc_diameter/2))*(nc_diameter/2)' Nnc='((1/nc_diameter)*(1/nc_diameter))/4'
Rnc='nc_area*nnc' C3='(epi_hfo2*nc_area)/doxhfo2' C2='(epi_hfsio*nc_area)/doxhfsio'
C1='(epi_sio2*nc_area)/doxsio2' const='channel_depth/sqrt(2*(-ln(nbulk/nchannel)))'
Neff=nchannel gamma='(doxsio2*sqrt(((2*epi_si)*e)*(nbulk+neff)))/epi_sio2'
phi_f='phi_t*ln(neff/ni)' Vfb='(-phi_f-phi_m)-(qo*doxsio2)/epi_sio2'
GAMMA1='1/(1+gamma/sqrt(2*phi_t))' Eg=1.12 msin='(1.045+450e-6*t)*mo'
+moxn='400e-3*mo' mHfO2='170e-3*mo' mHfSiO='200e-3*mo'

m0 d net9 s b PredictiveNMOS L=45e-9 W=100e-9

.ends NCFG_45nm_14

** End of subcircuit definition.

** Library name: NCFG_45nm_15

** Cell name: NCFG_45nm_15

** View name: schematic

** Inherited view list: hspiceD spice cmos_sch cmos.sch schematic

.subckt NCFG_45nm_15 b cg d s

```

```

m0 d net10 s b PredictiveNMOS L=45e-9 W=100e-9

xi0 cg net10 NanocrystalFloatingGate_45nm_15 Eo=8.85419e-12 Epi_Si='11.8*eo'
Epi_SiO2='3.9*eo' Epi_HfO2='17*eo' Epi_HfSiO='25*eo' Mo=910.938e-33 h=662.607e-36
k=13.8066e-24 e=160.219e-21 pi=3.14159 kappa=100e-3 time_step=10e-9

phi_HfO2_Pt=2.75 phi_HfSiO_Mg=1.25 phi_SiO2_Si=3.15 phi_HfO2_Mo=1.7
phi_HfSiO_Pt=3.1 phi_SiO2_Mg=2.9 Ni=14.5e15 Nbulk=50e21 Nchannel=4e24
channel_depth=20e-9 T=300 doxHfO2=18e-9 doxHfSiO=3.2e-9 doxSiO2=4e-9

phi_m=100e-3 phi_t='(k*t)/e' Qo=0 gate_length=45e-9 gate_depth=100e-9

Area='gate_length*gate_depth' nc_diameter=3e-9
nc_area='(pi*(nc_diameter/2))*(nc_diameter/2)' Nnc='((1/nc_diameter)*(1/nc_diameter))/4'
Rnc='nc_area*nnc' C3='(epi_hfo2*nc_area)/doxhfo2' C2='(epi_hfsio*nc_area)/doxhfsio'
C1='(epi_sio2*nc_area)/doxsio2' const='channel_depth/sqrt(2*(-ln(nbulk/nchannel)))'
Neff=nchannel gamma='(doxsio2*sqrt(((2*epi_si)*e)*(nbulk+neff)))/epi_sio2'
phi_f='phi_t*ln(neff/ni)' Vfb='(-phi_f-phi_m)-(qo*doxsio2)/epi_sio2'
GAMMA1='1/(1+gamma/sqrt(2*phi_t))' Eg=1.12 msin='(1.045+450e-6*t)*mo'

+moxn='400e-3*mo' mHfO2='170e-3*mo' mHfSiO='200e-3*mo'

.ends NCFG_45nm_15

** End of subcircuit definition.

```

\*\* Library name: NCFG\_45nm\_16

\*\* Cell name: NCFG\_45nm\_16

\*\* View name: schematic

\*\* Inherited view list: hspiceD spice cmos\_sch cmos.sch schematic

.subckt NCFG\_45nm\_16 b cg d s

xi0 cg net9 NanocrystalFloatingGate\_45nm\_16 Eo=8.85419e-12 Epi\_Si='11.8\*eo'  
 Epi\_SiO2='3.9\*eo' Epi\_HfO2='17\*eo' Epi\_HfSiO='25\*eo' Mo=910.938e-33 h=662.607e-36  
 k=13.8066e-24 e=160.219e-21 pi=3.14159 kappa=100e-3 time\_step=10e-9  
 phi\_HfO2\_Pt=2.75 phi\_HfSiO\_Mg=1.25 phi\_SiO2\_Si=3.15 phi\_HfO2\_Mo=1.7  
 phi\_HfSiO\_Pt=3.1 phi\_SiO2\_Mg=2.9 Ni=14.5e15 Nbulk=50e21 Nchannel=4e24  
 channel\_depth=20e-9 T=300 doxHfO2=18e-9 doxHfSiO=3.2e-9 doxSiO2=4e-9  
 phi\_m=100e-3 phi\_t='(k\*t)/e' Qo=0 gate\_length=45e-9 gate\_depth=100e-9  
 Area='gate\_length\*gate\_depth' nc\_diameter=3e-9  
 nc\_area='(pi\*(nc\_diameter/2))\*(nc\_diameter/2)' Nnc='((1/nc\_diameter)\*(1/nc\_diameter))/4'  
 Rnc='nc\_area\*nnc' C3='(epi\_hfo2\*nc\_area)/doxhfo2' C2='(epi\_hfsio\*nc\_area)/doxhfsio'  
 C1='(epi\_sio2\*nc\_area)/doxsio2' const='channel\_depth/sqrt(2\*(-ln(nbulk/nchannel)))'  
 Neff=nchannel gamma='(doxsio2\*sqrt(((2\*epi\_si)\*e)\*(nbulk+neff)))/epi\_sio2'  
 phi\_f='phi\_t\*ln(neff/ni)' Vfb='(-phi\_f-phi\_m)-(qo\*doxsio2)/epi\_sio2'  
 GAMMA1='1/(1+gamma/sqrt(2\*phi\_t))' Eg=1.12 msin='(1.045+450e-6\*t)\*mo'

+moxn='400e-3\*mo' mHfO2='170e-3\*mo' mHfSiO='200e-3\*mo'

m0 d net9 s b PredictiveNMOS L=45e-9 W=100e-9

.ends NCFG\_45nm\_16

\*\* End of subcircuit definition.

\*\* Library name: NCFG\_45nm\_RefNV

\*\* Cell name: NCFG\_45nm\_RefNV

\*\* View name: schematic

\*\* Inherited view list: hspiceD spice cmos\_sch cmos.sch schematic

.subckt NCFG\_45nm\_RefNV b cg d s

m0 d net9 s b PredictiveNMOS L=45e-9 W=100e-9

xi0 cg net9 NanocrystalFloatingGate\_NCFG\_45nm\_RefNV Eo=8.85419e-12

Epi\_Si='11.8\*eo' Epi\_SiO2='3.9\*eo' Epi\_HfO2='17\*eo' Epi\_HfSiO='25\*eo' Mo=910.938e-

33 h=662.607e-36 k=13.8066e-24 e=160.219e-21 pi=3.14159 kappa=100e-3 time\_step=10e-

9 phi\_HfO2\_Pt=2.75 phi\_HfSiO\_Mg=1.25 phi\_SiO2\_Si=3.15 phi\_HfO2\_Mo=1.7

phi\_HfSiO\_Pt=3.1 phi\_SiO2\_Mg=2.9 Ni=14.5e15 Nbulk=50e21 Nchannel=4e24

channel\_depth=20e-9 T=300 doxHfO2=18e-9 doxHfSiO=3.2e-9 doxSiO2=4e-9

```

phi_m=100e-3 phi_t='(k*t)/e' Qo=0 gate_length=45e-9 gate_depth=100e-9
Area='gate_length*gate_depth' nc_diameter=3e-9
nc_area='(pi*(nc_diameter/2))*(nc_diameter/2)' Nnc='((1/nc_diameter)*(1/nc_diameter))/4'
Rnc='nc_area*nnc' C3='(epi_hfo2*nc_area)/doxhfo2' C2='(epi_hfsio*nc_area)/doxhfsio'
C1='(epi_sio2*nc_area)/doxsio2' const='channel_depth/sqrt(2*(-ln(nbulk/nchannel)))'
Neff=nchannel gamma='(doxsio2*sqrt(((2*epi_si)*e)*(nbulk+neff)))/epi_sio2'
phi_f='phi_t*ln(neff/ni)' Vfb='(-phi_f-phi_m)-(qo*doxsio2)/epi_sio2'
GAMMA1='1/(1+gamma/sqrt(2*phi_t))' Eg=1.12

+msin='(1.045+450e-6*t)*mo' moxn='400e-3*mo' mHfO2='170e-3*mo' mHfSiO='200e-
3*mo'

.ends NCFG_45nm_RefNV

** End of subcircuit definition.

** Library name: NCFG_45nm_RefV

** Cell name: NCFG_45nm_RefV

** View name: schematic

** Inherited view list: hspiceD spice cmos_sch cmos.sch schematic

.subckt NCFG_45nm_RefV b cg d s

```

```

xi0 cg net10 NanocrystalFloatingGate_45nm_RefV Eo=8.85419e-12 Epi_Si='11.8*eo'
Epi_SiO2='3.9*eo' Epi_HfO2='17*eo' Epi_HfSiO='25*eo' Mo=910.938e-33 h=662.607e-36
k=13.8066e-24 e=160.219e-21 pi=3.14159 kappa=100e-3 time_step=10e-9
phi_HfO2_Pt=2.75 phi_HfSiO_Mg=1.25 phi_SiO2_Si=3.15 phi_HfO2_Mo=1.7
phi_HfSiO_Pt=3.1 phi_SiO2_Mg=2.9 Ni=14.5e15 Nbulk=50e21 Nchannel=4e24
channel_depth=20e-9 T=300 doxHfO2=18e-9 doxHfSiO=3.2e-9 doxSiO2=4e-9
phi_m=100e-3 phi_t='(k*t)/e' Qo=0 gate_length=45e-9 gate_depth=100e-9
Area='gate_length*gate_depth' nc_diameter=3e-9
nc_area='(pi*(nc_diameter/2))*(nc_diameter/2)' Nnc='((1/nc_diameter)*(1/nc_diameter))/4'
Rnc='nc_area*nnc' C3='(epi_hfo2*nc_area)/doxhfo2' C2='(epi_hfsio*nc_area)/doxhfsio'
C1='(epi_sio2*nc_area)/doxsio2' const='channel_depth/sqrt(2*(-ln(nbulk/nchannel)))'
Neff=nchannel gamma='(doxsio2*sqrt(((2*epi_si)*e)*(nbulk+neff)))/epi_sio2'
phi_f='phi_t*ln(neff/ni)' Vfb='(-phi_f-phi_m)-(qo*doxsio2)/epi_sio2'
GAMMA1='1/(1+gamma/sqrt(2*phi_t))' Eg=1.12 msin='(1.045+450e-6*t)*mo'
+moxn='400e-3*mo' mHfO2='170e-3*mo' mHfSiO='200e-3*mo'

m0 d net10 s b PredictiveNMOS L=45e-9 W=100e-9

.ends NCFG_45nm_RefV

** End of subcircuit definition.

```

\*\* Library name: FinalTest

\*\* Cell name: TestAll

\*\* View name: schematic

\*\* Inherited view list: hspiceD spice cmos\_sch cmos.sch schematic

xi0 sl0 wl0 bl0 0 NCFG\_45nm\_1

xi1 sl1 wl0 bl1 0 NCFG\_45nm\_2

xi2 sl2 wl0 bl2 0 NCFG\_45nm\_3

xi3 sl3 wl0 bl3 0 NCFG\_45nm\_4

xi4 sl0 wl1 bl0 0 NCFG\_45nm\_5

xi5 sl1 wl1 bl1 0 NCFG\_45nm\_6

xi6 sl2 wl1 bl2 0 NCFG\_45nm\_7

xi7 sl3 wl1 bl3 0 NCFG\_45nm\_8

xi8 sl0 wl2 bl0 0 NCFG\_45nm\_9

xi9 sl1 wl2 bl1 0 NCFG\_45nm\_10

xi10 sl2 wl2 bl2 0 NCFG\_45nm\_11

xi11 sl3 wl2 bl3 0 NCFG\_45nm\_12

xi12 sl0 wl3 bl0 0 NCFG\_45nm\_13

xi13 sl1 wl3 bl1 0 NCFG\_45nm\_14

xi14 sl2 wl3 bl2 0 NCFG\_45nm\_15

xi15 sl3 wl3 bl3 0 NCFG\_45nm\_16

xi16 0 net55 net54 0 NCFG\_45nm\_RefNV

xi17 0 net57 net56 0 NCFG\_45nm\_RefV

.hdl

"/afs/unity.ncsu.edu/users/j/jjiang11/thesis/NCFG\_45nm\_1/module\_NCFG\_45nm\_1/veriloga  
\_NCFG\_45nm\_1/veriloga.va"

.hdl

"/afs/unity.ncsu.edu/users/j/jjiang11/thesis/NCFG\_45nm\_2/module\_NCFG\_45nm\_2/veriloga  
\_NCFG\_45nm\_2/veriloga.va"

.hdl

"/afs/unity.ncsu.edu/users/j/jjiang11/thesis/NCFG\_45nm\_3/module\_NCFG\_45nm\_3/veriloga  
\_NCFG\_45nm\_3/veriloga.va"

.hdl

"/afs/unity.ncsu.edu/users/j/jjiang11/thesis/NCFG\_45nm\_4/module\_NCFG\_45nm\_4/veriloga  
\_NCFG\_45nm\_4/veriloga.va"

.hdl

```
"/afs/unity.ncsu.edu/users/j/jjiang11/thesis/NCFG_45nm_5/module_NCFG_45nm_5/veriloga  
_NCFG_45nm_5/veriloga.va"
```

.hdl

```
"/afs/unity.ncsu.edu/users/j/jjiang11/thesis/NCFG_45nm_6/module_NCFG_45nm_6/veriloga  
_NCFG_45nm_6/veriloga.va"
```

.hdl

```
"/afs/unity.ncsu.edu/users/j/jjiang11/thesis/NCFG_45nm_7/module_NCFG_45nm_7/veriloga  
_NCFG_45nm_7/veriloga.va"
```

.hdl

```
"/afs/unity.ncsu.edu/users/j/jjiang11/thesis/NCFG_45nm_8/module_NCFG_45nm_8/veriloga  
_NCFG_45nm_8/veriloga.va"
```

.hdl

```
"/afs/unity.ncsu.edu/users/j/jjiang11/thesis/NCFG_45nm_9/module_NCFG_45nm_9/veriloga  
_NCFG_45nm_9/veriloga.va"
```

.hdl

```
"/afs/unity.ncsu.edu/users/j/jjiang11/thesis/NCFG_45nm_10/module_NCFG_45nm_10/veril  
oga_NCFG_45nm_10/veriloga.va"
```

.hdl

"/afs/unity.ncsu.edu/users/j/jjiang11/thesis/NCFG\_45nm\_11/module\_NCFG\_45nm\_11/veriloga\_NCFG\_45nm\_11/veriloga.va"

.hdl

"/afs/unity.ncsu.edu/users/j/jjiang11/thesis/NCFG\_45nm\_12/module\_NCFG\_45nm\_12/veriloga\_NCFG\_45nm\_12/veriloga.va"

.hdl

"/afs/unity.ncsu.edu/users/j/jjiang11/thesis/NCFG\_45nm\_13/module\_NCFG\_45nm\_13/veriloga\_NCFG\_45nm\_13/veriloga.va"

.hdl

"/afs/unity.ncsu.edu/users/j/jjiang11/thesis/NCFG\_45nm\_14/module\_NCFG\_45nm\_14/veriloga\_NCFG\_45nm\_14/veriloga.va"

.hdl

"/afs/unity.ncsu.edu/users/j/jjiang11/thesis/NCFG\_45nm\_15/module\_NCFG\_45nm\_15/veriloga\_NCFG\_45nm\_15/veriloga.va"

.hdl

"/afs/unity.ncsu.edu/users/j/jjiang11/thesis/NCFG\_45nm\_16/module\_NCFG\_45nm\_16/veriloga\_NCFG\_45nm\_16/veriloga.va"

.hdl

```
"/afs/unity.ncsu.edu/users/j/jjiang11/thesis/NCFG_45nm_RefNV/module_NCFG_45nm_Ref  
NV/veriloga_NCFG_45nm_RefNV/veriloga.va"
```

.hdl

```
"/afs/unity.ncsu.edu/users/j/jjiang11/thesis/NCFG_45nm_RefV/module_NCFG_45nm_RefV  
/veriloga_NCFG_45nm_RefV/veriloga.va"
```

.END

**Appendix H Verification of Functionality Circuit**

\*\* Generated for: hspiceD

\*\* Generated on: Jun 20 13:02:03 2015

\*\* Design library name: FinalTest

\*\* Design cell name: SenseAmplifier

\*\* Design view name: config

.GLOBAL vdd!

.PARAM eo k t e gate\_length gate\_depth pi nc\_diameter nc\_area nnc epi\_hfo2

+ doxhfo2 epi\_hfsio doxhfsio epi\_sio2 doxsio2 channel\_depth nbulk nchannel

+ epi\_si neff phi\_t ni phi\_f phi\_m qo gamma mo

.TEMP 25.0

.OPTION

+ ARTIST=2

+ INGOLD=2

+ PARHIER=LOCAL

+ PSF=2

\*\* Library name: NCFG\_45nm\_1

\*\* Cell name: NCFG\_45nm\_1

\*\* View name: schematic

\*\* Inherited view list: hspiceD spice cmos\_sch cmos.sch schematic

.subckt NCFG\_45nm\_1 b cg d s

m0 d net9 s b PredictiveNMOS L=45e-9 W=100e-9

xi0 cg net9 NanocrystalFloatingGate\_45nm\_1

.ends NCFG\_45nm\_1

\*\* End of subcircuit definition.

\*\* Library name: NCFG\_45nm\_RefV

\*\* Cell name: NCFG\_45nm\_RefV

\*\* View name: schematic

\*\* Inherited view list: hspiceD spice cmos\_sch cmos.sch schematic

.subckt NCFG\_45nm\_RefV b cg d s

xi0 cg net10 NanocrystalFloatingGate\_45nm\_RefV

m0 d net10 s b PredictiveNMOS L=45e-9 W=100e-9

.ends NCFG\_45nm\_RefV

\*\* End of subcircuit definition.

\*\* Library name: FinalTest

\*\* Cell name: SenseAmplifier

\*\* View name: schematic

\*\* Inherited view list: hspiceD spice cmos\_sch cmos.sch schematic

m10 saout2 cs2 0 0 Predictive16VTLNMOS L=16e-9 W=32e-9

m9 saout1 cs1 0 0 Predictive16VTLNMOS L=16e-9 W=32e-9

m8 net07 en 0 0 Predictive16VTLNMOS L=16e-9 W=256e-9

m6 net0101 se net047 0 Predictive16VTLNMOS L=16e-9 W=64e-9

m5 net047 cs1 net07 0 Predictive16VTLNMOS L=16e-9 W=128e-9

m4 net0101 cs2 net07 0 Predictive16VTLNMOS L=16e-9 W=128e-9

m3 cs1 cs2 net0101 0 Predictive16VTLNMOS L=16e-9 W=64e-9

m0 cs2 cs1 net047 0 Predictive16VTLNMOS L=16e-9 W=64e-9

m11 saout2 cs2 vdd! vdd! Predictive16VTLP MOS L=16e-9 W=64e-9

m7 saout1 cs1 vdd! vdd! Predictive16VTLP MOS L=16e-9 W=64e-9

m2 cs1 cs2 vdd! vdd! Predictive16VTLP MOS L=16e-9 W=128e-9

m1 cs2 cs1 vdd! vdd! Predictive16VTLP MOS L=16e-9 W=128e-9

vbto ref net0106 iref

v24 net084 0 DC=1

v27 iref net047

vbto cell net089 icell

v22 net087 0 DC=1

v26 icell net0101

v21 net068 net088

v17 net044 0 DC=1

v16 net038 0 DC=1

v12 net042 0 DC=1

v13 net029 0 DC=1

vcell net053 net049

v4 se 0 DC=1

v3 en 0 DC=1

vref net052 net048

v0 vdd! 0 DC=1

xi14 0 net042 net054 0 NCFG\_45nm\_1

xi15 0 net029 net050 0 NCFG\_45nm\_RefV

m49 net082 net084 net0106 0 NMOS\_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15

PD=300e-9 PS=300e-9 M=1

m47 net085 net087 net089 0 NMOS\_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15

PD=300e-9 PS=300e-9 M=1

m43 net088 bout2 0 0 NMOS\_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15

PD=300e-9 PS=300e-9 M=1

m40 feedback bout2 0 0 NMOS\_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15  
PD=300e-9 PS=300e-9 M=1

m39 bout2 bout2 0 0 NMOS\_VTH L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15  
PD=300e-9 PS=300e-9 M=1

m37 bout1 bout2 net03 net03 NMOS\_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15  
PD=570e-9 PS=570e-9 M=1

m35 bout1 feedback 0 0 NMOS\_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15  
PD=300e-9 PS=300e-9 M=1

m14 net048 net044 iref net051 NMOS\_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15  
PD=300e-9 PS=300e-9 M=1

m19 net049 net038 icell 0 NMOS\_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15  
PD=300e-9 PS=300e-9 M=1

m12 net09 net038 net054 0 NMOS\_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15  
PD=300e-9 PS=300e-9 M=1

m17 net032 net044 net050 net051 NMOS\_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-  
15 PD=300e-9 PS=300e-9 M=1

m48 net082 outbias1 vdd! vdd! PMOS\_VTL L=50e-9 W=720e-9 AD=75.6e-15 AS=75.6e-  
15 PD=930e-9 PS=930e-9 M=1

m46 net085 outbias1 vdd! vdd! PMOS\_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15  
PD=300e-9 PS=300e-9 M=1

m45 net068 net068 net067 vdd! PMOS\_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15  
PD=300e-9 PS=300e-9 M=1

m44 net067 net067 outbias1 vdd! PMOS\_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-  
15 PD=300e-9 PS=300e-9 M=1

m42 outbias1 outbias1 vdd! vdd! PMOS\_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-  
15 PD=300e-9 PS=300e-9 M=1

m41 feedback bout2 vdd! vdd! PMOS\_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15  
PD=390e-9 PS=390e-9 M=1

m38 bout2 bout1 vdd! vdd! PMOS\_VTH L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15  
PD=300e-9 PS=300e-9 M=1

m36 bout1 bout1 vdd! vdd! PMOS\_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15  
PD=300e-9 PS=300e-9 M=1

m15 net032 net032 vdd! vdd! PMOS\_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15  
PD=300e-9 PS=300e-9 M=1

m13 net053 net09 vdd! vdd! PMOS\_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15  
PD=300e-9 PS=300e-9 M=1

```
m18 net052 net032 vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15  
PD=300e-9 PS=300e-9 M=1
```

```
m16 net09 net09 vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15  
PD=300e-9 PS=300e-9 M=1
```

```
r1 net03 0 3e3
```

```
.hdl
```

```
"/afs/unity.ncsu.edu/users/j/jjiang11/thesis/NCFG_45nm_1/module_NCFG_45nm_1/veriloga  
_NCFG_45nm_1/veriloga.va"
```

```
.hdl
```

```
"/afs/unity.ncsu.edu/users/j/jjiang11/thesis/NCFG_45nm_RefV/module_NCFG_45nm_RefV  
/veriloga_NCFG_45nm_RefV/veriloga.va"
```

```
.END
```