

ABSTRACT

WOOD, MICHAEL ROBERT. Magnetic Field Energy Harvesting for Localized Power Sources. (Under the direction of Dr. Wensong Yu).

This paper provides a walkthrough for the design of an AC-DC converter with an inductive magnetic field harvesting source and the controls to support it. The controls are specialized around a secondary coil used for MPPT (maximum power point tracking) measurements, unique to this project. Examples are shown on how to achieve maximum power transfer without being able to measure the real input voltage due to the inductive load. The device is designed to work within an enclosed medium voltage AC drive, harvesting power from the high magnetic fields present from the input filter.

The work has four main portions, the first being the design and iterations of a custom magnetic field harvesting device. Several designs are considered and tested in detail to work over the entire operational power range. The second portion is the theory of max power transfer and its application in magnetic field energy harvesting. The third portion is the design of the AC-DC converter and the associated sampling required for MPPT operation. Layout strategies are shown to provide noise immunity while still acquiring the sampling speed needed for control. The fourth portion is the design of the control that uses a secondary coil and a current loop for MPPT control. The current loop creates a modulation signal to provide the PWM signals to the switches. A PI controller and bandpass filter are implemented to maintain stability along with SOGI and ABDQ controllers to create the PLL and other needed signals.

A fully operational magnetic field harvester was created and tested at max bench power levels, achieving MPPT shown to be superior to equivalent open loop operation. A harvesting device was optimized to output a voltage of 2.96V and 455mW at a magnetic field level of 2mT load with a power density of 23.4 mW/cm³. An output power of 464mW was achieved at 2mT, while a series RC circuit found the real possible max power to be 485mW, giving a circuit efficiency of 95.6%; this efficiency does not include the DSP power draw. The circuit was unaffected by external or internal noise from the magnetic field or switching due to layout design and sampling methods.

High power devices often create high electric and magnetic fields, providing ample opportunity to reduce cost and isolation requirements by creating localized power sources. This work has shown that a configurable and mobile harvesting device can provide an alternative solution to the existing isolation transformers required in high power. Such devices can be customized for the application to provide the power required for operation.

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Magnetic Field Energy Harvesting for Localized Power Sources

By

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DEDICATION

To my wife Rachael who has dealt with my late nights and weekend absences, and my son who make each day a bit brighter and more colorful, I love you both.

BIOGRAPHY

Michael Wood is a student at North Carolina State University, pursuing his master's degree in electrical engineering with a focus in Power Electronics. Born in 1993 in Virginia USA, he graduated from Virginia Tech with his bachelor degree in electrical engineering in 2015. Since then, he has worked at VPT Power for two years as a test engineer before joining Danfoss as an electronics engineer in 2017. During the past five years he has taken night classes and completed his thesis work on the side while building a career in high power electronics work.

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Benefit to Company and Motivation

While determining the topic of this thesis work a study was done on the AC Drives that my company, Danfoss Drives, produces. These AC Drives are large cabinets that can have a variety of components and form factors customizable based on customer need and operate at power levels between 1MW - 6MW. These are large, enclosed, cabinets that can be placed inside ships or mines to provide precise control of heavy machinery. The energy harvesting topic was identified as solving several key issues over a range of topics that provided the motivation for this work.

The first topic is to make the device detached from any other device or power source, so it can be moved to new locations and provide localized power as needed. This requires the energy harvester to be customizable to change operation based on location, local power levels and needs as well as being done during customer setup to make it streamlined for manufacturing.

The second topic is to reduce cost by replacing expensive isolation transformers. An AC Drive contains multiple cabinet sections with different voltage classes determined by UL and/or IEC requirements. Energy harvesting can be done in locations that are difficult / expensive to supply power to and can power local sensor apparatuses for health monitoring of vital components. Besides the transformer cost, the wiring from source to end can be removed and can declutter the inside of the AC Drive.

The third topic is to reduce or eliminate the need for maintenance on battery power supplies. By harvesting local power, the harvester can charge itself and last indefinitely, eliminating the need to change out batteries every so often. This leads to increased customer interest and value as they do not need to shut down every so often for planned maintenance or possible failure due to dead batteries. Often these AC Drives have highly important roles, and any downtime can lead to hundreds of thousands in losses each day they are down, and the associated equipment cannot operate. The more 'enclosed' and 'self-regulating' they are the more competitive they will be in the market.

Ch 1 – Introduction to the Harvester System and Challenges

Design Motivation

While many parts of this work are referenced from other papers, all have been changed to fit into one larger design. No existing work could be found for an MV AC Drive enclosure pertaining to magnetic field harvesting. Most of the work used overhead power lines or custom setups to test unique shapes and focused on power density over circuit needs. This design drew from multiple examples to draw in the most power possible, within the confines of the enclosure, while also being movable within the enclosure for custom setups. It prioritizes manufacturability and robustness more than an optimal efficiency, while still expecting the maximum output possible.

The topology of this work previously existed as a Totem-Pole Bridgeless PFC. A unique part of this project is the replacement of the power source with the input series inductor itself, normally sized for the design. By making the input inductor the power supply filtering was removed that previously allowed for clean sampling of voltage and current values. Without these new solutions were developed to remove noise and sample, or recreate, the needed data from available sources. Sizing of all components needed to be considered as a wide range of power levels were possible that limited the design in several areas. This design then needs to be created at the circuit level and tested.

Controls then need to be designed to maximize output power from the variable input magnetic field seen by the harvester. Previous controls used clean samples no longer available and had to be redesigned for. New logic based on MPPT and including the use of SOGI and ABDQ controllers are used to track the input field and optimize when power is harvested. Customers can also quickly change the load on the medium voltage AC Drive and the harvester will need to adapt to these changing magnetic fields reliably. Besides a working simulation, code needs to be fit onto a processor fast enough to adapt to these changes and use as little power as possible. Several parameters will be considered for the processor and code method used, such as processor clock frequency, power requirements, fastest instruction cycles, peripherals and more. Coding style is considered by organizing firmware vs software code to make it easier to update in the future.

The Harvester

The energy harvesting system is made up of three main sections, the first section being the energy harvesting device which collects stray magnetic field energy for use. This harvester device is an inductor with a special ferrite core shape for greater field collection and a second auxiliary winding for an accurate measurement of the magnetic field. It is designed for a specific range of magnetic field strengths, distances from the source, and needed input voltage ranges for the system to work. It can be highly customized for the application and, in this case, is optimized for operation inside an enclosed AC motor drive. The motor drive has a wide power range possible, up to 3MW at 3.3kV, and that power directly relates to the range of magnetic field this harvester can experience and must work and survive in. This has been measured in Figure 1 below, where the load percentage of the driven motor is compared to the measured magnetic flux measured in tesla units by a magnetic field sensor unit; shown in Figure 2. Three of these sensors were assembled to create a 3-axis sensor for drive level measurements. At no load the drive still has some constant current flowing, which gives the lowest input of 1.1mT up to 5.82mT. This power is considered the lowest input that the harvester must work at.

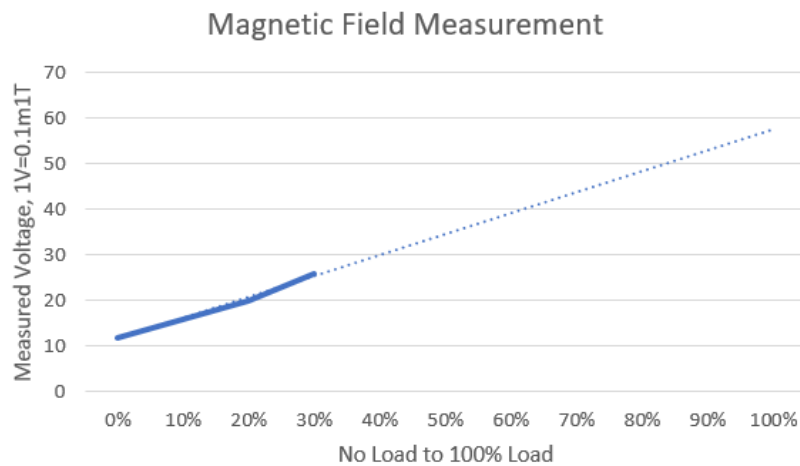


Figure 1 - Measured magnetic Field Range



Figure 2 - Magnetic Field Sensor MC95A

Circuit Topology

The second section is the circuit topology which can be designed to take the collected AC energy and rectify it into a stable DC power supply. This includes the topology, the component selection, thermal management, layout design and more. The input power from the harvester will determine the component voltage levels and power dissipation required for the circuit and can be tuned to match the application. One circuit can be designed with a power level range in mind while the harvester is tuned to match that range based on the available magnetic field. If the possible magnetic field range becomes too excessive, then the circuit design may need to be reduced in scope and multiple variants of the hardware created for different instances. Figure 3 shows the topology in PSIM that is used for open and closed loop simulation.

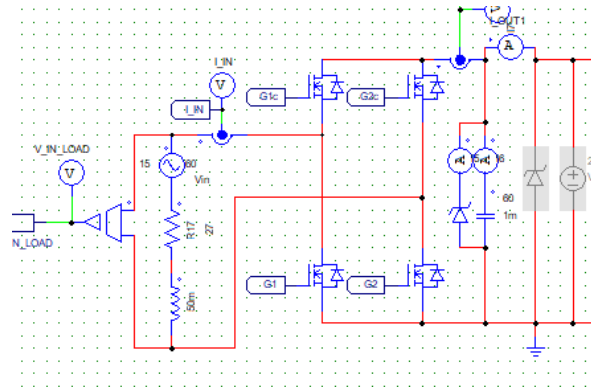


Figure 3 - PSIM Circuit Topology

Controls

The third section is the control methodology which senses the various voltages and currents and controls the circuitry in the most efficient way to rectify the power. The control is designed to implement PFC (power factor correction) through an MPPT (maximum power point tracking) methodology and to boost the output DC voltage to a stable level for use. The controller includes a PLL (phase lock loop) that senses the magnetic field induced AC voltage and matches that frequency for use in the rest of the control. The PLL is fed by a SOGI (second order generalized integrator) and ABDQ controller that takes in magnetic field voltage and produces a phase difference value based on the difference between the measured and calculated frequencies. There is a second SOGI and ABDQ used to create a DC reference of the input voltage, from the output voltage and modulation index signals, which is then used in the MPPT to track maximum power. Finally, all these signals are fed into the MPPT which compares input voltage and current over time to determine the max power modulation index. This is compared against a generated 30kHz triangle wave to create the PWM signals to control all four switches. Figure 4 shows an example of the PSIM control before discretization.

The second requirement is to make the harvester easily configurable. The harvester will not be placed in the same position each time as the LCL filter will be changed due to different customer configurations, different power levels and second source components used. The harvester can be tapped with multiple winding terminations to allow for a customized harvester for each drive. If a lower power drive is being used more windings could be added or if the harvester location is moved closer to the power source windings can be removed to achieve a usable operation range. It's ideal to have only one variant of harvester to cut down on waste in the manufacturing and logistics side of the product. Figure 6 [11] shows how an inductor can be tapped with multiple winding options.

The third requirement is for the harvester to be economical. There are many examples of ways to improve the harvester induction performance through ferrite rod design, but these are often customized and difficult or expensive to source. For this design all components should be off the shelf items found on common sourcing sites like Digikey or Mouser for easy second source options that prevent costly custom parts. The list of components chosen is listed in Appendix B. The only item not off the shelf is a customized 3D printed casing for the harvester that can still be sourced from multiple sites by send the source designs to different manufacturers.

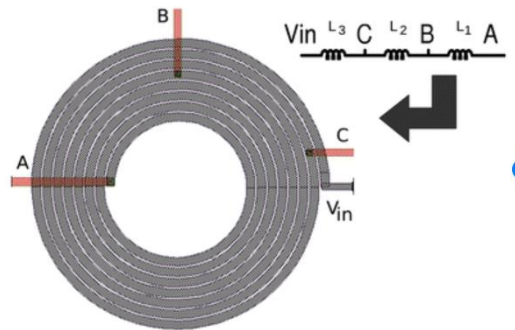


Figure 6 - Winding Tapping Example

Test Setup

During the evaluation of the harvester design two testing setups were used. The first setup, shown in Figure 7, is a bench test method using a Variac AC power source. This is a low power solution to generate a high magnetic field, but with low supply power. This method involves placing a variable AC current across a winding of wire. A separate cable is run multiple times through the winding to amplify the current induced into the cable. As there is no load across the cable the only load is the cable itself, so a high current is induced into the cable creating a high magnetic field for testing. This is the primary method used for device testing and will be the source of power for all results for this project.

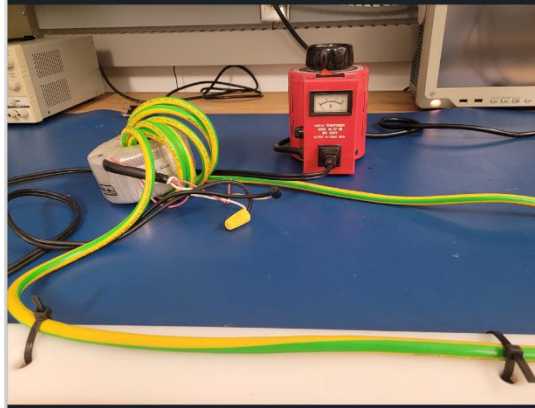


Figure 7 - Test Setup #1

The second setup, shown in Figure 8, involved the use of a medium voltage (MV) AC drive to measure the magnetic fields in a real-world environment. The input section of the drive includes a three-phase L-C filter that generates the magnetic fields intended for harvesting, primarily the fields from the inductor. Three magnetic field sensors are combined to create a three-axis field measurement sensor. This was moved around inside the drive until an optimal position was found with maximum magnetic field output in one direction with minimal noise. Such a device would be used during the commissioning of future AC drive cabinets to find the optimal spot for the harvester.



Figure 8 - Test Setup #2

The alternating phases create conflicting magnetic fields that can cancel one another out. Figure 9 shows a non-ideal sin wave measured from one position on all three-axis. The noise in the measurements can come from the conflicting magnetic fields of the three-phase inductor, other noisy devices, the enclosure, or conducted switching noise from the signal itself. This setup was used primarily to measure the magnetic field to find the minimum and maximum load for normal AC drive use conditions. Those results then determined that the Variac AC supply could output a magnetic field closely resembling the minimum magnetic field seen at an ideal point in the drive.

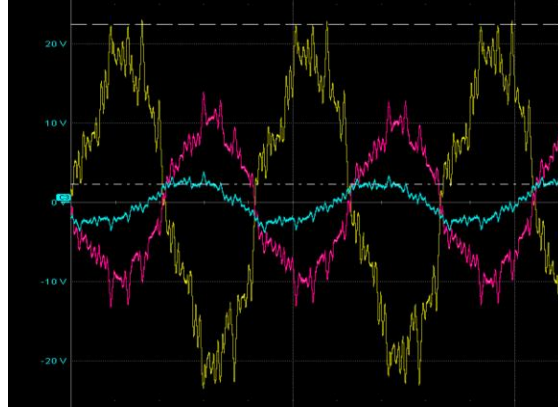


Figure 9 - Magnetic Field Measurements

Example Harvester Dimensioning and Math for Single Rod Core

To begin the harvester design its vital to understand how changing the dimensions of the harvester will change the output results. To do this a connection between the input magnetic field and the output voltage, or power, must be made. Take Figure 10, showing a winding of wire around a single rod of ferrite material. An AC magnetic field flows through the ferrite material inducing a voltage across the two ends of the wound wire. Using Faradays law in Equation 1 [1] a relationship is found between the output voltage and the magnetic field passing through the ferrite rod, these values are shown in Figure 11 [1] for dimensioning the harvester.



Figure 10 - Rod Core Winding

Equation 1 - Magnetic Field to Output Voltage

$$V_{Coil} = N * \omega * B_{ex} * A * u_{eff}$$

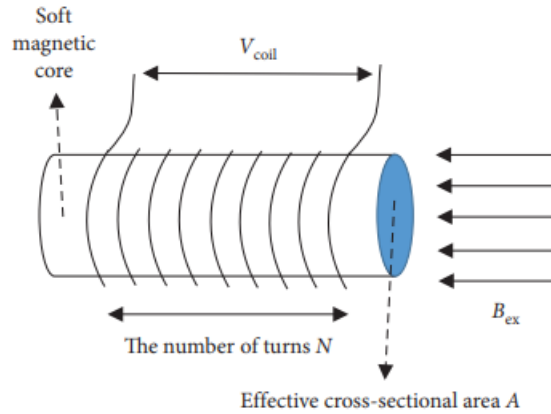


Figure 11 - Single Rod Core Dimensioning

For this equation, B_{ex} is the magnetic field passing through the core in units of tesla rms (root mean square). 'N' is the number of windings of wire around the ferrite rod. ' ω ' is the angular frequency of the magnetic field, converted from units of hertz to radians per second. 'A' is the effective cross-sectional area of the wire winding in meters². ' μ_{eff} ' is the effective permeability of the ferrite rod based on its material type and dimensions. It also includes any air gaps between the rod material and the wire winding, so while an μ_{eff} can be calculated for use, any space between the core and the winding will reduce this value. If no ferrite material is used then this value defaults to that of air, referred to as μ_0 , as it is considered an air winding with a value of $4\pi \times 10^{-7}$ Henries per meter. Finally, ' V_{coil} ' is the output voltage in rms, matching the type used from the input B_{ex} . From this equation a rough design can be started that gives a range of sizes and material types that will meet design requirements. While many of the harvester dimensions are considered in obvious ways in Faraday's equation, one not so obvious consideration is the length of the core used. The length is considered as part of μ_{eff} ; the effective permeability of the ferrite rod. This value is often provided in datasheets for common core materials off the shelf, but for new designs it can be calculated based on the size and shape of the core.

Equation 2, Equation 3, Equation 4 in show the methods to calculate this effective permeability for a single rod core.

Equation 2 [2] is a basic relationship between the diameter and length of the rod, the result being a higher length increases the output voltage while a higher diameter reduces the output voltage. This relationship is given as the results 'K' and 'd' and determines which equation is used in Equation 3 to calculate the effective permeability.

Equation 2 - Dimension Ratio

$$\text{Here, } K = l_{core} / r_{core},$$

Equation 3 [2] calculates the demagnetization factor of the single rod design. This equation is custom to the single rod design and will be changed based on the shape of the used ferrite core material. Demagnetization refers to the reduction of the effective permeability of the ferrite rod due to the demagnetization phenomenon shown in Figure 12 [2]. 'H₂' shows the magnetic flux through the core while 'H_D' shows the demagnetization effect. This phenomenon can be controlled somewhat by changes to the material shape and placement of the winding.

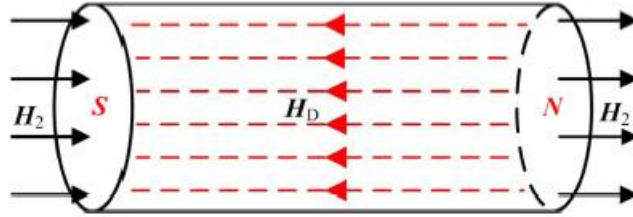


Figure 12 - Demagnetization Phenomenon

Equation 3 - Demagnetization Factor

$$\begin{cases} F = \frac{1.7(0.5K)^{0.13}}{d^3} \left(\frac{1}{K}\right)^2 \left[\ln\left(\frac{1+d}{1-d}\right) - 2d \right], & K > 2 \\ F = 0.33, & K = 2 \\ F = \frac{3.966(0.5K)^{-0.056}}{|d|^3} \left(\frac{1}{K}\right)^2 [|d| - \arctan |d|], & K < 2 \end{cases}$$

Equation 4 [2] finds the effective permeability of the core. Besides the demagnetization factor of the core, the other main factor for this equation is the base permeability of the ferrite material. This final equation combines the material geometry and properties to give the overall effective permeability of the ferrite core material used. This result then has a linear effect on the relationship between output voltage and input magnetic field. A keynote to remember is this effective permeability assumes the entirety of the core is used for the winding, which would include the portion containing the demagnetization effect. By altering the portion the winding encompasses the demagnetization effect can be further reduced.

Equation 4 - Effective Permeability

$$\mu_{\text{eff}} = \frac{B_{\text{coil}}}{\mu_0 H} = \frac{\mu_r}{1 + (\mu_r - 1)F}$$

$$B_2 = \mu_0 H_2 \frac{\mu_r}{1 + F(\mu_r - 1)}$$

Different Harvester Examples, Multi-Core, Dumbbell, Spiral

To increase the output power harvested from a set source of magnetic flux the relationship between input magnetic flux and output voltage must be improved. Based on Equation 1 there are several options for improving this ratio, however the only parameters that will not reduce output power or force a change in the supply, while still improving output voltage, involves altering the μ_{eff} or the cross-sectional area values controlled by the core geometry.

The Multi-Core, or split-core, harvester [4] is the first consideration for improving performance. Shown in Figure 13 [4], this solution attempts to take the standard rod core and improves performance by reducing core volume while increasing output power. Multiple thinner rods are placed parallel to one another and then spread out to increase the overall length of the core material. The magnetic flux now focuses itself through the ferrite material, ignoring the empty air, increasing the power density within the rods. The longer length also serves to reduce demagnetization by increasing the distance between the two ends of the ferrite material. The increased distance improves the effective permeability in the center of the rod area, increasing the output voltage in relation to the input magnetic field. The reduction of volume attempts to maximize power density, however a steep reduction in power is noted when reducing volume size too greatly. The splitting of the cores also reduces the overall magnetic field the passes into the core material, reducing the output voltage. While optimizing the power density of the ferrite material, the reduction of material does not necessarily create a smaller harvester device and multiple pockets of air will be present between the different rods. There is also the problem of accurately spacing out the rods at the correct lengths to achieve the optimal and a consistent demagnetization reduction, making this method problematic for manufacturing.

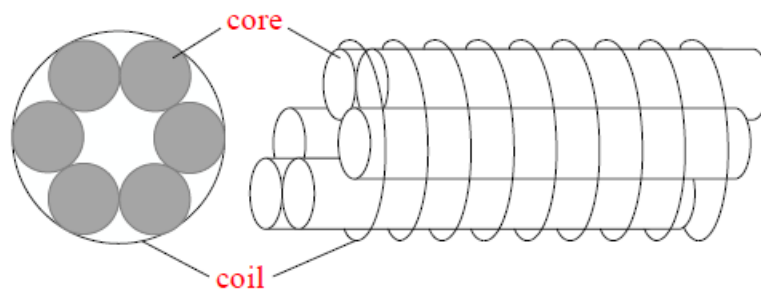


Figure 13 - Multi-Rod Core

The dumbbell harvester [2] design is the next consideration for improvement. This design re-uses the rod core and adds two 'cap' ferrites onto the ends of the rod, resembling a dumbbell in shape. The intention of the end caps is to increase the amount of magnetic flux entering the rod, as seen in Figure 14 [2], therefore increasing overall voltage linearly while also trapping much of the demagnetization effect closer to the edges and improving the effective permeability of the core. While a similar demagnetization occurs in a regular rod of the same diameter, demagnetization seen at the center of the dumbbell design will reduce effective permeability less as the smaller inner diameter has concentrated the flux greatly. The winding can then be focused on the inner core section to ignore the major of the demagnetization effect.

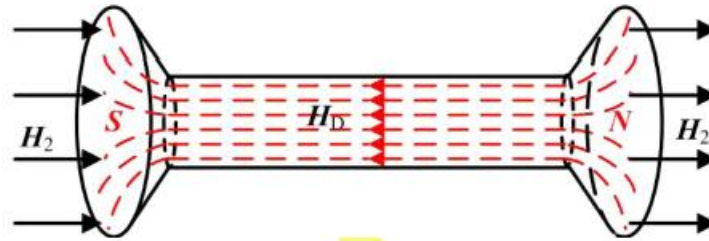


Figure 14 - Dumbbell Core

Figure 15 [3] shows an example of these benefits and is heavily discussed in [1 - 3]. While the thinner segment does show an improved effective permeability it also shows signs of the maximum density to power limits seen in the split core design. By reducing the overall diameter of the core, a saturation like effect occurs limiting the power that can be harvested from this design. Careful design must be done to match the max power output of the inner rod diameter with the expected harvesting limits.

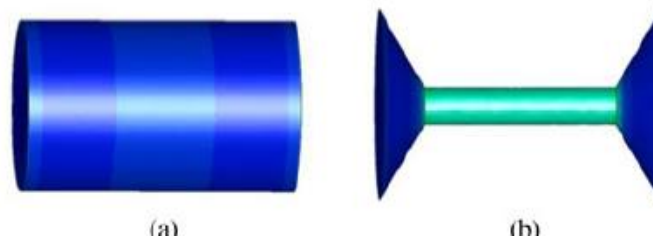


Figure 15 – Dumbbell Core

The spiral harvester [3] shown in Figure 16 [3] is the final consideration and attempts to combine all the improvements into one design. The benefit of which is the greatest improvement in flux to voltage ratio of the four options. The benefits are made possible by drastically increasing the overall effective length of the core by spiraling the ferrite material into wounds; all within a confined area. This allows the core to stay compact and fit within smaller areas while having a much higher effective length. The other benefit are the ferrite caps on both ends, increasing the area the magnetic flux passes into and then concentrating that on a thinner center section, thus reducing the demagnetization effect like the dumbbell design.

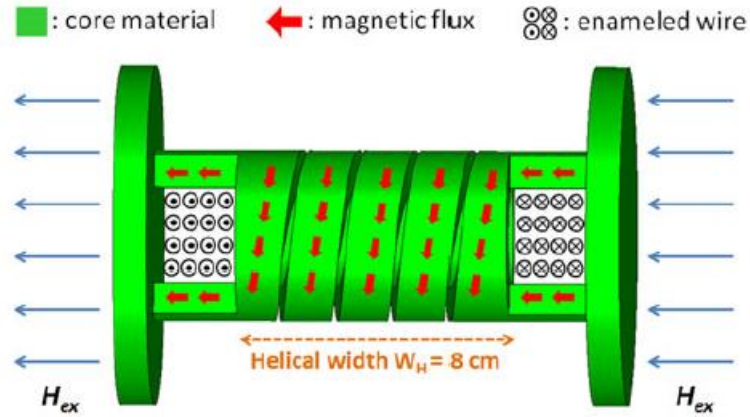


Figure 16 – Spiral Core

Simulation results from [3] show greater increases in magnetic flux as more loops are added to the spiral design. While this does provide room for customization and the greatest increase to output voltage of the four designs, there are several significant down sides to the spiral core design, most of which have to do with manufacturability and robustness. The spiral shape makes the core much more breakable than a solid rod design while the winding will also be more difficult to produce compared to a basic rod design. Both issues make this design less appealing, even with the much-improved performance over the other options. To compare these previous designs, work from [3] was converted to the equivalent 2mT input magnetic field level and reduced to stay within the 15V induced voltage limit. Figure 17 shows this comparison as a target for future harvester designs.

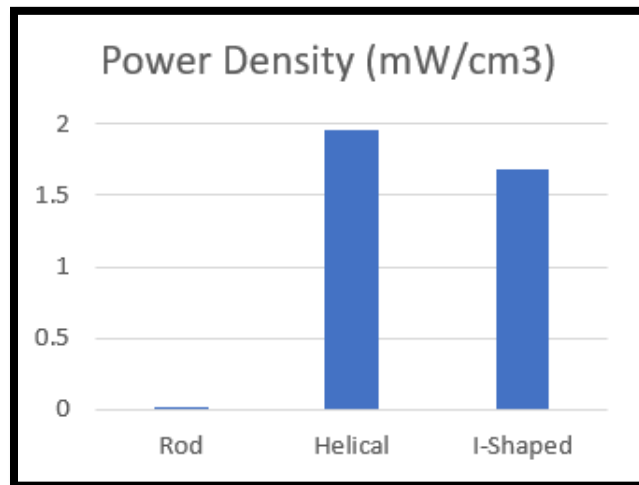


Figure 17 - Previous Work Comparison at 2mT Input

Different Harvester Examples, Sizing and Power

Now that the different types of core designs have been reviewed a comparison of power levels should be done to determine the likely power range that can be designed. Several examples are shown in [1] that give examples of what power levels to expect for different magnetic fields and core sizes and shapes. Figure 18 shows the power density of several designs within a 6.5uTrms field. When doing comparisons of power density between different magnetic fields the comparison is not one to one. The open circuit voltage, shown in Figure 21, has a positive linear relationship with magnetic field; shown in Equation 1. When determining total power, the voltage must be squared and then divided by the total resistance of the harvester, a factor of the number of turns and diameter of the rod core. To convert power densities between differing magnetic field strengths Equation 5 can be used. The magnetic field 'Bex' can be isolated, and the old field strength replaced with the new. From Figure 1 its seen the lowest magnetic field is for our setup is 1.1mT and when this is applied to Figure 18 grid-shape [b] the max power density becomes 1.9mW/cm³. A helical core from [1] and [3] is shown to have one of the highest power densities of 9.8uW/cm³ at 7uTrms. Converted to the minimum power density of 1.1mT it reached 121mW/cm³. The helical core, while efficient, is not practical for manufacturing, so a goal for power density is to stay between 1.9mW/cm³ and 121mW/cm³ at minimum power. Likely, the power density achieved can be higher than 1.9mW/cm³ as the core size can have an exponential effect on density compared to voltage. Table 1 shows examples from other works for optimized output powers for future comparison.

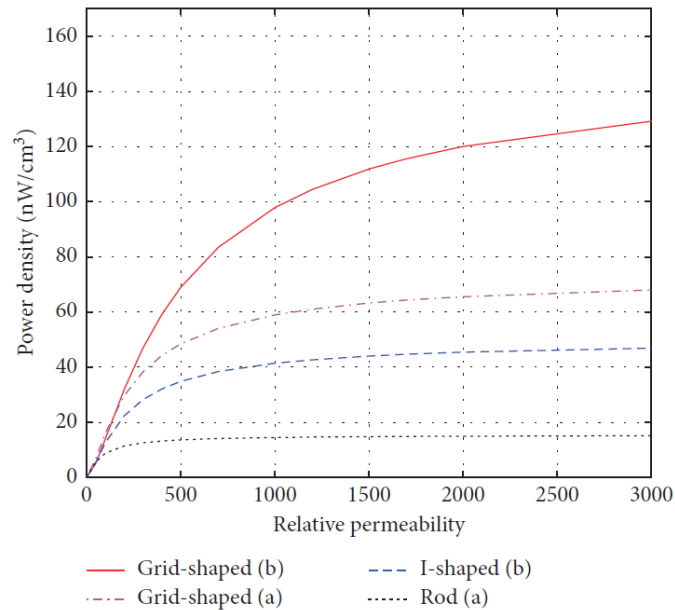


Figure 18 - Power Density Comparison

Equation 5 - Power Density Equation

$$\text{Power density} = \frac{(V_{\text{Coil}})^2}{R_{\text{wire}} * \text{vol}} = \frac{(N * \omega * B_{\text{ex}} * A * u_{\text{eff}})^2}{R_{\text{wire}} * \text{vol}}$$

Table 1 - Other Harvester Examples

parameter	Rod	Helical	I-Shaped	Split Core
Length	50 cm	15 cm	28 cm	unknown
Magnetic Flux Density	7 μ Trms	7 μ Trms	7 μ Trms	70.7 μ Trms
Number of Windings	40000	2000	40000	5000
Wire Diameter	unknown	0.4mm	0.33mm	unknown
Max Output Power	833 μ W	2.86mW	5.2mW	unknown
Power Density	0.12 μ W/cm ³	9.8 μ W/cm ³	8.4 μ W/cm ³	1.15 mW/cm ³
Planned Flux Density	1.4mTrms	1.4mTrms	1.4mTrms	1.4mTrms
Planned Output Power Density	4.9 mW/cm ³	400 mW/cm ³	343 mW/cm ³	460 mW/cm ³

Version 1 Harvester Design

The dumbbell design was chosen as a good compromise between the base rod and spiral designs. As previously mentioned, the dumbbell design has been extensively reviewed in other papers that show the tradeoffs between different dimensions. While the base rod has an effective permeability equation that accounts for all dimensions, there exists no such equation for the dumbbell design. The rod Equation 1 can be used to give a relationship between the input magnetic flux and the output voltage, but specifically leaves out the dimensions of the caps on the ends and the effect they have. Both the diameter and width of these caps will affect the overall effective permeability of the harvester and must be considered.

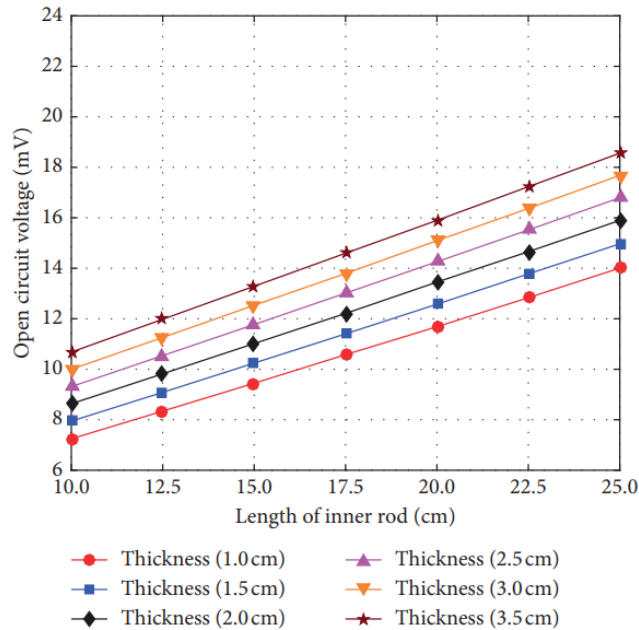


Figure 19 [1] shows the relationship between the outer cap thickness and the output voltage, showing how a thicker end cap allows for more magnetic flux flow into the rod and traps more demagnetization towards the ends, increasing output voltage.

Figure 20 [1] then shows the relationship between outer cap diameter and the overall power level achievable for the harvester, showing that a larger diameter allows more magnetic flux into the harvester, and therefore higher output power.

Finally,

Figure 21 [1] shows a general relationship between the base rod design and several variants of the dumbbell design, showing up to five times increase in output voltage compared to the base rod design.

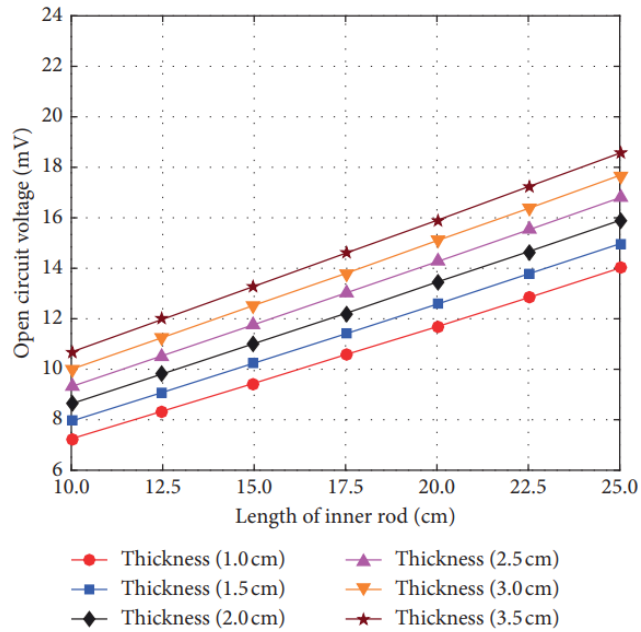


Figure 19 - End Cap Thickness

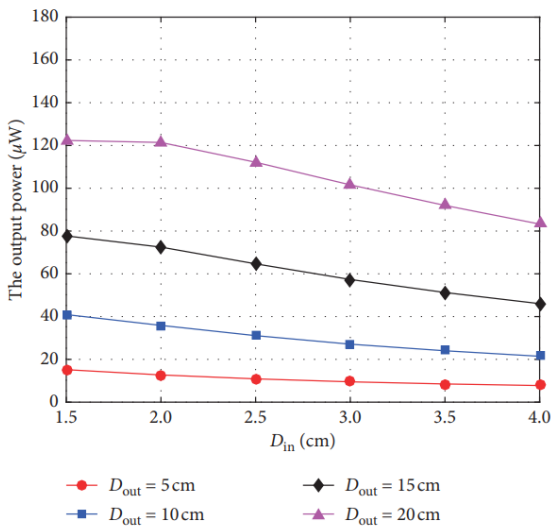


Figure 20 - End Cap Diameter

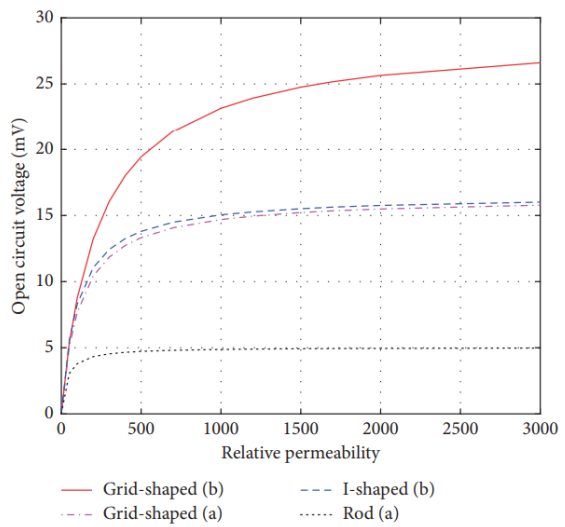


Figure 21 - Rod VS Dumbbell Comparison

Now with all pieces gathered the first prototype can be considered. The only question left is what output voltage range will be acceptable for the future power conversion stage the harvester will connect with. From Figure 1 the magnetic field input range is set from 1mT to 6mT, a multiplier of six, and the harvester device should be operational over the entire range. Assuming the output voltage will rise linearly, a starting output voltage range of 3V to 18V was decided on. Any lower and the input voltage would not be high enough to effect forward voltage drops of possible series diodes and any higher and the input voltage may exceed future component breakdown voltages.

Table 2 below shows the starting values and the dimensions to be varied during testing along with the final prototype calculations. The configurable portion includes values decided on from available components from sites like Digikey or Mouser. Other factors, such as the material permeability or the turns ratio 'N' were adjusted to fit the availability of parts and size of the harvester. One other design choice of note was the lack of ferrite end cap sizes tested, as they are a more limited item to buy off the shelf. One diameter of ferrite cap was used for all testing.

Table 2 – Prototype Calculations

Parameter	Unit	Value	Set/Configurable
Output Voltage_Low_Goal	V	3	Set
Output Voltage_High_Goal	V	18	Set
w	rad/second	376.9911184	Set
Bex_Low	T	0.001	Set
Bex_High	T	0.006	Set
Turns Ratio N	n/a	3000	Configurable
length_core	m	0.124	Configurable
diameter_core	m	0.0123	Configurable
width_cap	m	0.00254	Configurable
diameter_cap	m	0.0356	Configurable
material permeability μ_r	n/a	2000	Configurable
A (inner rod surface area)	m ²	0.000118823	Calculation
k	n/a	10.08130081	Calculation
d	n/a	0.980123747	Calculation
F	n/a	0.057901252	Calculation
μ_{eff}	n/a	17.13141305	Calculation
V_Low	V	2.302213859	Calculation
V_High	V	13.81328315	Calculation

With calculations complete a prototype of the harvester was assembled and measurements taken,

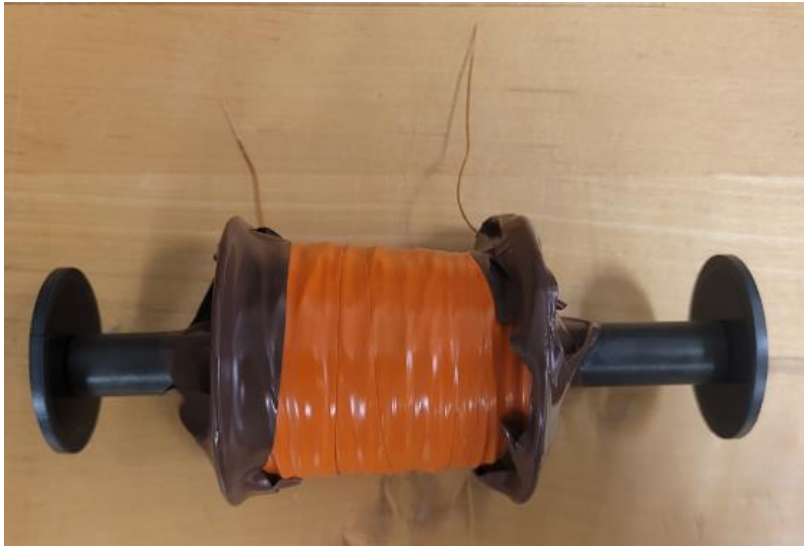


Figure 22 shows the prototype. The last factors to consider are the dumbbell end caps that were not included in the previous calculations. Measurements were taken to show a comparison of the output voltage induced into the coil with no caps, one cap, or two caps on each end; shown in Figure 23. Measurements show results consistently under the expected values on the rod design as seen in the calculated value of on

Table 2 of 2.3V at 1mT input and the measured value of 1.95Vac, likely caused by an array of non-ideal factors. These include an air gap between the winding and core increasing real cross sectional winding area, a non-ideal winding method that leaves air gaps between wires, windings that are further from the core because they are wound on a short spool, and the harvester being too long for test setup one to get the full magnetic field measured by the shorter sensor. All these factors combine to reduce induced voltage on the output. When comparing no caps to two end caps an increase of roughly 25% in voltage was seen. This could likely continue to increase with more caps if needed but, does not match over works simulated results.

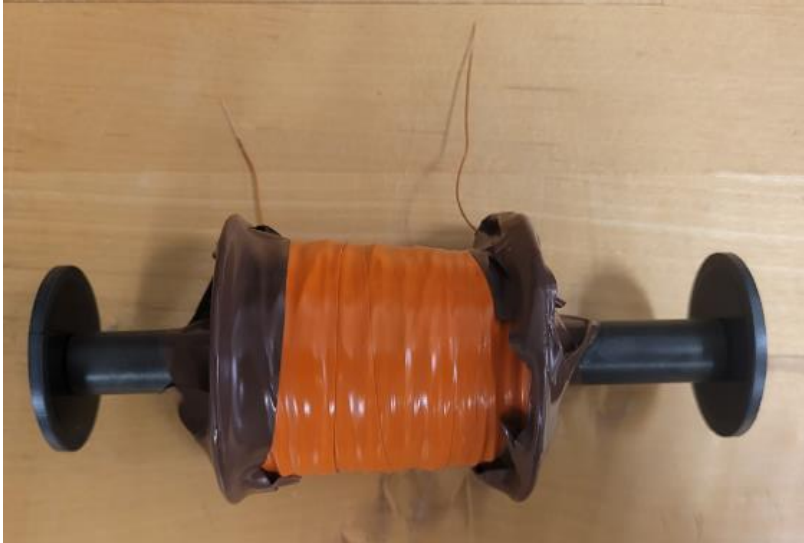


Figure 22 - Prototype Harvester

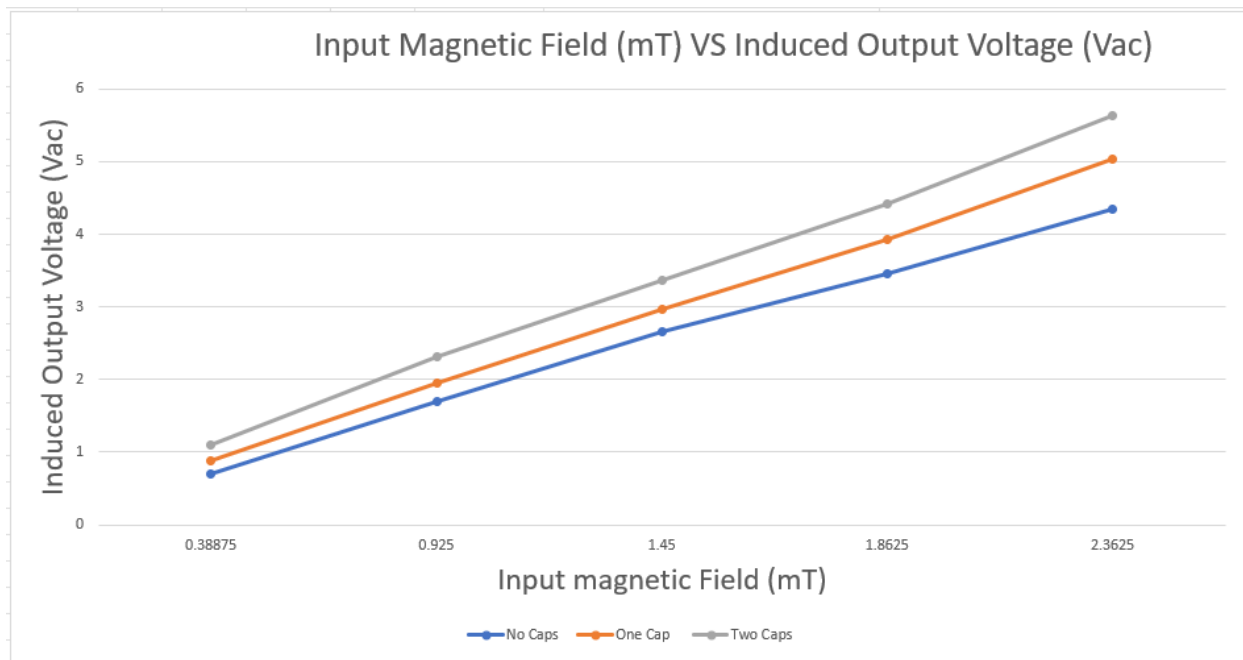


Figure 23 – Prototype Input Magnetic Field (mT) VS Induced Output Voltage (Vac)

Harvester Optimization Attempt

To optimize the harvester design, several dimensions have been changed. The main change has been a reduction in the core diameter from 1.24cm to 0.41cm, a nearly three times reduction, greatly increasing induced voltage. The inner rod core length was also reduced slightly from 124cm to 120cm due material constraints; however this does not greatly impact the result. The final change is the creation of a 3D printed core case as shown in Figure 24. The case greatly reduces the non-ideal factors mentioned before, while adding on the optimized core diameter. The case allows for protection with lids on either end to keep the ferrite caps from breaking and increases manufacturability by adding an easily spooled area for the winding and keeping the ferrite loading areas open. Figure 25 shows a comparison of the calculated and measure results of the new design.

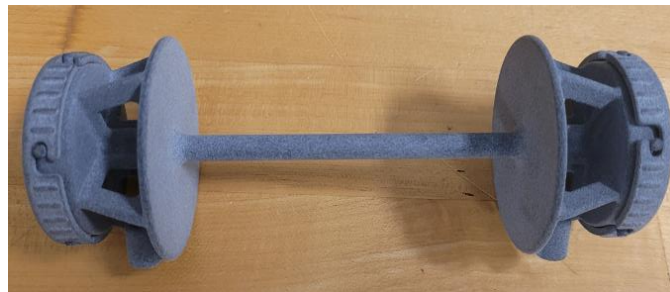


Figure 24 - 3D Printed Harvester Case

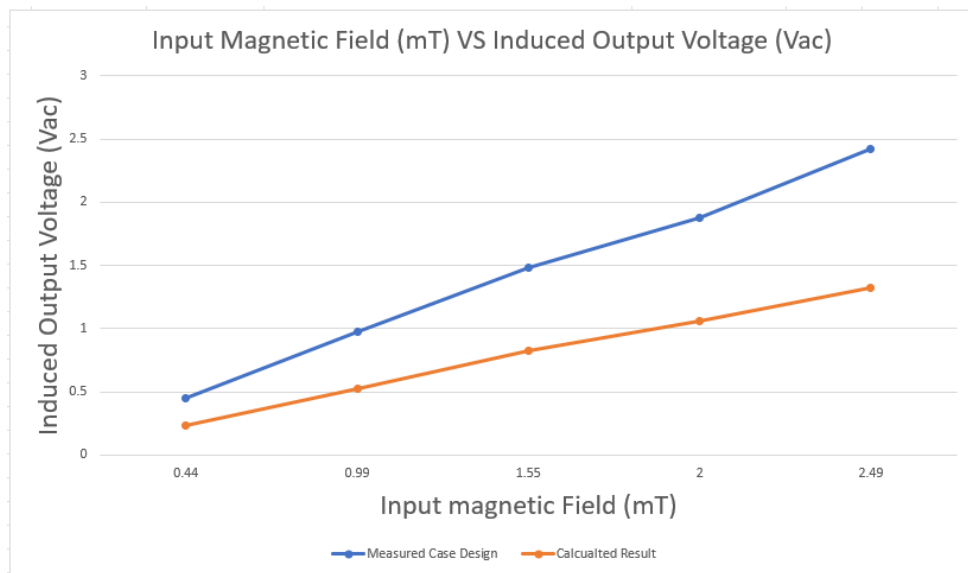


Figure 25 - New case Comparison

One other big difference is the change in turn windings. This was reduced from 3000 to 1500 to help reduce overall series resistance of the harvester, which can be seen as part of the reduction from 27.11 ohms to 4.4 ohms in Table 3. Reducing core diameter had a linear effect on changing maximum deliverable power and dissipated power within the harvester,

Equation 6 [4] and Equation 7 [4] were used to find these. The main benefit of the diameter reduction was a nearly ten times reduction in inductance, helping reduce component sizing needed on the future PCBA. The main drawback is the reduction in deliverable power, which must be considered as a trade-off.

Table 3 – Output power Comparison

Tests	Harvester Designs		
	Prototype	Optimized	units
Measured Inductance @ 60Hz	477	40	mH
Measured Resistance @ 60Hz	27.11	4.4	ohm
Measured Voltage @ 1mT Input	3.54	1	V
Max Delviered Power @ Measured Voltage From 1 mT Input	0.115562523	0.056818182	W
Power Dissipation Across Harvester	0.462250092	0.227272727	W

Equation 6 - Max Deliverable power (Watts)

$$P_{Max} = \frac{V^2}{4 * R_{Harvester}}$$

Equation 7 - Harvester Power Dissipation (Watts)

$$P_{Dissipation} = \left(\frac{V}{R_{harvester}} \right)^2 * R_{Harvester}$$

Version 2 Harvester Design and Mutual Inductance

One main addition made to the design was the addition of a secondary auxiliary winding to the case of the main power harvester. This auxiliary winding will output a clean sin wave of the magnetic field for control use and is needed due to the harvester also acting as the series inductance of the overall system, to be discussed. This auxiliary winding allows for a clean PPL control and much simpler MPPT control further on. The main concern with the secondary winding is the coupling effect between two windings. The main power windings will experience high frequency square waves from the circuit switching elements and this noise can be coupled into the secondary, interfering with the sampling done for control use. To prevent this a secondary coil was added, shown in Figure 26, with a reduced winding ratio and distance to prevent coupling. The ferrite core between them has also been kept separate by air, or the core case material.



Figure 26 - Final Harvester Core Structure

To find the coupling factor 'k' four measurements were taken. The Equation 8 [12] set shows how to find mutual inductance between two windings. 'M' represents the inductance between the two windings while 'k' is the percentage of signal that will pass from one winding to the other. L1 and L2 are individual inductance measurements at the switching frequency that noise is likely to come from. 'Laid' and 'Loppos' are inductance measurements with both attached in series, after measuring one way one windings polarity is reverse and measured again. The higher of the values is 'Laid' and the other 'Loppos' and plugged in to get the coupling factor. From Table 4 a coupling factor of 5.7% is found, which is acceptable for noise suppression.

Equation 8 - Mututal Inductance Set

$$L_{aid} = L_1 + L_2 + 2 * M$$

$$L_{oppos} = L_1 + L_2 - 2 * M$$

$$M = \left(\frac{1}{4}\right) * (L_{aid} + L_{oppos})$$

$$k = \frac{M}{\text{sqrt}(L_1 * L_2)}$$

Table 4 - Mutual Inductance Calculations

L1	0.000415
L2	0.0523
Laid	0.053
Lopos	0.05194
M	0.000265
k	0.056881

One issue found during testing was the core material not properly inducing a voltage at higher magnetic field levels. Once the harvester was ready to be tested an RC circuit was designed, based on Figure 27, that allows for maximum power transfer to the load. During this test it was noted that the version 2 harvester could not output the expected power. Figure 28 and Figure 29 show the testing results, and how the 1mT performed as expected, but the 2mT test did not. The cause of the phenomenon was not identified, but it was seen that the main cause was the smaller diameter used on version 2 compared to version 1. Other harvesters developed with similar size cores all had similar issues, showing that a larger core diameter was needed for the power range.

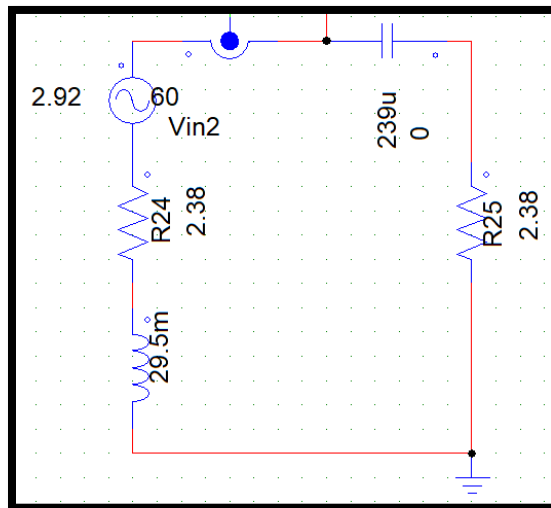


Figure 27 - RC Circuit Tester

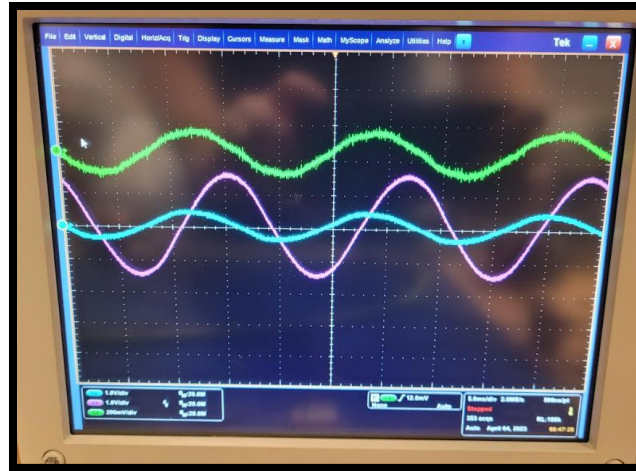


Figure 28 - 1mT Version 2 Harvester RC Circuit Test



Figure 29 - 2mT Version 2 Harvester RC Circuit Test

Version 3 Harvester Design

The version three harvester attempts to combine the benefits of version one and two. The sizing of core material was kept from version one, while the physical turns are placed directly on the core and reduced to only 500 turns. The end caps were then increased to improve the voltage range of the output. The result was a harvester capable of 1.4V to 8.4V over the operational range, with only 29.5mH of inductance and 2.38ohms of series resistance. The total volume of the core is increased to 35.188 cm³ due to the increased core diameter and extra end caps, giving a power density of 23.4 mW/cm³. Figure 30 shows the designed harvester during testing and Figure 31 shows the power comparison of version three harvester compared to harvesters from [3]. It should be noted that the paper referenced did not have the results at the magnetic field and induced voltage levels required for this design, so the end results were adjusted to account for both factors. This shows how the harvester needs to be customized for the intended magnetic field range. From the extrapolated chart its easy to see how the harvester must be designed for the correct magnetic field strength, otherwise subpar performance can occur. Most harvesters would still achieve a similar output power, but with widely different sizes and costs.



Figure 30 - Version 3 Harvester

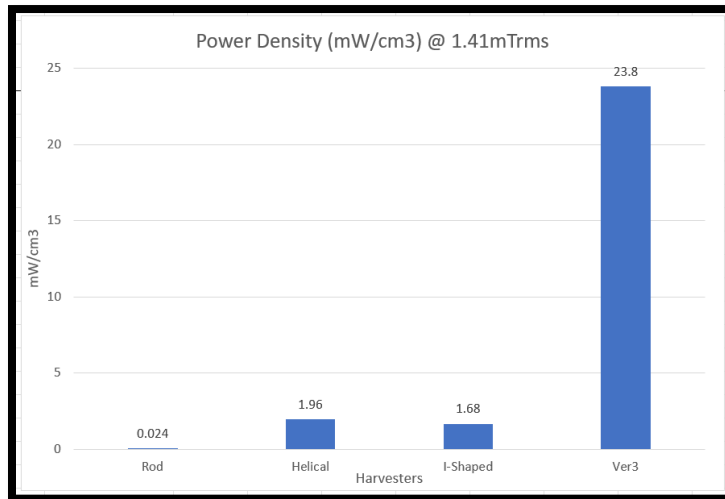


Figure 31 - Output Power Comparison

Harvester Design Conclusions

From previous tables it's found that there are clear trade-offs when changing the harvester dimensions. By reducing inner rod diameter, the total power transferred also gets reduced proportionally. Table 5 shows the output power possible from both designs at maximum magnetic field input and that only about one watt of real power can be transferred with these designs. While the larger diameter harvester could be optimized to improve output power somewhat, it would not make a large impact without higher magnetic field input. The trade-off for much lower inductance for slightly lower transferred power is acceptable for moving forward and the version 3 harvester is used for progressive work.

Table 5 - 6mT Output Power Calculations

Tests	Harvester Designs			units
	Ver 1	Ver 2	Ver 3	
Measured Inductance @ 60Hz	477	40	29.5	mH
Measured Resistance @ 60Hz	27.11	4.4	2.38	ohm
Measured Voltage @ 2mT Input	7	2	2.96	V
Calculated Delivered Power @ 2mT	225	113	460	mW

If more time was allowed for harvester design new measurements of MV AC Drive would be taken to try and find a higher magnetic field spot for harvesting. The inner rod diameter would be increased somewhat to allow for slightly higher power transfer at the expense of total inductance value along with better centering of the windings away from the cap ends. Also, larger diameter caps would be sourced to increase magnetic field collection and would be thickened to better trap the demagnetization effect on the ends. The power level seen is enough to supply either intermediate use or continuous use of low power circuitry and will be factored in for future designs.

Ch 3 – Max power Transfer Theory and Application in Harvester System

Maximum Power Transfer Theory with Impedance Matching

With the design of the harvester an inductive load has been created. Figure 32 shows a schematic example of the harvester, represented by R_S and L_S , along with a load R_L and an extra compensation capacitance C_S . When C_S equals zero and L_S is some value then the circuit is considered inductive (lagging) and when C_S equals some value and L_S is zero then the circuit is capacitive (leading). This is shown in Figure 33 where the area under both curves represents the total output power. The purely resistive circuit represents a power factor corrected circuit that maximizes output power. This is derived into the equations shown in Equation 9. Here X_S and R_S and the source inductance and resistance while

X_L and R_L are the compensation capacitor and the output resistance. Simplified, these show the maximum output power for a 2.92Vac source and 2.38ohm output resistance load, with perfect power factor correction, can be seen to be 455mW. In this case there is also a total of 455mW lost across the source resistance, meaning a total of 910mW is supplied to the circuit while only 50% makes it to the output. If the load impedance was reduced then the output power and overall efficiency would decrease, while if the load impedance were increased then the overall output power would decrease, but the overall efficiency would increase and thus less power lost in the source. Figure 34 shows the comparison of output power to efficiency and resistances, when looking at the lesser resistive matching scheme.

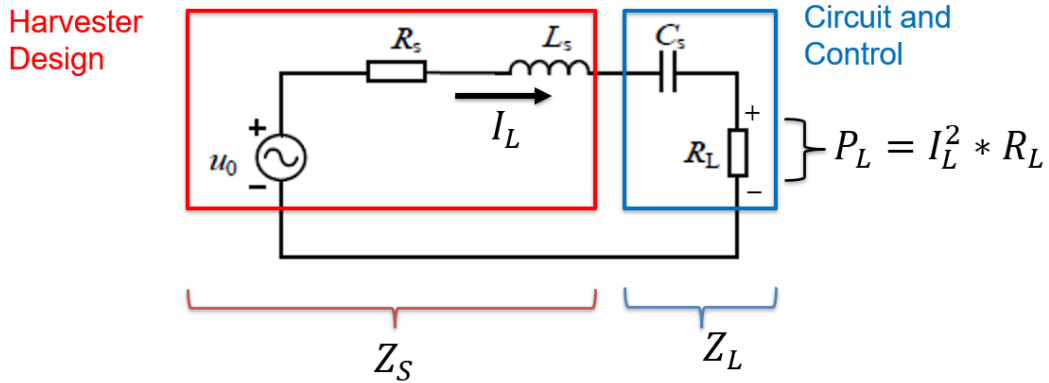


Figure 32 - Inductive Compensation

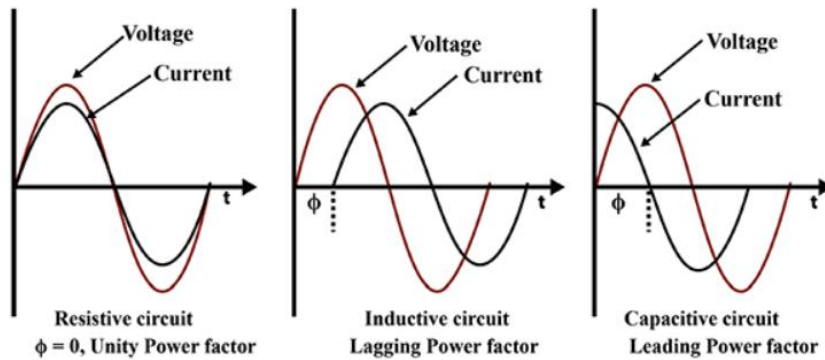


Figure 33 – Power Factor Correction Example

Equation 9 - PFC Equations

0: $X_L = 2 * \pi * freq * L$, $X_C = \frac{1}{2 * \pi * freq * C}$ 4: $\frac{\partial}{\partial R_L} P_L = \frac{V_{IN}^2}{2} * \frac{g * f' - g' * f}{g^2}$

1: $P_L = \frac{V_{IN}^2 * Real\{Z_L\}}{2 * (Z_S + Z_L)^2}$ 4.1: $f = V_{IN}^2 * R_L$

2: $P_L = \frac{V_{IN}^2 * R_L}{2 * (Z_S + Z_L)^2}$ 4.2: $g = \left(\sqrt{R_S^2 + (X_L - X_C)^2} + R_L \right)^2$

3: $P_L = \frac{V_{IN}^2 * R_L}{2 * \left(\sqrt{R_S^2 + (X_L - X_C)^2} + R_L \right)^2}$ 4.3: $f' = V_{IN}^2$

5: $\frac{\partial}{\partial R_L} P_L = \frac{V_{IN}^2}{2} * \frac{\left(\left(\sqrt{R_S^2 + (X_L - X_C)^2} + R_L \right)^2 * V_{IN}^2 - \left(2 * \sqrt{R_S^2 + (X_L - X_C)^2} + 2 * R_L \right) * V_{IN}^2 * R_L \right)}{\left(\sqrt{R_S^2 + (X_L - X_C)^2} + R_L \right)^4} = 0$

6: $\frac{\partial}{\partial R_L} P_L = \frac{V_{IN}^2}{2} * \frac{R_S^2 + (X_L - X_C)^2 - R_L^2}{\left(\sqrt{R_S^2 + (X_L - X_C)^2} + R_L \right)^4} = 0; \rightarrow$ **Conditions For Max Power**
 $X_C = X_L$ AND $R_S = R_L$

*Inductance and capacitance cancel out
*Input resistance and load resistance match

7: $V_{IN} = I_L * (Z_S + Z_L)$

8: $I_L = \frac{V_{IN}}{(2 * R_L)}$, IF $R_S = R_L$ AND $X_L = X_C$

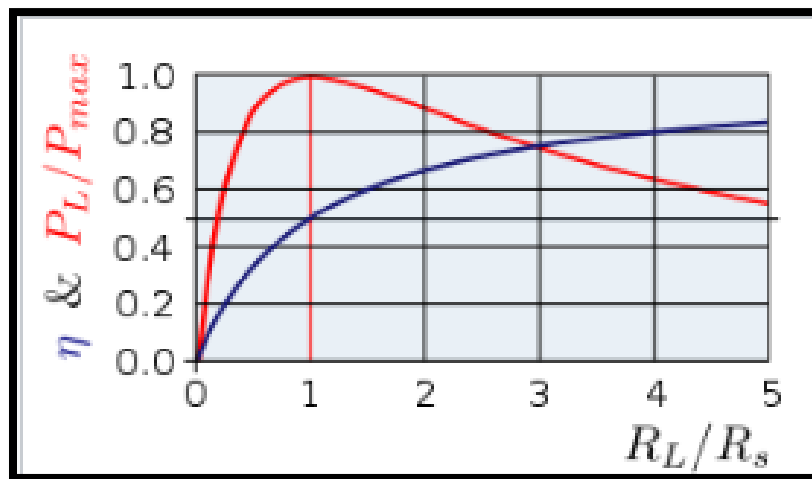


Figure 34 - Maximum Power Theory Comparison

If instead the inductance or capacitance were not corrected, then the power factor would be less than one. Take the previous values of a 2.92Vac source and 2.38ohm output resistance, but now add a 29.5mH inductance in series. This gives a X_S of 11.12 and using the same equations from before, gives a max delivered load of 69mW instead of 455mw. To correct this a series capacitance X_L can be sized to the same 11.12 as the inductor to cancel it out. Following the equations, the capacitance comes out to be 239uF and achieves a power factor of one. For the planned circuit the control will monitor the total power levels to maximize power by connecting the input inductor harvester with the output capacitors to create a resistive circuit to maximize power. The four switches will connect these two elements for differing periods of time so that the physical inductor and capacitors do not have to be specific values but can instead be connected for different intervals of time to create the same effect. Equation 10 shows a full example using the derived proof for MPTT, which matches future simulation power levels used. Noticed that values are not exactly the same, as the simulation results depend on measurements 'by eye' or cursors for those results. Regardless, these results are extremely close and well within any margin of error.

Equation 10 - MPTT Example

2mT Input	
0: $IF R_S = 2.38ohms, L = 29.5mH, V_{in} = 2.92V, freq = 60hz$	4: $PF = \frac{P_{L_{Calibrated}}}{P_{L_{Max}}} = 100\%$
1: $P_{L_{Max}} = \frac{V_{in}^2}{8 * R_L} = \frac{2.92^2}{8 * 2.38} = 447mW$	4.1: $PF = COS(\theta) \rightarrow \theta = COS^{-1}(PF)$
2: $X_L = 2 * \pi * freq * L = 11.12$	4.2: $\theta = COS^{-1}(1) = 0^\circ$
2.1: $C = \frac{1}{2 * \pi * freq * X_C} = 239uF, \quad \text{WHEN } X_L = X_C$	5: $PF = 100\%, \quad \theta = 0^\circ$
3: $P_{L_{Calibrated}} = \frac{V_{IN}^2 * R_L}{2 * \left(\sqrt{R_S^2 + (X_L - X_C)^2} + R_L \right)^2} = 447mW$	6: $I_L = \frac{V_{IN}}{2 * R_L} = 613mA$

To prove the theory true several simulations are performed. Figure 35 was created to show the MPTT theory with and without compensation. Figure 36 shows the voltage and current waveforms without any capacitor compensation, causing the sinewaves to be out of phase and reducing delivered power greatly. Figure 37 shows the maximum delivered power to the load of the non-compensated circuit to be 69mW. Figure 38 and Figure 39 in turn show the results of adding in the correctly calculated capacitor compensation. Instead of 69mW delivered a max of 455mW is delivered.

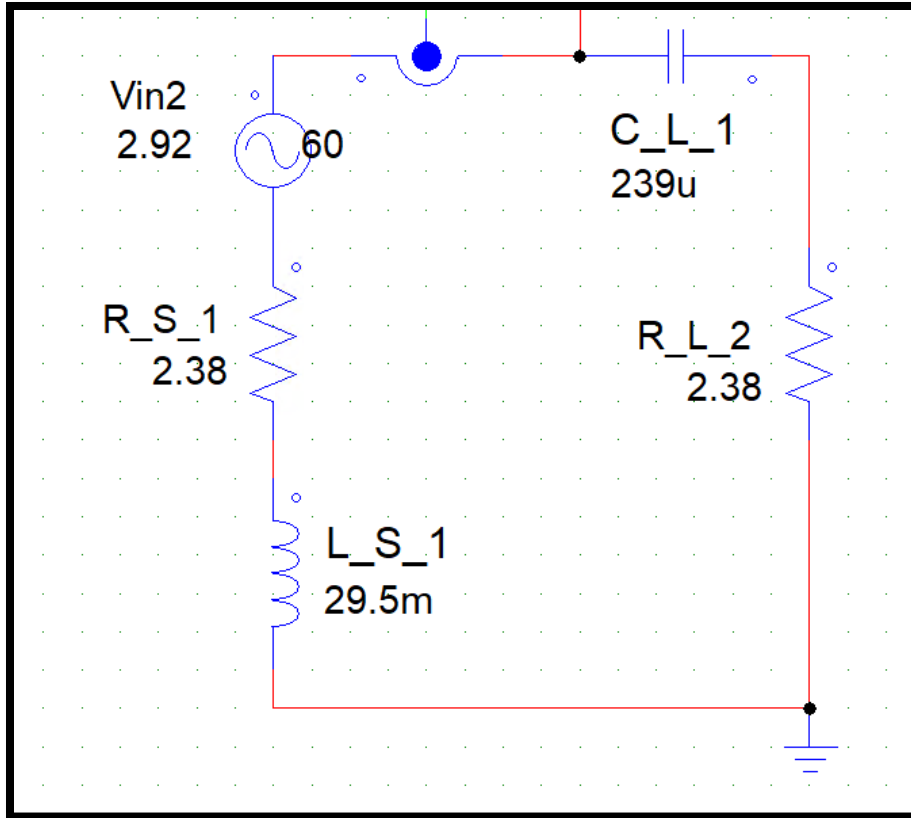


Figure 35 - PSpice Compensation Circuit

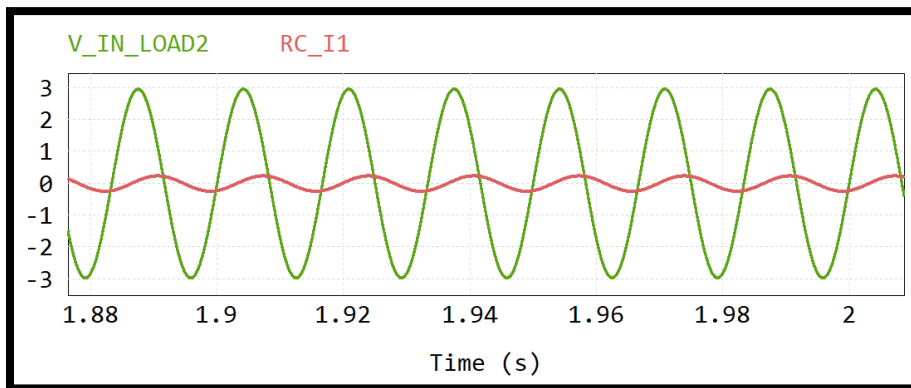


Figure 36- No Compensation Waveform

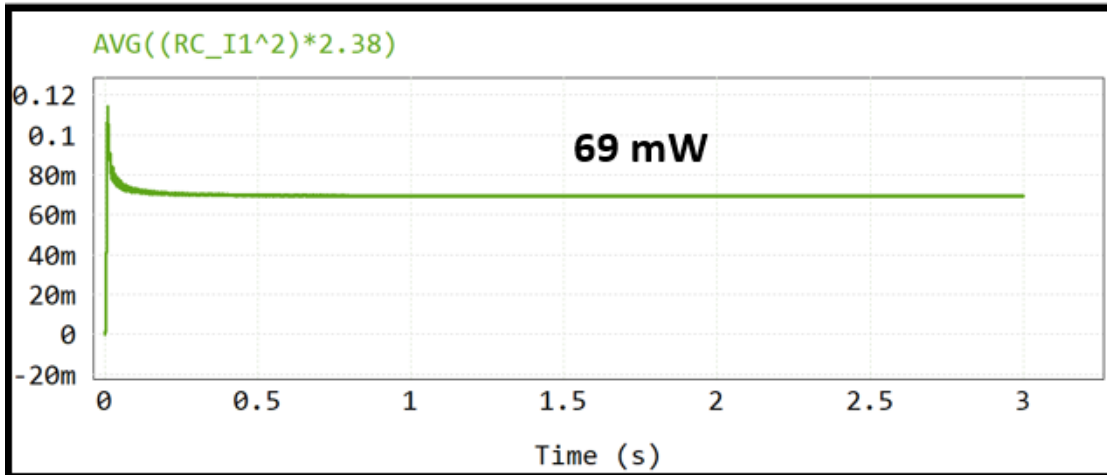


Figure 37 - No Compensation Delivered Power

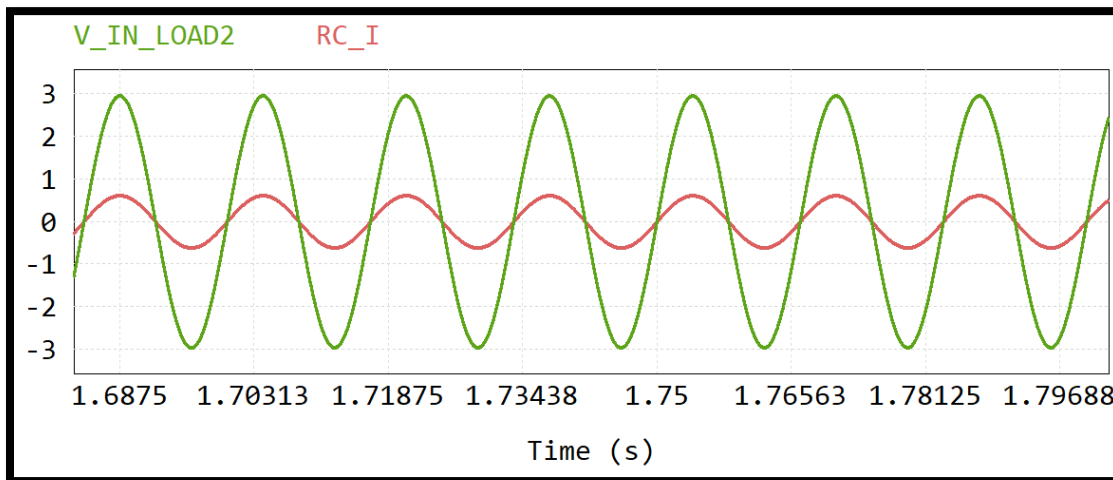


Figure 38 - Compensated Waveform

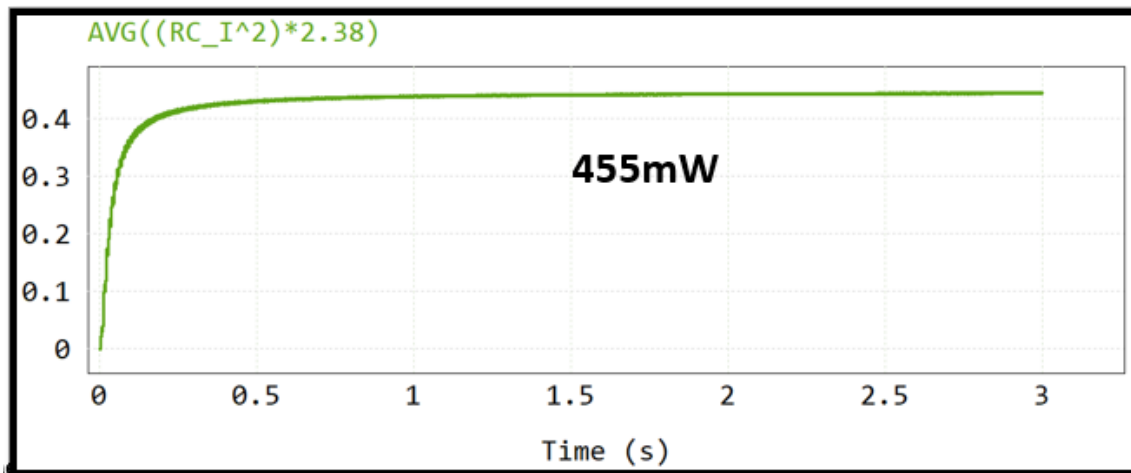


Figure 39 - Compensated Delivered Power

To confirm the theory, simulations and real world match a comparison was done using the calculated delivered power and a simple series RC circuit. This circuit was made with the same values as in the compensated series RC circuit from Figure 35. The results are shown in Figure 40 and show a matching result, with the real measurements being slightly higher likely due to a high input power than expected. The series RC measurements are then used as the 'gold standard' for all future efficiency calculations.

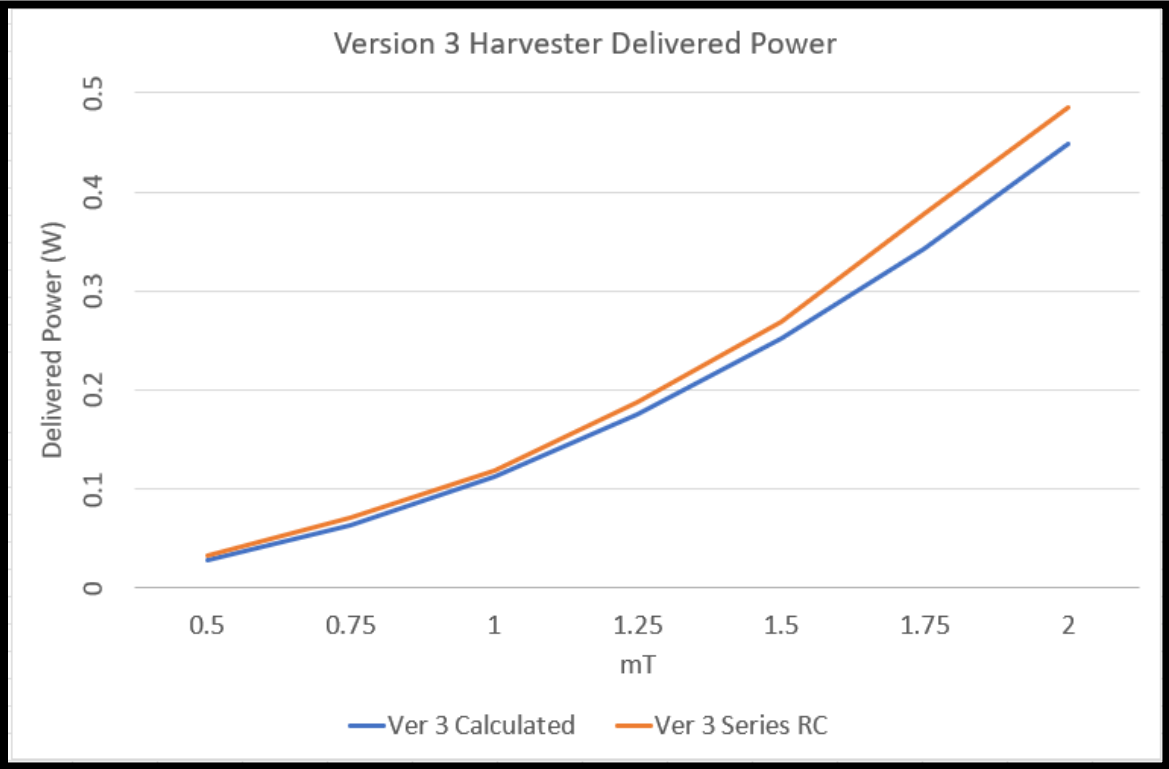


Figure 40 - Series RC Circuit Power Comparison

Ch 4 – Power circuit topology

Passive Rectification and Charge Pump

As the input has been designed as a single-phase inductive AC source, topologies were reviewed to allow for AC to DC conversion from this source. The most obvious option is a passive rectifier using four diodes called a full bridge rectifier; shown in Figure 41 [13]. This option is popular in industry as a reliable AC to DC conversion method but lacks the benefits of an active solution. The main benefit is the passive nature of the bridge rectifier not needing any active control while the main drawback would be lower efficiency from the forward voltage drop across the diode and that voltage drop at lower voltages can drastically reduce output power. Another drawback in this case is the lack of PFC (power factor correction) that could be achieved using active switches with no forward voltage drop. PFC is necessary to allow for MPPT (maximum power point tracking) which was an earlier requirement for this project. While not chosen for the final design, this was used to validate the harvester calculations and bench test power source. Figure 42 below shows the prototype created to validate the magnetic field harvesting calculations while Figure 43 shows the schematic of this device.

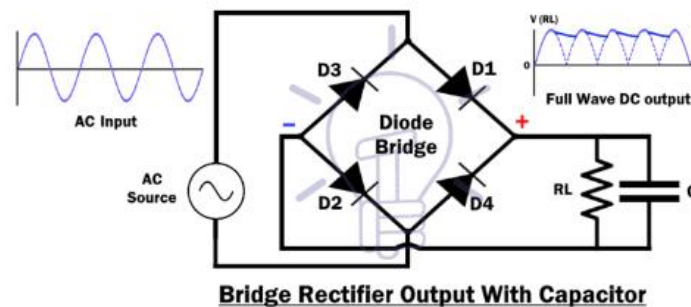


Figure 41 - Example Passive Rectification

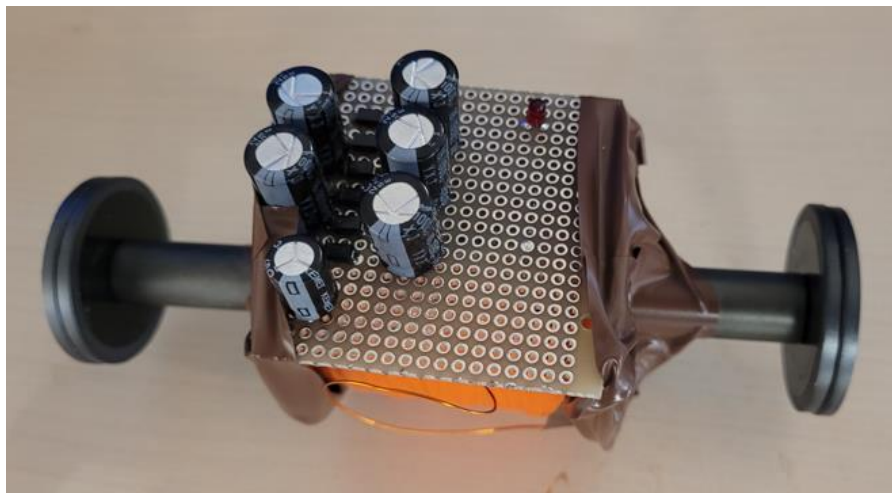


Figure 42 - Charge Pump Harvester

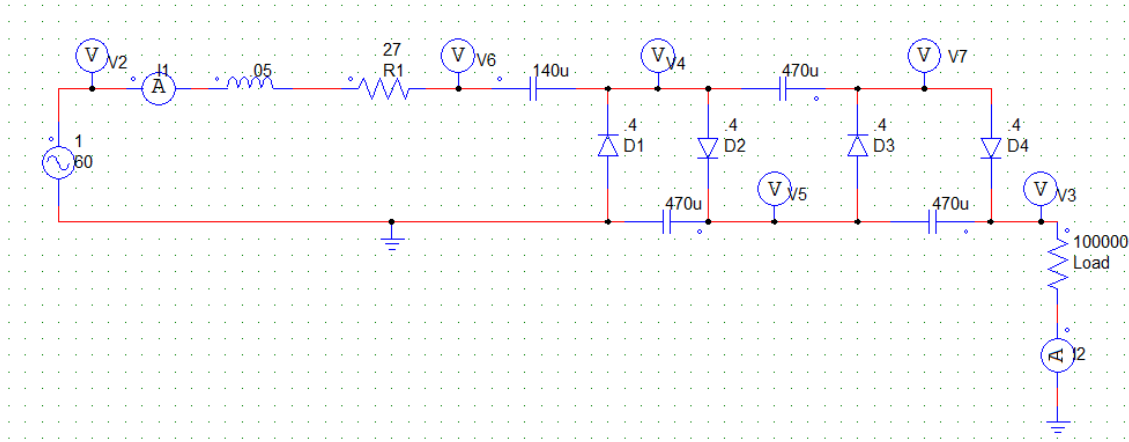


Figure 43 - Charge Pump Schematic

Another addition to this circuit, not used in the final design, is a charge pump to increase the input voltage to a usable level for bench testing. Due to the low magnetic field generated by the variac AC source and therefore low voltage generated by the prototype magnetic harvester, a charge pump is used to increase the output voltage to a usable level for validation. Charge pumps are low efficiency solutions that can increase a voltage by stacking capacitors in series and charging each one during the positive and negative cycles of the AC source. The diodes prevent the discharge of the capacitor during the opposite voltage cycle but end up reducing the output voltage by their forward voltage drop. Figure 44 below shows a simulation of the output voltages created by the charge pump and shows how the final output voltage V3 is first boost and then reduced by a factor of the diode forward voltage drop when compared to the input voltage of V2; these are based on the schematic shown above in Figure 43. Each subsequent charge pump level will double the voltage, shown by V5 as the first boost and V3 as the second boost.

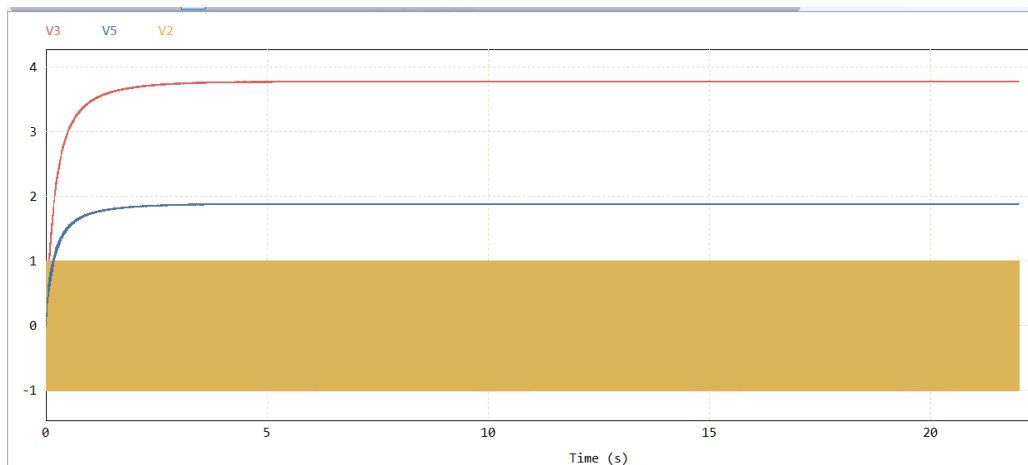


Figure 44 - Charge Pump Output Voltages

Active Rectification

From previous work it is seen that both resistive and capacitive matching is required for any topology chosen. Figure 45 shows two options for topology selection, the left having a single passive line frequency leg and only one switching leg. Because one leg is purely passive, it cannot achieve capacitive cancellation and will not work for full MPTT operation. The second has both legs switching and can either switch one at line or both at carrier frequency. A similar approach was used in [7] called a Totem-Pole Bridgeless PFC, shown in Figure 46. This topology has one leg dedicated to line frequency and the other toward carrier frequency. In this design the line frequency uses slower silicon mosfets that mostly see conduction losses, while it uses silicon carbide mosfets for the higher carrier frequency to reduce switching losses. This paper was designed for a three-phase system and was able to justify the different component types as the line frequency allowed for easier sampling of the input voltage and current values. For this projects single phase system, it is more desirable to have a simplified BOM and thus uses the same mosfets and gate drivers for all switches. As the switches and drivers are often sized for the switching frequency they run at, it is not ideal to have one leg running at line frequency. Because of this an alternative to measuring the input voltage and current is needed and solved using the auxiliary winding previously discussed.

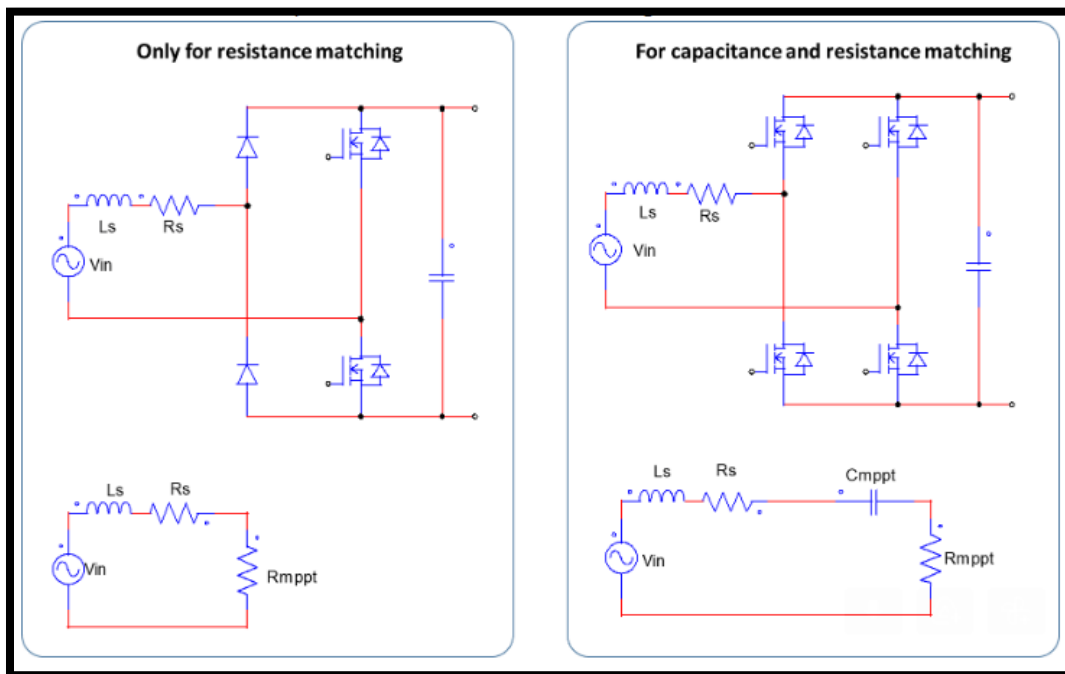


Figure 45 - Topology Comparison

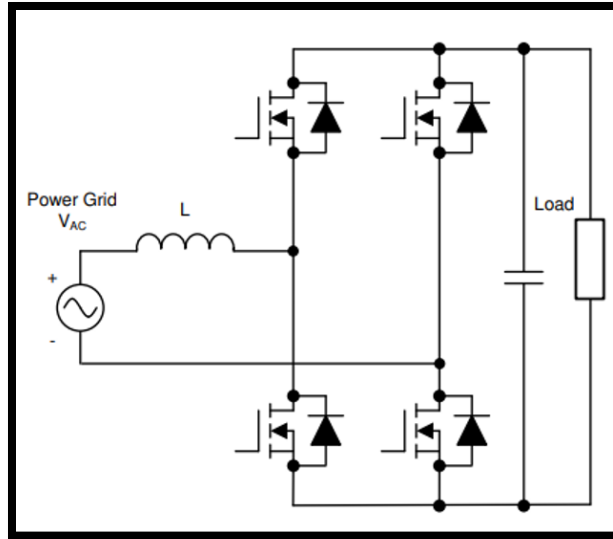


Figure 46 - Totem Pole Bridgeless PFC

During the transition between mosfets turning on and off both mosfets are set to the off state, creating a floating point between the mosfets. During on and off states this middle point between the mosfets are either connected to the DC bus voltage or ground as they act as pull-up or pull-down switches. The 'Bridgeless' aspect come from the replacement of the passive diode rectifier, seen in previous sections, with active switches that can greatly increase efficiency by removing the forward voltage drop across diodes. The 'PFC' comes from the switches ability to turn on and off to perfectly match input inductance with output capacitance and remove the phase difference between input voltage and current, therefore maximizing output delivered power. Figure 47 [7] shows an example of the left leg switching while the right leg stays in the static off position, where the top switch stays on and the bottom switch stays off. By switching only the left leg, the power flow can either build in the inductor, raising the output voltage, or be passed to the output to deliver power. This process changes back and forth based on the input voltage polarity.

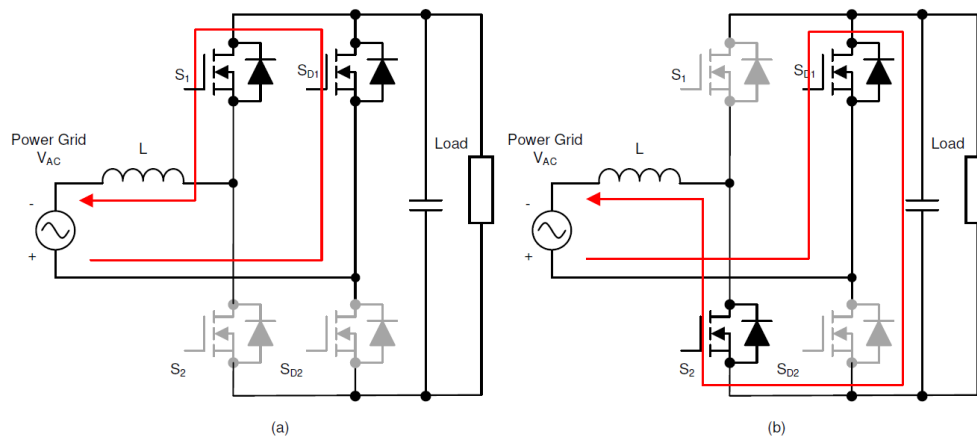


Figure 47 - Example TP-PFC Switching

Chosen Topology

The topology chosen, previously mentioned [7], is an active rectifier circuit. The circuit accepts an AC voltage and outputs a rectified DC voltage of either higher or lower voltage than the input. In-line with the input voltage source is a series inductor that allows current to build up and be passed to the output capacitor based on the control logic. This build up is dependent on the duty cycle of the individual switches and directly controls the output voltage. The four active switches also allow for PFC to occur, better balancing the input leading inductance with the output lagging capacitance and increasing power delivered. Figure 46 shows the base design of this topology while Figure 48 shows the modified topology for this work. Figure 49 shows how the topology is seen from the max power transfer theory viewpoint. For this the harvester contains the source, a resistance and an inductance. The rest of the circuit is the relative capacitance and resistance caused by the switches, capacitors and the actual load.

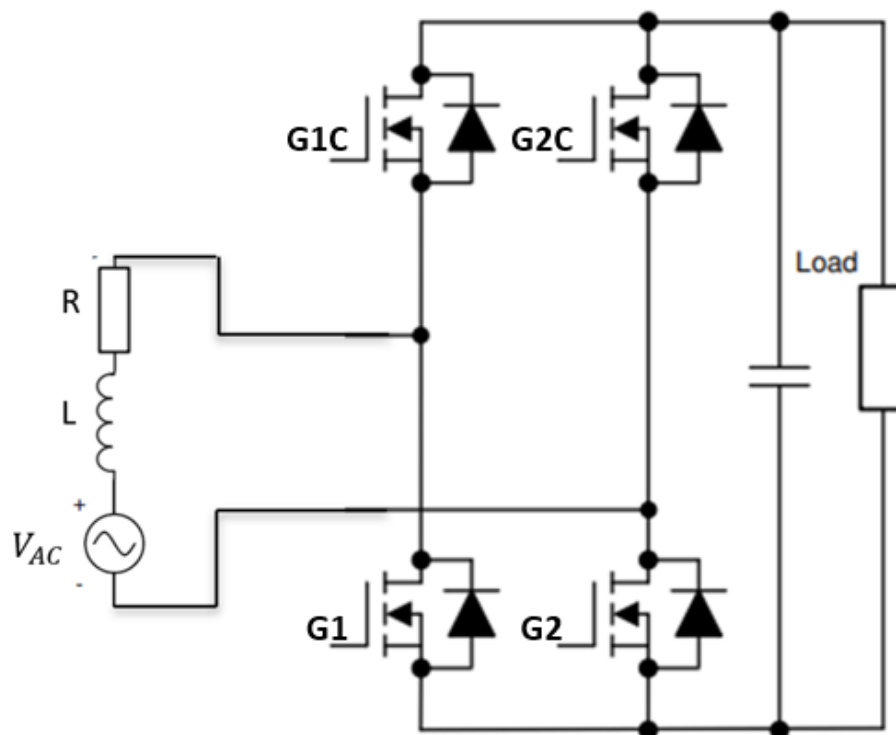
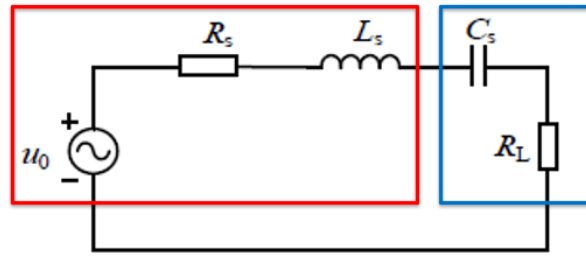


Figure 48 - Harvester Circuit

The key difference to note is the combining of the voltage source into the in-line inductance. By combining these the ability to sample input voltage and current using the previous method no longer exists. Figure 50 [7] shows the previous method of sampling, using the in-line inductance to filter out the noise from the switching events. Without this filter the ADC sampling rates are too low to differentiate the noise from the real signal. Figure 51 shows how the switching noise can be coupled into an otherwise clean sine wave and distort the signal. The ADC sampling rate is likely to be lower than the noise, meaning the sampled waveform will not show short peaks, but often longer distortions, deteriorating the controls' ability to function. To prevent this both hardware and software filters are implemented to reduce the noise reaching the ADC sampling as well as changes mentioned in the harvester design to reduce magnetic coupling as much as possible.

Harvester
Design



Circuit and
Control

Figure 49 - MPTT Relative Circuit

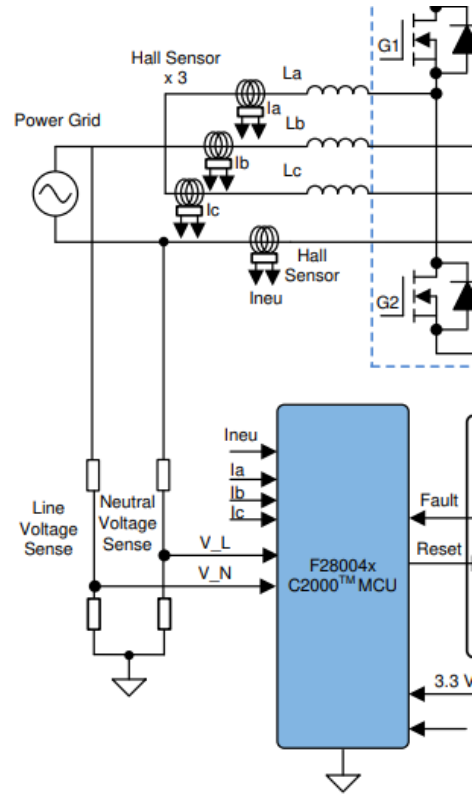


Figure 50 - Previous Sampling Method

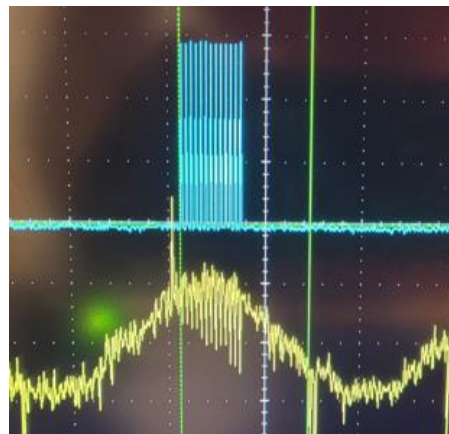


Figure 51 - Coupled Noise

For control of this topology the series RC circuit results can be reviewed. When the harvester is loaded the induced input voltage can no longer be measured. Instead, the voltage becomes 'V_RC' which is the overall resistance and capacitance voltage that the harvester sees on the series RC circuit. While the active rectifier does not strictly see this resistance and capacitance, with proper control of the mosfets the same performance can be replicated. Figure 52 shows the series RC circuit and the active rectifier relationship through V_RC while Figure 53 shows a simulation of how correct control of the active rectifier can replicate the series RC V_RC waveform. This represents a correct tuning of the modulation to achieve MPTT, as the series circuit was crated as perfectly tuned MPTT circuit.

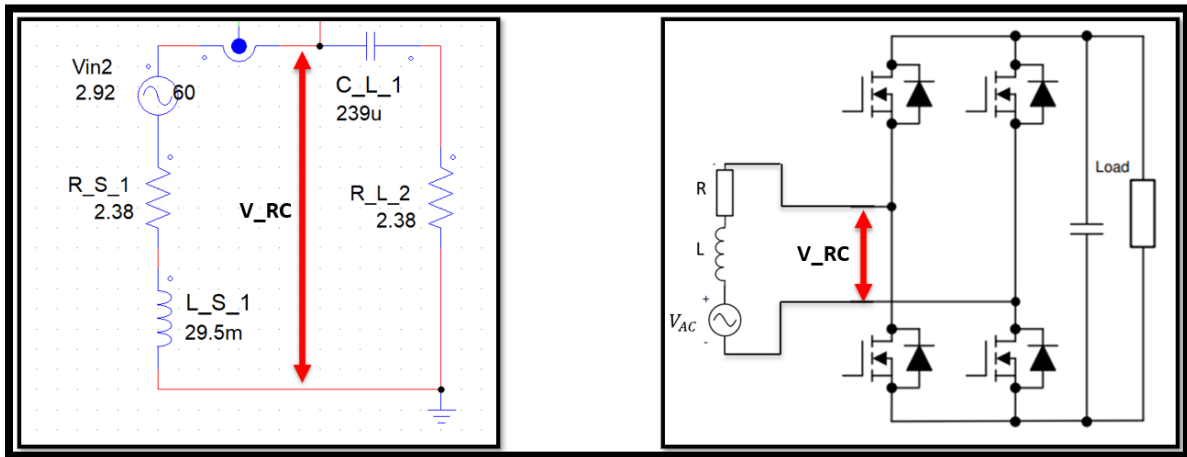


Figure 52 - Series to Active Rectifier Relationship

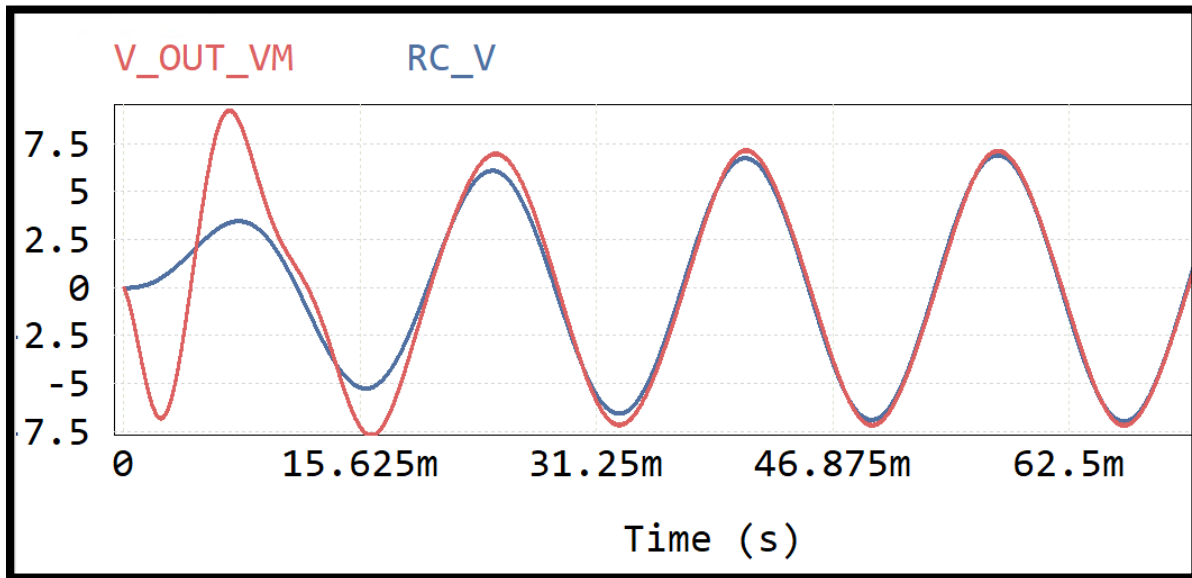


Figure 53 - Series RC VS Rectifier Modulation Signals

Sensor Circuit Modifications

It is seen from Figure 50 [7] that the control for this topology originally used the input voltage and current to calculate maximum power to control the circuit. With the in-line inductor now acting as the source itself this is no longer possible. The measured voltage has changed from a sine wave into a square wave without the inductor to filter out the switching noise. The input current was also measured using a hall effect sensor, detecting the changing magnetic field from the current passing through. This is no longer possible as the device will operate in a high magnetic field, distorting any readings. Both values are needed for MPPT calculations and alternatives must be found. Besides the previous two additions, a third addition is needed for the auxiliary winding. The measurement from this winding will be an AC signal, but the ADC can only read in positive signals of a specific range. DC offset and range limits must be added to make the auxiliary winding read correctly.

The first sensed value needed is input voltage. Ideally this would be the exact AC sine wave from the magnetic field that could be monitored for the rise and fall in value to determine if MPPT is being achieved. However, this value is impossible to sense as there is no longer a filter between the input and switching node. Instead, the auxiliary winding is used to take the main windings input voltage measurement. By knowing the ratio of the two windings turns, and placing them in line with one another, an accurate input voltage can be measured from the non-loaded auxiliary winding.

The second value needed is the input current. This current can be sensed with some difficulty. Two normal methods include a hall effect sensor, which monitors the magnetic field around the trace to give an accurate magnetic field measurement. This method is used in the previous work but, for a device intending to be used in high magnetic fields it is possible this sensor would give unreliable readings and would not be trustworthy. The second option would be a simpler current sense resistor, where the voltage on both ends of the resistor is measured and converted to current. While this method is possible, alone it is not enough. The switching frequency of the rectifiers creates a 30kHz square wave with an amplitude several magnitudes higher than the intended measured signal, making any sampling of the signal difficult. Samples will occur that catch either the end of a square wave or the real current itself, creating large discrepancies in the ADC measurement. Figure 54 shows the simulated current measurements. The blue and red signals are the ends of the sense resistor while the green signal is the real current. The red signal is nearly completely overlapped by the blue signal and only visible when zooming in on Figure 55. Even when sampling at 100kHz the likelihood of mis-sampling is too great and will not be reliable.

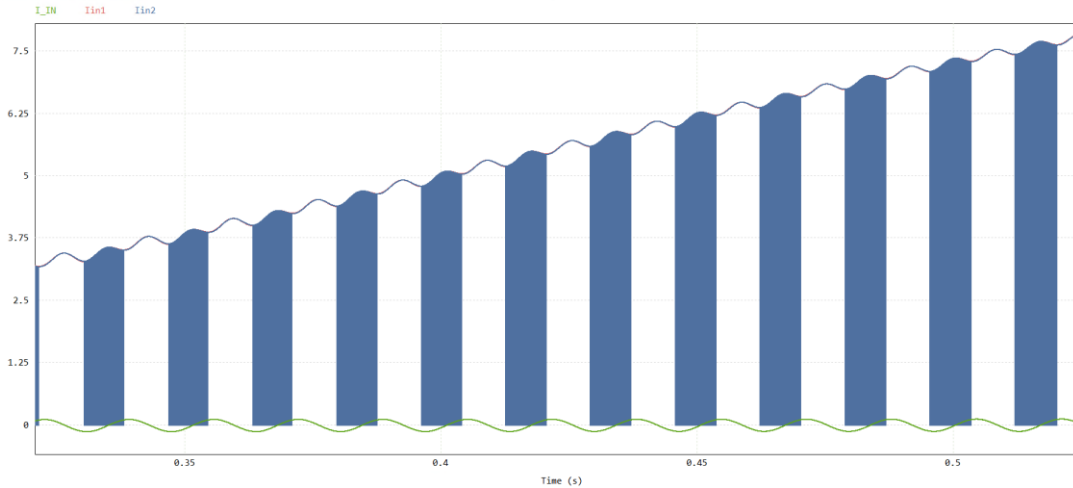


Figure 54 - Current Sense Resistor Measurements

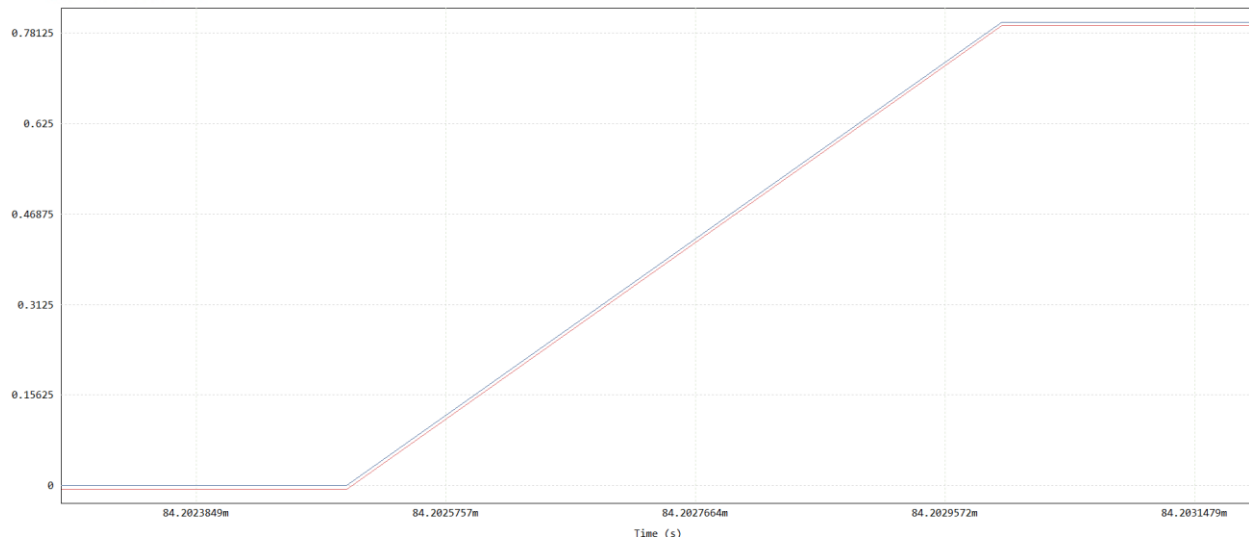


Figure 55 - Current Sense Resistor Measurements Closeup

Figure 56 shows the method to filter these signals for use. An LMP8601 comparator is used which has built in CMRR rejection, filter tuning to the 3rd order, offset voltage adjustment, and works within the range of the circuit design. Figure 57 shows the current sense resistor and the nets that connect it to the comparator. Figure 58 shows the internals of this part and how a series 100kohm resistor already exists. By adding a capacitor to local ground, a low pass filter is created and can be tuned for maximum noise rejection. The capacitance chosen is 100pF and when combined with the internal 100kohm resistor creates a corner frequency at 15.9kHz. This value was tuned to allow for enough filtering of higher frequency signals caused by the 10kHz switching square wave while also causing the lowest amount of delay to the ADC sampler. Equation 11 shows the formula used to tune this value.

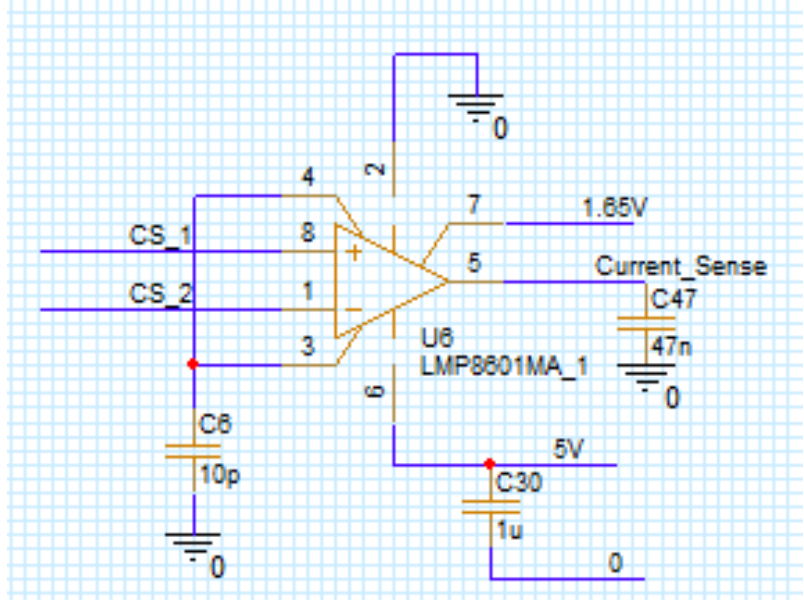


Figure 56 - LMP8601 Current Sense Comparator

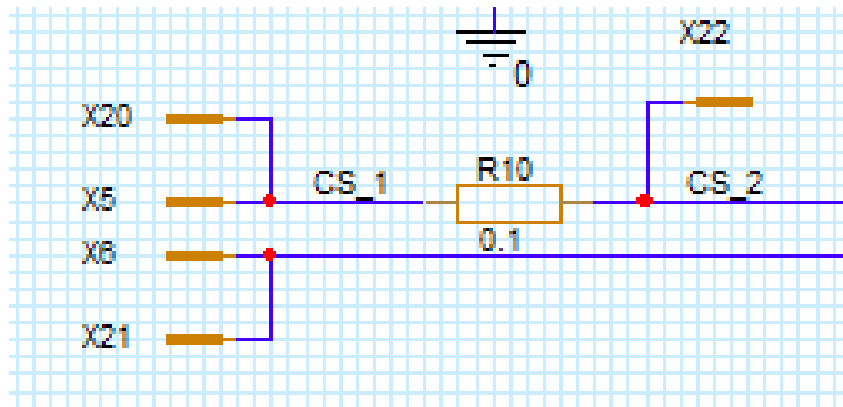


Figure 57 - Current Sense Resistor

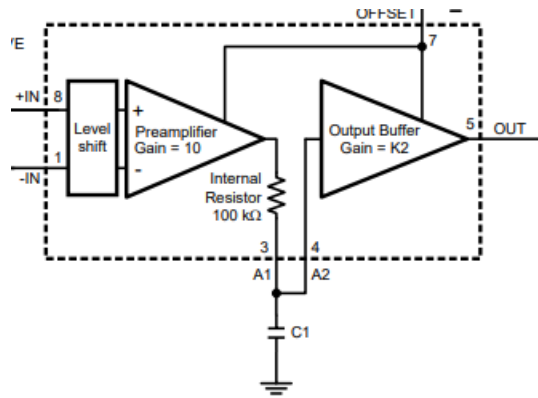


Figure 58 - LMP8601 Tuning Method

Equation 11 - Low Pass Filter Corner Frequency

$$f_c = \frac{1}{2 * \pi * R * C}$$

As previously mentioned, magnetic coupling between the main and auxiliary windings allows noise to pass from the switching events to the clean sine wave measured from the input magnetic field. To reduce this noise further a low-pass filter is added between the measured auxiliary input signal and the ADC sampling pin. This filter is tuned to provide maximum filtering while also reducing the added delay time. Added delay from hardware or software filtering will delay the switching events, causing lower power transfer. Figure 59 shows filter in schematic view along with a resistor divider that boosts the end voltage by 1.65V. The boosted voltage is needed as the future ADC sampling can only accept values of 0V or higher and the auxiliary signal will naturally be a sine wave signal that goes negative. Boosting the voltage to a mid-point of 1.65V will force the signal to always stay positive. 1.65V works because a future ADC will have a voltage limit of 3.3V that can be sensed, and the auxiliary winding will have a maximum value of 1.5Vac_pk at maximum load. This gives the auxiliary input a range of 0.165V to 3.15V at the ADC input, which is within measurable range.

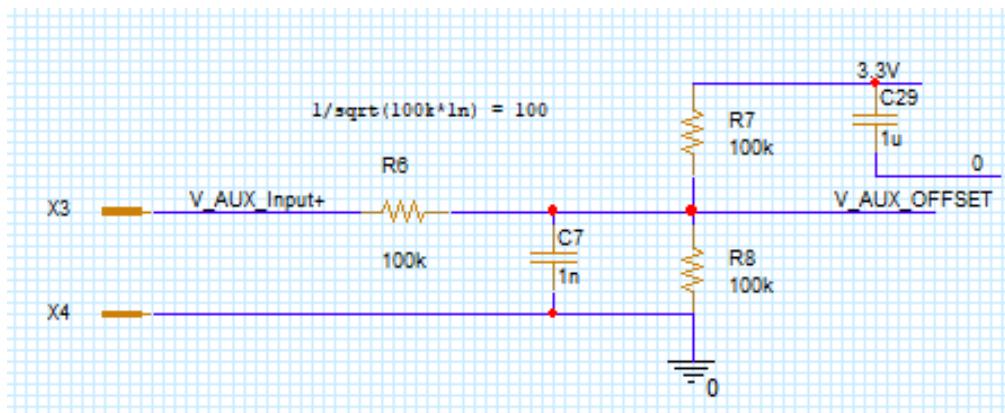


Figure 59 – Aux Filtering and

Gate Driver and Mosfets

To correctly switch four mosfets a gate driver system is needed. The topology calls for two legs of switches, two on each leg, totaling four switches. The NCP3420 was chosen as the gate driver due to its matching qualities to the mosfets used in the design. It is capable of driving both the top and bottom switches of one leg; known as the high-side and low-side switches. Notable features include a wide input range from 4.6V to 13.2V, ability to drive a 3.3nF load at 1MHz frequencies, and operates off a simple low power PWM signal. It also controls the deadtime between both switches and will wait a certain amount of time between the turn off of one to make sure it is fully off, as seen in Figure 60. Due to the high-side of the switch being referenced to the neutral point of the leg instead of ground a normal 12V gate signal will not turn on the mosfet correctly. To solve this issue the drive also includes a bootstrapped circuit referenced to the switching node through a bootstrap capacitor, as shown in Figure 61. The capacitor builds up a voltage equivalent to the switching node value which then gets added to the 12V input reference to drive the high-side switch. The capacitor is charged by the diode that only lets power pass in one direction. The value of this capacitor is recommended to be 1uF and this value was kept, but it can be precisely sized for future work if capacitor sizing or switching speed needs change. With this addition, a single driver can control both the high-side and low-side switches at the maximum 12V gate input. Figure 62 shows the schematic view of these drivers and their connection to the overall circuit.

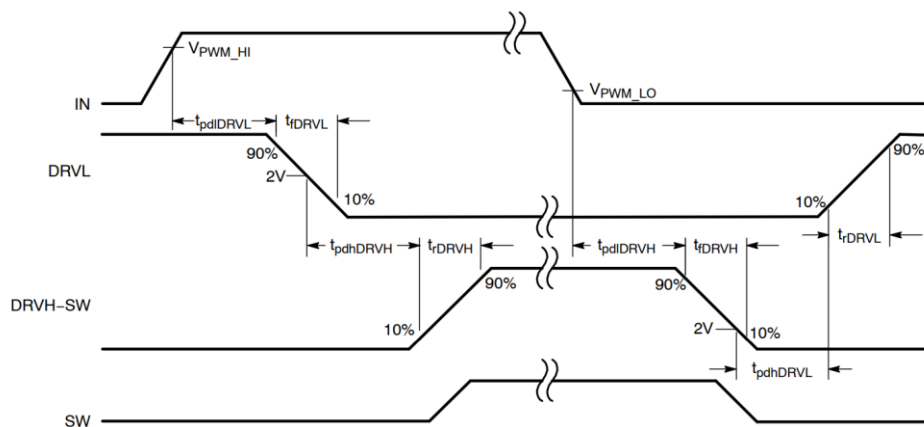


Figure 60 - Driver Switching Timing Guide

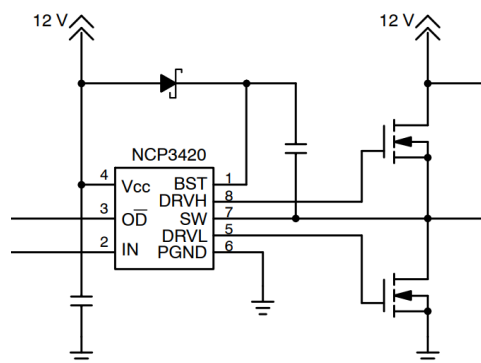


Figure 61 - Driver Setup Example

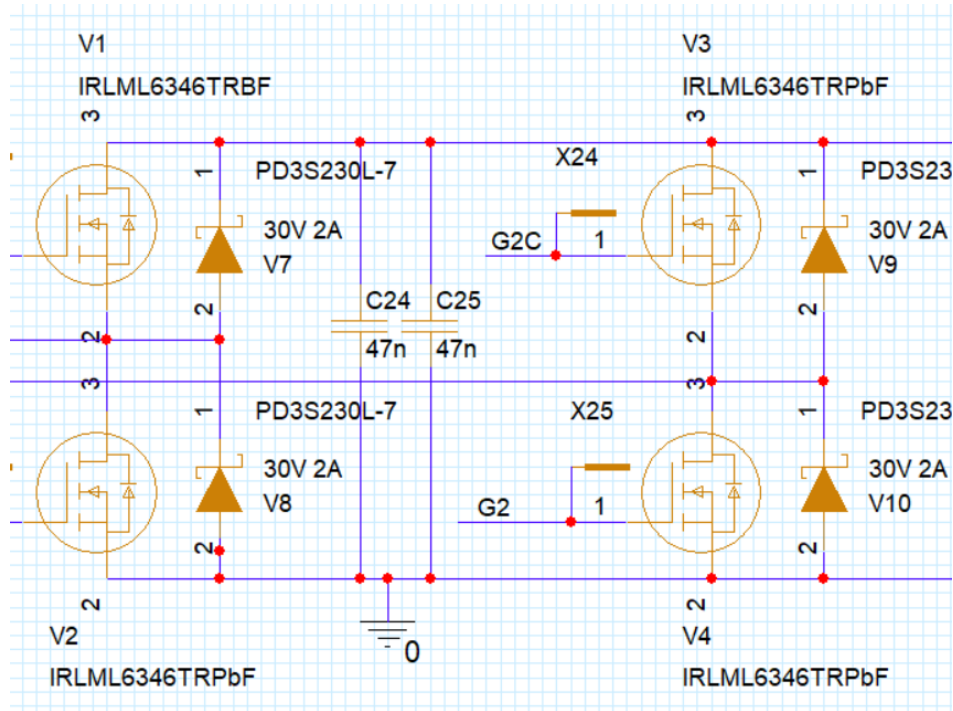


Figure 63 - IRLML6346TRbF Mosfets

Other Circuit Modifications

Each mosfet switch contains a built-in body diode that is part of the makeup of the device, shown in Figure 64, which can carry power in a set direction without the device being turned on. While it technically acts as a regular diode, the body diode is often inefficient, and a more correctly sized diode is often placed in parallel if needed. For this design a second diode is added across each switch, seen in Figure 65, that allows the output capacitor to charge up during start up conditions; before the control can turn the switches on and off. This allows the topology to benefit from both passive and active rectification, depending on the control ready state and start up conditions. The diodes across the mosfets are 30V fast acting Schottky diodes, capable of quickly responding to any transients seen from the switching events. There are also 20V Zener diodes placed closely across the output capacitors. These are slower but can handle a much greater amount of power and are meant to prevent the output voltage from rising higher than the max voltage of the various circuit components. Future designs could raise these to 30V or higher to allow for a greater output range of voltage.

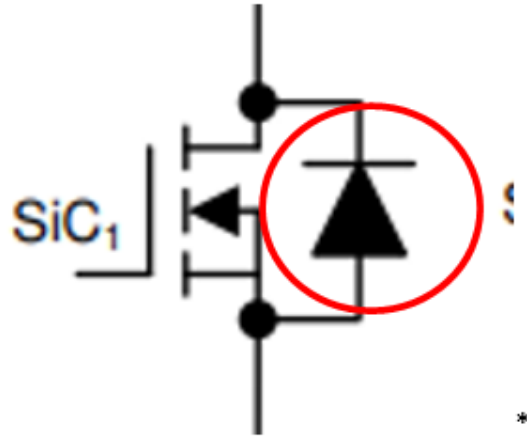


Figure 64 - Mosfet Body Diode

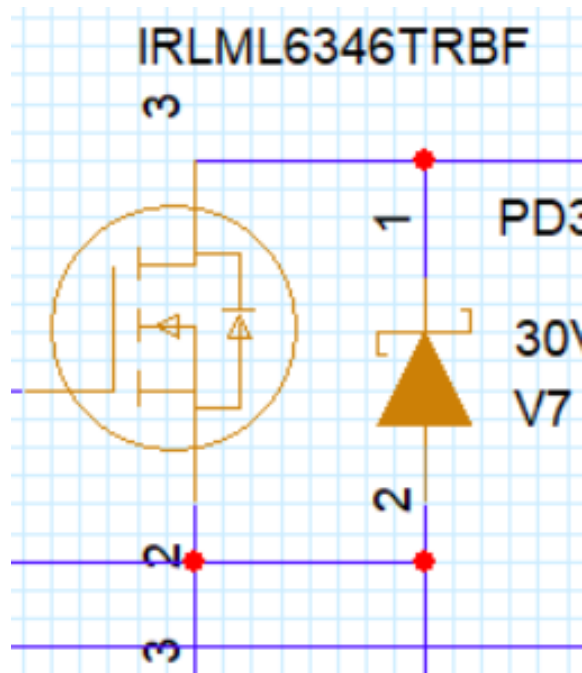


Figure 65 - Mosfet Parallel Diodes

Various capacitors were used throughout the system for energy storage and noise filtering, examples of these are shown in Figure 66. The 5300uF capacitors were chosen for output power storage as they can be scaled from a single capacitor to a total of eight equaling 42.4mF of capacitance. This allows tuning of the output storage based on planned use of the device, making it easier to raise the voltage or allowing for greater loads on the output with less ripple voltage effect.

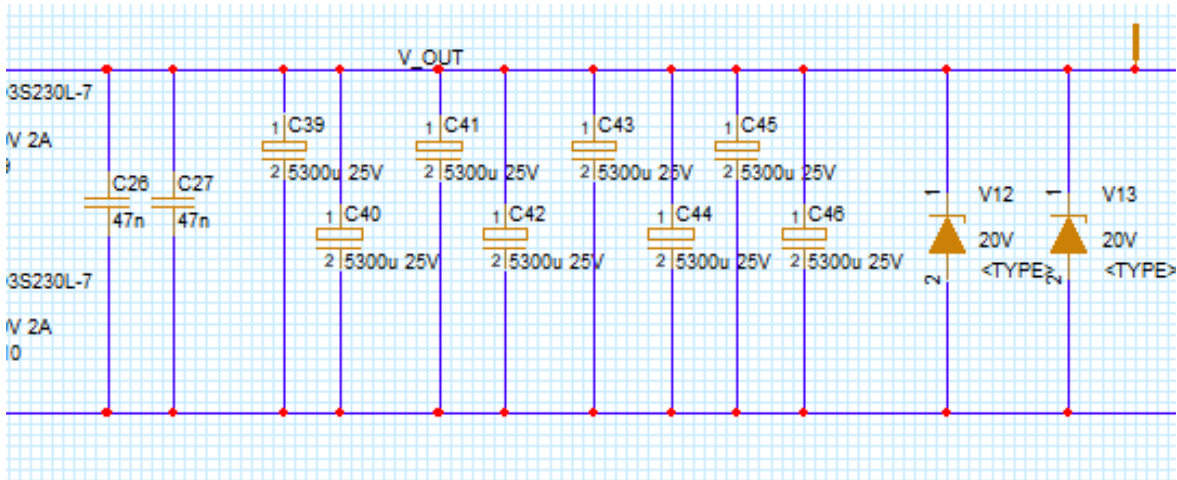


Figure 66 –Output and Filter Capacitors

The other capacitors of note are the 47nF and 1uF capacitors used through the system. The 47nF capacitors are used to filter out noise on the faster 10kHz signals while the 1uF capacitors are used in a similar fashion for the 60Hz signals. The 47uF capacitors are seen on positions such as the mosfets outputs and the current sense IC that deals with filtering these 10kHz signals. The 1uF capacitors are used to help regulate dc voltages created by the resistor dividers or to filter out noise on the slower 60Hz signals. These are placed primarily near any ADC or IC as noise can be picked up from long traces or from the mosfet switching. To size the capacitors Equation 12 can be used if specific loading values like number of loads or max current to switch a load from low to high. The main design consideration for the 47nF bypass capacitors was internal capacitances of the various ADC inputs and outputs. From the datasheet most input capacitances ranged from 10pF to 100pF in value, so adding the 47nF capacitance in parallel does significantly increase the rise time of those signals. It is small enough to not be noticeable to the control and big enough to filter out noise.

Equation 12 - Capacitor Bypass Equation

$$C_{Bypass} = \frac{(I * N * \Delta t)}{\Delta V}$$

Component Power Loss and Thermal Calculations

To size the various electrical components for the PCBA, as well as the needed trace widths, an understanding of the power levels expected, and their ranges is needed. From the previous Table 3 and Table 5, it's found that a minimum of 57mW and a maximum of 1.022W will be delivered to the output of the harvester circuit. Based on this range the electrical components need to have a maximum power loss of 57mW at minimum load to still deliver power to the output and need to survive the voltage

required to achieve the maximum load. As such, all power calculations below are done for a magnetic field input of 1mT, which is the minimum input possible.

First, to check if minimum load is possible the most likely source of power draw and loss are considered. These are the processor, mosfets, gate drivers, and current sense IC. The bypass capacitors, resistor dividers, and diodes are sized as to be such a low power loss as to not be an issue. For instance, the output voltage measurement is taken across a total resistance of 1Mohm, which draws of 3500 times less power at the planned 15V output than the minimum delivered power; safely being ignored for initial calculations.

The first component to consider is the processor chosen, the TMS320F28379D. The processor used on the PCBA is a launch-pad housing which is the plugged into the PCBA and powered off an extra 5V supply. This is done as it was not possible to order this CPU during the timeframe of this project due to excessive lead times and no alternatives were found, so the entire launch pad was used instead of the single processor and its supporting components. As such, the power losses for the launch-pad were not considered during these calculations. For reference, the datasheet for this processor listed the expected power draw to be 0.6W at the used clock frequency of 100MHz, as shown in Figure 67. This does not factor in power saving modes that can be used and the real value can be significantly less. Future work could attempt using lower power processors that can be factored into the overall power loss, but this must be done when market availability becomes better.

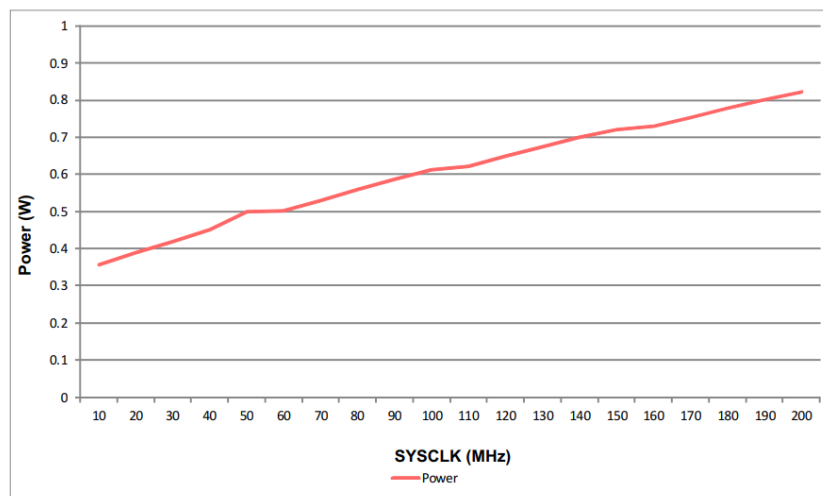


Figure 67 - Expected TMS320F28379D Power Draw

The next components for consideration are the mosfets and gate drivers. These are expected to have the highest losses made up of switching and conduction losses. There are three types of losses, switching, gate, and conduction losses. The main contributor to the switching losses is the turn on and off times along with the drain to source voltage. The contributor to conduction losses is the on resistances when power is flowing through the mosfet and can vary with temperature. The contributors to gate losses are the gate charge required and the switching frequency. The datasheet gives the gate

charge for each mosfet at 2.9nC, which equates to a total gate loss of 0.696mW for all four mosfets. For conduction losses an on resistance of 0.063ohms is found to be the worst case possible and when factoring in current and duty cycle times a loss of 3.25mW is found. For switching losses the turn on and off times of the mosfet are found when comparing the times to the expected drain to source voltage of 15V; which is the planned output voltage, this calculates to a loss of 1.18mW of loss. Table 6 below shows the calculations done and their associated equations and gives a max power loss of 5.13mW of power at minimum input power, which is roughly 9% of expected power. Note that these calculations are based on ma current possible, where the real current will depend on available energy and power factor correct ability.

Table 6 - Power Loss Calculation

Component	Unit	Value	Calculated Variable	Calculations	Equations written out
Mosfet			del_Vboot	1.2	$V_{dd}(GD) - V_f - V_{gs_Min}$
	Vgs	6	C_bst	2.41667E-09	$= Q_g / \text{del_Vboot}$
				increase this by 10 times to have 120mV droop allowed	
	Rdson_Max	0.063			
	Rg_internal	3.9	I_f_avg	0.000029	$= Q_g * f_{sw}$
	Qg	2.9E-09			
	ton_total	7.7E-09	P_conduction_total	0.003254132	$= R_{dson} * I_{ds}^2 * (2 * \text{Duty})$
	toff_total	1.69E-08	P_switching_total	0.001186011	$= 4 * (1/2) * V_{ds} * I_{ds} * (t_{on} + t_{off}) * f_{sw}$
	Thermal Resistance (C/W)	100	P_gatecharge_total	0.000696	$= 4 * Q_g * V_{gs} * f_{sw}$
	Fsw	10000			
Vgs_Min	4.5	P_Total_Losses	0.005136143		
Rg_external	0				
Gate Driver					
	Thermal Resistance (C/W)	123			
	Output res, sourcing current, max	3			
	Output res, sinking current, max	2.5			
	Vdd / Vgs	6			
	Vforward	0.3			
	Vgs_Min				
Harvester					
	Vin_Min_ac_pk	1			
	Vin_min_RMS	0.707106781			
	Iin_Min	0.160706087			
	Rin	4.4			
	Pin_Min	0.113636364			
	Vds	15			

Following the mosfet losses are the ICs used in the design. Besides the main processor, the gate drivers and current sense IC also have losses to consider. The gate drive losses have largely already been considered as they are the same losses from the mosfet gate charge losses above. The power lost from charging the gate drivers capacitors is transferred to the mosfets input capacitances before being lost, so these are already accounted for. Besides gate charge loss, the gate drivers also have operational loss to consider. Based on datasheet values these are found to be 3.5mW at 5V input in typical use. When factoring in that two drivers are used, and removing the gate charge losses, the operational losses are expected to be 5.6mW. Table 7 shows the datasheet expected power use for reference. For the current sense IC the typical current draw is 1mA, with a planned input voltage of 5V a loss of 5mW will occur. Table 8 shows the datasheet power use as a reference.

Table 7 - Gate Driver Datasheet Power Use

Supply						
Supply Voltage Range	V _{CC}	-	4.6	-	13.2	V
Supply Current	I _{sys}	BST = 12 V, IN = 0 V	-	0.7	6.0	mA

Table 8 - Current Sense IC Power Use

GND (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN ⁽¹⁾	TYP ⁽²⁾	MAX ⁽¹⁾	UNIT
OVERALL PERFORMANCE (FROM -IN (PIN 1) AND +IN (PIN 8) TO OUT (PIN 5) WITH PINS A1 (PIN 3) AND A2 (PIN 4) CONNECTED)					
I _s	Supply current	1			mA
		Over full temperature range			
		0.6		1.3	

With the most likely sources of power loss accounted for the total power loss at minimum power input is 15.73mW, or 27.6% of the expected minimum input of 57mW. This leaves roughly 41mW of delivered power to the output for operation. This is a small amount of power that would likely not allow an output to run in continuous mode, so for such an instance a power monitoring circuit would need to be developed to charge a battery until enough power is stored for operation. This number does not take into account the future processor power needs nor the other losses that will come from resistors, diodes, and capacitors.

For maximum input load situations, the components need to be sized for both the voltages and power levels they may see. From Table 5 its expected that the optimized harvester will have an input voltage of 4.4V into the circuit. This is planned to be boosted to an output of 15V, making 15V the voltage many of the components must be able to withstand. Many devices have been sized to twice the rated voltage, so 30V for the mosfets and diodes. The lower the device rating the higher the efficiency due to the internal build of the device being thinner, but thus it becomes more difficult to protect. The output capacitors are rated to 25V and due to the high amount of power that can be stored there the capacitors are protected by two 20V Zener diodes. All ceramic capacitors are rated for 50V while all resistors, besides the current sense resistor, are rated for a quarter watt each minimum, more than enough for any powers they will see. The current sense resistor is rated at one watt since it will see the highest concentration of power, but even then, should not see more than a half a watt at most. Figure 71 shows an example 3D image of the final PCBA design before production. This gives an idea of what realistic sizing can be expected for future placement.

Layout Method and Commutation loops

With components sized the layout can be created. Figure 68 shows the overall PCBA layout designed for this work in Cadence. The PCBA is four layers, making use of an internal ground layer for greater noise immunity. The top layer contains the switching electronics that create a great amount of noise, along with much of the power transmission across the PCBA. Layer 2 acts as a commutation loop layer, specifically for the mosfet switching noise across the purple planes; shown in Figure 69. Layer three is a generalized ground plane for the entire PCBA that, while directly tied to the commutation loop layer, will be free of the majority of the switching noise due to the effect of path of least resistance from the commutation loop. Layer four then contains several sensor circuits that tie back into the ADC. Figure 70 [14] shows an example of commutation loops in practice. 'Loop 1' is the top layer where the majority of switching noise is present. The 'LP1' and 'C_Decouple' connect both ends of 'Loop 1' together so that current has a completed path and place for current to flow. While current could flow out into 'Loop 2', the commutation loop previously discussed creates an easier path to take that makes most of this noise stay isolated from the rest of the circuit and prevents noise from passing into other signals.

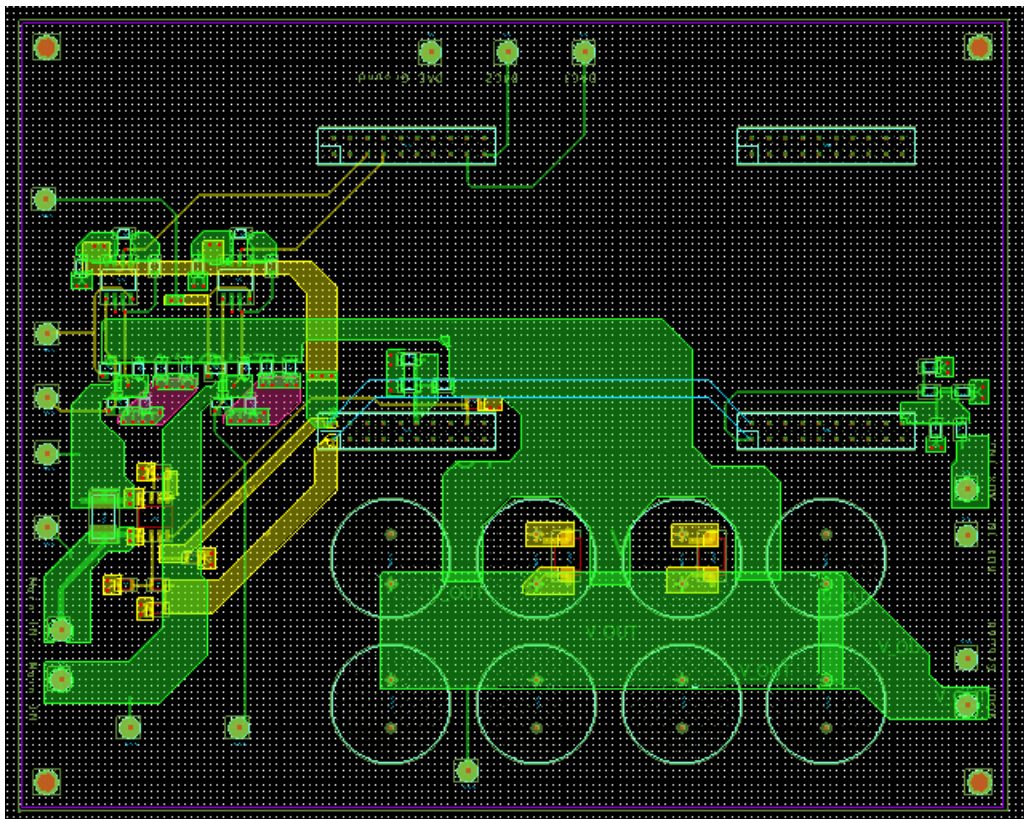


Figure 68 - PCBA Layout Overview

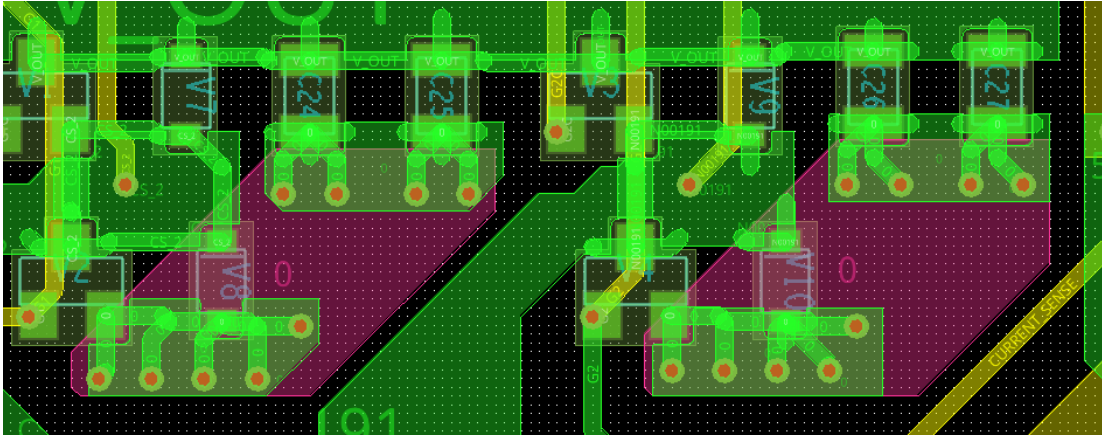


Figure 69 - Commutation Loop

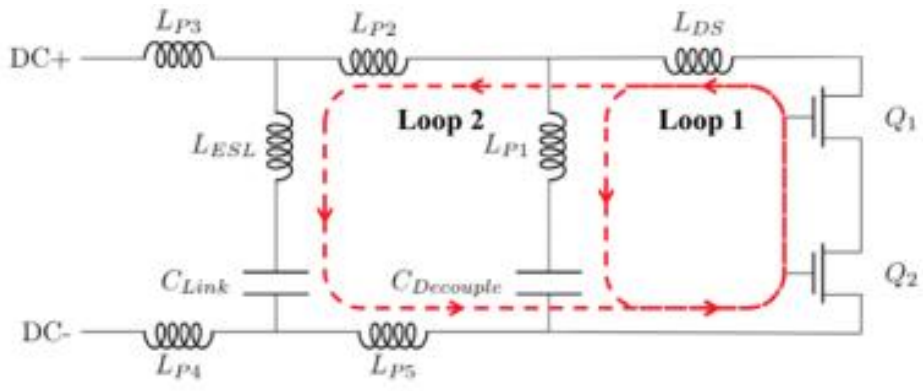


Figure 70 - Commutation Loop Example

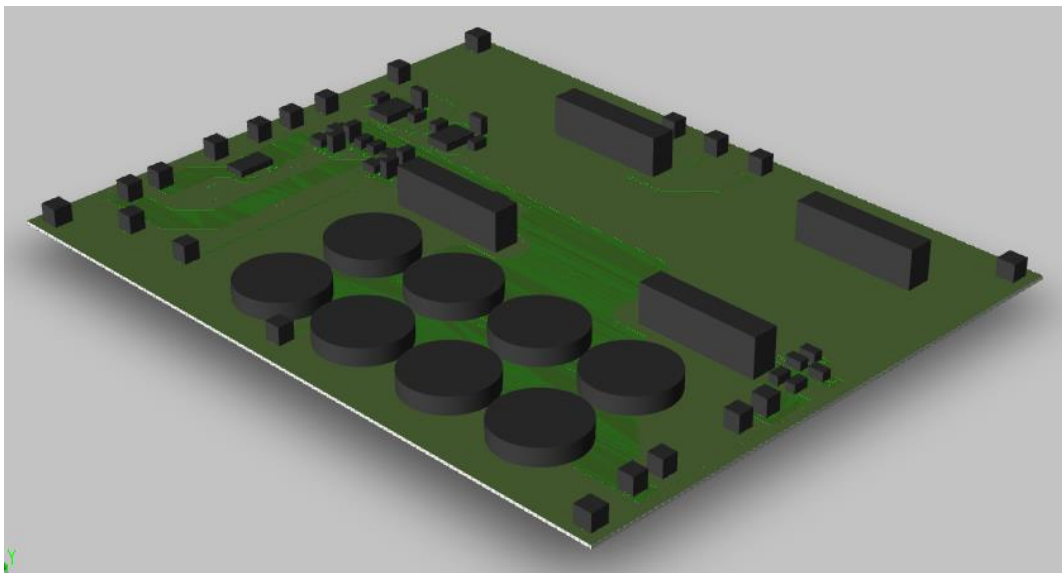


Figure 71 - PCBA in 3D Form

During component placement, positioning of the ICs, bypass capacitors [10], and safety components is vital. Figure 72 shows the current sense resistor placed directly above the inputs to the IC sensing these values. This reduces the potential noise from longer traces greatly. Figure 73 shows the placement of one bypass capacitor. By placing this as close to the sense pin of the ADC as possible the noise picked up on the long trace across the PCBA can be greatly attenuated. Figure 74 shows placement of the protection diodes for the output capacitors. By placing these close to several capacitor pins the delay from the diodes turning on to protect the output capacitors is greatly reduced, along with any instantaneous voltage spikes being reduced. Figure 75 shows the gate driver layout showing how the passive components are placed as closely as possible to the driver to maximize operation. One downside of this design is the distance from the driver output to the switch it operates, however this is only 11mm and should not cause a noticeable issue at the intended switching frequency of 10kHz. Finally, the MCU processor chosen could not be sourced due to stock issues. Instead, a launch pad housing this processor was used on this PCBA and four connectors, shown in Figure 68, we placed to allow the launchpad to be plugged in for use. Pins chosen for future ADC sampling were based on proximity to circuit placement to reduce overall travel path as much as possible.

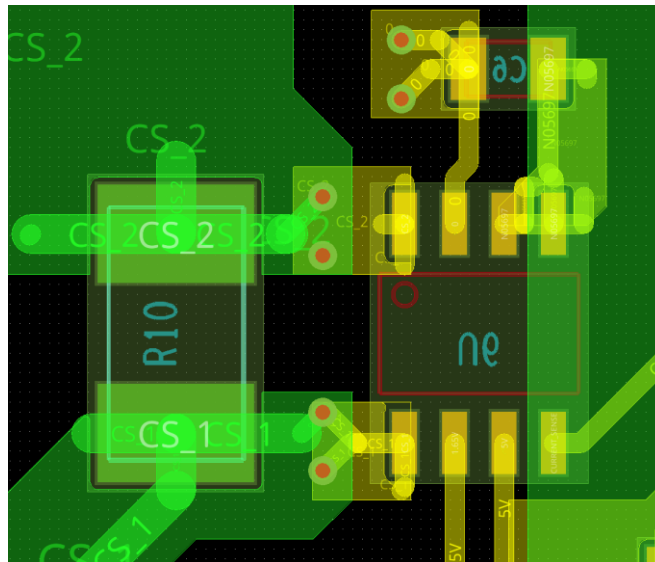


Figure 72 - Current Sense Resistor Placement

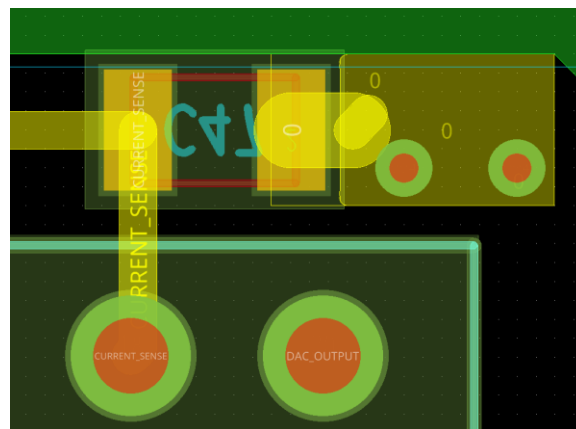


Figure 73 - Bypass Capacitor Placement

Shown in Figure 76 and Figure 77 are thermal images of the harvester working at minimum input power. The hottest portion is the launchpad which reaches the low 30C's while the actual switching stage does not rise above 26C. The switching stage is directly under the launchpad which makes thermal imaging difficult. What is shown are two side views on the greatest losses of the circuit, excluding the TMS IC.



Figure 76 - Thermal at Minimum Power



Figure 77 - Thermal at Minimum Power 2

Ch 5 – Digital Control

Previous TTPL-PFC Controller Logic

From previous work [7] it was seen that the output of the initial Totem-Pole PFC could be controlled by sampling the values of the input voltage, input current and output voltage of the circuit. These then act as inputs into the designed controller which generates the duty cycle signals to turn the mosfet switching devices on and off. The duty cycle is commonly referred to as the PWM (pulse width modulation) signal and Figure 78 [7] shows an example of the in action. Here the switch Q1 is always off while Q2 is always on, Q3 and Q4 then alternate on and off states based on the duty cycle being 'high' or 'low'. Figure 79 [7] shows how the duty cycle 'D' is generated from the triangle wave output from the designed controller. Here the duty cycle goes high when the triangle wave goes below a certain set value and vice versa.

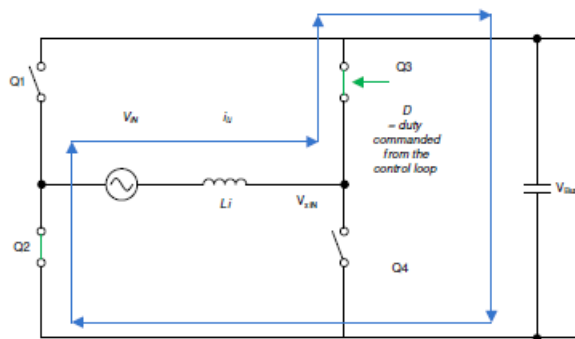


Figure 78 - PWM Mosfet Control

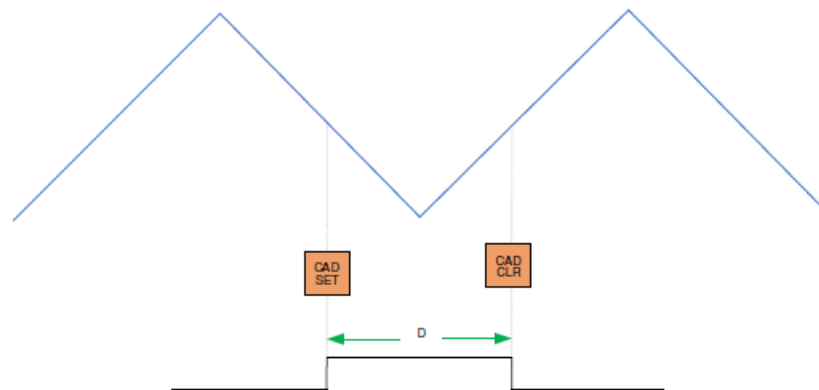


Figure 79 - Duty Cycle Generation

To create the triangle signal from Figure 79 two control loops are used. The first is a current control loop that samples the output bus voltage and a calculated input current reference to generate the triangle signal responsible for the duty cycle value. The bandwidth of this loop is fairly fast as it quickly updates the output reference based on changes to the output voltage, input voltage, and current reference. Figure 80 [7] shows the current loop control model.

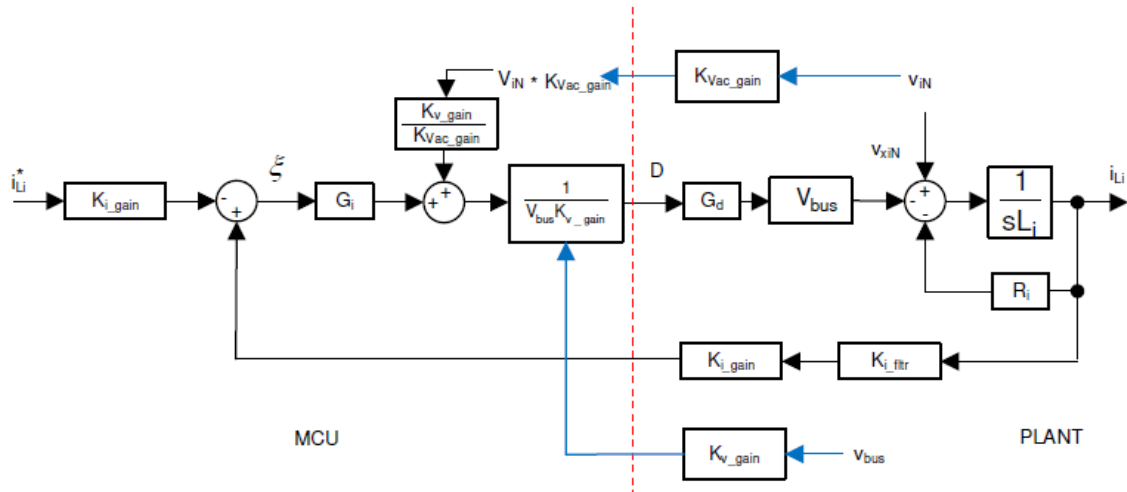


Figure 80 - TTPL Current Control Loop

The second control loop is the DC bus regulation loop, shown in Figure 81 [7]. This loop is responsible for monitoring the power levels of the circuit and providing a reference current value to the current control loop. This loop has a much lower bandwidth compared to the previous and only has the input and output voltages as inputs for operation.

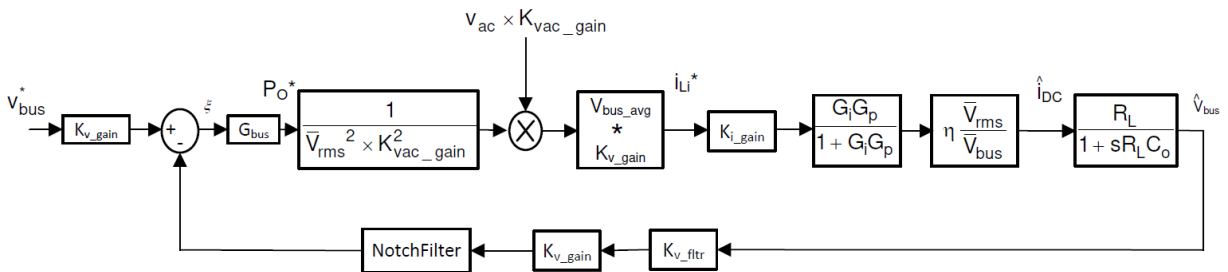


Figure 81 - DC Bus Voltage Control Loop

MCU Processor Selection

When uploading a program onto a processor, consideration for the size and capabilities must be given. Each processor has unique benefits and detriments to consider when choosing that will determine what kind of work can be done on one. Some base considerations to give are number of ADCs for sampling, max speed of processor (cycles per second), number of free GPIO ports, low power options, Floating Point Unit (FPU), PWM module, and more. The processor for this project was chosen before the controls were finished and as such did not work optimally. As such, two were tried and only the second worked well enough for full use.

The first processor attempted is an MCU; MSP430FR2476 shown in Figure 82, mounted on a launchpad for quicker use. When searching for a processor only two things were originally considered. The first was the need for an ultra-low power mode, which the MSP430 has and can operate in this mode at 135 $\mu\text{A}/\text{MHz}$, equating to a real power draw of 4.4mW at 10MHz operation. This was well within the needed limit for low power operation based on previous calculations at minimal input power, and at the time 10Mhz was a clock speed consideration. The second consideration was a minimum of three analog to digital converters at 12-bit resolution, which this has 12 single channels of; or 6 dual channels if needed. Two main downsides were found for this processor that prevented its eventual use. The first was the lack of an FPU (floating point unit) module within the MCU, which allows for faster cycle by cycle processing of data. A function to process two floating point values would take 200 cycles instead of the expected 10 cycles, drastically increasing time needed to complete the control work. This then led to the second downside, where the fastest clock cycle rate for this MCU peaks at 16Mhz. While a solution was attempted with fixed point math, it did not reduce the cycle time requested for control calculations enough to allow use of this MCU.



Figure 82 - MSP430FR2476 MCU

The next and final MCU attempted is the TMS320F28379D. This is a popular MCU used at NCSU for multiple projects, so its reliability is already known. It solves the previous two issues discussed as it has a max clock rate of 200Mhz and a built in FPU module for easier programming and faster function clock speeds. All previous benefits were retained and more added if needed. It also uses the same CCS library as the previous attempted MCU so code already written can be reused with minor adjustments. Figure 83 shows this MCU mounted on a launchpad. Two items of note are the expected increase in power draw and the lack of individual chips available for purchase. The power draw was accepted as the goal of the project is to confirm the rest of the circuit and this merely acts as the tool to prove the control logic and topology use; alternatives to this MCU and the higher power draw can be found in future updates. Also, this project was completed during the covid epidemic and supply chains struggled to find any of this IC for individual purchase. Because of this the entire launchpad was incorporated into the layout design instead of the individual IC, which keeps power draw very high and makes it unrealistic to include for power comparisons further on.

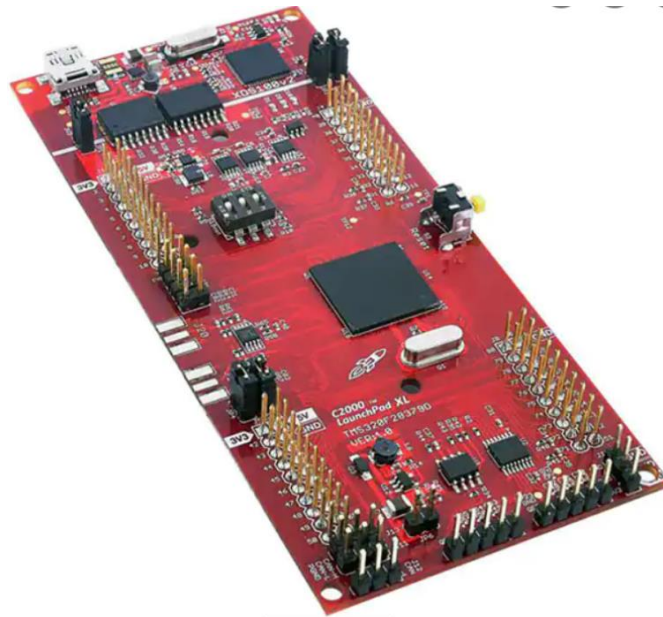


Figure 83 - TMS320F28379D MCU

Firmware and Software

To use the MCU to control the circuit a distinction between two types of code needs to be made. Software is code written specifically to replicate the control work done in simulation. The blocks and comparisons shown in future simulation work can be directly digitized into equations capable of being loaded onto the MCU for processing. Software does not care about what voltage range the hardware will see, or send, and completes its logic assuming all inputs and outputs are scaled to fit properly. Firmware is coding to scale all signals correctly so that the software logic works properly. Figure 84 shows that the input signal 'V_IN_LOAD' which is used by the control to complete a function. The signal is subtracted by some other unknown value and then the result is multiplied by '0.8' and sent further into the control. The software portion includes by the subtraction and multiplication of the signal, while the signal itself is created by the firmware.

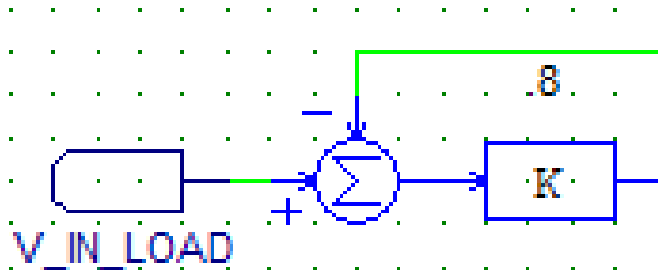


Figure 84 - Input Signal Example

To create the input signal the firmware will scale the input voltage range to match the MCU ADC voltage range. Figure 85 shows the ADC input range for a single ended setup, allowing a maximum of 4.6V AC input and a minimum of -0.3V AC, with Vssa being ground of 0V, but can reach as low as -0.3V. This assumes the maximum voltage supply of 5V is used while lower supply voltages are recommended. This shows an accepted voltage range of -0.3V to 4.6V AC, while voltages outside of this range can cause either damage to the MCU or create errors in the ADC conversion process. In either case, these need to be scaled to the correct range, read into the ADC, and then returned to the correct range. While the first part of reducing the range is done by analog circuitry, the firmware is then responsible for accurately scaling these inputs back to the real values for control calculations. In this way the firmware is customized for the circuitry the provides the value. A simple resistor divider than scales the output voltage, that can reach as high as 30V, down to a maximum of 3V which can be accepted by the ADC. The firmware than calibrated to scale this value back to the correct value for software use.

8.10.1.2.3 ADC Operating Conditions (12-Bit Single-Ended Mode)

over recommended operating conditions (unless otherwise noted)

	MIN	TYP	MAX	UNIT
ADCCLK (derived from PERx.SYSCLK)	5		50	MHz
Sample window duration (set by ACQPS and PERx.SYSCLK) ⁽¹⁾	75			ns
V _{REFHI}	2.4	2.5 or 3.0	V _{DDA}	V
V _{REFLO}	V _{SSA}	0	V _{SSA}	V
V _{REFHI} - V _{REFLO}	2.4		V _{DDA}	V
ADC input conversion range	V _{REFLO}		V _{REFHI}	V

Analog voltage	V _{DDA} with respect to V _{SSA}	-0.3	4.6	V
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Figure 85 - TMS320F28379D Datasheet Values

SOGI Controller and ABDQ

Before delving into the closed loop topology, an overview on some of the techniques used is needed. These are discussed in papers [6, 9]. Two key methods used are the SOGI and ABDQ controllers. A second order generalized integrator (SOGI) is a system to create two AC signals from a single AC input. A SOGI system is also called an orthogonal voltage system, meaning it can create signals at an orthogonal angle, or a 90-degree phase delay, to the original source. The SOGI has two inputs, the AC input, and a reference frequency value that are compared to the frequency of the input source. The SOGI will use the reference frequency to filter out any noise on the input to provide a clean output signal of the same frequency and same phase as the first signal. The second signal is taken from the first, but phase delayed by 90 degrees using a second integrator. Figure 86 [6] below shows a noisy input signal 'Vg' along with the two outputs 'V' and 'qV'.

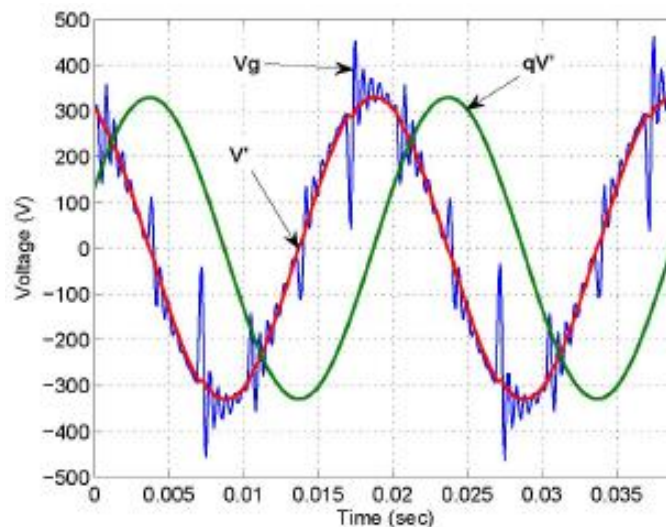


Figure 86 - SOGI Example

After the SOGI controller is the park transform, or ABDQ controller, shown by the ABDQ block in Figure 95. With two signals, separated by 90 degrees from the SOGI controller, the ABDQ controller can make two different reference signals shown in Figure 87. The first is a 'DC' reference signal, shown the first plot, and based on the peak input voltage measurement from the two input signals. As the AC signal peak voltage rises and falls, the two signals will have changing peaks tracked in 'Vd'. The second is a phase reference signal, shown on the second plot, that shows how in phase the input signal is with the theta reference. This theta reference will be used in a closed loop feedback to change the theta value until it is in phase with the first input signal. Equation 13 below shows the equations that make up the parks transform, while Figure 88 shows the graphical representation of these equations. Ux and Uy represent the input signals, generated by the SOGI controller, while Ud and Uq are the dc equivalent and phase representation signals.

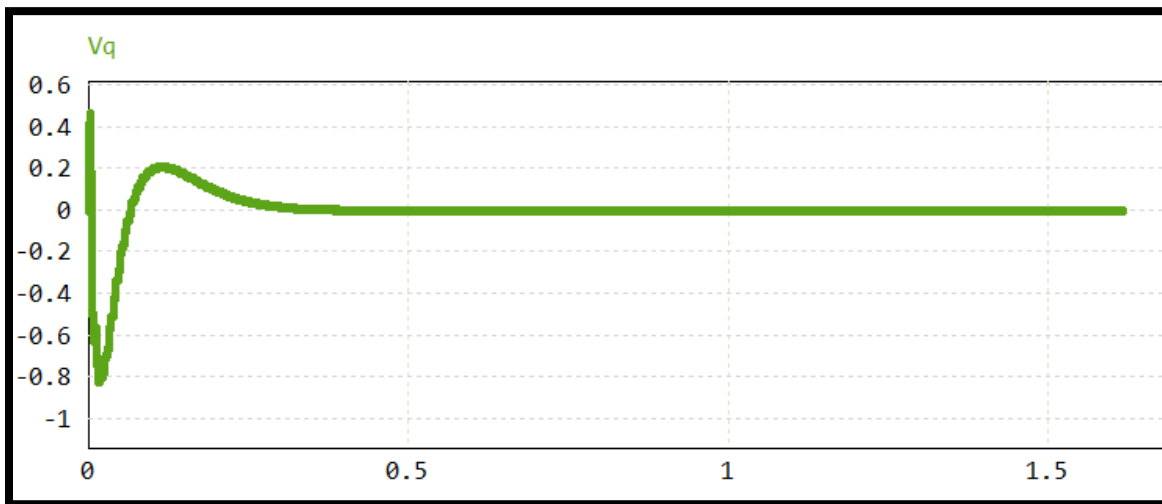
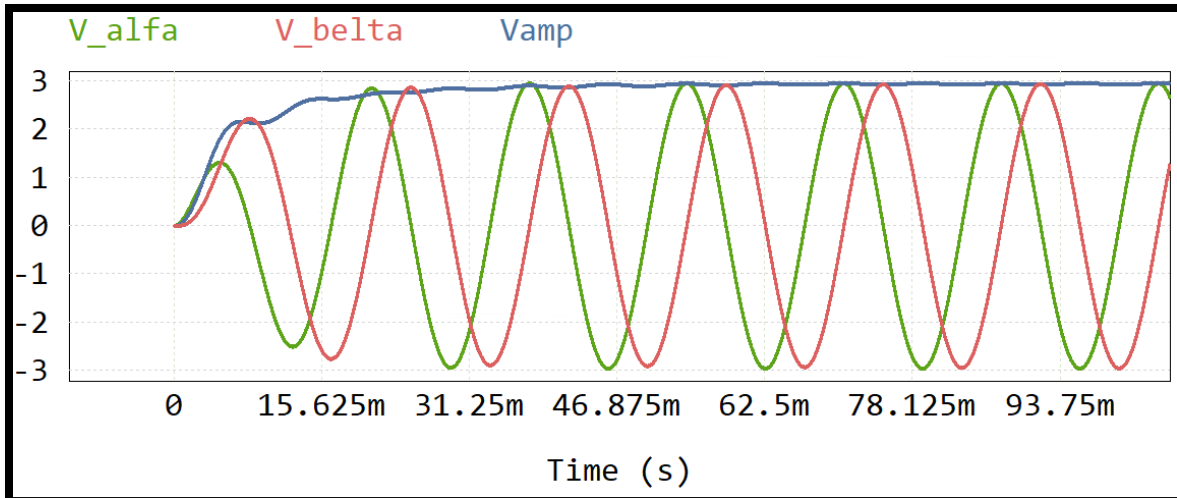


Figure 87 - PSIM ABDQ Outputs

Equation 13 - ABDQ Equations

$$\vec{v}_{DQ} = \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix} \cdot \vec{v}_{XY}$$

$$\hat{u}_D = \cos(\theta)\hat{u}_X + \sin(\theta)\hat{u}_Y$$

$$\hat{u}_Q = -\sin(\theta)\hat{u}_X + \cos(\theta)\hat{u}_Y$$

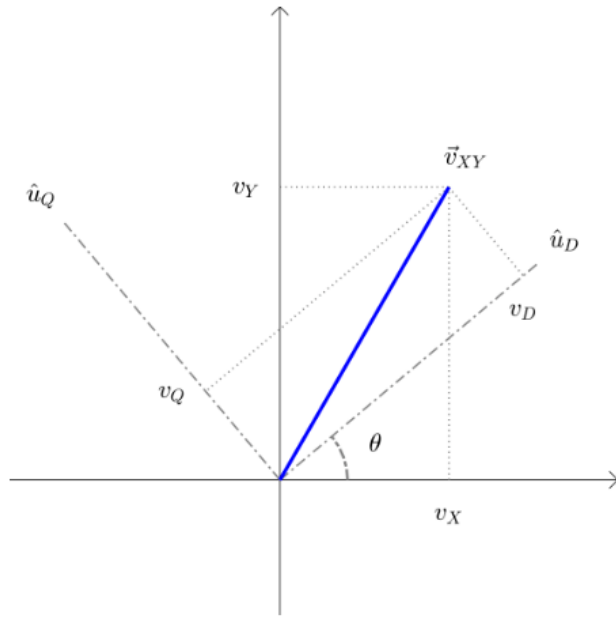


Figure 88 - ABDQ Equation Plot

PI Controller and Theta Generation

With a reference value of the frequency stabilization from the ABDQ controller, a theta signal can be generated. The reference value shows how out of phase our starting theta value is and is used to adjust it to match for correct operation. A PI controller is added to speed up the matching signals to be in phase and provide stability during this operation. Figure 89 shows this with and without a PI controller and how the option with a controller finishes much faster. Finally, to stabilized reference is added to the our desired 60 hertz value and sent through a modulus function to create a triangle waveform from zero to 2π in value. This works by taking to added value and integrating to get a linearly increasing value of 60 hertz plus the reference value. This is then sent through the modulus function which maxes out at a set value, in this case of 2π .

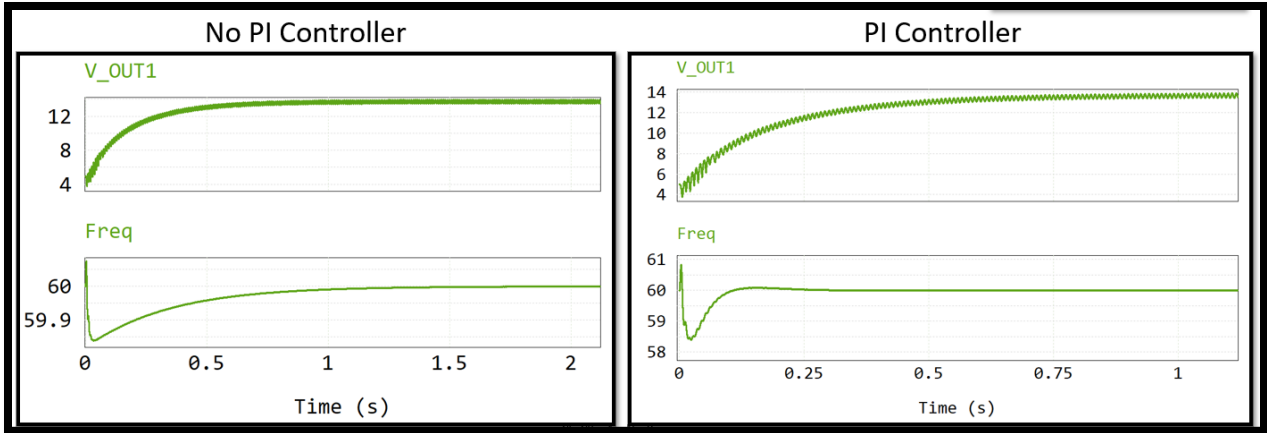


Figure 89 - PI Controller Comparison

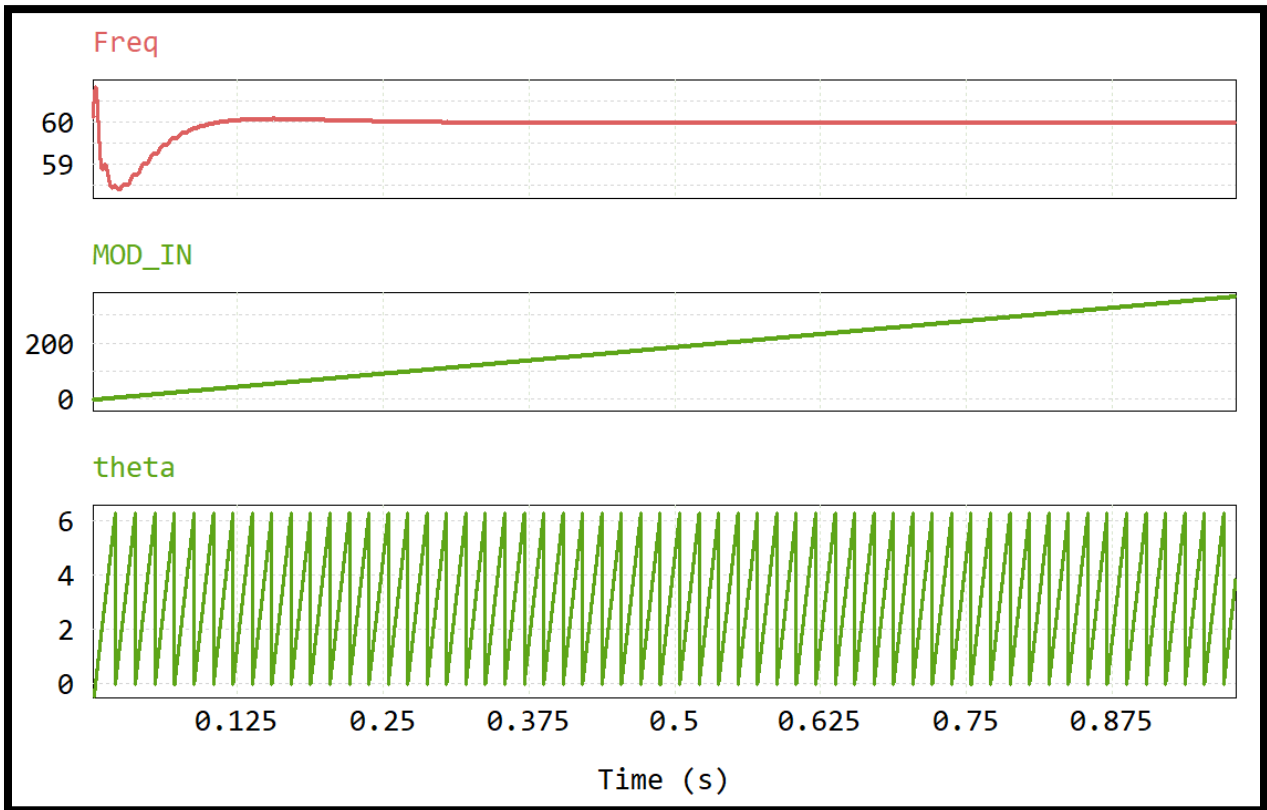


Figure 90 - Theta Generation

Open Loop Operation

The final step before designing full control code is to confirm operation of the topology in open loop. To do this Figure 91 reads in a filtered auxiliary signal of the input magnetic field sine wave. With this source a PLL is created, using the previously discussed techniques, outputting a theta value of the input signal, theta being the radian equivalent of the AC signal angle. Equation 14 is then used to generate the modulation signal (V_m) based off a setpoint for the intended output voltage. The modulation signal is then compared to a 30kHz triangle voltage source and the output creates the PWM signals that drive the switches. At this stage the open loop controls consist of only the PLL and the modulation equation, so there are no feedback signals to change operation based on input power. As the setpoint value is lowered the modulation signal lowers, reducing the on time of the charging portion of the cycle, but increasing the output voltage. At some point the setpoint value is lowered so much that not enough power is sent to the output to power the load at the specified output voltage. Figure 91 shows a close up on the PWM generation from a comparison of the 30kHz source and the modulation signal.

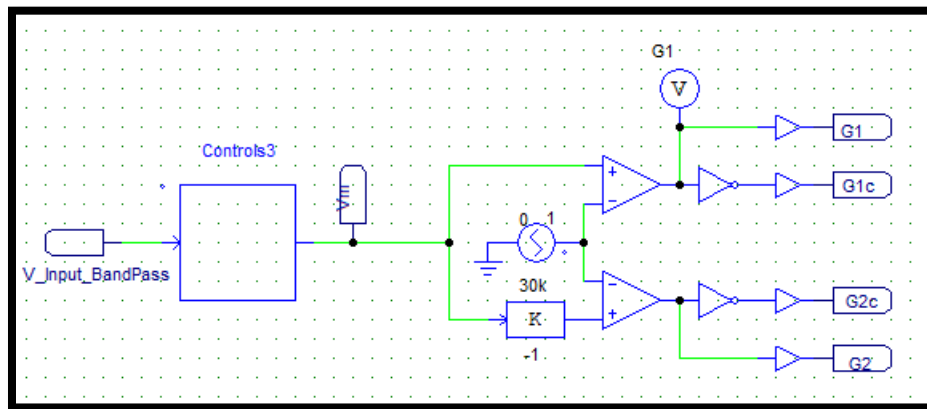


Figure 91 – PSIM Open Loop Control

Equation 14 - V_m Open Loop Equation

$$V_m = -\text{Cos}(\text{theta}) * \text{Setpoint}$$

Figure 92 shows the simulated results of open loop control. Theta is set to match the input voltage on V_IN_LOAD2, and by setting it to negative the modulation signal is simply opposite the input voltage. By adjusting the setpoint the gate signals generated by the 30kHz comparison are changed, resulting in different output levels. It's important to note that the modulation signal is not meant to be in phase with the input voltage, so a subpar result is expected.

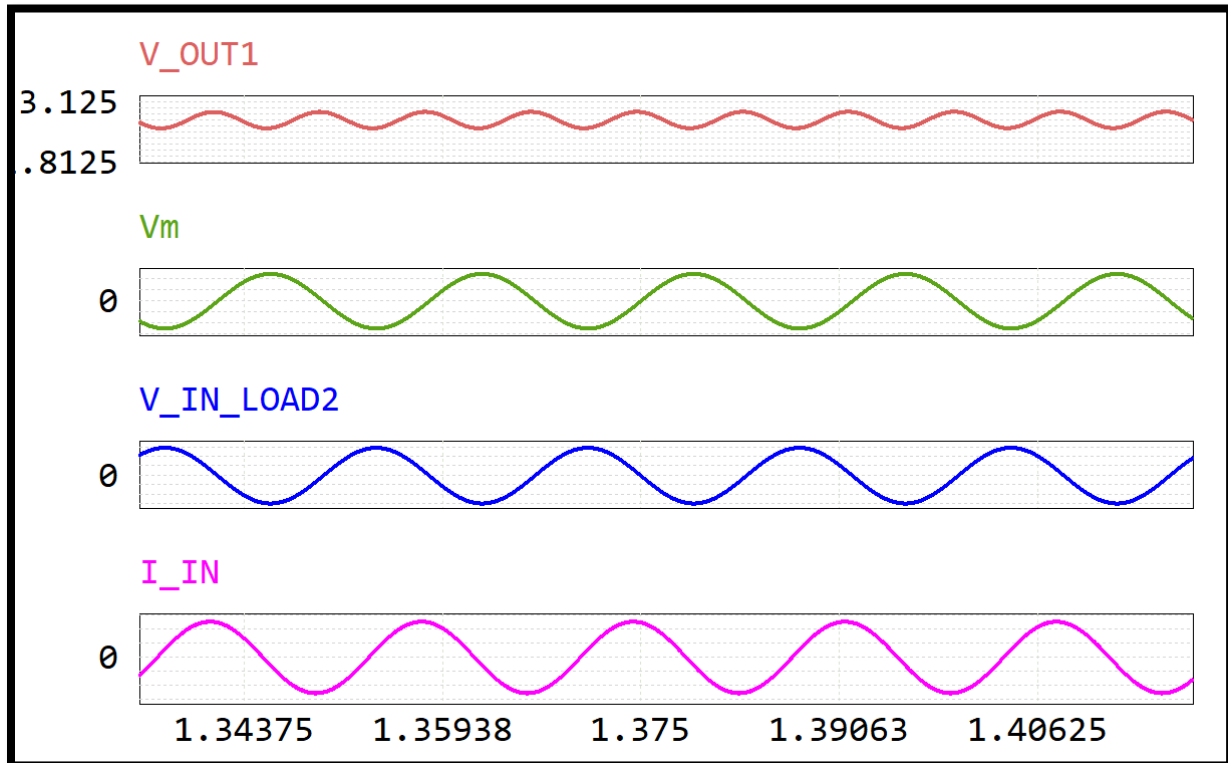


Figure 92 - PSIM Open Loop Check

Needed Controller Sampling Points

With a working open loop topology, the control scheme can now be devised. The goal of this control scheme is to switch the mosfets to achieve maximum power point tracking (MPPT), this will maximize input power to the energy harvester by aligning the input voltage and input current waveforms. In a purely passive system these two waveforms are out of phase by a factor related to the inductance and capacitance of the system. The MPPT scheme will control how often these two passive components see one another to affect the overall PFC of the system. To control this circuit the total input power needs to be monitored by either sampling or recreating the input voltage and current.

To begin the control design, we first review what signals can be sampled to be used in the control scheme. The previous work references the use of input voltage and current as key inputs to the closed loop feedback of the control seen in Figure 93 [7]. These two inputs are unreliable in this system because the input voltage source has become the inductor itself and the filtering the inductor, which filtered out most of this square wave noise, no longer exists. This causes the input voltage source to be a pure square wave of the middle points of the two legs, while the input current measurement, measured by a current sense resistor, is offset by the same square wave signal with a much smaller real current measurement on top. This square wave is switching at 30kHz, which is still possible to be sampled at the 100kHz CPU sampling rate designed in, but with less accuracy than desired. Of these two signals, input voltage and input current, input voltage is not feasible to sample. Input current is still sampled using an analog solution, or external IC, to the controller to cancel out the square wave noise. This IC is mentioned in previous sections and is vital for creating a 60Hz current waveform capable of being measured reliably.

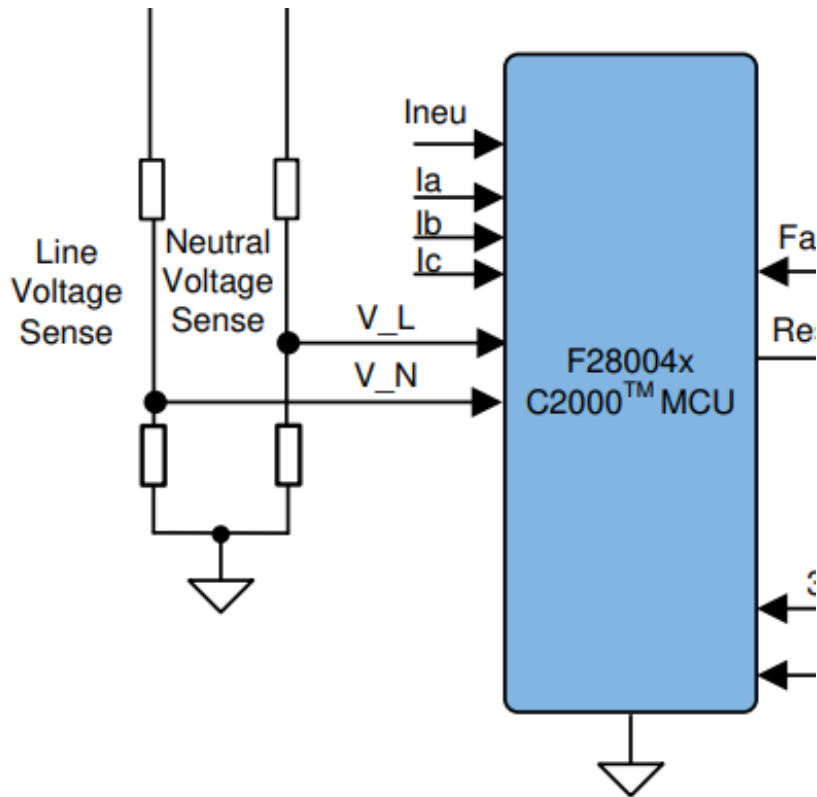


Figure 93 - TTPL Input Sensing

The next option to try uses input and output currents instead of the input voltage [5], but still retains an inductive source for the system. This option replaces the input voltage sampling with an output current sampling to replicate the MPPT max input power method by instead using a specialized perturb and observe method. This control alternatives response between the phase angle and RMS input current measurements to achieve MPPT. It then monitors average output current to maximize input power. While this option would work, it does involve using a second IC to measure output current like how input current is measured. It also uses a half bridge design instead of a full bridge, meaning there would be several diode drops reducing the output power more than desired, for that reason it was avoided. Figure 94 [5] shows the logic of this controller.

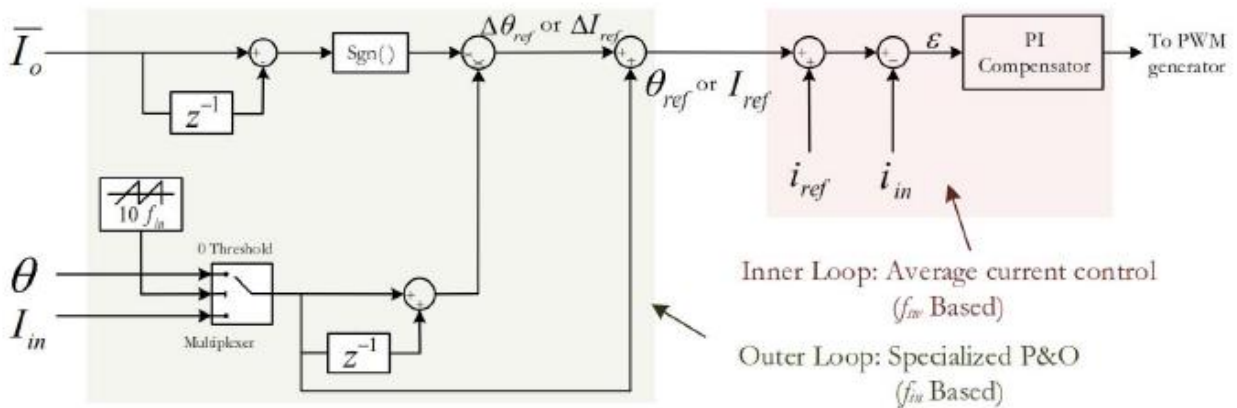


Figure 94 - Input-Output Current MPPT

The final option, and chosen method, is to use a combination of the input current and a separate winding to measure input voltage. The winding will not be loaded, so it gives an accurate representation of the harvester induced voltage at a much-reduced scale. This winding can have a turns ratio of 10 – 100 times less than the harvester as it is not meant to supply power. The voltage measured can then be treated the same as the series RC input voltage to find current. Equation 15 shows how to calculate current from the auxiliary winding measurement, which is then compared to input current of the harvester to perform MPPT.

Equation 15 - IREF Generation

$$I_{REF} = \frac{V_{AUX} * N_{TurnsRatio}}{2 * R_S}$$

Closed Loop Operation

With a working open loop topology, the control scheme can now be devised. The goal of this control scheme is to switch the mosfets to achieve maximum power point tracking (MPPT), which will maximize input power to the energy harvester by aligning the input voltage and input current waveforms. In a purely passive system these two waveforms are out of phase by a factor related to the inductance and capacitance of the system, while in an active system the MPPT scheme will control how often these two types of passive components see one another to affect the overall PFC of the system. To control this circuit the total input power needs to be monitored by either sampling or recreating the input voltage and current signals. To do this a closed loop control was developed in PSIM that sampled three voltage signals to maximize output power to the load.

The first portion of the control code is the PLL (phase lock loop). The PLL is responsible for sensing the frequency of the AC input signal and creating a reference 'theta' value that will then be used by other portions of the control, Figure 95 shows this control portion. The auxiliary winding of the harvester replicates the input AC voltage seen by the power circuit, without the switching noise. This is inputted into PLL as 'V_IN_LOAD2' and goes into the SOGI controller to generate two sine waves 90 degrees out of phase. The SOGI controller output is based off the calculated value of the input signal frequency w_{PLL} . The PLL settles onto the correct input frequency quickly thanks to the PI controller, which then allows the two output phases to be correctly aligned. As these align the ABDQ controller outputs a phase V_q value that determines how aligned the input signal frequency is with the referenced theta value. V_q then is an input into a PI controller that amplifies and slows the signal slightly to prevent the output theta from becoming unstable. Without the PI controller the theta value would take much longer to settle and have worse stability if the input frequency was subject to changing.

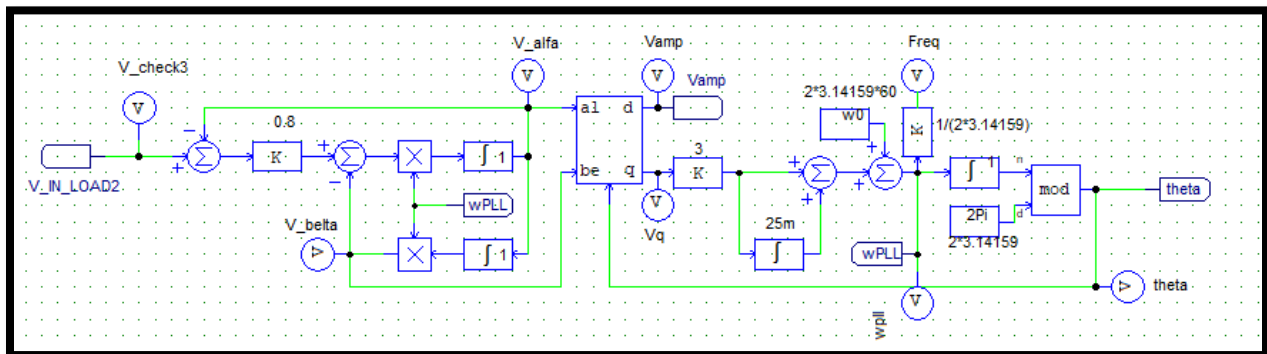


Figure 95 - PSIM Control PLL Generation

The second portion of control is shown in Figure 96. The first part is the MPPT logic, which creates a reference current value based on the auxiliary winding measurement. Many other MPPT methods exist using total input power or input and output currents, slowly adjusting values to find the optimal point. By using a secondary winding, a real input voltage can be measured and then divided by the harvester series resistance to get the current that provides maximum power. This logic is taken from the series RC circuit measurements and allow for much simpler MPPT management if the harvester series resistance is known. The reference current is then subtracted by the real input current, through a current loop operation, to create an error signal showing the difference between the optimal current and the real current, this error is shown in Figure 97.

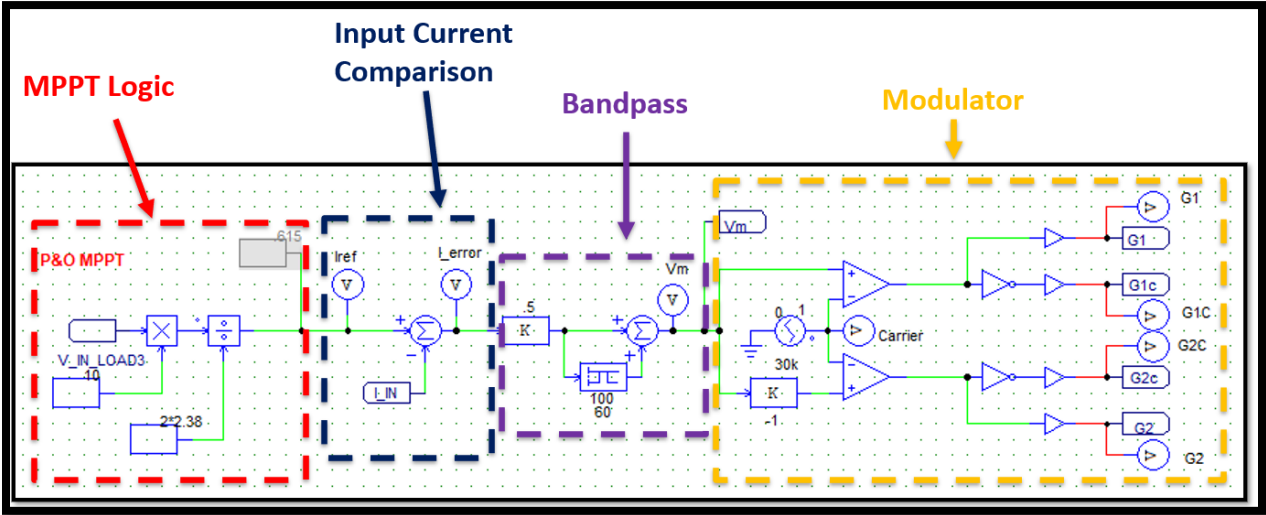


Figure 96 - PSIM Control MPPT and Current Loops

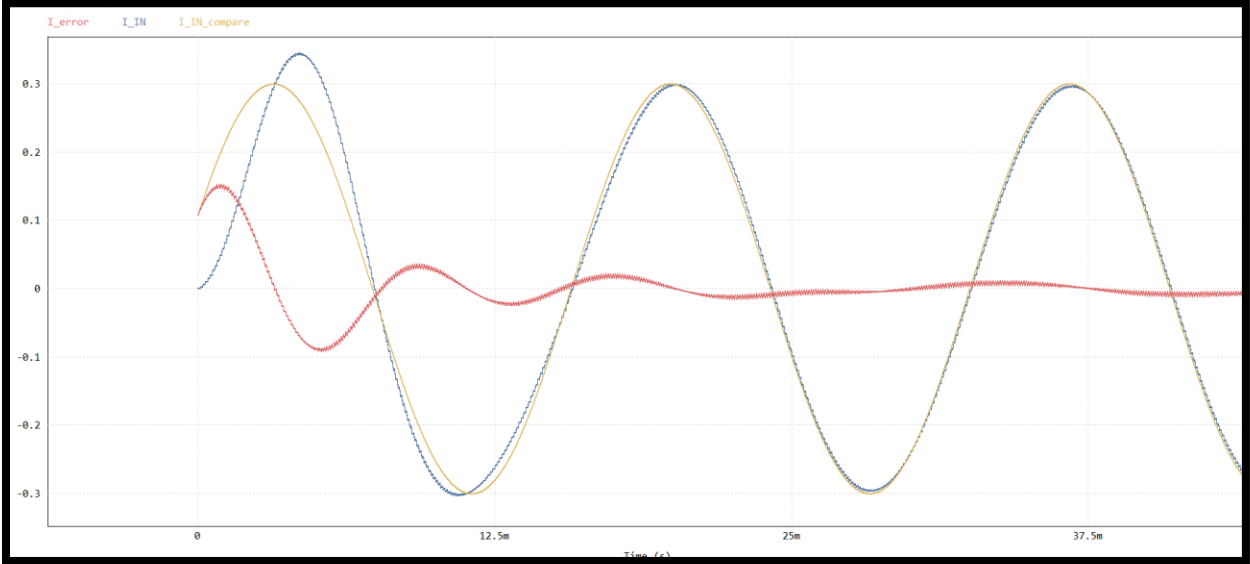


Figure 97 - Current Error Signal

The error is then sent through a bandpass filter, set for the line frequency, and has gain applied to boost the signal to modulation levels for comparison. Figure 98 shows the error signal and the final modulation signal 'VM' after the bandpass operation. With the control finalized the individual parts can be checked. Figure 99 shows the generated PLL signal aligned with the auxiliary voltage. Figure 100 shows the circuit operation with and without code running. Without code the circuit operates in purely passive mode though the four Shockley diodes across the mosfets. This allows for some power transfer but does not cancel out the inductance value or match the loads. The second waveform shows the current aligned with the auxillary voltage and that it has increased to the optimal current level. Figure 101 shows the moment that the output voltage raises above 15V, showing the MPPT being disabled and aux voltage and input current going out of phase. This occurs to prevent output voltage from raising above the safe levels. Figure 102 shows the bench test setup used for minimum power testing.

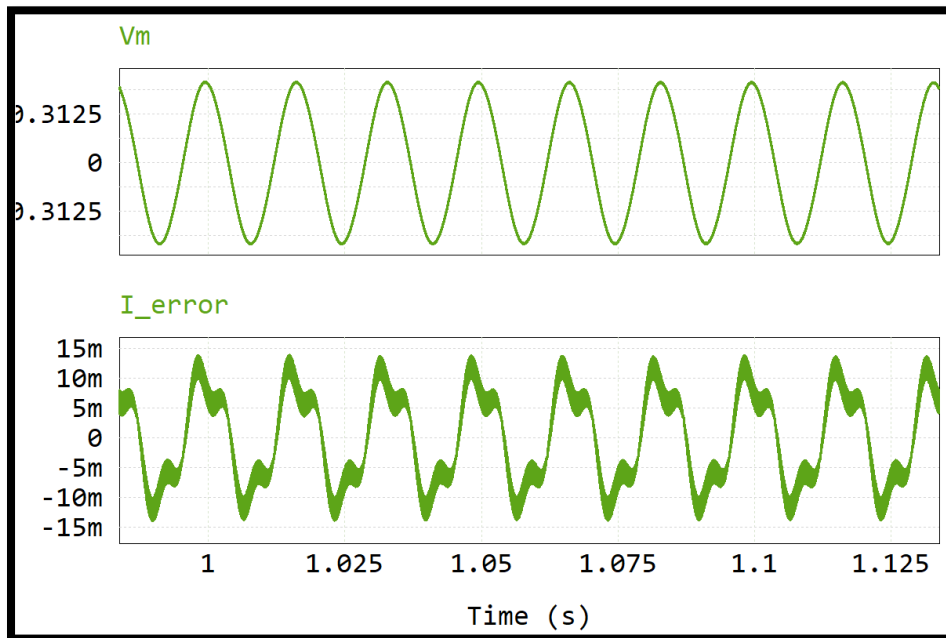


Figure 98 - Bandpass Operation

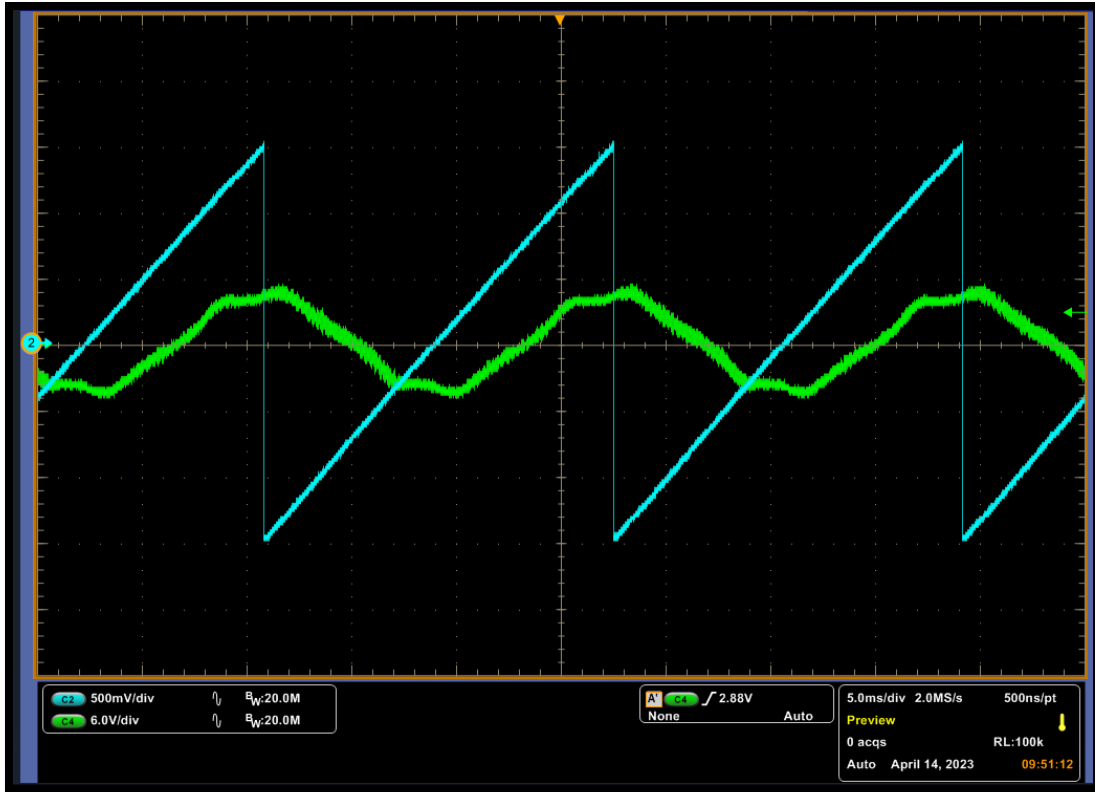


Figure 99 - PLL Example, B-theta, G-Aux Voltage

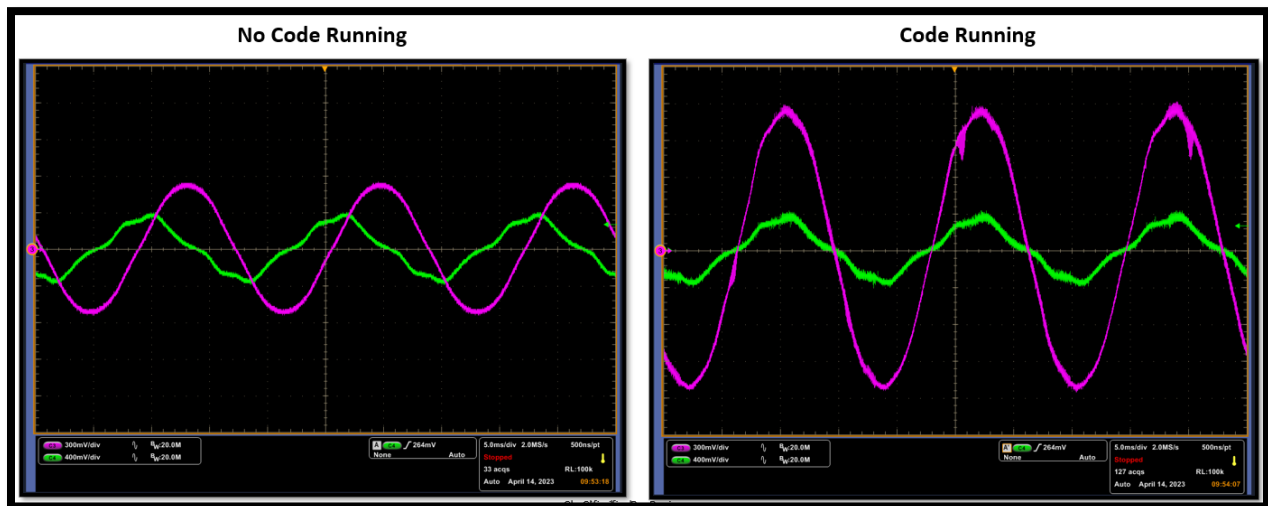


Figure 100 - Closed Loop Regulation, G-Aux Voltage, P-Input Current

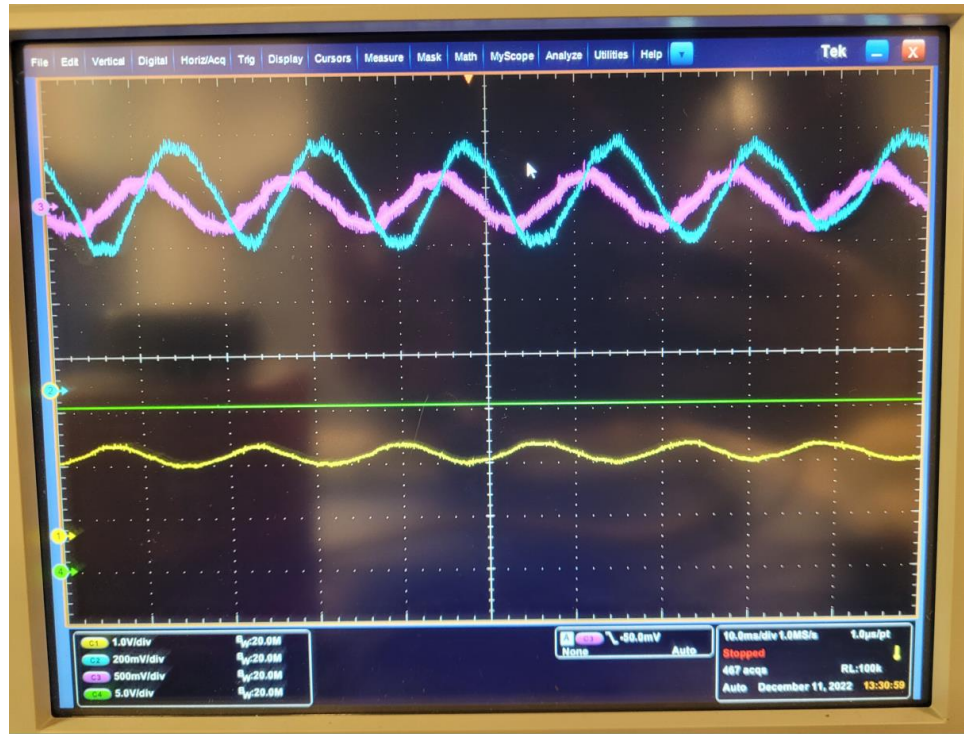


Figure 101 - Closed Loop Regulation Turned Off, P-Aux Voltage, B-Input Current, G-Output Voltage

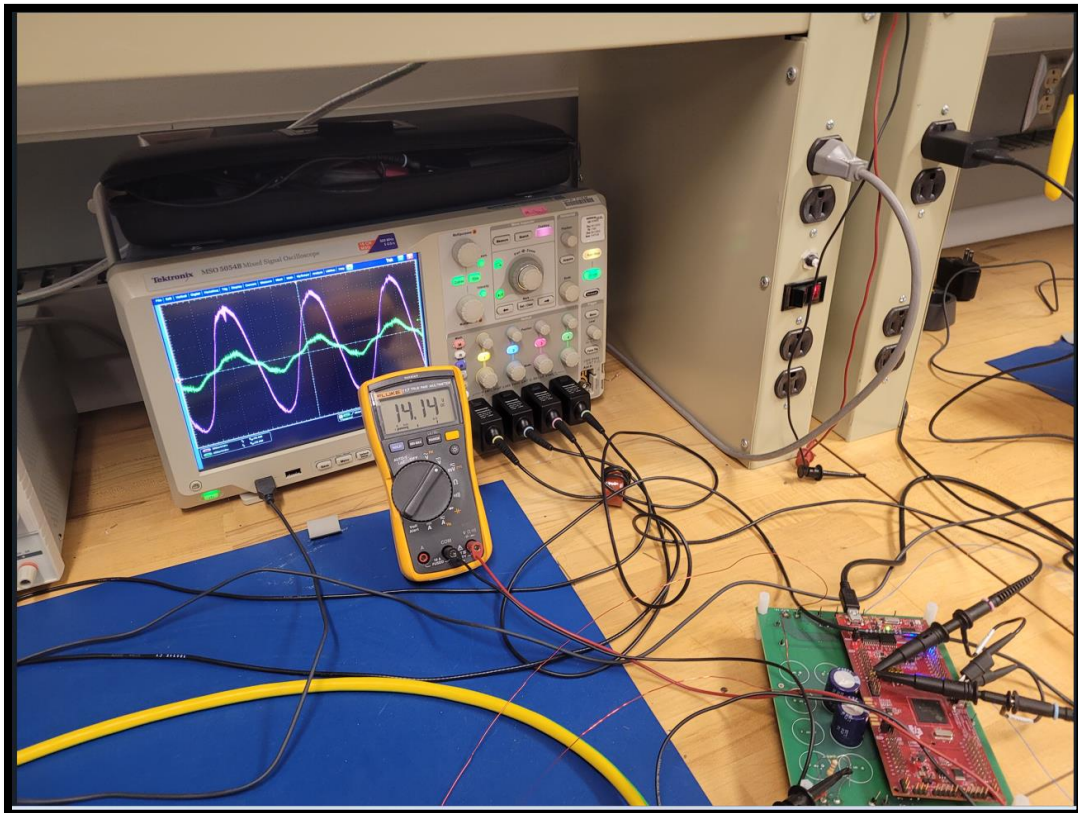


Figure 102 - Final PCBA Test Setup

Results and Maximum Power Transfer Theory Validation

To confirm that MPPT has been achieved a fixed IREF test was performed. Using the optimal calculated IREF value the set IREF value in the CCS code was changed to above and below the calculated optimal current. Figure 103 shows the results of this test when operating at a 1mT input value. Here the calculated optimal current peak is 316.8 mA and values of this were tested, above and below, in increments of 10mA. It's seen that a peak of 120.5mW is achieved and changing the set current to above or below that 316.8mA value only decreases total power. While this does increase the total current it also moves the input current out of alignment with the input voltage, dropping power. Figure 104 then shows the final power measurements for the harvester circuit from 0mT to 2mT max bench power. It's seen that the series RC circuit has the highest delivered power of 485mW while both the set IREF and MPPT control match quite closely and achieve a maximum of ~460mW. The matching of the IREF and MPPT results shows that the control can achieve MPPT accurately without being a set value. The difference of these values from the series RC circuit are the conduction, switching and gate losses from the designed circuit and give a converter efficiency of ~95%. It can be seen from Figure 102 that, at max bench power of 2mT, the MPPT circuit had a stable output of 14.14V over a load of 430.9ohms. This equates to an output of 464mW, in line with showed results.

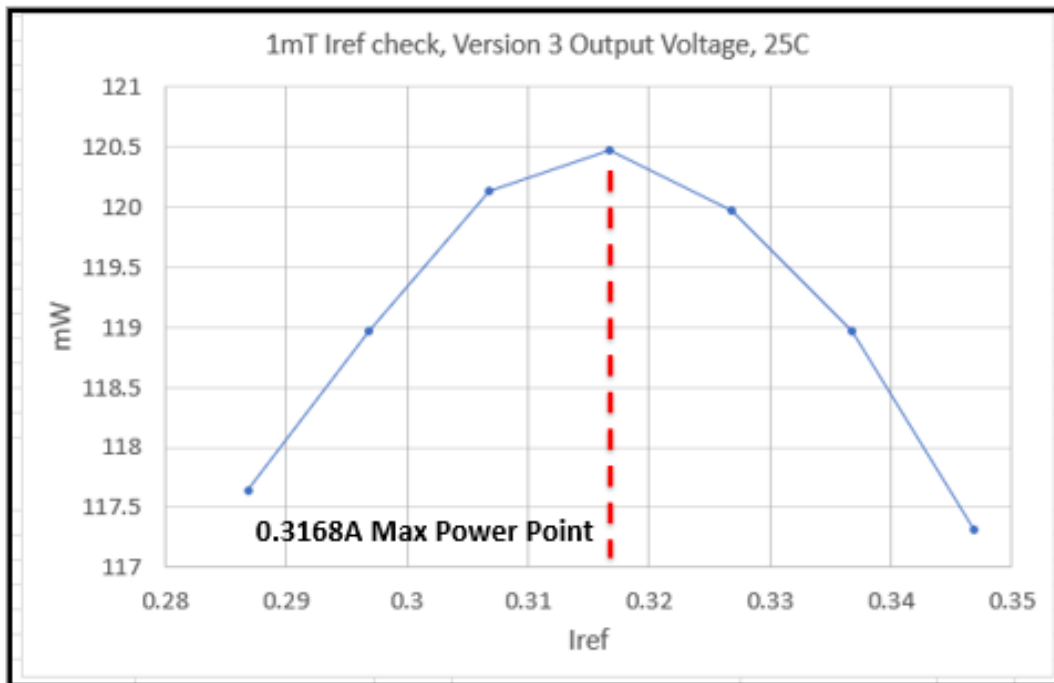


Figure 103 - MPPT Check

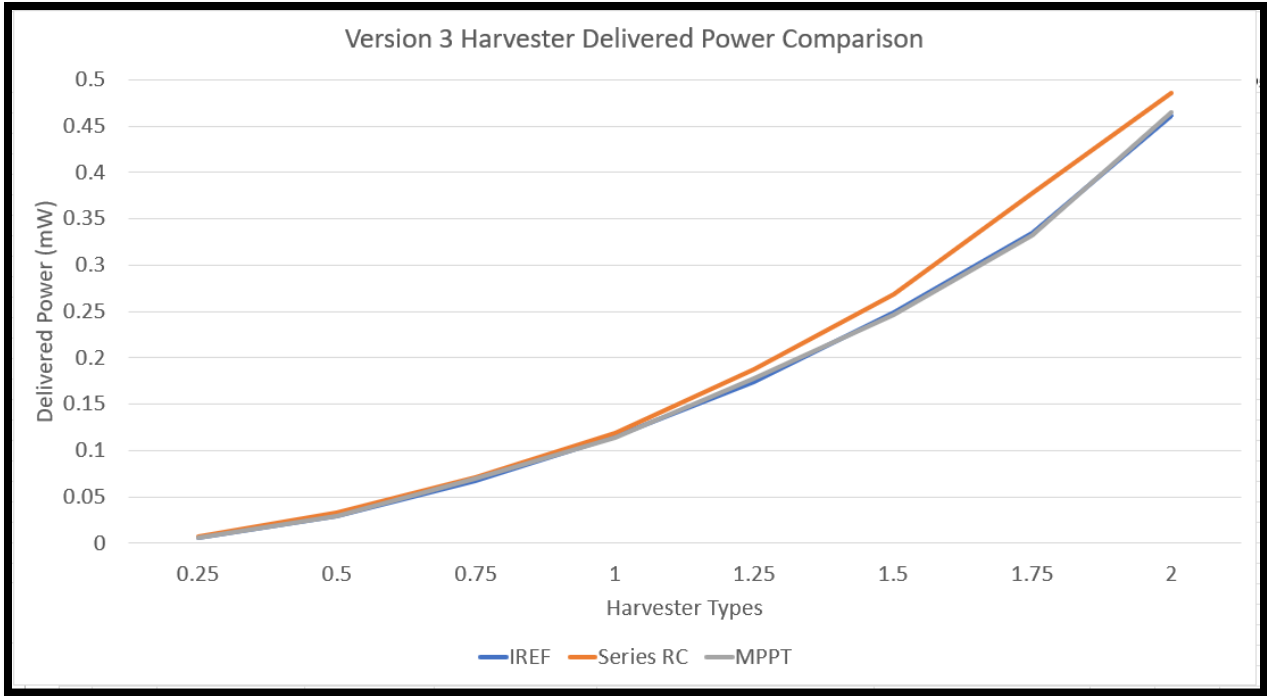


Figure 104 - Final Power Comparisons

Languages and Programming Methods

To program the MCU, CCS (Code Composer Studio) was used as the compiler to upload the digitized control onto the MCU. C-code was used as the language along with built in libraries for the TMS320F family of MCUs. CCS provided many examples of how to use the libraries and built-in functions to start the project, one of which related to the previously discussed challenges of lack of an FPU. Without the FPU on the MSP430F the only way to get similar performance was to convert the control into fixed point math. Figure 105 and Figure 106 show a comparison of these methods and the difficulty of implementing fixed point. While floating point math allows for the same variables to be retained in the digitized, fixed point requires each variable to first be scaled appropriately and then calculated with the correct format to not lose any bits of data. Unlike floating point that can accept a wide array of bit sizes and retain all data, fixed point will easily overflow and give erroneous signals. The time to implement fixed point can easily be several times longer than floating point, even with a dedicated library to work from. The benefits of fixed point however can outweigh the negatives, as this code can then run on smaller and lower power ICs while accomplishing the same calculations. The main things to understand with fixed point is that the exact range of inputs and outputs must be confirmed, otherwise the risk of overflow and erroneous signals can lead to unreliable system. The control was digitized into both FPU and fixed-point c-code to compare the benefits of each method, but ultimately the FPU code was chosen for reliability speed reasons.

```
//SOGI 2
Vin_error1=(-V_out*Vm)-(int1out);
//multiple error by 2
Vin_error_adj=Vin_error1*K; //origin:
Vin_error2=Vin_error_adj-((wpl1)*int2out);
int1in=wpl1*Vin_error2; //int1in=wpl1*Vir
```

Figure 105 - FPU Programming Method

```
//sogi 2
q11_Vin_error1=(q11_MainVoltage2-q11_MainVoltage1)-q11_int1out;
q11_Vin_error_adj=_Q15rsmpy(q11_Vin_error1,q15_oh_eight); //q11
q11_temp3=_Q9rsmpy(q5_wpl1,q15_int2out); //q11=q5,q11
q11_Vin_error2=q11_Vin_error_adj-q11_temp3;
q5_int1in=_Q11rsmpy(q5_wpl1, q11_Vin_error2); //q8=q5, q11
```

Figure 106 - Fixed point Programming Method

Conclusion and Future Work

This paper provided a guide to designing each aspect of an AC-DC converter for maximum power transfer. A magnetic field harvesting device was first designed and optimized to work inside a medium voltage AC drive. This harvester operates within a magnetic field strength range of 0mT to 2mT and outputs between 0V and 2.92V. A maximum 455mW output was designed for at max magnetic field strength while a minimum of 112mW was expected using bench testing at replicated minimum field strength. A PCBA was then designed that filtered out both induced switching noises and radiated EMI from the high magnetic field using commutation loops and bypass capacitors. Finally, a current loop scheme was then created in PSIM and then converted into C code on the TMS320F28379D launchpad. The control is made up of current loop and auxiliary winding measurement that are compared to achieve MPPT. The achieved MPPT operation outperforms the equivalent open loop method and matches set reference current outputs. It was observed that the controls PLL remained stable throughout testing, and the measured input current and auxiliary voltage lined up during closed loop operation; showing the power factor correcting needed for MPPT. The internal voltage limit, set to 15V out, also successfully disengaged the MPPT control to prevent over voltage on the output with a ripple voltage of 1.25% (200mV) on the output.

While many successes came out of this work, there are still many avenues of improvement to be done in the future. The optimization of the harvester did improve the harvesting density and efficiency; however, it did not improve the quantity of power harvested which could be increased through re-design of the harvester form factor. The Layout worked quite well, but the TMS320F28379D launchpad was never meant to be part of the layout itself. This IC could not be purchased at the time of this project, so a redesign using only the IC would allow proper accounting of those power requirements along with decreasing the size of the PCBA to match the harvester for better packaging. Finally, the code could still use optimization and potentially a lower power IC chosen. While the control was successfully converted into C code and run on the launchpad, it was left in floating point instead of being optimized into fixed point. By doing this, possibly a lower power MCU could be used to run the control. Finally, more work can be done related to total efficiency of the converter. A max efficiency of 47.8% was achieved out of a possible 50% from the maximum power transfer theory, when factoring in overall circuit efficiency. A higher percentage, and thus higher maximum power, could be achieved through re-evaluation of the control and the speed required to achieve power factor correction. There exist delays between the current being sensed and the MCU updating the reference current that reduces MPPT that could be reduced further. The test setup could also be improved to provide a consistent magnetic field, as the one used for bench testing likely was not accurate and led to lower power than expected.

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APPENDICES

Appendix A – Full Schematic and Layout Screenshots

Revision Description

Rev_Drawn	Rev_Appr.	Drawn	Description	Sheet name	Sheet Nr.
				PAGE1	(**)
Confidential				DrawingNo	Revision
				<Revision>	

Danfoss Drives
 Ranskanne SA
 06530 VAAASA
 FINLAND
 WWW.DANFOSS.COM

Legend:
 X14
 X15
 X16
 X17

Appendix B – Bill of Material

<u>Part Type</u>	<u>Where Used</u>	<u>Value</u>	<u>Quantity</u>	<u>Manufacturer part number</u>	<u>RefDes</u>
Gate Driver	PS	NCP3420DR2G	2	NCP3420DR2G	U4, U5
Mosfet	PS	IRLML6346TRPBF	4	IRLML6346TRPBF	V1, V2, V3, V4
Diode	Output Protection	20V	2	CZRB557B-HF	V12, V13
Diode	Mosfet Protection, Gate Driver	30V	6	DFLS130LQ-7	V5, V6, V7, V8, V9, V10
Capacitor	Gate Driver, 3.3V regulation, 5V regulation	1u	7	CL21B105KBFNFNE	C10, C11, C12, C13, C28, C29, C30
Capacitor	Output Capacitance	5300u	8	ELBK250ELL532AM20S	C39, C40, C41, C42, C43, C44, C45, C46
Capacitor	Output Capacitance Noise Filter, Output voltage divider noise filter	47n	6	N/A	C24, C25, C26, C27, C31, C47
Capacitor	Current Sense	100p	1	N/A	C6
Resistor	Output voltage divider, low pass filter, resistor dividers,	100k		N/A	R3, R4, R5, R6, R7, R8
Resistor	Output voltage divider	900k	1	N/A	R2, R4, R5, R6, R7, R8
Resistor	Current Sense	0.1	1	73M1R100F	R10
Standoff	Standoff	25523	4	25523	X14, X15, X16, X17
Current Sense IC	Current Measurement	LMP8601MA/NOPB	1	LMP8601MA/NOPB	U6

Appendix C - C code for Code Composer Studio

```
//  
// Included Files  
//  
#include "driverlib.h"  
#include "device.h"  
#include "board.h"  
#include "math.h"  
  
//  
// Defines  
//  
  
#define EPWM2_TIMER_TBPRD 3300 // Period register  
#define EPWM2_MAX_CMPA 3300  
#define EPWM2_MIN_CMPA 0  
#define EPWM2_MAX_CMPB 3300  
#define EPWM2_MIN_CMPB 0  
#define EPWM_CMP_UP 1  
#define EPWM_CMP_DOWN 0  
  
#define myGPIOOutput0 10  
  
uint16_t dacVal = 2048;  
  
#define EX_ADC_RESOLUTION 12
```

```

uint16_t adcAResult1;
uint16_t adcAResult2;
uint16_t adcAResult3;
uint16_t adcDResult0;
uint16_t adcDResult1;
uint16_t adcDResult2;

uint16_t Flag_Control=0;
uint16_t PWM_Test=0;

typedef struct
{

    uint32_t epwmModule;
    uint32_t epwmCompADirection;
    uint32_t epwmCompBDirection;
    uint32_t epwmTimerIntCount;
    uint32_t epwmMaxCompA;
    uint32_t epwmMinCompA;
    uint32_t epwmMaxCompB;
    uint32_t epwmMinCompB;
} epwmInfo;

epwmInfo epwm2Info;
volatile uint32_t compAVal, compBVal;

//

```

```

// Function Prototypes
//
void configureADC(uint32_t adcBase);
void initEPWM();
void initADCSOC(void);
__interrupt void adcA1ISR(void);
void initEPWM2(void);

__interrupt void epwm2ISR(void);

void updateCompare(epwmInfo*);

void configureDAC(void);
void __no_operation(void);

float Vm_Calc=0;

float xyz=0;
float V_out=5.0;
float Vin_Main1=0;
float Vin_Main2=0;
//sogi
float int3out=0;
float int3in=0;
float int3in_old = 0;

```

```
float int4out=0;
float Vin_Source=0;
float Vin_error12=0;
float Vin_error22=0;
float Vin_error_adj2=0;
float wpll=0;
//ab2dq
float vd2=0;
float vq2=0;
float v_alpha2=0;
float v_beta2=0;
float theta=0; //was 0;
//ppl
```

```
float freq=0;
float P_out=0;
float I_out=0;
float PI_out=0;
float mod_n=-1.2;
//float mod_n=0;
float mod_remainder=0;
```

```
float I_in1=0;
float I_in2=0;
```

```
float Vm_temp=0;
float PI_out1=0;
float P_out1=0;
```

```
float I_out1=0;
```

```
//sogi
```

```
float int1out=0;
```

```
float int1in=0;
```

```
float int1in_old = 0;
```

```
float int2out=0;
```

```
float Vin_error1=0;
```

```
float Vin_error2=0;
```

```
float Vin_error_adj=0;
```

```
//ab2dq
```

```
float vd=0;
```

```
float vd2nd=0;
```

```
float vd_previous=0;
```

```
float vq=0;
```

```
float v_alpha=0;
```

```
float v_alpha_squared=0;
```

```
float v_beta=0;
```

```
float v_beta_squared=0;
```

```
float wt=0;
```

```
//MPPT
```

```
float Vpv=0.0;
```

```
float Ipv=0.0;
```

```
float Ppv=0.0;
```

```

//double Iref=.1/64; fixed point
float Iref=.7; //was 0.7
//float Iref=0;
float Vac=0.0;
float Vpv_previous=0.0;
float Ppv_previous=0.0;
float deltaVpv=0.0;
float deltaPpv=0.0;
float lstep=0.001; //0.005 normal //was 0.005
//double lstep=0.005/64; //0.005 normal fixed point

float int5out=0;
//ZOH declarations
float previous_t=0.0; //Global update in ZOH
// PI / bandpass values and place holders
//float y[3] = {0,0,0};
float y_0=0;
float y_1=0;
float y_2=0;
//float u[3]= {0,0,0};
float u_0=0;
float u_1=0;
float u_2=0;
//float y_lp[3] = {0,0,0};
float y_lp_0=0;
float y_lp_1=0;

float y_lp_11=0;
float y_lp_01=0;

```

```
float u_lp_01=0;

//float u_lp[3]= {0,0,0};

float u_lp_0=0;
float u_lp_1=0;
//float y_lp_lin[3] = {0,0,0};
float y_lp_lin_0=0;
float y_lp_lin_1=0;
float y_lp_lin_2=0;
float y_lp_lin_3=0;
//y_lp_lin[0]=0.1;
//float u_lp_lin[3]= {0,0,0};
float u_lp_lin_0=0;
float u_lp_lin_1=0;
float u_lp_lin_2=0;
float u_lp_lin_3=0;

float y_lp_vd_0=0;
float y_lp_vd_1=0;
float u_lp1_lin_0=0;
float u_lp1_lin_1=0;
float y_lp1_lin_0=0;
float y_lp1_lin_1=0;
float y_lp1_vd_0=0;
float y_lp1_vd_1=0;
float u_lp_vd_0=0;
float u_lp_vd_1=0;
float vd_Final=0;
float y_lp_vout_0=0;
```

```
float y_lp_vout_1=0;
float u_lp_vout_0=0;
float u_lp_vout_1=0;
float vout_Final=0;
```

```
float u_terms=0;
float y_terms=0;
float Vm=1.0;
float Vm_Previous=0.0;
float id_ref=0;
float I_in=0;
float i_error=0;
float previous_t2=0.0; //Global update in ZOH
```

```
float count=5000;
float count2=5000;
```

```
float int3out_old=0;
float temp1=0;
float temp2=0;
float temp3=0;
float temp4=0;
float I_in_DC=0;
```

```
float Xtra1=0;
float Xtra2=0;
```

```
float Xtra3=0;
float Xtra4=0;
float t=0;
float t_old=0;
float I_in_Final=0;
float I_in_Final1=0;
```

```
float Vin_Main=0;
```

```
float E=1.65;
float F=13.3333;
float G=0.0001;
float H=.9999;
float G1=0.00001;
float H1=.99999;
float G2=0.001;
float H2=.999;
float G3=0.3;
float H3=.7;
float G4=0.001;
float H4=.999;
```

```
float I=0.9999;
```

```
float J=0.0001;
float K=0.8;
float L=0.5;
float L1=0.33;
float L2 = 0.1;
```

```
float L10=1;
float M=10;
float N=6.283185;
float O=376.9908;
float P = 0.159155; // 1/(2*PI)
float Q = 0.0471;
float Q1 = 0.471;
float Q2 = 0.01;
float Q3 = 0.00471;
float R = 1.999;
float S = 0.9991;
float R1 = 1.9;
float S1 = 0.9;
```

```
float T = 15.05;
float U = 3.3;
float V = 1.0/4096.0;
float W = 0.99;
float W1 = -0.99;
float W2=0.95;
float Y = 0.2;
float Z = 0.05;
float cos_theta=0;
float sin_theta=0;
float time100k=0.00001;
```

```
float adcAResult1_float=0;
float adcAResult1_float_prev=0;
```

```
float adcAResult2_float=0;
float adcAResult2_float_prev=0;
float adcAResult3_float=0;
float adcAResult3_float_prev=0;
float adcDResult1_float=0;
float adcDResult2_float=0;
float adcDResult3_float=0;
```

```
float u_lp_Vaux_0=0;
float y_lp_Vaux_0=0;
float y_lp_Vaux_1=0;
float Vaux_Final=0;
float Vaux=0;
```

```
float Boost_OpenLoop=.125;
```

```
void main(void)
```

```
{
```

```
    Device_init();
```

```
    Device_initGPIO();
```

```
    Interrupt_initModule();
```

```
    Interrupt_initVectorTable();
```

```
    Board_init();
```

```
    EALLOW;
```

```
    GPIO_setPinConfig(GPIO_18_GPIO18);
```

```
    GPIO_setDirectionMode(myGPIOOutput0, GPIO_DIR_MODE_OUT);
```

```

GPIO_setPadConfig(myGPIOOutput0, GPIO_PIN_TYPE_STD);
GPIO_setMasterCore(myGPIOOutput0, GPIO_CORE_CPU1);
GPIO_setQualificationMode(myGPIOOutput0, GPIO_QUAL_SYNC);
EDIS;
Interrupt_register(INT_EPWM2, &epwm2ISR);
Interrupt_register(INT_ADCA1, &adcA1ISR); ///ADC interrupt
configureADC(ADCA_BASE);
configureADC(ADCD_BASE);
SysCtl_disablePeripheral(SYSCTL_PERIPH_CLK_TBCLKSYNC);
initEPWM(); // this ePWM will be used to sync ADC sampling
initEPWM2();
SysCtl_enablePeripheral(SYSCTL_PERIPH_CLK_TBCLKSYNC);
initADCSOC();
Interrupt_enable(INT_EPWM2);
Interrupt_enable(INT_ADCA1);
EINT; // Enable Global interrupt INTM
ERTM; // Enable Global realtime interrupt DBGM
EPWM_enableADCTrigger(EPWM1_BASE, EPWM_SOC_A);
EPWM_setTimeBaseCounterMode(EPWM1_BASE, EPWM_COUNTER_MODE_UP);
configureDAC();

while(1)
{

    if (Flag_Control==1)
    {
        adcAResult1_float=10*adcAResult1*U*V; //aux DC
        adcAResult2_float=adcAResult2*U*V; //I_DC offset
        adcAResult3_float=10*adcAResult3*U*V; // Vout
    }
}

```

```
cos_theta=cosf(theta);
```

```
sin_theta=sinf(theta);
```

```
DAC_setShadowValue(DACA_BASE, 4096*(theta)/N);
```

```
Vin_Source=adcAResult1_float; //input * 3.3 /2000
```

```
// this removes the DC offset from lin
```

```
u_lp_lin_0=adcAResult2_float;
```

```
y_lp_lin_0=G*u_lp_lin_0+H*y_lp_lin_1;
```

```
I_in_Final=(adcAResult2_float-y_lp_lin_0);
```

```
y_lp_lin_1=y_lp_lin_0;
```

```
I_in=I_in_Final; //added '/2' because input current has a 20X gain over it when sampling over a  
1/10th resistor
```

```
// Vout adjusted and slowed once
```

```
V_out=adcAResult3_float; //increase by 10 to account for resistor divider
```

```
//SOGI
```

```
Vin_error12=Vin_Source-(int3out);
```

```
Vin_error_adj2=Vin_error12*K; //was *2 //Vin_error_adj2=Vin_error12*K; //was *2
```

```
Vin_error22=wpll*int4out; //Vin_error22=Vin_error_adj2-(wpll*int4out);
```

```
Vin_error22=Vin_error_adj2-Vin_error22; //Vin_error22=Vin_error_adj2-(wpll*int4out);
```

```
int3in=wpll*Vin_error22; //int3in=wpll*Vin_error22;
```

```
int3out = temp1 + L*(time100k)*int3in; //int3in_old
```

```

temp1=int3out+L*(time100k)*int3in;
int3in_old = int3in;
//backward euler
int4out = temp2 + L*(time100k)*int3out;
temp2= int4out + L*(time100k)*int3out;
// int3out_old=int3out;
//reset to here if things get worse
v_alpha2=int3out;
v_beta2=(wpll)*int4out; //v_beta2= wpll*int4out;
u_lp_0=Vin_error_adj2;
//u_lp[0]=Vin_error12;
y_lp_0=I*u_lp_0+(J)*y_lp_1; //I and J
v_beta2=(v_beta2-y_lp_0);
y_lp_1=y_lp_0;

//AB2DQ
vd2=cos_theta*v_alpha2+sin_theta*v_beta2;
vq2=-sin_theta*v_alpha2+cos_theta*v_beta2;

//multiply input by 3 as part of PI controller 'P'
//P_out=vq2*3.0; //vq2*3 normal
P_out=vq2*16.0;
//I_out = I_out+(time100k)*40*P_out; //.025 normal .25 works well // I_out = I_out+(t-
t_old)*P_out/(0.025); //.025 normal .25 works well
I_out = I_out+(time100k)*10*P_out;
PI_out=P_out+I_out;

```

```

wpll=PI_out+O;
freq=wpll*P;
mod_n=mod_n+(time100k)*wpll;
//mod_n=mod_n; //account for capacitive delays
theta=fmodf(mod_n,N);

if (mod_n >= N) //reduce mod_n so it does not overflow
{
    mod_n=mod_n-N;
}

Iref=vd2*5.1;

i_error=(Iref*cos_theta)-(I_in);

//i_error=(44.8*Vaux)-(I_in);

u_0=i_error;

// y_0=Q1*u_0-Q1*u_2-(-R1*y_1+S1*y_2);
y_0=Q1*u_0-Q1*u_2-(-R1*y_1+S1*y_2);

if (V_out <=T) //limit boost output to 60V or less
{
    //Vm=L*(i_error+2*y_0);
    Vm=L*(i_error+y_0);
}

```

```
}  
else if (V_out > T)  
{  
    //Vm=L*(i_error);  
    //Vm=2*(i_error-y_0);  
}
```

```
// Vm=L*(i_error+y_0);
```

```
u_2=u_1;
```

```
u_1=u_0;
```

```
y_2=y_1;
```

```
y_1=y_0;
```

```
Flag_Control=0;
```

```
//Vm=-cos_theta*0.125;
```

```
}
```

```

    }
}

// ADC A Interrupt 1 ISR
//
__interrupt void adcA1ISR(void)
{

    adcAResult1 = ADC_readResult(ADCARERESULT_BASE, ADC_SOC_NUMBER0);
    adcAResult2 = ADC_readResult(ADCARERESULT_BASE, ADC_SOC_NUMBER1);
    adcAResult3 = ADC_readResult(ADCARERESULT_BASE, ADC_SOC_NUMBER2);
    adcDResult0 = ADC_readResult(ADCDCRESULT_BASE, ADC_SOC_NUMBER0);
    adcDResult1 = ADC_readResult(ADCDCRESULT_BASE, ADC_SOC_NUMBER1);
    adcDResult2 = ADC_readResult(ADCDCRESULT_BASE, ADC_SOC_NUMBER2);

    ADC_clearInterruptStatus(ADCA_BASE, ADC_INT_NUMBER1);

    if(true == ADC_getInterruptOverflowStatus(ADCA_BASE, ADC_INT_NUMBER1))
    {
        ADC_clearInterruptOverflowStatus(ADCA_BASE, ADC_INT_NUMBER1);
        ADC_clearInterruptStatus(ADCA_BASE, ADC_INT_NUMBER1);
    }

    Interrupt_clearACKGroup(INTERRUPT_ACK_GROUP1);
    Flag_Control=1;
}

// epwm2ISR - EPWM2 ISR to update compare values
//

```

```
__interrupt void epwm2ISR(void)
```

```
{
```

```
    updateCompare(&epwm2Info);
```

```
    EPWM_clearEventTriggerInterruptFlag(myEPWM2_BASE);
```

```
    Interrupt_clearACKGroup(INTERRUPT_ACK_GROUP3);
```

```
}
```

```
void initEPWM(void)
```

```
{
```

```
    EPWM_disableADCTrigger(EPWM1_BASE, EPWM_SOC_A);
```

```
    EPWM_setADCTriggerSource(EPWM1_BASE, EPWM_SOC_A, EPWM_SOC_TBCTR_U_CMPA);
```

```
    EPWM_setADCTriggerEventPrescale(EPWM1_BASE, EPWM_SOC_A, 1);
```

```
    EPWM_setCounterCompareValue(EPWM1_BASE, EPWM_COUNTER_COMPARE_A, 0);
```

```
    EPWM_setTimeBasePeriod(EPWM1_BASE, 999);
```

```
    EPWM_setClockPrescaler(EPWM1_BASE, EPWM_CLOCK_DIVIDER_1, EPWM_HSCLOCK_DIVIDER_1);
```

```
    EPWM_setTimeBaseCounterMode(EPWM1_BASE, EPWM_COUNTER_MODE_STOP_FREEZE);
```

```
}
```

```
void initEPWM2()
```

```
{
```

```
    EPWM_setTimeBaseCounterMode(myEPWM2_BASE, EPWM_COUNTER_MODE_DOWN);
```

```
    EPWM_setTimeBasePeriod(myEPWM2_BASE, EPWM2_TIMER_TBPRD);
```

```
    EPWM_disablePhaseShiftLoad(myEPWM2_BASE);
```

```
    EPWM_setPhaseShift(myEPWM2_BASE, 0U);
```

```
    EPWM_setTimeBaseCounter(myEPWM2_BASE, 0U);
```

```
EPWM_setClockPrescaler(myEPWM2_BASE, EPWM_CLOCK_DIVIDER_1,  
EPWM_HSCLOCK_DIVIDER_1);
```

```
EPWM_setCounterCompareShadowLoadMode(myEPWM2_BASE, EPWM_COUNTER_COMPARE_A,  
EPWM_COMP_LOAD_ON_CNTR_ZERO);
```

```
EPWM_setCounterCompareShadowLoadMode(myEPWM2_BASE, EPWM_COUNTER_COMPARE_B,  
EPWM_COMP_LOAD_ON_CNTR_ZERO);
```

```
EPWM_setCounterCompareValue(myEPWM2_BASE, EPWM_COUNTER_COMPARE_A,  
EPWM2_MIN_CMPA);
```

```
EPWM_setCounterCompareValue(myEPWM2_BASE, EPWM_COUNTER_COMPARE_B,  
EPWM2_MAX_CMPB);
```

```
EPWM_setActionQualifierAction(myEPWM2_BASE, EPWM_AQ_OUTPUT_A,  
EPWM_AQ_OUTPUT_LOW, EPWM_AQ_OUTPUT_ON_TIMEBASE_PERIOD);
```

```
EPWM_setActionQualifierAction(myEPWM2_BASE, EPWM_AQ_OUTPUT_A,  
EPWM_AQ_OUTPUT_HIGH, EPWM_AQ_OUTPUT_ON_TIMEBASE_DOWN_CMPA);
```

```
EPWM_setActionQualifierAction(myEPWM2_BASE, EPWM_AQ_OUTPUT_B,  
EPWM_AQ_OUTPUT_LOW, EPWM_AQ_OUTPUT_ON_TIMEBASE_PERIOD);
```

```
EPWM_setActionQualifierAction(myEPWM2_BASE, EPWM_AQ_OUTPUT_B,  
EPWM_AQ_OUTPUT_HIGH, EPWM_AQ_OUTPUT_ON_TIMEBASE_DOWN_CMPB);
```

```
EPWM_setInterruptSource(myEPWM2_BASE, EPWM_INT_TBCTR_ZERO);
```

```
EPWM_enableInterrupt(myEPWM2_BASE);
```

```
EPWM_setInterruptEventCount(myEPWM2_BASE, 1U);
```

```
// Start by increasing CMPA & decreasing CMPB
```

```
epwm2Info.epwmCompADirection = EPWM_CMP_UP;
```

```
epwm2Info.epwmCompBDirection = EPWM_CMP_DOWN;
```

```
// Clear interrupt counter
```

```
epwm2Info.epwmTimerIntCount = 0;
```

```
// Set base as ePWM2
```

```

epwm2Info.epwmModule = myEPWM2_BASE;
// Setup min/max CMPA/CMP values
epwm2Info.epwmMaxCompA = EPWM2_MAX_CMPA;
epwm2Info.epwmMinCompA = EPWM2_MIN_CMPA;
epwm2Info.epwmMaxCompB = EPWM2_MAX_CMPB;
epwm2Info.epwmMinCompB = EPWM2_MIN_CMPB;

}

// updateCompare - Update the compare values for the specified EPWM
//
void updateCompare(epwmInfo *epwm_info)
{

if (Vm>=0) //check where sinewave is, is positive then run first leg and zero second leg
{
    //Vm=-Vm;
    //if (Vm>W2) //0.95
    Vm_Calc=Vm*4095;

    if (Vm_Calc>4000)
    {
        Vm_Calc=4000;
    }
    else
    {
        //Vm_Calc=Vm*4095;
    }
}
}

```

```

if (Vm_Calc < 100)
{
    Vm_Calc=100;
}

EPWM_setCounterCompareValue(epwm_info->epwmModule, EPWM_COUNTER_COMPARE_A, 0);

    EPWM_setCounterCompareValue(epwm_info->epwmModule, EPWM_COUNTER_COMPARE_B,
Vm_Calc);
}
else if (Vm<0) //check where sinewave is, is negative then run second leg and zero first leg
{
    //Vm=-Vm;
    Vm_Calc=-Vm*4095;
    if (Vm_Calc>4000) //0.95
    {
        Vm_Calc=4000;
    }
    else
    {
        //Vm_Calc=-Vm*4095;
    }

    if (Vm_Calc < 100)
    {
        Vm_Calc=100;
    }
}

```

```
    EPWM_setCounterCompareValue(epwm_info->epwmModule, EPWM_COUNTER_COMPARE_A,  
Vm_Calc);
```

```
    EPWM_setCounterCompareValue(epwm_info->epwmModule, EPWM_COUNTER_COMPARE_B, 0);
```

```
}
```

```
return;
```

```
}
```

```
void configureADC(uint32_t adcBase)
```

```
{
```

```
    //
```

```
    // Set ADCCLK divider to /4
```

```
    //
```

```
    ADC_setPrescaler(adcBase, ADC_CLK_DIV_4_0);
```

```
#if(EX_ADC_RESOLUTION == 12)
```

```
    ADC_setMode(adcBase, ADC_RESOLUTION_12BIT, ADC_MODE_SINGLE_ENDED);
```

```
#elif(EX_ADC_RESOLUTION == 16)
```

```
    ADC_setMode(adcBase, ADC_RESOLUTION_16BIT, ADC_MODE_DIFFERENTIAL);
```

```
#endif
```

```
    ADC_setInterruptPulseMode(adcBase, ADC_PULSE_END_OF_CONV);
```

```
    ADC_enableConverter(adcBase);
```

```
    DEVICE_DELAY_US(1000);
```

```

}

void initADC SOC(void)
{
    uint16_t acqps;

    if(EX_ADC_RESOLUTION == 12)
    {
        acqps = 14; // 75ns
    }
    else //resolution is 16-bit
    {
        acqps = 63; // 320ns
    }

    ADC_setupSOC(ADCA_BASE, ADC_SOC_NUMBER0, ADC_TRIGGER_EPWM1_SOC,
        ADC_CH_ADCIN1, acqps);
    ADC_setupSOC(ADCA_BASE, ADC_SOC_NUMBER1, ADC_TRIGGER_EPWM1_SOC,
        ADC_CH_ADCIN2, acqps);
    ADC_setupSOC(ADCA_BASE, ADC_SOC_NUMBER2, ADC_TRIGGER_EPWM1_SOC,
        ADC_CH_ADCIN3, acqps);
    ADC_setupSOC(ADCD_BASE, ADC_SOC_NUMBER0, ADC_TRIGGER_EPWM1_SOC,
        ADC_CH_ADCIN2, acqps);
    ADC_setupSOC(ADCD_BASE, ADC_SOC_NUMBER1, ADC_TRIGGER_EPWM1_SOC,
        ADC_CH_ADCIN3, acqps);
    ADC_setupSOC(ADCD_BASE, ADC_SOC_NUMBER2, ADC_TRIGGER_EPWM1_SOC,
        ADC_CH_ADCIN4, acqps);

    ADC_setInterruptSource(ADCA_BASE, ADC_INT_NUMBER1, ADC_SOC_NUMBER2);

```

```
ADC_enableInterrupt(ADCA_BASE, ADC_INT_NUMBER1);
ADC_clearInterruptStatus(ADCA_BASE, ADC_INT_NUMBER1);
}

void __no_operation(void)
{
    ;
}

void configureDAC(void)
{

    DAC_setReferenceVoltage(DACA_BASE, DAC_REF_ADC_VREFHI);

    DAC_enableOutput(DACA_BASE);

    DAC_setShadowValue(DACA_BASE, 0);

    DEVICE_DELAY_US(10);
}

//
// End of file
//
```