ABSTRACT

ZHAO, WENXU. RF-only Logic Enabled RFID Transponder Size Reduction. (Under the direction of Dr. Paul D. Franzon.)

Low-power passive wireless devices are the key enablers of the emerging internet-of-things. These passive devices harvest RF power from ambient or dedicated sources for circuit operations. RF-DC rectifiers are usually used in these devices to generate the local DC power supply from the harvested RF signals. The RF-DC rectifier and storage capacitor often consume at least 25% of the chip area if not more, thus introducing additional cost for these cost-sensitive applications. In this dissertation, we have presented a new logic family that permits digital operations directly with an AC power supply, thus eliminating the need for RF-DC rectifier and reducing chip cost. We analyzed its characteristics and synthesized its system design methodology. An UHF Gen-2 compliant RFID tag has been developed using RF-only logic to demonstrate its advantages on area saving.

RF-only Logic Enabled RFID Transponder Size Reduction

by
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DEDICATION

To my parents Chunming Zhao, Yuli Qu and wife Wei Li

To all the happiness and suffering along the way

BIOGRAPHY

I have been waiting for this moment for years, and I am glad I make it to this point. I was born in Taiyuan, China and spent my first 19 years there until completion of high school. After that, I spent four years at Fudan University in Shanghai for my undergraduate study. I started my graduate study in NC State University in 2010. Throughout the past six and half years, I have participated in two interesting yet tough research projects, interned at Cirrus Logic in 2013 and nVidia Research in 2016, assisted teaching of four graduate courses. And finally here I am: a circuit design graduate ready to adventure the real world.

ACKNOWLEDGMENTS

It is snowing again in Raleigh, just like the first winter I started my journey of graduate study at NC State University. I have been waiting for this moment for years, and I am glad I make it to this point. It has been a luxury for me to design integrated circuits with a stable DC power supply, and I do cherish the fun and suffering along the way. There have been many people who have walked alongside me during the last six and half years. They have guided me, placed opportunities in front of me, and showed me the doors that might be useful to open. Now is an unforgettable moment for me to thank all the people I am deeply indebted to.

First, I would like to thank Professor Paul Franzon, my advisor, for his mentorship and guidance throughout this endeavor. I am lucky to have been part of his group, which exposed me to a wealth of different research areas. He always cared whether I enjoyed my work and was always supportive and optimistic during the ups and downs of research. His spirits as the everlasting beacon of hope are definitely one of the things I miss most after leaving NCSU. I would also like to thank Professor Brain Floyd for his help and support on many occasions, for his excellent Analog Electronics and RFIC courses, and for those valuable comments on my work. I am grateful to Professor Rhett Davis and Jesse Jur for being on my committee and for their comments and feedback on my work.

My particular thanks go to Dr. Steve Lipa for his incredibly knowledgeable feedbacks on my work and his patient support on those measurement days and nights. I had the pleasure of sharing much of my time with my fellow group members. They provided friendship and

interesting discussions on various topics. I was fortunate to intern at nVidia Research and got to know these incredible colleagues. Their encouraging stories enlightened me and helped me went over the last few months of my Ph.D. time.

Finally, I would like to thank my parents and wife for their love and support. I appreciate their sacrifices, and I would not have been able to get to this stage without them. They are the source of my determination and perseverance in pursuing all my endeavors. I enjoyed the decisions we made together, along with all the complaints and happiness.

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Introduction

1.1 Motivation

Low-power and low-cost wireless devices are the key enablers of the emerging internet-of-things (IoT). IoT devices provide connectivity to a broad variety of objects. Passively-powered wireless nodes, compared with their battery-assisted counterparts, reduce cost and minimize their footprints. By eliminating the battery, it mitigates battery depletion problem and extends device lifetime. Having a miniaturized form factor and being battery-less are highly desirable.

A passive wireless device usually scavenges energy from external sources such as propagation radio waves, solar radiation, thermal energy, and kinetic energy. Power harvesting from either ambient or directed radio frequency (RF) source using a power rectifier is one of the most popular methods as shown in Figure 1.1. The RF power incident

on the device is rectified into a DC voltage using a rectifier. On-chip capacitors store the harvested energy as a reservoir and reduce power level fluctuations during operation.

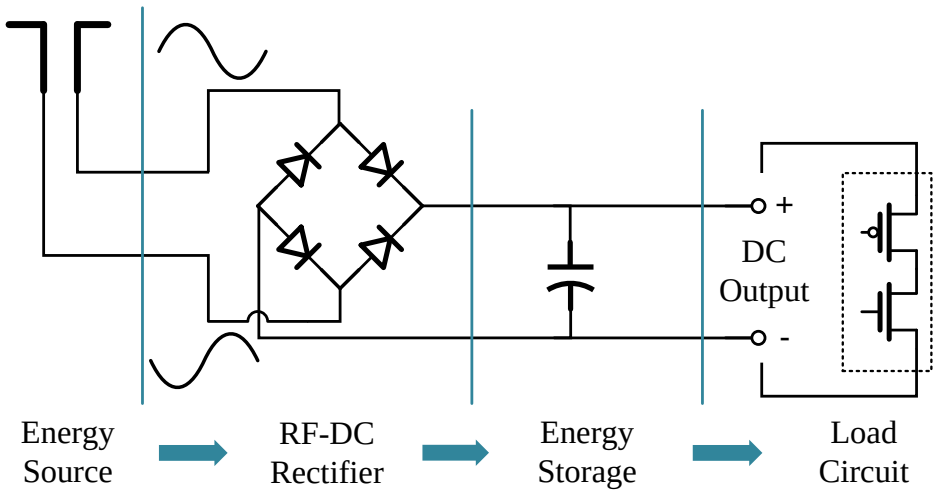
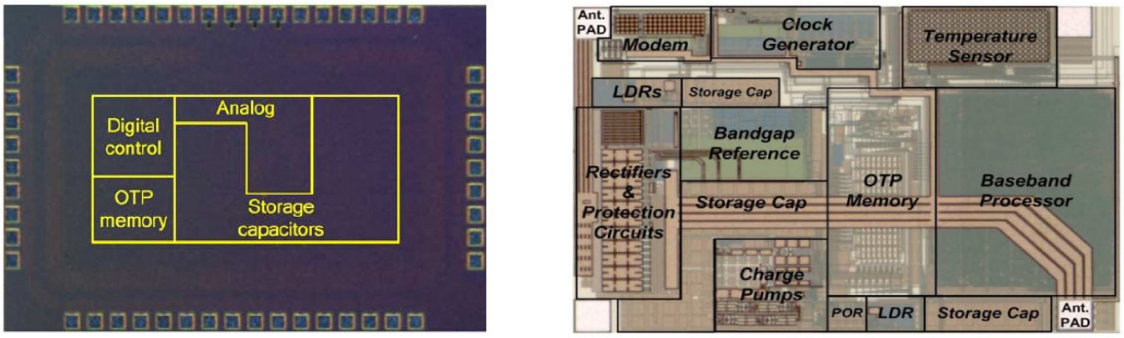


Figure 1.1 Power solution front-end for passively-powered wireless devices

Most low power radios in wireless applications are fabricated in Complementary metal-oxide-semiconductor (CMOS) technology. The rectifiers are usually fully integrated for low cost and small form factor purpose. The transistors of a rectifier are usually large to reduce the resistive power loss. The minimum amount of storage capacitance is defined by the maximum allowed supply voltage variation and the energy budget for duty-cycled operations. These design considerations usually lead to a minimum on-chip storage capacitor in the hundreds of pF range, which takes significant amount of chip area in CMOS technology. Therefore, the AC-DC rectifier based powering solution for passive wireless devices takes up considerable chip area. Inspecting their chip layouts usually indicates that these functions take up 25% or more of the chip area [1] [2] [3] [4].



(a) [1] (b) [2]

Figure 1.2 Die photos of sample RFID chips showing the area used for power rectifier and storage capacitors

Therefore, it would be desirable to make the received RF signal useful without the need to perform an RF-to-DC power conversion. If the RF-DC rectifier and the storage capacitors can be eliminated while maintaining reasonable robust operations, it will reduce the design complexity and cost of passive wireless devices.

1.2 Proposed Solution and Original Contributions

The RF-only logic was proposed for passive wireless devices and helps to eliminate the need for AC-DC rectifier [5]. The RF-only logic family supports direct operation with AC power supply instead of DC. Figure 1.3 presents the basic circuit structure and operations of

an RF-only inverter. Therefore, the passive wireless devices designed using RF-only logic can operate directly with the recovered RF signals without rectification.

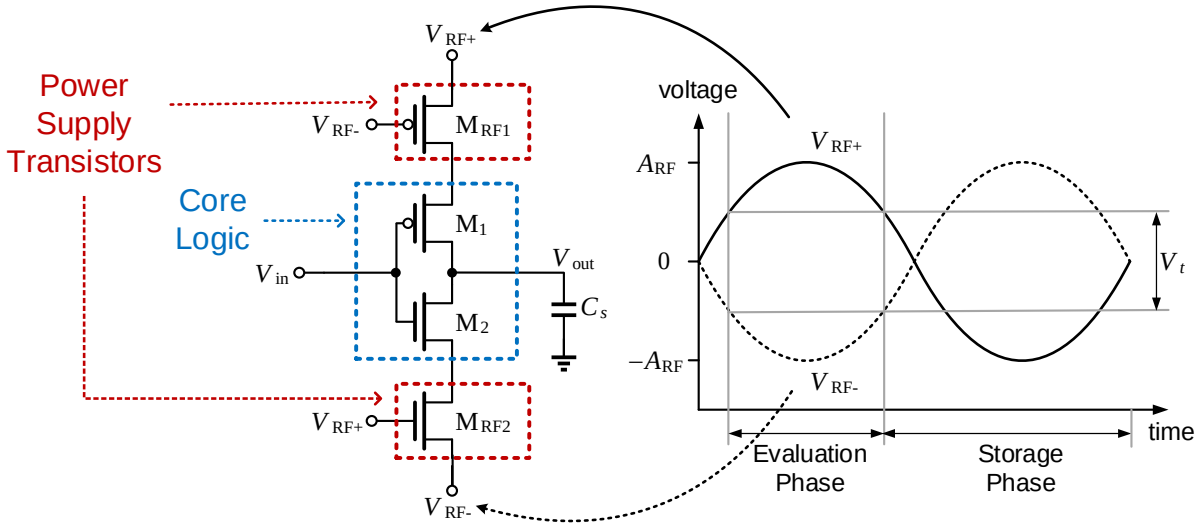


Figure 1.3 Basic structure and operations of RF-only logic

In this dissertation, we investigated the feasibility of building the rectifier-free passive devices using RF-only logic from both circuit and system levels. Critical circuits were analyzed, design challenges and potential risks were identified and tackled. This work includes the following major original contributions:

- Analyzed the characteristics of single-phase RF-only circuits, which included propagation delay, power consumption, and robustness of logic operations. Several test circuits were designed, fabricated, and measured to verify the analysis.

- Designed and characterized the first standard cell library for RF-only logic in 0.13μm CMOS technology.
- Analyzed the optimal operating conditions of RF-only logic for various application scenarios from a design perspective. Introduced a system design methodology for designing with RF-only logic.
- Developed an algorithm for sharing power supply transistors among mutually exclusive gates to reduce area overhead of the RF-only logic. Incorporated the algorithm into digital design flow.
- Designed a rectifier-free EPC Class-1 Generation-2 compliant radio frequency identification (RFID) tag using RF-only logic to demonstrate the proposed circuit and system level techniques.

1.3 Related Works

AC-powered circuits have been investigated primarily in the scenario where there is an available AC power source. These prior works all targeted at either lowering the circuit power consumption or reducing the chip area. Table 1.1 summarizes the related works on the AC-powered circuit and classifies them into three categories based on the AC source frequency and the supported data rate.

Table 1.1 Summary of state-of-the-art works on AC-powered circuits

Frequency relation	Work	Power	Area
AC < Clock	Wenck [6]	-	reduce
AC = Clock	Adiabatic [7]	reduce	increase
AC > Clock	Gadfort [5]	increase	reduce/increase
	Briole [8]	-	reduce

Adiabatic logic was first proposed to achieve near-zero power dissipation, by ensuring that the potential across the switching devices was kept close to zero. Therefore, almost no energy would be dissipated as heat on the switch while energy stored on the capacitor could be recycled [9] [7]. This was achieved by linearly ramping the supply voltage up and down between *VDD* and *VSS*, at a period of *T*, which was much larger than the RC time constant of the switch. Adiabatic logic primarily trades off power consumption with area.

He and Min [10] have implemented all the digital building blocks of a Low Frequency (LF) RFID tag with adiabatic logic, while kept a rectifier-based DC power supply for the remaining analog blocks. Mok and Chan [11] proposed a High Frequency (HF) RFID tag fully implemented with adiabatic logic to reduce the chip area and power consumption by directly powering the logics with the RF carrier. The intrinsic area overhead of adiabatic logic offsets the potential area saving obtained by eliminating the rectifier in both of these two works.

Wenck [6] proposed to power the conventional CMOS digital circuits using the harvested AC voltage, while the RF frequency had to be orders of magnitude lower than the data path clock frequency. For each power supply cycle, the load circuit must be powered on, perform computation, and turn off sequentially. In addition, dynamic memory cells were implemented to preserve states between power supply cycles. Substantial chip area was dedicated to power level detection and data retention memory.

Briole [8] proposed and implemented a dual phase AC-powered logic circuit, in which the AC frequency was orders of magnitude higher than the clock frequency. However, the doubling of transistor counts and the overhead of transmission gates did not lead to area saving. Gadfort [5] has proposed and implemented an RF-only logic family that worked directly from an AC power supply, whose frequency was orders of magnitude higher than the logic circuit data rate. While silicon results were shown to prove the concept, no analysis about its characteristics was presented on the logic family. Ledford [12] also proposed and implemented RF-only logic based static random-access memory (SRAM) bit cells.

1.4 Dissertation Outline

This dissertation is organized as follows. In Chapter 2, the characterization of RF-only logic is analyzed, including its structure, operation, propagation delay, power consumption, and robustness of operation. Chapter 3 discusses the design methodology and considerations for designing with RF-only logic at the system level. Several application scenarios are

presented, and the optimal operating conditions are introduced along with simulated results. In Chapter 4, the design of a passive ultra-high frequency (UHF) Class-1 Gen-2 compliant RFID tag using RF-only logic is presented as a case study. The key design considerations and implementation of both circuit and system level are discussed. Summary and future work are given in Chapter 5.

Chapter 2

RF-only Logic: An Area-Efficient AC-Powered Logic Family

In this chapter, we discuss the RF-only logic, a novel AC-powered logic [5]. RF-only logic achieves area savings for passively-powered wireless nodes by eliminating the need for AC-DC rectifier and the storage capacitors. We first analyze the structure and operations of the single-phase RF-only logic, and subsequently consider its dynamic performance (delay), power consumption, and robustness of logic operations. These metrics are characterized as a function of amplitude and frequency of the RF power source. An RF-only inverter is used as a sample throughout this chapter's analysis. Circuit level design considerations, limitations, and trade-offs are also presented throughout this chapter.

2.1 Circuit Structure

The RF-only logic is a dual-rail, AC-powered logic. There are two types of RF-only logic as shown in Figure 2.1: single phase which utilizes only half of the RF cycle and dual phase which utilizes the full RF cycle [5]. In this chapter, we focus on the analysis of the single-phase RF-only logic.

The structure of an RF-only logic can be divided into two parts: the logic evaluation part ("Core Logic") and a set of power supply transistors ("PST") M_{RF1} and M_{RF2}. The core logic can be implemented in different topologies such as conventional CMOS or transmission gates [5]. This work focuses on the conventional CMOS-based implementation. The power supply transistors supply current to the circuit when the RF supply permits the circuit to operate, and they limit the leakage current when the supply cannot power the circuit. The output capacitance C_s represents the sum of the parasitic capacitance at the output node. It stores the charges on the output node to retain the voltage level when the power supply transistors are off. From a system perspective, the power supply transistors form a distributed power rectifying structure, which is custom-designed to meet the local charging pattern and power requirements.

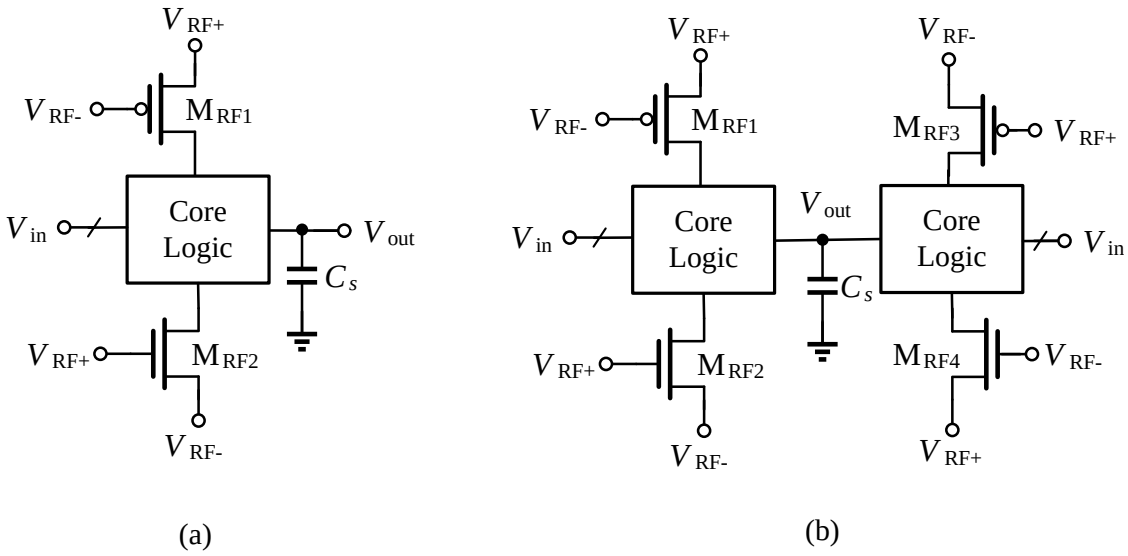


Figure 2.1 Generic structure of the RF-only logic gate. It consists of a logic evaluation part (Core Logic) and a set of power supply transistors (a) single phase (b) dual phase

2.2 Circuit Operations

The single-phase RF-only inverter shown in Figure 2.2(a) is used to illustrate the operations of RF-only logic, with the applied RF signals shown in Figure 2.2(b). There are two operating phases based on the operating regions of the power supply transistors. The evaluation phase: when $V_{RF+} - V_{RF-} > V_L$, where V_L is given by Equation (2.1) [13]. V_L is the minimum voltage for a metal-oxide-semiconductor (MOS) channel to be in weak inversion:

$$V_L = V_{FB} + \phi_F + \gamma\sqrt{\phi_F + V_{sb}} \tag{2.1}$$

where V_{FB} is the transistor flat-band voltage, ϕ_F is the Fermi potential, V_{sb} is the source to body voltage, and γ is the body effect coefficient.

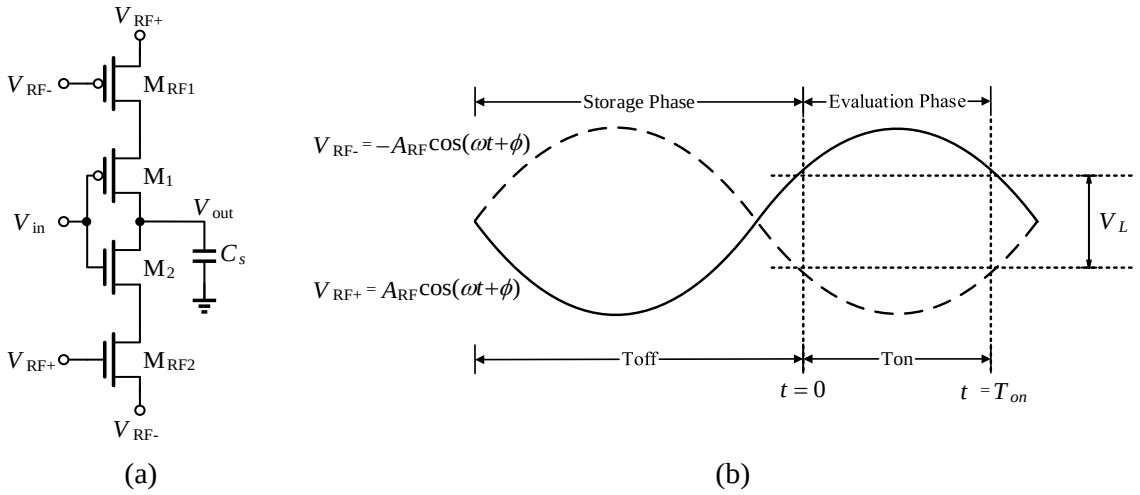


Figure 2.2 (a) Schematic of an RF-only inverter (b) Differential supply signals with operating regions indicated

During the evaluation phase, M_{RF1} and M_{RF2} are both subject to $V_{gs} > V_L$ allowing them to supply current to the logic circuit while the transistor channels are in weak or strong inversion. The storage phase establishes when $V_{RF+} - V_{RF-} > V_L$. During the storage phase, the channels of power supply transistors are brought to accumulation by the RF supply signals. Therefore, the logic circuit retains the output voltage level on the output capacitance while the power supply transistors block leakage current from C_s. The length of evaluation phase T_{on} is defined as:

$$T_{on} = \frac{\arccos \frac{V_L}{2A_{RF}}}{\pi f_{RF}} \tag{2.2}$$

where f_{RF} and A_{RF} are the frequency and amplitude of the RF signal, respectively. The RF supply signals V_{RF+} and V_{RF-} are defined as

$$V_{RF+} = A_{RF}\cos(\omega t+\phi) \tag{2.3}$$

$$V_{RF-} = -A_{RF}\cos(\omega t+\phi) \tag{2.4}$$

where

$$V_{RF+}(0) = V_{RF+}(T_{on}) = \frac{V_L}{2} \tag{2.5}$$

Operations of the RF-only inverter in both steady-state and logic transitions are analyzed in the following section using first order RC model.

2.2.1 Steady-State Analysis

We start with the analysis of steady-state operation when no logic transition takes place. Figure 2.3 shows the operation of an RF-only inverter with a logic “0” applied to the input. The simulated waveform of output voltage is plotted in Figure 2.4.

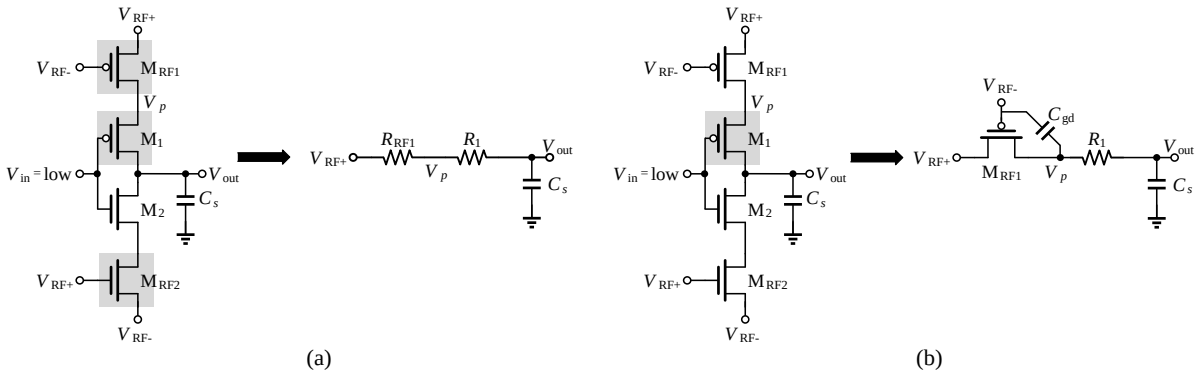


Figure 2.3 (a) Equivalent circuit of the RF-only inverter in the evaluation phase when $V_{in} = V_{OL}$ (b) Equivalent circuit of the RF-only inverter in the storage phase when $V_{in} = V_{OL}$

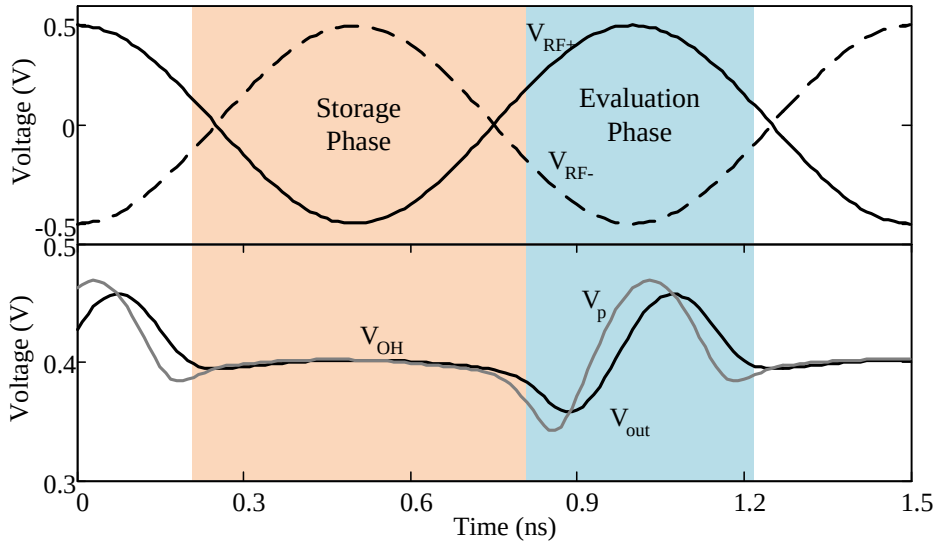


Figure 2.4 Simulated waveforms of the RF-only inverter in the steady-state when $V_{in} = V_{OL}$. V_{OH} is defined as the output voltage during the storage phase

During the storage phase, the two power supply transistors M_{RF1} and M_{RF2} are turned off. The charges are held on the output capacitance C_s to retain the logic level. The

equivalent circuit of the inverter in the storage phase is shown in Figure 2.3(b). The negative RF signal V_{RF-} is fed through to the output node via capacitive coupling effect of C_{gd}. Its impact on the output voltage is trivial since C_s is orders of magnitude larger than C_{gd}. To simplify the analysis, we assume the output voltage stays constant during the storage phase. The simulated output voltage in the storage phase verifies this assumption as shown in Figure 2.4. We further define the high and low output levels V_{OH}, V_{OL} as the corresponding output voltages during the storage phase. We assume the transistors are sized to achieve a balanced driving strength for pull up and pull down networks so that $V_{OH} = -V_{OL}$.

During the evaluation phase, M_{RF1} and M_1 are turned on and can be modeled as average "on" resistors R_{RF1} and R_1. The equivalent circuit is shown in Figure 2.3(a). It is equivalent to a track-and-hold circuit. The output voltage V_{out} tracks the RF supply signal V_{RF+} with a phase delay defined by the time constant $\tau = (R_1 + R_{RF1})C_s$. Applying phasor analysis on the equivalent circuit and considering the initial condition of $V_{out}(0) = V_{OH}$, the output voltage V_{out} as a function of time can be derived as

$$V_{out} = (V_{OH} - \frac{A_{RF}}{\sqrt{1+\omega^2\tau^2}}\cos(\phi + \theta))e^{-\frac{t}{\tau}} + \frac{A_{RF}}{\sqrt{1+\omega^2\tau^2}}\cos(\omega t + \phi + \theta) \qquad (2.6)$$

where phase delay $\theta = -\arctan(\omega\tau)$. Since the "on" resistances of M_{RF1} and M_1 vary with the RF amplitude, θ also changes with the RF amplitude. Equation (2.6) indicates that the steady-state transient response of the output voltage consists of two parts: a decaying initial response

defined by the initial condition, and a magnitude-attenuated and phase-shifted version of the RF signal V_{RF+}. At the end of the evaluation phase, V_{out} settles to V_{OH}, yielding

$$V_{OH} = \frac{A_{RF}}{\sqrt{1+\omega^2\tau^2}(1-e^{-\frac{T_{on}}{\tau}})}(\cos(\omega T_{on} + \phi + \theta) - e^{-\frac{T_{on}}{\tau}}\cos(\phi + \theta)) \quad (2.7)$$

Equation (2.7) unveils the DC output voltage level that can be achieved with the single-phase RF-only logic circuits. To capture more trackable expressions of V_{out} and V_{OH}, let's consider two typical operating scenarios defined by the RF cycle time and the time constant τ. Note that the RF-only logic operates in the large signal domain in which the transistors exhibit considerable non-linearity; therefore, the first order analysis conducted in this section is intended to gain design insights rather than to derive accurate models.

- $T_{RF} \gg \tau$ (high RF amplitude and low RF frequency), the decaying initial transient response can be ignored and the phase shift $\theta \approx$ -arctan (0) = 0. It leads to the simplified output voltage V_{out} and V_{OH} as

$$V_{out} = A_{RF}\cos(\omega t + \phi) \quad (2.8)$$

$$V_{OH} = A_{RF}\cos(\omega T_{on} + \phi) = V_{RF+}(T_{on}) = \frac{V_L}{2} \quad (2.9)$$

  The output voltage tracks the RF source with zero phase shift and amplitude attenuation. The output logic level V_{OH} reaches its minimum of half the turn-on

voltage V_L. The output node exhibits large voltage ripples during the evaluation phase, which leads to excessive static power consumption and reduced noise margin.

- $T_{RF} \ll \tau$ (low RF amplitude and high RF frequency), the phase shift θ approaches $\pi/2$. Under these conditions, we have

$$e^{-\frac{t}{\tau}} \approx 1 - t/\tau \tag{2.10}$$

$$\sqrt{1+\omega^2\tau^2} \approx \omega\tau \tag{2.11}$$

The output voltage V_{out} and V_{OH} can be simplified as

$$V_{out} = (V_{OH} - \frac{A_{RF}}{\omega\tau}\sin(\phi))(1 - \frac{t}{\tau}) + \frac{A_{RF}}{\omega\tau}\sin(\omega t + \phi) \tag{2.12}$$

$$V_{OH} = \frac{2A_{RF}}{\omega T_{on}}\sin(\omega T_{on} + \phi) = \frac{A_{RF}}{\arccos\frac{V_L}{2A_{RF}}}\sin(\omega T_{on} + \phi) = A_{RF}\frac{\sin(\alpha)}{\alpha} \tag{2.13}$$

where α is the evaluation angle defined as $\alpha = \omega T_{on} + \phi = \arccos\frac{V_L}{2A_{RF}}$. The steady-state logic level V_{OH} is almost equal to A_{RF}; therefore, the voltage ripple during evaluation phase is minimized.

A simulation of output logic level V_{OH} as a function of both the RF amplitude and frequency was also conducted to explore the operating region in between these two scenarios we discussed. The results are plotted in Figure 2.5. Figure 2.6 shows the same results with

V_{OH} normalized to the RF amplitude A_{RF}. For a constant RF frequency, V_{OH} is linearly proportional to RF amplitude A_{RF}. As RF frequency increases, this proportional coefficient increases as well. For a constant RF amplitude, the V_{OH} gets closer to A_{RF} as RF frequency increases.

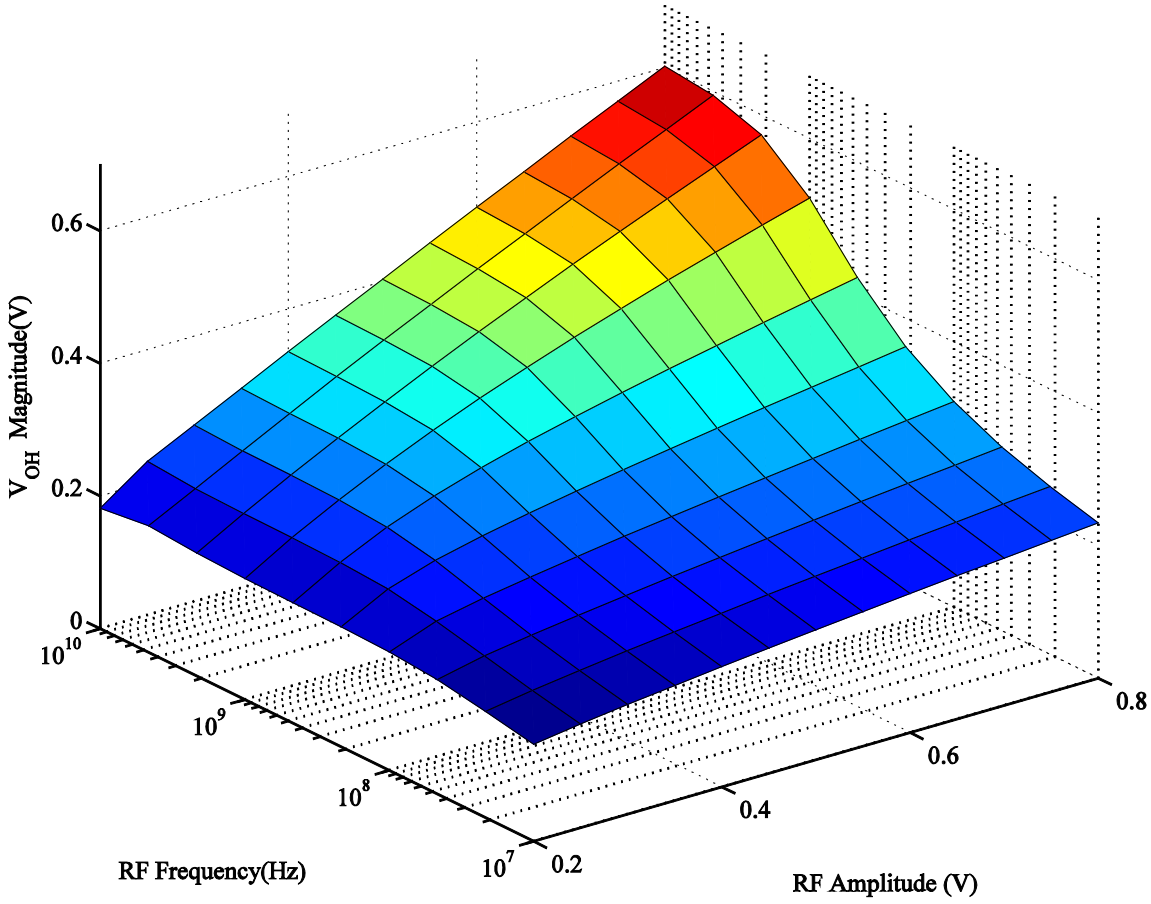


Figure 2.5 Output logic high V_{OH} as a function of RF amplitude and frequency

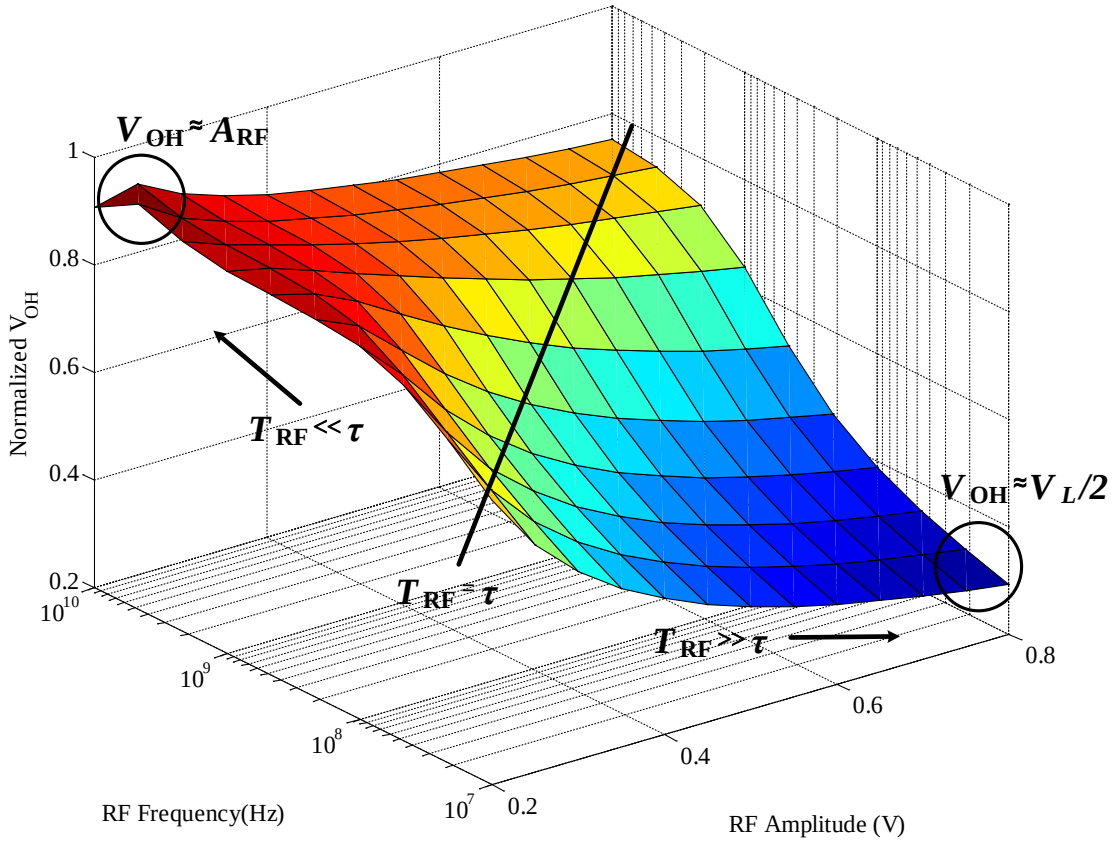


Figure 2.6 The output logic high V_{OH} as a function of RF amplitude and frequency, normalized to RF amplitude A_{RF}

2.2.2 Dynamic Operation Analysis

Dynamic operation analysis addresses the operation characteristics in the present of logic transitions. The following discussion proceeds under the assumption that the input signal to the inverter abruptly changes from V_{OH} to V_{OL} at the beginning of the evaluation phase. The dynamic operation of an RF-only inverter features different behavior in the two operating scenarios as we defined in the steady-state analysis.

- $T_{RF} \gg \tau$: a logic transition can complete within one RF cycle, and the output capacitance C_s is charged up directly by the supply current through the equivalent resistors R_{RF1} and R_1. A simulated waveform of an inverter working under this scenario is shown in Figure 2.7 to illustrate the logic transition. The output voltage V_{out} can be derived in the same approach as we did in the steady-state analysis, only with a different initial condition $V_{out}(0) = V_{OL}$,

$$V_{out} = (V_{OL} - \frac{A_{RF}}{\sqrt{1+\omega^2\tau^2}}\cos(\phi+\theta))e^{-\frac{t}{\tau}} + \frac{A_{RF}}{\sqrt{1+\omega^2\tau^2}}\cos(\omega t+\phi+\theta) \qquad (2.14)$$

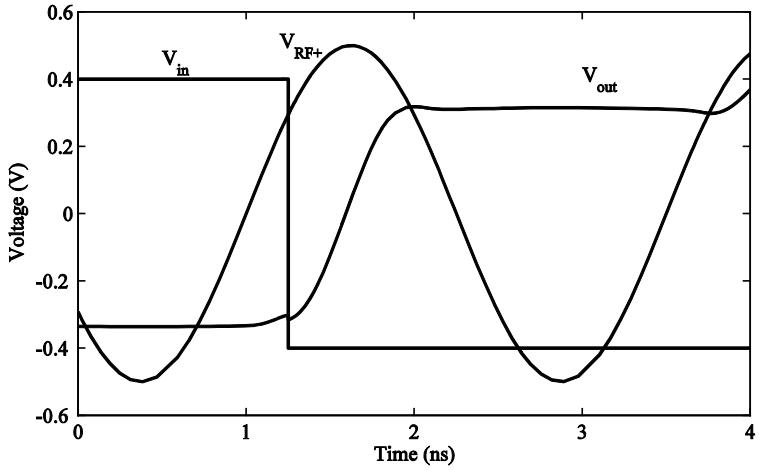


Figure 2.7 Simulated transient response of a logic transition for an RF-only inverter operating at $T_{RF} \gg \tau$

- $T_{RF} \ll \tau$: a logic transition takes multiple consecutive RF cycles to finish as shown in Figure 2.8. In the evaluation phases, the output capacitance C_s is charged directly by the supply current through the equivalent resistors R_{RF1} and R_1. In the storage phases, the charges on C_s are retained. For each evaluation phase during the logic transition, the output voltage can be derived as

$$V_{out(i)} = (V_{i-1} - \frac{A_{RF}}{\sqrt{1+\omega^2\tau^2}}\cos(\phi+\theta))e^{-\frac{t}{\tau}} + \frac{A_{RF}}{\sqrt{1+\omega^2\tau^2}}\cos(\omega t+\phi+\theta) \qquad (2.15)$$

with $V_{out(i)}$ the output voltage in the i-th RF cycle, V_{i-1} the initial output voltage in the i-th RF cycle, respectively.

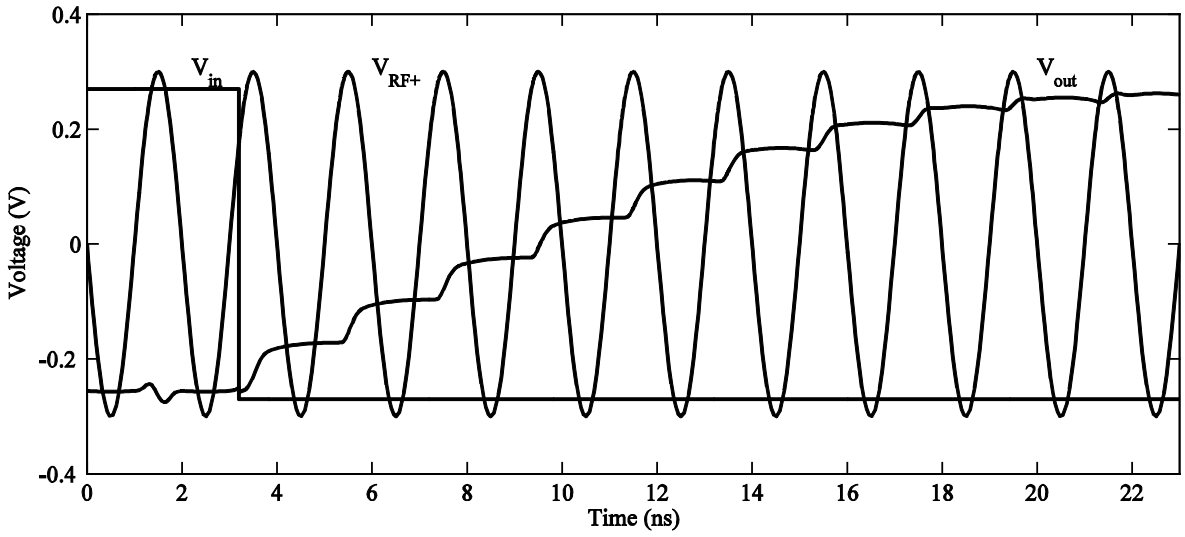


Figure 2.8 Simulated transient response of a logic transition for an RF-only inverter at $T_{RF} \ll \tau$

For the following analysis of propagation delay and power consumption, we derive tractable equations for parameters of interest based on the equivalent RC circuits. Simulations help to determine these characteristics in the transition region between these two scenarios we discussed.

2.3 Propagation Delay

The propagation delay of an inverter is defined as the time it takes for the output voltage to reach half of full swing. The following analysis proceeds under the assumption that the input signal to the inverter abruptly changes from V_{OH} to V_{OL} or vice versa. We further

assume that the input transition happens exactly at the beginning of the evaluation phase and the load capacitance C_s is constant during the logic transition. The leakage current and capacitive coupling effect on load capacitance C_s are also ignored. Figure 2.9 shows the equivalent circuit of an RF-only inverter during a high-to-low logic transition. Transistors M_{RF1} and M_1 are modeled as average "on" resistors in series, through which the load capacitance C_s is charged up. The load capacitance analysis of RF-only logic is identical to the classic CMOS circuit [14].

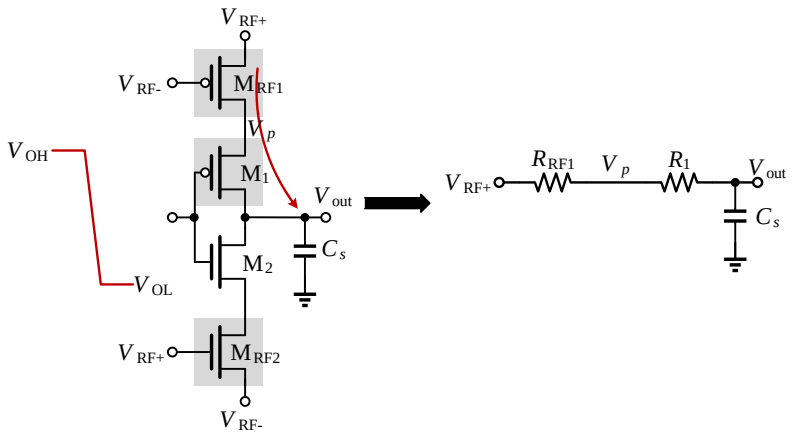


Figure 2.9 Equivalent circuit of a single-phase RF-only inverter during a high-to-low logic transition

2.3.1 $T_{RF} >> \tau$: Single-RF-Cycle Transition

As derived in the dynamic operation analysis, the output voltage as a function of time is shown in Equation (2.14), and repeated here

$$V_{out} = (V_{OL} - \frac{A_{RF}}{\sqrt{1+\omega^2\tau^2}}\cos(\phi+\theta))e^{-\frac{t}{\tau}} + \frac{A_{RF}}{\sqrt{1+\omega^2\tau^2}}\cos(\omega t+\phi+\theta) \quad (2.16)$$

Given the propagation delay T_p is defined as

$$V_{out}(T_p) = 0 \quad (2.17)$$

Substitute Equation (2.17) into Equation (2.16), and solve for T_p, we can obtain

$$T_p = \tau \ln\frac{V_{OH}+V_0}{V_p} \approx \tau\ln 2 \quad (2.18)$$

where

$$V_{OH} = A_{RF}\cos(\omega T_{on}+\phi) \quad (2.19)$$

$$V_0 = \frac{A_{RF}}{\sqrt{1+\omega^2\tau^2}}\cos(\phi+\theta) \quad (2.20)$$

$$V_p = \frac{A_{RF}}{\sqrt{1+\omega^2\tau^2}}\cos(\omega T_p+\phi+\theta) \quad (2.21)$$

The first order approximation of single-RF-cycle transition delay, given by Equation (2.18), is identical to the conventional CMOS gates. Equation (2.18) indicates that one can speed up RF-only logic by increasing the RF amplitude A_{RF} or increasing the W/L ratio of the transistors (before intrinsic capacitance dominates). Since τ is inversely proportional to A_{RF} to first order, the propagation delay T_p is linearly proportional to the RF amplitude in the single-RF-cycle logic transitions.

2.3.2 $T_{RF} \ll \tau$: Multiple-RF-Cycle Transition

During a multiple-RF-cycle logic transition, the output capacitance is charged in evaluation phase and retains the charges in the storage phase. A logic transition finishes within multiple consecutive evaluation phases. Assuming the output voltage takes n RF cycles to reach half of the peak-to-peak value, the overall propagation delay can be expressed as

$$T_p = (n\text{-}1)T_{RF} + T_n \tag{2.22}$$

where T_n is the transition time of the last RF cycle. We derive the output voltage in the last RF cycle in the same way as Equation (2.16), yielding

$$V_{out(n)} = \left(V_{n\text{-}1} - \frac{A_{RF}}{\sqrt{1+\omega^2\tau^2}}\cos(\phi+\theta)\right)e^{-\frac{t}{\tau}} + \frac{A_{RF}}{\sqrt{1+\omega^2\tau^2}}\cos(\omega t+\phi+\theta) \tag{2.23}$$

with $V_{out(n)}$ the output voltage in the n-th RF cycle, $V_{n\text{-}1}$ the initial output voltage in the n-th RF cycle, respectively. To solve for T_p, the cycle count n and transition time T_n must be solved first. To simplify the solution, we assume that $T_n = T_{on}$. According to the propagation delay definition, we have

$$V_{out(n)}(T_{on}) = 0 \tag{2.24}$$

At the end of the i-th RF cycle, we have

$$V_i = (V_{i-1} - \frac{A_{RF}}{\sqrt{1+\omega^2\tau^2}}\cos(\phi+\theta))e^{-\frac{T_{on}}{\tau}} + \frac{A_{RF}}{\sqrt{1+\omega^2\tau^2}}\cos(\omega T_{on}+\phi+\theta) \quad (2.25)$$

Also, in the first RF cycle, we have

$$V_1 = (V_{OL} - \frac{A_{RF}}{\sqrt{1+\omega^2\tau^2}}\cos(\phi+\theta))e^{-\frac{T_{on}}{\tau}} + \frac{A_{RF}}{\sqrt{1+\omega^2\tau^2}}\cos(\omega T_{on}+\phi+\theta) \quad (2.26)$$

There are n unknowns, being $V_1 \ldots V_i \ldots V_n$, and n equations as in the same pattern of Equation (2.25) for each unknown. Solving these n equations for V_n, and substituting Equation (2.26) into the results, we can derive

$$V_n = V_1 + (V_1 + V_{OH})\frac{e^{-\frac{T_{on}}{\tau}}}{1-e^{-\frac{T_{on}}{\tau}}}(1-(e^{-\frac{T_{on}}{\tau}})^{n-1}) = 0 \quad (2.27)$$

Given that $T_{RF} \ll (R_{RF1}+R_1)C_s$ holds for the multiple-RF-cycle transition scenario, Equation (2.26) hence can be simplified and re-arranged as

$$V_1 = V_{OL}(1 - \frac{2T_{on}}{\tau}) \quad (2.28)$$

Substitute Equation (2.28) into Equation (2.27), and solve for RF cycle count n as

$$n = [\log_{(\frac{\tau - T_{on}}{\tau})} 0.5\ ] + 1 \tag{2.29}$$

We define the effective evaluation time as

$$T_{eff} = \frac{T_{on}}{\tau} = \frac{\arccos \frac{V_L}{2A_{RF}}}{\pi f_{RF} \tau} \tag{2.30}$$

Finally substitute Equation (2.30) into Equation (2.29), we can obtain the expression for multiple-RF-cycle propagation delay

$$T_p = \frac{-0.7}{\ln(1-T_{eff})} T_{RF} + T_{on} \tag{2.31}$$

Since the effective evaluation time T_{eff} is linearly proportional to the RF amplitude A_{RF} from Equation (2.30), the propagation delay T_p is reversely proportional to $\ln(1-A_{RF})$ from Equation (2.31).

2.3.3 Simulation Results

To evaluate how propagation delay varies with the design parameters across the entire operating range, such as RF amplitude and frequency, SPICE simulation of a ring oscillator consisting of 61 stages minimum sized RF-only inverter implemented in 0.13μm CMOS technology was conducted and the results are presented. The ring oscillator was chosen instead of a single inverter to minimize the delay variation due to the phase relation, which

we will discuss in next section. The same ring oscillator consists of classic CMOS inverters was also simulated for comparison. The default simulation settings are listed in Table 2.1.

Table 2.1 Default parameters for propagation delay simulations

Inverter Size	400nm/160nm
PST size	400nm/160nm
RF amplitude	500mV
RF frequency	1GHz
Data rate	1Mbps
Load	10fF
Transition time	1ps

Figure 2.10 shows the simulated oscillation periods in logarithmic scale as a function of the RF amplitude for both designs. The supply voltages were set to the same root-mean-square (rms) values for fair comparison. Two observations can be drawn from the results:

- The propagation delay of RF-only logic versus supply level features the same trend as the classic CMOS as we discussed in the first-order analysis. The delay is relatively insensitive to supply variations for high power level. However, it decreases in logarithmic relation with the power supply when the power level decreases below 0.4V as the transistors operate in the sub-threshold region.
- For the same rms voltage level, the RF-only logic based ring oscillator runs slower in the super-threshold region and faster in the sub-threshold region compared to its CMOS counterpart. This is a mixed result of supply level sensitivity and delay

penalty due to storage phase. For the same rms voltage level, the peak-to-peak overdrive voltage across RF-only transistors is higher than classic CMOS gate transistors which are powered by a DC supply. In the super-threshold region where the delay is insensitive to power supply variation, the delay penalty due to storage phase dominates. Therefore, RF-only logic based ring oscillator runs slower. Whereas in the sub-threshold region, the propagation delay has an exponential relation with the power level, thus the RF-only logic based ring oscillator powered by a higher overdrive voltage runs faster.

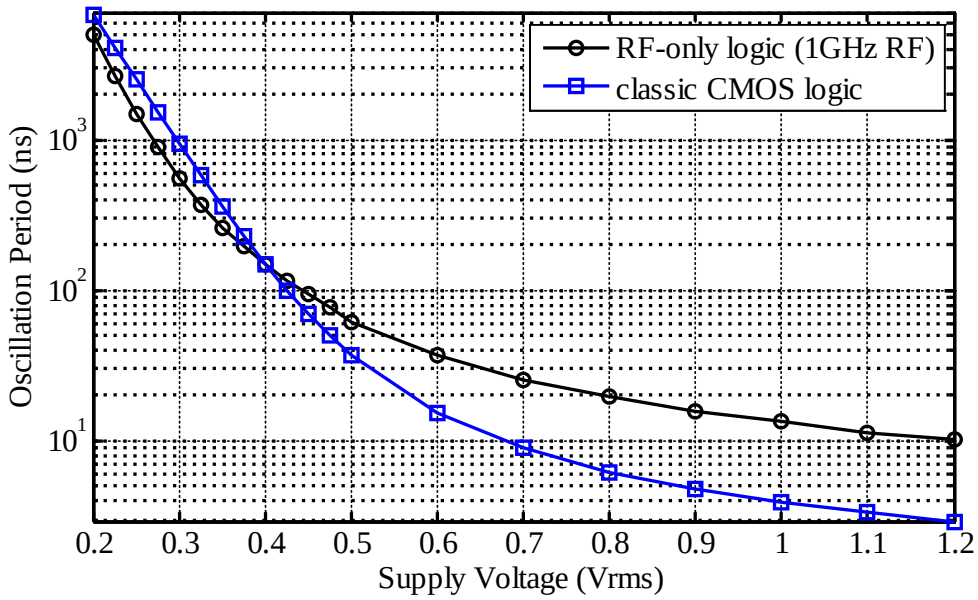


Figure 2.10 Oscillation periods of ring oscillator based on RF-only logic and classic CMOS logic as a function of RF amplitude

The impact of RF frequency on propagation delay is explored by simulating the ring oscillator under different RF frequencies. The results are plotted in Figure 2.11. Overall, the gate delay is insensitive to RF frequency and slightly decreases as the frequency increases. However, some non-monotonic data points observed due to the delay penalty caused by the phase relation of RF signal and input transition. As RF frequency increases, additional storage phases may be added to the transitions which lead to a longer delay.

In summary, the propagation delay of RF-only logic is a strong function of the RF amplitude and weakly impacted by the RF frequency.

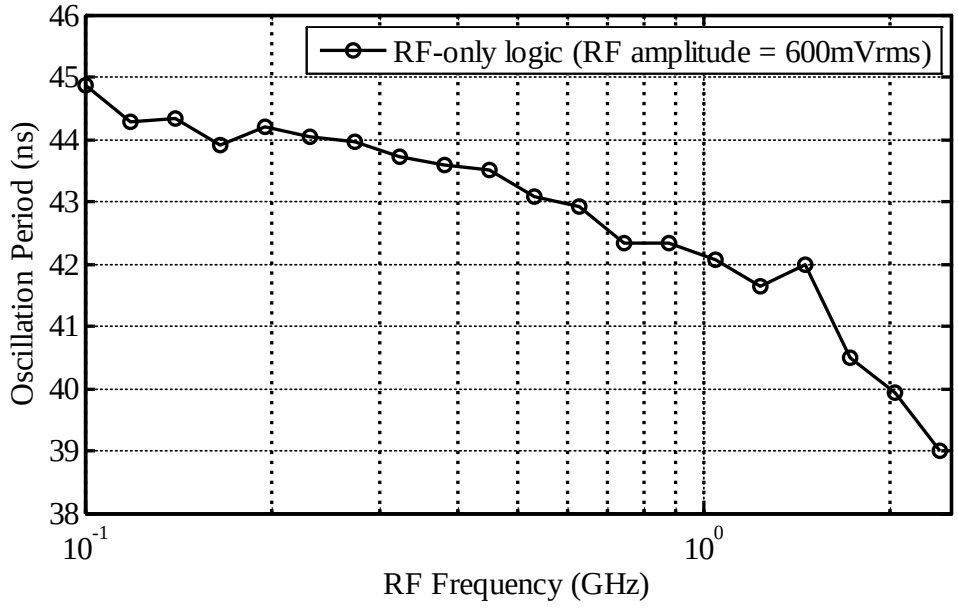


Figure 2.11 Oscillation periods of RF-only logic based ring oscillator as a function of RF frequency

2.3.4 Other Parameters

We assumed the input logic transition happened exactly at the beginning of the evaluation phase to simplify the analysis. However, the logic transitions can occur at any time during the evaluation phase. The propagation delay is not constant and varies with the phase relationship between the input transition and the RF supply. Simulation of propagation delay of an RF-only inverter versus transition phase shows a delay penalty for the transitions happening close the end of evaluation phase. The simulation results are plotted in Figure 2.12 with the delay penalty annotated. Note the penalty usually equals the length of storage phase. This effect is reduced for logic path consisting of multiple gates. However, enough timing margin needs to be added to compensate for the delay penalty in logic design and synthesis.

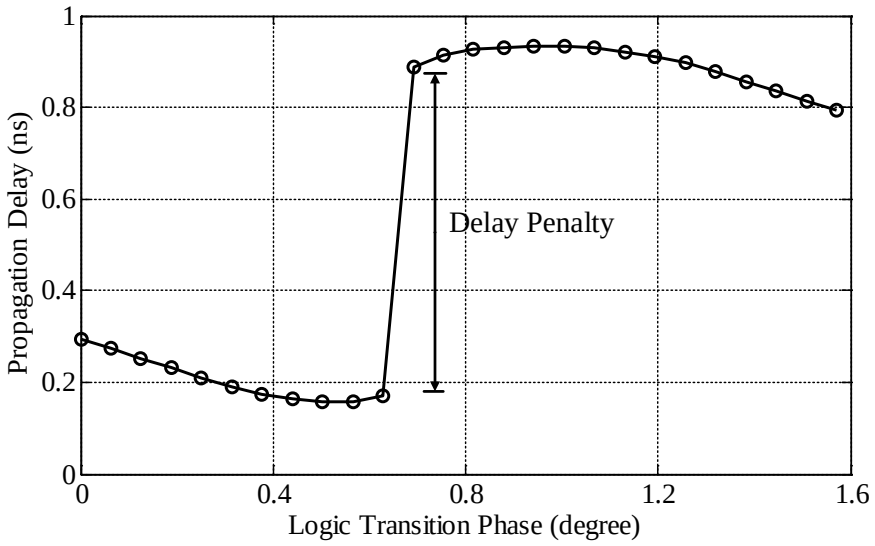


Figure 2.12 Simulated propagation delay of an RF-only inverter as a function of the logic transition phase. Zero phase indicates the input transition happens right at the beginning of evaluation phase.

The propagation delay of the RF-only inverter is simulated as a function of the core logic sizing and the results are plotted in Figure 2.13. It indicates an optimal W/L ratio which minimizes the propagation delay. Further increasing the W/L ratio beyond the optimal point leads to the intrinsic capacitance dominating output capacitance and a longer delay.

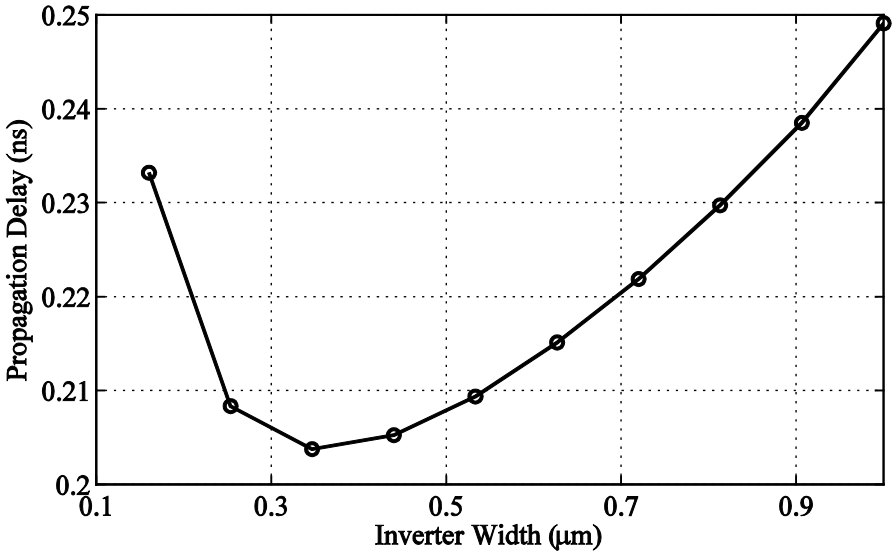


Figure 2.13 Simulated propagation delay of the RF-only inverter as a function of the core logic sizing

The propagation delay of the RF-only inverter is simulated as a function of power supply transistor sizing, and the results are plotted in Figure 2.14. Increasing PST width reduces the propagation delay with a diminishing return, due to the effective "on" resistance R_1 dominating the overall resistance (R_1+R_{RF1}).

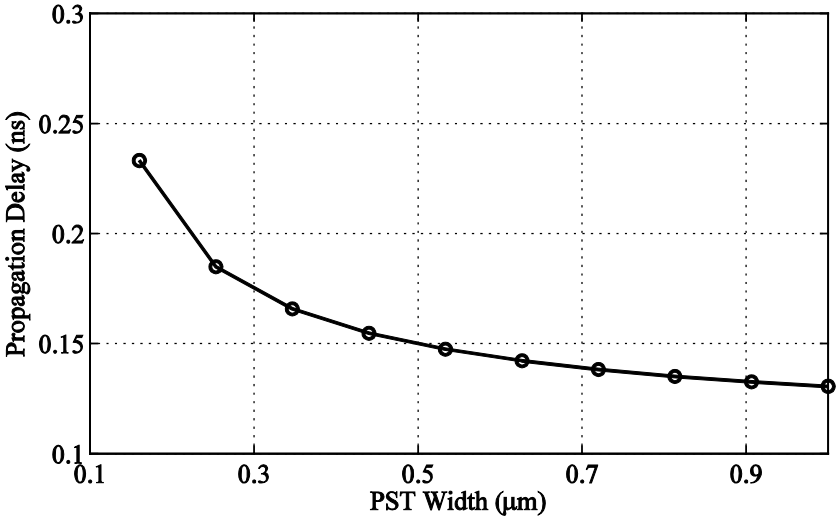


Figure 2.14 Simulated propagation delay of RF-only inverter as a function of power supply transistor sizing

2.4 Power Consumption

The power consumption of a CMOS circuit consists of dynamic and static consumption [14]. Dynamic power consumption results from the charging and discharging of capacitances while input switches and static power consumption is defined as the power dissipated in the absence of switching activity. The power consumption of RF-only logic circuits consists of the following four parts:

- Dynamic power dissipation of charging output capacitance
- Dynamic power dissipation of direct-path current
- Static power consumption of RF feedthrough in evaluation phase

- Static power consumption of capacitive coupling

Compared to conventional CMOS circuit, the RF-only logic circuits dissipate more static power due to the RF feedthrough to the output nodes during the evaluation phase. While the dynamic power consumption is not a function of (T_{RF}/τ), static power consumption reduces as (T_{RF}/τ) decreases. This is analyzed in detail in the following section.

2.4.1 Dynamic Power: Charging Output Capacitance

Schematic of a single phase RF-only logic inverter is shown in Figure 2.15. Upon a high-to-low input switch, the output capacitance C_s gets charged to V_{OH} or V_{OL}. The energy drawn from the power supply is dissipated on the transistors along the charging path; whereas the energy stored on C_s keeps constant. The following analysis of dynamic power consumption is conducted in the two scenarios same as the propagation delay analysis.

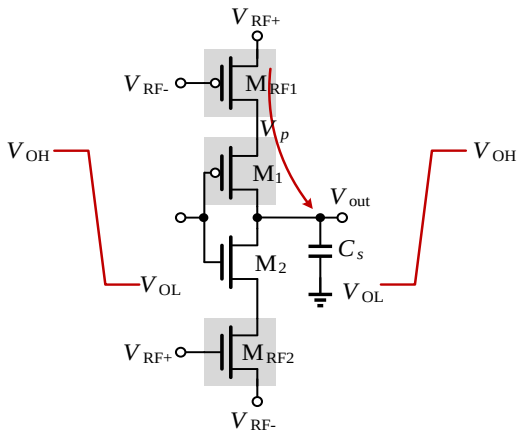


Figure 2.15 An RF-only inverter during the low-to-high transition, with charging current flow annotated

a. $T_{RF} >> \tau$

A precise measurement for the energy consumption can be derived. Let's first consider the low-to-high logic transition. We assume, initially, that the input waveform has zero rising and falling time. The energy taken from the supply V_{RF+} during one transition can be derived by integrating the instantaneous power over the period of interest:

$$E_{RF} = \int_0^{\infty} V_{RF+} i_{RF}(t)\ \mathrm{d}t = \int_0^{\infty} A_{RF}\cos(\omega t + \phi) C_s \frac{\mathrm{d}V_{out}}{\mathrm{d}t}\mathrm{d}t = \int_{V_{OL}}^{V_{OH}} A_{RF}\cos(\omega t + \phi) C_s \mathrm{d}V_{out} \qquad (2.32)$$

To derive a tractable equation for the dissipated energy, we first calculate half of the energy drawn. It is the energy dissipated up to V_{out} reaching half output swing:

$$\frac{E_{RF}}{2} = \int_0^{T_p} V_{RF+} i_{RF}(t)\ \mathrm{d}t = \int_{V_{OL}}^{0} A_{RF}\cos(\omega t + \phi) C_s\ \mathrm{d}V_{out} \qquad (2.33)$$

As mentioned in the delay analysis, the output voltage of single-RF-cycle transition in Equation (2.16) can be simplified under the condition of $T_{RF} \gg \tau$ as

$$V_{out} = (\ V_{OL} - A_{RF}\cos(\phi)\ ) e^{-\frac{t}{\tau}} + A_{RF}\cos(\omega t + \phi) \qquad (2.34)$$

For convenience, we repeat prior equations here, written as

$$V_{RF+}(0) = A_{RF}\cos(\phi) = \frac{V_L}{2} \tag{2.35}$$

$$V_{out}(T_p) = 0 \tag{2.36}$$

$$V_{OH} = \frac{V_L}{2} \tag{2.37}$$

Substitute Equations (2.34)(2.35)(2.36)(2.37) into Equation (2.33), and solve for energy dissipation

$$E_{RF} = C_s V_{OH}^2 \left(5 - 12e^{-\frac{2T_p}{\tau}}\right) \tag{2.38}$$

Substituting the expression of propagation delay T_p from Equation (2.18) into Equation (2.38), we can derive a more straightforward equation for energy consumption similar to the conventional CMOS circuits as

$$E_{RF} \approx 2C_s V_{OH}^2 \tag{2.39}$$

We can also confirm that the energy drawn from the RF source and stored on output capacitor C_s at the end of transition is zero:

$$E_{C_s} = \int_0^{\infty} V_{out} i_{RF}(t)\, dt = \int_0^{\infty} V_{out} C_s \frac{dV_{out}}{dt} dt = C_s \int_{V_{OL}}^{V_{OH}} V_{out} dV_{out} = 0 \tag{2.40}$$

Notice that not like conventional CMOS circuits, no extra energy is stored on the output capacitance. All the energy drawn from the RF source is dissipated on the transistors along the charging path. These results can also be derived for a high-to-low logic transition. In summary, each logic transition takes a fixed amount of energy, equal to $2C_sV_{OH}^2$. Therefore, for one on-and-off transition, the dynamic energy dissipated is

$$E_{RF} = 4C_sV_{OH}^2 = C_s(2V_{OH})^2 \tag{2.41}$$

The dynamic energy consumed is equivalent to the dynamic energy dissipation of a conventional CMOS inverter with a power supply of $2V_{OH}$. If the gate is switched on and off f_s times per second, the dynamic power consumption is given by

$$P_{dyn} = 4C_sV_{OH}^2f_s = C_s(2V_{OH})^2f_s \tag{2.42}$$

b. $T_{RF} \ll \tau$

During a multiple-RF-cycle logic transition, the dynamic energy dissipated can be defined as

$$E_{RF} = \sum_{i=1}^{m} \int_{V_i}^{V_{i+1}} V_{RF+}C_s \, dV_{out} \tag{2.43}$$

where m is the number of RF cycles for the logic transition to finish, and V_i is the output voltage at the end of the i-th RF cycle. The energy dissipated during the (i+1)-th cycle is

$$E_{i+1} = \int_{V_i}^{V_{i+1}} V_{\mathrm{RF}+} C_s \, \mathrm{d}V_{\mathrm{out}(i+1)} \tag{2.44}$$

where the (i+1)-th output voltage can be rewritten under the condition of $T_{\mathrm{RF}} \ll \tau$ as

$$V_{\mathrm{out}(i+1)} = \left(V_i - \frac{A_{\mathrm{RF}}}{\omega\tau}\sin(\phi)\right)\left(1 - \frac{t}{\tau}\right) + \frac{A_{\mathrm{RF}}}{\omega\tau}\sin(\omega t + \phi) \tag{2.45}$$

Substitute Equation (2.25) and (2.45) into Equation (2.44) and we can obtain the energy consumed during the (i+1)-th RF cycle as

$$E_{i+1} = \frac{C_s T_{\mathrm{on}}}{4\tau}\left(2A_{\mathrm{RF}}^2 + V_L V_{\mathrm{OH}}\right) - \frac{T_{\mathrm{on}}^2 C_s}{2\tau^2} V_{\mathrm{OH}}^2 - \frac{C_s T_{\mathrm{on}}}{\tau} V_i V_{\mathrm{OH}} \tag{2.46}$$

Substitute Equation (2.46) back to Equation (2.43) and we can get

$$E_{\mathrm{RF}} = m\left(\frac{C_s T_{\mathrm{on}}}{4\tau}\left(2A_{\mathrm{RF}}^2 + V_L V_{\mathrm{OH}}\right) - \frac{T_{\mathrm{on}}^2 C_s}{2\tau^2} V_{\mathrm{OH}}^2\right) - \frac{C_s T_{\mathrm{on}}}{\tau} V_{\mathrm{OH}} \sum_{i=1}^{m} V_i \tag{2.47}$$

To solve E_{RF}, we need to substitute V_i with known values. Recall that for the (i+1)-th RF cycle, the output voltage is already derived and is repeated here

$$V_{i+1} = (V_i - \frac{A_{RF}}{\omega\tau}\sin(\phi))\,(1 - \frac{T_{on}}{\tau}) + \frac{A_{RF}}{\omega\tau}\sin(\omega T_{on} + \phi) \tag{2.48}$$

Substitute Equation (2.25) into Equation (2.48) and re-arrange it, we can obtain

$$\frac{T_{on}}{\tau}V_i = V_i - V_{i+1} + \frac{T_{on}}{\tau}(V_{OH} - \frac{T_{on}}{2\tau}) \tag{2.49}$$

Substitute Equation (2.49) into Equation (2.47) and re-arrange it, we can derive the dynamic energy dissipated during one multi-RF-cycle transition as

$$E_{RF} = 2C_sV_{OH}^2 + m\,(\frac{C_sT_{on}}{4\tau}\left(2A_{RF}^2 + V_LV_{OH} - 4V_{OH}^2\right)) \tag{2.50}$$

We show later in the next section that $m\,(\frac{C_sT_{on}}{4\tau}\left(2A_{RF}^2 + V_LV_{OH} - 4V_{OH}^2\right))$ is the static energy dissipated due to RF feedthrough in the evaluation phase. Therefore, the dynamic energy consumption due to logic transition is

$$E_{RF} = 2C_sV_{OH}^2 \tag{2.51}$$

This result is identical to the one we derived in the single-RF-cycle transition case. No extra energy is stored on the output capacitance, and all the energy drawn from RF source is dissipated during the logic transition. These results can also be derived during the high-to-low transitions. In summary, each logic transition takes a fixed amount of energy, equal to $2C_sV_{OH}^2$. If the gate is switched on and off f_s times per second, the power consumption is given by

$$P_{dyn} = 4C_sV_{OH}^2f_s = C_s(2V_{OH})^2f_s \tag{2.52}$$

The dynamic power consumption of a minimum sized RF-only inverter driven by a 1MHz clock signal is simulated, and is plotted versus supply voltage in Figure 2.16. The simulated dynamic power of a CMOS inverter with the same size is also plotted for comparison. Observe that the dynamic power of the two inverters features the same trend versus supply voltage. For the same rms supply voltage, V_{OH} is usually higher than the DC power supply voltage. Therefore, the RF-only inverter consumes more power than the CMOS inverter at the same supply voltage.

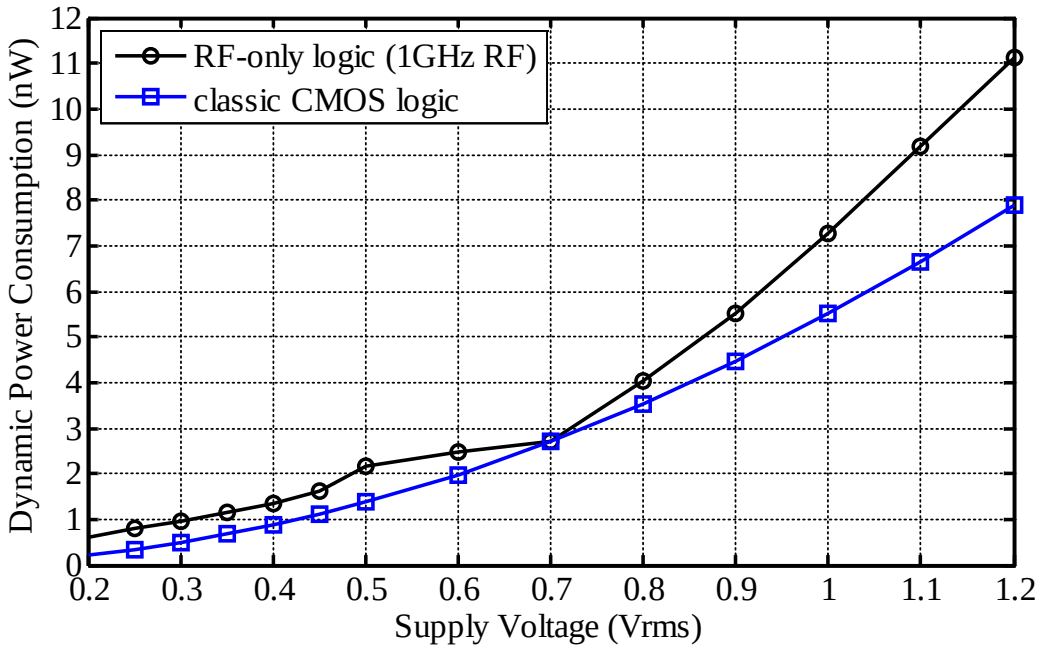


Figure 2.16 Dynamic power consumption of RF-only inverter and classic CMOS inverter as a function of supply level

Figure 2.17 shows RF frequency's impact on dynamic power consumption. V_{OH} increases as RF frequency increases, resulting in more dynamic power dissipated. At high RF frequency, the circuit operates in $T_{RF} \ll \tau$ region and V_{OH} close to A_{RF}, resulting in a flattened dynamic power consumption.

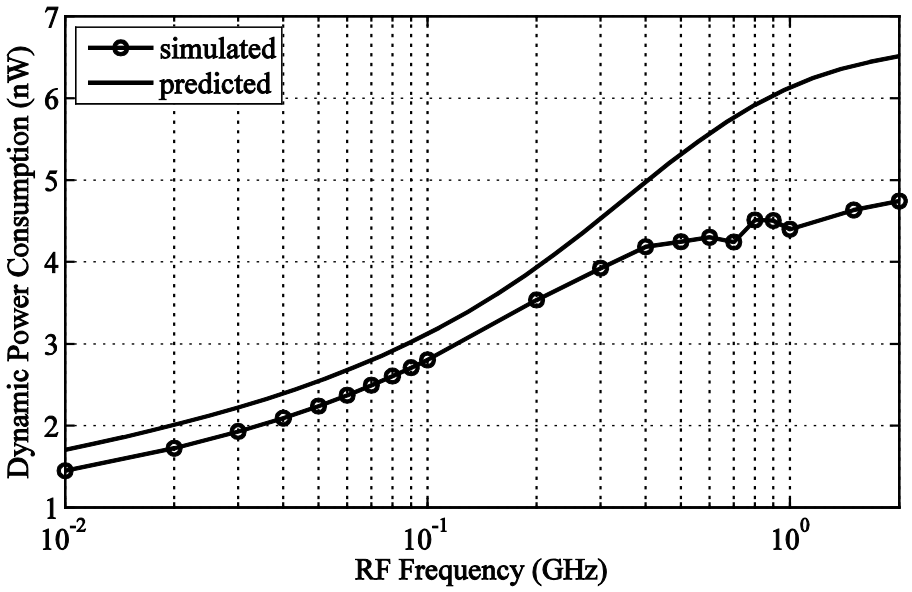


Figure 2.17 Dynamic power consumption of an RF-only inverter as a function of RF frequency f_{RF}, both simulated and predicted included.

2.4.2 Dynamic Power: Direct-Path Current

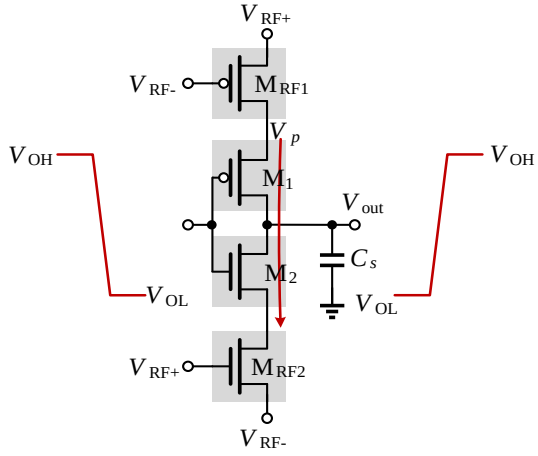


Figure 2.18 Direct-path current during logic transition

In reality, the input signal changes gradually, which results in a direct current path between the two power supplies for a short period during the logic transition. We follow the same derivation as shown in [14], the average power consumption due to direct-path current is

$$P_{\mathrm{dp}} = 2t_{\mathrm{sc}}A_{\mathrm{RF}}I_{\mathrm{peak}}f_s \tag{2.53}$$

where

$$t_{\mathrm{sc}} = \frac{2A_{\mathrm{RF}} - 2V_L}{2A_{\mathrm{RF}}}\frac{2T_p}{0.8} = 2.5T_p\frac{A_{\mathrm{RF}} - V_L}{2A_{\mathrm{RF}}} \tag{2.54}$$

I_{peak} is determined by the saturation current of the devices and is hence directly proportional to the size of the transistors [14].

2.4.3 Static Power: RF Feedthrough

Not like the conventional CMOS circuits, the RF-only logic circuits dissipate a significant amount of static power due to the persistent voltage ripples on the output nodes as discussed in Section 2.2.1. The voltage ripple is amplitude-attenuated, phase-delayed version of the RF signal during the evaluation phase.

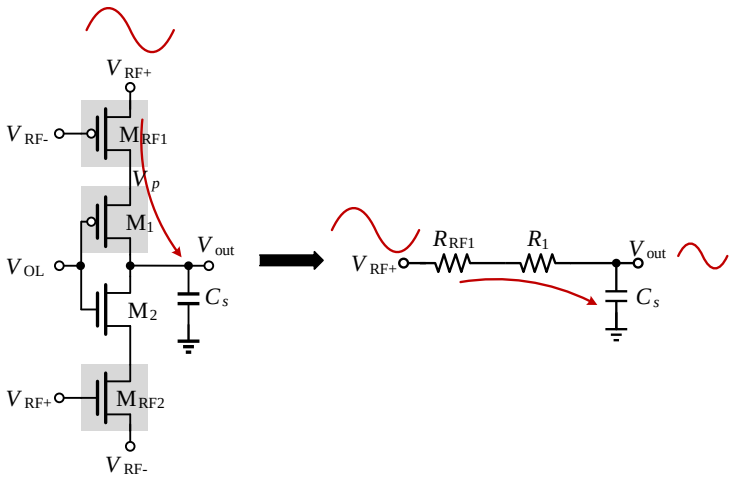


Figure 2.19 Equivalent circuit of the RF-only inverter in evaluation phase with the charging and discharging path labeled

Consider the case of an inverter with input set to logic low, and the equivalent circuit is pictured in Figure 2.19. The energy taken from the supply V_{RF+} during one RF cycle can be derived by integrating the instantaneous power over the evaluation period:

$$E_{TH} = \int_0^{T_{on}} V_{RF+} i_{RF}(t)\ \mathrm{d}t = \int_0^{T_{on}} A_{RF}\cos(\omega t + \phi) C_s \frac{\mathrm{d}V_{out}}{\mathrm{d}t}\ \mathrm{d}t \qquad (2.55)$$

In the scenario of $T_{RF} >> \tau$, the overall energy dissipated E_{TH} approaches zero since there is approximately no phase shift between the RF source and output voltage.

In the scenario of $T_{RF} \ll \tau$, the voltage on output node and steady-state output voltage were derived and is repeated here

$$V_{out} = (V_{OH} - \frac{A_{RF}}{\omega\tau}\sin(\phi))(1 - \frac{t}{\tau}) + \frac{A_{RF}}{\omega\tau}\sin(\omega t + \phi) \quad (2.56)$$

$$V_{OH} = \frac{2A_{RF}}{\omega T_{on}}\sin(\omega T_{on} + \phi) = A_{RF}\frac{\sin(\alpha)}{\alpha} \quad (2.57)$$

Substitute Equations (2.56) and (2.57) into Equation (2.55), the energy dissipated during steady-state evaluation phase can be expressed as

$$E_{TH} = \frac{C_s T_{on}}{4\tau}\left(2A_{RF}^2 + V_L V_{OH} - 4V_{OH}^2\right) = \frac{T_{on}}{4\tau}A_{RF}^2 C_s\,(1 + \frac{\sin\alpha\cos\alpha}{\alpha} - \frac{2\sin\alpha^2}{\alpha^2}) \quad (2.58)$$

The power dissipated can be obtained by multiplying E_{TH} with RF frequency f_{RF}

$$P_{th} = \frac{T_{on} f_{RF}}{4\tau}A_{RF}^2 C_s\,(1 + \frac{\sin\alpha\cos\alpha}{\alpha} - \frac{2\sin\alpha^2}{\alpha^2}) \quad (2.59)$$

Substitutes T_{on} in Equations (2.2) into Equation (2.59) and yield the following expression for P_{th}

$$P_{th} = \frac{K}{4(R_1 + R_{RF1})}A_{RF}^2 \quad (2.60)$$

where static power consumption coefficient K is defined as

$$K = \frac{\alpha}{\pi}\left(1 + \frac{\sin\alpha\cos\alpha}{\alpha} - \frac{2\sin\alpha^2}{\alpha^2}\right) \tag{2.61}$$

Note that Equation (2.60)(2.61) only valid under the condition of $T_{RF} \ll \tau$, where α is close to zero. Since effective on-resistance ($R_1 + R_{RF1}$) is inversely proportional to the RF amplitude, the static power consumption under this condition has a cubical relationship with RF amplitude as shown in Equation (2.60).

The effective "on" resistance ($R_1 + R_{RF1}$) is inversely proportional to the size of the transistors. Therefore, static power dissipation decreases with the transistor size. The simulated static power consumption as a function of transistor W/L ratio is shown in Figure 2.20. For the same PST sizing, static power increases linearly with core logic W/L ratio. Larger PST sizing also results in more static power dissipation.

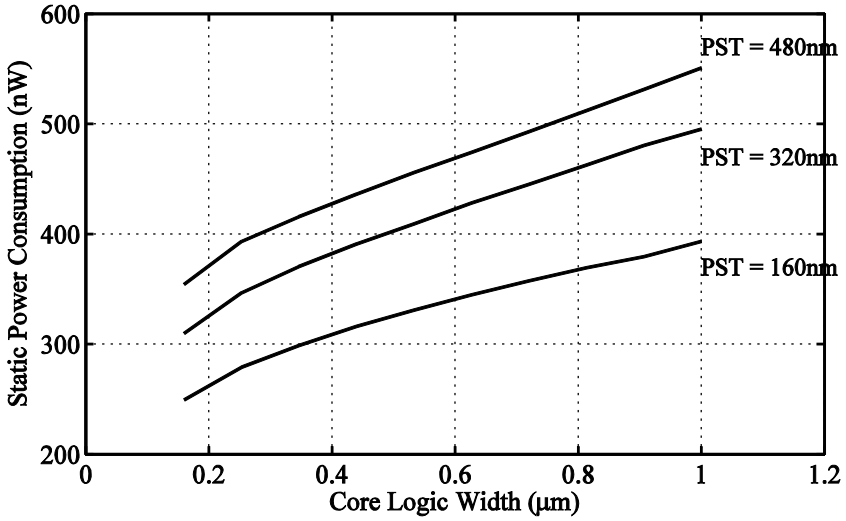


Figure 2.20 Simulated static power consumption as a function of transistor W/L ratio

As RF frequency increases, the operating region moves from $T_{RF} >> \tau$ to $T_{RF} \ll \tau$, thus the power dissipation increases. This relationship is also captured in the simulation and plotted in Figure 2.21. Power dissipation increases approximately linearly with RF frequency in the transition region. In $T_{RF} \ll \tau$ region, power consumption is simulated as a function of amplitude and plotted in Figure 2.22. As predicted from our first order analysis, the static power increases cubically with RF amplitude in this region.

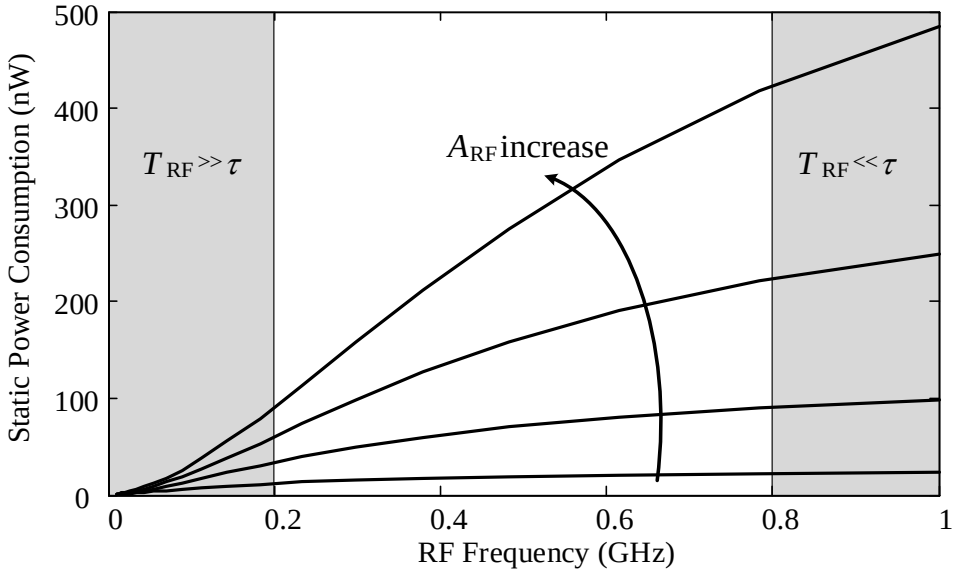


Figure 2.21 Simulated static power consumption of RF-only inverter as a function of RF frequency and amplitude

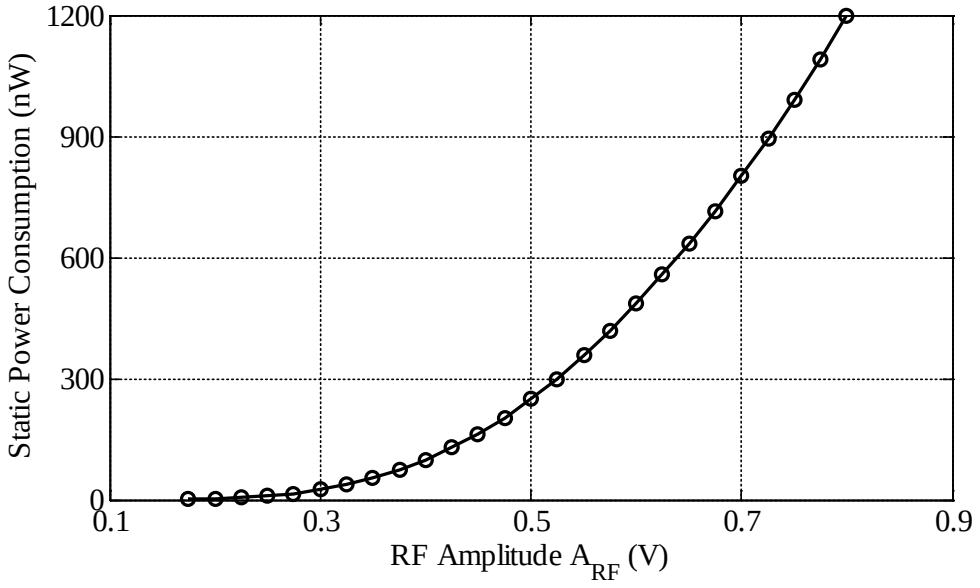


Figure 2.22 Simulated static power consumption of RF-only logic as a function of RF amplitude in $T_{RF} \ll \tau$ region

2.4.4 Static Power: Capacitive Coupling

The capacitive coupling effect, which causes RF supply signal feeding through to output node, exists during the entire RF cycle. However, due to its limited effect on the output node, it only dominates during the storage phase while power transistor M_{RF1} is off. Considering the case of an inverter with input set to logic low, the energy taken from the supply V_{RF-} during one RF cycle can be derived by integrating the instantaneous power over one RF period:

$$E_{CC} = \int_0^{T_{RF}} V_{RF+} i_{RF}(t)\ \mathrm{d}t = \int_0^{T_{RF}} A_{RF}\cos(\omega t + \phi) C_s \frac{\mathrm{d}V_{out}}{\mathrm{d}t}\ \mathrm{d}t \qquad (2.62)$$

In the scenario of $T_{RF} >> \tau$, the overall energy dissipated $E_{CC} = 0$ since there is no phase shift between RF source and output voltage. In the scenario of $T_{RF} \ll \tau$, the capacitive coupling power can be derived as

$$P_{cc} = \frac{\tau}{2} A_{RF}^2 C_s \tag{2.63}$$

Power consumption due to capacitive coupling is orders of magnitude lower than other power dissipation sources, and we can usually ignore its contribution.

2.4.5 Put It All Together

The total power consumption of the RF-only inverter is now expressed as the sum of its four components:

$$P_{tot} = P_{dyn} + P_{dp} + P_{th} + P_{cc} \tag{2.64}$$

The static power consumption components vary with different operating regions of the circuit as analyzed in preceding sections. The derived equations for all the power components and their trend over major design parameters are listed in Table 2.2.

Table 2.2 Summary of power consumption of RF-only logic

	$T_{RF} \gg \tau$	$T_{RF} \ll \tau$	A_{RF}	f_{RF}	W/L	f_s
P_{dyn}		$C_s(2V_{OH})^2 f_s$	O(n)	-	Optimal	O(n)
P_{dp}		$2t_{sc}A_{RF}I_{peak}f_s$	O(n^2)	-	-	O(n)
P_{th}	0	$\frac{K}{4(R_1 + R_{RF1})}A_{RF}^2$	O(n^3)	O(n)	O(n)	-
P_{cc}	0	$\frac{\tau}{2}A_{RF}^2 C_s$	O(n^3)	-	Optimal	-

The capacitive dynamic power dissipation and static consumption are the dominant factors. A family of contour curves that represent the operating points at which power dissipation due to these two components are equal are shown in Figure 2.23. For each curve, the area beneath is the dynamic-power-dominant area. For low power designs, it is better to set the operating point of the circuit in the dynamic power dominant region. Note that they are not constant power consumption contours. The curves extend up to A_{RF} = 500mV to ensure $f_{RF}/f_s > 10$ for robust operation, and the lower boundary stops at 100mV to prevent too large propagation delay to sustain the data rate.

In summary, RF-only logic consumes more power than conventional CMOS logic under same power level. This is the primary limitation of RF-only logic.

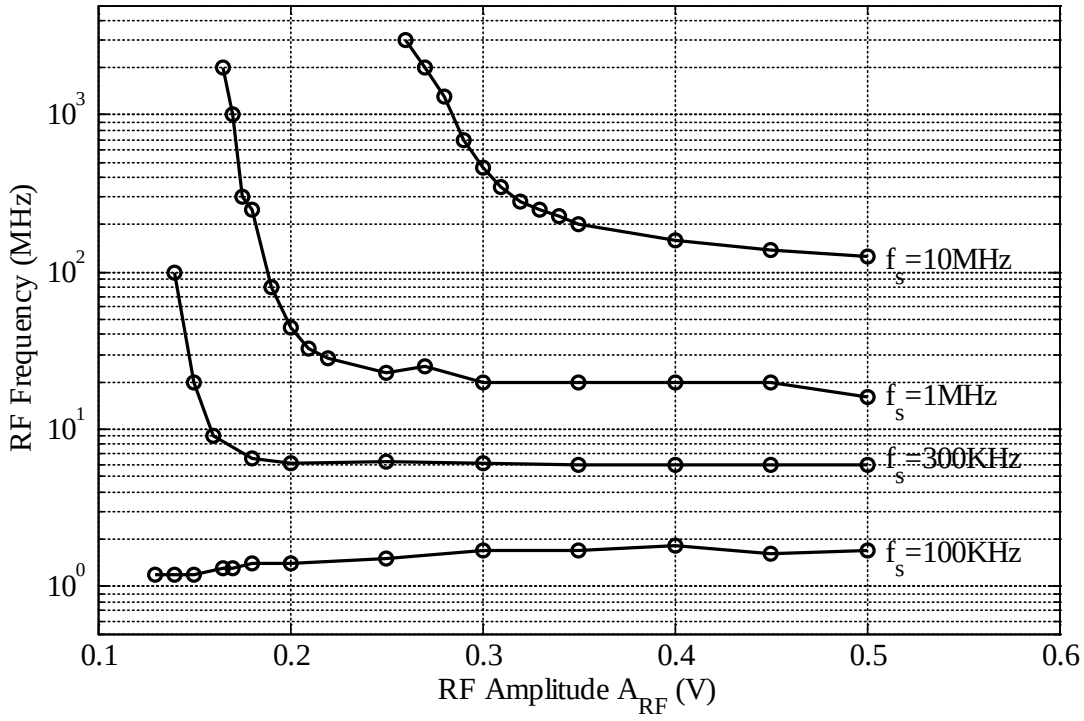


Figure 2.23 Contours of operating points at which the capacitive dynamic power dissipation equals static power consumption

2.5 Robustness

In this section, the robustness of RF-only circuit is investigated mainly through the analysis of an RF-only inverter's noise margin, and how the noise margin is impacted by the RF amplitude and frequency. Following that, the operating ranges of RF amplitude and frequency are identified based on the worst case Static Noise Margin (SNM) analysis.

2.5.1 Noise Margin Analysis

Due to the output voltage ripples in steady-state, the noise margin of RF-only logic is smaller compared to the conventional CMOS logic with the same power supply amplitude ($VDD = 2A_{RF}$). Furthermore, it is not intuitive to derive an analytical expression for RF-only logic's noise margin based on the well-known "mirror-and-maximum square method" [15], since the voltage transfer function is not monotonic due to the voltage ripples. Instead, we leverage the worst case SNM which is easily determined by circuit simulation to evaluate circuit robustness and study how it varies with design parameters [15]. The simulation methodology based on cross-coupled inverters with a series noise source that emulates an infinite inverter chain is adopted here [16].

The simulated worst-case SNM of an RF-only inverter as a function of the RF frequency is plotted in Figure 2.24. The inverter is powered by an RF amplitude A_{RF} of 0.5V. The plot extends from 10MHz to 5GHz. As the RF frequency increases, the magnitude of output logic level V_{OH} increases, resulting in a larger SNM.

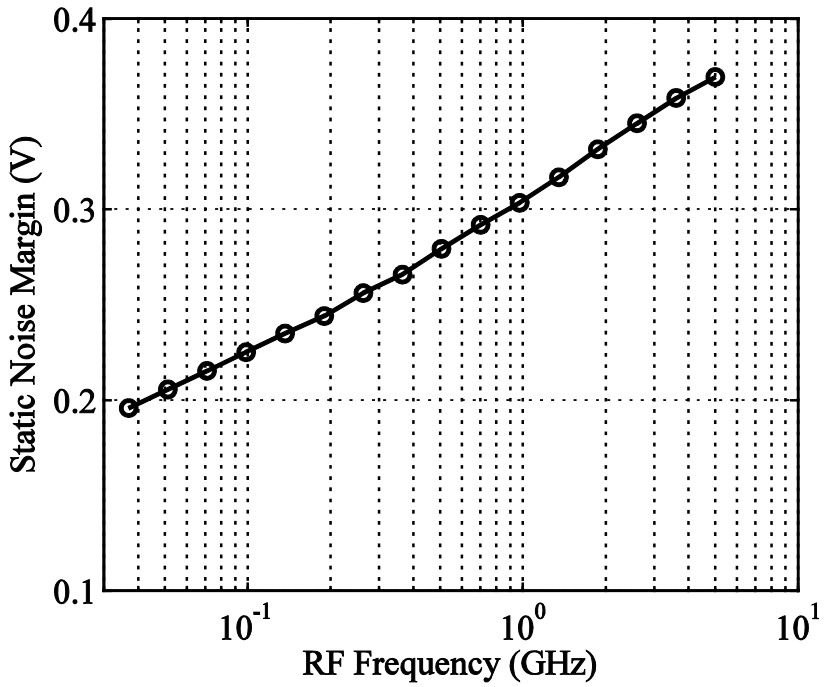


Figure 2.24 Simulated worst case SNM of an RF-only inverter as a function of RF frequency (A_{RF} = 0.5V)

The simulated worst-case SNM and the SNM normalized to the RF amplitude of an RF-only inverter are plotted in Figure 2.25. It is observed that as RF amplitude decreases, the SNM deteriorates due to reduced output swing. Moreover, inspecting the normalized SNM provides the following insights:

- In the super-threshold region, as A_{RF} decreases, the normalized SNM increases. Two schemes are involved. Firstly, the normalized effective swing V_{OH}/A_{RF} increases as A_{RF} decreases, as we discussed in operation analysis and depictured in Figure 2.6. Second, the gain of the RF-only inverter in transition region increases as amplitude reduces, resulting in a larger normalized SNM.

- In the sub-threshold region, the normalized SNM decreases as A_{RF} decreases. This is a result of deterioration of the gate characteristic while the transition region gain approaches one.

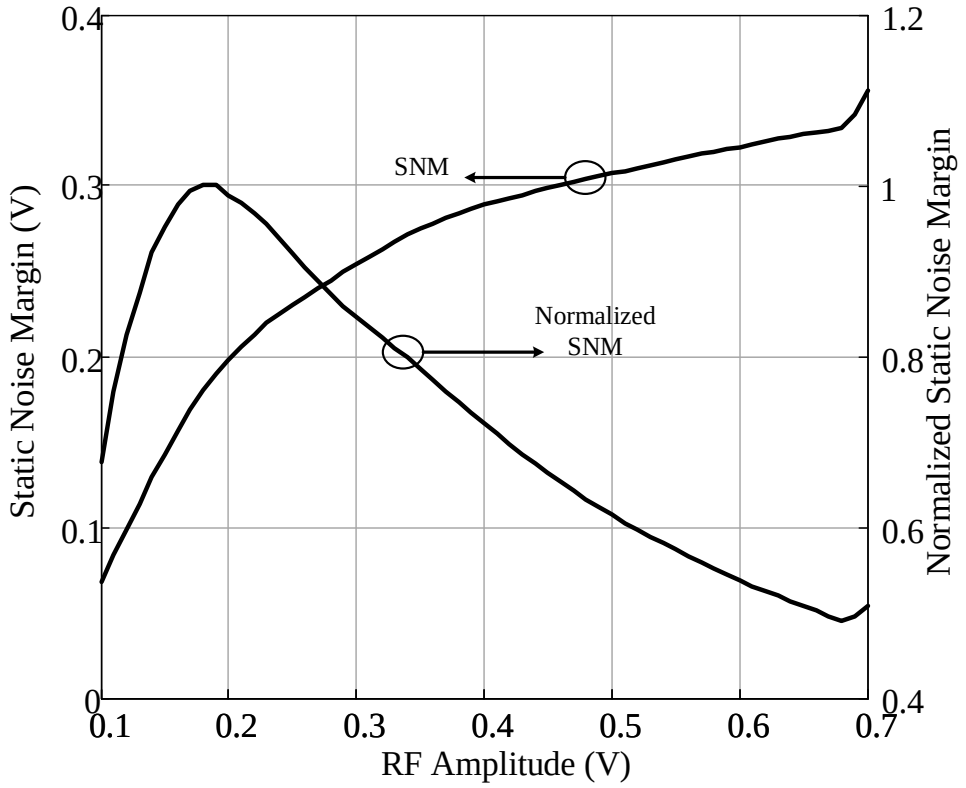


Figure 2.25 Simulated worst-case SNM (both absolute and normalized value) of an RF-only inverter as a function of RF amplitude

2.5.2 Constraints to the RF Supply

The single-phase RF-only topology allows for an RF supply independent design for circuits to operate over a wide range of RF amplitudes and frequencies. In this section, the potential constraints the operating ranges of RF source are discussed.

a. constraints to RF amplitude

The fundamental limit for supply voltage reduction in digital circuits is the excessive degradation of the transistor on-to-off current ratio as supply decrease. A general metric to evaluate the potential limits to the voltage scaling for conventional CMOS logic is the transition region gain. A fundamental constraint to voltage scaling is when the transition region gain approaches one [14]. This metric assumes a nominal operating condition, and not taking into account the process variation. To incorporate process variation, a modeling method based on worst-case SNM and Monte-Carlo simulation is adopted [17]. At each RF amplitude, a worst-case SNM distribution is obtained from Monte-Carlo simulation that captures process variation. Therefore, the probability of a failure corresponds to the area of SNM < 0. It yields the failure probability P_2 for a pair of cross-coupled inverters as a function of RF amplitude. To apply this result to a design with N gates, the acceptable failure rate for a pair of cross-coupled inverters is approximately

$$P_2 = 1 - Y^{\frac{1}{N/2}} \tag{2.65}$$

with Y the desired yield. Given a desired yield, the estimated minimum RF amplitude can be determined as a function of N. Monte-Carlo simulation of 2000 points were conducted, and

the results are plotted in Figure 2.26 for yields of 80% and 90%. From a design perspective, once the number of gates and desired yield are known to the designer, the minimum RF amplitude can be determined by this approach.

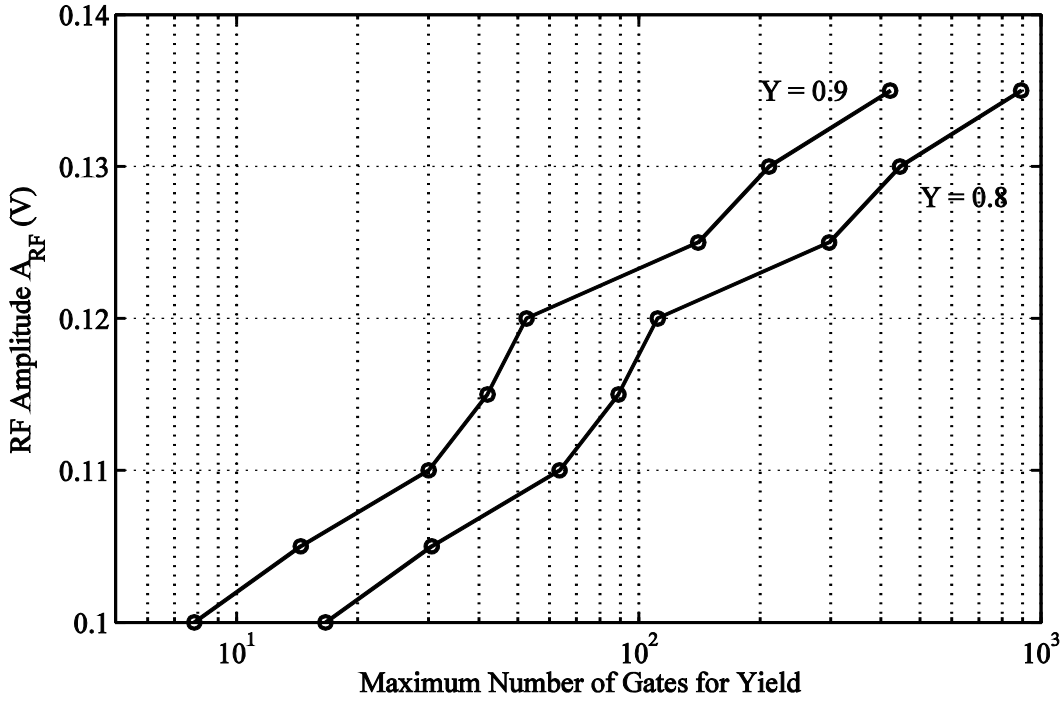


Figure 2.26 The minimum RF amplitude to achieve certain yield levels as a function of numbers of logic gates, based on 2000 point Monte-Carlo simulation

b. constraints to RF frequency

The minimum RF frequency f_{RF_min} to operate an RF-only logic is defined by the leakage current during storage phase. As RF frequency decreases, the length of storage phase T_{off}

increases, rendering a reduced output swing due to the leakage current. There are two primary mechanisms for the leakage current, as shown in Figure 2.27:

- Transistor off-state current I_{off} [18]

  The drain current when the gate voltage is zero keeps discharging the output capacitor during storage phase. For an advanced process with shorter channels and reduced threshold voltage, this leakage current substantially increases, resulting in a higher f_{RF_min}.

- Gate leakage I_{gate} [19]

  Gate leakage current due to direct tunneling through the thin gate oxide turns the gate impedance from capacitive to resistive at low frequencies. The gate frequency f_{gate} is defined as the frequency that capacitive and resistive impedance are equal. This phenomenon sets the lower boundary of RF frequency as $f_{RF\_min} > f_{gate}$. For advanced processes, f_{gate} moves into MHz ranges.

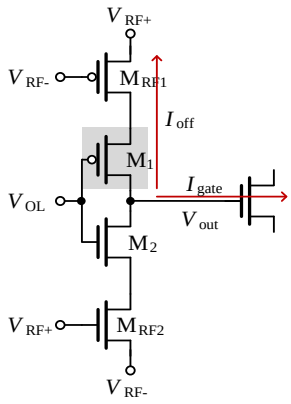


Figure 2.27 Leakage current mechanisms of RF-only inverter in storage phase

The degradation of the output voltage due to leakage currents reduces the noise margin of the following gate, as detailed in the noise margin analysis. Therefore, we can evaluate the RF frequency's impact on the logic operation by monitoring how SNM degrades as RF frequency decreases. We adopt the same simulation method as in noise margin analysis. The simulated worst-case SNM as a function of RF frequency for various RF amplitudes are plotted in Figure 2.28. As RF frequency drops below 1MHz, the SNM is less than 100mV, where process variation starts to dominate the logic failure. As we analyzed earlier, an advanced process will push this f_{RF_min} operating point higher than 1MHz.

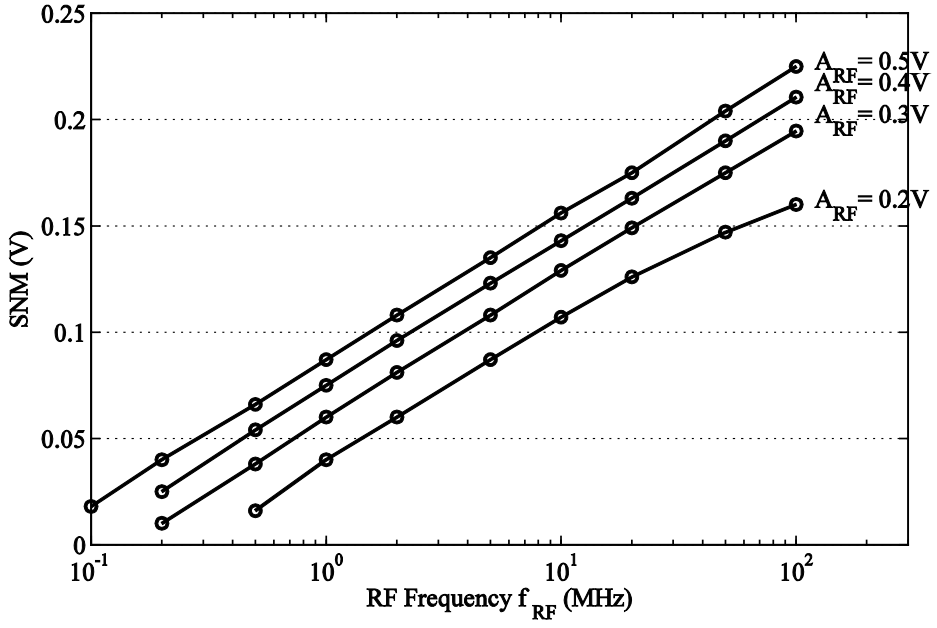


Figure 2.28 Worst case SNM as a function of RF frequency for various RF amplitudes

The upper boundary of RF frequency to operate the single-phase RF-only logic is the f_T of transistors under the corresponding bias condition. We simulate the f_T of both PMOS and NMOS in 0.13μm CMOS technology as a function of RF amplitude and plot the results in Figure 2.29.

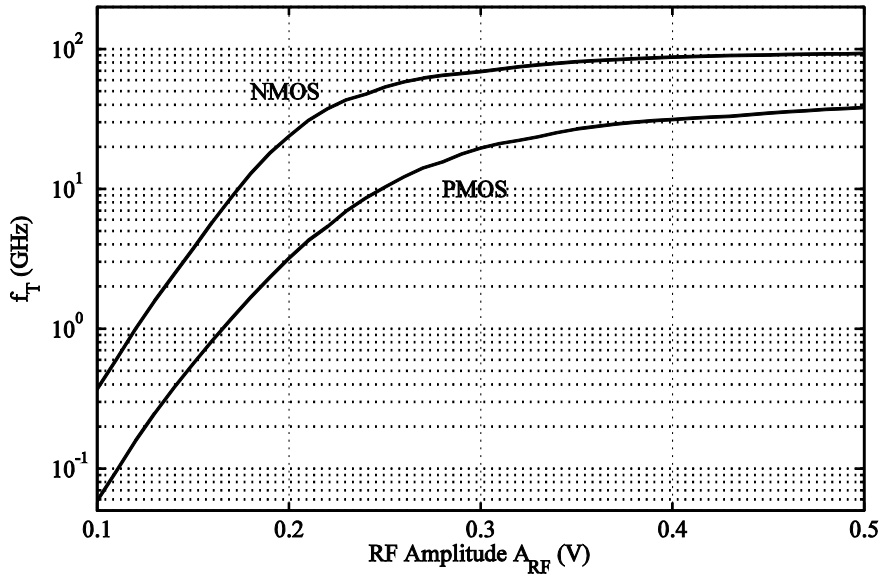


Figure 2.29 Simulated f_T as a function of RF amplitude for both PMOS and NMOS transistors in 0.13μm CMOS technology

Combining the lower and upper boundaries of RF frequency, we get the operating RF frequency range for RF-only logic as a function of RF amplitude, as shown in Figure 2.30. The lower boundary $f_{\text{RF\_min}}$ is defined by achieving a certain level of SNM, while the upper boundary is defined by f_T of PMOS transistor. As RF amplitude increases, the RF frequency range increases substantially. Note this range strongly depends on the process technology.

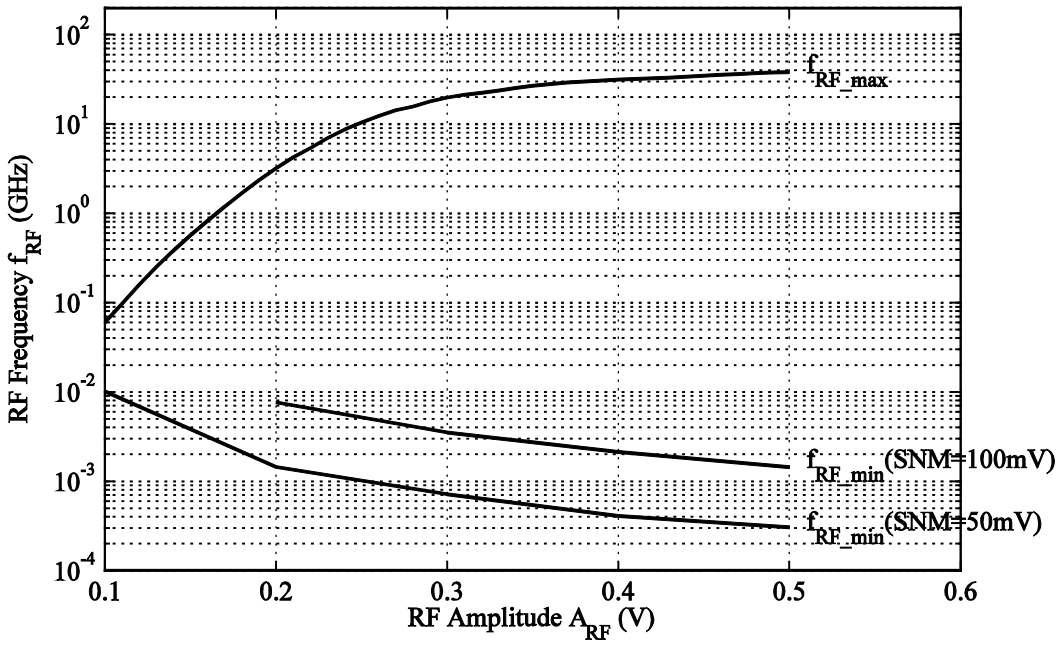


Figure 2.30 Simulated RF frequency range for RF-only logic as a function of RF amplitude

In summary, increasing either RF amplitude or frequency improves the robustness of RF-only logic by increasing its static noise margin.

2.6 Case study: Ring Oscillator

A 61-stage RF-only inverter based ring oscillator was designed and fabricated in 0.13μm CMOS technology to characterize the RF-only logic. The schematic of the

implementation and die photo are shown in Figure 2.31 and Figure 2.32 respectively. The inverter and power supply transistors are minimum sized.

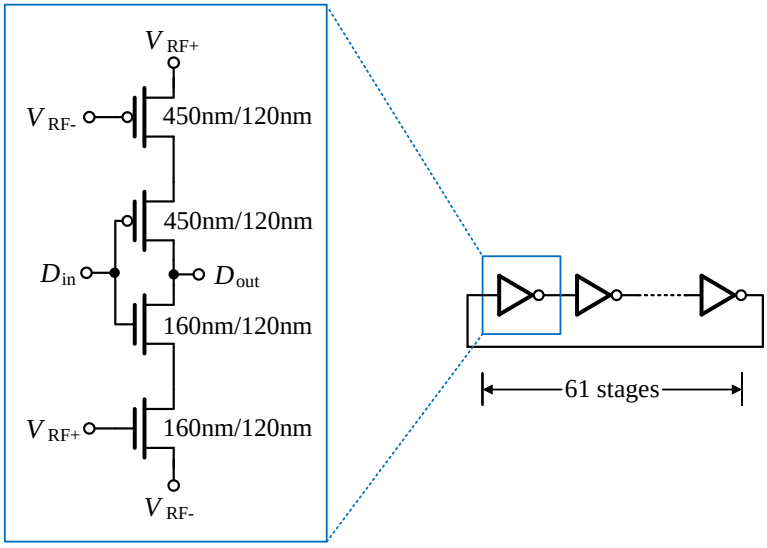


Figure 2.31 Schematic of a 61-stage RF-only logic based ring oscillator

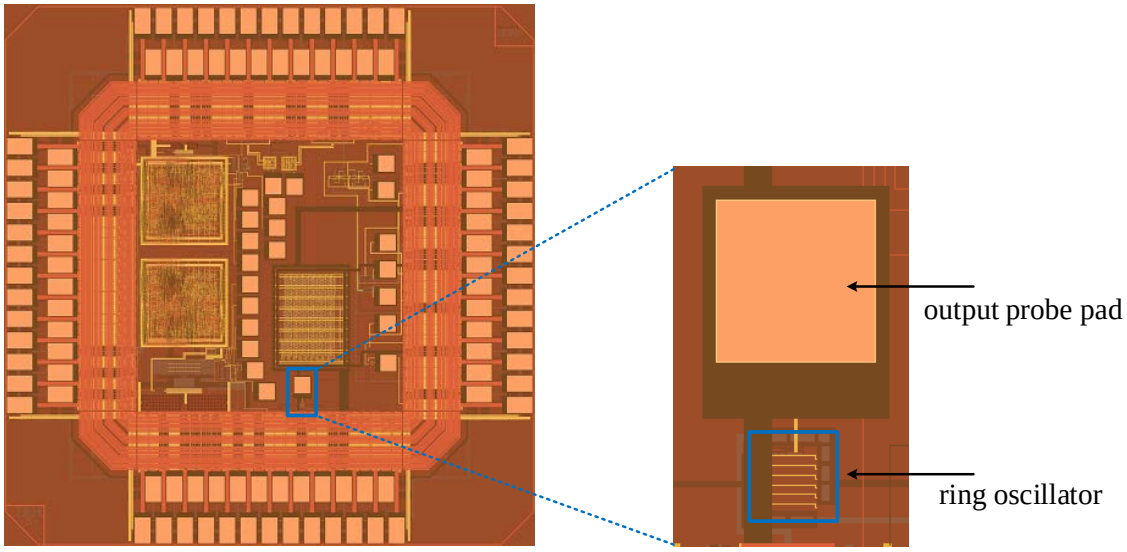


Figure 2.32 Rendered die photo showing the ring oscillator and output probe pad

A testing board was designed for the measurement of this ring oscillator, and the chip was wire-bonded to the testing board. Input signals were fed through SMA connectors and pin headers while ring oscillator output was directly measured using a GGB-35 active high-impedance probe via on-chip probe pad. Figure 2.33 and Figure 2.34 show the setup for speed measurement for the ring oscillator. A Marconi 2024 signal generator was used to generate the RF power signal, which was converted to differential RF signals through a TI ADC-WB-BB balun. The differential RF power signals were fed into the DUT via on-board transmission lines. The ring oscillator output was monitored on the TDS 684B oscilloscope. Ring oscillator speed was measured under various RF amplitude and frequency conditions. The instruments were controlled via a GPIB controller, and MATLAB codes were developed for tuning the RF power supply and extract measurement results. Figure 2.36 shows the captured waveform of the ring oscillator output.

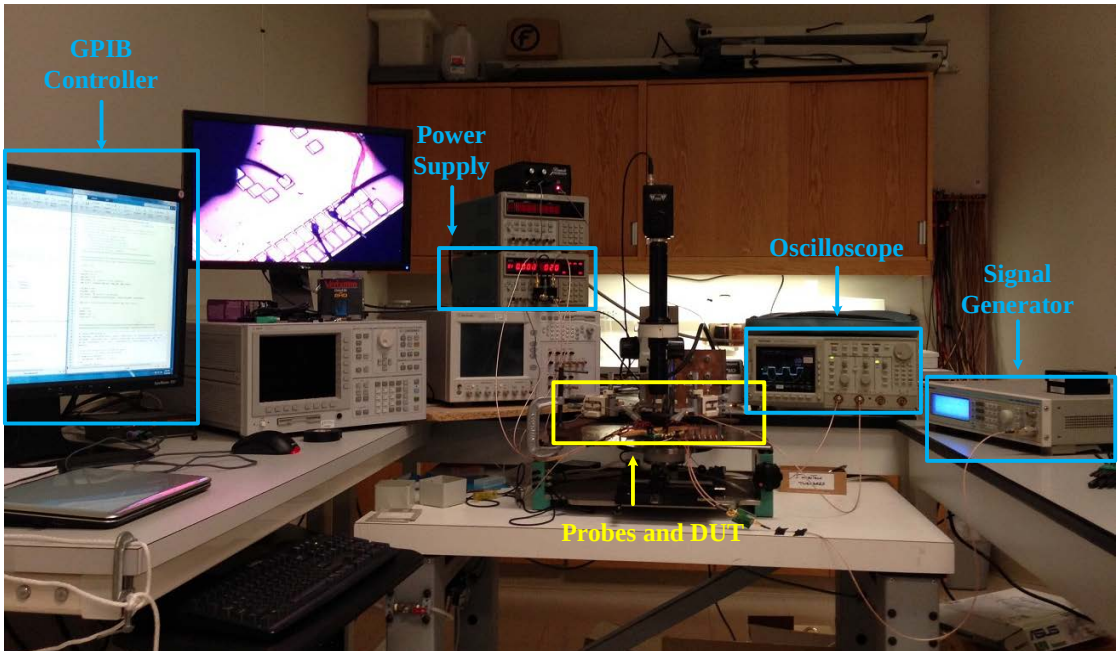


Figure 2.33 Setup for measurement of ring oscillator performance

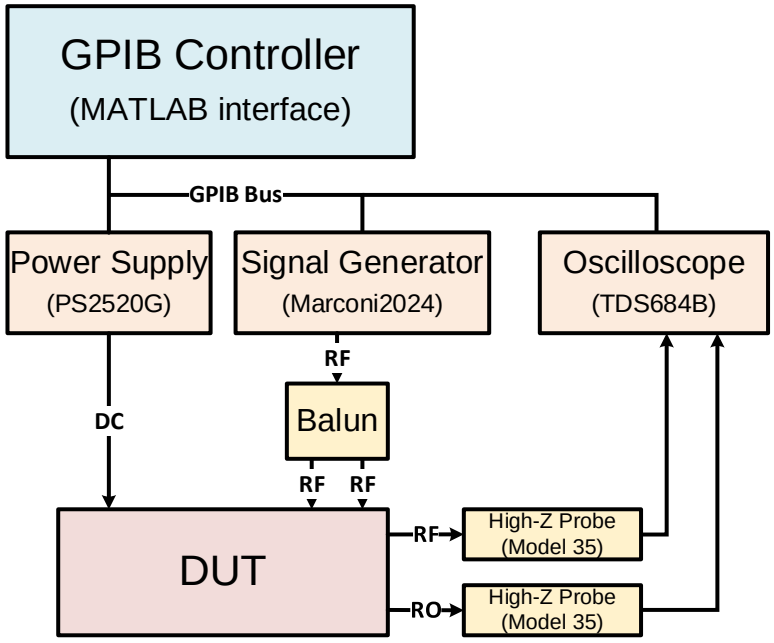


Figure 2.34 Block diagram of ring oscillator performance measurement setup

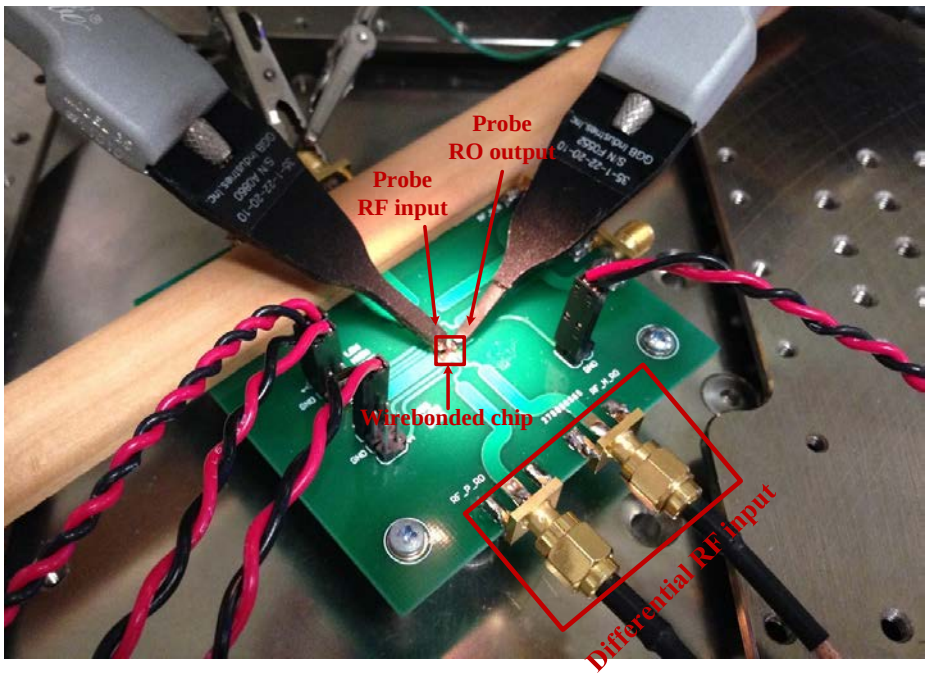


Figure 2.35 Measurement board setup for ring oscillator performance test

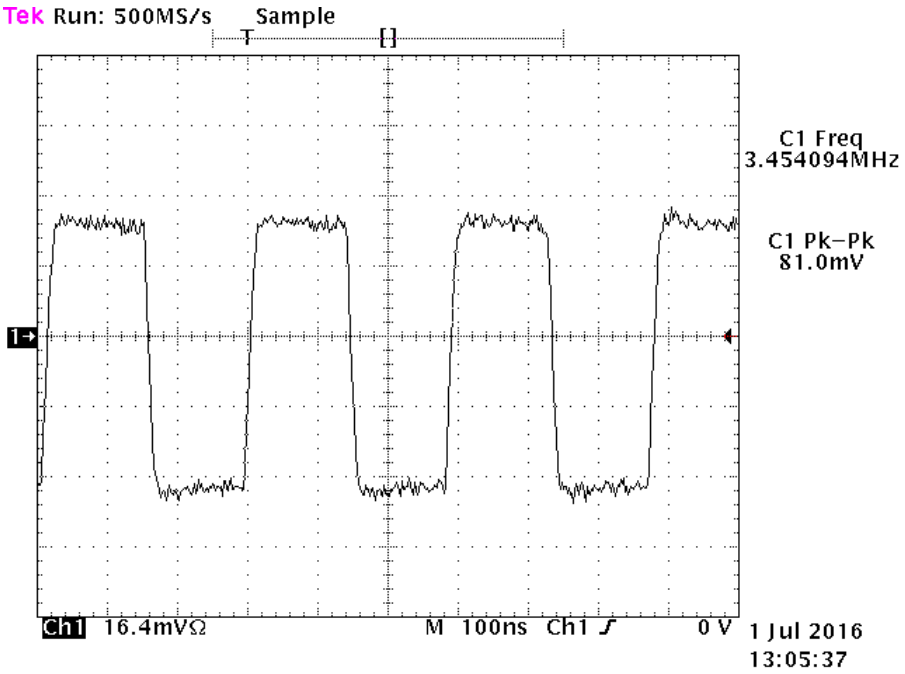


Figure 2.36 Screen capture of the ring oscillator output waveform from oscilloscope

The measured oscillation frequencies are plotted in Figure 2.37 for RF amplitude ranging from 0.2V to 0.5V. As analyzed in Section 2.3, the RF-only logic speed quadratically increases with the RF amplitude. Moreover, RF-only logic's propagation delay is more sensitive to RF frequency in measurement results compared to the simulation results.

The minimum functional RF amplitude for the ring oscillator was also measured from 10MHz to 1GHz, and the results are plotted in Figure 2.38. With the 1GHz RF supply, the minimum RF amplitude achieved is 130mV. As the RF frequency decreases, the noise margin of RF-only logic reduces for the same RF level. Therefore, to maintain the same noise margin, the minimum RF level needs to be increased.

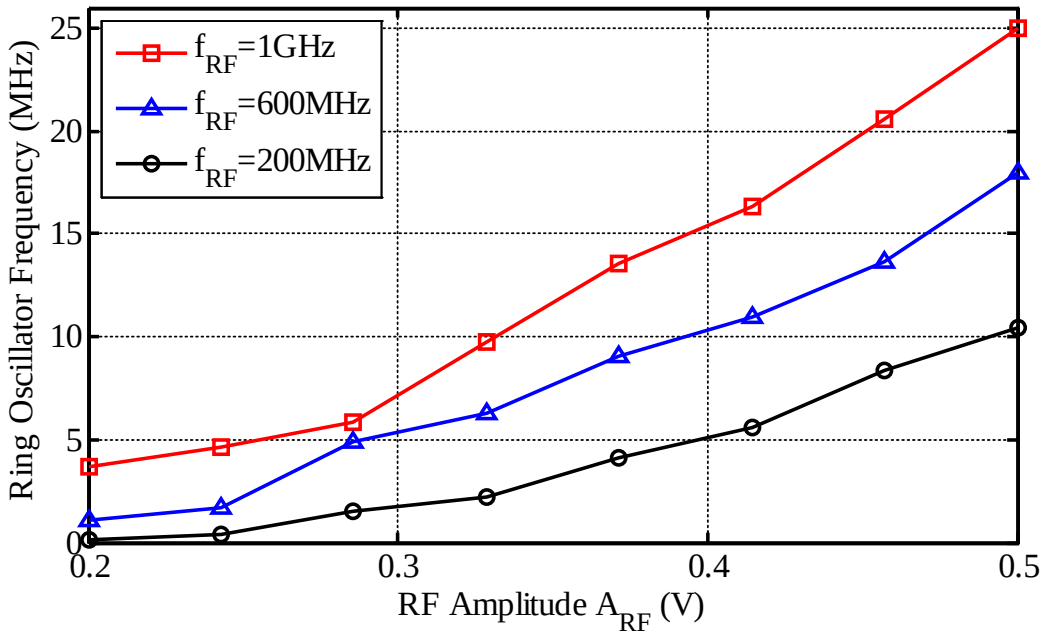


Figure 2.37 Measured ring oscillator speed as a function of RF amplitude for various RF frequencies

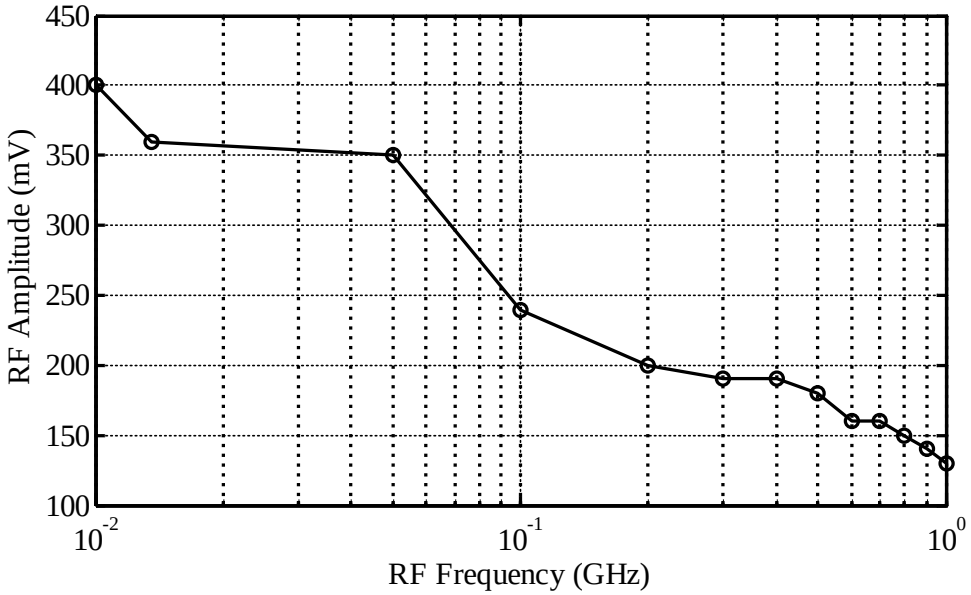


Figure 2.38 Measured minimum functional RF amplitude for ring oscillator as a function of RF frequency

2.7 Summary

In this chapter, basic characteristics (delay, power, and robustness) of a single phase RF-only inverter is analyzed with first-order RC model, simulations, and measurement results. The key characteristics of RF-only logic circuit are summarized as follows:

- The propagation delay as a function of the supply voltage is similar to the classic CMOS gates.
- The propagation delay of RF-only logic is also a function of RF frequency. As RF frequency increases, the propagation delay reduces linearly.

- The power dissipation is dominated by the static power consumption when the circuit operates in the super-threshold region. The static power increases as RF frequency increases. The total power consumption of RF-only logic is generally higher than classic CMOS gates under the same supply level.
- The static noise margin of RF-only logic is generally less than the classic CMOS gates under the same supply level. Increasing RF frequency or amplitude improves static noise margin of RF-only logic.
- The lower frequency boundary of the RF source to power RF-only logic is determined by the channel and gate leakage as well as the technology node.
- The lower amplitude boundary of the RF source to power RF-only logic is around 100mV.
- Dual phase implementation is advantageous regarding robustness, but consumes double the circuit area.
- Dedicated DC biasing voltage is needed to bias the body terminal of the MOS devices to prevent forward biased PN junctions.

Chapter 3

A System Design Methodology for RF-only Logic

In chapter 2, the gate level characteristics of RF-only logic have been rigorously analyzed. We now extend this discussion to address the design methodology and considerations of implementing a complete system using RF-only logic. We analyze RF-only logic for different application scenarios as follows:

- Minimum power consumption operating point for certain performance level
- Minimum energy operating point for digital design. This is equivalent to minimize the power-delay-product (PDP)
- Minimum circuit area for constant performance

While many different parameters can impact the optimal operating points, this chapter focuses on the dual knobs of amplitude and frequency of the RF power supply. A two dimensions design space is established based on these two knobs. Power and performance

simulations of the characterization circuits over a range of RF amplitudes and frequencies provide insight into the behavior of the optimal operating points.

A 4-bit multiplier was designed as the characterization circuit. The multiplier was synthesized based on a dedicated standard cell library for RF-only logics. The details of this standard cell library is covered in Chapter 4. The structure of the implemented test design is shown in Figure 3.1. The multiplier contains a combinational feedback allowing ring oscillation mode operation, which helps to characterize its performance. It requires certain input vector and S<5> is fed back to A<2> ($B = (1100)_2$, $A = (1101)_2$).

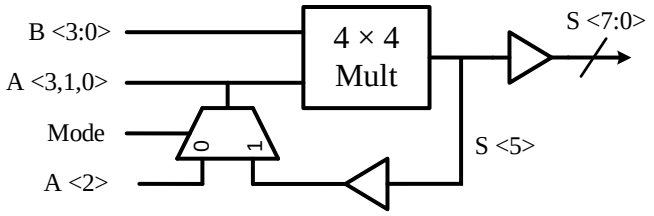


Figure 3.1 Block diagram of a 4×4 multiplier as the testing structure

3.1 Potential Applications

The applications that potentially benefit from RF-only logic's area efficiency must meet two requirements:

- An existing AC/RF power source
- Moderate operating speed

A typical application scenario that meets these two requirements is energy-harvesting-enabled circuits. In the energy harvesting setup, there is usually an RF power source and an AC-DC rectifier that rectifies the received RF power into a DC power supply. Due to the limited power density from harvesting, these applications themselves usually operate at kHz to MHz range. Typical applications include passive RFID tags, micro sensor nodes, and power-up radios. By eliminating the rectifier and storage capacitors, the RF-only based implementation can reduce the circuit area and therefore reduce the chip cost.

As discussed in chapter 2, the dynamic power consumption dominates when the RF-only logic operates in the sub-threshold region. It indicates that the power consumption profile of RF-only logic is comparable with the conventional CMOS logic when operating in the sub-threshold region. On the other hand, the power conversion efficiency of the AC-DC rectifiers in the conventional power harvesting systems decreases as the available power level reduces. Therefore, for power-harvesting-enabled applications that require very low data rate, RF-only logic based approach operates in the sub-threshold region can potentially reduce power consumption and increase operating distance compared to conventional approaches.

3.2 Power for Constant Performance

Minimizing the power consumption while maintaining a certain performance level has always been one of the key design efforts for low power applications. Though the majority of the power harvesting applications operate at moderate to low speed due to the intrinsic power limitations, the communication protocols usually define the minimum performance level for the physical layer. For example, the digital baseband of UHF Gen-2 compatible RFID tags usually operates at 2MHz – 4MHz to support the up to 640kbps data rate. Reducing the power consumption while maintaining the performance level effectively increases the operating distance of these power harvesting based systems.

We simulate the 4-bit multiplier design and show the performance and power consumption contours on the 2-D design space of RF amplitude and frequency. The minimum power consumption point for each performance level are identified and connected to one line by overlapping the two contours. The multiplier is configured in oscillation mode, and we define the performance as its oscillating frequency. Simulation results of the power consumption of this 4-bit multiplier under various RF amplitudes and frequencies are shown in Figure 3.2. In these simulations, the RF amplitude varies from 0.2V to 0.5V, and RF frequency ranges from 100MHz to 2.4GHz. The power consumption numbers are normalized to the minimum level within the simulated region. It is clearly shown that the power consumption increases as RF amplitude or frequency increases. While larger RF amplitude contributes to both dynamic and static power consumption, a higher RF frequency only contributes to more static power consumption.

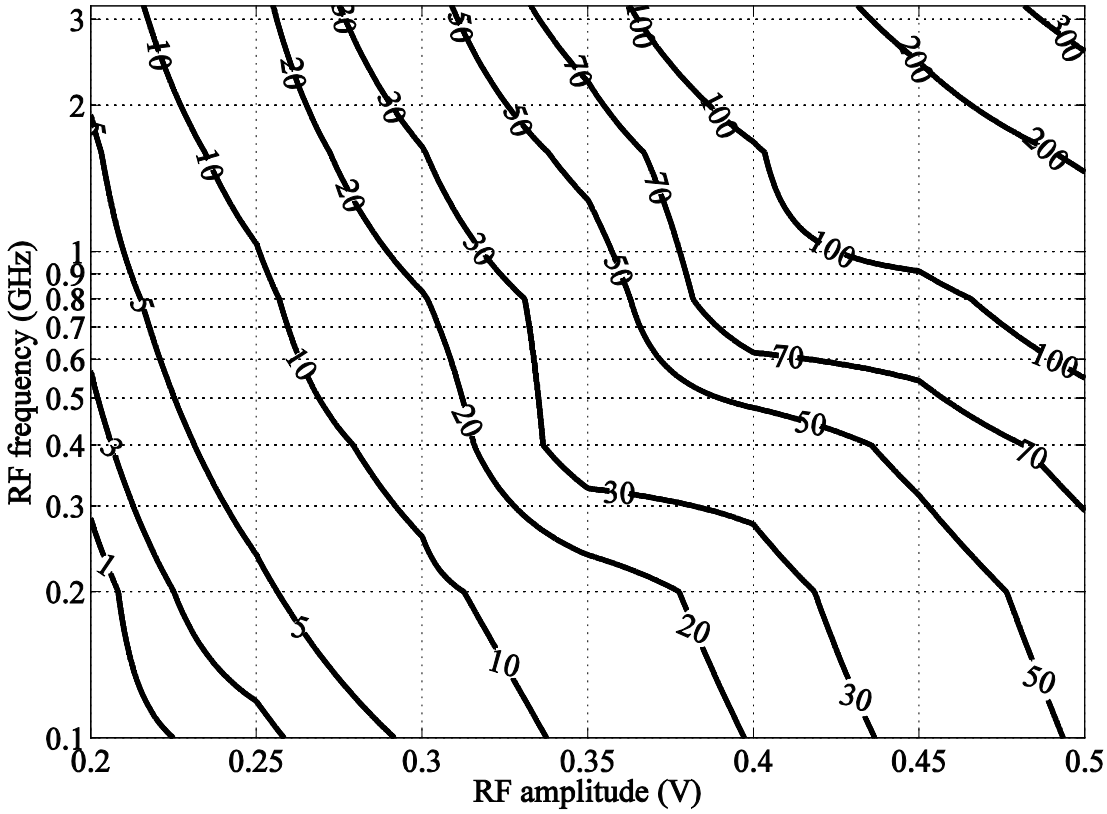


Figure 3.2 Simulated power consumption contours of the 4-bit multiplier on the 2D design space of RF amplitude and frequency, normalized to minimum power level

Figure 3.3 shows the simulated performance contours of the 4-bit multiplier as a function of both RF amplitude and frequency. It indicates that the RF frequency barely affects the performance of the RF-only based multiplier, whereas the performance increases as RF amplitude increases.

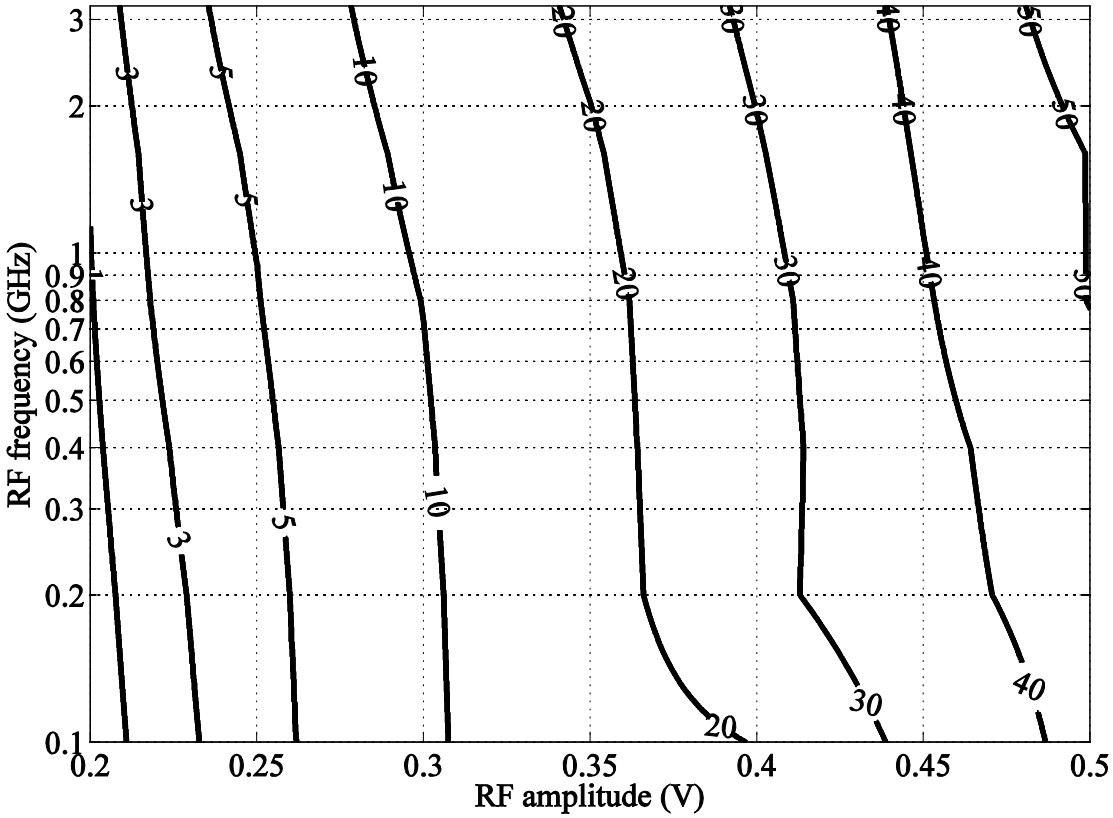


Figure 3.3 Simulated performance contour of the 4-bit multiplier on the 2D design space of RF amplitude and frequency, normalized to minimum level

The power consumption and performance contours are combined and plotted in Figure 3.4. For each performance level, there are operating points on the 2-D design space that corresponds to the low power consumption. Notice that these operating points for low power consumption lie along the low RF frequency region as highlighted in red. This is expected since increasing RF frequency barely improves performance but contributes to static power consumption. The drawback of operating at the low RF frequency region, are the reduced static noise margin due to the large voltage ripples and therefore reduced robustness.

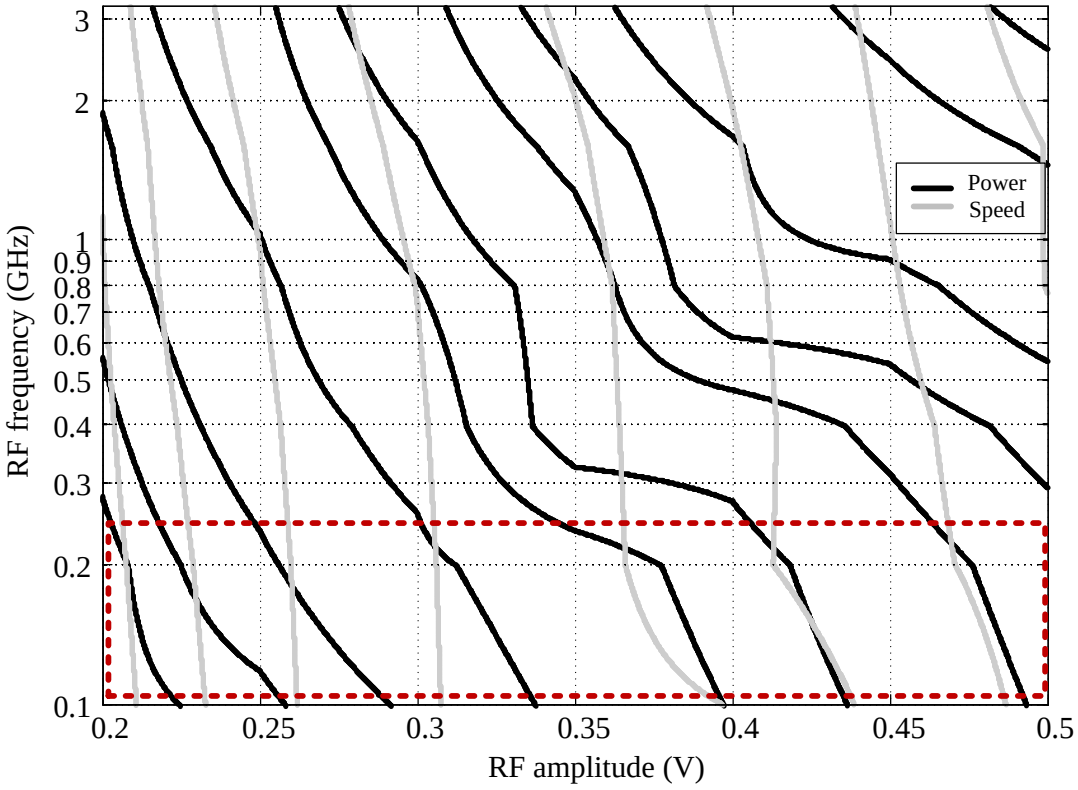


Figure 3.4 Simulated operating points for minimum power consumption of various performance

3.3 PDP: Energy-per-Operation

There is an emerging set of severely energy-constrained applications that have low-speed requirements [20]. Micro-sensor nodes and wake-up radios are two typical applications of this kind. They usually operate on the harvested energy and run at several kHz or even slower. The primary design effort in these applications is to minimize the PDP, namely energy-per-operation.

Simulation of the 4-bit multiplier demonstrates how RF amplitude and frequency affect the PDP. Figure 3.5 shows the constant energy-per-operation contours that normalized to the minimum value. The minimum energy-per-operation point occurs at A_{RF}=0.3mV and f_{RF}= 100MHz. At this point, the multiplier runs at around 10kHz. Since increasing RF frequency does not boost the performance but consumes more static power, the minimum PDP point is close to the RF frequency lower boundary. On the other hand, the RF amplitude for minimum energy point is a result of balancing between dynamic and static energy. By plotting the operating speed of the multiplier on top of the constant PDP contours, we can extract the optimal operating curve which contains the points of lowest PDP for each performance level. The curve is highlighted in red in Figure 3.6. For applications require certain speed, the operating point can be chosen from this curve.

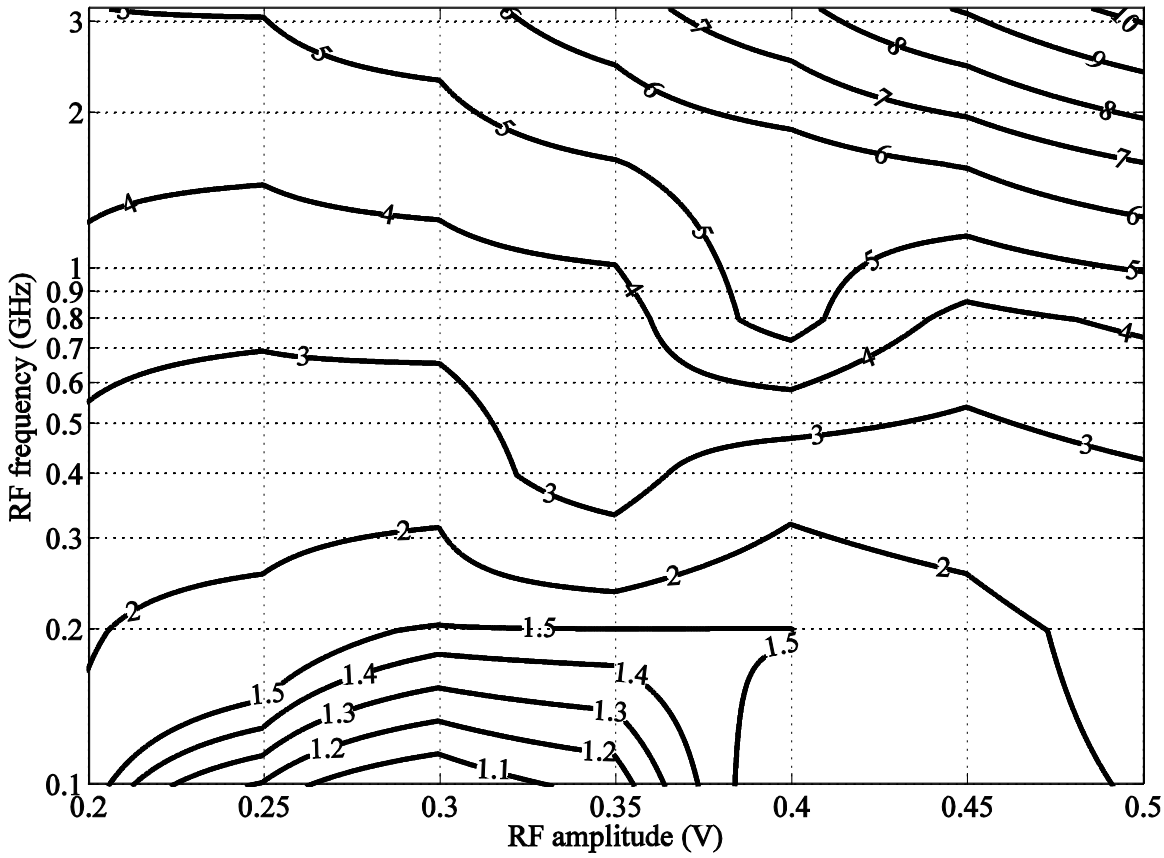


Figure 3.5 Simulated constant energy per operation contours as a function of RF amplitude and frequency

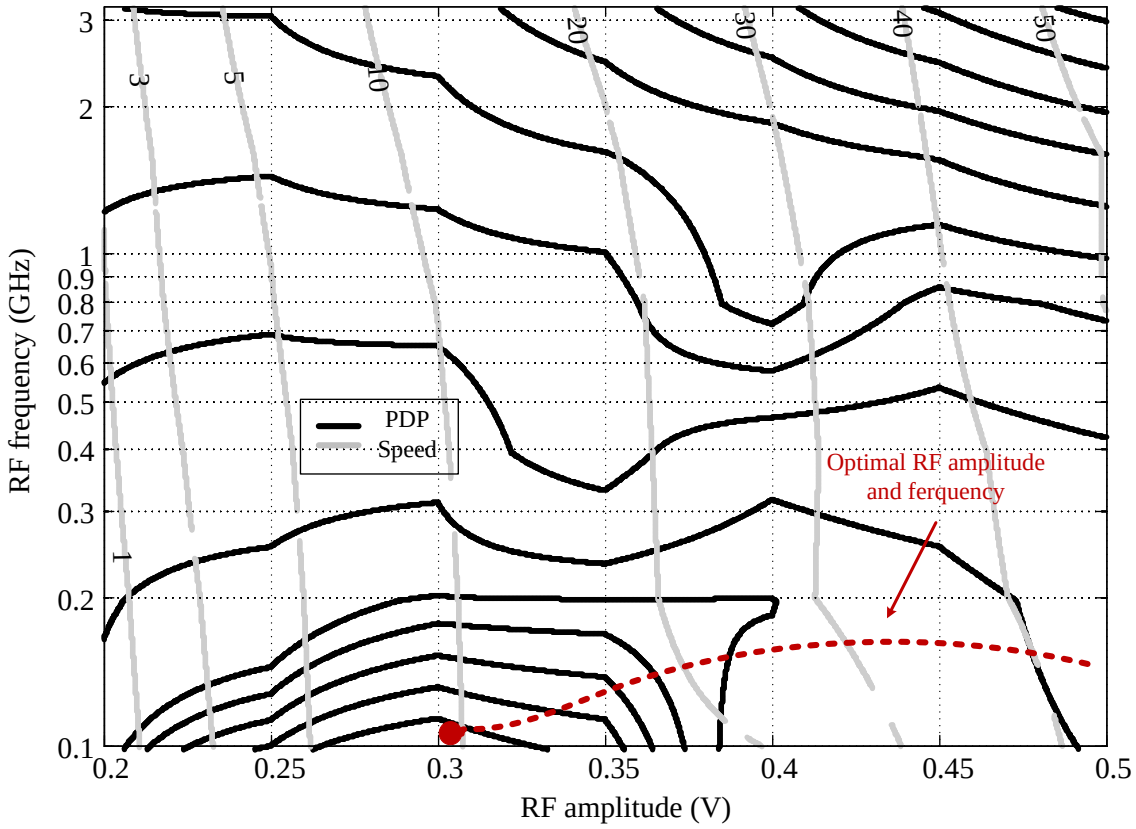


Figure 3.6 Simulated constant energy-per-operation contours as a function of RF amplitude and frequency. Optimal operating point to minimize PDP for each performance level is highlighted in red.

The energy delay product (EDP) is a metric that gives more weight to performance compared to PDP. It is primarily used to evaluate high-performance applications. Since RF-only logic is for low power low-speed designs, we analyzed EDP of RF-only logic for the sake of completeness. Figure 3.7 shows the constant EDP contours that normalized to the minimum value. The minimum EDP point occurs at A_{RF}= 0.45mV and f_{RF}= 200MHz. At this point, the multiplier runs at around 35 kHz.

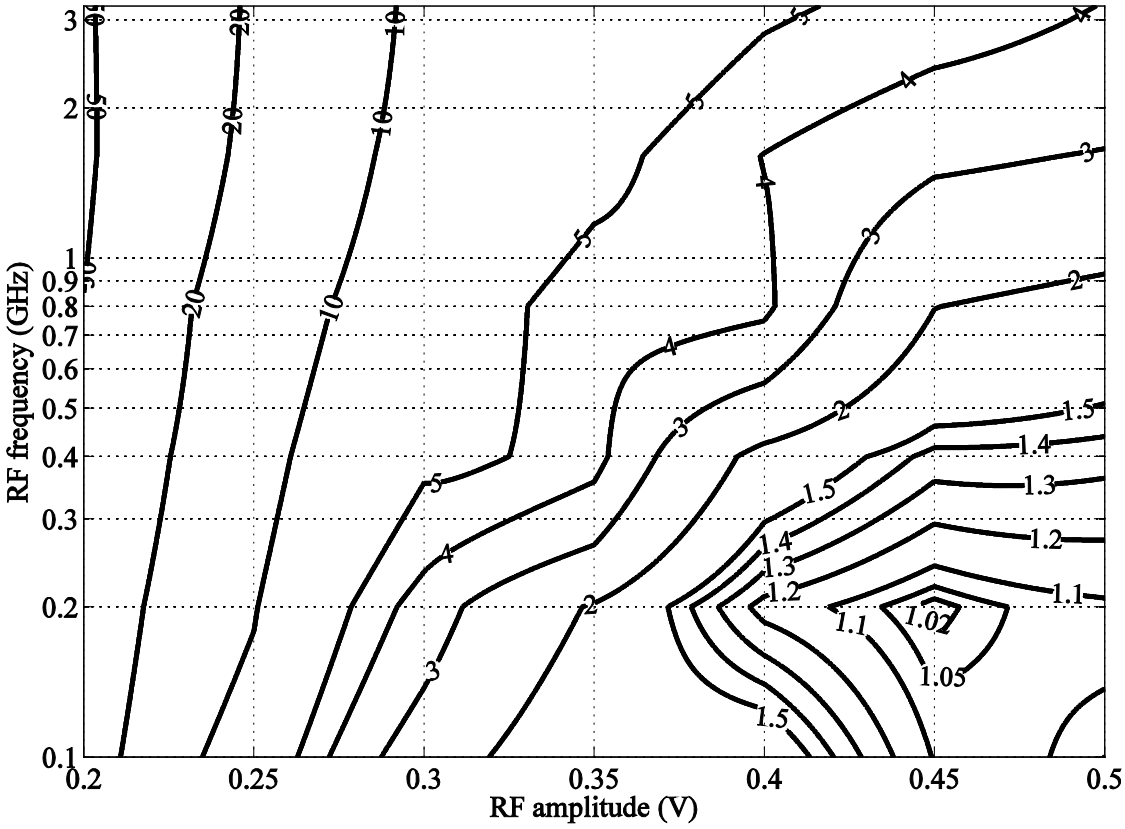


Figure 3.7 Simulated constant energy delay product (EDP) contours as a function of RF amplitude and frequency.

3.4 Area Saving and PST Sharing

Prior discussions of RF-only logic assume that each core logic gate is exclusively powered by a pair of power supply transistors. We call such a pair of power supply transistors a PST cell. To reduce the area overhead introduced by PST cells, a group of core logic gates can share one PST cell in a way that similar to the coarse-grained power gating technique. A cluster of core logic gates can share one PST cell without deteriorating their performance as long as no two gates can charge or discharge simultaneously. Such gates are called mutually exclusive gates [21]. Figure 3.8 illustrates the concept of PST sharing. PST sharing also improves circuit performance by charge sharing during storage phase and reducing voltage ripples during the evaluation phase.

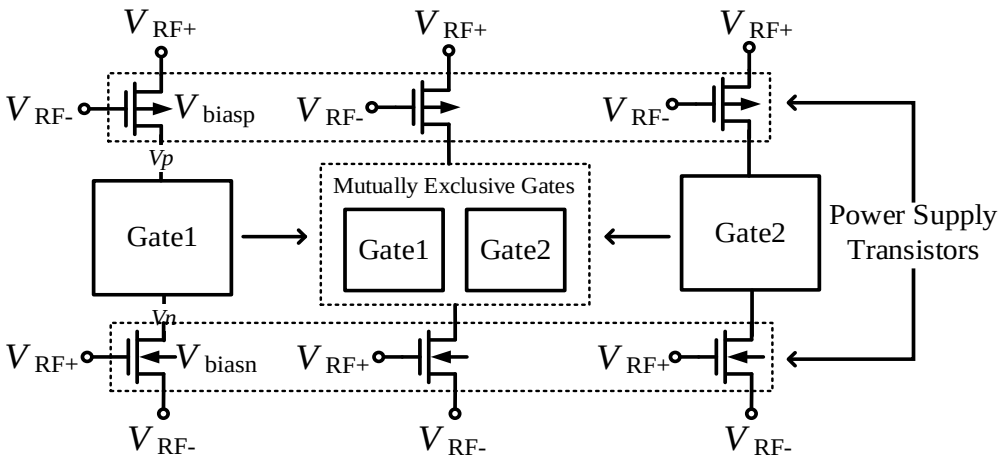


Figure 3.8 Sharing power supply transistor among mutually exclusive gates

The primary approach of PST sharing is to identify the mutual exclusiveness among all the logic gates in a circuit by analyzing their charging patterns, and then group them into clusters while minimizing the cluster count. Putting this approach into the context of the classic digital design flow, the input to this process is the post-synthesis gate level netlist. The output is the gate level netlist with PST cells inserted. Subsequent physical design starts with this manipulated gate level netlist. In this section, the PST sharing methodology is presented in detail and followed by implementation considerations. A sample design is provided in the end with the evaluation of its area saving and performance.

3.4.1 PST Sharing Methodology

The PST sharing methodology assumes each logic gate is of the same unit delay. The possible switching time slots calculated from this model are used as the criteria for mutual exclusiveness (ME) [21]. The switching time for each gate is obtained by analyzing both the structural interconnections and their logic functions. Given the gate level netlist of a circuit, the PST sharing process takes three steps as illustrated in Figure 3.9.

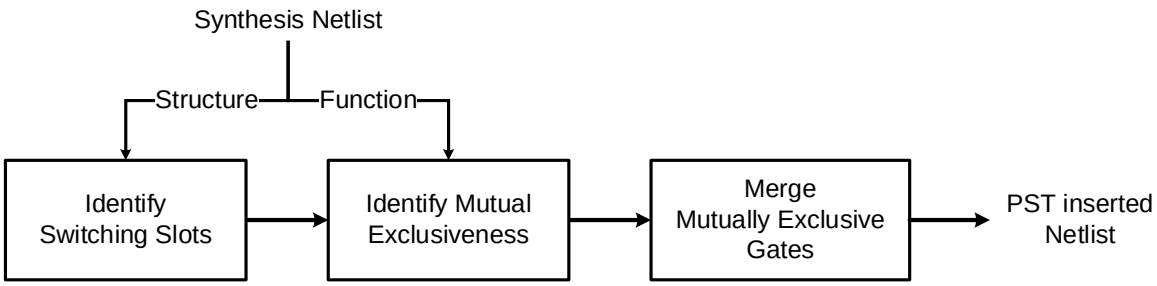


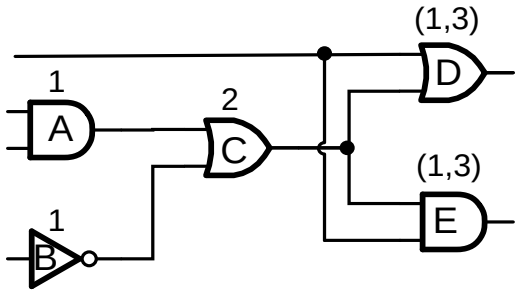
Figure 3.9 Implementation flow of power supply transistor sharing algorithm

1) For each gate in the netlist, identify all the possible time slots that it can switch based on the structural interconnection [21].
2) Explore more mutual exclusiveness by taking into consideration the functionality of the gates as a more rigorous criterion [22].
3) Group logic gates into clusters so that each cluster consists of mutually exclusive gates. Insert one PST cell for each cluster. The number of clusters should be minimized.

a. Identify switching slots based on structural interconnection

A logic gate charges current from its PST cell upon a logic switching. Therefore, the first step towards identifying ME within a given netlist is figuring out the possible switching time of each gate. To simplify the analysis, we adopt the unity delay assumption: each gate features the same propagation delay of an unit period regardless of its functionality or the logic transition directions. Though logic switching pattern is a function of both the

interconnection and functionality, we only consider the interconnection at step one. By defining the block inputs and flip-flop outputs as the start of logic transitions (time slot = 0) and block outputs and flip-flop inputs as the end of all logic transitions, all the possible switching time slots can be obtained. During the analysis, the propagation path for each gate is also recorded and used later in the functionality based ME evaluation. A random gate level circuit is shown in Figure 3.10 as an example. All the gates that may switch at each time slot are also summarized in the figure.



Time Slot	Gate
1	A, B, D, E
2	C
3	D, E

Figure 3.10 Logic gates annotated with all possible switching time slots based on interconnection and unit delay assumption

b. Mutual exclusiveness check based on functionality

Two gates are mutually exclusive if there is no overlap of the possible switching time slots. These charging relations can be represented by a relation graph G_r (V, E) [22]. A vertex $v_i \in V$ stands for one gate, and an edge $(v_i, v_j) \in E$ stands for mutual exclusive relation for gates v_i and v_j. The relation graph can be updated using the switching time slots based on structural interconnections. However, this is an underestimate of mutual exclusiveness since

the charging pattern of a gate also depends on its logic function. Therefore, for each time slot, every pair of gates are checked against their logic function to identify potential logic conflicts along their propagation paths that prohibit their simultaneous switching. If such signal conflict is identified, these two gates are mutually exclusive at this time slot, and their edge in relation graph will not be deleted [22]. We perform conflict check on gate D and E since they are identified as non-ME gates from the topology-based analysis and thereby can switch simultaneously. Gate D and E share the two input nodes n and m as shown in Figure 3.11. For them to switch at time slot 1, node m needs to stay constant, and node n triggers the switching event. In this scenario, for the OR gate D to switch, m needs to stay logic “0”. However, m = 0 desensitizes the AND gate E from switching regardless of node n value. On the other hand, node m staying logic “1” desensitizes gate D from switching. Therefore, gate D and E cannot switch simultaneously based on functional analysis. Thus they are mutually exclusive gates. By repeating the analysis at time slot 3, we can draw the same conclusion. The relation graph is updated after the analysis of each pair of gates. The final relation graph for this sample netlist is shown in Figure 3.11.

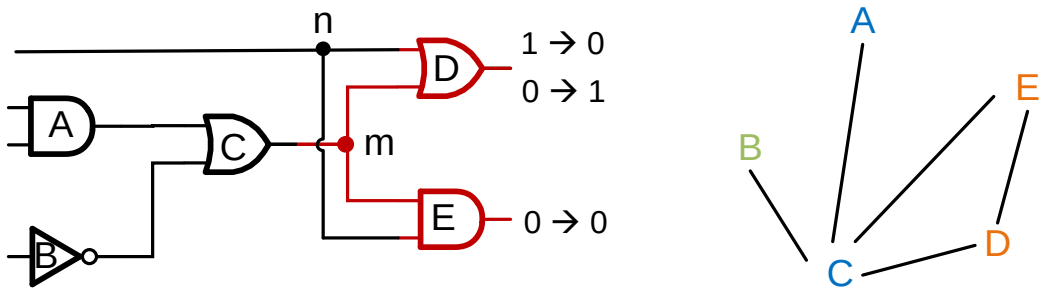


Figure 3.11 Simultaneous switching check based on functionality and final relation graph

c. Merge ME gates

After all the bilateral mutual exclusiveness is obtained and represented in the relation graph, gates can be merged into clusters such that each pair of the gates is mutually exclusive within one cluster. To minimize the area overhead, the number of such clusters should be minimized. The merging process is performed by merging the vertices with existing edges in the relation graph. In [22], a heuristic algorithm is used to merge the two vertices with the largest set of common neighbors at each iteration. It features a computation complexity of $O(n^3)$. Instead, we adopt a hybrid algorithm that features a computation complexity of $O(n^2)$. For each iteration, the vertex with the largest set of neighbors is identified first and then merged with the vertex that has the largest set of common neighbors. The merging completes when there is no pair of vertices to combine. The detailed algorithm implementation of PST sharing including all the three steps is presented in Appendix A.

3.4.2 Impact on Performance

Sharing one PST cell among a cluster of mutual exclusive gates improves gate switching speed and reduces voltage ripple on output node thereby improves noise margin. This is a result of the increased parasitic capacitance on the virtual power nodes V_p and V_n. A sample schematic of three mutually exclusive inverters sharing one PST cell is shown in Figure 3.12. Upon a logic transition, the parasitic capacitors C_p or C_n stores charge during evaluation phase and keeps charging up the output node during storage phase, thus reducing the propagation delay. The parasitic capacitors along with the equivalent turn-on resistors of

transistors also serve as low pass filters to attenuate the output voltage ripples during the evaluation phase.

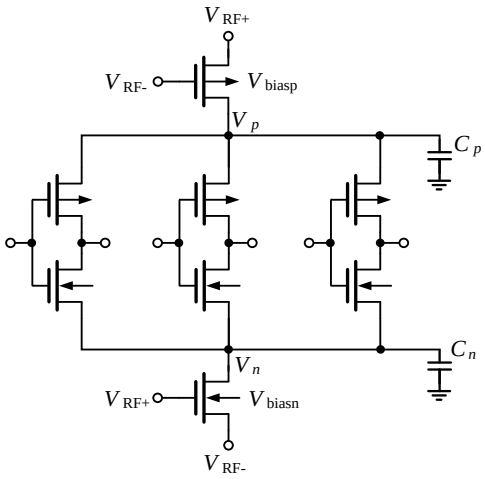


Figure 3.12 Three mutual exclusive RF-only inverters sharing one PST cell

3.4.3 Measured PST Sharing Results

Two 4-bit multipliers were implemented in 0.13μm CMOS technology to study PST sharing's impact on area saving and circuit performance. The PST sharing algorithm was implemented in Python and applied to one of the multipliers, whereas each gate has its own PST cell for the other multiplier. The structure of the implemented test design is shown in Figure 3.1. The multiplier contains a combinational feedback allowing oscillation mode operation for performance measurements. The gate-level netlist of the multiplier was synthesized based on the standard cell library we developed for RF-only logics. The multiplier circuit consists of 135 logic gates, and 34 PST cells were inserted by applying the

algorithm. The layout of these two implementations are presented in Figure 3.13. A summary of the area saving achieved by PST sharing is listed in Table 3.1. A 75% reduction of PST cell count is achieved by sharing the PST cells. The PST cells take 16% of the total circuit area for the PST-sharing-based design, whereas the rectifiers and storage capacitors typically take more than 25% of the chip area.

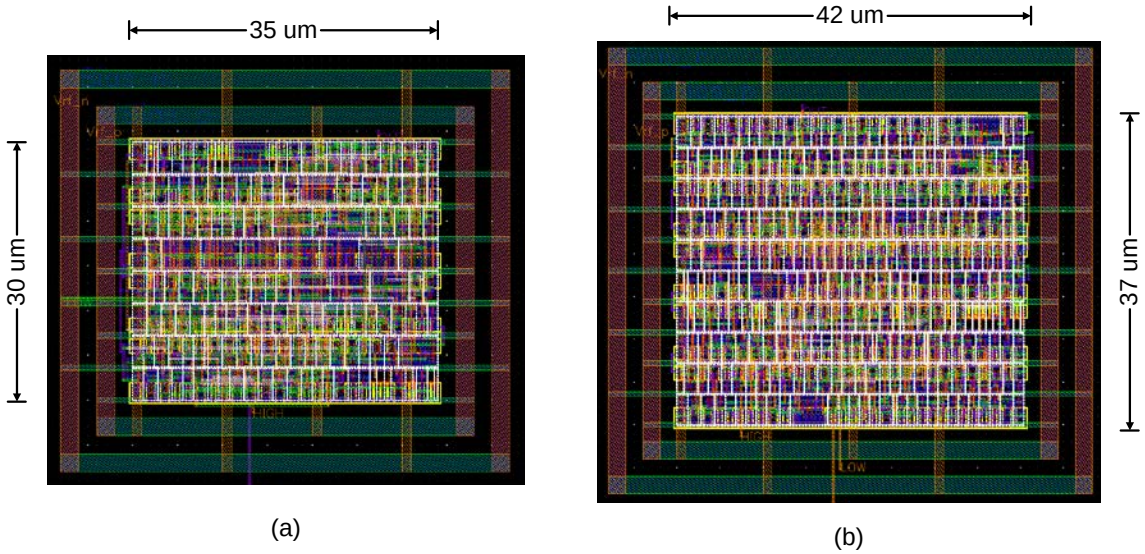


Figure 3.13 Layout of 4×4 multipliers (a) PST sharing implemented (b) Dedicated PST cell for each logic gate without PST sharing

Table 3.1 Summary of area saving from PST sharing

	Gate count Logic + PST	Layout area (μm^2) Logic + PST	PST saving	Overall saving
With PST sharing	135 + 34	734 + 146	75%	33%
Without PST sharing	135 + 135	734 + 583		

The measurement setup for the two multipliers was similar to the ring oscillator design. The multipliers were set to oscillation mode for measurement of their operation performance. High-speed active probes were used to measure the outputs, and their speeds were measured under various RF amplitudes and frequencies. Figure 3.14 shows the performance comparison between the two multipliers implemented with and without PST sharing. As expected from the preceding analysis, PST sharing helps to reduce gate delay by charge sharing among the mutually exclusive gates. Therefore, the one with PST sharing runs faster than its counterpart under the same RF amplitude and frequency. On the other hand, operation speed increases as RF amplitude or frequency increases, which is aligned with the conclusion in Chapter 2.

Overall, the PST sharing algorithm helps to reduce the PST area overhead and improve circuit performance by charge sharing.

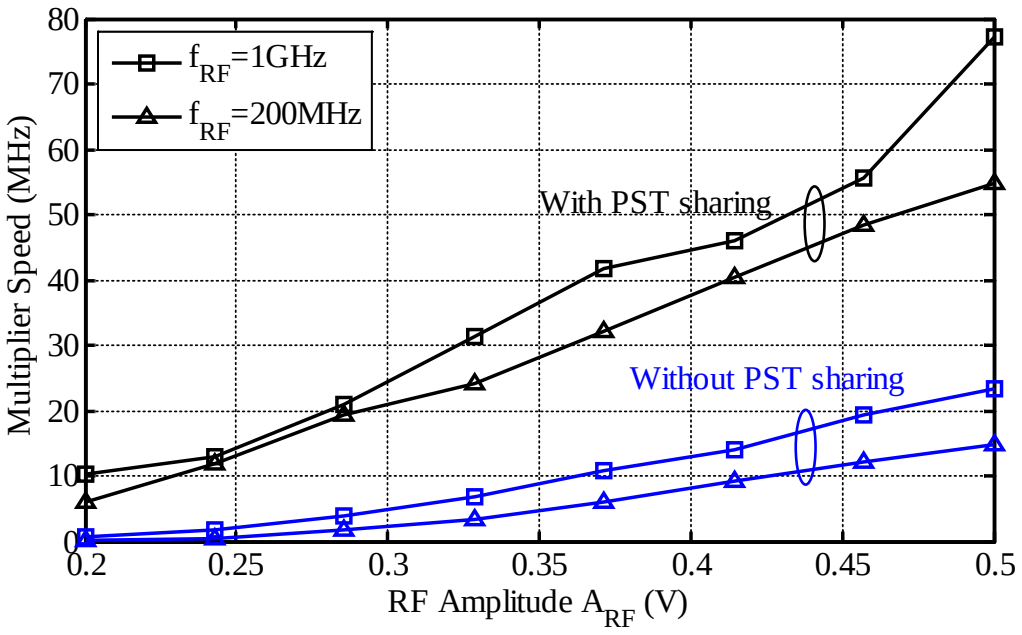


Figure 3.14 Speed of multipliers with and without PST sharing implemented as a function of RF amplitude and frequency

3.5 Area Analysis

The RF-DC power rectifier and storage capacitors take a significant amount of chip area in conventional wirelessly powered circuits. They can be eliminated in RF-only logic based implementation and thus saves chip area. However, the power supply transistors of RF-only logic introduce additional area overhead. This section analyzes the area overhead introduced in these two powering approaches by reviewing state-of-the-art designs. It shows that RF-only logic implementation that employs PST sharing features a smaller circuit size compared

to the rectifier based implementation, though at the expense of increased power consumption. Note the area analysis is based on achieving a constant performance level. We ignore any area saving techniques within register-transfer level (RTL) design or logic synthesis, since they can be applied to both approaches.

3.5.1 Area Overhead of RF-only Logic Approach

The primary area overhead of RF-only logic based design stems from the power supply transistors. It is independent of the operating RF amplitude or frequency. On the other hand, it is a function of the sizing ratio of core logic and PST cell, gate level netlist topology, and the aggressiveness of the PST sharing algorithm. A PST cell can be sized relatively small compared to the core logic to reduce area overhead but at the expense of reduced driving strength and speed. For ultra-low power and low-speed applications, this may not be a major concern. Applying PST sharing algorithm to post-synthesis gate level netlist helps to reduce the number of PST cells without sacrificing the circuit performance. The compression ratio of PST algorithm depends on both the gate level netlist topology as well as the algorithm itself. The PST sharing algorithm is most efficient for balanced circuits and sparsely connected netlists [21]. The PST sharing algorithm introduced in this chapter explores the first order mutual exclusiveness in which no two gates can switch simultaneously within one cluster. More aggressive or higher order mutual exclusiveness that allows more than one gates switch simultaneously can further reduce the number of PST cells.

Here we estimate the average area overhead introduced by PST cells under first order PST sharing. The baseband logic of UHF Gen-2 protocol was implemented in RTL and

synthesized with the RF-only logic library. Table 3.2 summarizes the number of PST cells inserted for each block and the overall area overhead introduced with respective to the core logic. It indicates that the average area overhead of PST cells is around 20% of the core logic gates.

Table 3.2 Number of PST cells inserted for each block and associated area overhead

Modules	CRC5	RNG	CRC16	Seq	Mem_ctr	Encode	Demo	Ctrl	Deco	**Total**
Gate count	35	85	112	215	353	363	763	1 172	1 340	**4 786**
PST count	24	56	71	93	180	163	370	516	655	**2 142**
Gate area	604	1 786	1 941	1 860	2 666	3 746	9 531	12 228	12 813	**47 175**
PST area	103	241	306	401	777	704	1 598	2 229	2 829	**9 214**
Overhead	17%	13%	15%	21%	29%	18%	16%	18%	22%	**19%**

3.5.2 Area Overhead of Rectifier Approach

The area overhead of rectifier based approach stems from the AC-DC power rectifier and storage capacitors. There is no formula to estimate this area overhead due to the various implementations and operating conditions. The MOS devices in a rectifier are usually sized large to reduce the resistive power loss. The number of stages is a function of the minimum operational power level as well as the output voltage level. The minimum amount of storage capacitor is defined by the maximum allowed voltage ripple on the power supply as well as the energy budget for duty-cycled operations. These design considerations usually lead to a minimum on-chip storage capacitor of several hundreds of pF. Table 3.3 summarizes the area

overhead of rectifier and storage capacitors from existing literatures of wireless-powered nodes. It shows that rectifier and storage capacitors usually take a quarter, if not more, of the die area.

Table 3.3 Summary of rectifier and storage capacitor area overhead from literature

Work	Rectifier + capacitor area	Total chip area (mm^2)	Technology (nm)
Yin 2010 [2]	25%	1.1	180
Duong 2013 [23]	50%	3.45	180
Yao 2014 [4]	50%	0.9	180
Lee 2014 [3]	50%	1.1	130

3.6 System Implementation Considerations

The preceding sections discussed the impact of RF amplitude and frequency on various application scenarios and how to identify the optimal operating points. In this section, a few system level considerations for designing with RF-only logic are presented.

3.6.1 Powering Scheme

In a real operating scenario, the RF power signal may fluctuate due to changes in distance, multipath fading, and modulation. The performance of RF-only logic is more

sensitive to RF amplitude than RF frequency. For ultra-low power applications, a varying RF amplitude is not a major concern as long as it is higher than the minimum level for the circuit to operate. However, a constant and stable RF amplitude is necessary for any application with specific speed requirements. The optimal RF amplitude is identified based on the primary metric, and the circuits are characterized for that amplitude. It is also the minimum RF level the circuit can maintain the required performance level. With the help of an AC voltage limiter that clamps the RF signal to the threshold level, the circuits can operate with RF amplitude higher than the optimal level.

For RF-powered passive circuits, the RF signal is usually used as the carrier for communication modulation. Frequency shift keying (FSK) and phase shift keying (PSK) modulated RF signals can power RF-only logic directly since RF-only logic's performance is not sensitive to RF frequency or phase. On the other hand, the amplitude shift keying (ASK) modulated RF signals pose challenges for directly powering RF-only logic. One solution in ASK scenario is to pause circuit operations during ASK low periods and resume operation during ASK high periods.

3.6.2 Communication Scheme

In a typical wireless communication scenario, how to implement modulation and demodulation using RF-only logic is a major concern. Demodulation of ASK signals is limited to the ones that useful information only encoded in the ASK high periods since RF-only logic can barely operate during ASK low periods. Demodulation of FSK and PSK signals are possible with a passive mixer and low noise LO. The primary challenge is the

generation of an accurate low noise carrier signal. A ring oscillator designed with RF-only logic can provide a moderate noise level reference signal, but the frequency is lower than the original RF frequency. Passive frequency multiplication schemes need to be explored here to generate the LO.

For passive wireless nodes without active transmitter, backscatter is an efficient method for reverse link communication. The node talks to the interrogator by modulating its load impedance. ASK modulation is not preferred in backscatter since it varies the amplitude of RF signals, therefore disturbing the circuit performance. On the other hand, PSK and FSK are preferred since it keeps a constant RF amplitude by manipulating the load reactance only.

3.6.3 Others

The RF-only logic is inherently built for digital logic circuits. Therefore, RF-only logic gates can perform both combinational and sequential logic operations. However, due to the lack of accurate voltage or current sources, most of the mixed-signal or analog blocks are quite difficult to be built using RF-only logic. One can design an RF-only based discrete time comparator by sampling the input signals that drive cross-coupled inverters. For robustness considerations, the typical data rate an RF-only logic circuit can support is at least one order of magnitude lower than the RF frequency. Therefore, RF-only logic is typically used in moderate-speed, low-power, and low-cost applications.

3.7 Summary

This chapter discussed how RF amplitude and frequency impact RF-only logic design at the system level, by scrutinizing typical design scenarios. The conclusions of prior discussions are summarized in Figure 3.15 and listed as follows:

- RF-only logic is most suitable for area/cost sensitive, moderate speed, low power passive wireless applications. The primary design knobs at system level are the amplitude and frequency of RF power supply.
- To minimize power consumption for constant performance applications, the circuit should operate at low RF frequency region.
- The optimal energy per operation operating point is around 0.3V amplitude, 100MHz frequency.
- The optimal EDP operating point is around 0.45V amplitude, 200MHz frequency.

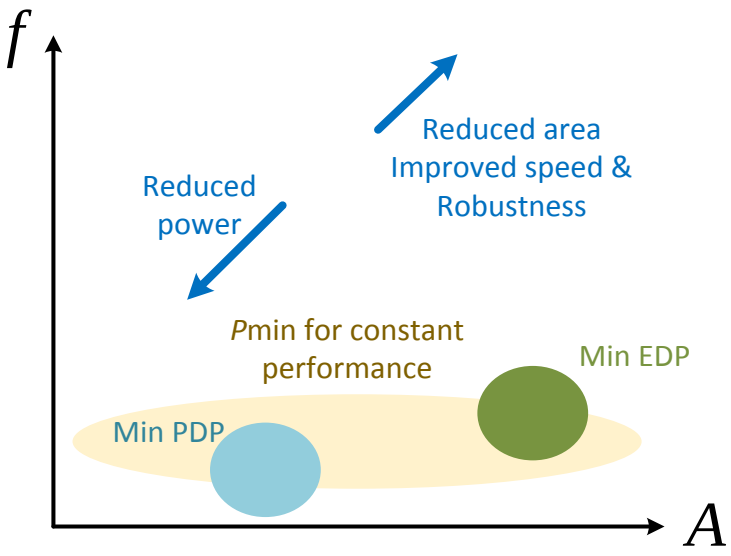


Figure 3.15 RF-only design space and trends on the major metrics

Here are some of the key insights comparing RF-only logic based design with the classic rectifier based approach:

- RF-only logic based power solution can be treated as a fully distributed solution as shown in Figure 3.16. It features the smallest circuit area at the cost of high power consumption. Whereas the classic rectifier + storage capacitor power solution is on the other side of the spectrum: large circuit area with minimum power consumption. The PST sharing scheme of combining mutually exclusive gates is one step further towards the center of the spectrum, where there might be an optimal solution.

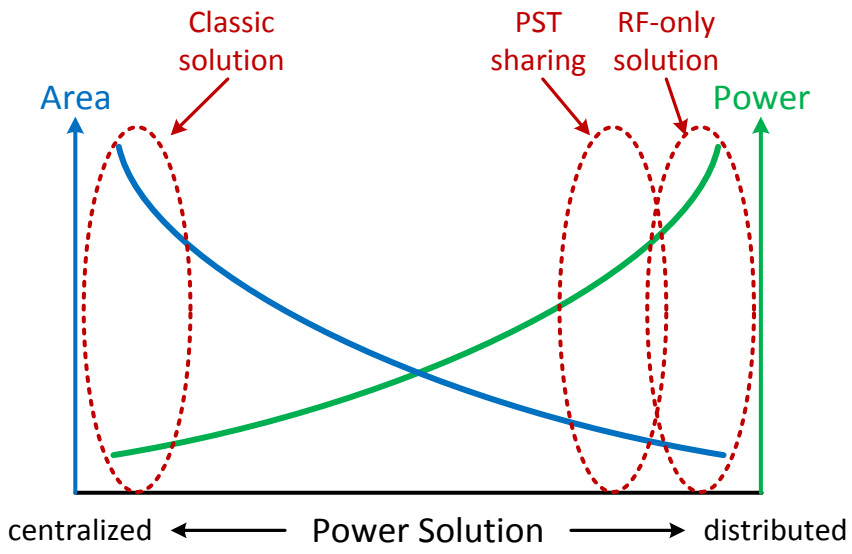


Figure 3.16 Comparison of classic power solution and RF-only logic based power solution

- RF-only logic based solution is one stage rectification solution and here is no voltage multiplication. It comes with intrinsic low sensitivity.
- In the classic rectifier + storage capacitor power solution, the capacitor works as a reservoir which accumulates energy and therefore supports ultra-low power applications and duty-cycled operations. The lack of such energy storage mechanism in RF-only logic solution limits its effectiveness in low-power applications.

Chapter 4

Design of a Rectifier-Free Gen-2 Compatible RFID Transponder Using RF-Only Logic

This chapter presents the design of an EPC Class-1 Generation-2 compliant RFID tag using RF-only logic. RFID enables asset tracking, supply chain management, payment system, security and access control. It is a rapidly growing billion dollar market. Figure 4.1 shows the projected market size. RFID transponders equipped with various sensors open a host of other applications and perform as a key enabler of the Internet-of-things. Due to their long operating range and low cost, the EPC Class-1 Generation-2 compliant RFID tags working at UHF are the most widely used tags.

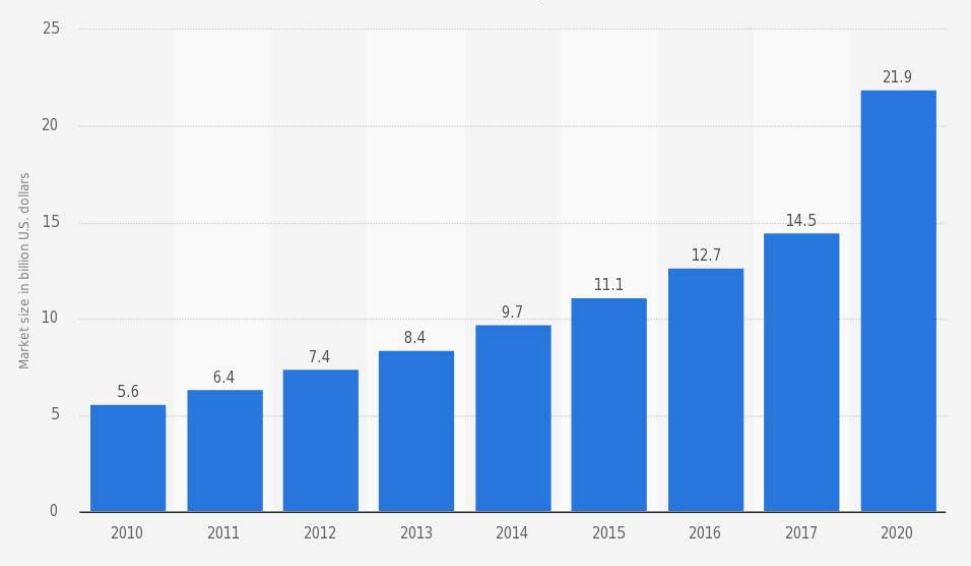


Figure 4.1 Total RFID market projections in US$ billions [24]

Therefore, we designed a rectifier-free RFID tag using RF-only logic as a case study of the design methodology discussed in the preceding chapters. By eliminating the AC-DC rectifier and storage capacitors that exist in the conventional passive RFID tags, our approach managed to reduce the RFID chip area and cost. The RFID tag was implemented in a 0.13 μm CMOS technology and featured dimensions of 0.6 mm × 0.3 mm. Its sensitivity is 3.3 dBm from measurement. This chapter starts with the overview of RFID technology and UHF Gen-2 protocol. After that, the design and implementation details of the RFID tag are presented. The measured results and comparison with state-of-the-art designs are discussed at the end of this chapter.

4.1 Overview

RFID usually refers to a wireless communication system that identifies the location of the tagged items and tracks the movements of physical objects, especially in non-line-of-sight scenarios. An RFID system usually consists of an interrogator (or reader) and a transponder (or tag), that is attached to the object of interest. For the scope of this work, we focus on the RFID tags. RFID tags can be classified into active, semi-active and passive tags based on their power source. Active tags are equipped with local energy sources (usually batteries) that power both the baseband circuitry and the active RF transceivers. A semi-passive tag usually uses the local battery to power the baseband circuitry only while utilizes backscatter approach for tag-to-reader communication. Passive tags have no independent power source and depend on rectification of the received power from the reader to support the operation of their circuitry [25]. The tremendous advantages of passive tags being low-cost, simple, and maintenance-free make them the most widely used tags. The rest of discussion centers on passive RFID tags. Passive RFID tags are distinguished by their operating frequencies. They feature various operating ranges and applications as summarized in Figure 4.2.

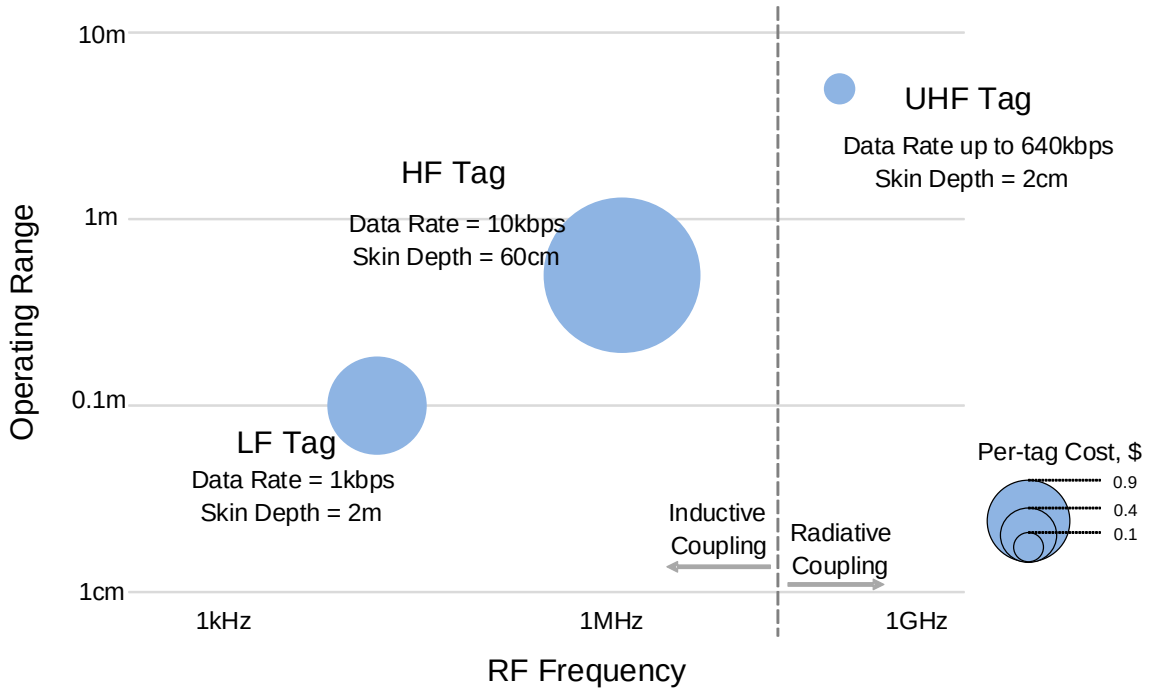


Figure 4.2 Passive RFID tags classification based on operating frequency

Low frequency (LF) and high frequency (HF) tags support sub-meter operating ranges. They are particularly appropriate for animal ID, access control, and smart cards applications due to the deep penetration into animal tissues and water. UHF tags benefit from long operating range and faster data rate. Therefore, passive UHF tags are the most widely used tags for asset tracking and supply chain management, where the extended operating range adds flexibility. An example of a typical UHF passive tag is shown in Figure 4.3. The tag consists of a plastic inlay, a dipole antenna, and a RFID tag chip.

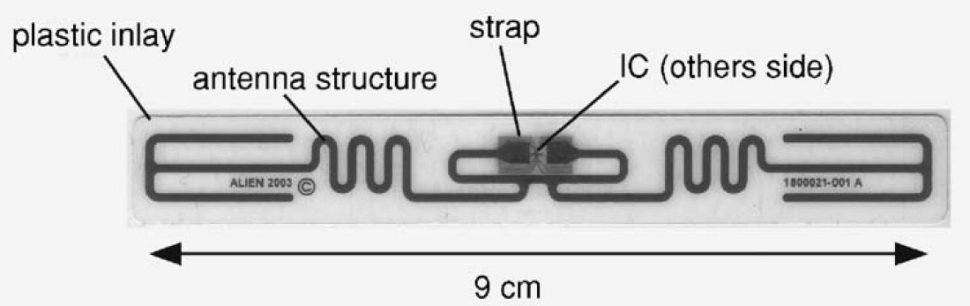


Figure 4.3 A typical commercial passive UHF RFID tag (Alien Technology model 9238 'Squiggle') [25]

Figure 4.4 shows the simplified block diagram of a typical passive UHF tag illustrating power management, RF front end, and baseband processing components. A typical passive RFID tag harvests RF power by rectifying the received RF signal into a DC voltage with a multi-stage rectifier. This DC voltage is regulated to a stable power supply by the regulator, followed with large storage capacitors to store energy and reduce supply level fluctuation. Inspecting RFID chip layouts usually indicates that these functions take up 25% or more of the chip area. Therefore, passive RFID tags fit the candidate criteria to show how RF-only logic can be used to reduce chip area and cost by eliminating the AC-DC rectifier and storage capacitors.

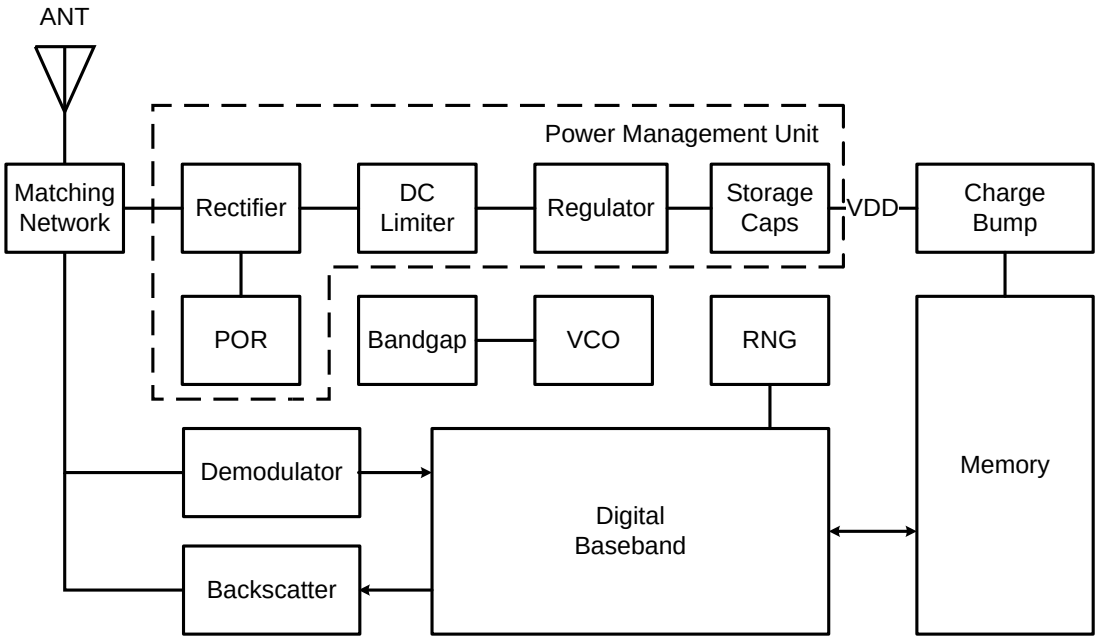


Figure 4.4 Block diagram of a typical passive UHF RFID transponder

4.2 UHF Gen-2 Protocol

Similar to all the other communication technologies, a RFID system has its communication protocols that define data link layer and physical layer operations. This work targets at the EPC UHF Class-1 Generation-2 protocol, which is the most widely used one for RFID. The UHF Gen-2 is a half-duplex, interrogator-talks-first communication protocol for a RFID system operating in the 860MHz – 960MHz ISM (industrial, scientific and medical) frequency band. In this section, the Gen-2 protocol is briefly introduced focusing on the powering, encoding, and modulation aspects.

4.2.1 Interrogator-to-Tag (forward link) Communication

An interrogator communicates with a tag by modulating the RF carrier using ASK with pulse-interval encoding (PIE). The forward link PIE symbols are shown in Figure 4.5. *T*ari is the duration of a data-0, which is in the range of 6.25μs - 25μs. Therefore, the forward link supports data rate ranges from 40kbps to 160kbps. The conventional approach to demodulating an ASK signal is to compare the RF carrier's envelope with its mean.

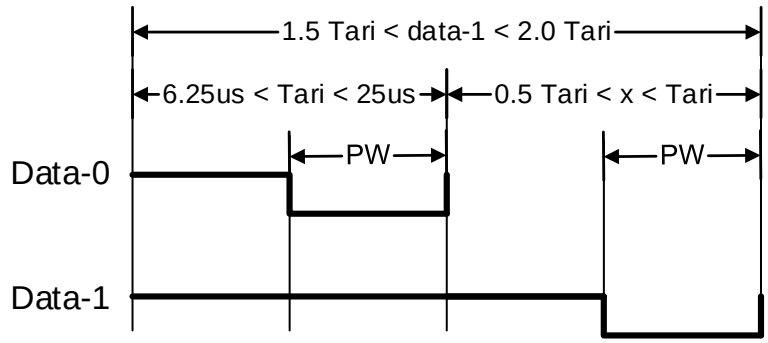


Figure 4.5 Forward link PIE symbols [26]

4.2.2 Tag-to-Interrogator (reverse link) Communication

A tag communicates with an interrogator using backscatter ASK and PSK modulation. Tags encode the backscattered data as either FM0 baseband or Miller modulation of a subcarrier at the data rate. The detailed discussion of these two encoding schemes can be found in [26]. Reverse link supports data rate ranges from 40kbps to 640kbps.

4.2.3 Powering and RF Envelope

Tags harvest energy from the modulated forward link carrier. This ASK modulated carrier features a nominal modulation depth of 90% and a power-up rise time of 1μs-500μs. In typical implementation, an AC-DC power rectifier rectifies the incoming RF carrier into a stable DC power supply, which charges up the storage capacitor as an energy reservoir. During the attenuated periods of the ASK modulated carrier, the storage capacitor operates as the power supply. Thus, the local circuitry is continuously operating with a stable DC power supply.

4.3 System Design

Figure 4.6 illustrates the system block diagram of the proposed rectifier-free UHF Gen-2 compliant RFID tag. It integrates a power and timing management unit, communication blocks, and the digital baseband. The induced differential RF voltages (the RF carrier) are clamped by the AC limiter to generate the constant amplitude differential RF supply signals, which are used to power the rest of the chip. An on-chip ring oscillator generates the global clock for digital baseband. The power level detecting circuit detects the power level transitions of the ASK modulated RF carrier, which triggers the baseband operations to pause or resume accordingly. Read-only memory was implemented due to the lack of RF-only non-volatile memory. The reserved and EPC memory banks were hardwired with pre-defined values. Fully custom designed blocks include the standard cells for digital baseband, power

and timing management unit, and the backscatter circuits. The baseband logic and the demodulating block were designed in a fully automated digital design flow which also incorporated PST sharing algorithm. The powering and communication schemes for a direct RF-powered implementation are discussed in this section. The digital implementation and custom designed peripheral blocks are presented in the following sections.

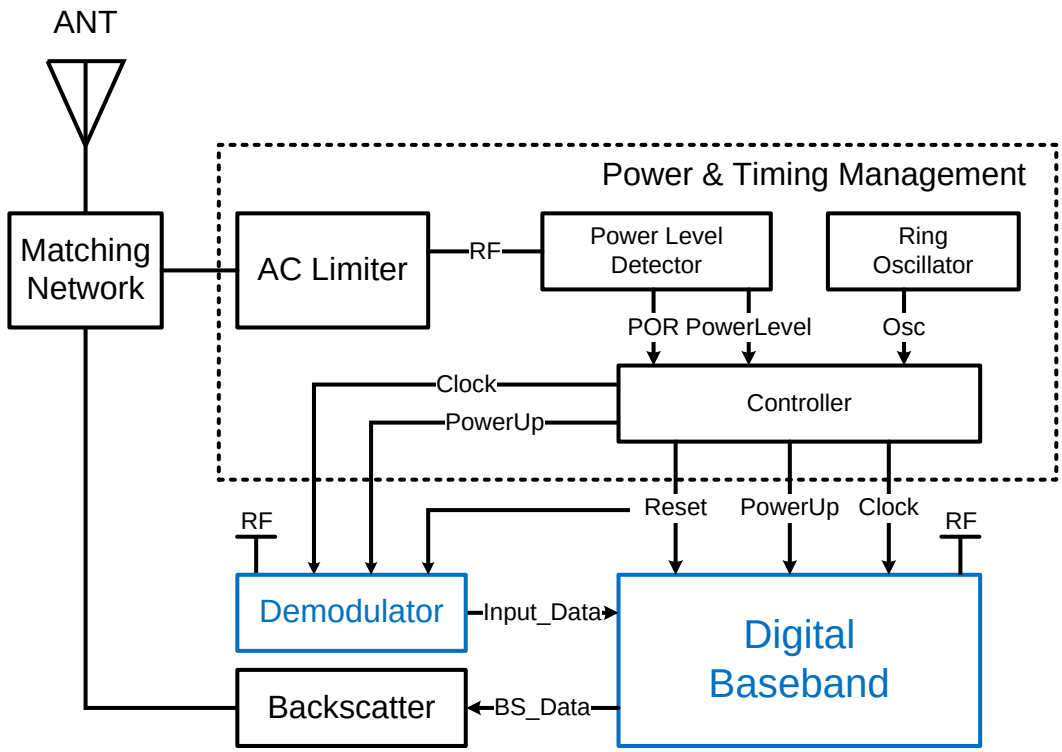


Figure 4.6 System block diagram of the proposed UHF Gen-2 compatible RFID tag

4.3.1 Powering Scheme

A Gen-2 interrogator sends data to a tag by modulating the RF carrier using ASK. A tag harvests the operating energy from this same modulated RF carrier. The amplitude of the received RF carrier fluctuates due to changes in distance and ASK modulation. For RF-only logic based implementation, the amplitude of RF power supply needs to be stable since the performance of RF-only logics is a function of the RF amplitude. Two schemes are proposed to tackle the RF supply fluctuation. First, an AC limiter is deployed at the front end of the tag to clamp the RF amplitude in ASK high periods to the pre-defined level. It is 500mV in this design. It also sets the minimum power level the RFID tag can operate.

The nominal ASK modulation depth in Gen-2 protocol is 90%. The power management unit in a conventional RFID tag generates a constant DC power during the entire inventory round by storing energy on capacitors. Due to the lack of energy storage mechanism, the RF-only logic based design cannot operate during ASK low periods. Therefore, the second powering scheme is to pause circuit operation during ASK low periods. Figure 4.7 illustrates the proposed powering scheme to manage this interruption. During the ASK high periods, the logic circuit operates as normal. During the ASK low periods, the logic circuit ceases operation while the state information is preserved in the flip-flops. These flip-flops are custom-designed data-retention flip-flops that can hold their state for at least 12.5 μs without power, which is the maximum length of ASK low period defined in Gen-2 protocol. An RF-only based power level detection circuit monitors the RF level transitions in ASK modulation. During a high-to-low transition, the clock signal is set to high, therefore prevents the state value in data-retention flip-flops from being contaminated by any unintentional

latching. During a low-to-high transition, the clock is not resumed until the state values in data-retention flip-flops are restored to CMOS logic level and propagate through the entire logic paths. Overall, the baseband logic operates as if there are no ASK low periods. Upon the initial power on of the RFID tag, an active-low power-on-reset (POR) signal is generated to reset all the flip-flops. The POR signal does not respond to the power level changes due to ASK modulation.

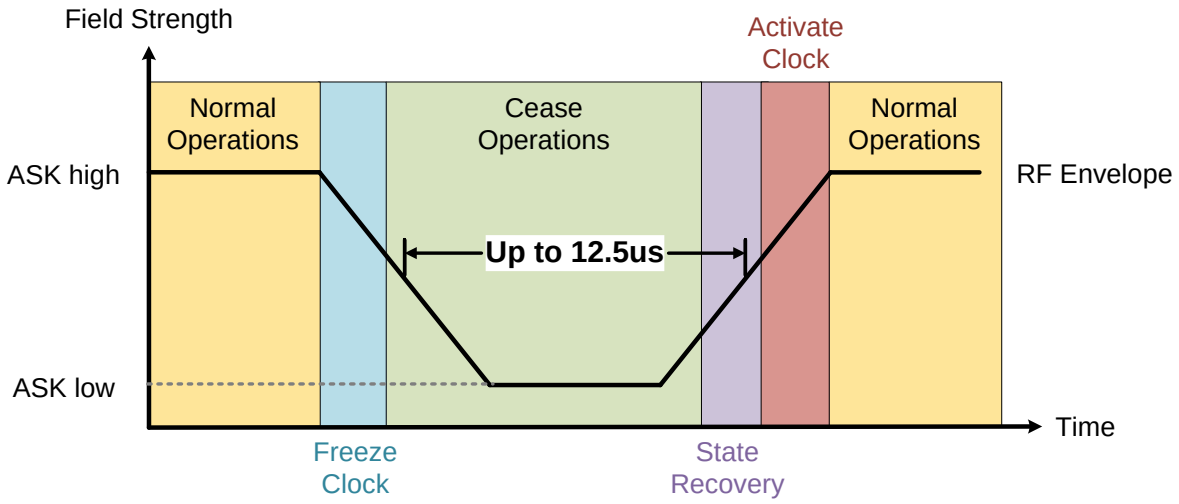


Figure 4.7 RF carrier envelope of Gen-2 forward link ASK modulation with proposed powering scheme annotated

The body terminal of a MOS device needs to be properly biased to prevent leakage current. In classic CMOS circuit implementation, the PMOS body is often connected to the highest voltage on chip (VDD) and the NMOS body is connected to the lowest voltage on

chip (VSS). In RF-only logic design, two DC biasing voltages are generated from the RF source using a peak detection circuit to bias the body terminals of MOS devices properly.

4.3.2 Communication Scheme

An interrogator communicates with a tag by ASK modulation of the RF carrier. In the conventional rectifier-based approach, an ASK modulated signal is demodulated by comparing its envelope and the mean. The conventional envelope detecting technique cannot be implemented during ASK low periods without an energy storage mechanism and power supply. However, the PIE used in Gen-2 forward link indicates that all the useful information is encoded as the length of the ASK high periods, as illustrated in Figure 4.5. Therefore, a fully digital approach that counts the duration of each ASK high period is deployed for the forward link demodulation. The demodulation block consists of a finite state machine (FSM) and several pulse interval counters that are driven by the global 4MHz clock. An inverter chain based ring oscillator is designed as the 4MHz clock source. The power-up signal generated by power level detector is used as the enabling signal for updating the FSM.

A Gen-2 compatible RFID tag talks back to the interrogator by backscattering an unmodulated RF carrier: modulating the loading impedance of antenna thus modulating the incident power. Phase modulation by changing the input capacitance is used in this design since it maintains a constant RF amplitude for robust circuit operations.

4.3.3 Critical Global Signals

To implement the powering and communication schemes discussed above, three global signals that drive the baseband logic are generated from the power and timing management unit. They are:

- **Reset**: global power-on-reset signal that resets all the flip-flops in FSMs and data path. It is active “low” for the the initial power up and kept “high” during the entire inventory round.
- **Clock**: global 4MHz clock that synchronizes all the digital baseband logic. It is kept logic “high” during power level transition periods to avoid potential malfunction.
- **PowerUp**: enable signal for demodulator FSM updating that is active for one clock cycle at the beginning of each ASK high period, which indicates a new round of ASK high period.

The waveforms of these three signals in the initial power on and ASK modulation power-up scenarios are plotted in Figure 4.8 and Figure 4.9, respectively. Notice the only difference between these two scenarios is the logic level of “Reset” signal. The details of the generation of these signals are discussed in section 4.5.

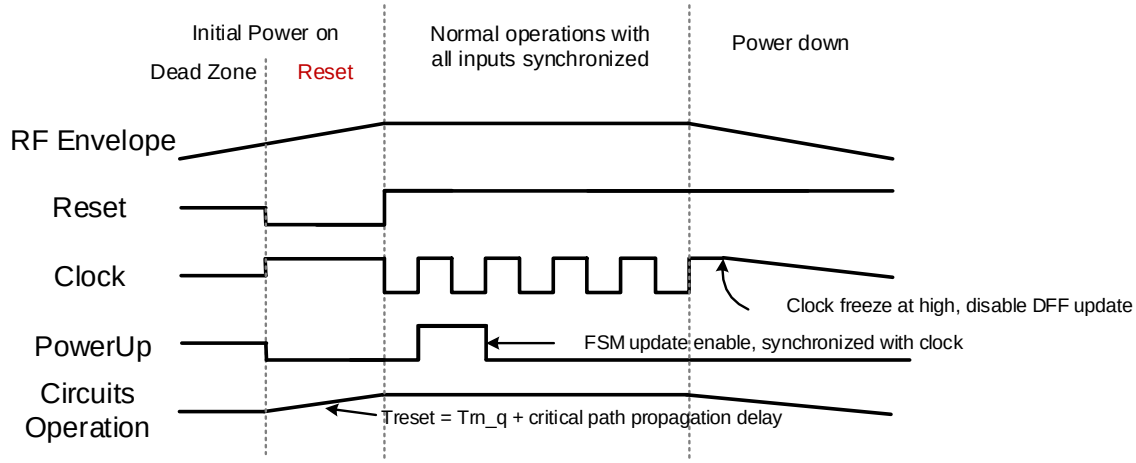


Figure 4.8 Waveform of RFID initial power up and down. Reset and DFF output hold during ASK low

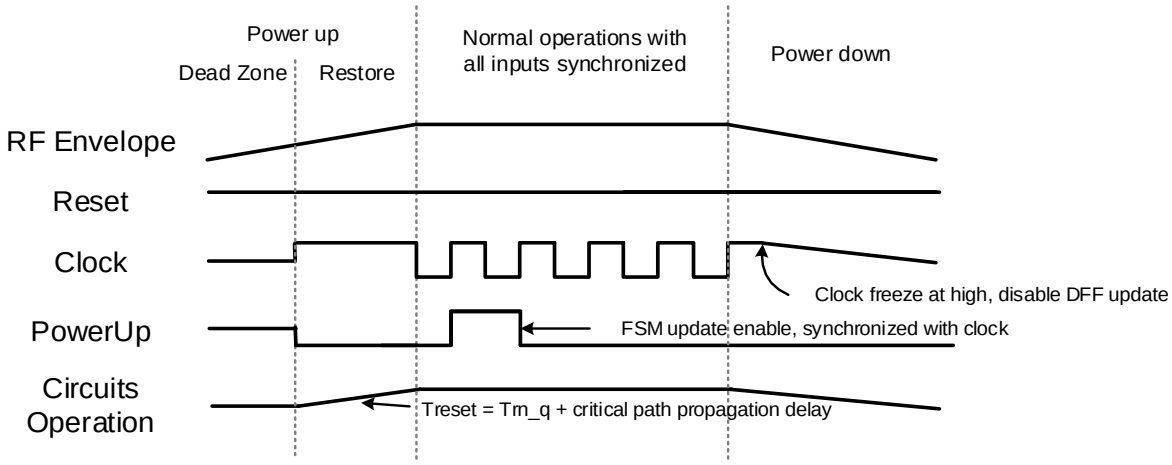


Figure 4.9 Waveforms of RFID power on and off during ASK modulation

4.4 Digital Implementation

Figure 4.10 shows the fully automated digital design flow for RF-only logic. The RTL design is synthesized to a dedicated standard cell library for RF-only logic. To facilitate PST sharing, core logic gates and PST were developed as separate cells. The post-synthesis gate level netlist only contains the core logic cells. PST cells are inserted by performing the PST sharing algorithm on the post-synthesis netlist. The resulting netlist is ready for back-end physical design. The key innovations in digital implementation are the development of the first standard cell library for RF-only logic and incorporating PST insertion into the digital design flow. This section focuses on the discussion of these two parts.

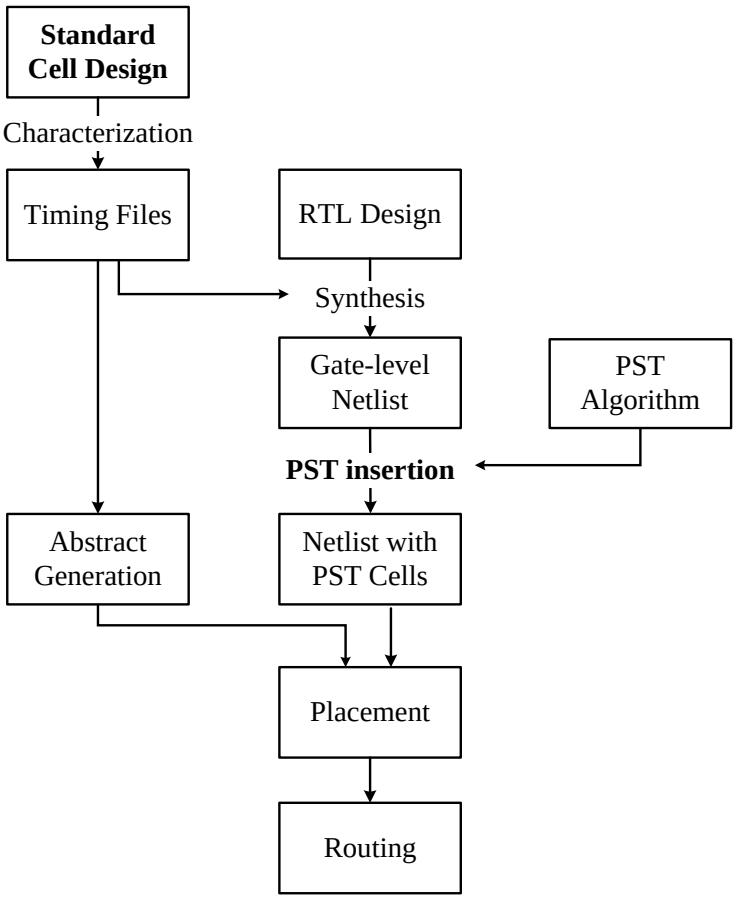


Figure 4.10 Digital design flow for RF-only logic

4.4.1 Standard Cell Library Development

A basic standard cell library for the single-phase RF-only logic family was developed for IBM 0.13µm CMOS technology. It includes three logic gates (INV, NOR2, NAND2), one PST cell, two data-retention flip-flops, buffers, and filler cells. The standard cell of each logic gate only contains the core logic parts, and the PST is implemented as a separate cell to facilitate the PST sharing step. Standard cell characterization was conducted in Cadence Virtuoso using custom-designed test bench and ocean scripts. The resulting timing information was used in the logic synthesis and physical design.

a. Sizing strategy

The core logic and PST cells in RF-only standard cell library were minimum sized to save area while maintaining certain level of performance. The PMOS/NMOS width ratio of each cell was optimized to achieve a balanced driving strength for both pull up and pull down networks. Several progressively sized buffers were also developed to be inserted during physical design for driving large loads. Larger driving strength was achieved by sizing up the core logic and PST at the same ratio. Buffers and flip-flop cells have their own power supply transistors, therefore, do not participate in the PST sharing process. Table 4.1 summarizes the standard cells and their transistor sizing.

Table 4.1 List of standard cells and corresponding transistor width

Cells	**PST**	**INV**	**NOR2**	**NAND2**	**DFFR**	**DFFS**	**BUFFER**	**Fill**
PMOS (µm)	0.4	0.4	0.8	0.4	NA	NA	NA	NA
NMOS (µm)	0.16	0.16	0.16	0.32	NA	NA	NA	NA

b. Structure and layout

Since standard cell of each logic gate only contains the core logic part, the transistor connection is identical to their CMOS counterparts with pin locations being the only difference. Figure 4.11 shows the schematic and layout of the RF-only inverter cell. It has two signal pins A and Y, two virtual power pins V_p and V_n, and two global body biasing pins V_{biasp} and V_{biasn}. In contrast, a typical CMOS inverter only has two global power pins VDD and VSS which are also used as body biasing for the transistors. The layout of RF-only inverter is shown in Figure 4.11(b). To minimize the potential routing congestion caused by the two extra virtual power pins, two dedicated routing channels were allocated for them. The two global body biasing nets were placed at the top and bottom of standard cell routed with Metal M1, whereas the two virtual power pins were treated as regular signal pins by the routing tool.

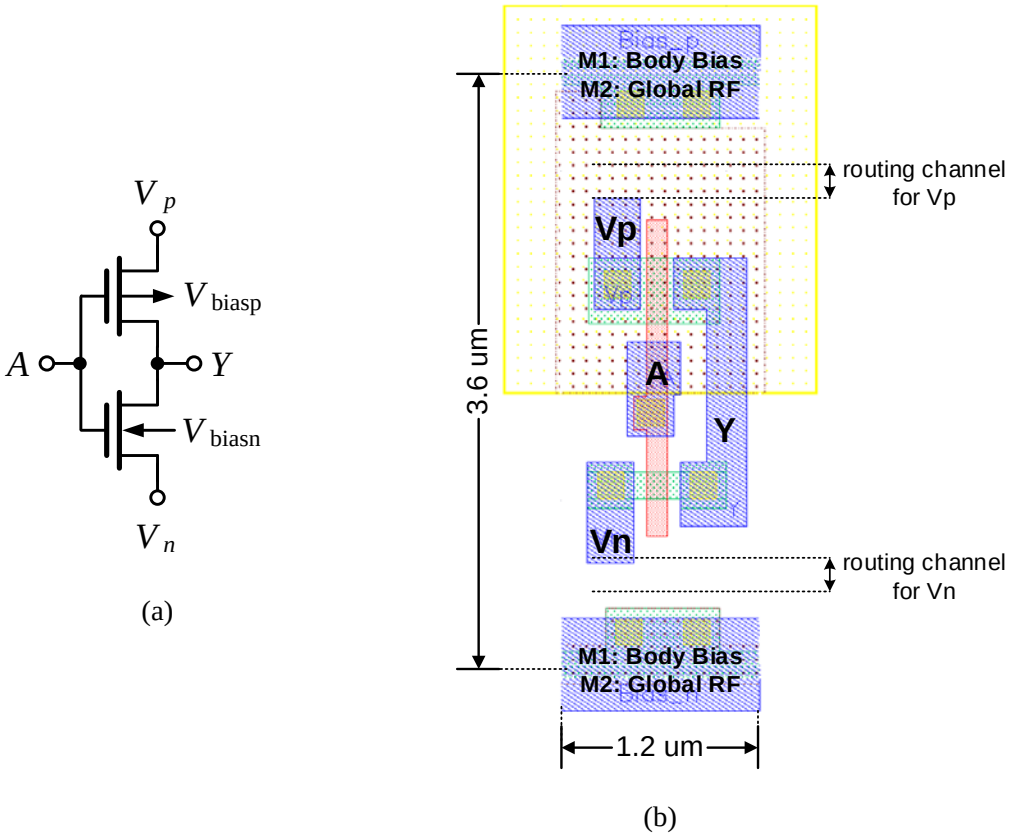


Figure 4.11 RF-only inverter (a) core logic schematic (b) core logic layout

The two power supply transistors were implemented as a separate standard cell. Figure 4.12 shows the schematic and layout of a PST cell. There is no data pin in the PST cell. Instead, it has two global power supply pins V_{RF+} and V_{RF-}. Its layout was designed in the same height of other logic cells to fit them in the same grid. To minimize the area overhead, the two global power nets V_{RF+} and V_{RF-} were routed with Metal M2 right on top of the body biasing nets. Note that V_{RF+} and V_{RF-} nets exist in core logic cells as well so that the global nets are connected automatically by abutting the cells. A summary of the common nets in

each standard cell is listed in Table 4.2. The physical specification of standard cell layout design is listed in Table 4.3.

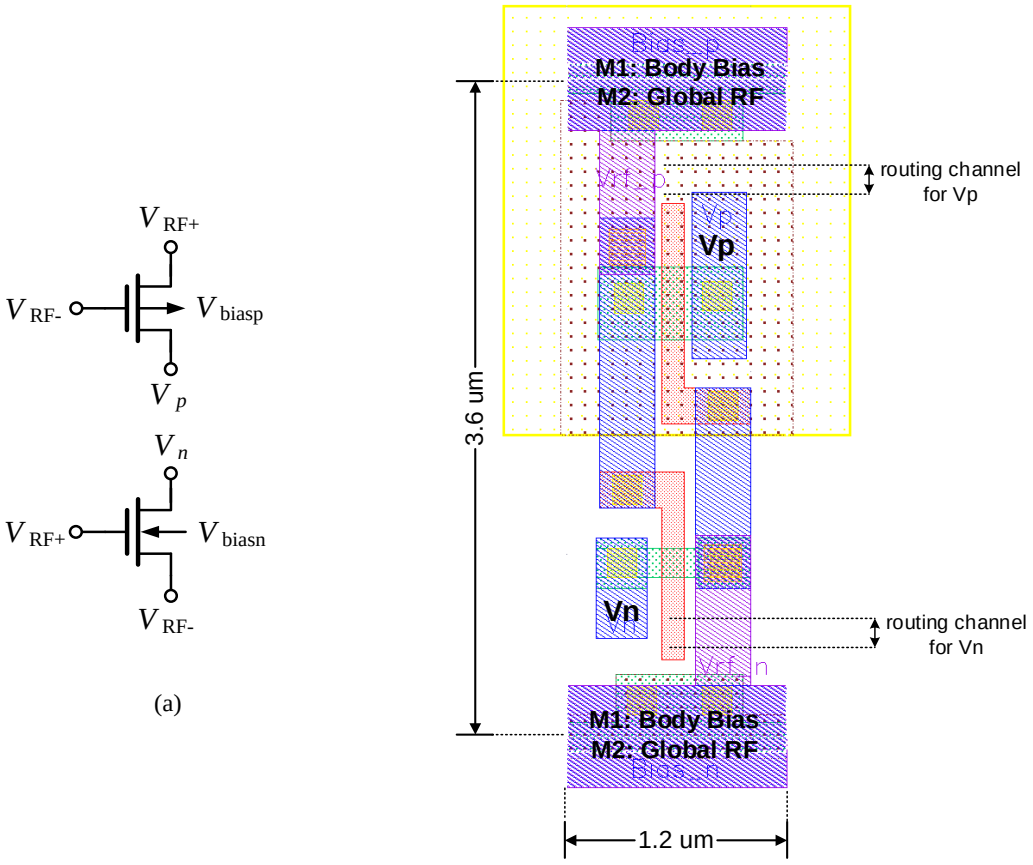


Figure 4.12 PST cell (a) PST schematic (b) PST layout

Table 4.2 Common nets in RF-only standard cells

	Global Nets		Local Nets
Net Name	V_{RF+}/V_{RF-}	V_{biasp}/V_{biasn}	V_p/V_n
Signal	differential RF supply	body biasing	Virtual power supply
Metal Layer	M2	M1	M1
Net Routing	Self-aligned along standard cell array		Routed as signal nets

Table 4.3 Physical specifications for RF-only standard cell library

Drawn Gate Length (μm)	0.12
Layers of Metal (MA last metal option)	8 (3-2-3)
Layout Grid (μm)	0.01
V_p and V_n Rail Width (μm)	0.16 (Metal M1)
Body Biasing Signal Rail Width (μm)	0.36 (Metal M1)
Global RF Power Rail Width (μm)	0.56 (Metal M2)
Cell Height (μm)	3.6

c. Characterization and PST insertion

The timing and power information of each logic cell were characterized. The characterization results were written in liberty files (.lib) for logic synthesis. The characterization was conducted in a standard scenario, and each logic cell was exclusively powered by one PST cell. The mutual exclusive sharing algorithm ensures the cell performance does not degrade from the characterized value since no two of the logic cells would charge current through the same PST cell simultaneously. The standard cells were characterized for a nominal RF supply of 900MHz and 500mV amplitude. Table 4.4 lists the corner conditions for characterization.

Table 4.4 Electrical specifications for RF-only standard cell library

Corner	RF Amplitude A_{RF}	Temperature	RF Frequency
typical-typical	0.5V	25ºC	900MHz
slow-slow	0.45V	125ºC	900MHz
fast-fast	5.5V	-40 ºC	900MHz

The characterization was performed using transient simulation on post-layout parasitic-extracted netlist. Figure 4.13 shows the simulation setup for characterization of the RF-only inverter. The transition time of input square wave and output loading capacitance are the primary parameters of interest. Dynamic power consumption and propagation delay were characterized in a two-dimensional space as listed in Table 4.5.

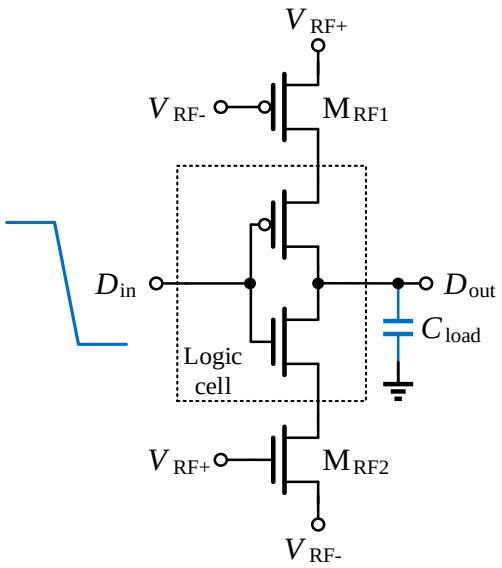


Figure 4.13 Characterization bench of RF-only logic cells

Table 4.5 Parameter range for characterization

Input transition (ns)	0.1	0.2	0.4	0.8	1.6	3.2	6.4
Output load (fF)	0.79	2.054	4.74	10.112	20.856	42.186	85.32

A sample transient simulation waveform of the RF-only inverter is shown in Figure 4.14. The input signal swing is set as V_{OH} to -V_{OH}. The propagation delay t_p is defined as the time interval between the input crossing 50% of full swing and the output crossing 50% of full

swing. The transition time is defined as the time interval between output crossing 10% of full swing and 90% of full swing. Note that the full swing (V_{OH} to $-V_{OH}$) here is roughly 400mV to -400mV. The dynamic power consumption is also defined as the power dissipated during the transition time. The input logic switch was set to start right before the evaluation phase when $V_{RF+} = V_{RF-}$. As discussed in Chapter 2, the propagation delay of RF-only logic is a function of the logic switching phase, and there might be a maximum delay penalty of $T_{RF}/2$ associate with it. In contrast, dynamic power consumption is not impacted by the switching phase. PST sharing may reduce the propagation delay of the logic cells due to charge sharing during storage phase. It potentially leads to hold violation as the gates are running faster with PST sharing than when they were characterized. In this particular implementation, the potential hold violation is eliminated by using master-slave flip-flops. In most cases, conventional master-slave structures have negative hold time and thereby immune to hold violation [27].

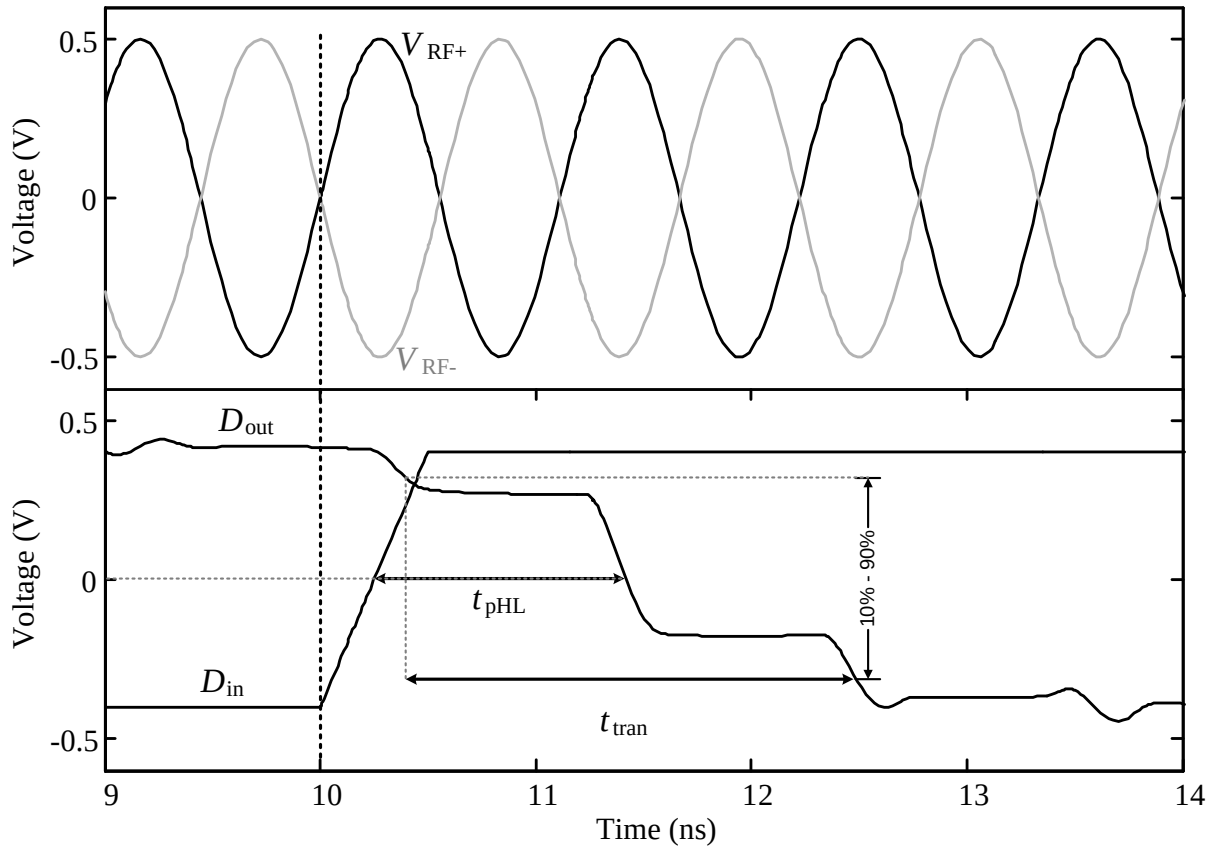


Figure 4.14 Transient simulation waveform of RF-only inverter cell with timing characteristics annotated

d. Data-retention flip-flop design

A data-retention flip-flop in RF-only style is designed to meet the UHF Gen-2 protocol requirements. The flip-flop is designed to retain state for at least 12.5μs without RF power. It is rising edge triggered and features asynchronous active low reset. Each flip-flop has its exclusive power supply transistors.

The schematic of the proposed data-retention flip-flop is presented in Figure 4.15. It is a master-slave type flip-flop in a differential configuration to enhance the driving strength. The master latch unit consists of clocked feedback inverters. Moreover, the slave latch utilizes stacked transmission gates to reduce leakage during low RF level periods. The storage circuit is designed in differential 2-T DRAM configuration to enhance driving strength and reduce leakage. The storage circuit is driving a cross-coupled sense amplifier that senses the voltage difference between the stored charges and resolves to CMOS logic level at the output during the power recovery phase.

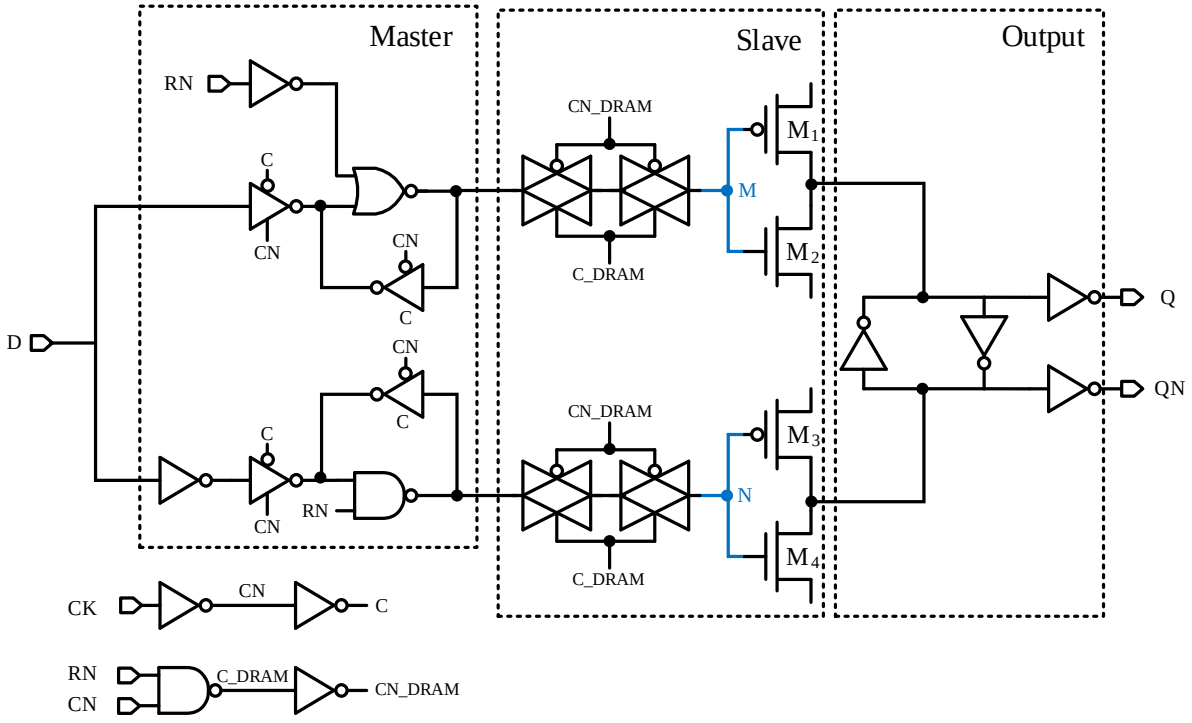


Figure 4.15 Schematic of the RF-only data-retention flip-flop

There are four operation modes of the flip-flop that correspond to four phases of the RF envelope level during the ASK modulation, as illustrated in Figure 4.16. The flip-flop operates as a conventional rising edge triggered flip-flop when the RF envelope is high and stable, which corresponds to phase I. Figure 4.17 shows a typical waveform of the data-retention flip-flop operating in phase I. In phase II when there is a high-to-low RF level transition, the clock input is kept at logic high to prevent any undesirable latching of an input signal. The previously latched logic value is stored at the gates of M_1 to M_4 during phase III when the RF envelope level is low. In phase IV when there is a low-to-high RF level transition, the stored logic value is restored to CMOS logic levels by the sense amplifier. The clock input is at logic high before the complete recovery of stored logic value. Figure 4.18 and Figure 4.19 show the simulated transient waveforms of the data-retention flip-flop operating in Phase II and Phase IV. Notice the differential voltage remained on the storage gate after a maximum power off period of 12.5μs is 50mV, which is enough for recovery in Phase IV. The flip-flop is characterized following the methodology introduced in [27].

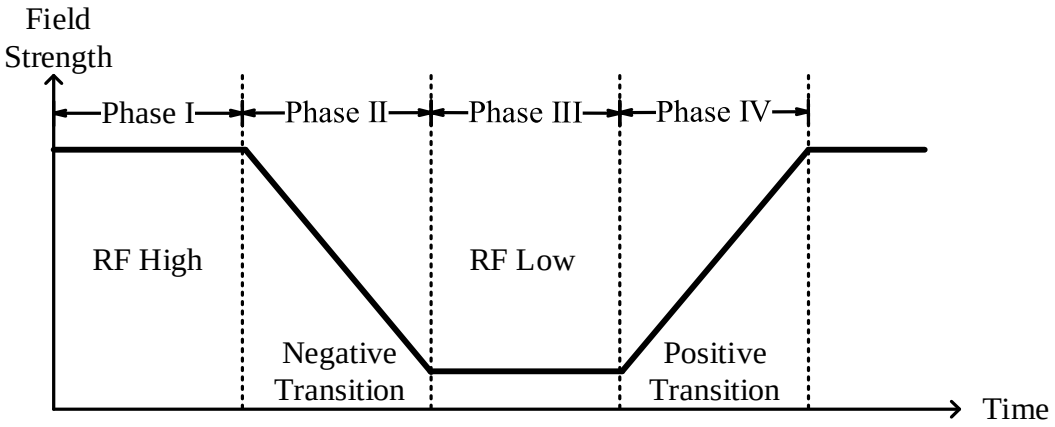


Figure 4.16 Four phases of operation for the RF-only data-retention flip-flop during ASK modulation

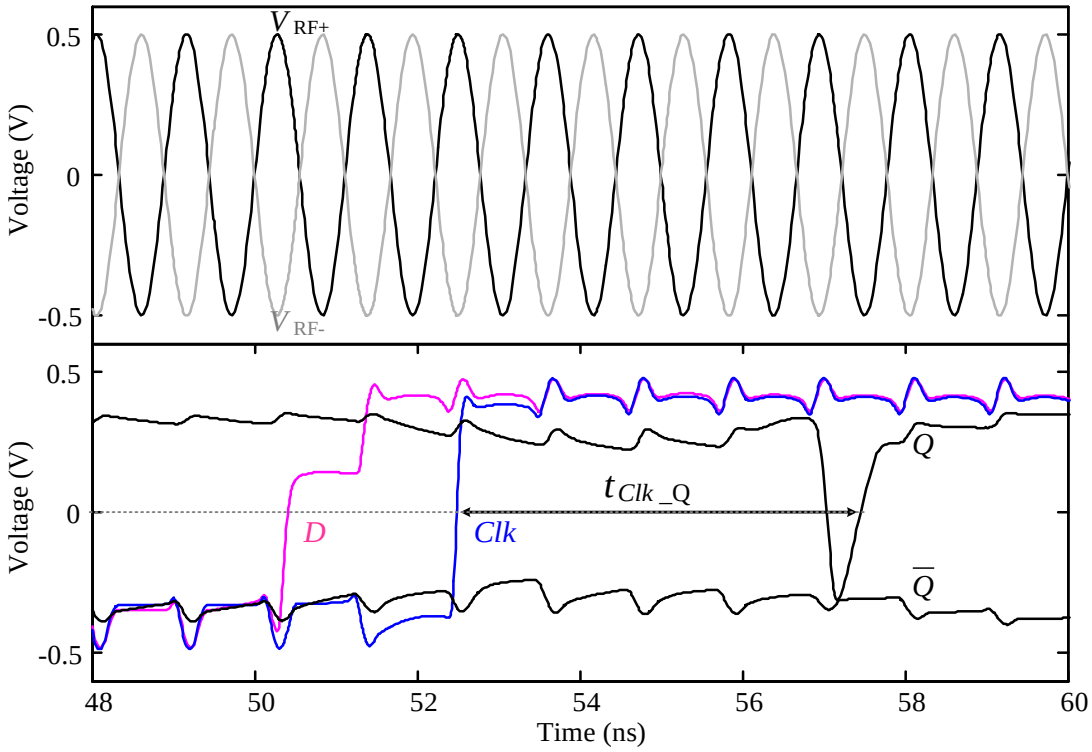


Figure 4.17 Typical data-retention flip-flop waveforms (Phase I)

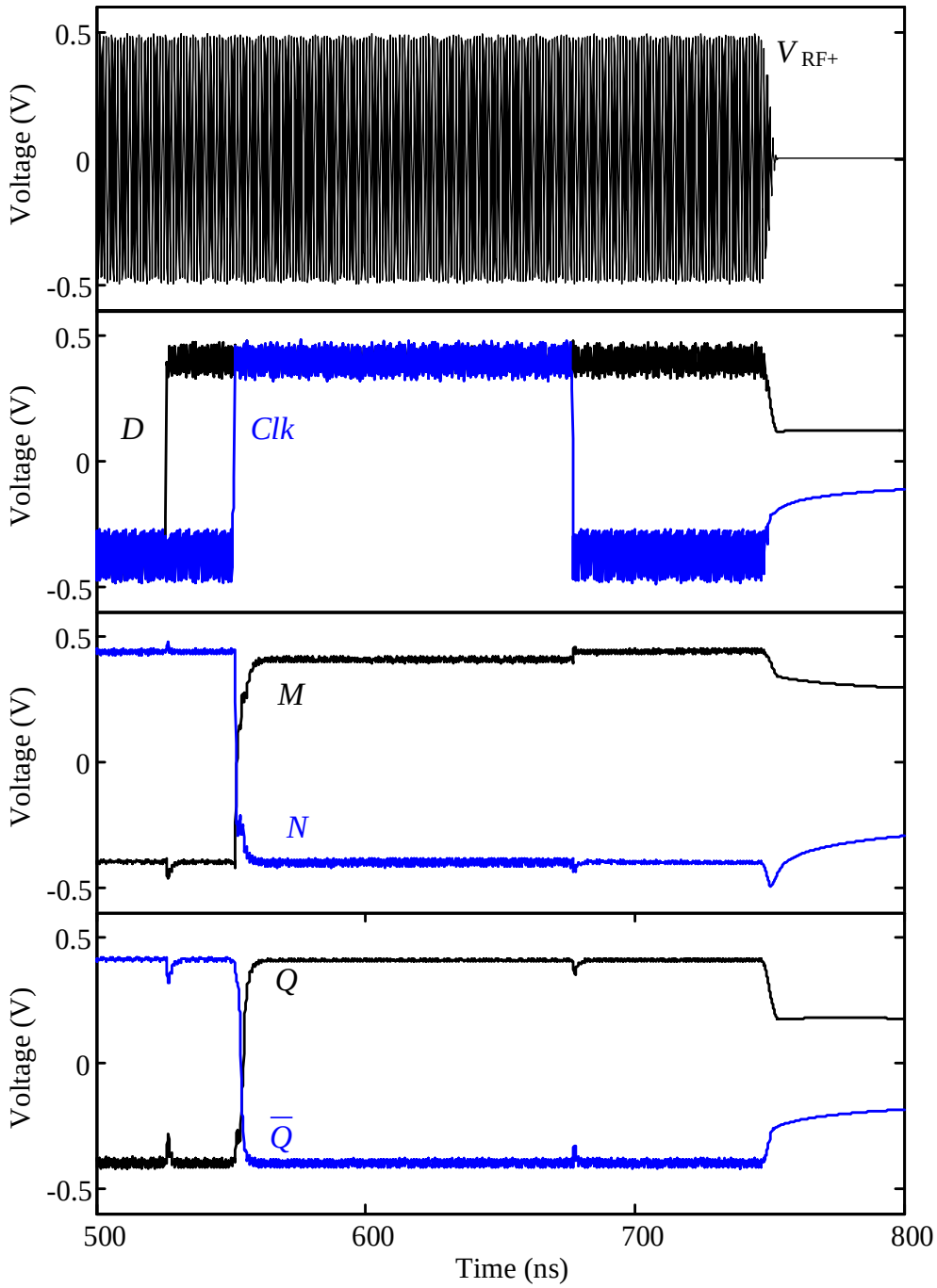


Figure 4.18 Simulated transient waveforms of data-retention flip-flop in high-to-low power level transition (Phase I and II)

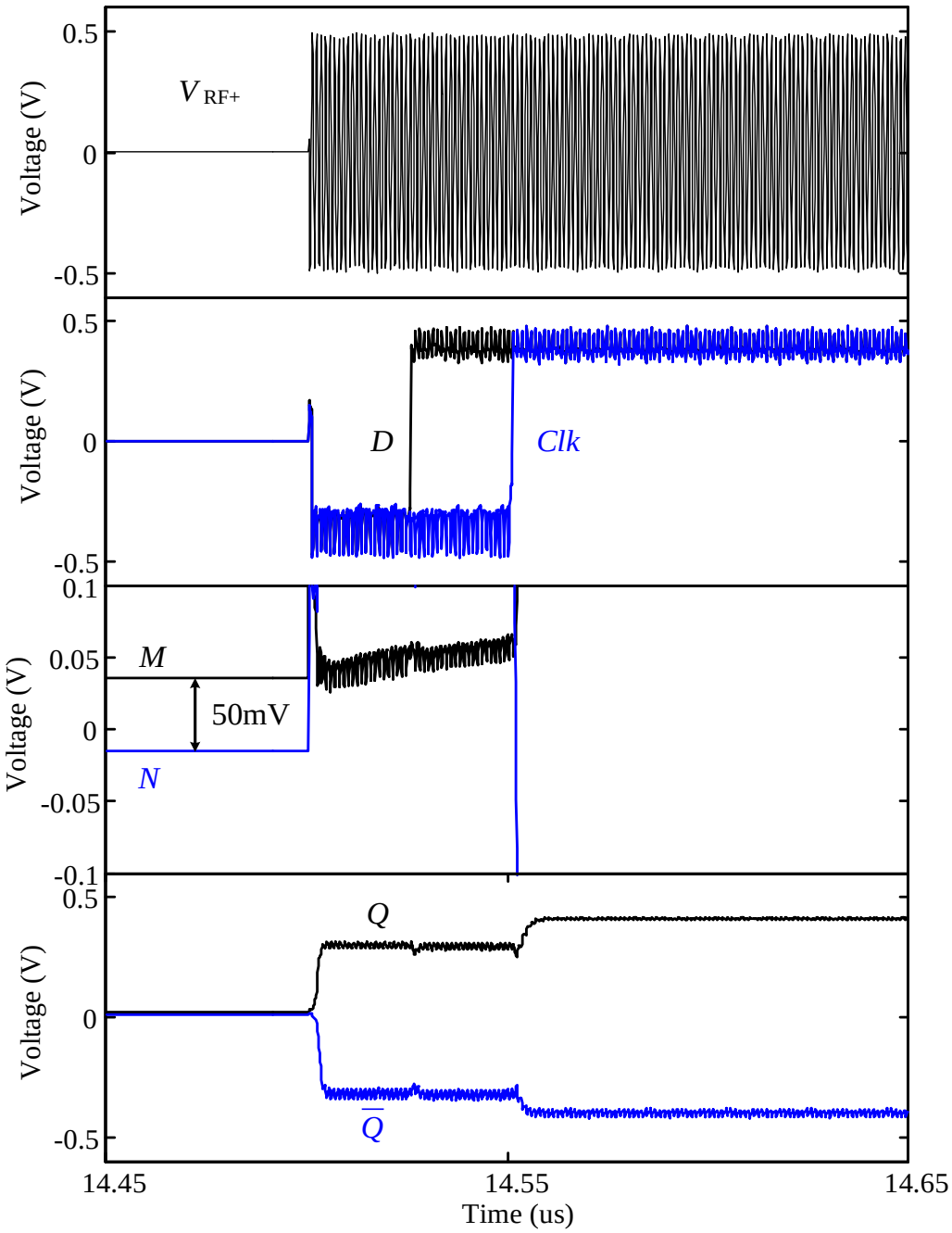


Figure 4.19 Simulated transient waveforms of data-retention flip-flop in low-to-high power level transition after power off of 12.5μs (Phase III and IV)

4.4.2 RTL Design of Gen-2 Baseband

The implementation of Gen-2 baseband protocol starts with RTL design. It includes the fully digital demodulator block. A block diagram of the Gen-2 baseband is shown in Figure 4.20. The demodulator extracts symbols from the ASK modulated RF carrier. These recovered symbols are decoded into commands. The controller executes these commands and coordinates the sequencer and encoder to properly encode the random number or memory data for reverse link communication. The digital baseband is synchronized to a global clock and employs an asynchronous reset scheme. The primary input signals driving the digital baseband are “Reset”, “Clock”, and “PowerUp”. The primary output signal is “BS_data” that drives the backscatter circuit. Figure 4.8 and Figure 4.9 show the waveforms and timing of the primary inputs. Figure 4.21 shows the waveforms of critical internal signals for digital baseband.

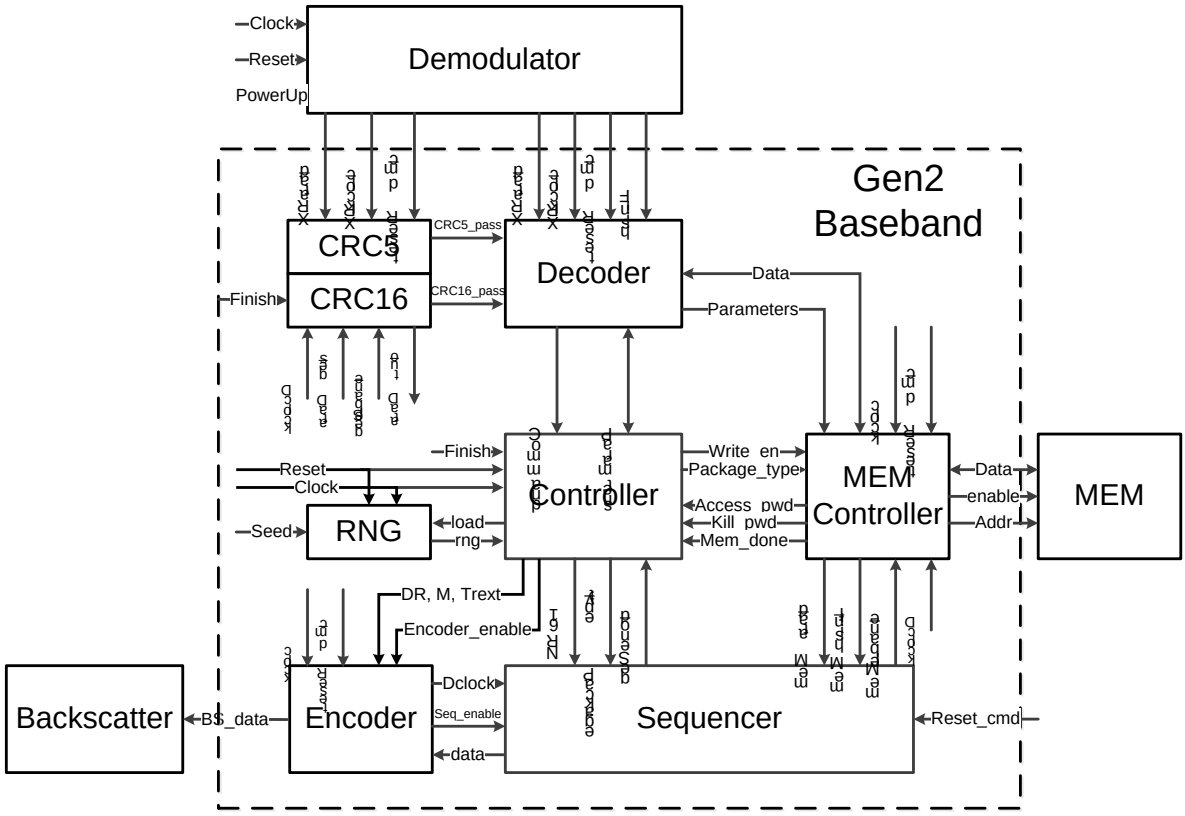


Figure 4.20 Block diagram of Gen-2 baseband design

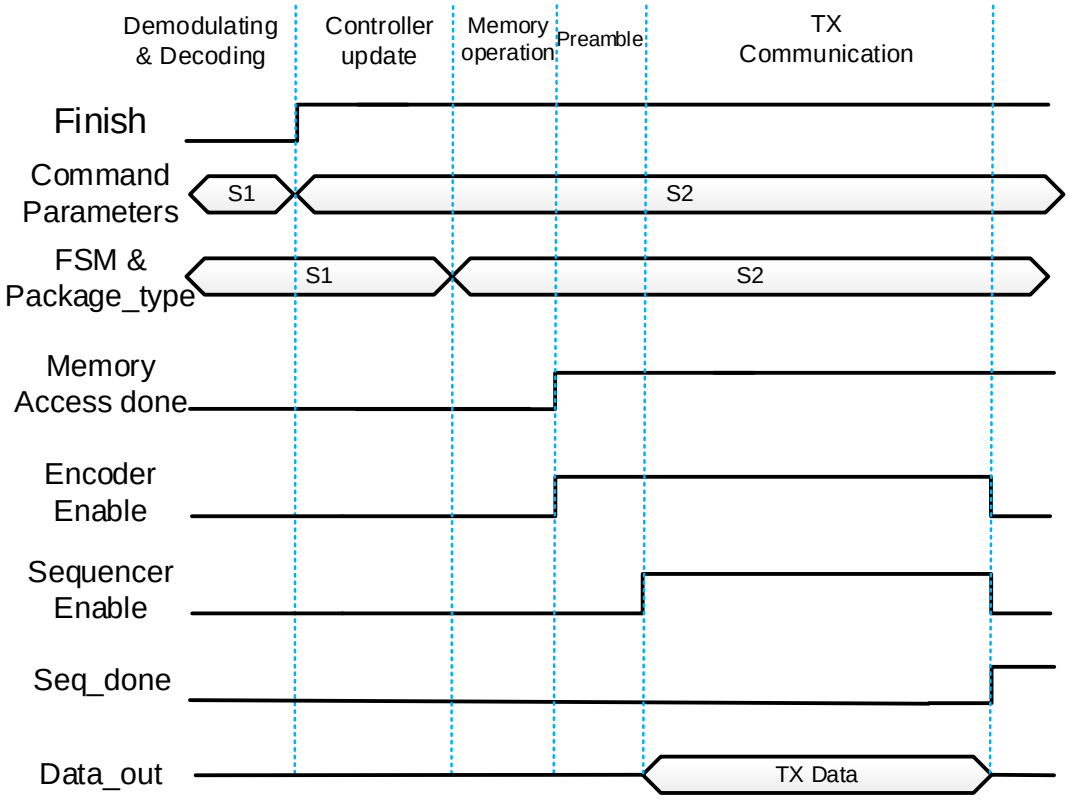


Figure 4.21 Waveforms and operation regions of critical signals in Gen-2 baseband

4.4.3 Logic Synthesis and PST Insertion

The Gen-2 baseband was first synthesized to gate level netlist using the standard cell library for RF-only logic. Before PST insertion, the gate level netlist only contained the core logic gates while the virtual power nodes V_p and V_n were not connected. A sample gate level netlist of the CRC5 module after logic synthesis is presented in Figure 4.22. The highlighted gate U30 is an instance of an inverter. Note the virtual power nodes V_p and V_n connections are not explicitly shown in the netlist before PST insertion.

```
module CRC5 ( clock, reset, RX_clock, data, CRC_pass );
  input clock, reset, RX_clock, data;
  output CRC_pass;
  wire   n20, n21, n22, n23, n24, n28, n29, n30, n31, n
         n37, n38, n39, n40, n41, n42, n43, n44, n45, n
         n51;
  wire   [4:0] CRC;

  DFFSX1TF CRC_reg_0_ ( .D(n24), .CK(clock), .SN(n29),
  DFFRX1TF CRC_reg_1_ ( .D(n23), .CK(clock), .RN(reset)
  DFFRX1TF CRC_reg_2_ ( .D(n22), .CK(clock), .RN(reset)
  DFFSX1TF CRC_reg_3_ ( .D(n21), .CK(clock), .SN(reset)
  DFFRX1TF CRC_reg_4_ ( .D(n20), .CK(clock), .RN(n29),
  INVX1TF U30 ( .A(reset), .Y(n28) );
  INVX1TF U31 ( .A(n28), .Y(n29) );
  NOR2X1TF U32 ( .A(CRC[4]), .B(CRC[3]), .Y(n31) );
```

Figure 4.22 Sample gate level netlist of CRC5 module after logic synthesis and before PST insertion

Next, PST cells were inserted to the gate level netlist based on the PST sharing algorithm that we discussed in Section 3.4. All the gates were grouped into clusters of mutual exclusive gates and PST cells were inserted for each cluster. The virtual power nets V_p and V_n were connected and explicitly shown in the resulting netlist. In Figure 4.23, the netlist with inserted PST cells is presented. As highlighted in the netlist, Gate U47, U49 and U50 are the mutual exclusive gates with U30 and they share the same PST cell P3. Notice that virtual power nets V_p and V_n of each core logic gate are created and connected to those of the corresponding PST cells. Flip-flop cells have their own PST cells therefore do not participate in the PST sharing process.

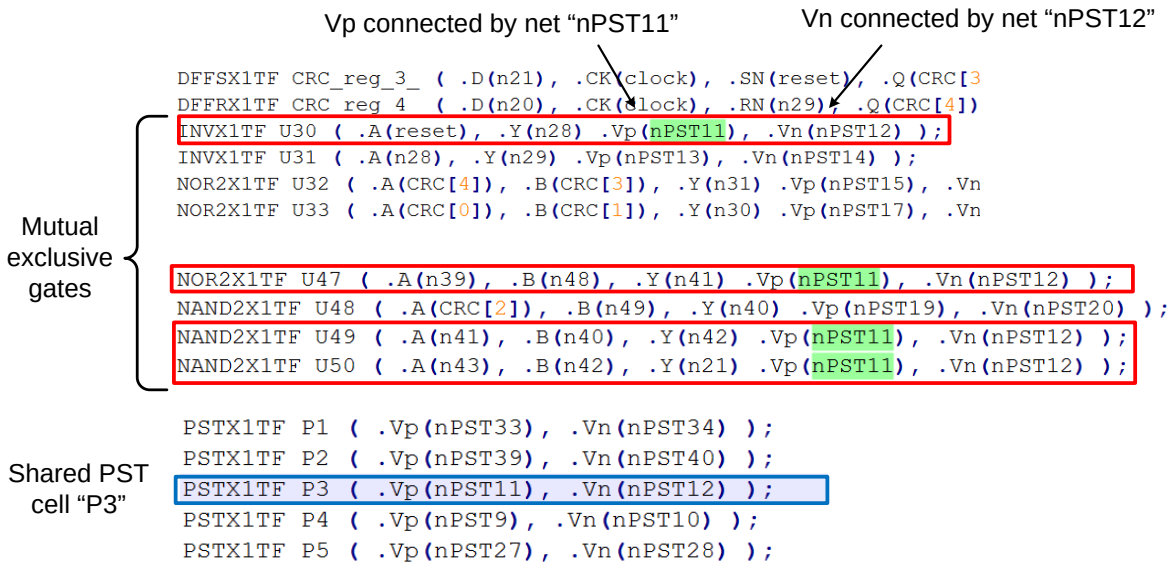


Figure 4.23 Gate-level netlist of CRC5 module after PST insertion

The logic design was synthesized with a global clock running at 4MHz and targeting at minimizing the circuit area. The setup time slack for the critical path at slow-slow corner was 125ns, which left 125ns time margin for the delay penalty introduced by the RF phase. The gate-level netlist after PST insertion was ready for back-end physical design. Table 3.2 summarizes the number of PST cells inserted for each block and the overall area overhead introduced with respective to the core logic.

4.4.4 Physical Design

Back-end physical design starts with the gate level netlist after PST insertion. The PST cells were designed the same height as core logic cells so that they can fit into the same grid. During placement, PST cells were treated as regular logic cells by the tool and placed close to their current consumers. Figure 4.24 shows a sample layout of such scheme of two logic cells (INV, NOR2) sharing one PST cell. Note that the four global nets delivering RF power and body biasing are automatically connected by abutting the cells. The virtual power supply nets V_p and V_n were treated as regular signal nets and routed by the tool automatically through the dedicated routing channels. One drawback of RF-only logic digital design is that timing analysis based on post-layout annotation is not accurate due to the non-DC powering scheme. Therefore, leaving enough time margin during logic synthesis is necessary.

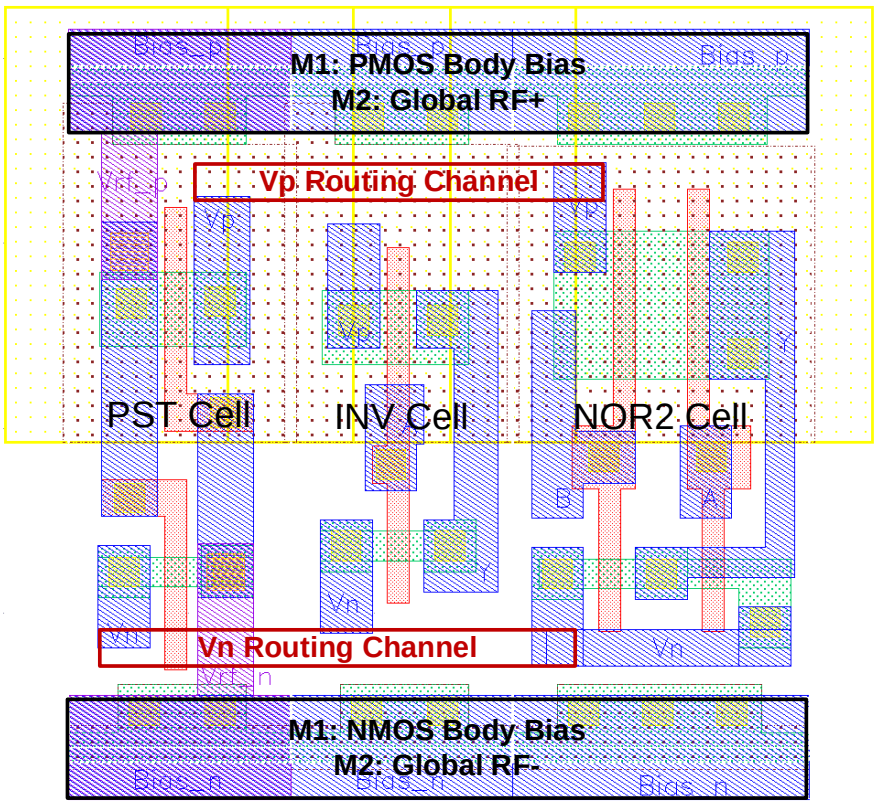


Figure 4.24 Sample RF-only standard cells placement and routing

4.5 Peripheral Circuit Design

The peripheral circuits in the proposed RFID design include a power management unit, a timing management unit, and a backscatter block as shown in Figure 4.6. The power management unit consists of an AC limiter that stabilizes the differential RF power supply and a peak detector that generates the proper bias voltages for transistor body terminals. The timing management unit consists of a power level detector, a ring oscillator, and a controller. It generates the primary input signals for the digital baseband. The backscatter block is fed with the binary data stream for reverse link communication. It modulates the antenna load impedance accordingly.

Due to the lack of accurate voltage or current reference, RF-only based analog circuit is difficult to implement. Therefore, the peripheral circuits were designed in a digital manner that performed analog-oriented functions. These blocks were custom-designed circuits instead of employing an RTL-to-GDS approach. Besides, the logic gates used in peripheral circuits were implemented without PST sharing and in a dual-phase configuration rather than the single-phase [5]. Dual-phase configuration features improved performance and noise margin at the expense of doubling the area.

4.5.1 AC Limiter

An AC voltage limiter was designed to clamp the received RF signal at a certain amplitude for robust circuit operations and preventing possible damages to the circuits due to voltage surging whenever the reader and tag are close. It also sets the minimum RF power

level that the RFID tag can operate. The AC limiter schematic is shown in Figure 4.25. The diode connected MOSFETs M_1 and M_4 define the output voltage. As the input voltage exceeds the turn-on voltage of the MOSFET, additional current is drawn from the other two legs to maintain a constant output voltage. The output RF amplitude versus the input RF amplitude is plotted in Figure 4.26. The RF amplitude is clamped within a range of 200mV for an input ranging from 0.5V to 1V.

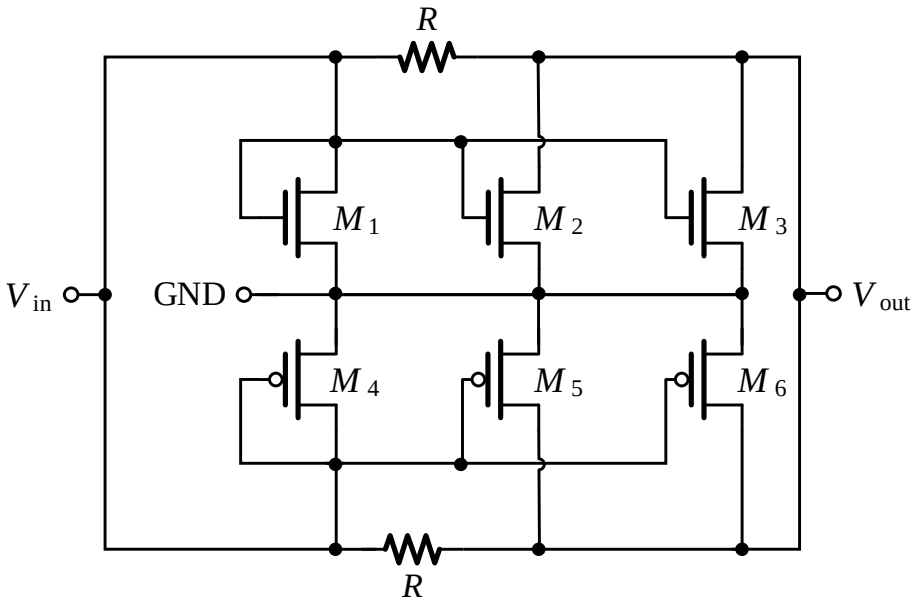


Figure 4.25 Schematic of AC limiter

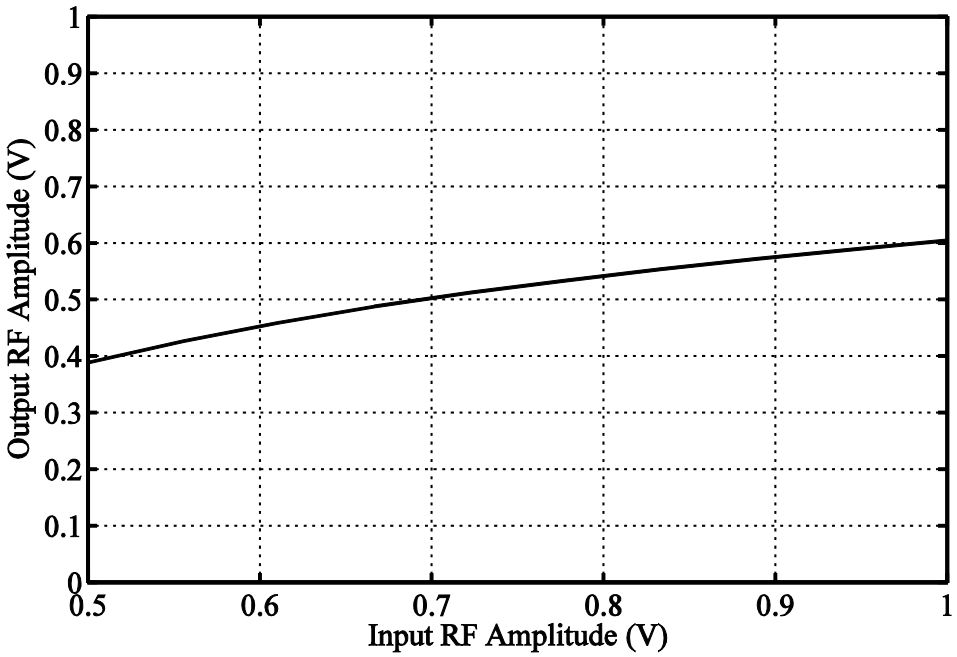


Figure 4.26 Simulated AC limiter output RF amplitude versus input RF amplitude

4.5.2 Peak Detector

A peak detector was designed to generate the biasing voltages for MOSFET body terminals. The peak detector is of cross-coupled inverters as shown in Figure 4.27. Upon power up, the cross-coupled inverters generate opposite logic levels and thereby the output of XOR gate is set to logic high. The large capacitive loading of peak detector helps to reduce the voltage ripples and maintain a stable DC voltage. Figure 4.28 shows the transient simulation results of the generated biasing voltages. Note the absolute value of the DC biasing voltage is approximately 100mV lower than the RF amplitude. As discussed in the RF-only logic operations in section 2.2.1, the steady-state output logic level V_{OH} is a function of $\omega\tau$ and is usually lower than the RF amplitude A_{RF}.

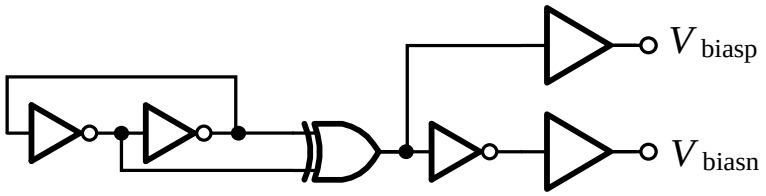


Figure 4.27 Schematic of peak detector

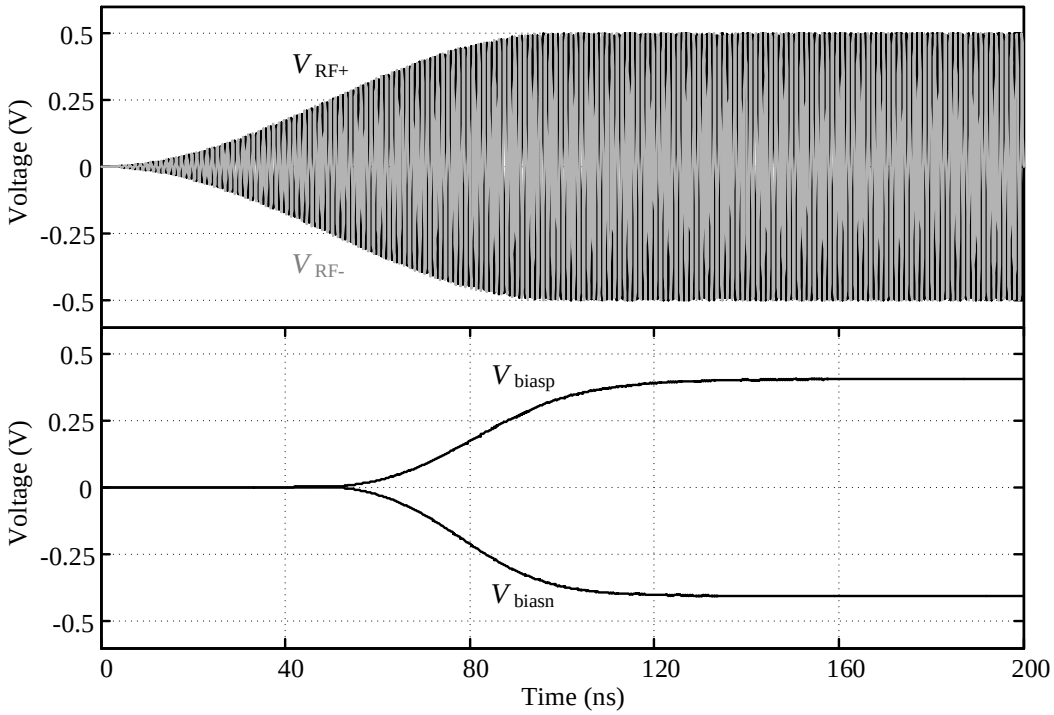


Figure 4.28 Simulated biasing voltages with a differential 900MHz RF supply

4.5.3 Power Level Detector

The power level detector was designed to detect the initial power up and power level transitions of ASK modulation. Two signals, POR (power-on-reset) and PowerLevel are generated to identify these two scenarios. These two signals are fed into controller to produce the “Reset” and “PowerUp” signals that drive the digital baseband.

Figure 4.29 shows the schematic of power level detector. Signal V_{env} tracks the RF envelope with a relatively small time constant. The diode-connected PMOS M_1 and capacitor C_{large} form a peak detector with a much larger time constant. The voltage V_{ref} on the capacitor C_{large} operates as a reference voltage for the RF carrier envelope. Therefore, the crossing points of the two signals indicate the power level transitions. V_{env} and V_{ref} are sampled and compared by cross-coupled inverters that work as a sense amplifier. The difference in voltage is then resolved to logic levels using a latch, which is clocked by a free-running on-chip oscillator at 33MHz. The simulated waveform of PowerLevel is shown in Figure 4.30. During a high-to-low power level transition, PowerLevel is set to low as soon as the faster varying V_{env} drops below V_{ref}. During a low-to-high power level transition, PowerLevel is set to high as soon as the faster varying V_{env} increases greater than V_{ref}.

The reference signal V_{ref} is fed into a threshold-tilted delay chain. The delay chain drives a diode-connected PMOS and a large capacitor to generate the POR signal. The delay chain is designed with stronger NMOS and weaker PMOS; thus the switching threshold is moved higher than the nominal level. The delay time is set to be long enough for resetting all the flip-flops. Upon initial power up, V_{ref} is at ground. It drives the POR signal to logic low as shown in Figure 4.34. As RF amplitude increasing and V_{ref} rising higher than the switching

threshold of the delay chain, POR is driven to high. During the subsequent power level transitions of ASK modulation, V_{ref} is kept high, and POR is constant at logic high. The measured POR signal is shown in Figure 4.45 and Figure 4.46.

The key specifications of the power level detector are the response time $T_{response}$ and the effective range. The effective range can cover the 1 μs to 8 μs as defined in UHF Gen-2 protocol. The corresponding response time normalized to the transition time is shown in Figure 4.31.

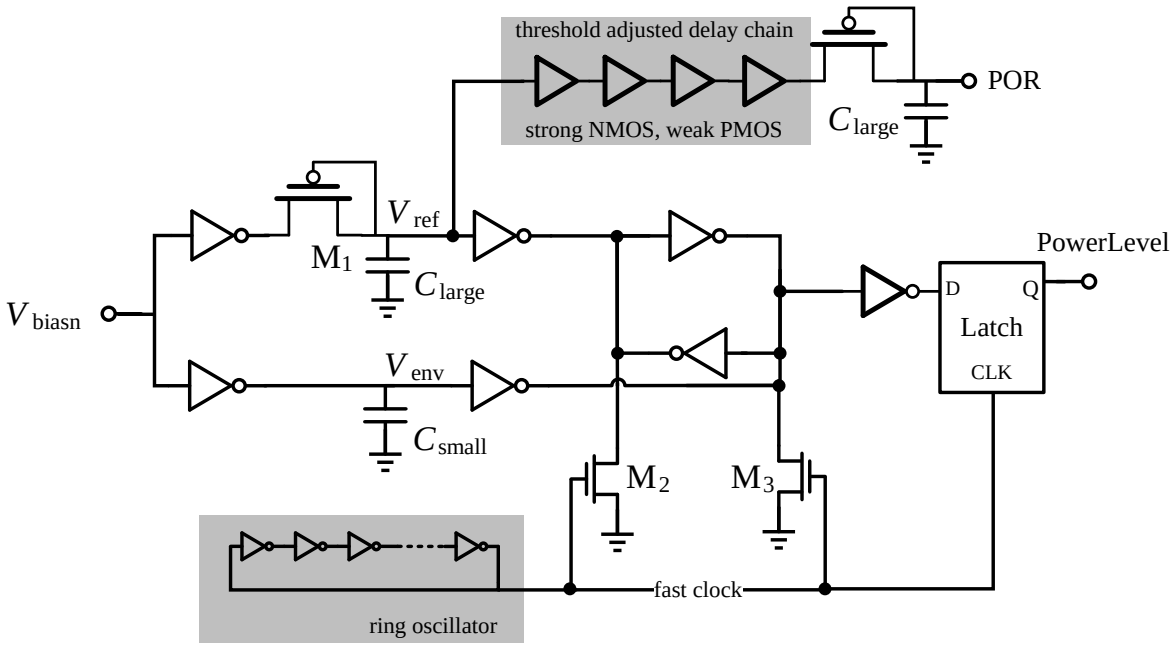


Figure 4.29 Schematic of the power level detector circuit

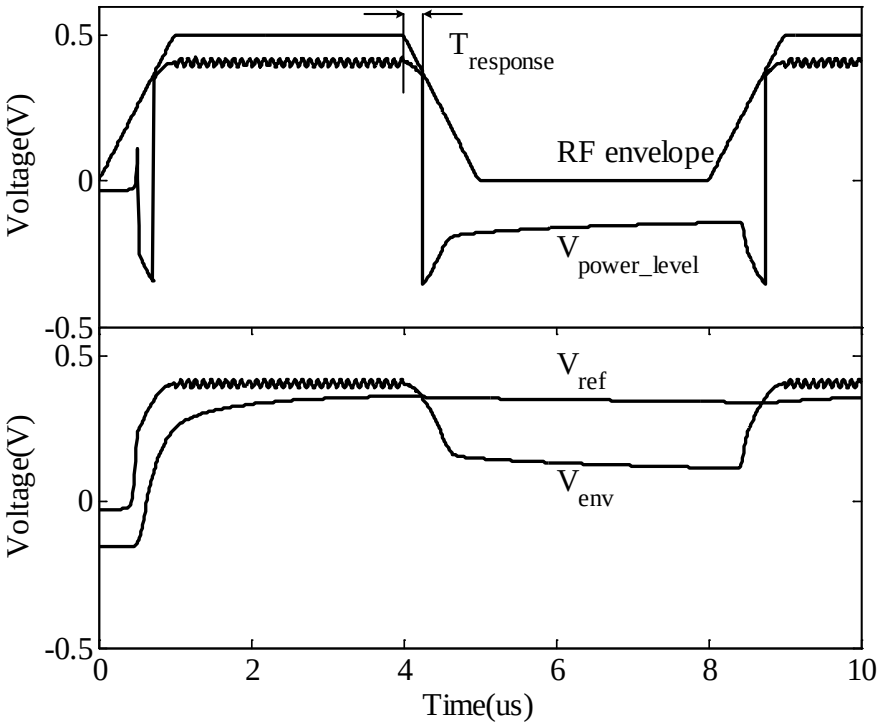


Figure 4.30 Simulated signal outputs of power level detector

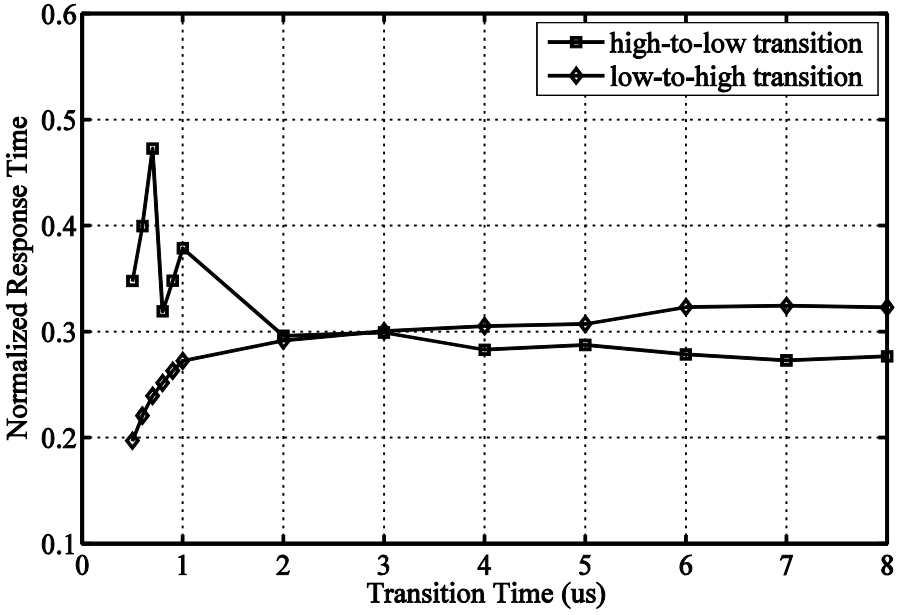


Figure 4.31 Simulated response time of power level detector

4.5.4 Ring Oscillator

A ring oscillator was designed to generate the global clock that synchronizes all the digital baseband logics. It is running at 4MHz under the nominal RF power supply. The ring oscillator consists of 31 stages dual-phase RF-only inverters as shown in Figure 4.32. To start up the oscillation at power up, switching thresholds of adjacent inverters were adjusted to opposite directions. As a result, the duty cycle of the clock signal is not 50%. The measured ring oscillator output is shown in Figure 4.44.

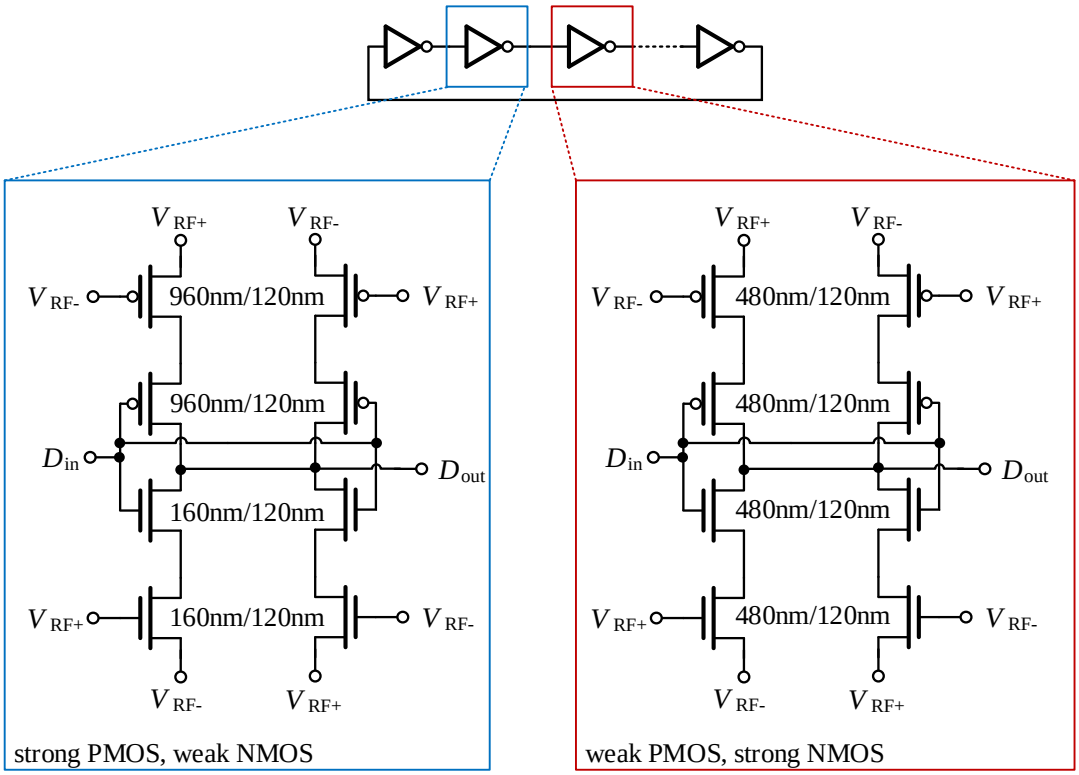


Figure 4.32 Schematic of the dual-phase RF-only inverter based ring oscillator

4.5.5 Controller

The controller takes output signals from power level detector and ring oscillator, then generates the three signals that directly drive the demodulator and digital baseband. Figure 4.33 and Figure 4.34 show the simplified diagram and simulated waveforms of the controller, respectively. The global “Clock” is set to high during power level transition periods. The global “Reset” signal is synchronized to the global clock signal. The “PowerUp” that indicates starting of a new data bit is also synchronized to the global clock signal. It is set to high for one clock cycle at the beginning of each ASK high period. The measured controller output signals are shown in Figure 4.47 to Figure 4.50.

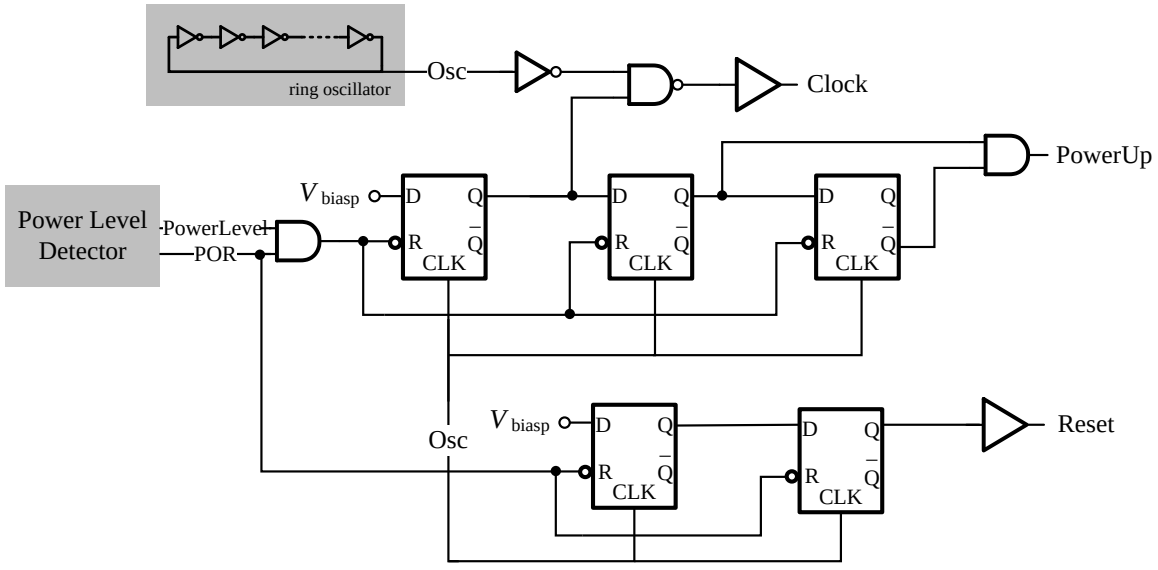


Figure 4.33 Simplified gate level diagram for controller

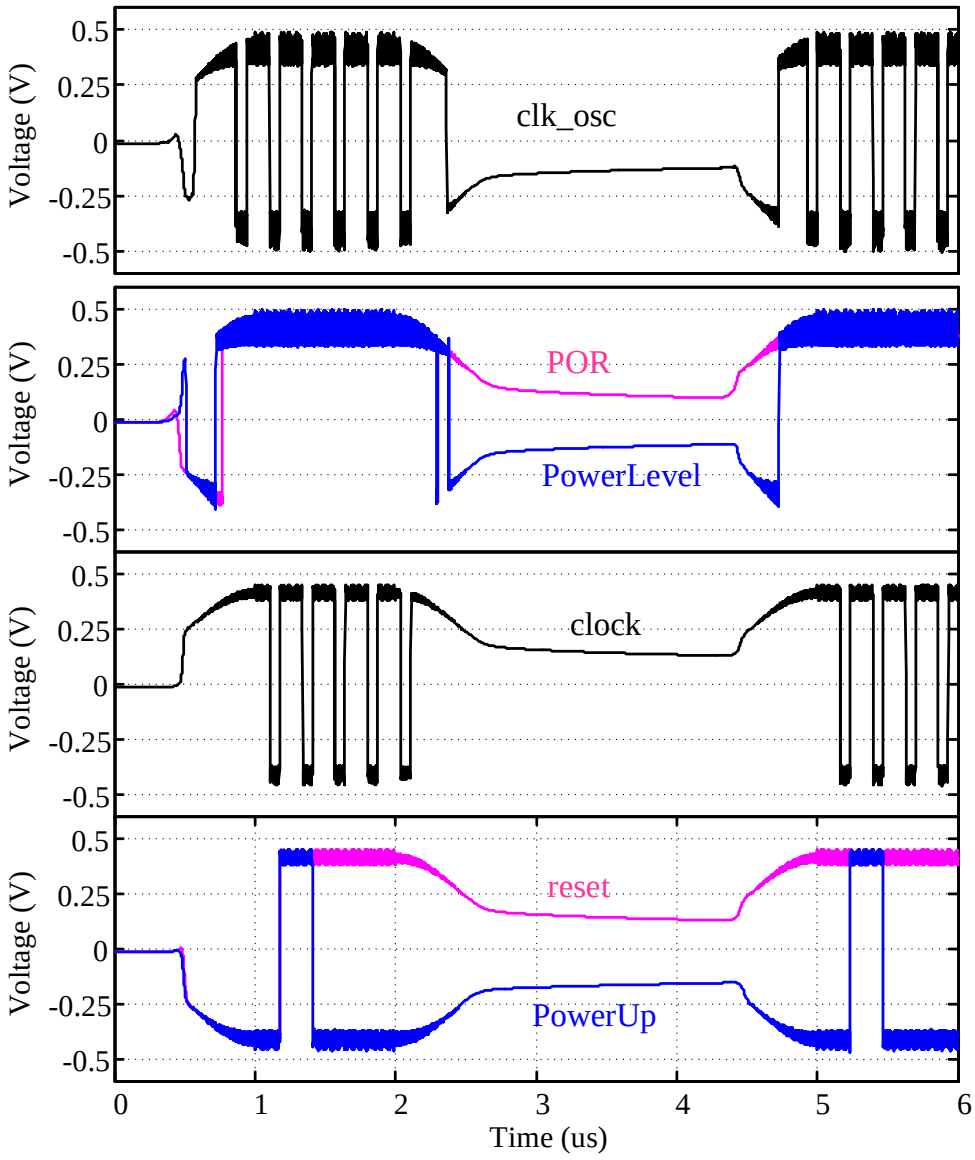


Figure 4.34 Simulated waveform of controller output signals

4.5.6 Backscatter

A reactive backscatter circuit was implemented as shown in Figure 4.35. Two vertical natural capacitors $C_{bs1}$and C_{bs2} were connected in serial and controlled by two large switching transistors M_1 and M_2. The load reactance is modulated by M_1 and M_2 respectively.

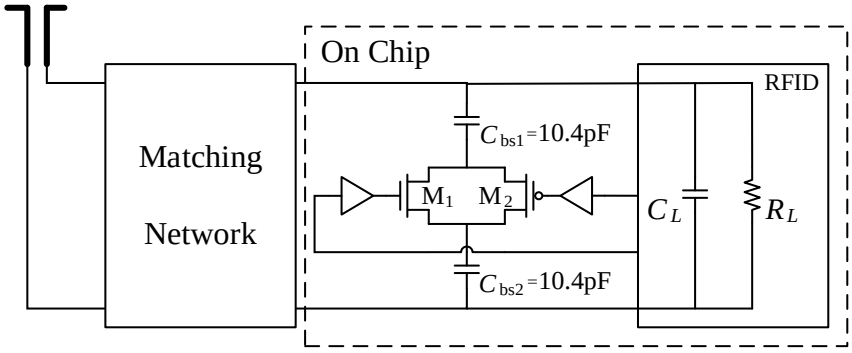


Figure 4.35 Simplified schematic for capacitive backscatter circuits

4.6 Measurements

The rectifier-free UHF Gen-2 compatible RFID tag was implemented in a 0.13μm CMOS technology and features dimensions of 0.6 mm × 0.3 mm. A die micrograph of the test chip is shown in Figure 4.36.

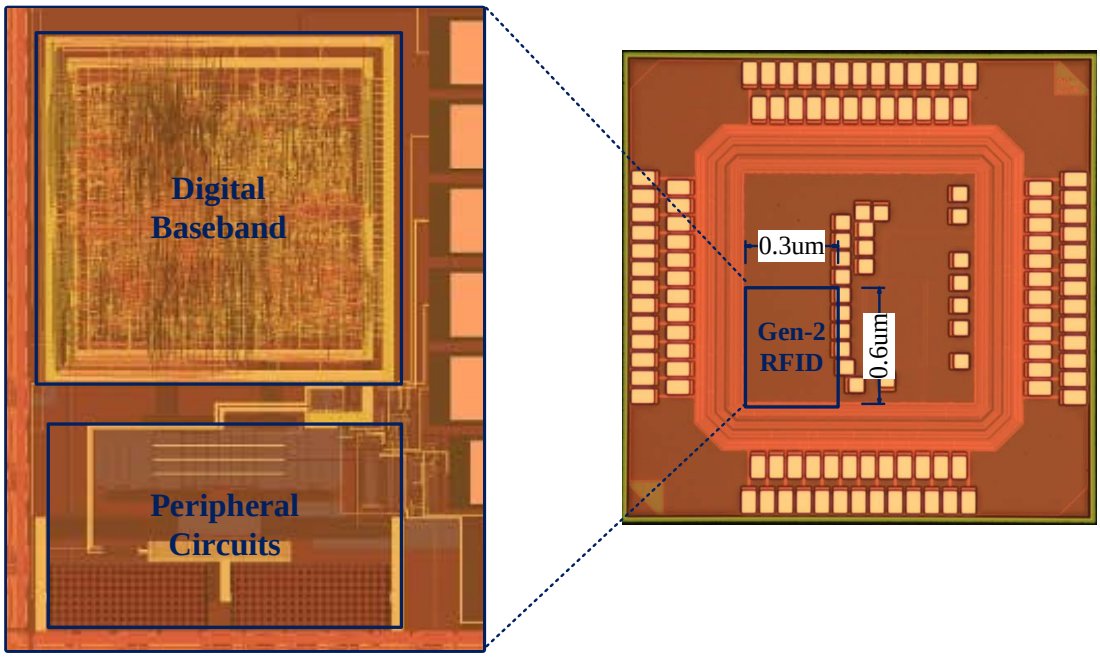


Figure 4.36 Die micrograph of the implemented chip and layout of the Gen-2 compatible RFID tag

4.6.1 First Attempt

The RFID tag was first powered up with a constant amplitude RF carrier. The timing management output signals were probed and checked against the default power up values. Among the six signals checked (Osc, POR, PowerLevel, Clock, Reset, PowerUp), the output of power level detector "PowerLevel" was not correct. There are several potential causes:

- As shown in Figure 4.29, the voltage V_{ref} was designed to be lower than V_{env} due to the voltage drop across the diode-connected transistor M_1. However, the transistor M_1 and capacitor C_{large} serve as a peak detector which may accumulate a higher voltage than V_{env} on C_{large} after a long period of time.

- Functionality of the ring oscillator used for clocking the sampler cannot be checked due to lack of observation point.
- As informed by the foundry, this fabrication run suffers from severe gate leakage problems, which may lead to malfunction of the cross-coupled inverters.

4.6.2 Second Attempt

The measurement proceeds by bypassing part of the power level detector and externally generating the "PowerLevel" signal, which is the envelope of the ASK modulated RF carrier. A photo of the measurement setup is shown in Figure 4.37 and a corresponding block diagram is presented in Figure 4.38. The Tektronix HFS 9009 generated the RF envelope signal according to Gen-2 protocol. The Agilent E4438C was driven by the envelope signal and generated the ASK-modulated RF carrier. The "PowerLevel" signal was a delayed version of the envelope signal, and was driving the rest of circuitry through a passive DC probe. The internal signals were observed by probing with GGB-35 active high-impedance probe, whereas the backscatter output signal was obtained via wirebonding to the testing board. Figure 4.39 shows the close view of the testing board setup for RFID measurement. The instruments were controlled via a GPIB controller, and MATLAB codes were developed for RF envelope generation and output waveform capture.

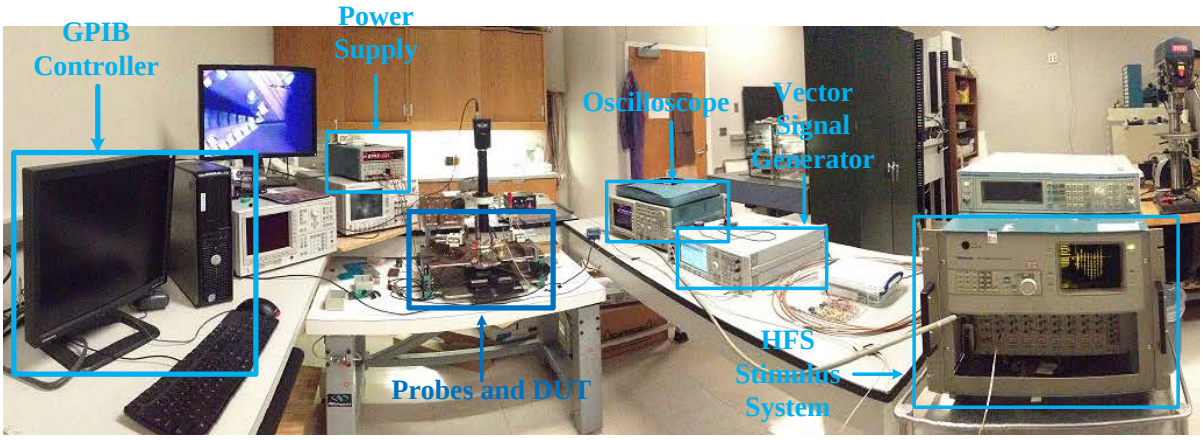


Figure 4.37 Measurement setup for RFID testing

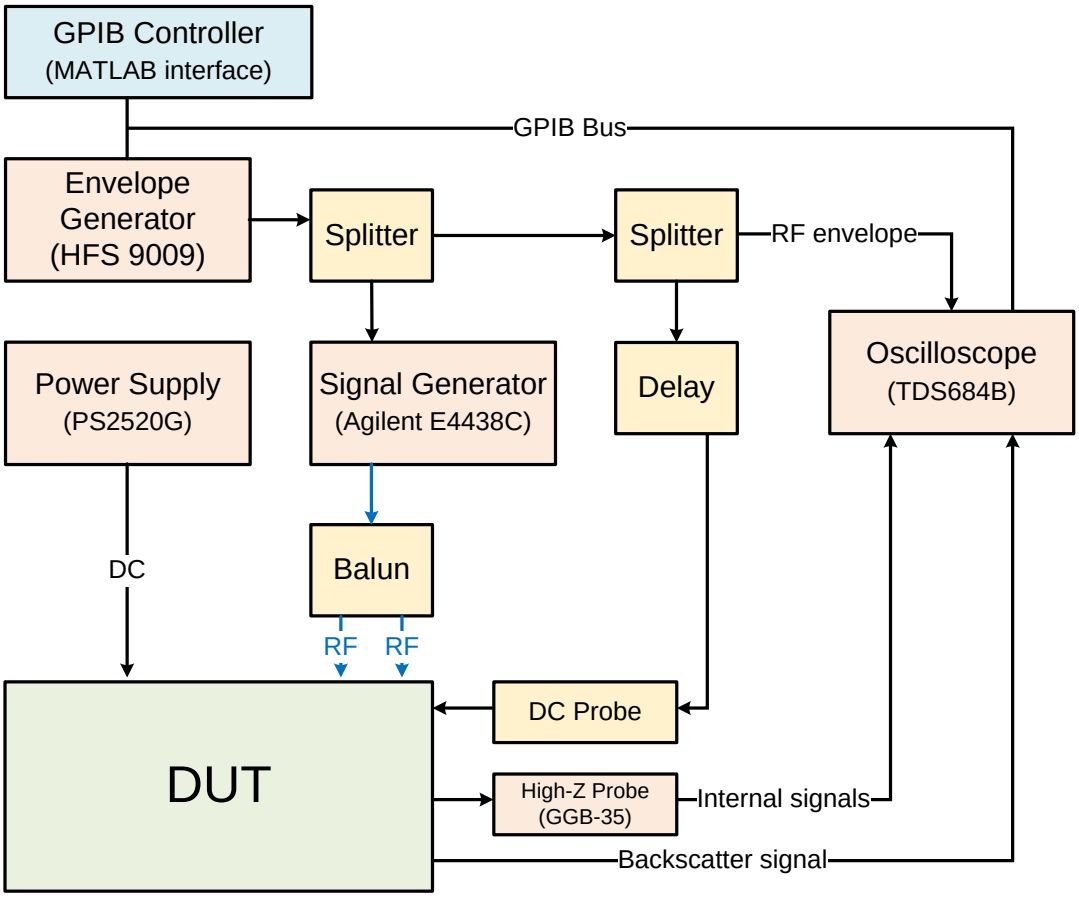


Figure 4.38 Block diagram of RFID measurement setup

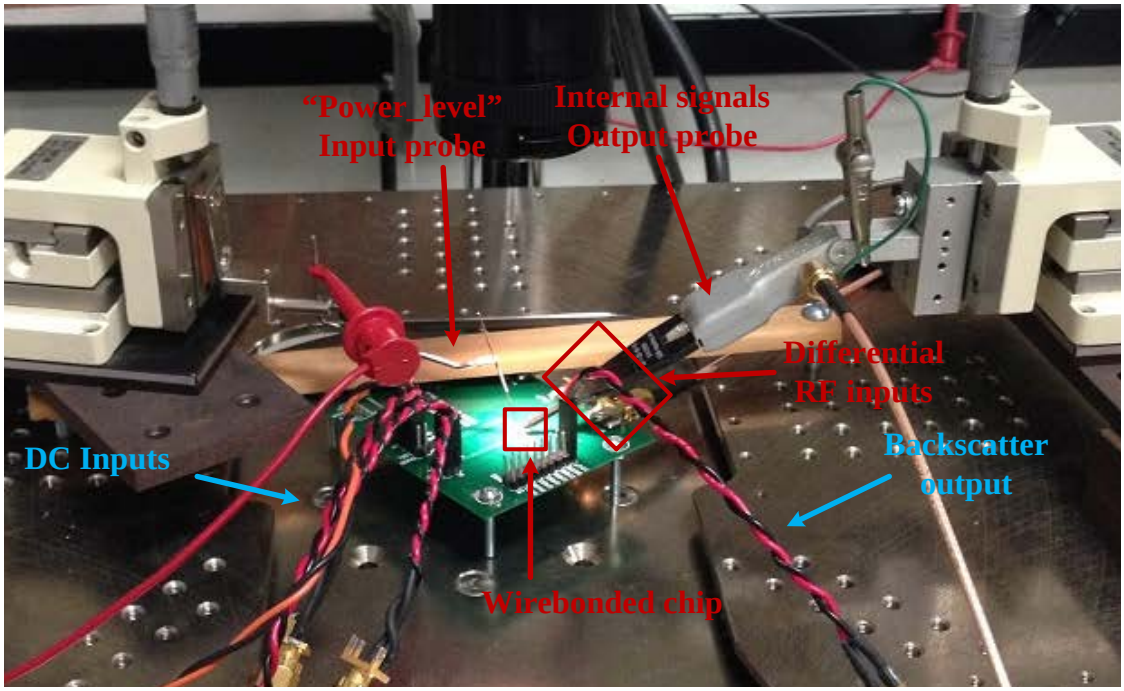


Figure 4.39 Testing board setup for RFID measurement

A "Query" command defined in Gen-2 protocol was used as the stimulus for RFID testing. The command level timing diagram of a complete "Query" inventory is shown in Figure 4.40. In Gen-2 protocol, each new round of inventory starts with a continuous wave (CW). It is followed by a preamble which defines the forward-link and reverse-link parameters. Then the command "Query" is sent. After that, the reader sends the CW for a certain period of time to power the tag and wait for the tag's response. The definitions of preamble and "Query" command can be found in [25] and the official RFID protocol [26]. Table 4.6 lists the parameter settings used for this testing. As the tag recognizes the "Query" command, it sends back a predefined preamble followed by a 16-bit random number (RN16)

as a token. Figure 4.41 shows the measured waveform of the tag response. The incident power to the RFID tag was 10 dBm in the measurement. The power consumption of the RFID is calculated from the incident power and S11 of the tag input port. The simulated S11 magnitude of RFID across the Gen-2 frequency band is shown in Figure 4.42. The calculated power consumption of the RFID tag based on the incident power and S11 is shown in Figure 4.43. Sensitivity is usually used in RF applications that defines the minimum power level at which the RF circuit can properly function. In this case, the tag sensitivity is 3.3 dBm at the nominal RF frequency (900 MHz). It corresponds to power consumption of 2.1 mW.

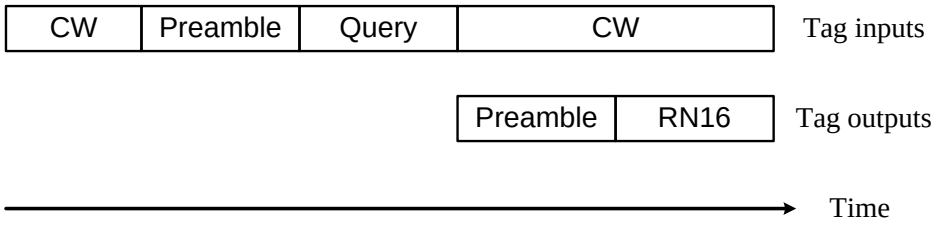


Figure 4.40 Forward-link and reverse-link timing diagram of a "Query" command defined in the Gen-2 protocol

Table 4.6 Parameter setting of preamble and "Query" command

Parameter	Value
RF frequency	900MHz
RF amplitude	500mV
Tari	20μs
RTcal	60 μs
TRcal	100 μs
DR	8
TRext	0
M	1
Q	0
Sel	00
Session	00
Target	0

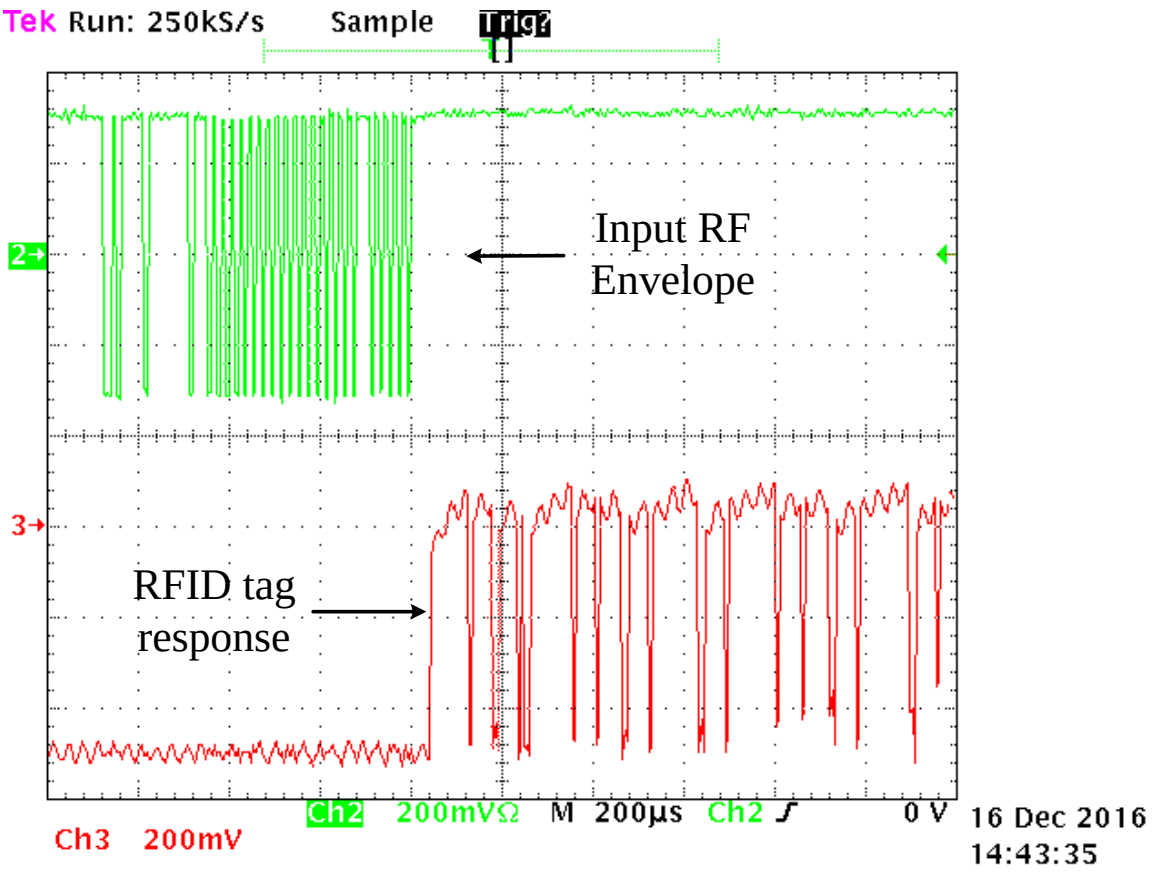


Figure 4.41 Measured RF carrier envelope for a "Query" command and the RFID tag response

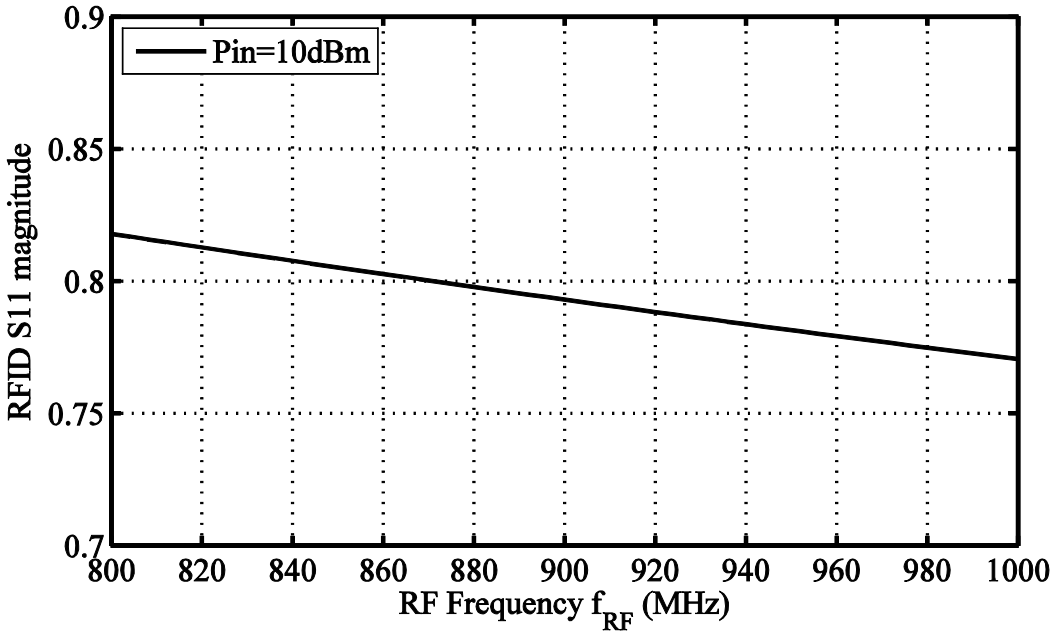


Figure 4.42 RFID S11 magnitude in the Gen-2 frequency band

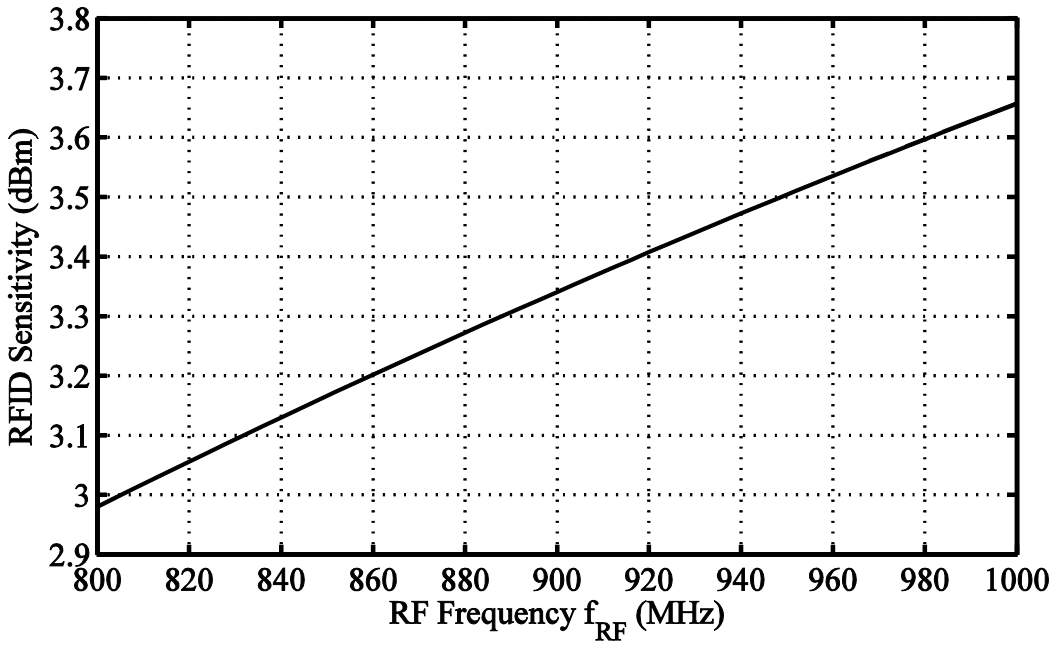


Figure 4.43 RFID sensitivity in the Gen-2 frequency band

The functionality of the timing management block was also verified by probing the intermediate outputs. The measured waveforms of the five key intermediate output signals are plotted in Figure 4.44 to Figure 4.50. They all match with the design specification.

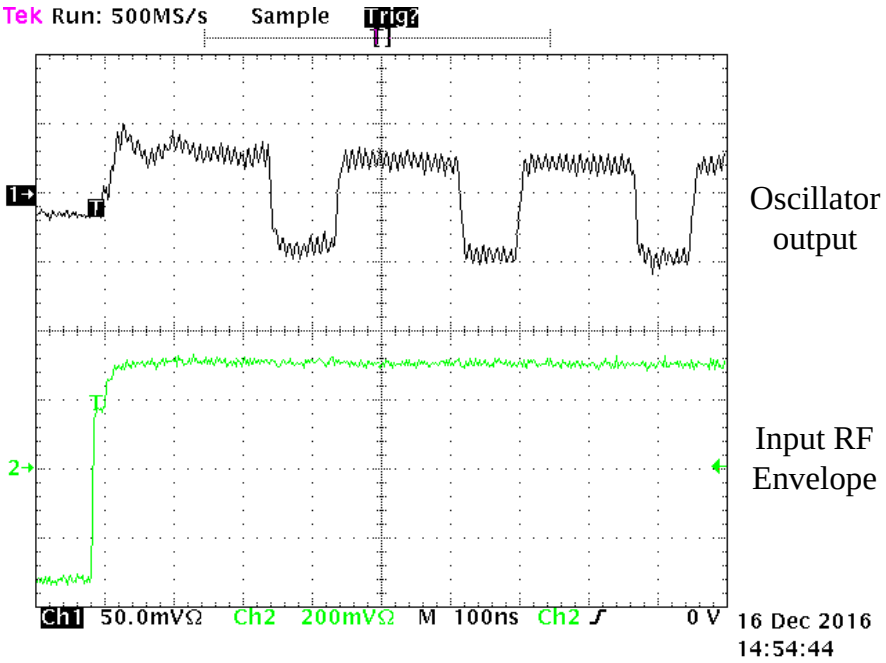


Figure 4.44 Measured free-running oscillator output at low-to-high ASK power level transition

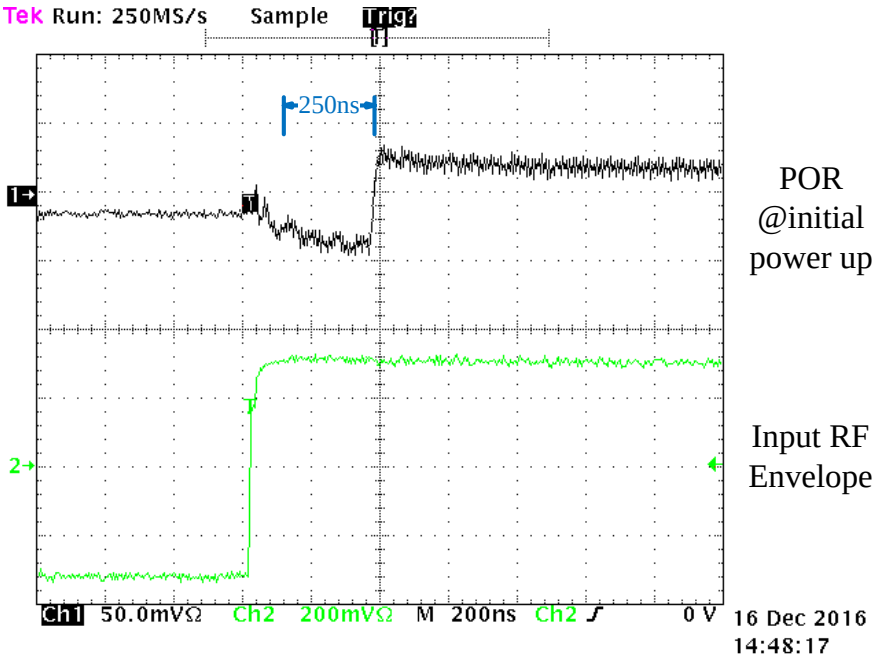


Figure 4.45 Measured POR signal at initial power up. Note the logic low period (250ns) for initial power up reset

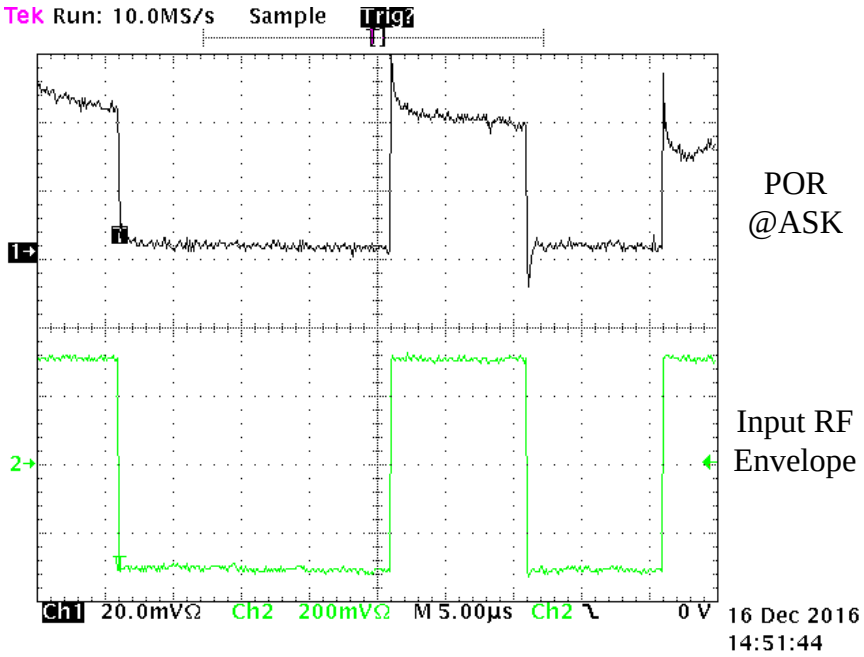


Figure 4.46 Measured POR signal at ASK power on and off. Note the absence of logic level low

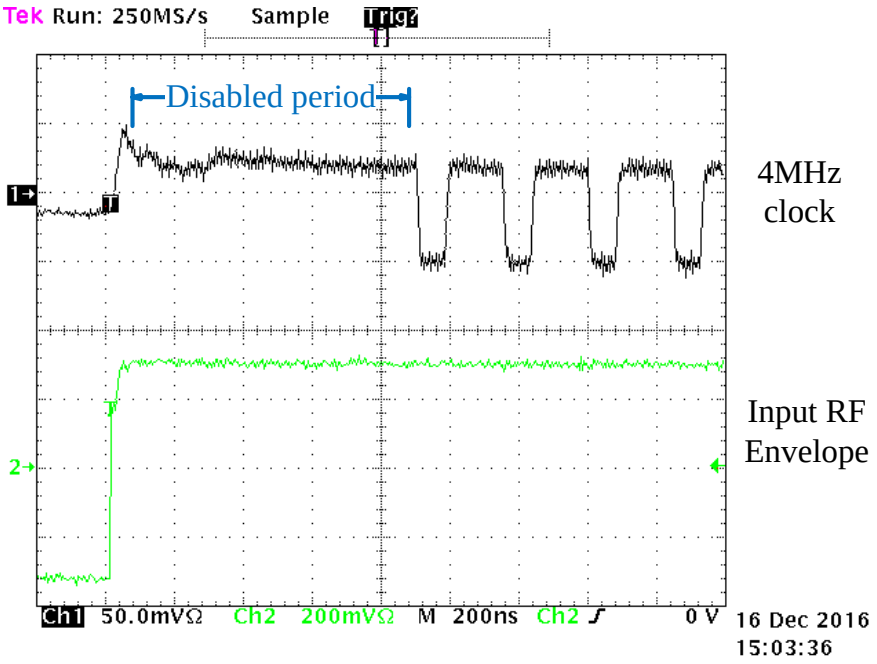


Figure 4.47 Measured 4 MHz clock signal at low-to-high ASK power level transition. Notice the initial disabled period for logic value restore

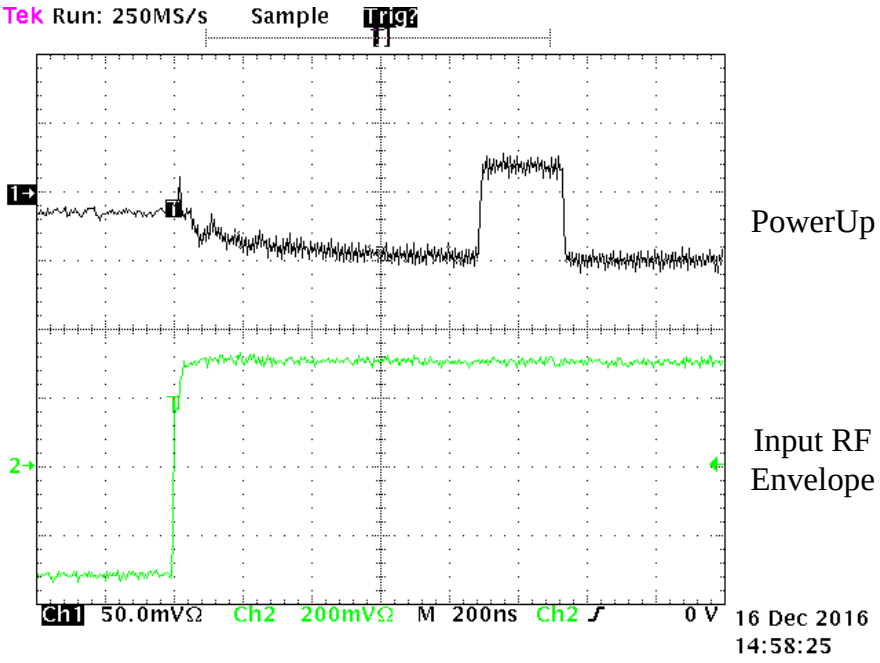


Figure 4.48 Measured signal PowerUp at low-to-high ASK power level transition indicating the starting of a new ASK high period

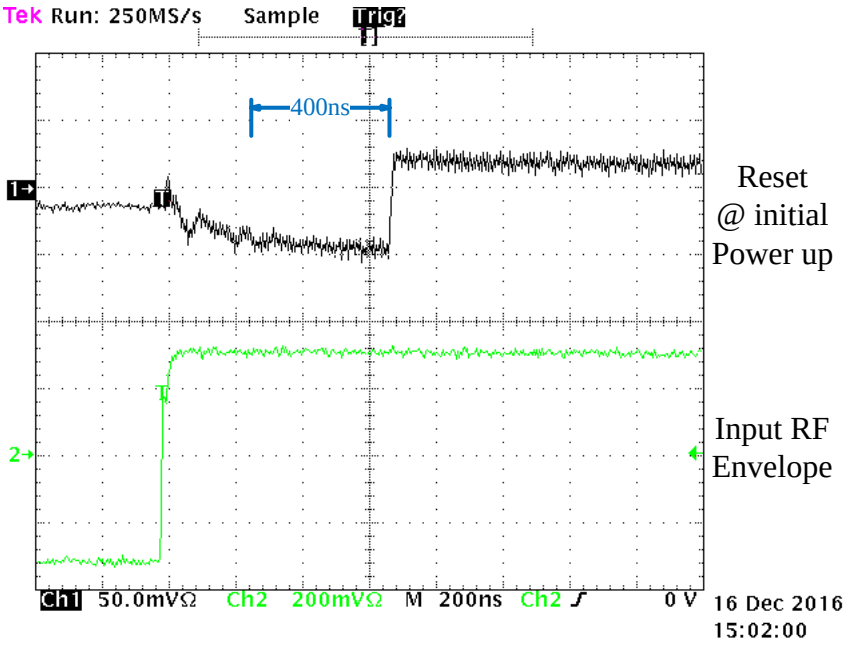


Figure 4.49 Measured global asynchronous reset signal at initial power up for 400ns

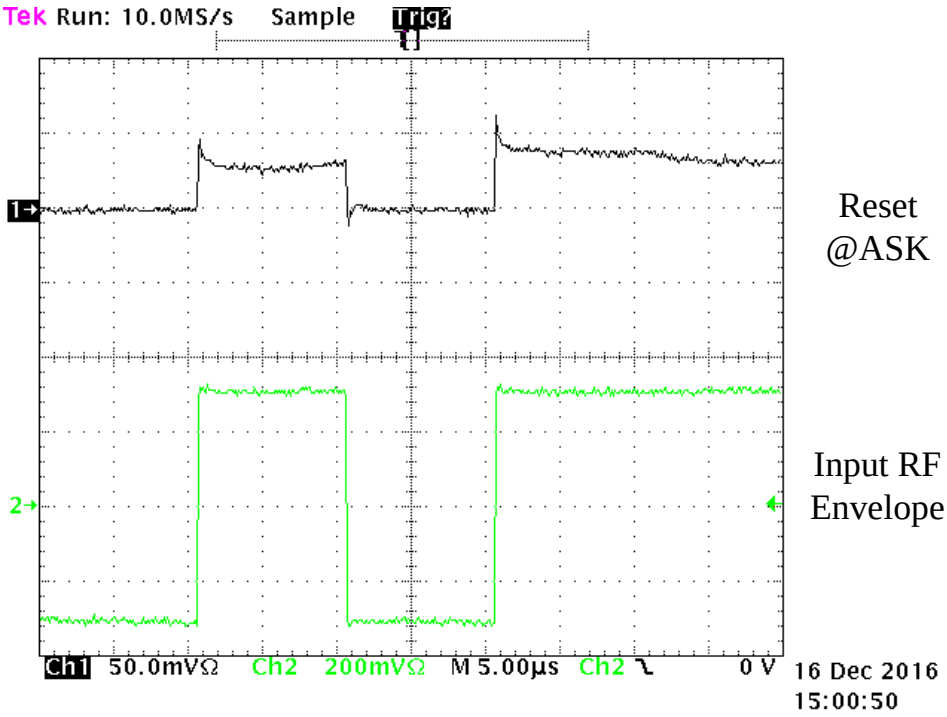


Figure 4.50 Measured reset signal during ASK power on and off. Note the absence of reset active

The functionality of timing management blocks and baseband logic has been verified with the silicon results from the measurements. It also proves the effectiveness of the digital design flow which incorporates PST sharing algorithm and the powering solution under ASK modulation. On the other hand, part of the power level detection circuit was not working correctly. The measurement was conducted under well controlled environment without introducing the complexity with RFID reader and antennae. The robustness of the tag working in a more realistic environment has not been tested.

4.7 Summary and Discussion

In this chapter, we presented a rectifier-free UHF Gen-2 compliant RFID tag that built with RF-only logic. The system level design methodology and circuit level implementation were discussed. From the silicon measurement results, we show that this design reduces circuit area at the expense of reduced sensitivity. It features a chip area of 0.18 mm^2 and a measured power consumption of 3.3 dBm. A summary of this work and comparison with state-of-the-art designs are shown in Table 4.7.

Table 4.7 Summary of related works

	This work	[28]	[1]	[29]	[30]	[2]	[4]	[3]
Process (nm)	130	160	180	130	130	180	180	130
Standard	Gen-2	-	Gen-2	Gen-2	Multiple	Gen-2	-	-
Tag size (mm^2)	0.18	0.28	3.45	0.55	0.95	1.1	0.9	1.1
Sensitivity (dBm)	3.3	-20	-	-14	-10	-6	-21	-12
Rectifier area ratio	-	-	50%	-	-	25%	50%	50%
Frequency (MHz)	900	-	900	900	13.56/900/ 2400	900	900	900

4.7.1 Summary

The primary conclusions from this chapter are as follows:

- The RF-only based design of RFID tag significantly reduces the circuit area by eliminating the power rectifier and storage capacitors.

- RF-only logic based design suffers from lower sensitivity compared to classic CMOS implementation due to the extra power dissipation of static voltage ripples.
- Only limited analog functions can be achieved with RF-only logic. We have not figured out a way to design non-volatile memory in RF-only logic.
- For digital design with RF-only logic, the timing information from characterization cannot accurately represent the timing behavior in real circuit operations. The reason being the propagation delay of a logic gate is a function of the RF phase, which the designer cannot predict during the standard cell characterization and itself varies during circuit operation. In other words, the timing of a logic path may vary dynamically as the RF phase changes. To prevent the potential setup violation, enough timing margin needs to be left during logic synthesis.
- The timing analysis for post-layout parasitic extracted netlist is of limited use due to the lack of timing model for parasitic resistance and capacitance powered by RF signals.

4.7.2 Final Thoughts on Low Power Design

As discussed in the prior chapters, the dynamic power consumption of RF-only logic dominates the total power dissipation, and the profile is similar to classic CMOS as RF amplitude decreases. Therefore, an RFID characterized at a lower RF level may potential achieves a comparable sensitivity with those classic designs. On the other hand, we presented that there is a primary trade-off between the circuit area and power consumption while

keeping the performance constant. To maintain the same performance level at a lower RF amplitude (a lower power level), there are two major approaches:

- Employ more parallelism for computation and data path, which needs more hardware blocks.
- Size up standard cells to increase their driving strength and reduce propagation delay. It also helps to reduce process variation and mismatch which are critical issues for near-threshold designs.

With the same standard cells characterized for 500mV RF amplitude, we synthesized the same RTL code of the digital baseband for lower RF amplitudes. Instead of re-characterizing these cells at lower RF levels, we explored their performance degradation ratios at lower RF amplitudes and applied these ratios to the clock periods to emulate the lower RF level scenarios. The timing and area results from logic synthesis are summarized in Table 4.8. It indicates that a design characterized at 350mV (3dB sensitivity improvement) still achieves a timing slack of more than half of the clock period while the circuit area increases only by 7%.

Table 4.8 Timing and area results from logic synthesis for lower RF amplitudes

RF amplitude	Degrade ratio	Clock period	Critical path	Gate count	Area (μm^2)
500 mV	1	250 ns	125 ns	6928	56428.44
450 mV	1.3	192 ns	83 ns	7140	59325.12
400 mV	1.8	136 ns	64 ns	7174	59474.36
350 mV	2.8	87 ns	41 ns	7352	60314.12

Chapter 5

Conclusion and Future Work

In this dissertation, we presented the RF-only logic, a new logic family that permits digital operations directly with an AC power supply instead of DC. We analyzed its characterizations and synthesized its system design methodology. A Gen-2 compliant RFID tag has been developed using RF-only logic to demonstrate its advantages on area saving. The primary conclusions of this dissertation are as follows:

- RF-only logic enabled passively powered circuit design can save circuit area compared to conventional implementation by eliminating the AC-DC power rectifier and storage capacitors.
- At the same RF power level, the RF-only logic based design typically consumes more power than conventional CMOS implementation due to RF feedthrough.

There are several interesting directions in future research. As pointed out in Fig. 59, the conventional rectifier based power solution and RF-only logic based power solution are at

the two ends of the power solution spectrum for passively powered circuits. The conventional approach implements a centralized power source whereas RF-only based design is a fully distributed solution. These two solutions trade power consumption with circuit area. A powering scheme that characterize the power supply according to local charging patterns may potentially be the optimal solution which balances power and area. PST sharing among mutually exclusive gates is the first step towards this direction. Future research may explore higher order PST sharing that permits multiple gates charging simultaneously.

Another interesting direction is how to implement more analog circuits and memory cells using RF-only logic. Currently, only a limited number of analog functions can be implemented. We would like to extend the RF-only logic to more analog circuits which will enable more applications.

In this dissertation, we only explored the application of passively powered circuits. There are potentially other applications that may benefit from RF-only logic's AC powering feature. One interesting direction is dynamic voltage scaling. The current DC-powered dynamic voltage scaling involves DC voltage level converting by DC-DC converters, which are not as power efficient as their AC counterparts. Besides, the response time of AC transformers is usually faster than the DC-DC converters.

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APPENDICES

A PST Sharing Algorithm

The goal of the PST sharing process is to identify the mutually exclusive gates and group them into clusters, each cluster of gates powered by one PST cell. The input to this process is the post-synthesis gate-level netlist. The output is also a gate level netlist, with the PST cells added. Subsequent physical design starts with this manipulated gate level netlist.

Given a netlist, the PST sharing process takes three steps:

- For each gate in the netlist, identify all the possible switching slots based on topology
- Identify mutual exclusiveness by checking functionality.
- Group logic gates into clusters so that each cluster consists of gates that are mutually exclusive. To minimize the total PST cell number, the number of clusters should be minimized.

Following sections will discuss in details the algorithms implemented to achieve these goals.

A.1 Switching Slot Identification

Assuming a unit delay model for each gate, then one can calculate all the possible time slots that any particular gate can switch based on topology [21].

Input: gate level netlist

Input: *rn_l*: list of root nets, includes block inputs and flip-flop outputs

Input: *ng_dic* (*N*, *G*): dictionary from net (*N*) to its loading gates (*G*)

Input: *gn_dic* (*G*, *N*): dictionary from gate (*G*) to its output nets (*N*)

Output: *gtp_dic* (*G*, (*T*, *P*)): dictionary for each gate (*G*), all delay time slots (*T*) that it may transit; for each time slot (*T*), all the paths (*P*) that may trigger the transition at this particular time slot

```
1:  for all rn ∈ rn_l do
2:      if rn ∈ ng_dic then
3:          for all g ∈ ng_dic[rn] do
4:              append (gtp[g][0], rn)
5:              FIND_CHILDREN_GATE (g, 0)
6:      else
7:          continue
8:  function FIND_CHILDREN_GATE (gate, delay)
9:      n = gn_dic [gate]
10:     if n ∈ ng_dic then
11:         for all g ∈ ng_dic [n] do
12:             UPDATE_DELAY (gate, g, delay)
13:             FIND_CHILDREN_GATE (g, delay+1)
14:     else
15:         return 0
16: end function
```

17: **function** UPDATE_DELAY (*father*, *child*, *delay*)

18: append (*gtp_dic* [*child*][*delay*], *father*)

19: **end function**

A.2 ME Identification

More gates can be clustered if the functionality of the circuit is also taken into consideration. A relation graph G_r (V, E) is defined to represent the (dis)charging relation among gates. A vertex $v_i \in V$ stands for one gate, and an edge $(v_i, v_j) \in E$ stands for mutual exclusive relation for gates v_i and v_j.

Input: *gtp_dic* (*G*, (*T*, *P*))

Input: st_dic (*T*, *G*): time slot dictionary, for each time slot (*T*), include all gates (*G*) that may transit at that slot

Output: G_r(*V*, *E*): mutual exclusive relation graph

1: **for** all $t \in T$ **do**

2: **for** all $(g_i, g_j) \in G$ **do**

3: **if** FIND_ME_GATES (g_i, g_j, t) = 1**then**

4: **continue**

5: **else**

6: remove $(g_i, g_j) \in E$

7: **function** FIND_ME_GATES (g_i, g_j, t)

8: **for** $p_i \in gtp\_dic\ [g_i][t]$ **do**

9: **for** $p_j \in gtp\_dic\ [g_j][t]$ **do**

10: **if** FIND_ME_PATH $(p_i, p_j) = 1$ **then**

11: **continue**

12: **else**

13: **return** 0

14: **end function**

15: **function** FIND_ME_PATH (p_i, p_j)

16: **if** FIND_ME_TRANSITION $(p_i, p_j,$ '01', '01') = 0 **then**

17: **return** 0

18: **else if** FIND_ME_TRANSITION $(p_i, p_j,$ '10', '10') = 0 **then**

19: **return** 0

20: **else**

21: **return** 1

22: **end function**

23: **function** FIND_ME_TRANSITION (path0 path1, tran0, tran1)

24: trace back delay path to determine all the logic values on output of each gate

25: **if** value conflict identified **then**

26: **return** 0

27: **else**

28: **return** 1

29: **end function**

A.3 ME Gate Grouping

Input: G_r (V, E): mutual exclusive relation graph

Output: grouped relation graph

1: **while** ($E \neq 0$)

2: find $v_i \in V$ with the largest set of neighbors

3: find $(v_i, v_j) \in E$ that v_j with the largest set of common neighbors

4: s $\leftarrow v_i \cup v_j$

5: $V \leftarrow V \cup$ s

6: delete edges linked to v_i, v_j

7: add edges for *s* and its neighbors