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[54] **THIN FILM TRANSISTOR WITH LARGE GRAIN SIZE DRW OFFSET REGION AND SMALL GRAIN SIZE SOURCE AND DRAIN AND CHANNEL REGIONS**

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- [51] Int. Cl.⁶ **H01L 29/04**; H01L 31/036
- [52] U.S. Cl. **257/66**; 257/327; 257/64; 257/393
- [58] **Field of Search** 257/64, 65, 66, 257/67, 69, 70, 327, 390, 391, 392, 393, 401

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[57] ABSTRACT

A thin film transistor includes: a) a thin film transistor layer comprising a source region, a channel region and a drain region; the thin film transistor layer further comprising a drain offset region positioned between the drain region and the channel region; b) the channel region being substantially polycrystalline and having a first average crystalline grain size; and c) the drain offset region being substantially polycrystalline and having a second average crystalline grain size, the second average crystalline grain size being larger than the first average crystalline grain size. A method for forming such a construction using polycrystalline materials, preferably polysilicon, and an amorphizing silicon implant with subsequent recrystallization is also disclosed.

6 Claims, 5 Drawing Sheets

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