

ABSTRACT

ZHU, NING. Modeling, Design and Simulation of Low Cost Digitally Controlled DC/DC Converter. (Under the direction of Alex Q. Huang.)

In the past a few years, the attraction drawn by digital control of switching power regulators have been rising steadily. Low cost implementation is of many people's interest.

First of all, this thesis discussed general stability issue associated with modulation. The choice of voltage mode or current mode control is made based on the nature of the modulation. A more precise digital domain modeling method is presented next. Unlike the emulation and the old direct design method, the new transfer function is derived under the observation that switching power converter is discrete in nature. With the new transfer function, the ambiguous sample and hold delay is eliminated from the design flow. The control design is straightforward with this modeling approach. Therefore low cost voltage mode controller can be implemented without the penalty of performance. Example of mixed mode simulation flow is show in the thesis.

This thesis also proposed a low cost low power solution from circuit perspective. Its principle and circuit implementation are discussed in detail. The method is proposed to solve the cost issues raised by the requirement of the external memory. At the same time, the power consumption is kept low. Finally, a novel control method is potentially good for digital implementation is introduced. Some experimental results are shown.

Modeling, Design and Simulation of Low Cost Digitally Controlled DC/DC
Converter

by

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Chapter 1

INTRODUCTION

In the past few years, the interest on digitally controlled DC/DC switching power regulators has been rising steadily. In the years before 2001, there were fewer than 5 digital control papers in the major IEEE power electronics conference APEC each year. In the year 2007, this number increased to 40. The reason behind the numbers is that the industry hopes digitally controlled converter can replace the analog counterpart in the future.

1.1 What is digital power?

Digital circuit has been embedded in the power controller IC's since the first day of their existence in the market. Because of the discrete nature of the pulse width modulation (PWM), digital circuit is inevitable in even the oldest analog controller. Power circuits can not operate without protection offered by digital circuits. Protection circuits are usually 'digital'. Figure 1.1 shows one of the oldest analog controllers chip diagram [1]. The digital circuits are highlighted in the diagram.

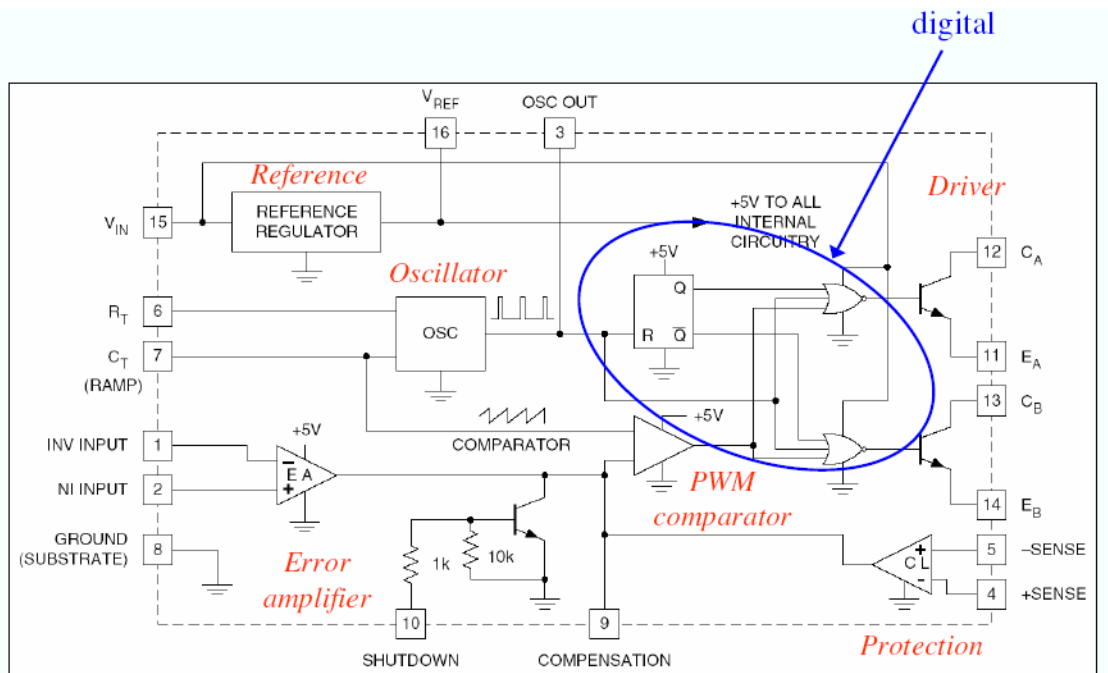


Figure 1.1: A classic ‘analog’ PWM controller chip diagram [1].

The so called ‘*digital power*’ is referred to power converter systems that are digitally controlled. Digital power generally falls into three categories:

A). *digitally controlled analog system*: The control core is built on the conventional opamp based analog control techniques, either voltage mode control or current mode. Digital blocks are installed to provide peripheral functions like: a) serial communication (I^2C Bus, SMBus, etc.); b) digital commanded reference; and c) small amounts of memory on-chip.

B). *microcontroller based control*: it is a useful architecture in terms of flexibility, especially in applications that require programmability. As conventional digital algorithms are sequential in nature requiring several clock cycles to execute an instruction, they are inherently slow and thus are not useful in applications requiring fast response.

C). *pure digital control*: A custom designed non-sequential machine, with hard-wired logic implementation that can produce a fast response comparable to an analog system.

In this thesis, only stand alone digital controller in the last category is discussed.

1.2 General digital controller architecture

Figure 1.2 shows general digital controller architecture [2], which consists of four sub-circuit systems: a) interface between the analog power stage and digital control algorithm executor; b) digital control algorithm executor; c) digital modulator for driver; d) external memory.

The interface part is an analog to digital converter (ADC). It senses analog signals from power stage, such as voltage, current and sometimes temperature. Different from general purpose ADC, the ADC used in digital controller is usually specifically designed according to power converter specifications. Since the ADC is typically integrated with other blocks on the controller chip, a digital controller IC chip is actually a mixed signal IC. On the other hand, a general purpose ADC that meets the system requirements could be used in converter prototype design.

The major control part is the digital arithmetic processor that computes the duty cycle by executing the control algorithm. Digital PID control is the most commonly used control strategy. It is a combination of state machines, arithmetic blocks and oftentimes look-up tables (LUT).

The modulator generates the switch on/off command to drive the power switches. It could be a digital pulse-width modulator (DPWM), or it could be a digital to analog

converter (DAC) followed by a conventional analog PWM used in analog controllers. From circuit complexity point of view, the first method is preferred.

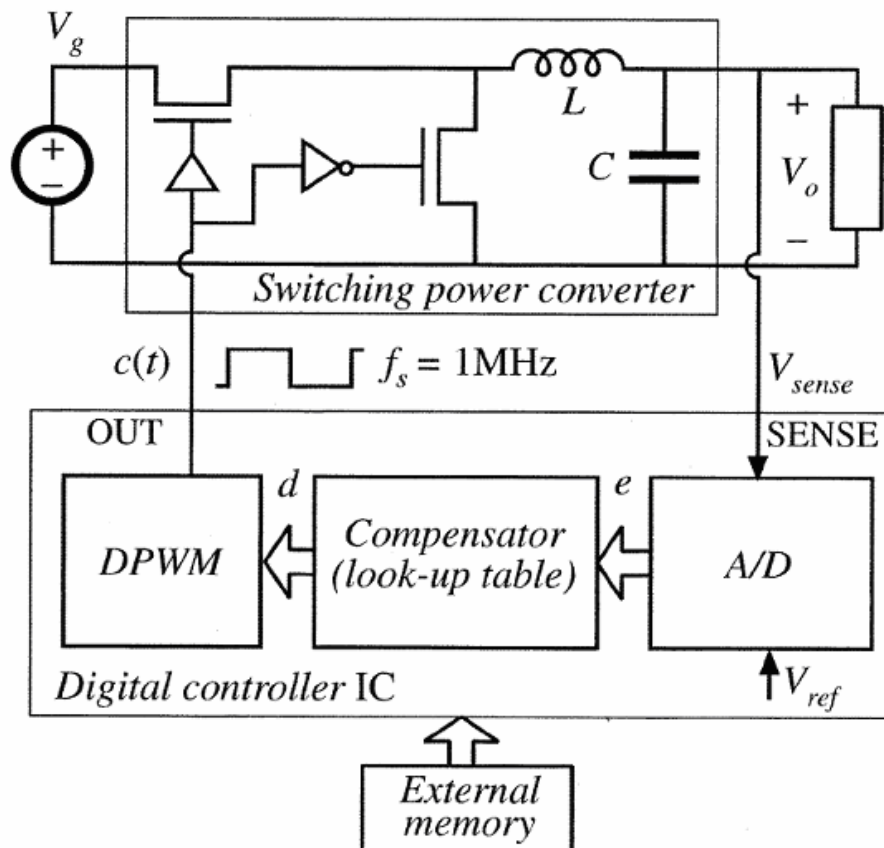


Figure 1.2: Diagram of digitally controlled power converter [2].

External memory is used as a control parameter storage element in the form of a programmable LUT. However, when programmability is not needed in a system, the dedicated control parameters can be integrated with the executor.

1.3 Take advantage of digital control

By observing the architecture, one would immediately notice some interesting features of digital controller over the analog counterpart. It allows advanced control algorithms and strategies to be implemented; it can be programmable and flexible; it has fewer external part counts and so on. These are considered the advantage of digital control: flexibility and programmability. Another major reason behind the big push behind digital solutions for power supply is to take advantage of the Moore's law [3] because digital circuit can scale with the technology easily hence potentially making it cheaper than the analog solution.

In this thesis, a controller's duties are classified into two categories. The first category is the control core, which is the indispensable system stabilizer. The design choice can be, for example, analog versus digital control, voltage mode versus current mode control, state space versus nonlinear control and so on. The second category is the control peripheral, which provides auxiliary functions for the control core, for example, programmability, memory and protection. Other control practice, such as online calibration, is considered somewhere in between.

1.3.1 Control core

Digital controller has the capacity of being versatile, which many believe will lead to better converter performance. However, advanced control method might not appeal to engineers' interest too much, because the plant, DC/DC converter, itself is relatively simple and the classical linear control works well and is easily understood. Advanced control also implies more information is required for control decision making. In the case of power

electronic applications, sensors usually reduce power efficiency. Engineers are generally reluctant to use unnecessary sensors. More information processing requires more computation power, which either adds to design cost or degrades the speed. At last, advanced control methods are usually not well understood by the application engineers and customers. They have steep learning curves for the end users.

In actuality, only a very limited set of standard control methods are used. Most analog controller cores are based on classic feedback control method [4][5]. Dependent on the dynamic response and cost requirement, lead, lag, PID or current mode control are feasible options. These classic control methods work very well. Variations of modulation methods result in different control schemes, such as constant ON time, constant OFF time control. Feed forward control is also a frequently used technical solution for some applications [6].

Digital controller can add more functions to classic linear control. Digital platform makes the combination of linear control and bang-bang control more easily and more reliably. This so-called 'digital nonlinear' control is reported to have improved the response speed during load transient [7].

After all, in digital controller, the control core is usually designed upon the translation from S-domain to Z-domain. S-domain transfer function is extensively used because of both its familiarity to engineers and the true existence of continuous signal/power path in the converter system. How to design a digital version of the traditional analog controller without the penalty of performance becomes a very important issue in the design flow.

Among the analog controllers in the industry, current mode control is very popular. It is generally believed that current mode control is superior in terms of response speed. Therefore, when digital controller is designed, designers prefer current mode control as well.

They tried very hard to replicate the current mode control in digital domain [8]. But is current mode a good choice for digital implementation? Can voltage mode do the same job equally? These questions lead to one of the major contributions of this thesis: the selection of voltage mode or current mode control. A detailed discussion on this issue is presented later.

1.3.2 Control peripheral

The programmability is the most distinguished feature that digital controller has when compared with analog controller. A programmable controller must have rewritable ROM, as depicted as the external memory in Figure 1.2. It allows change of the control parameters offline. Hence, the digital controller chip can fit into different applications. This is considered a marketing advantage for stand alone digital power management chips.

An external memory is very undesirable, because it occupies all the space saved from removing compensation network components in analog controllers, if not more. And the memory chip itself also adds to the total cost. Modern power management technologies provide the designers with the option of built-in E²PROM. The memory can be integrated with the controller core. However, this non-standard option simply means more process steps and more masks, hence making the digital chip more expensive. As can be seen from Figure 1.3 [9], the mask cost has been increasing drastically in the recent years. Obviously, this on-chip memory option may not be a low cost solution.

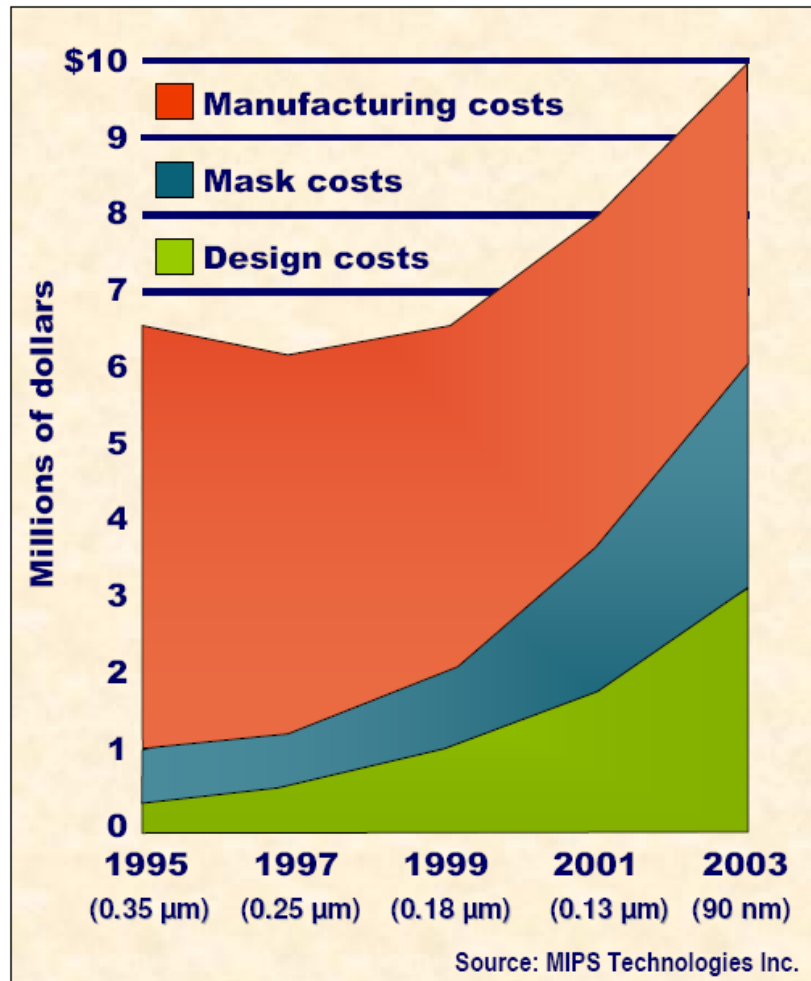


Figure 1.3: Cost evolutions with technologies [9].

Online parametric calibration is reported to be used in sensor gain correction. There are sensing methods that are lossless or low loss, while those methods are not accurate enough to provide useful information. Online calibration adjusts the sensor gain and enables such methods to be used in digital control [10]. It is a general trend to develop online calibration or system identification method to eliminate the need for external memory. Some

methods were proposed in [11][12]. However, these methods are based on complex computation. It is very costly to design and its control reliability is in question.

This thesis proposed a simple online detection method utilizing pre-stored ROM tables to eliminate the need for external memory.

1.4 Thesis overview

This thesis is an attempt to provide simple low cost low power solution of power management digital controller. The emphasis is focused primarily on Buck type converter. The major contributions of this thesis are:

- a) new discrete analysis technique is presented to prove the equivalency of voltage mode and current mode control in both analog and digital implementation;
- b) more accurate digital domain model was developed and verified by mixed mode simulation;
- c) and online detection method and comparator reuse scheme was proposed as a low cost low power circuit solution.

After this introduction chapter, general stability issue associated with modulation is discussed. The choice of voltage mode or current mode control in digital controller is analyzed.

In the third chapter, a more precise digital domain modeling method is presented. Unlike the traditional emulation method, the new Z-domain transfer function derived is based on the observation that switching power converter is discrete in nature. With the new transfer

function, the ambiguous sample and hold delay is eliminated. The control design is more straightforward with this modeling approach.

The fourth chapter discusses the mixed signal mode simulation methodology used in designing a mixed signal digital controller. Based on this design flow, the proposed model was verified by both simulation results and experimental results.

The fifth chapter proposed low cost low power solution to eliminate the need for external memory. Its principle and possible circuit implementation are discussed. Finally, a novel control method is potentially good for digital implementation is introduced. Some experimental results are shown.

Chapter 2

VOLTAGE MODE VERSUS CURRENT MODE

Before the implementation of a digital controller is discussed, the first question comes into a designer's mind would be the choice of voltage mode control or current mode control. The discussion is focused on the most extensively used buck regulators.

2.1 Modulator instability examples

A more general discussion on the modulator is helpful to this key design decision making. Figure 2.1 shows the diagram of a typical voltage mode controlled Buck converter. The highlighted area is the modulator in question. A design example is shown below to illustrate the issue with the modulator. In the example, The power stage parameters are: $f_s = 1\text{MHz}$, $L = 100\text{nH}$, $C = 1640\mu\text{F}$, $R = 0.1\Omega$, $V_{in} = 12\text{V}$ and $V_o = 1\text{V}$.

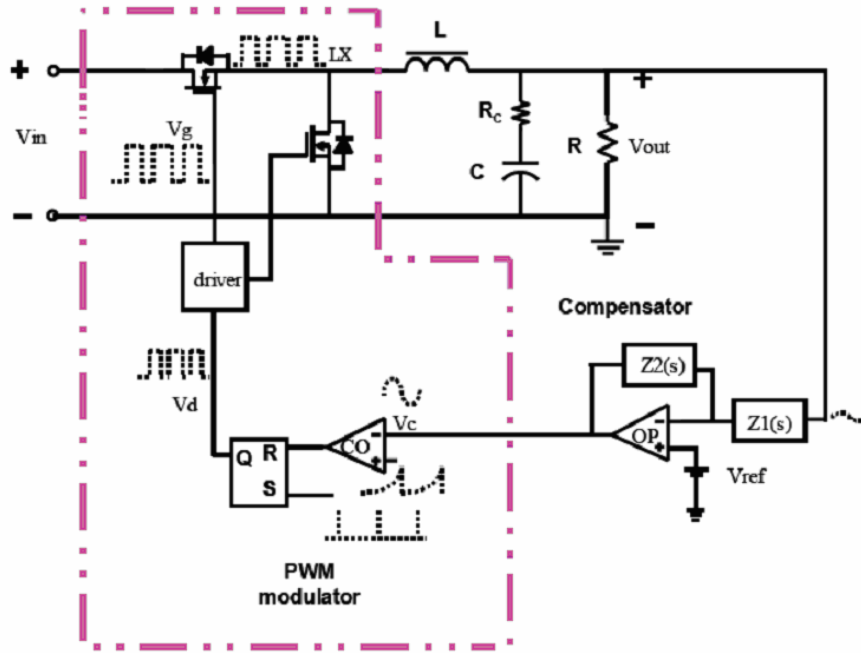


Figure 2.1: Buck regulator diagram.

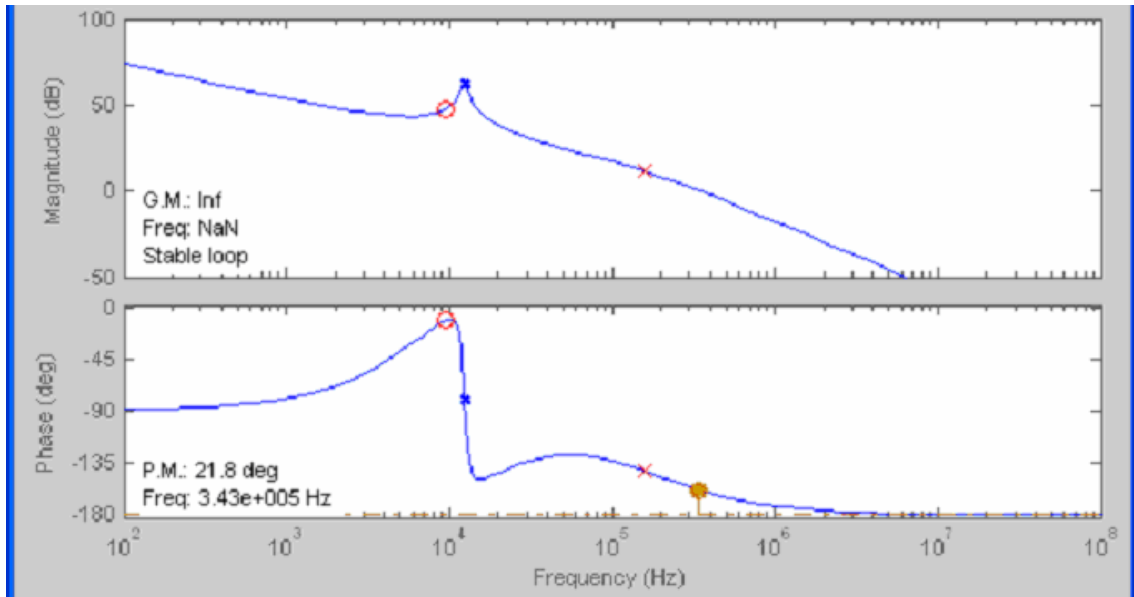
The ideal control to output transfer function is:

$$G_{vd} = \frac{V_{in}}{1 + \frac{L}{R}S + LCS^2}$$

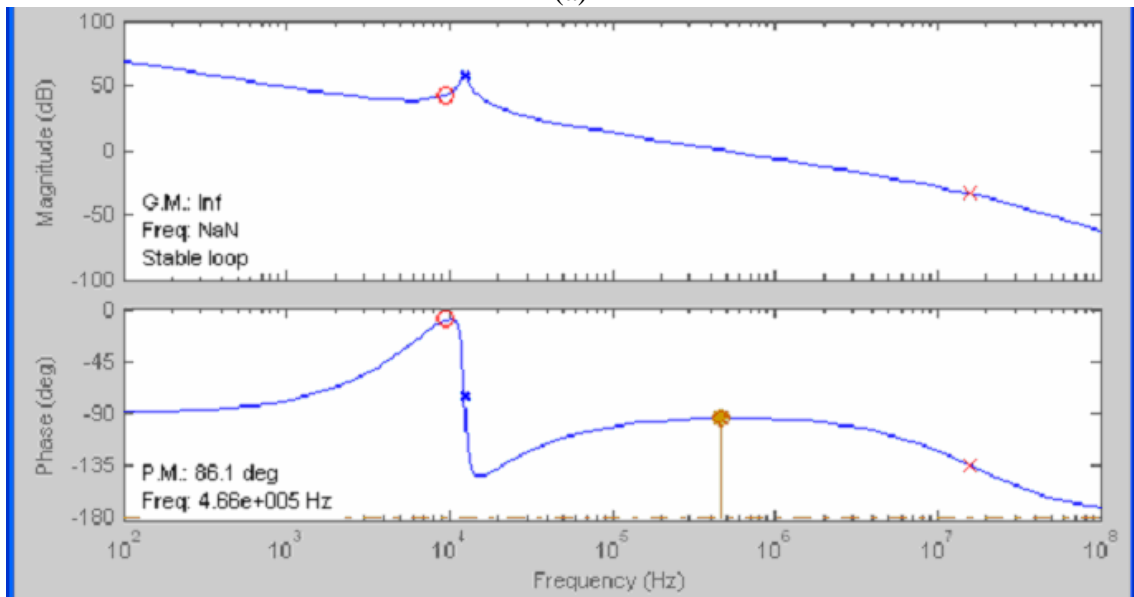
Two PID compensators are designed. Both of them are in the form of:

$$\frac{\omega_i (1 + S/\omega_{z1})(1 + S/\omega_{z2})}{S (1 + S/\omega_{p1})(1 + S/\omega_{p2})}$$

For both designs, ω_{z1} , ω_{z2} and ω_{p2} are fixed. In case a, ω_{p1} is chosen to be 10^6 rad/second. In case b, ω_{p1} is chosen to be 10^8 rad/second. The gain ω_i is the variable that adjusts the bandwidth. The bode plot of the two designs are shown in Figure 2.2.



(a)



(b)

Figure 2.2: Bode plots of two designs.

In both cases, the gain ω_i is increased as high as possible. As can be seen, in case (a), the Bode plot shows the phase margin is decreasing with the increasing gain. Meanwhile, in

case (b), the Bode plot shows almost constant 90 degrees of phase margin within certain bandwidth range, because the pole positions are in very high frequencies. From small signal perspective, both designs should result in a stable closed loop system, even though there is very small phase margin in case (a). A small phase margin is not a good design practice, but as long as it is positive, the closed loop system should have no stability issues.

However, when the gain is increased to a certain point that makes the crossover bandwidth approach approximately half of the switching frequency, the converter with case (a) loop gain design exhibits instability. Meanwhile, surprisingly, the case (b) converter is always stable no matter how high the gain is.

2.2 Multi-frequency small signal model

Frequency response around half of the switching frequency is referred to as fast scale analysis. When design is based on slow scale analysis, the well known averaging technique is a very good approximation of the system [4]. However, averaging method average out the fast scale dynamic behavior, thus it is usually considered to be inaccurate. Sample and hold effect is one popular way to explain the bandwidth limitation and the instability [13][14]. From Nyquist theorem, it is widely accepted that the bandwidth cannot be higher than Nyquist frequency, namely half of the switching frequency. To treat this issue properly, analytical model based on the side bands interaction, resulting from the sample and hold, was developed in a recent work [15].

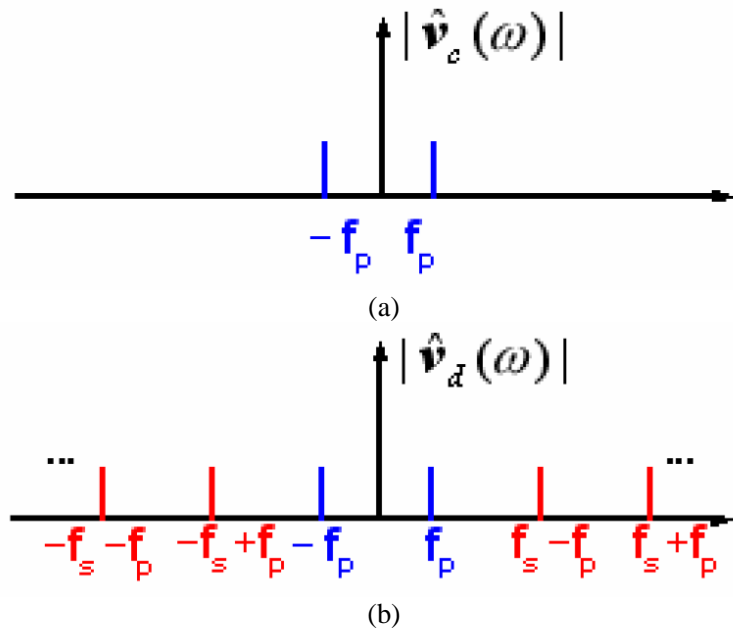


Figure 2.3: Sampling result of PWM scheme: (a) input spectrum of the PWM comparator; (b) output spectrum of the PWM comparator.

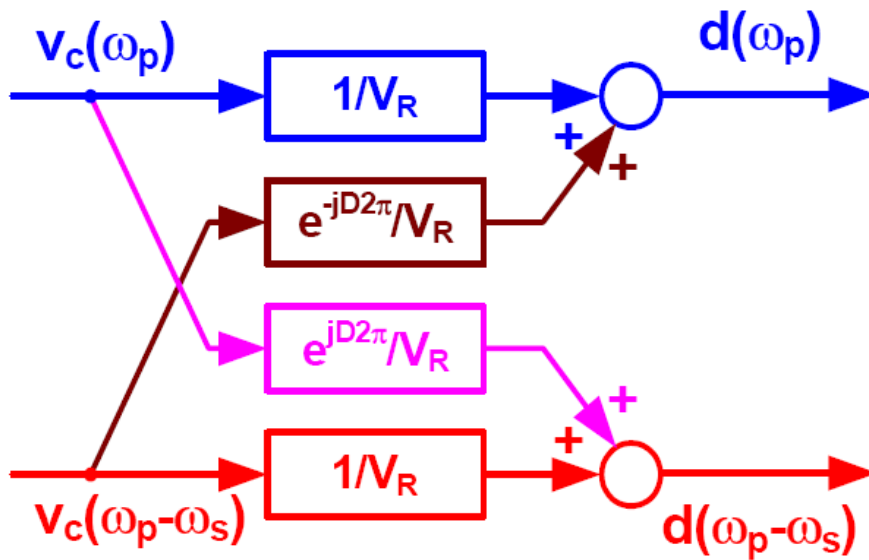


Figure 2.4: Multi-frequency PWM model [15].

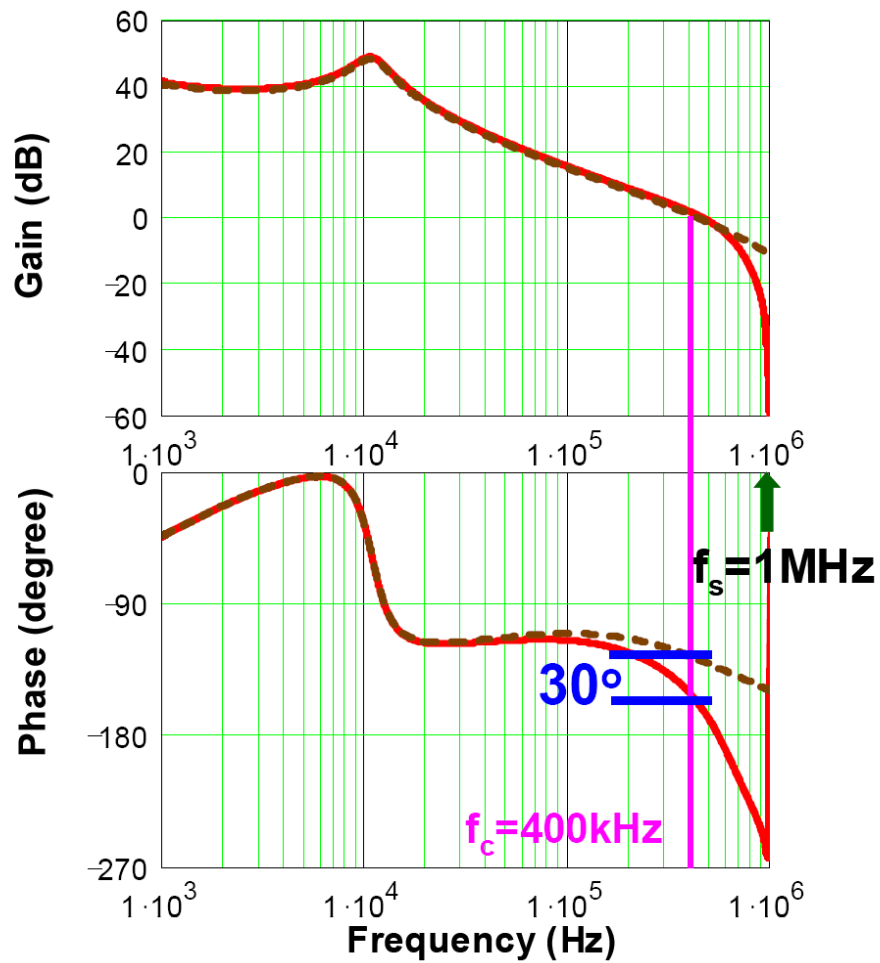


Figure 2.5: Phase delay caused by the sidebands [15].

The old average model averages out all the high frequency components. A more accurate small signal model can be obtained if the nonlinearity of the modulator is carefully accounted for. The spectra of the modulator under fixed frequency perturbation are shown in Figure 2.3. v_c is the control voltage and v_d is the duty. A multi-frequency model, which takes sidebands into consideration, was derived in [15].

The basic idea was to find the different frequency phase delay as they are cross coupled in the modulator, as shown in Figure 2.4. After some math manipulations, the improved loop gain is as follows,

$$T_v(\omega_p) = \frac{T_{av}(\omega_p)}{1 + T_{av}(\omega_p - \omega_s)}$$

Based on this model, the Bode plot can be re-drawn in Figure 2.5, which clearly shows the improved model shows a phase delay in high frequencies. When the bandwidth is approach switching frequency, the phase delay drops to -360 degrees. This model was developed to explain the barrier of achieving high gain high bandwidth from small signal perspective.

The work presented in [15] seems to be a legitimate explanation of the instability observed in case (a), but it is not able to explain why case (b) is always stable, because -360 degree phase shift implies small signal instability, no matter what.

2.3 A new modulation perspective

The above mentioned multi-sideband high frequency modeling has two assumptions. One of the assumptions is the existence of sample and hold. The other assumption is the small ripple is negligible. However, ripples are quite important in switching converters. There are some fast response control methods proposed purely based on output voltage ripple [16]. The previous model is true in small signal sense, but power converter modulation can not operate effectively without ripple.

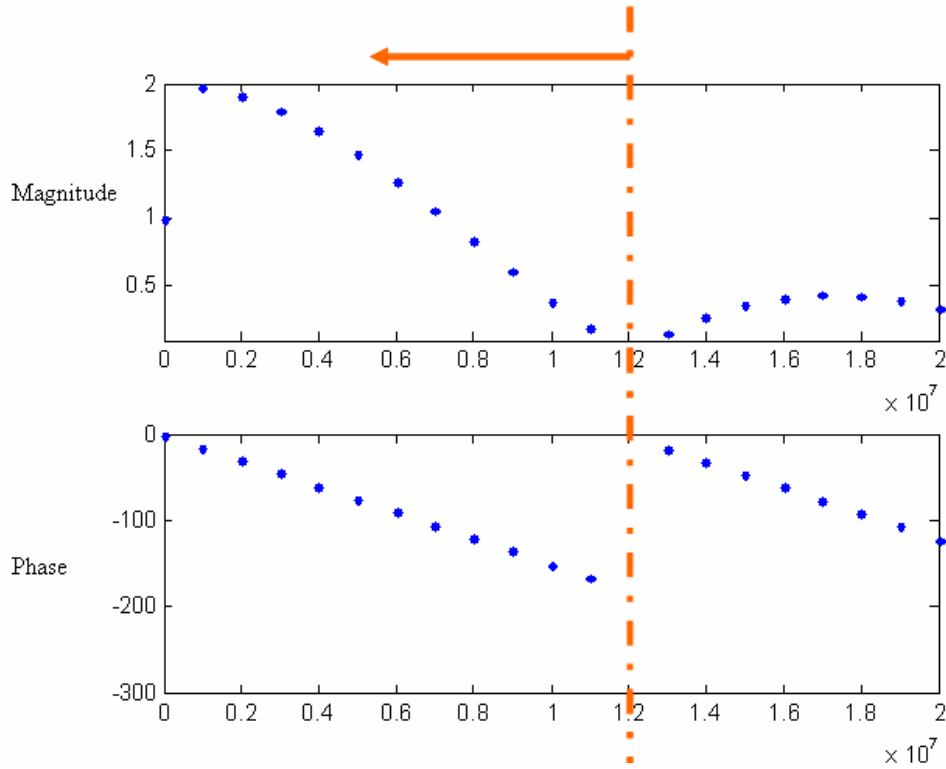


Figure 2.6: Switching node spectrum.

In the steady state, the voltage on the switching node (LX in Figure 2.1) is a sequence of square wave with fixed duty, assuming the input voltage does not vary. In the frequency domain, this chopped supply contains DC, switching frequency and all higher order harmonic components. An analytical form of Fourier series can be obtained:

$$C_n = DV_g \text{Sinc}(nD\pi) e^{-jnD\pi}$$

$$p(t) = \sum C_n e^{jn\omega_s t}$$

where D is the steady state duty, ω_s is switching frequency. Figure 2.6 illustrated the spectrum with approximately 1/10 duty cycle at 1MHz switching frequency. As can be seen from the spectrum density, most of the spectrum power comes from the range between the

switching frequency and 10 times of it. This is an even more accurate statement in practical converters, because the finite rising or falling time of the switching node voltage tends to reduce high frequency components.

Having the information of the input spectrum, we can predict the frequency response at any point in the linear feedback loop, which starts from the switching node to the output of the compensation amplifier. But we still need to know how the modulator works, and that is the most controversial part.

For low bandwidth design, the control voltage, the output of the compensator, is almost a constant value, because the high frequency components are greatly attenuated. The sawtooth carrier in the modulator stabilizes the steady state duty cycle.

If the compensator output voltage is not constant, and instead it also has a triangular shape but has opposite direction as that of the carrier, as shown in Figure 2.7, a linear voltage to time modulator is formed.

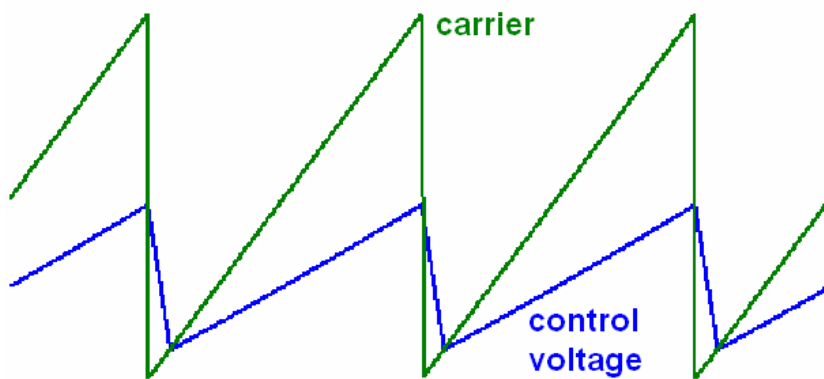


Figure 2.7: Triangular shaped modulation scheme.

Regardless of the Nyquist criterion of stability in linear system, it is intuitive such a modulator would be more stable. An immediate observation is that the ripple is important to the control the converter.

To obtain the triangular waveform of the controller is straightforward. Since the input of the linear loop is a square waveform, a $1/S$ response beyond switching frequency would generate the desired waveform. This requires that the loop transfer function, excluding the modulator gain, has an asymptote of $1/S$ in high frequency domain. At first glance, it is too challenging to realize this in any system, because there are numerous unmodeled modes in high frequencies. However, as discussed before, the spectrum density is highly concentrated in between f_s and $10f_s$. Therefore, the $1/S$ asymptote is only needed in this frequency range. Correspondingly, in phase response, the phase shift should not be too far off 90 degrees.

If the bandwidth is low, we would still expect to see a nearly flat-line control voltage. The design guideline proposed here does not change much of the converter performance. The nice thing about this new design guideline is that, with the control voltage well shaped, it is possible to push the linear loop gain to very high value to obtain higher bandwidth. When the bandwidth is higher, the amplitude of the control voltage becomes higher. The shape of the control voltage plays the role in modulation stability. Assuming the crossover frequency is larger than switching frequency, if the frequency response is designed as aforementioned in the range of interest, the concept of the phase margin at crossover is no longer meaningful due to the nonlinear modulator, which operates in lower frequency domain.

2.4 Proof of the modulation stability

Now, the fundamental question naturally pops up. How to examine the stability of the converter, if such high bandwidth is indeed achieved? According to the proposed design guideline, the Nyquist criterion is automatically satisfied in most of cases, because of the 90 degree phase margin. And we also said that the phase margin is no longer a valid concept in high frequencies. It would be contradictory to use bode plot as a proof. The third reason is that other researcher already published complex modified small signal frequency response. Figure 2.5 is one of the examples.

After all, this modulation design guideline is only based on intuition. More rigorous proof has to be presented. The discrete and numerical methods were used for the analysis. A closed loop buck converter can be described in continuous state space functions, as follows:

$$\dot{X} = \begin{bmatrix} \dot{X}_p \\ \dot{X}_c \end{bmatrix} = \begin{bmatrix} A_p & 0 \\ -B_c C_p & A_c \end{bmatrix} \begin{bmatrix} X_p \\ X_c \end{bmatrix} + \begin{bmatrix} B_p & 0 \\ 0 & B_c \end{bmatrix} \begin{bmatrix} V_g \\ V_{ref} \end{bmatrix}$$

$$Y = \begin{bmatrix} 0 & C_c \end{bmatrix} \begin{bmatrix} X_p \\ X_c \end{bmatrix} = C_c X_c$$

where A_p , B_p and C_p are the system, input and output matrices of the power stage respectively. They can be determined from the differential equations of the circuit. Note that the system has discontinuous input. Therefore, during the ON time, the input vector is B_p ; while during the OFF time, part of the input vector is zero. A_c , B_c and C_c are the system, input and output matrices of the compensator respectively. They can be formulized in control canonical form from the small signal transfer function. The $-B_c C_p$ term comes from the feedback in the loop. The output $Y = C_c X_c$ is the control voltage.

The discrete expression of the system can be written in the following form

$$X_{[(k+1)T]} = e^{AT} X_{[kT]} + e^{A(1-d_k)T} \int_0^{d_k T} e^{A\tau} B_p V_g d\tau + \int_0^T e^{A\tau} B_c V_{ref} d\tau$$

Unfortunately, it can not be written in a closed analytical form, because the duty d has to be determined numerically. The DC solution is calculated by Newton-Raphson method:

$$X_0^{i+1} = X_0^i - [I - DP(X_0^i)]^{-1} [X_0^i - P(X_0^i)]$$

The duty is obtained by solving the following equation,

$$\varphi \equiv e^{Ad_k T} X_{[kT]} + \int_0^{d_k T} e^{A\tau} B_p V_g d\tau + \int_0^{d_k T} e^{A\tau} B_c V_{ref} d\tau - V_{pp} d_k = 0$$

The stability is examined by observing the locations of Jacobian matrix eigenvalues. If the eigenvalues are in the unity circle, the system is stable; otherwise, it is not stable. The Jacobian Matrix is as follows for the buck converter,

$$DP = e^{AT} - e^{(1-d)AT} BVT \left[\frac{\partial \varphi}{\partial d_k} \right]^{-1} \frac{\partial \varphi}{\partial X_{[kT]}}$$

Figure 2.8 shows the trajectories of the eigenvalues of the previous two designs with the gain increasing. For case (a), when the bandwidth increases to around half of the switching frequency, one of the eigenvalues intercepts the unity circle even though there is still some degrees of phase margin in the averaged model loop gain. On the other hand, the eigenvalues in case (b) are always in unity circle, no matter how large the gain is. This result verifies the previous simulation result and proves the ‘linear’ modulation intuition is correct.

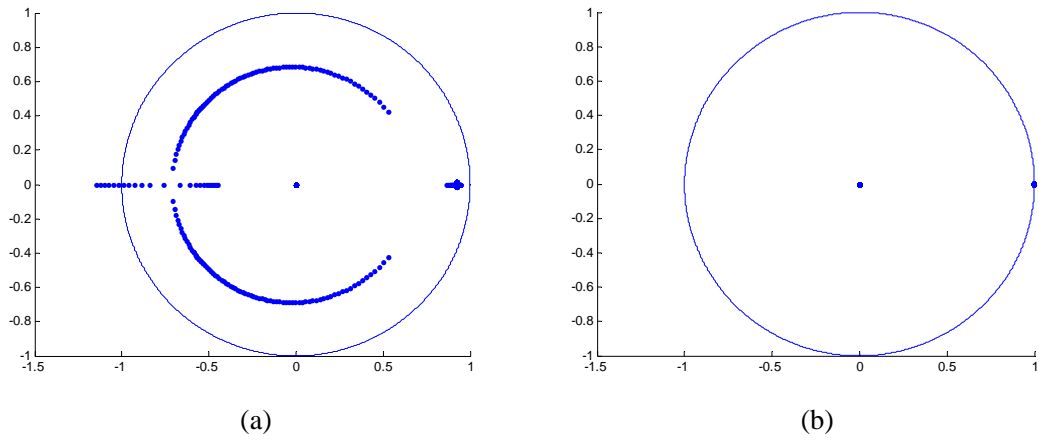
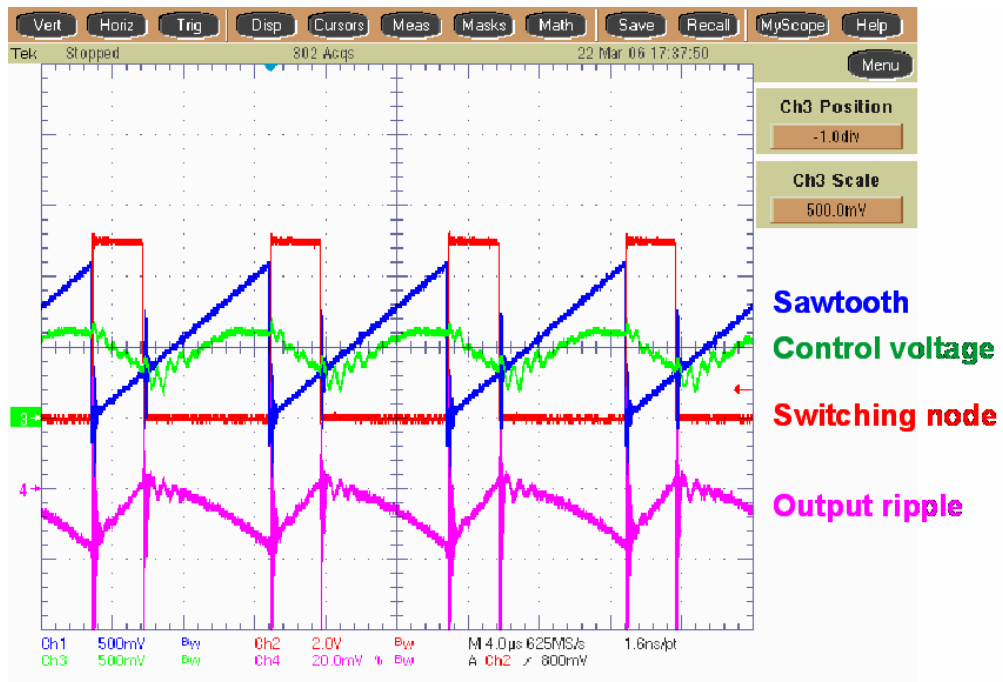
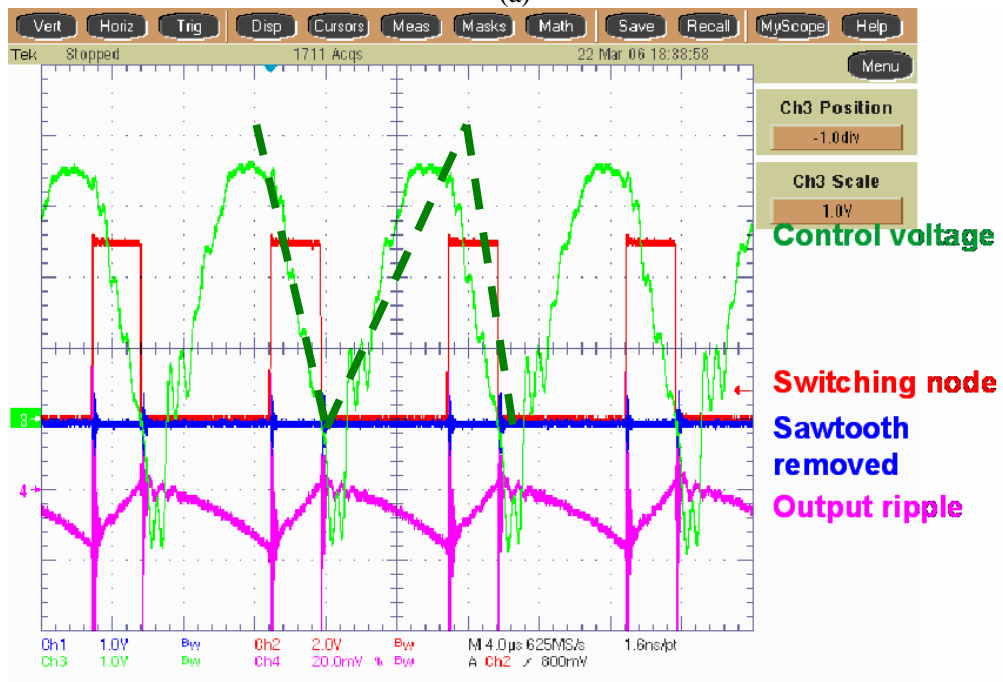


Figure 2.8: Trajectories of the discrete Jacobian matrix eigenvalues.

When the modulation carrier is DC (carrier amplitude is zero), the linear loop gain of the regulator can be considered to be very large. Under such condition, if the compensator is designed following the proposed modulation stability guideline, the regulator is still stable. Figure 2.9 shows the experimental proof. Figure 2.9 (a) is the operation with the sawtooth carrier and Figure 2.9 (b) is the operation without carrier (carrier voltage = 0). Under both conditions, the regulator is stable, even though the control voltage is not perfectly triangle, as indicated by the dashed line.



(a)



(b)

Figure 2.9: Experimental waveforms with and without external sawtooth carrier.

2.5 Conclusions on the modulator

From the preceding discussion, it is obvious that the modulation, the only nonlinear element in the buck regulator control loop, play an important role in the system stability. There are small signal stability and large signal stability during the modulation process. The latter is determined by the ripple. When the control loop gain becomes large enough, the large signal stability will be dominant in the overall system stability.

In industrial practice, both voltage mode and current mode control are extensively used. The old cliché about the fast response of the current mode control has existed for years. However, even in voltage regulator module (VRM) application, which has the most stringent requirement on control loop design [17], voltage mode control are still extensively used to make commercial products. Voltage mode control could achieve the same performance by carefully designing the compensator. Voltage mode control simulation example in Figure 2.10 shows that fast voltage mode control allows the inductor current to follow the load change well. This was originally believed to be only achievable with current mode control.

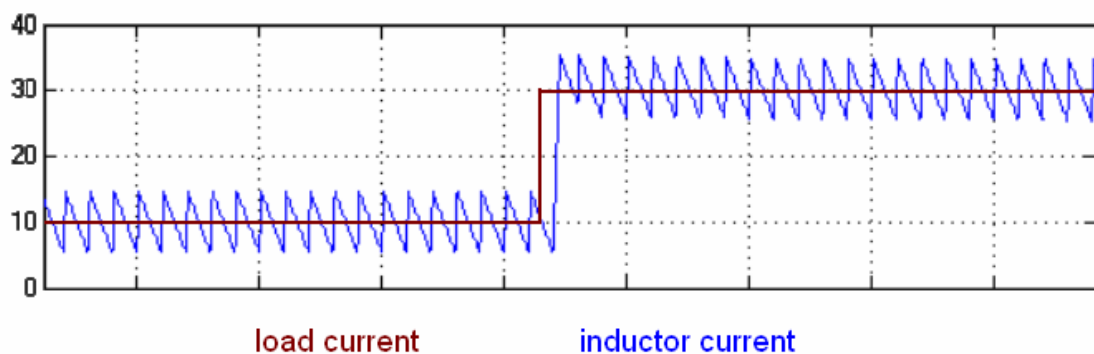


Figure 2.10: Voltage mode control simulation shows fast load tracking ability.

From pure control perspective, current mode control just provides a clean ‘linear’ modulator, which help stabilize the power converter. Current mode modulation scheme is shown in Figure 2.11. Old current mode control modeling paper tried to incorporate small signal with large signal [14]. However, the readers might recall that the well known sub-harmonic instability is the direct result of large signal instability.

$$\left| \frac{m_2 - m_a}{m_1 + m_a} \right| < 1$$

This large signal instability is not unique in current mode control; it is the nature of the PWM modulator, as we have just proven in our previous discussion.

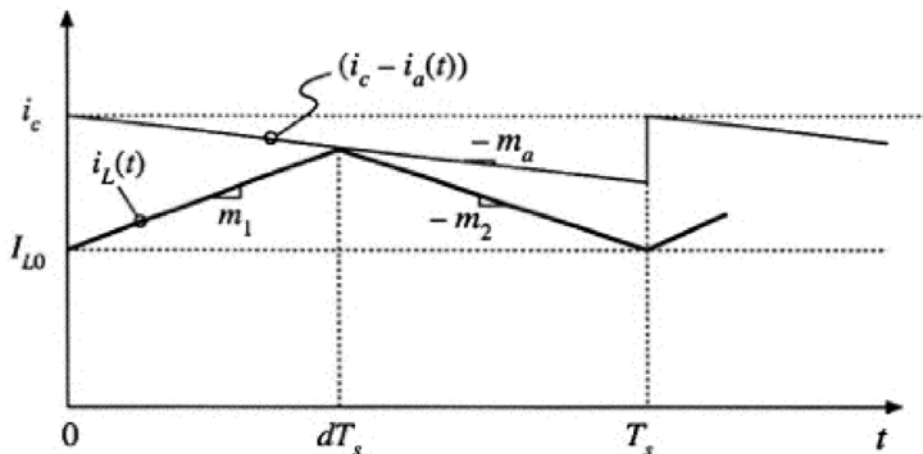


Figure 2.11: Current mode modulation with artificial ramp.

From functionality perspective, current mode control automatically has a short circuit protection built in. This is perhaps the most important reason why current mode control is preferred to voltage mode control.

To achieve certain dynamic performance in a system, voltage mode control can do exactly as well as current mode control, if the large signal stability is properly accounted for.

2.6 Digital modulation

To come back to the discussion of digital control, it is worth to have a look of the analog and digital modulation schemes shown in Figure 2.12. The following aspects need to be taken into considerations:

- a. DPWM is generated from a discrete command. It is a stable modulator in nature, partly because it is discrete and immune from the ripple, and partly because the quantization rejects small perturbations;
- b. Discrete current information will not be helpful in modulation. Over sampling current need additional high performance ADC, which is very costly;
- c. Digital PID compensation is more flexible than that in S-domain;
- d. Discrete current information will not be helpful in protection. A simple analog comparator can be easily added to the digital controller to provide over current protection;
- e. Multiple current sampling during PWM cycle requires very fast ADC. It is a huge waste of power and silicon.

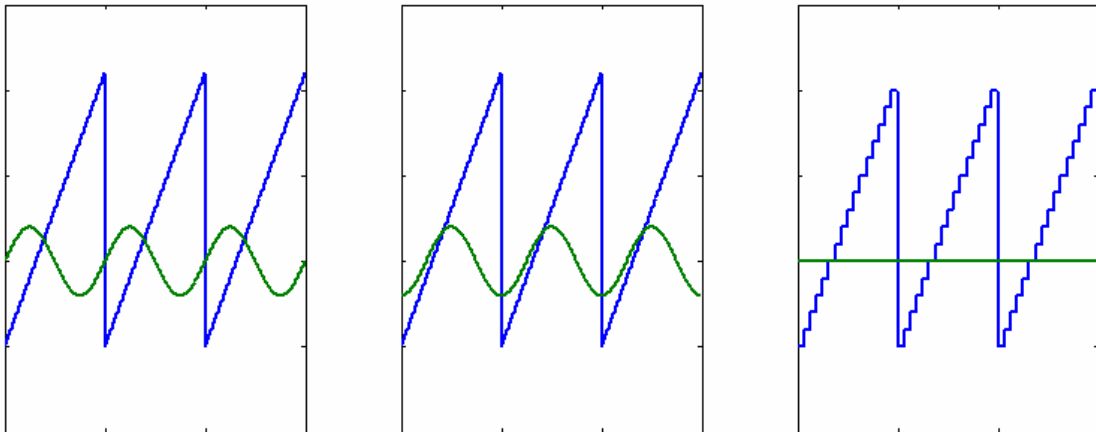


Figure 2.12: Analog modulation, analog modulation with phase shift and digital modulation.

In conclusion, the digital voltage mode control is a good choice in the design of the digital controller. Some vendors, like ADI, also noticed the unnecessary to implement digital current mode controllers [18].

Voltage mode control is simple and is well understood by the engineers. It is a good low cost design choice.

Chapter 3

DISCRETE MODEL AND CONTROL

Control design always comes before the circuit implementations. In digital control of power supplies, the mostly used control method is digital PID.

A buck converter without parasitic components is used as an example throughout this chapter. The ideal control to output transfers function in S-domain can be written as,

$$G_{vd} = \frac{V_{in}}{1 + \frac{L}{R}S + LCS^2}$$

3.1 Design by emulation

This is also known as digital redesign approach. In this method, an analog controller is first designed in the continuous domain as if one were building continuous time control system. However, the effects of sampling and hold associated with the ADC and the DPWM circuits cannot be totally ignored. They set an upper limit of the control bandwidth. To account for this, a Pade polynomial term will be inserted into the original transfer function.

The analog controller is then converted to a discrete-time compensator by some approximate techniques.

The conventional analog compensator can be lead, lag or PID in the S-domain. The sample and hold delay changes the pole positions a little bit, but the design method remains the same as in the analog controller design.

This transfer function is then digitized. With the Matlab control toolbox, this conversion can be easily done. Different transformation method may be used. They result in different controller coefficients, as each method has its own approximations and limitations. In general, the Tustin (bilinear) method is a safer transform. It tends to produce closer results between continuous system and discrete system.

3.2 Direct digital design

With the direct digital approach, the digital controller is designed in the discrete time domain based on a model of the plant already in the Z-domain. This transform takes the ZOH effect into account.

$$G(Z) = (1 - Z^{-1}) \mathfrak{Z} \left\{ \frac{G(S)}{S} \right\}$$

Once a discrete time approximation is obtained, the discrete time compensator is designed directly in the z-domain using methods similar to the continuous time frequency response method or root locus method. This has the advantage that the poles and zeros of the digital controllers are located directly, resulting in a better load transient response, as well as better phase margin and bandwidth for the closed loop operation of the power converter.

3.3 Discrete modeling

Unfortunately, the previous two design approaches are based on S-domain transfer functions. Both of them suffer from the approximations made in the transformation, which limit the bandwidth that can be possibly achieved. Power converter control is discrete in nature. Some designers obtained another model based on the approximations in [19]. This open loop transfer function exhibits -360 degree phase shift at half of the switching frequency, as shown in Fig. 3.1. It is counter intuition, because buck should only have 180 degree phase shift at half of the switching frequency without ESR.

$$G_{vd}(Z) = \frac{(T_s^2 / LC)V_g}{Z^2 - (2 - T_s / LC)Z + (1 + T_s^2 / LC - T_s / RC)}$$

A more general approach to derive the discrete transfer function is presented. This method essentially used the same technique in Chapter 2.

The system differential equations are:

$$\frac{d}{dt} \begin{pmatrix} v(t) \\ i(t) \end{pmatrix} = \begin{pmatrix} -1/(RC) & 1/C \\ -1/L & 0 \end{pmatrix} \begin{pmatrix} v(t) \\ i(t) \end{pmatrix} + \begin{pmatrix} 0 \\ V_{in}/L \end{pmatrix} q(t)$$

The system is represented in discrete state space form:

$$X(kT + T) = \Gamma_1 + e^{A_1(1-d_k)T} \left(e^{A_0 d_k T} X(kT) + \Gamma_0 \right)$$

where

$$A_0 = A_1 = A$$

$$\Gamma_0 = \int_0^{d_k T} e^{A_0 t} B_0 V_{in} dt$$

$$\Gamma_1 = \int_0^{(1-d_k)T} e^{A_1 t} B_1 V_{in} dt = 0 \quad (\text{buck})$$

Since the first item on the right side is zero, the equation can be simplified as,

$$X(kT+T) = e^{A_1(1-d_k)T} \left(e^{A_0 d_k T} X(kT) + \Gamma_0 \right)$$

$$\begin{aligned} X_{[k+1]} &= e^{AT} X_{[k]} + e^{AT} \int_0^T e^{-A\tau} B V_{in} d\tau \\ &= e^{AT} X_{[k]} - e^{AT} A^{-1} (e^{-AdT} - I) B V_{in} \\ &= e^{AT} X_{[k]} + A^{-1} (e^{AT} - e^{A(1-d)T}) B V_{in} \end{aligned}$$

where $e^{AT} = I + AT + \frac{1}{2}A^2T^2 + \frac{1}{3!}A^3T^3 + \dots$, ignore the high order items,

$$X_{[k+1]} \approx e^{AT} X_{[k]} + B V_{in} d$$

Therefore, the transfer function can be obtained:

$$\frac{X(z)}{d(z)} = (zI - e^{AT})^{-1} B V_{in}$$

Another method is based on time domain differential equation solution.

$$\begin{aligned} \begin{pmatrix} v(t) \\ i(t) \end{pmatrix} &= e^{-k(t-t_0)} \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \cos(\omega(t-t_0)) \\ &+ \begin{pmatrix} -k/\omega & 1/(Cw) \\ -1/(L\omega) & k/\omega \end{pmatrix} \sin(\omega(t-t_0)) \end{aligned} \left[\begin{pmatrix} v(t) \\ i(t) \end{pmatrix} - V_{in} \begin{pmatrix} 1 \\ 1/R \end{pmatrix} q(t) \right] + V_{in} \begin{pmatrix} 1 \\ 1/R \end{pmatrix} q(t)$$

where $k = 1/(2RC)$ and $\omega = \sqrt{1/(LC) - k^2}$.

After some math manipulations and Taylor series expansion, the following result can be obtained:

$$\frac{V(z)}{d(z)} = \frac{e^{\frac{T}{\tau}} \sin(\omega T) T V_{in} Z}{\left(Z^2 - 2e^{\frac{T}{\tau}} \cos(\omega T) Z + \left(e^{\frac{T}{\tau}} \right)^2 \cos^2(\omega T) - \frac{\left(e^{\frac{T}{\tau}} \right)^2 \sin^2(\omega T)}{\omega^2 \tau^2} + \frac{\left(e^{\frac{T}{\tau}} \right)^2 \sin^2(\omega T)}{\omega^2 CL} \right) \omega CL}$$

Comparing the bode plots of the old model and the new model in Figure 3.1, one can easily observe the difference in phase in high frequency region. The phase response makes more sense in the new model.

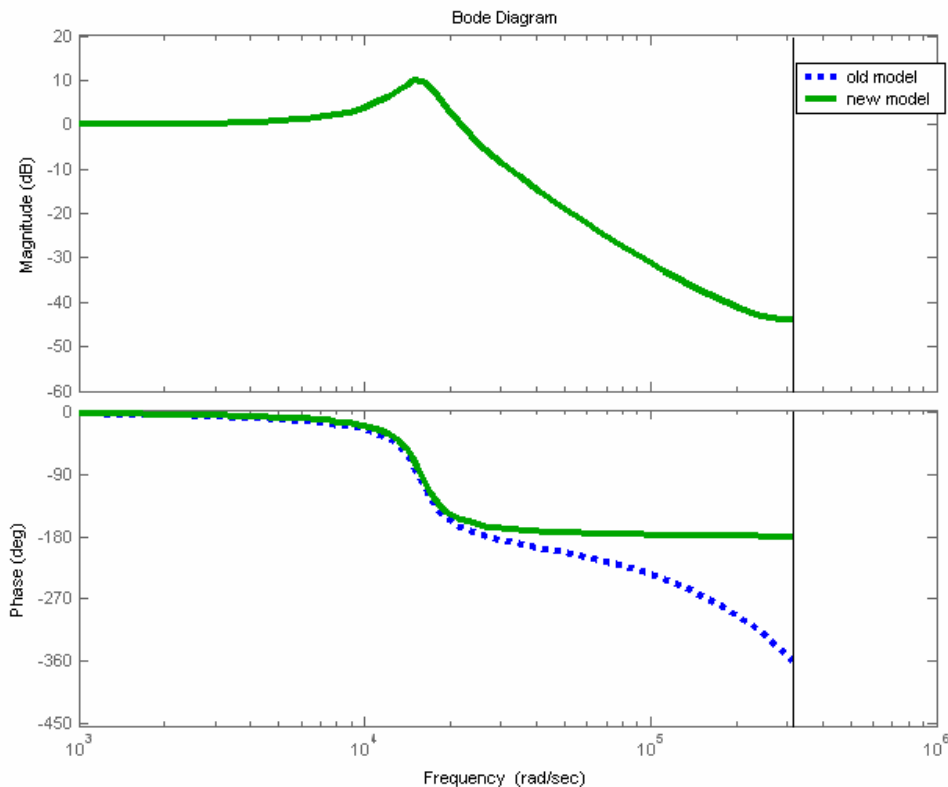


Figure 3.1: Bode plot comparison between old model and new model.

3.4 Notes on design implementation

The PID compensator could be very complex, if the real difference function is implemented, because every single coefficient needs a relatively high resolution multiplier. The multipliers would certainly limit the operating speed and they cost a lot of area.

Common practice is to build look up tables (LUT) by pre-calculating the results. The LUT diagram is shown in Figure 3.2.

In analog compensation design, the compensator transfer function is obtained by wrapping RC components around opamp and it is difficult to realize a double pole or zero with merely RC. But in digital domain, it is quite simple. Just change the coefficients will do the job. And it costs no extra hardware.

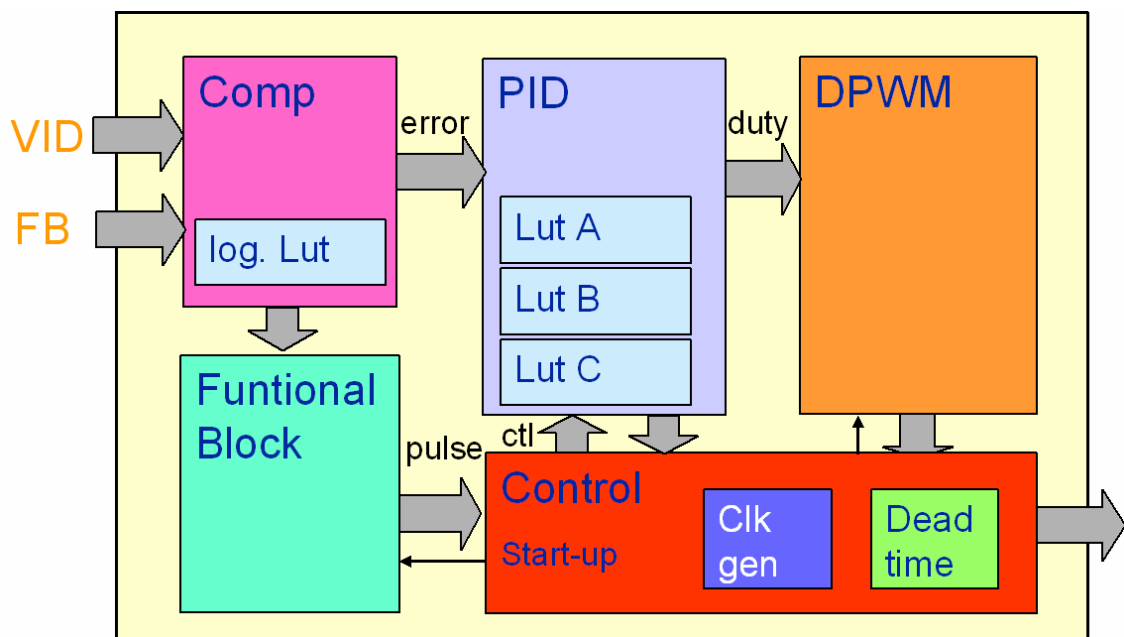


Figure 3.2: Typical LUT diagram in the digital controller.

Chapter 4

MIXED SIGNAL VERIFICATION AND EXPERIMENTS

Digitally controlled power converters are mixed signal system. Mixed signal simulation is therefore required to increase the productivity.

While designing mixed signal circuits, modern simulation tool, like SpectreVerilog, is very helpful as it allows both digital and analog circuits to be described in a way that is most suitable for each type of circuit. With digital circuits, either gate or behavioral level Verilog-HDL is used, and with analog circuits, either transistor or behavioral level Verilog-A is used. The tool combines the two parts of the circuit smoothly during the simulation. Moreover, both analog and digital designers can design with languages that are familiar and comfortable for them, and yet they can still work together.

To design such a mixed signal system, two design methodologies are often used. One is Top-down design; the other is Bottom-Up. Top-down design is a design methodology that is useful when designing large complex systems. The starting point is to design and verify the system at an abstract or 'block diagram' level. The detailed design of the individual blocks is started after that. Top-down design would be used in lieu of the more traditional approach referred to as bottom-up design. In bottom-up design, one fully designs the individual blocks before focusing on the design of the block diagram of the system. Bottom-up design

generally requires that the individual blocks be over designed so that when connected together to form the system there is enough margin to overcome unexpected problems. The big risk being that the required system performance might not be achievable with the blocks as designed, meaning that one or more blocks would have to be re-designed.

With top-down design, the individual block performance needed to meet the overall system performance requirements is carefully studied and understood before the blocks are developed. This reduces the need for over design in the individual blocks, but at the risk that the anticipated performance for one or more blocks is unachievable, which would require that the system design be revisited.

Clearly, to reduce the expense and time required for rework, there must be extensive communication between the system and block level designers. Fortunately, power converter controller is simple enough for a single designer to handle.

4.1 Bottom-Up Design

The traditional approach to design is referred to as bottom-up design. In it, the design process starts with the design of the individual blocks, which are then combined to form the system. The design of the blocks starts with a set of specifications and ends with a transistor level implementation. Each block is verified as a stand-alone unit against specifications and not in the context of the overall system. Once verified individually, the blocks are then combined and verified together, but at this point the entire system is represented at the transistor level.

The problems with this approach are:

- a. Once the blocks are combined, simulation takes a long time and verification becomes difficult.
- b. The close loop system performance is hard to predict.
- c. When there is architectural change, a lot of redesign needs to be done.
- d. It is difficult to communicate between each other, if more than one designer is involved.

Therefore, it is not very effective and efficient.

4.2 Moving to Top-Down Design

In order to address these challenges, many design teams are either looking to, or else have already implemented, a top-down design methodology. In a primitive top-down approach, the architecture of the chip is defined as a block diagram and simulated and optimized using a system simulator such as Simulink or SpectreVerilog. From the high-level simulation, requirements for the individual circuit blocks are derived. Circuits are then designed individually to meet these specifications. Finally, the entire chip is laid out and verified against the original requirements.

4.3 Digitally controlled power converter mixed mode simulation steps

This chapter is a cookbook that walks the readers through the simulation steps. It also serves the purpose to verifying our design and discussion in the previous two chapters.

The library name is *'DigitalPower'*. It contains a Verilog file, a Verilog-A file and a config schematic file. The Verilog file *'dctrl'* represents the digital compensator and DPWM.

The Verilog-A file 'ad7' is the description of A/D converter. The config file 'dpsys' is the whole system schematic.

All important aspects of integrated circuit design are discussed, such as digital hardware modeling in Verilog, analog hardware modeling in Verilog-A, schematic entry, simulation, logic synthesis, layout implementation.

This simulation should be run under Cadence mixed signal environment. Use 'icms' or 'msfb' to open the Command Interpreter Window (CIW).

4.3.1 Verilog entry

This section describes how to enter a behavioral (Register Transfer Level) description of a digital cell into the database. The cell is described in the Verilog language.

In the library manager, select library 'DigitalPower', which has been already setup and attached to a certain technology profile by the designer, and next click **File -> New -> Cell View ...** and fill out the Create New File window as follows:

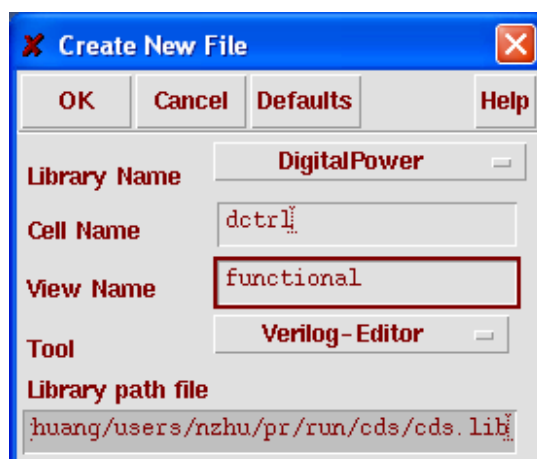
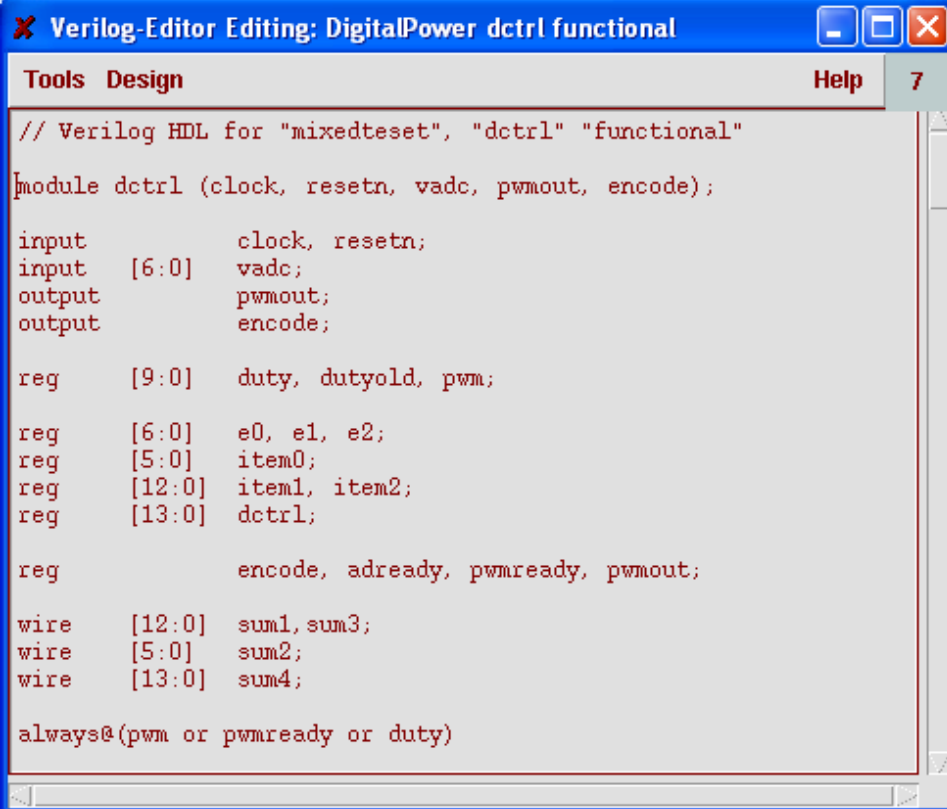


Figure 4.1: Mixed mode simulation screen capture 1.

Click on OK and edit the Verilog file or copy from the source code, which describe the function of the compensator and DPWM part behaviorally.



```
Verilog-Editor Editing: DigitalPower dctrl functional
Tools Design Help 7
// Verilog HDL for "mixeddteset", "dctrl" "functional"
module dctrl (clock, resetn, vadc, pwmout, encode);
input      clock, resetn;
input [6:0] vadc;
output     pwmout;
output     encode;

reg [9:0]  duty, dutyold, pwm;

reg [6:0]  e0, e1, e2;
reg [5:0]  item0;
reg [12:0] item1, item2;
reg [13:0] dctrl;

reg      encode, adready, pwmready, pwmout;

wire [12:0] sum1, sum3;
wire [5:0]  sum2;
wire [13:0] sum4;

always@(pwm or pwmready or duty)
```

Figure 4.2: Mixed mode simulation screen capture 2.

When you check and save the description, it will be checked on a correct syntax. If something is wrong, you will be notified that there is HDL parse error and you will be offered the opportunity to watch the errors and edit the description again. If you save the description and the syntax is ok, you will be informed that symbol '*dctrl*' does not exist, and you will be asked if it should be created. Click **Yes**.

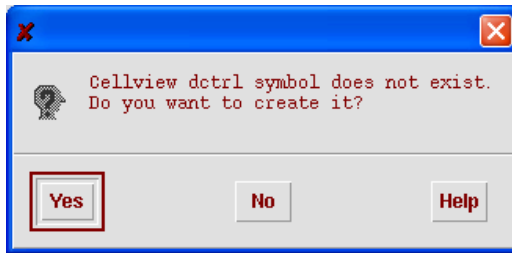


Figure 4.3: Mixed mode simulation screen capture 3.

A symbol view will be created for *'dctrl'* that you can watch by clicking in the library manager on library *'DigitalPower'*, next on cell *'dctrl'*, and next (two times) on view symbol. A Virtuoso window will open that shows the symbol view of *'dctrl'*. The symbol view will be used to represent the *'dctrl'* cell as an instance in another cell.

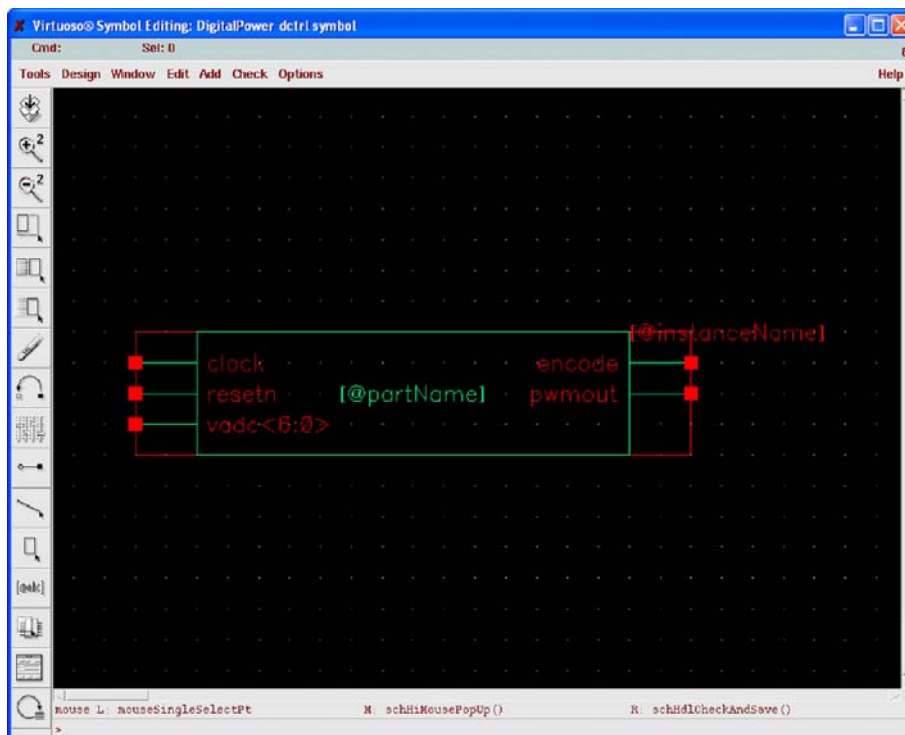


Figure 4.4: Mixed mode simulation screen capture 4.

Close the window by clicking **Window -> Close**.

This step could also be done by the Cadence import Verilog facility.

4.3.2 Verilog-A entry

This section describes how to enter a behavioral description of an analog cell into the database. The cell is described in the Verilog-A language. The procedure is much the same as when entering a behavioral description of a digital cell.

In the library manager, click **File -> New -> Cell View ...** and fill out the Create New File window as follows:

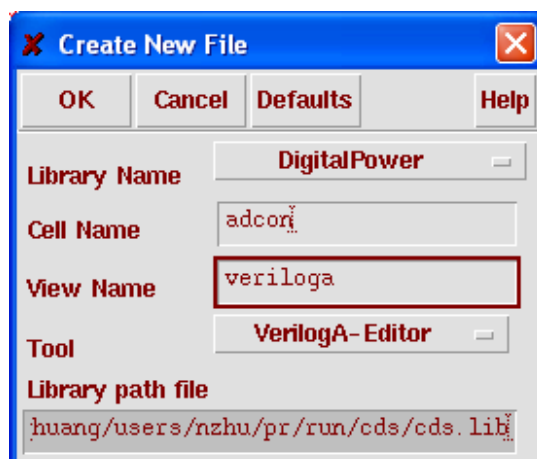


Figure 4.5: Mixed mode simulation screen capture 5.

Click on **OK**. Next you will be asked if you would like to use Modelwriter to create the new cell view. Modelwriter is a tool to automatically generate a Verilog-A description of a component from a predefined library by specifying a set of parameters.

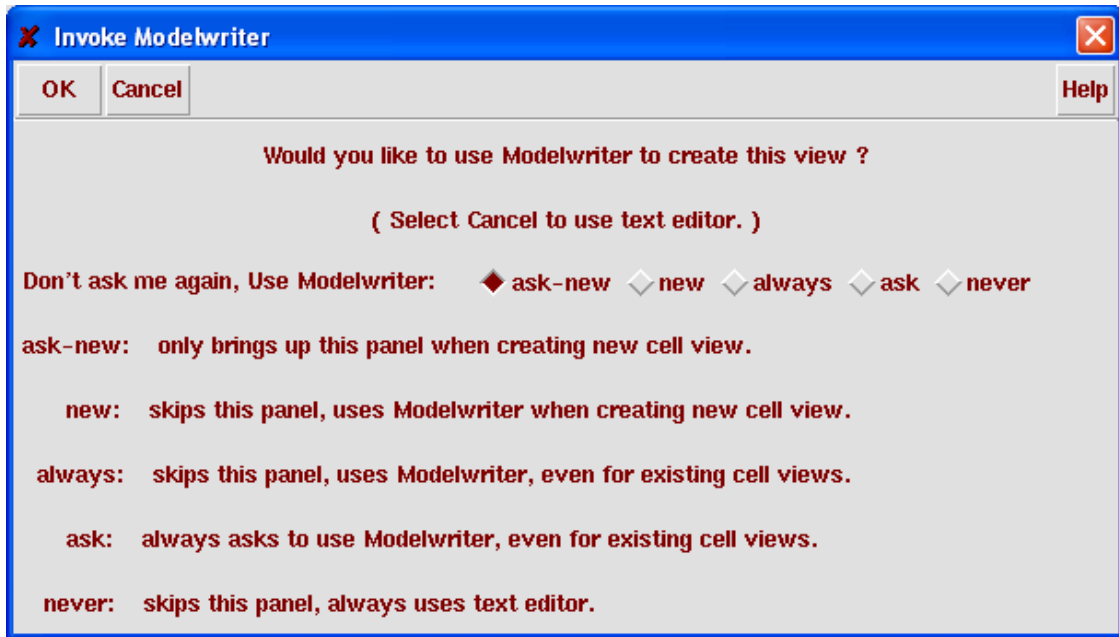
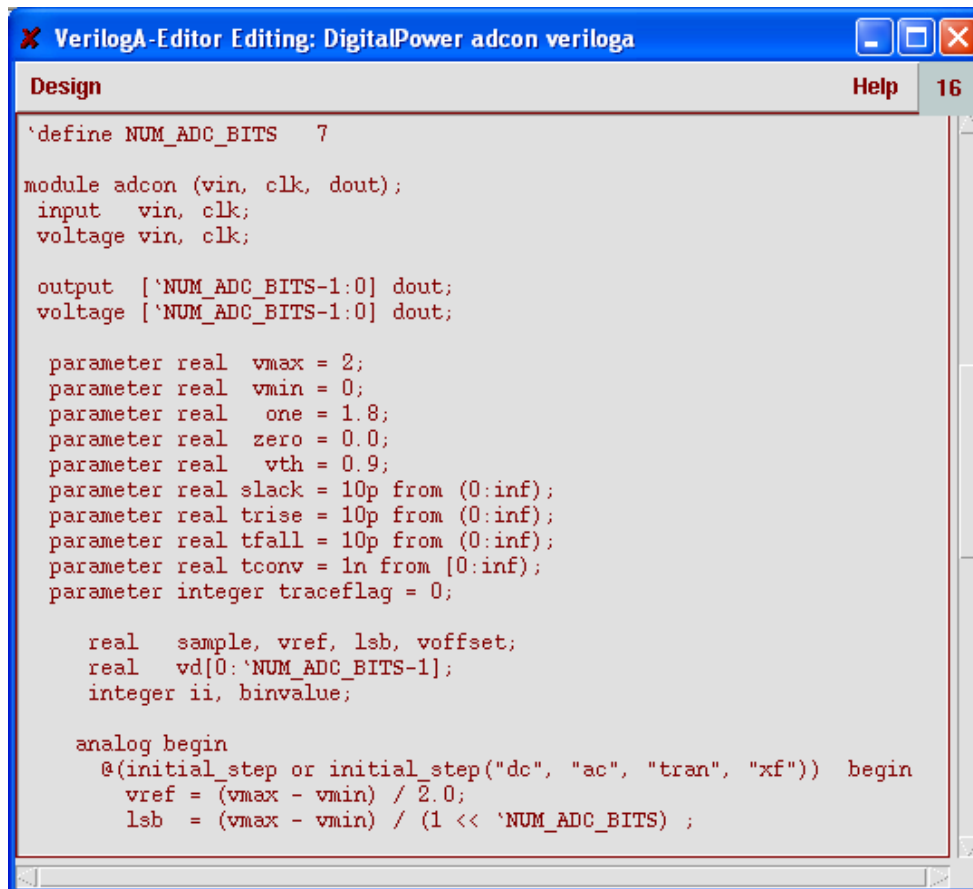


Figure 4.6: Mixed mode simulation screen capture 6.

For a short illustration, see the end of this section. In our case we will create the Verilog-A description ourselves, so therefore click on **Cancel**.

In the text window that appears, specify the Verilog-A behavioral description of the AD converter.



```
VerilogA-Editor Editing: DigitalPower adcon veriloga
Design Help 16
`define NUM_ADC_BITS 7
module adcon (vin, clk, dout);
input  vin, clk;
voltage vin, clk;

output  [`NUM_ADC_BITS-1:0] dout;
voltage [`NUM_ADC_BITS-1:0] dout;

parameter real  vmax = 2;
parameter real  vmin = 0;
parameter real  one = 1.8;
parameter real  zero = 0.0;
parameter real  vth = 0.9;
parameter real  slack = 10p from (0:inf);
parameter real  trise = 10p from (0:inf);
parameter real  tfall = 10p from (0:inf);
parameter real  tconv = 1n from (0:inf);
parameter integer traceflag = 0;

real  sample, vref, lsb, voffset;
real  vd[0:`NUM_ADC_BITS-1];
integer ii, binvalue;

analog begin
  @(initial_step or initial_step("dc", "ac", "tran", "xf")) begin
    vref = (vmax - vmin) / 2.0;
    lsb = (vmax - vmin) / (1 << `NUM_ADC_BITS) ;
  end
end
```

Figure 4.7: Mixed mode simulation screen capture 7.

After saving this description you will be informed that ‘*daconv*’ symbol does not exist, and you will be asked if it should be created. Click **Yes**.

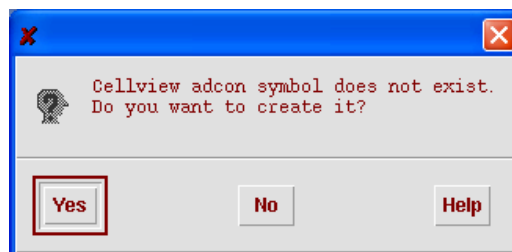


Figure 4.8: Mixed mode simulation screen capture 8.

In this case you will be offered a window to specify Symbol Generation Options. Specify the options as follows:

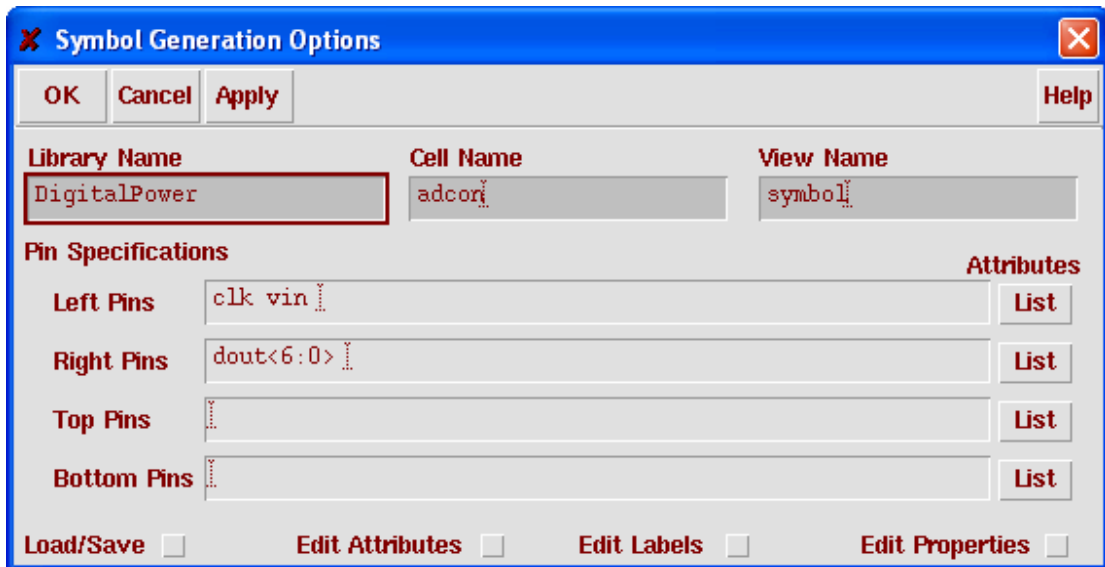


Figure 4.9: Mixed mode simulation screen capture 9.

Click on the **List** button behind the lines where you specify the pin names, to obtain a window for specifying the pin attributes. Specify a direction for input and output. Usually, the inputs are placed on the left and the outputs are placed on the right.

Next, when you click **OK** the symbol will be generated. When you open the symbol view from the library manager, it will look as follows:

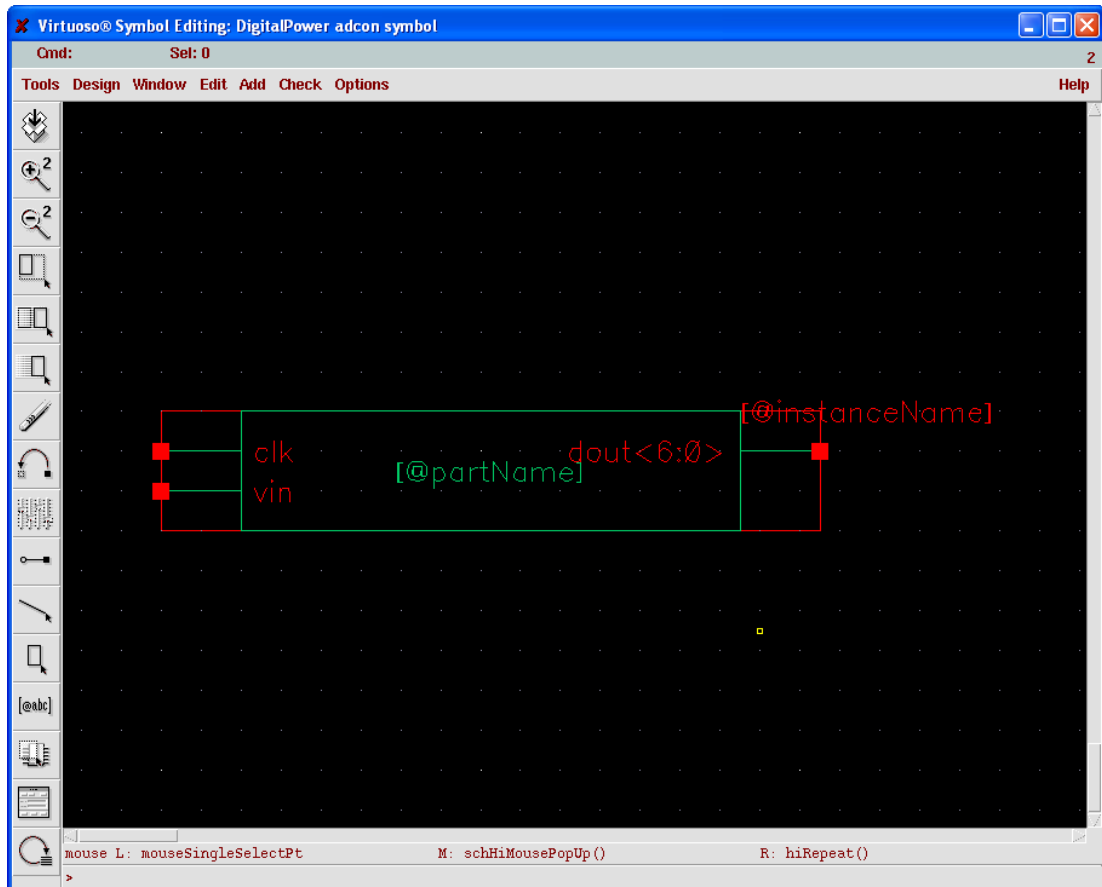


Figure 4.10: Mixed mode simulation screen capture 10.

4.3.3 Using Modelwriter

The Modelwriter can be used after clicking **File -> New -> Cell View ...** and specified as tool the Verilog-A editor (see above), or it can be executed from the terminal window as a stand-alone tool:

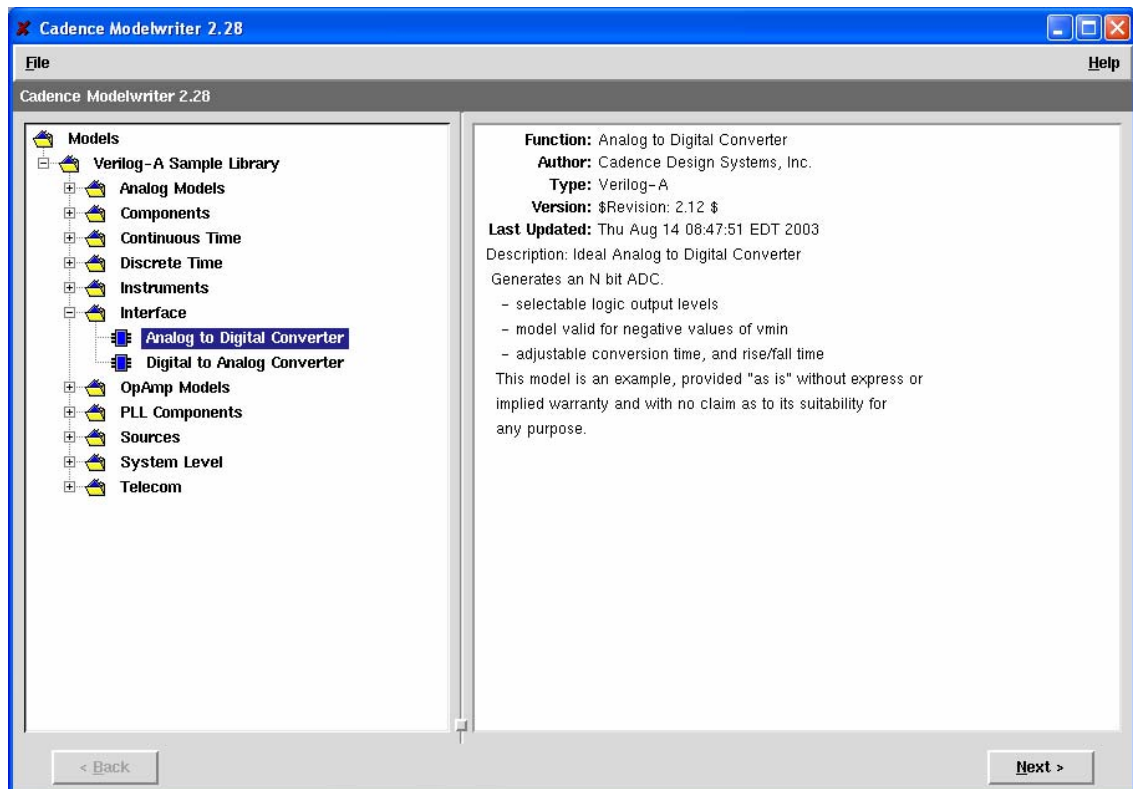


Figure 4.11: Mixed mode simulation screen capture 11.

When you use Modelwriter, you first select the type of component from the library. There are lots of commonly used Verilog-A models are ready to use in the model writer. Therefore, the designers do not have to write the codes themselves.

Next, specify the parameters for the component.

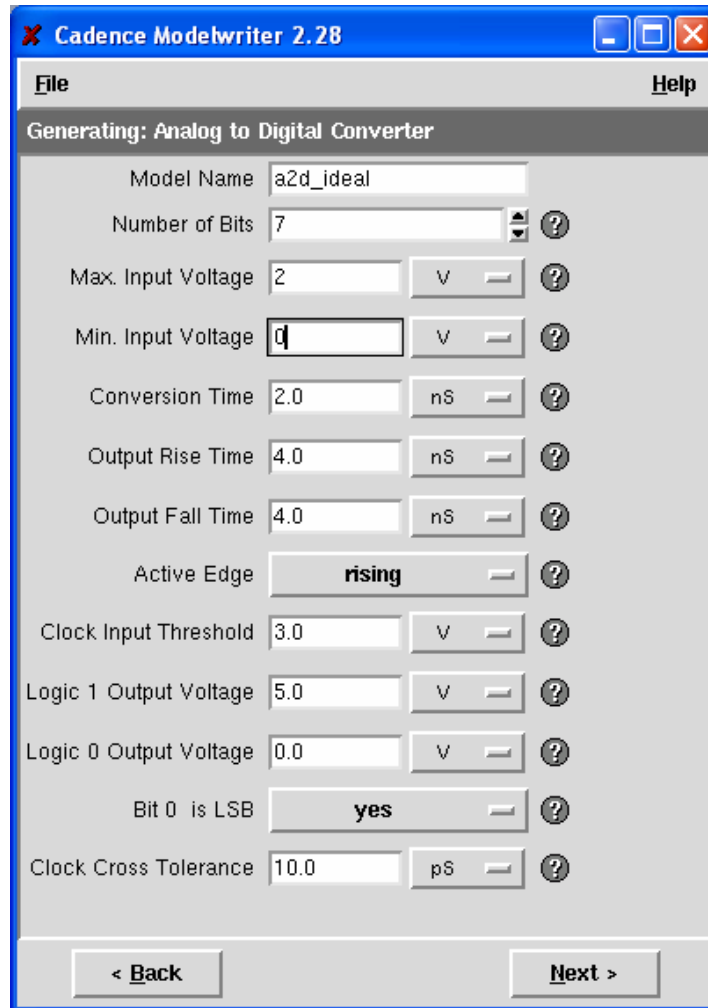


Figure 4.12: Mixed mode simulation screen capture 12.

Then, the Verilog-A code will be generated, which you can save into the database if you have started Modelwriter from the New File window in Cadence, or into a file if you started Modelwriter stand-alone.

4.3.4 Schematic Entry

The whole system schematic can then be easily generated.

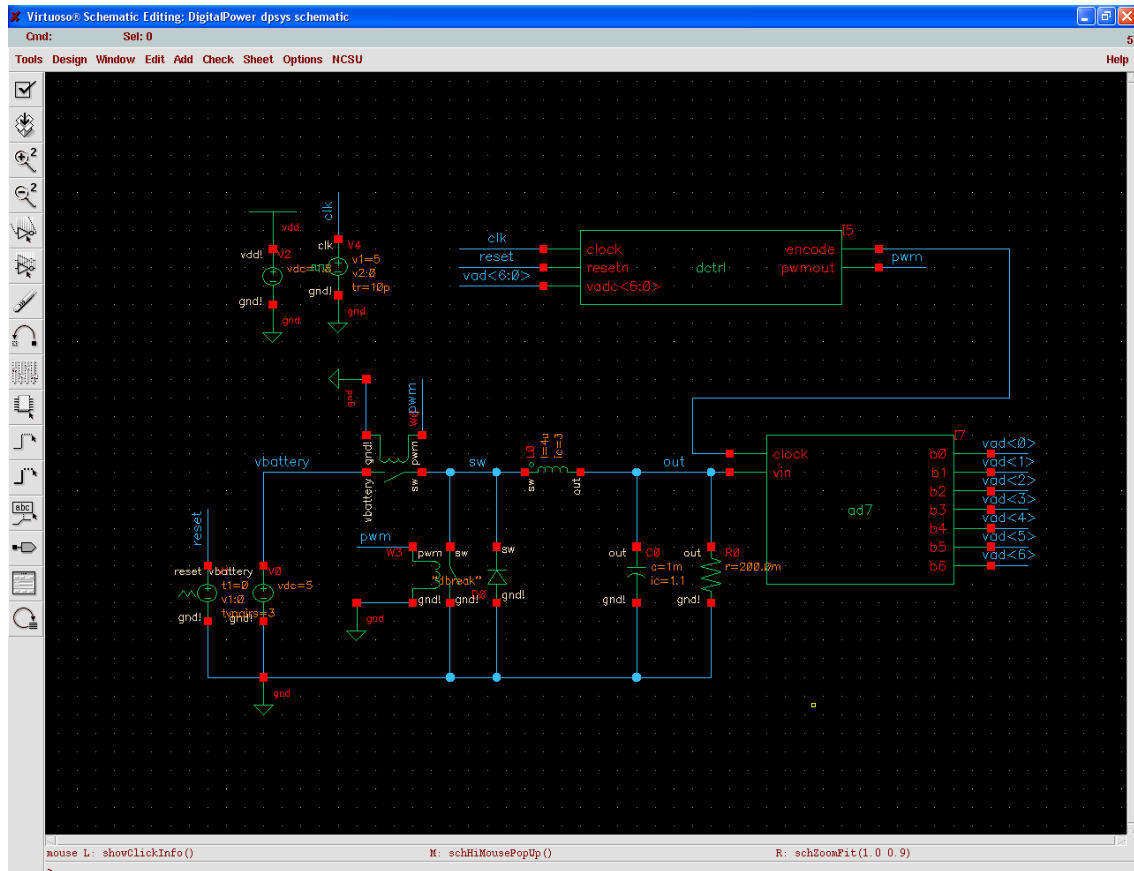


Figure 4.13: Mixed mode simulation screen capture 13.

First, a config view for simulation has to be simulated.

Besides a schematic view for cell 'dpsys' circuit we will create a so-called config view for cell 'dpsys' in which we can specify for each instance which view should actually be used for simulation.

To create a config view for cell 'dpsys', in the library manager, select library 'DigitalPower' and click on **File -> New -> Cell View**. In the Create New File form, use 'DigitalPower' for Library Name, 'dpsys' for Cell Name, and Hierarchy-Editor for Tool. Notice that automatically for View Name config will be filled in.

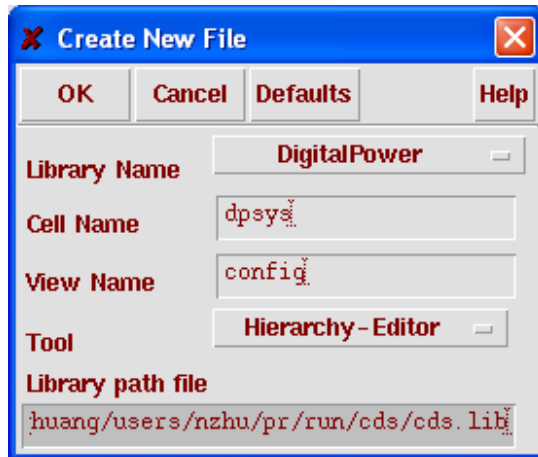


Figure 4.14: Mixed mode simulation screen capture 14.

After clicking **OK**, the Hierarchy Editor window will appear with the New Configuration window on top of it. In the New Configuration window, for View in the Top Cell field, specify schematic and next click on **Use Template....** and choose spectreVerilog for Name and click on **OK**. The New Configuration window will then look as follows.

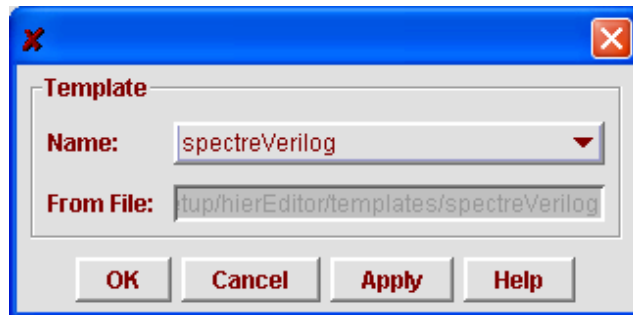


Figure 4.15: Mixed mode simulation screen capture 15.

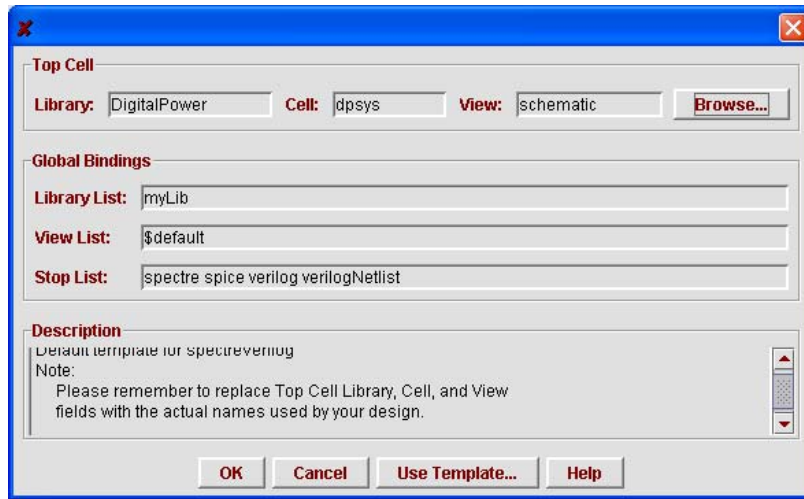


Figure 4.16: Mixed mode simulation screen capture 16.

Click on **OK** and the Hierarchy Editor will show the following contents:

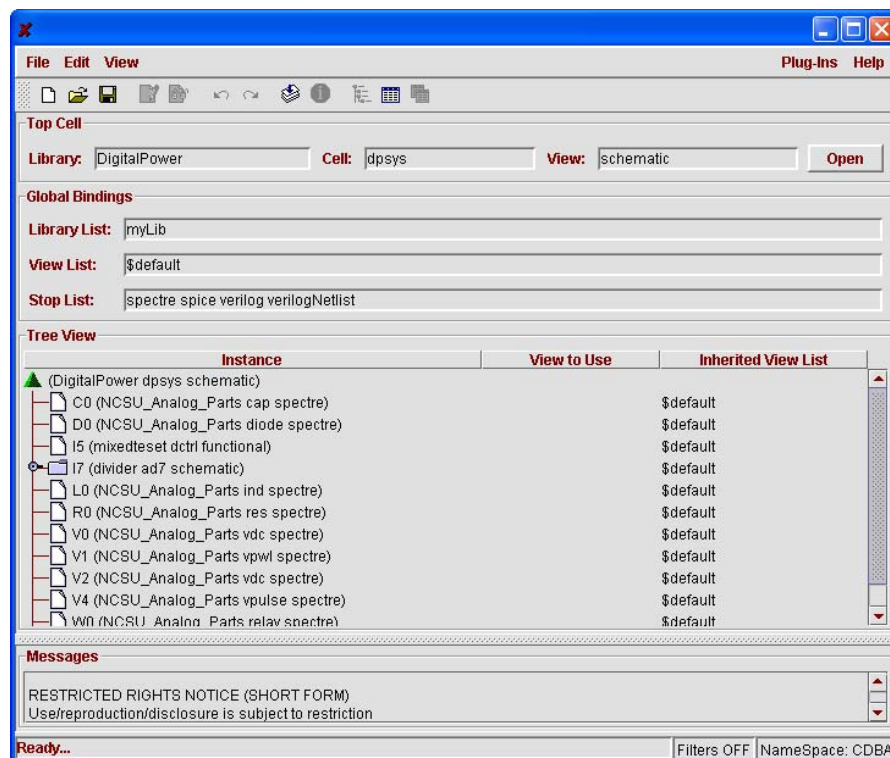


Figure 4.17: Mixed mode simulation screen capture 17.

The window lists the cells that are present in the '*dpsys*' cell hierarchy and the views that are found and used for these cells. Alternatively, the instances can be displayed in a more hierarchical way in the Hierarchy Editor. Therefore, click on **View -> Tree**. Choose which form you find is more convenient. Next, click on **File -> Save** to save the information.

In the Hierarchy Editor window, in the section Top Cell, click on **Open**. A Composer window will appear for the schematic view of the '*dpsys*' cell. In the title bar of the window, it is printed that this schematic view is connected to a config view.

If you do not have the Hierarchy Editor window open, you can open the schematic view (and the config view) by double clicking on the config view in the library manager.

4.3.5 Starting the simulation setup

The simulation interface is started from the '*dpsys*' schematic window using **Tools -> Analog Environment**. In our case we will be performing a mixed-level simulation (electrical components are mixed with Verilog and Verilog-A descriptions), so we will use the spectreVerilog simulator. Therefore, in the Analog Environment window, click on **Setup -> Simulator/Directory/Host...** and select for Simulator spectreVerilog. In case a netlist is simulated with only electrical components, use the spectre simulator. Note that in order to use the spectreVerilog simulator, the schematic view that is simulated must be opened from a config view (as is the case here). The window will then look as follows:

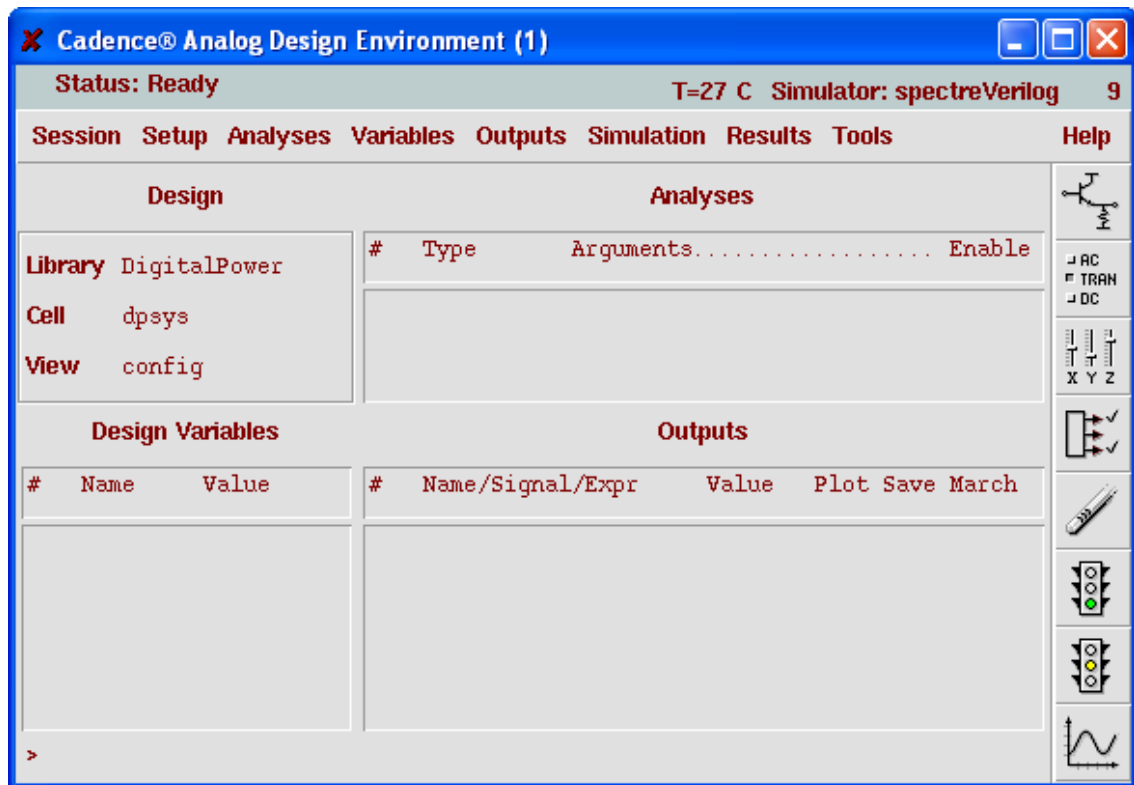


Figure 4.18: Mixed mode simulation screen capture 18.

4.3.6 Defining D/A and A/D conversion information

We will be performing a mixed-level simulation in which a part of the schematic is described at the digital level (*'dctrl'*), and a part of the schematic is described at the analog level (*'adcon'*). To convert digital signals to analog signals, and vice versa, some parameters need to be specified. These parameters can be specified using the menu **Mixed-Signal -> Interface Elements** in the schematic window. To e.g. specify the default conversion information for the complete library, click **Mixed-Signal -> Interface Elements -> Library**. The IE Model Property Editor window will appear. For Model IO set to input and output, the window will respectively look as follows:

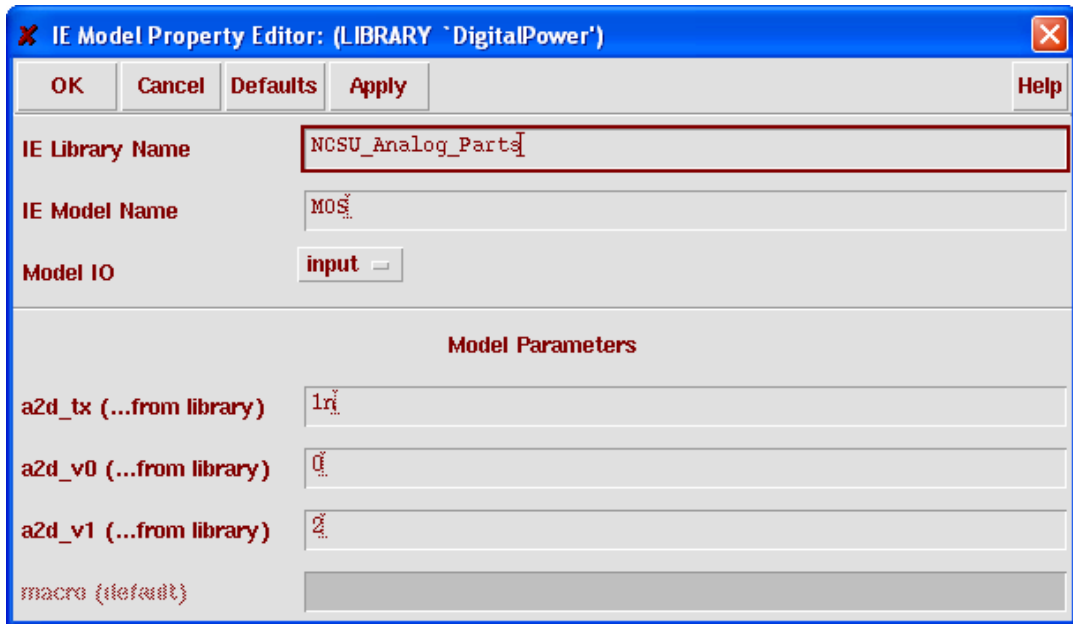


Figure 4.19: Mixed mode simulation screen capture 19.

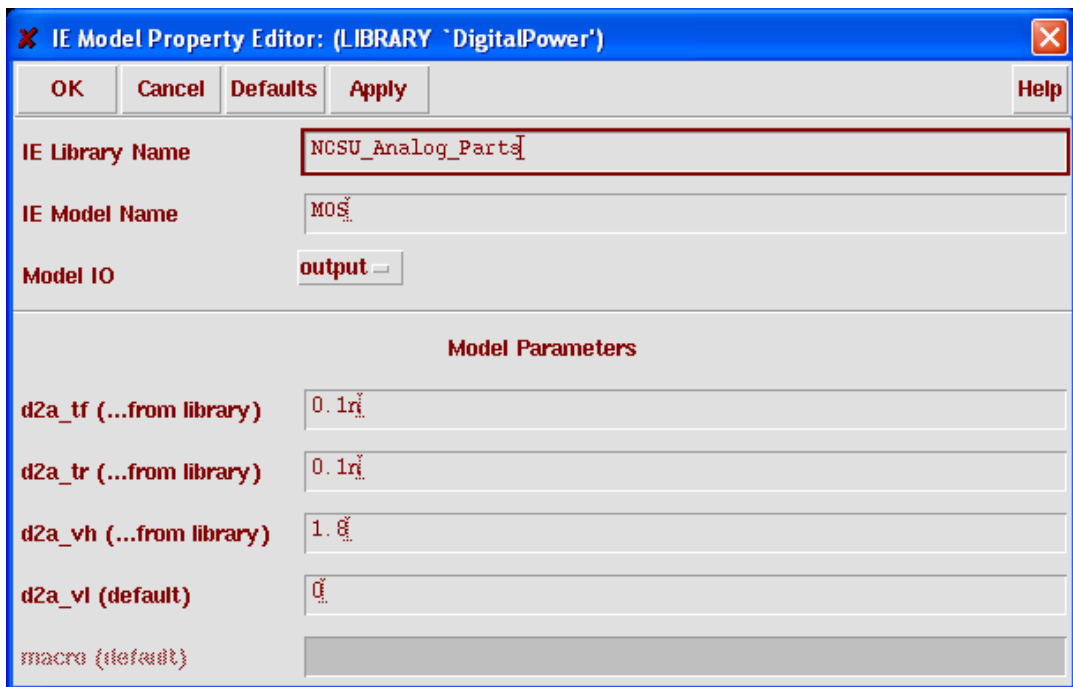


Figure 4.20: Mixed mode simulation screen capture 20.

4.3.7 Debugging simulation and verification

After the previous step, mixed mode simulation can be started.

Since there are behavioral Verilog blocks in the simulation, it is important that the digital portion is traceable. Ensure to select Simvision Debugger in the Simulation Options.

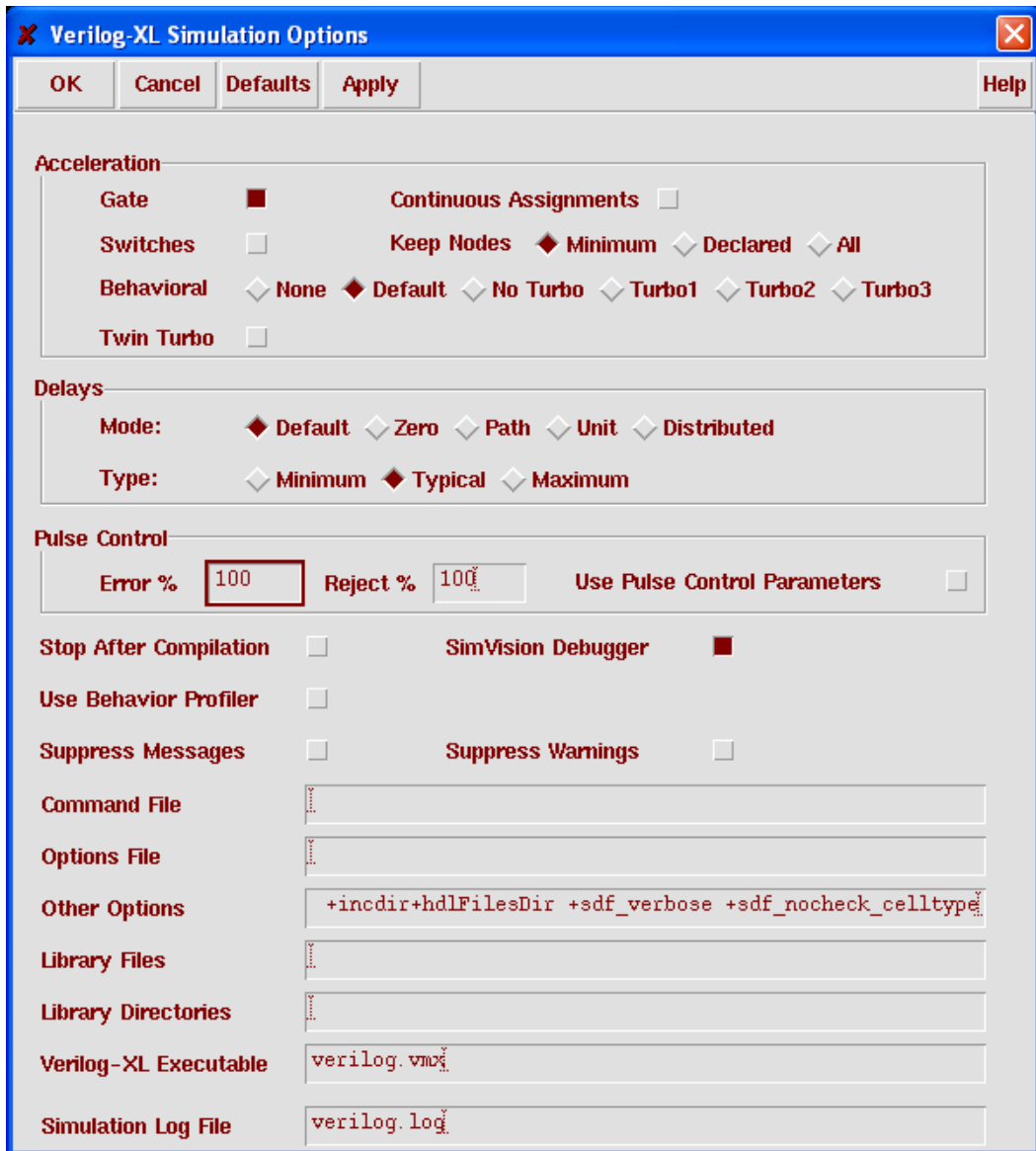


Figure 4.21: Mixed mode simulation screen capture 21.

When simulation result is correct, the digital Verilog can be synthesized by Synopsys and run through the Place&Route flow. Post-layout simulation can be preformed then to verify to design.

4.4 Design, simulation and experimental example

In the design example, the power stage parameters are: $f_s = 100\text{KHz}$, $L = 4\mu\text{H}$, $C = 1000\mu\text{F}$, $R = 0.2\Omega$, $V_{in} = 5\text{V}$ and $V_o = 1\text{V}$.

DPWM is the easiest block to simulate behaviorally. Although there are many papers discussing the circuit implementation of DWPM, the circuit level discussion of DPWM is out of the scope of this thesis. In this high level simulation, it can be well represented by a counter. To be realistic, the resolution of the counter is 10 bit. That means 100MHz system frequency, which is not too fast. Since ideal switches are used, the dead time is set to 0.

The other part described in the behavioral Verilog file is the controller itself. In voltage mode control, the linear PID control law is in the following form:

$$d_{control} = d_0 + a_0e_0 + a_1e_1 + a_2e_2$$

Figure 3.2 is redrawn here in Figure 4.22, where FB is the output of the ADC and VID is simply a reference value. The control parameters a_i are designed based on the model developed in the previous chapter. The multipliers are avoided by using LUTs. The product of a_0e_0 is stored in LUT A, a_1e_1 in LUT B and a_2e_2 in LUT C.

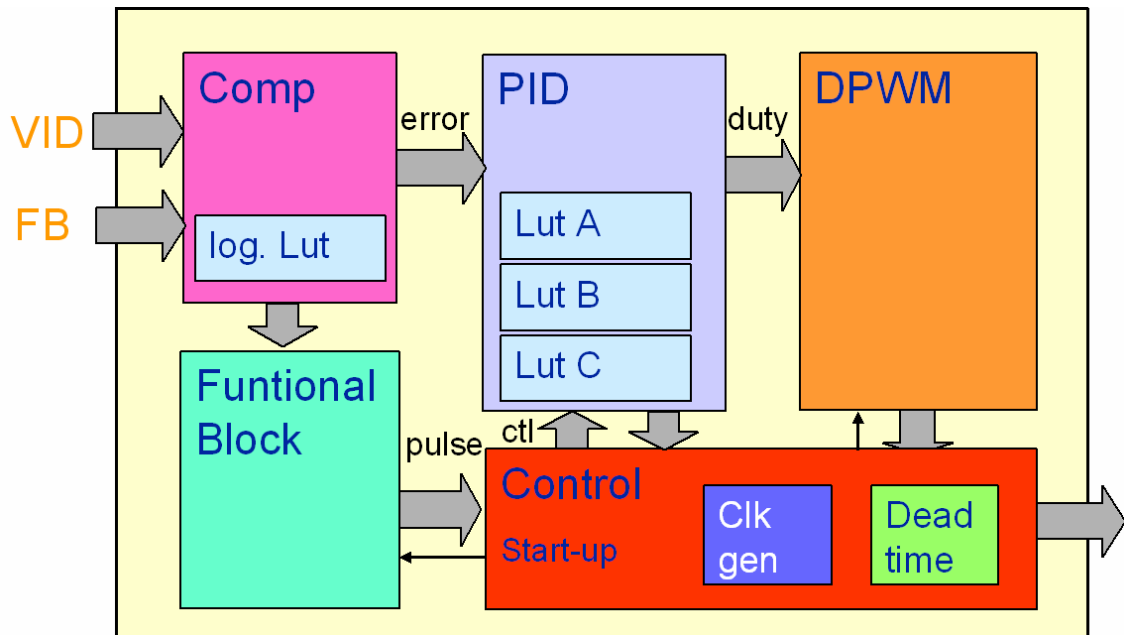


Figure 4.22: Typical LUT diagram in the digital controller.

The resolution is as important. The voltage error should be low enough to avoid limit cycle oscillation [20],

$$\Delta V_{ADC} < \Delta V_{DPWM} = V_{in} / N_{counter}$$

Meanwhile, it should be high enough to avoid slow response of the control. Here, the ADC resolution is 16mV.

Mixed mode simulation waveforms are shown in Figure 4.23. The output voltage increases from an initial point to the steady state final value. The output voltage rapidly approaches to the final value. It takes longer time to reach zero error point. The inductor current waveform exhibits typical second order behavior. But the waveform is not very smooth. This is also the typical quantization effect in digital controller. The longer response

time is the combination of the three factors: digital quantization, very low resolution of ADC and large output capacitance.

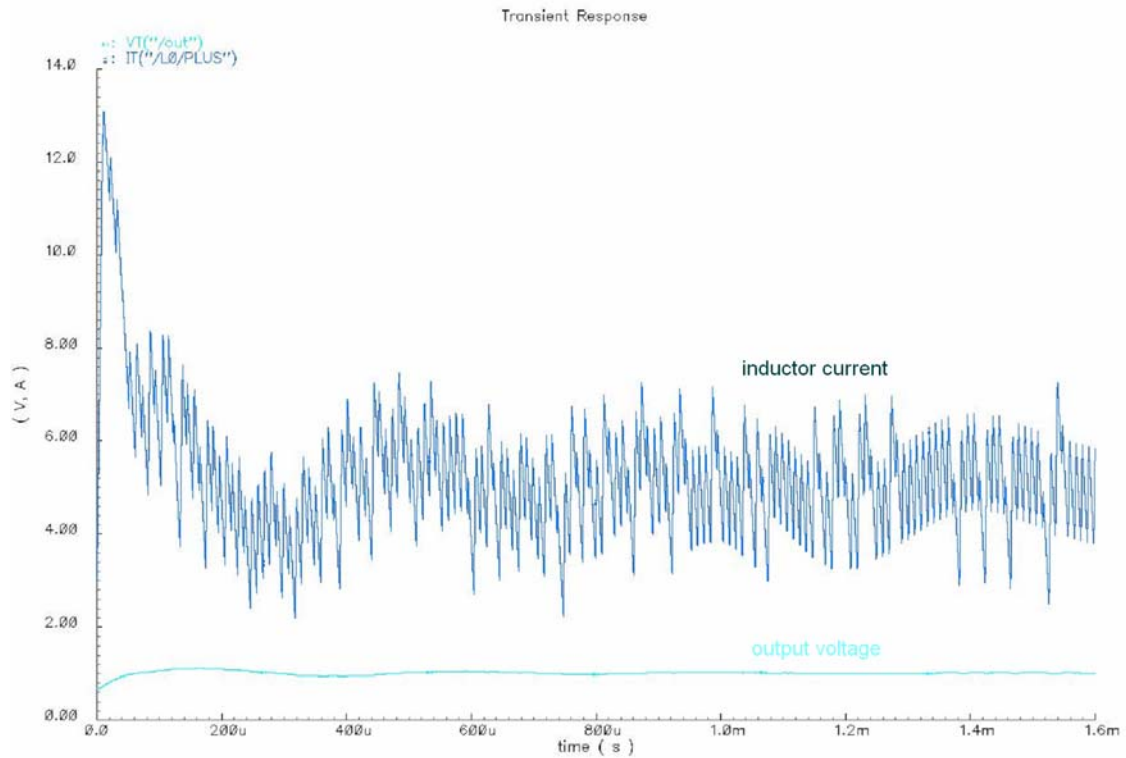


Figure 4.23: Simulation of the transition from detection mode to normal operation.

Figure 4.24 shows the Simvision digital waveforms from the same simulation. It supports the above discussion. At the time around 1.4ms, all the three error signals are close to 40, which is the target value. One bit change results in big duty variation. It reflects large gain and low resolution in the system.

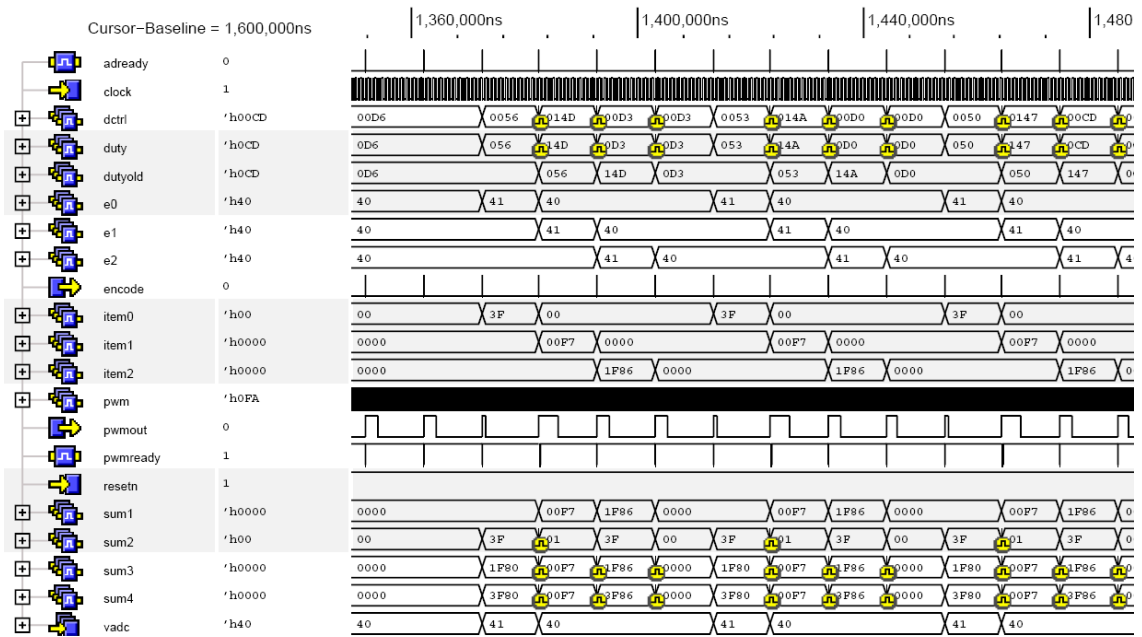
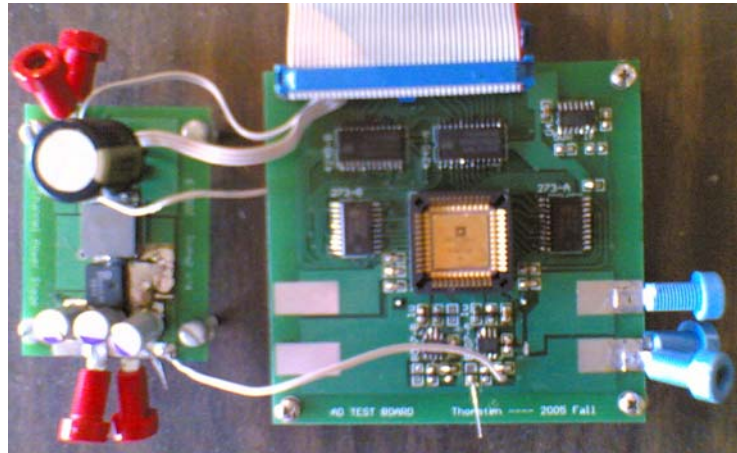
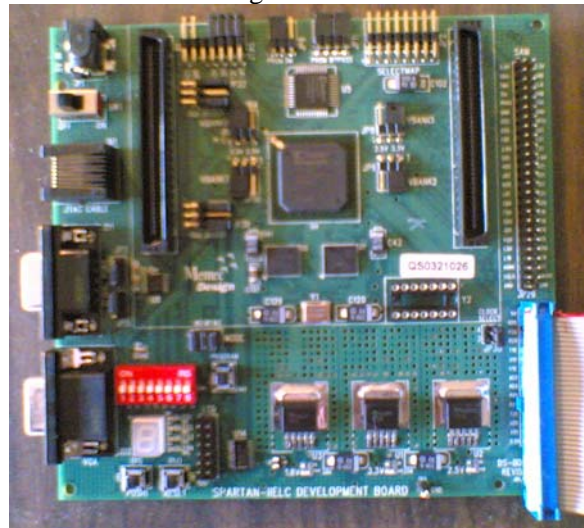


Figure 4.24: Simvision digital waveforms.

An experiment was performed with the same power stage parameters. The experimental setup was built on a Xilinx FPGA board with custom designed power stage and ADC board, as shown below in Figure 4.25. Load transient results are shown in Figure 4.26. The system is very stable under both loading step change and unloading step change conditions.



Power stage and ADC board



FPGA board

Figure 4.25: Experimental setup, including power stage, ADC board and FPGA board.

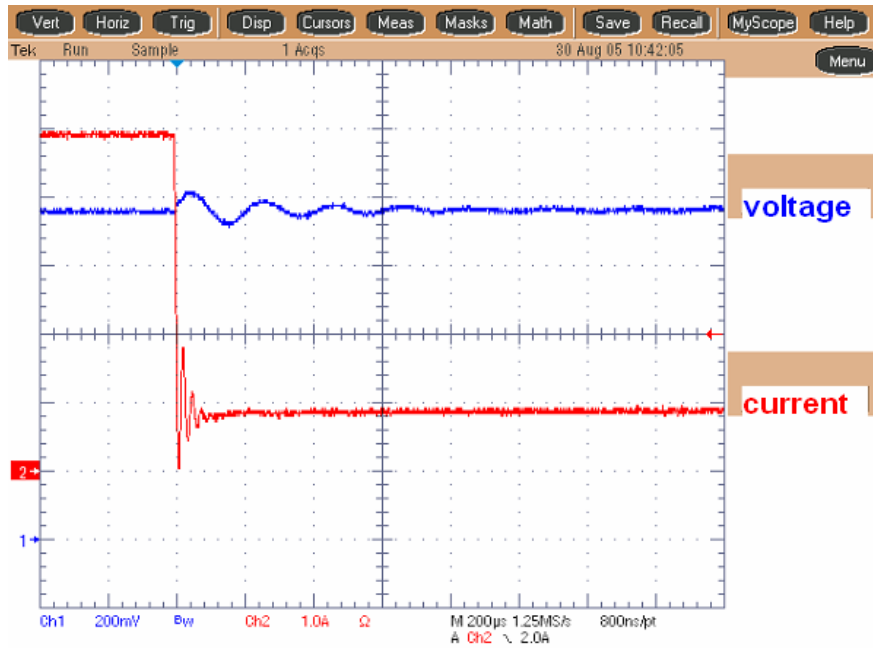
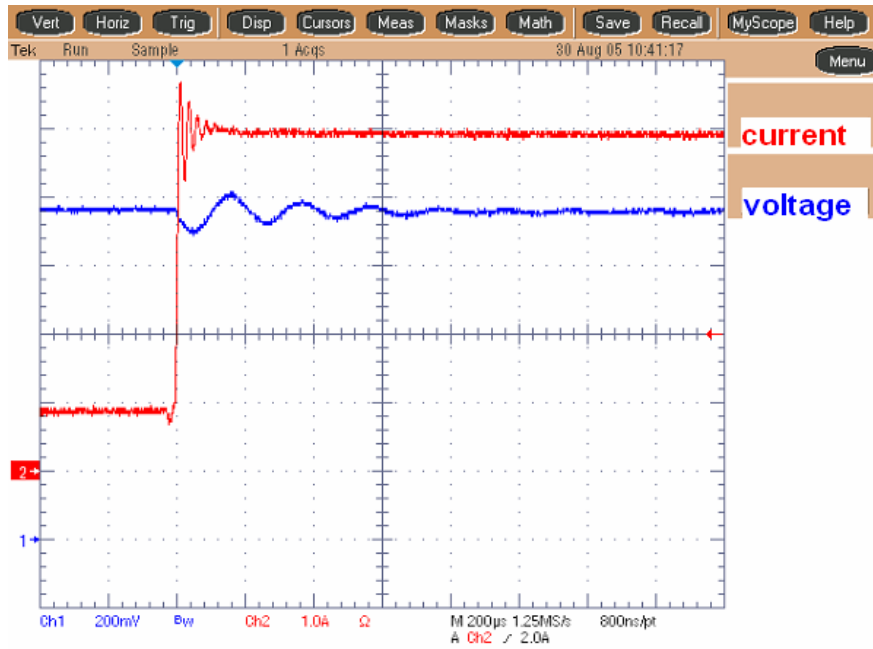


Figure 4.26: Loading and unload step response.

Chapter 5

LOW COST DIGITAL IMPLEMENTATION AND OTHER FUTURE WORKS

5.1 Online Double Pole Frequency Detection

Large power management systems usually involve a lot of external passive components with parametric variations. High quality components have low standard deviation and they are expensive, while low price components may have very large parametric variations. Power management chips are also operating under a wide range of temperatures. Temperature change makes the things even worse. In analog controller design, control parameters are adjusted to satisfy the worst case condition. A worst case design sacrifices the performance. If the uncertainties are significant, they will compromise the system static and dynamic response enormously.

In such situation, programmability makes digital controller much superior to the analog counter parts. The control parameters can be flexibly changed based on performance requirement. External memory (E²PROM) is required for programmability. However, as described in Chapter 1, external memory increases the power management chip cost.

In order to solve this issue, a low cost digital solution is to implement an online detection method that can automatically detect the system parameters of the power converter. This method reduces cost because it allows the elimination of the external memory. Although the proposed concept is not fully verified, circuit implementation is discussed. More detailed intensive study can be a future research area.

5.1.1 Double pole frequency detection method

In designing buck power converter controller, the most important thing is the location of the double pole on frequency spectrum. The control loop compensation parameters are typically designed according to the double pole location. In digital controller, if the double pole location can be found first and then the control parameters can be selected from pre-stored LUTs.

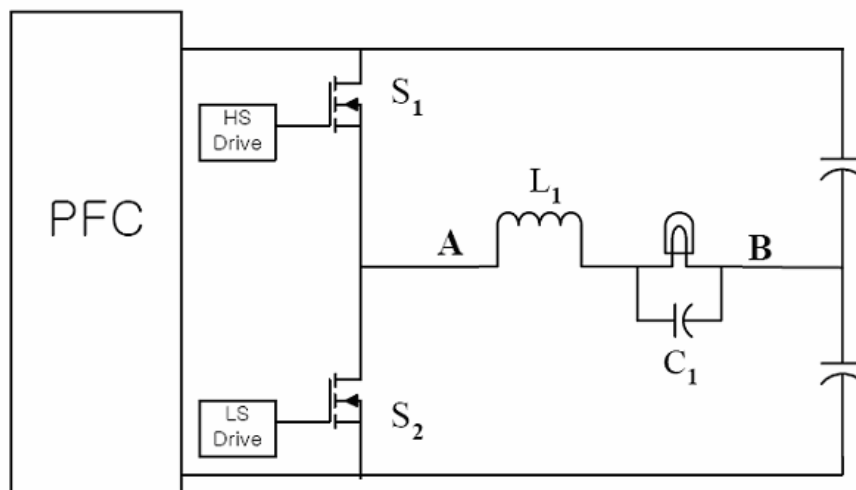


Figure 5.1: Half bridge circuit for lighting applications.

The proposed detection concept is similar to the ignition method in lighting application. In florescent lamp ballast application, the power stage topology is usually a half bridge circuit as shown in Figure 5.1. The lamp is connected to a LC tank. The lamp needs relatively high voltage to ignite. After Power ON and a preheat time, the ignition state is entered and the switching frequency will be swept down. During this process, the circuit approaches the resonance frequency of the load tank. This will excite a high voltage across the lamp, which instantaneously ignites the lamp.

Above concept can also be applied to Buck converter and use it in the double pole frequency detection. The frequency response of buck converter near resonance is shown in Figure 5.2. In principle, by changing the duty cycle pattern, the resonance frequency can be detected as in the half bridge circuit.

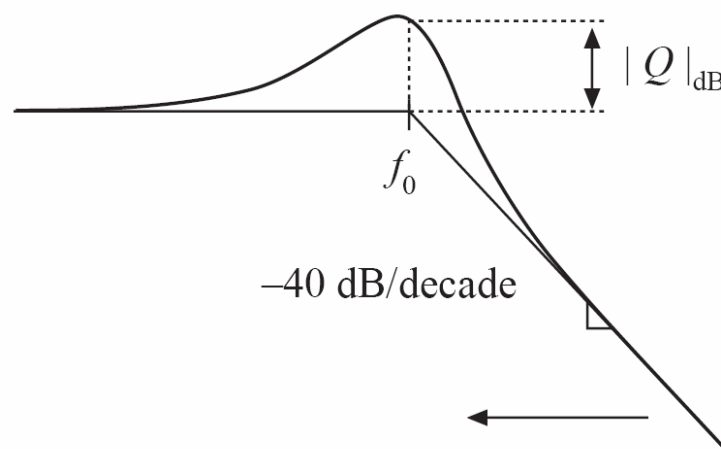


Figure 5.2: Frequency response of buck converter near resonant frequency.

The easiest way to do frequency sweep is changing the duty on the gates. The digital command will vary periodically around a fixed duty, as show in Figure 5.3, so that $D(t)=D_0+\text{sign}[\cos(\omega t)]\Delta d$, where Δd is the injected duty cycle perturbation and ω is the

perturbation frequency. This will introduce lower frequency components to the switching node and output. This low frequency period is changed from high ω_{\max} to low, where $\omega_{\max} > \omega_0$. During any given ω , the output will contain a single dominant frequency component in addition to the switching frequency. For this method to work, $\omega_{\max} < \omega_{\text{sw}}$.

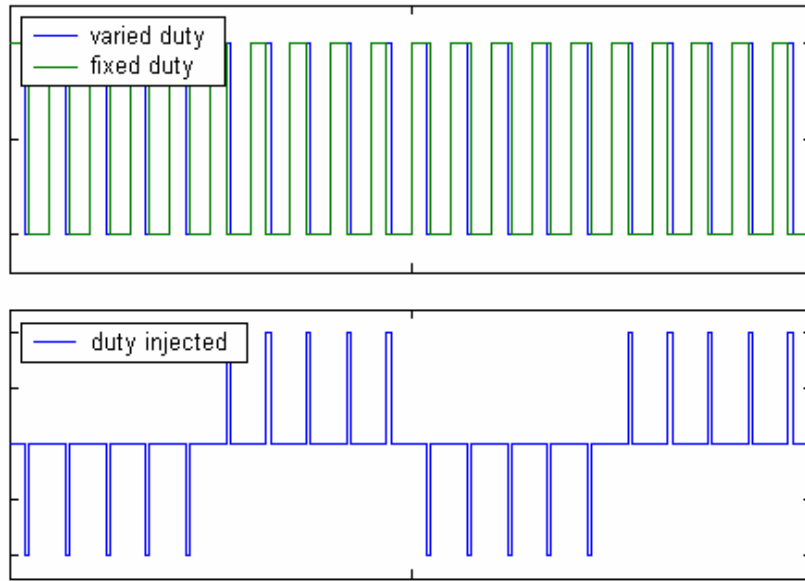


Figure 5.3: Periodic modulation on fixed duty.

The injected duty cycle Δd is small. The pulses are so narrow that they can be considered as a series of pulse trains. The Fourier series coefficients can be derived.

$$C_n = \frac{\Delta d}{kT} \frac{1 - \cos(n\pi)}{\sin\left(\frac{n\pi}{k}\right)}$$

where k is cycle numbers that are repeating. The fundamental frequency is k times switching frequency.

Since the frequency response rolls off by -40dB in higher frequencies, the harmonics are attenuated very rapidly. Only the base modulation frequency needs to be considered. The output voltage looks like the waveform in Figure 5.4. Perturbation Δd is predetermined, to allow certain swing amplitude at the output. Once the output swing is large enough so that the detection threshold is reached, corresponding to the double pole gain peaking, the double pole frequency is found.

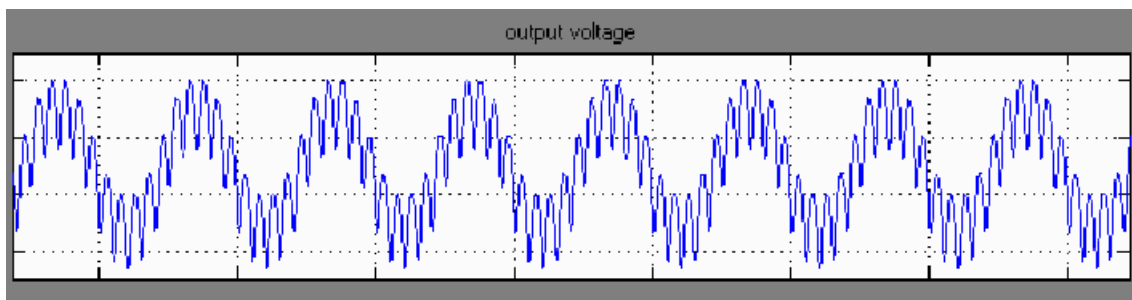


Figure 5.4: Output voltage under periodic modulation.

After the double pole frequency is detected, the best fit PID parameters can be obtained from pre-stored LUTs. Therefore, no external memory is needed any more. The size of LUT is determined by the fluctuation range we need to consider for the double pole frequency.

5.1.2 voltage level definitions and operation sequence

In order not to mess up with normal converter operation, the above proposed detection should be conducted during the Buck converter start up phase, before the output voltage reaches the final steady state regulation value. For a clear illustration, the following voltage levels are defined and drawn in Figure 5.5.

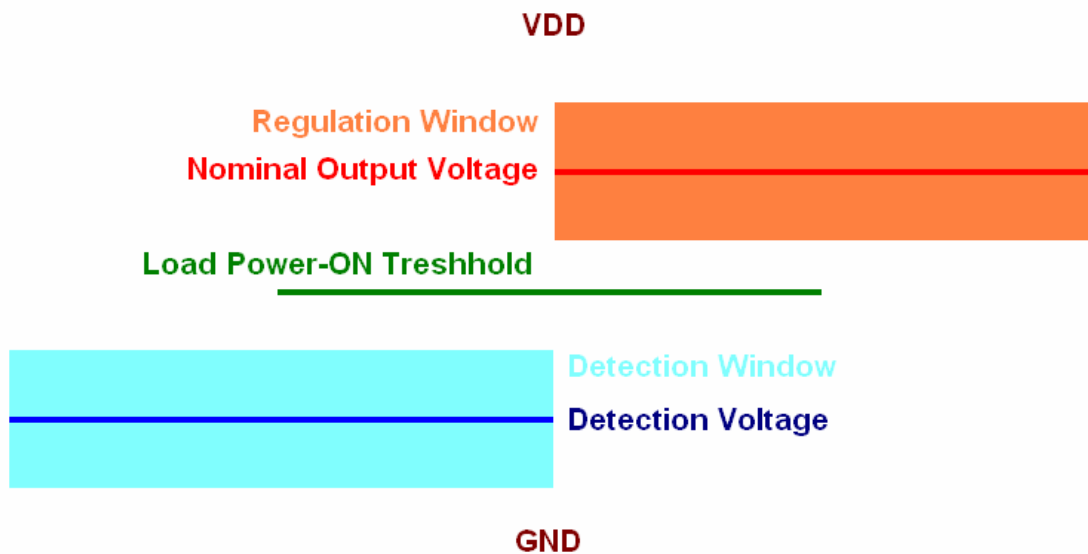


Figure 5.5: Voltage level definitions.

For most applications, there is a voltage regulation window specification in normal operation. It requires the output voltage never exceed the two boundaries, even during the load transients. The load is usually current source type IC and will not be powered on until the regulator voltage is higher than the load chip trigger/protection level.

Since the load is current source type, the small signal control to output transfer function is the same, no matter the load is ON or OFF. Not to interrupt the normal operation of the switching converter and the load, the detection mode should happen at voltage levels below the Power ON threshold to keep the load inactive. The detection window has the same width as the regulation window. The detection operation sequence is described below.

First, a start-up circuit or a slower but stable default compensator drives the converter output to the center of the detection window. Then, periodic perturbations are added to the fixed duty. Finally, the proper control parameters are selected and the regulator runs in

normal condition. Figure 5.6 shows the time domain illustration of the proposed detection process.

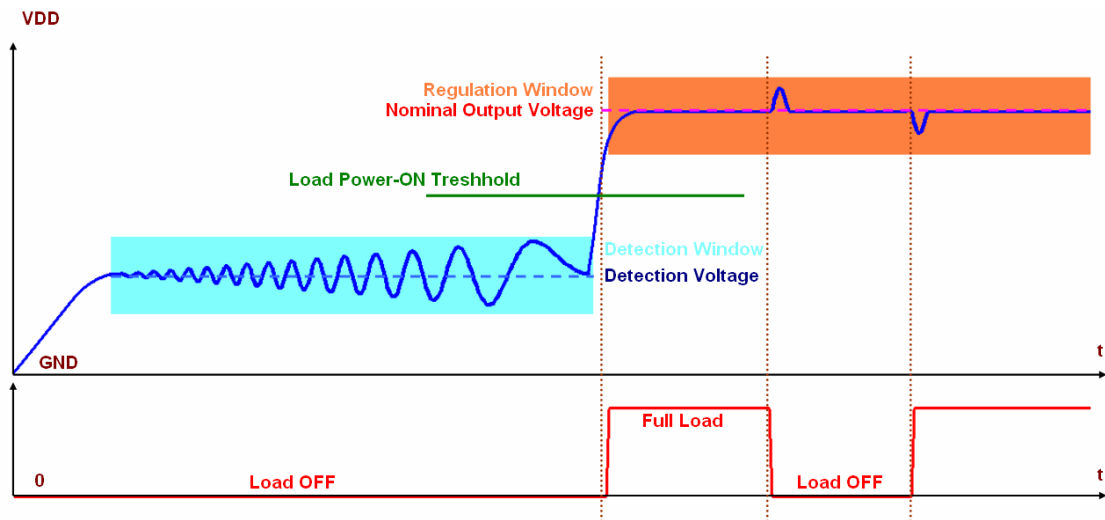


Figure 5.6: Regulator starts from detection mode.

5.1.3 Windowed flash ADC

One of the important building blocks in digital control is the ADC. It turns out that the flash type ADC, as shown in Figure 5.7, is the best candidate for this application. The reasons are explained below.

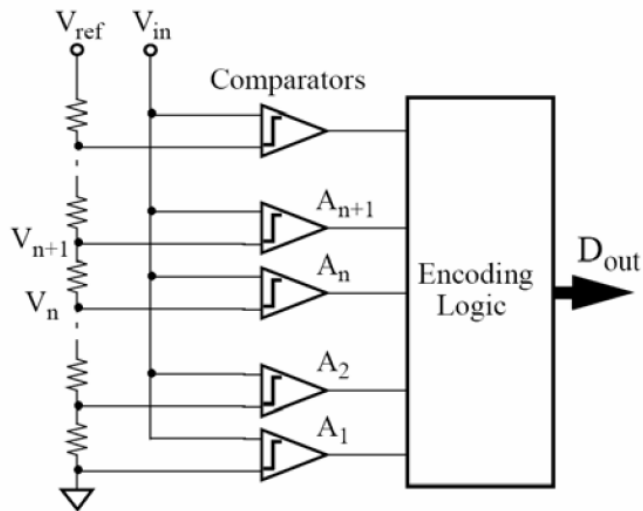


Figure 5.7: Diagram of flash ADC.

In normal operation, the output voltage will never exceed the regulation window. Therefore, a full scale number of the comparators are not necessary. The number of the comparators is determined by the window width and the ADC resolution. This makes the silicon area and the power consumption of the comparators significantly reduced. This architecture is called windowed flash.

Basically, some other types of ADCs divide the full scale signal region into some sub-sections and process the signal in each sub-section separately. Those sub-circuits have the same function as windowed flash. Hence, other structures are generally not considered.

Another reason is the speed. Although the switching frequency is relatively low comparing with the state-of-the-art ADCs, the ADC decision making should be as fast as possible. The ADC is in the digital control loop, excessive interface and computation delay will result in duty delay for one switching cycle.

Some key design parameters should be carefully chosen. The first one is the equivalent ADC speed. The windowed flash is operating synchronized with the switching cycles. But the ADC circuit itself should have higher speed capability, due to the delay reason. The speed is better to be 20-50 times faster than the switching frequency.

The resolution is as important. It should be low enough to avoid limit cycle oscillation [20]. Meanwhile, it should be high enough to avoid slow response of the control.

5.1.4 Low power design

As described in the previous sections, before the load Power-ON, an additional detection mode is added. The detection window has the same width as the regulation window. The same ADC will be used as a detector in this mode. Perturbation Δd used for modulation is calculated to avoid exceeding the ADC window. Therefore the proposed detection mode does not require any additional ADC.

In the windowed flash ADC, the building block is comparator. Typical comparator structure is shown in Figure 5.8. A pre-amplifier is placed before each latch.

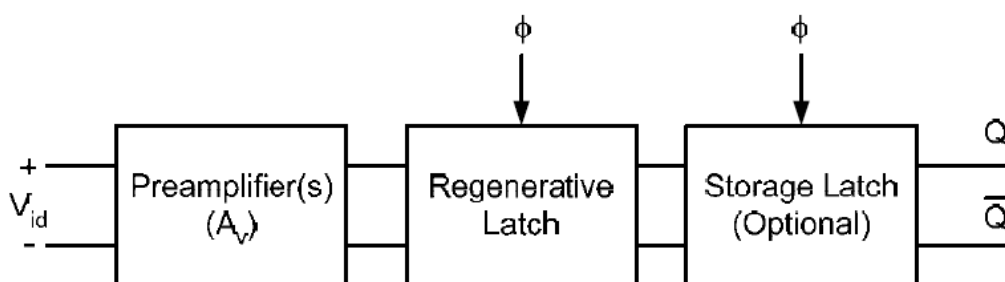


Figure 5.8: Comparator structure.

For the digital controller application, a single common amplifier can be used. It amplifies the each band of window voltage to full scale common mode voltage of the latches, as illustrated in Figure 5.9. This amplifier is connected to different reference in different operation mode.

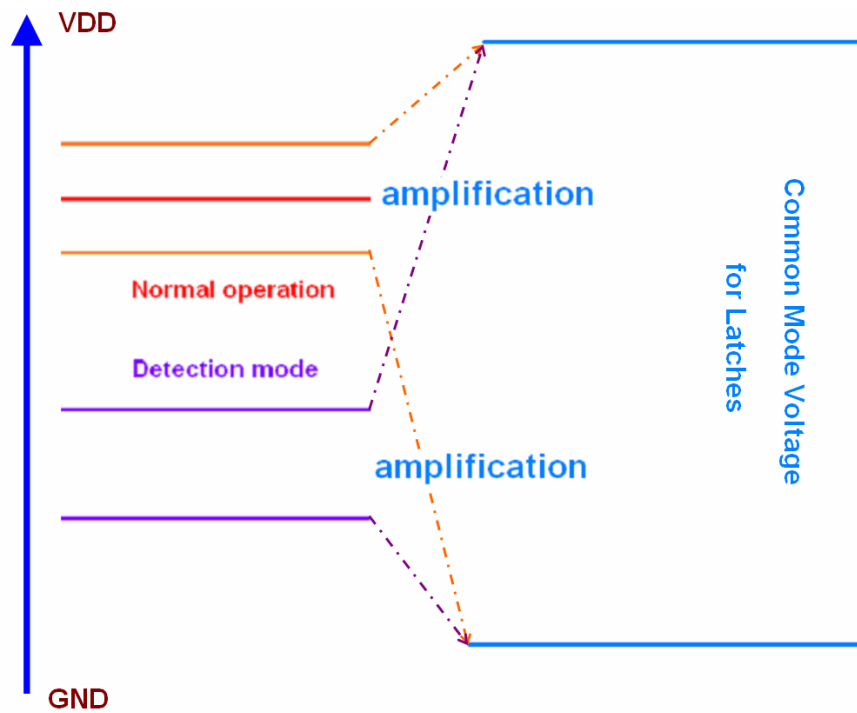


Figure 5.9: Window amplification and comparator reuse.

Switch capacitor circuit is a potential candidate to implement the common preamplifier. Figure 5.10 shows a possible implementation. Although single ended circuit is shown, the real design can be differential.

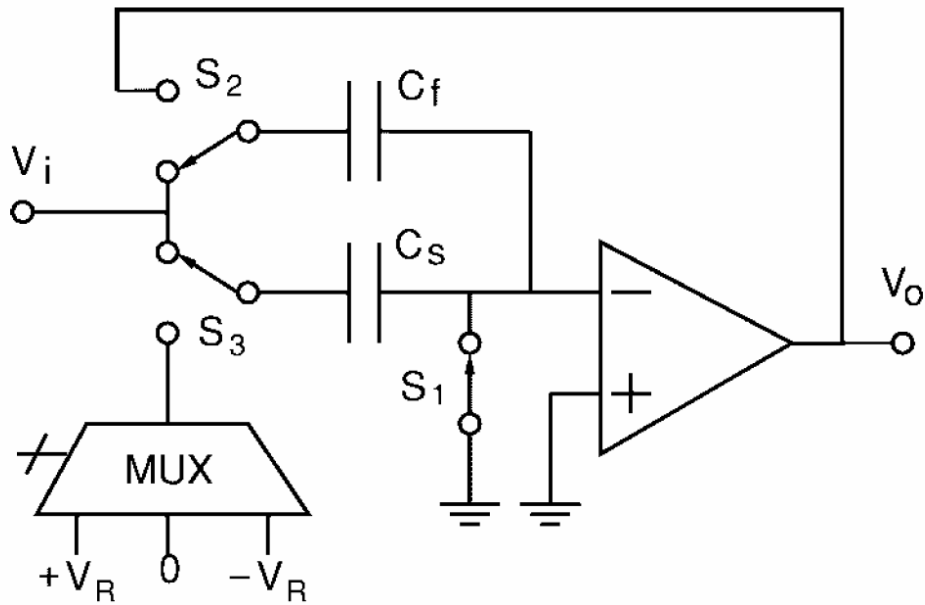


Figure 5.10: A candidate of switch capacitor amplifier implementation.

The transfer function of the above circuit is:

$$V_o = \left(1 + \frac{C_s}{C_f} \right) V_i \pm V_{ref}$$

Now, the ADC is very similar to the two stage flash converter. But the input offset of the amplifier is not critical, because we are more interested in the resolution within the window. The pre-amplifiers in the comparators can be removed, because the signal is already amplified. Another reason is that not many comparators are used in windowed flash ADC, and kickback noise is not severe. Therefore, the clocked latch can be used alone, as shown in Figure 5.11 [21].

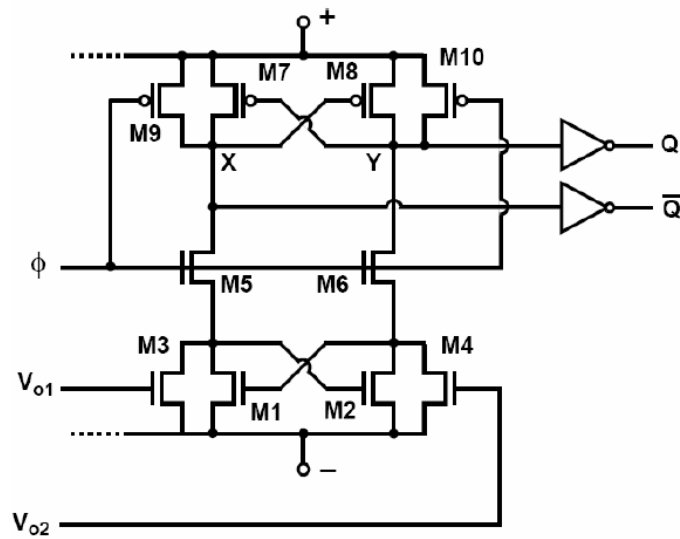


Figure 5.11: Clocked latch.

The power consumption is determined by the sizes of the transistors. The sizing is based on the precision requirement.

$$\Delta V_{GS} = \Delta V_{TH} - \frac{g_m}{I_D} \frac{\Delta \beta}{\beta}$$

$$\sigma(\Delta V_{TH}) \cong \frac{A_{VTH}^2}{WL}$$

$$\sigma\left(\frac{\Delta \beta}{\beta}\right) \cong \frac{A_{\beta}^2}{WL}$$

Both of the factors are area dependent, as long as the technology is fixed. Since the output signal is amplified by G, the area can also be saved by G. So does power.

The power consumption can be estimated from the existing data for a given technology, as shown in Figure 5.12 [22]. There are several factors that affect power consumption: technology, ratio between the window and the full scale, resolution, speed,

structural saving. After picking an available technology, read the power/speed number from the figure. All the other factors are basically some ratio.

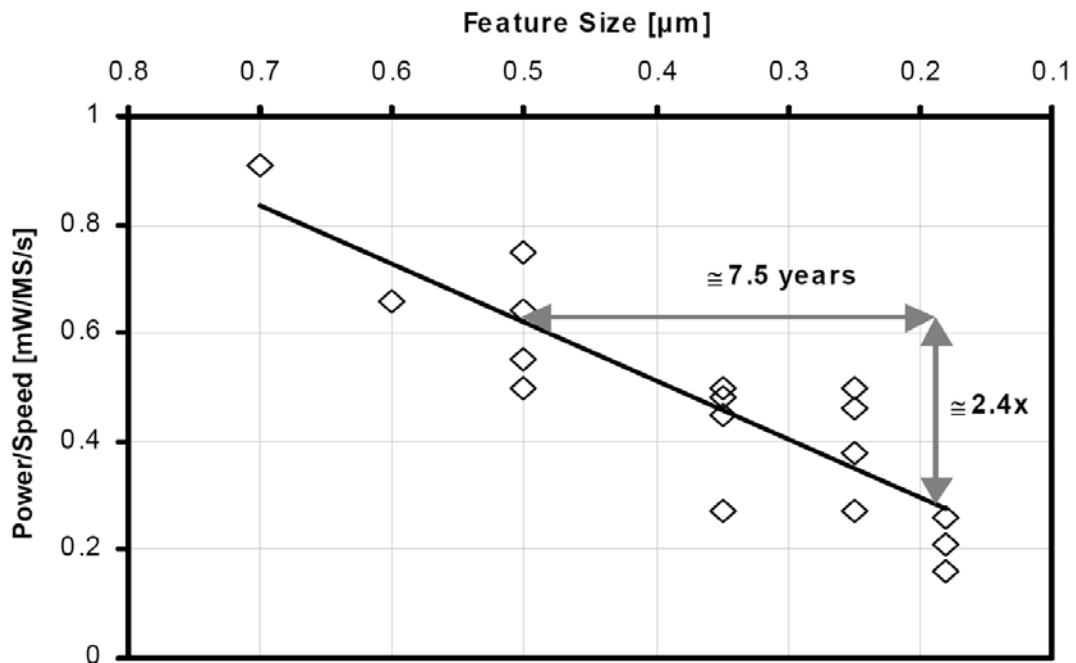


Figure 5.12: Published flash ADC performance vs. technology [22].

5.2 Future work for online detection method

There are some issues with this online detection method worth deeper investigation in the future research.

A double pole in the converter system has two dimensional freedoms. The first information is the resonant frequency, which is the target of the proposed the method. The second information is the Q value, which is also shown in Figure 5.2. In the previous section, the effect of the Q value is totally ignored under some ‘unspoken’ nature of the power converter. Firstly, reasonably high power efficiency is assumed, which implies high Q value.

Secondly, if the detection is not too far off the target frequency, the control effectiveness is not affected very much.

But the Q value does have some effect on detection. The previous section did not talk about the frequency resolution in the detection. If the resolution is too low, esp. when the Q value is high, the frequency detection would not be accurate. On the other hand, if the resolution is too high, the system might take excessive time in the detection mode. Research has to be conducted to determine the proper frequency resolution under the influence of different Q values.

Another factor that has been ignored is the effect of the switching ripple, as can be seen in Figure 5.4. When the ripple becomes large, it may or may not affect the detection amplitude. Therefore, how to calculate Δd under the influence of switching ripple is another topic.

This double pole detection method is simple and cheap to implement, comparing with more theoretical system identification method. A broader and more interesting research area is to find a smart way to improve the accuracy of system characteristic detection, while keeping the simplicity and low cost.

5.3 Discrete OGY method good for digital implementaion

Power converters are nonlinear (piecewise linear) systems in nature. In recent years, the possibility of controlling nonlinear dynamical systems has been the subject of extensive investigation. E.Ott, C.Grebogy and J.A.Yorke (OGY) attempted to solve the problem of controlling chaos by means of small, time-dependent parameter or input perturbations [23][24]. It is noticeable that many unstable periodic orbits (UPO) embed in a strange attractor. Therefore, chaotic systems are more flexible than non-chaotic ones since the attractor spans a large volume of the state space and with proper control, one can rapidly switch among many different behaviors. This gives a direction to improving the response as well as the domain of operation in systems that exhibit chaos for some parameter values. According to OGY method, when system comes near the target UPO on a given Poincaré section, a small perturbation is applied to the parameter in order to make the next Poincaré intersection land on the stable manifold of the saddle fixed point.

The OGY method is developed in the same framework explained in Chapter 2. Similar discrete technique is used to treat the system. The control algorithm is discrete, so it is a good candidate for digital implementation.

In order to study the nonlinear dynamical behavior of the converter, a Poincaré map has to be constructed, which in this case is chosen to be a stroboscopic map due to the T -periodicity imposed by the ramp signal. The stroboscopic map P is obtained by considering the current and voltage at every T -switching. It is defined as follows,

$$(V_n, I_n) \mapsto (V_{n+1}, I_{n+1})$$

where $V_n = v(nT)$ and $I_n = i(nT)$.

Since system equations are piecewise linear, it is relevant to point out that the discrete map can not be determined in closed form, because of the transcendental form of the equations.

Unstable periodic fixed point can not be apparently seen in bifurcation diagram, but it is of fundamental importance in controlling chaos. It is our target of the control process. Without loss of generality, we may describe the system by the following discrete Poincaré map, dimension of which is two in this study,

$$X_{n+1} = P(X_n, p)$$

where it contains an accessible parameters p . Assume that this dynamical system undergoes chaos when parameter is assigned at $p = p^*$. Since we are going to control the system by means of setting accessible parameter properly at each iteration, the previous equation is rewritten as follows,

$$X_{n+1} = P(X_n, p_n)$$

where $p_n = p^* + \Delta p_n$. Δp_n is parameter perturbation in the periodic cycle, which are constrained in a certain range.

Assume that $X^* = P(X^*, p^*)$ is a saddle fixed point in the Poincaré map, namely an UPO solution of the system. P is smooth in the neighborhood of (X^*, p^*) . The system would soon exhibit chaotic behavior when a small perturbation occurs. The parameter is accessible that it can be varied as it is designed. Then a linear stability analysis with $X_n = \Delta X_n + X^*$ and $p_n = p^* + \Delta p_n$ leads to the following discrete system approximately,

$$\Delta X_{n+1} \approx DP \times \Delta X_n + Jp \times \Delta p_n$$

where

$$DP = \left(\frac{\partial}{\partial X_n} \right) P(X^*, p^*), \quad Jp = \left(\frac{\partial}{\partial p_n} \right) P(X^*, p^*)$$

Let λ_s and λ_u be the eigenvalues of the Jacobean matrix DP , stable and unstable respectively. They are classified by the condition, $|\lambda_s| < 1 < |\lambda_u|$ and correspondingly have their eigenvectors e_s , e_u and contra variant basis vectors f_s , f_u , which have following property,

$$f_s \bullet e_s = f_u \bullet e_u = 1, \quad f_s \bullet e_u = f_u \bullet e_s = 0$$

The Jacobean matrix can be written in the form of

$$DP = \lambda_u e_u f_u^T + \lambda_s e_s f_s^T$$

Considering that we are aiming at stable solution of the system, vector $X_{n+1} - X^*$ is forced to be tangent to the stable manifold at X^* , thus obtaining

$$f_u \bullet \Delta X_{n+1} = 0$$

This control strategy is discrete and tries to change the accessible parameter cycle by cycle,

$$\Delta p_{0n} = -\lambda_u \frac{f_u \bullet \Delta X_n}{f_u \bullet Jp}$$

When the system converge to the fixed point, the control strategy still keeps running for the precaution that noise or measurement error may cause the state variable to fall into chaos again. Figure 5.13 illustrates the stable, unstable manifold and its stabilization.

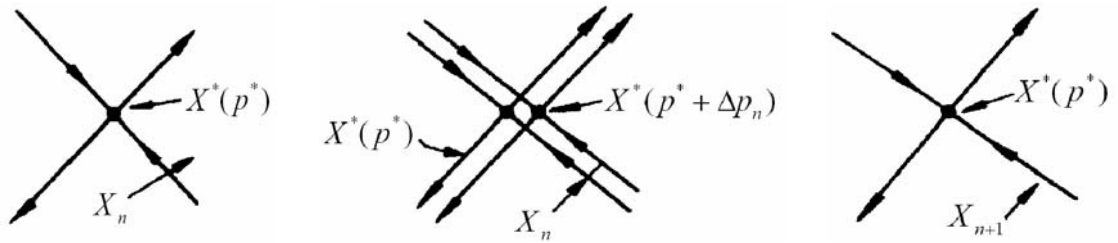


Figure 5.13: Illustration of the stable, unstable manifold and its stabilization.

The control diagram in a boost type converter circuit is shown in Figure 5.14. Experimental waveforms are shown in Figure 5.15.

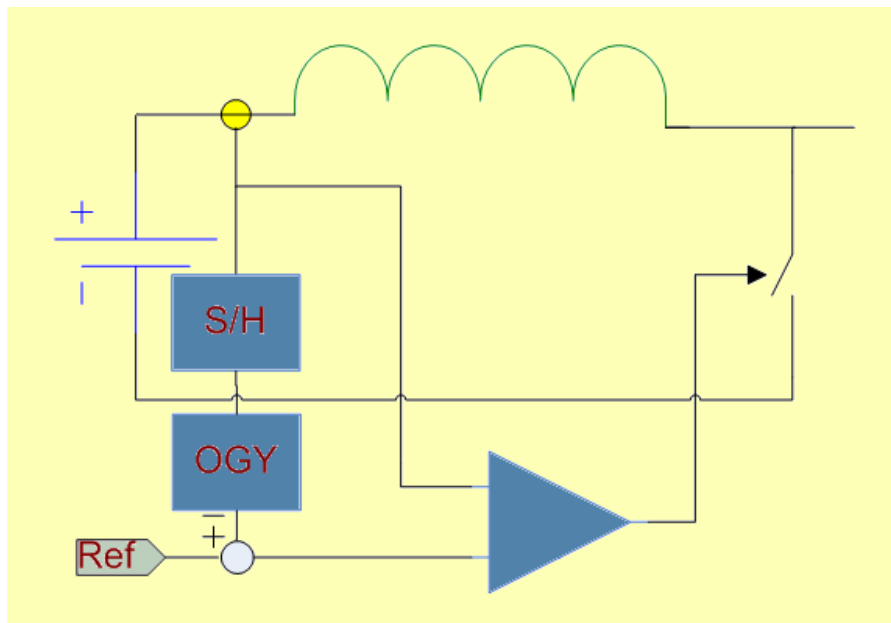
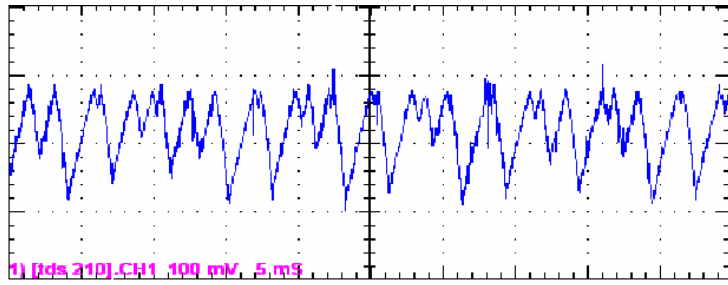


Figure 5.14: OGY control diagram.

before



after

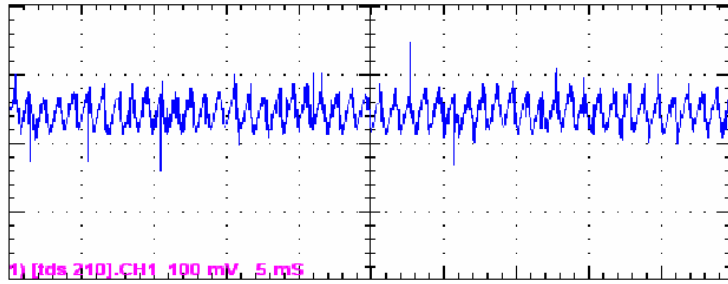


Figure 5.15: OGY control experimental waveforms.

Chapter 6

CONCLUSIONS

Digital controller has a promising future in power management. This thesis is organized from the cost perspective. Rigorous analysis of the system stability and modulator design lead to the conclusion that simple voltage control was preferred to current mode control in digital domain. This will result in lower cost. An improved Z-domain transfer function was also developed to facilitate better direct compensator design in Z-domain.

In the future, detection mode and system identification method will become more and more important to fully utilize the capability of digital signal processing. Adaptive control or online calibration will be the most attractive market selling point. A novel detection method and its implementation are proposed. Future experimental work to verify the proposed method is needed.

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