



US006767806B2

(12) **United States Patent**  
Basceri et al.

(10) **Patent No.:** US 6,767,806 B2  
(45) **Date of Patent:** Jul. 27, 2004

(54) **METHOD OF FORMING A PATTERNED SUBSTANTIALLY CRYSTALLINE Ta<sub>2</sub>O<sub>5</sub> COMPRISING MATERIAL, AND METHOD OF FORMING A CAPACITOR HAVING A CAPACITOR DIELECTRIC REGION COMPRISING SUBSTANTIALLY CRYSTALLINE Ta<sub>2</sub>O<sub>5</sub> COMPRISING MATERIAL**

|                |        |                      |         |
|----------------|--------|----------------------|---------|
| 5,641,702 A    | 6/1997 | Imai et al. ....     | 438/396 |
| 5,726,083 A    | 3/1998 | Takaishi .....       | 438/210 |
| 5,893,734 A    | 4/1999 | Jeng et al. ....     | 438/239 |
| 6,117,725 A    | 9/2000 | Huang .....          | 438/241 |
| 6,200,893 B1   | 3/2001 | Sneh .....           | 438/685 |
| 6,235,572 B1 * | 5/2001 | Kunitomo et al. .... | 438/240 |
| 6,399,438 B2   | 6/2002 | Saito et al. ....    | 438/253 |

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(\* ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 62 days.

(21) Appl. No.: **10/243,386**

(22) Filed: **Sep. 13, 2002**

(65) **Prior Publication Data**

US 2003/0013277 A1 Jan. 16, 2003

**Related U.S. Application Data**

(62) Division of application No. 09/827,759, filed on Apr. 6, 2001.

(51) **Int. Cl.<sup>7</sup>** ..... **H01L 21/20**

(52) **U.S. Cl.** ..... **438/487; 438/486**

(58) **Field of Search** ..... 438/459, 486, 438/487, 240

(56) **References Cited**

**U.S. PATENT DOCUMENTS**

|               |        |                      |         |
|---------------|--------|----------------------|---------|
| 5,292,673 A   | 3/1994 | Shinriki et al. .... | 438/287 |
| 5,486,488 A * | 1/1996 | Kamiyama .....       | 438/396 |

**OTHER PUBLICATIONS**

Bin Yu, et al., "70nm Mosfet with Ultra-Shallow, Abrupt, and Super-Doped S/D Wxtension Implemented by Laser Thermal Process (LTP)", IEEE, Mar. 1999.

Somit Talwar, et al., "Ultra-Shallow, Abrupt, and Highly-activated Junctions by Low-Energy Ion Implantation and Laser Annealing", Verdant Technologies, San Jose, CA.

Ken-ichi Goto, et al., "Ultra-Low Contact Resistance for Deca-nm Mosfets by Laser Annealing", IEEE, Sep. 1999, pp. 20.7.1-20.7.3.

\* cited by examiner

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(57) **ABSTRACT**

In part, disclosed are semiconductor processing methods, methods of depositing a tungsten comprising layer over a substrate, methods of depositing a tungsten nitride comprising layer over a substrate, methods of depositing a tungsten silicide comprising layer over a substrate, methods of forming a transistor gate line over a substrate, methods of forming a patterned substantially crystalline Ta<sub>2</sub>O<sub>5</sub> comprising material, and methods of forming a capacitor dielectric region comprising substantially crystalline Ta<sub>2</sub>O<sub>5</sub> comprising material. In one implementation, a semiconductor processing method includes forming a substantially amorphous Ta<sub>2</sub>O<sub>5</sub> comprising layer over a semiconductive substrate. The layer is exposed to WF<sub>6</sub> under conditions effective to etch substantially amorphous Ta<sub>2</sub>O<sub>5</sub> from the substrate. In one implementation, the layer is exposed to WF<sub>6</sub> under conditions effective to both etch substantially amorphous Ta<sub>2</sub>O<sub>5</sub> from the substrate and deposit a tungsten comprising layer over the substrate during the exposing.

**30 Claims, 7 Drawing Sheets**

