ABSTRACT

TEDESCO, JOSEPH LEO. Electrical Characterization of Transition Metal Silicide Nanostructures Using Variable Temperature Scanning Probe Microscopy. (Under the direction of Robert J. Nemanich.)

Cobalt disilicide ($CoSi_2$) islands have been formed on Si(111) and Si(100) through UHV deposition and annealing. Current-voltage (I-V) and temperature-dependent current-voltage (I-V-T) curves have been measured on the islands using conducting atomic force microscopy (*c*-AFM) with a doped diamond like carbon cantilever. Thermionic emission theory has been applied to the curves and the Schottky barrier heights, Φ_B, and ideality factors, n, for each island have been calculated. Barrier heights and ideality factors are evaluated as functions of temperature, island area, and each other. While all islands were prepared in UHV conditions, one set was removed from UHV and measurements were performed in ambient conditions while the other set remained in UHV. The islands measured in ambient conditions were known as "air-exposed samples" due to the fact that the surface was assumed to be passivated upon exposure to atmospheric conditions. The islands measured in UHV were known as "clean samples" because the surface was not passivated. Air-exposed samples were $CoSi_2$ islands on Si(111) and exhibited a negative linear correlation between the barrier height and the ideality factor. Measured values of Φ_B on the air-exposed samples approached reported bulk values. Measurements from $CoSi_2$ islands on clean Si(111) and Si(100) revealed no correlation between Φ_B and n. Furthermore, it was observed that the measured barrier heights of $CoSi_2$ islands on clean Si surfaces are ~0.2 – 0.3 eV less than the barrier heights measured from $CoSi_2$ islands on air-exposed surfaces. This negative shift in the clean surface barrier heights was attributed to Fermi level pinning by the non-passivated silicon surface states. Additionally, a slight trend toward lower barrier

height as a function of decreasing island area was detected in all samples. This trend is attributed to increased hole injection and generation-recombination in the smaller islands, but it may also be due to effects caused by increased spreading resistance as the island size decreases. Non-linearity in activation energy plots, as well as correlations between decreasing barrier height and decreasing island area-to-island periphery ratio, are attributed to generation-recombination. These measurements indicate that the Schottky barrier height decreases and ideality factor increases with decreasing temperature, even if there is no direct linear correlation between Φ_B and n. These temperature-dependent relationships are attributed primarily to hole injection and generation-recombination, with barrier height inhomogeneity as a minor effect.

Titanium silicide ($TiSi_2$) islands have been formed by UHV deposition of titanium on atomically flat Si(100) and Si(111). Scanning tunneling microscopy (STM), scanning tunneling spectroscopy (STS), and a variant of current imaging tunneling spectroscopy (CITS) have been used to characterize single electron tunneling (SET) through the islands. SET is observed to occur in the islands and is evaluated based on the predictions of the orthodox model. The observation of SET suggests that the Schottky barrier could be effective in future SET-based electronic devices. SET was not observed as often as expected, however, suggesting that there is a mechanism limiting SET. Possible mechanisms for SET limiting are evaluated and it is concluded that SET is limited due to a combination of Schottky barrier lowering, a low resistance substrate, and Fermi level pinning by the non-passivated surface states of the silicon. These factors make SET in $TiSi_2$ islands on silicon potentially too variable to be used in future devices unless the SET-limiting mechanism is resolved.

Electrical Characterization of Transition Metal Silicide Nanostructures Using Variable Temperature Scanning Probe Microscopy

by

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DEDICATION

To my family, all of them, who always believed in and supported me, through the good times, the bad times, and everything in between.

BIOGRAPHY

Joseph Leo Tedesco was born on June 20, 1979 to Patrick and Cecile Tedesco of Virginia Beach, VA. He has one sister, Marie, who was born just over three years later. His early childhood was spent, as most young boys' early lives should be, with playing outside and going to school. He was a good student, and despite a penchant in the early grades for not finishing his work, he enjoyed learning and was naturally curious. He played soccer and baseball, but he knew that his future never lay in the athletic world.

He developed an interest in math and science early on, and his career aspirations extended from them, moving from writer (still an interest), to architect, to architectural engineer. In the eighth grade, he developed an interest in astrophysics and that was that. He graduated from Tallwood High School in Virginia Beach, VA in June of 1997, and that Fall began his studies at the University of Virginia with the intention of studying astrophysics. He quickly reached the conclusion that while he enjoyed astrophysics and found it interesting, he did not want to make it a career. Over the next few years, he happened upon condensed matter physics, and decided that he liked the field enough that he could spend his life in the field. With that in mind, he applied to several graduate schools, all of which had strong research programs in condensed matter, and was accepted to North Carolina State University. After graduating from the University of Virginia, he moved to Raleigh, and joined the Surface Science Lab on June 25, 2001.

During his time at the University of Virginia, not only did he happen upon the field of condensed matter physics, but he also found the woman who would become his wife, Stephanie Mullins. They danced around each other for several months (mostly his fault), but

finally began dating and became inseparable. They were engaged in April of 2001 and married in June of 2004.

In the meantime, he had been working for Dr. Nemanich as a member of the Surface Science Lab and taking classes. He passed the Ph.D. Qualifying Examination in April and May of 2003. This was when the Qualifier consisted on four hour tests in the both morning and afternoon, on Monday, Wednesday, and Friday.

Dr. Nemanich left North Carolina State University to assume the position of chair of the Department of Physics at Arizona State University in August, 2006. Undaunted, Joseph continued his research and passed his Preliminary Oral Exam on February 23, 2007. At that time, his plan called for his final defense to be in February or May of the following year, however, eventually, his defense was set for November 6, 2007. Having decided on this date at the end of September, he had to fit three months of work into six weeks, which he was able to do with many late nights and an understanding wife. He defended successfully at 10:30 AM in 302 Partner's III.

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Throughout this entire process, I have had the complete and total support of my wonderful wife, Stephanie. Her love has made all the difference in things being bearable or not. And her occasional motivational foot in the rear helped me to get a move on and get into the lab. It's not that I'm not motivated, but sometimes it takes a little bit of time for me to get going. Her pushing me was an immense help. Additionally, her tactic of allowing me to "not exist" when it came to housework and cooking and things of that sort so that I could finish my defense and dissertation was invaluable. I thank her for everything she did.

My parents, Patrick and Cecile, and my wife's parents, Orville and Barbara Mullins, were also constant sources of support. They never stopped believing in me, and they always encouraged me. They never grew tired of hearing about what I was doing. I thank them for that and for helping me to feel that I was working toward something. I also want to thank my sister, Marie, and my brother-in-law, Jeff, for always making it sound like what I was doing was so complicated and impressive.

I also want to thank my little dog, Baby Pup, for always being there to provide constant love and the need to go for a walk. It's hard to be unhappy when you get home and your dog runs up to you and jumps up and down. She also helped keep me grounded by wanting to go for those walks, regardless of what was going on. She provided love and joy and I want to thank her for that.

As for the academic side of my graduate career, I would like to thank Dr. Robert Nemanich for being a great advisor and for providing advice and aid and for always pushing me. I also want to thank him for putting up with me, especially during the first nine months I was at NC State, when it seemed that my research consisted of me fixing equipment that I

broke. I know that you learn a lot about something by repairing it, but you can also learn a lot without breaking things. So, I thank him for putting up with the slow periods of research that seemed to dominate the early part of my career.

I would also like to thank Dr. Jack Rowe, who stepped in as my day-to-day advisor when Dr. Nemanich left NC State to become the chair of the Physics Department at Arizona State University. He had different ideas than Dr. Nemanich, and different experiences in the field, and so he provided a different outlook on my research. I thank him for that.

I also thank the other members of my committee, Dr. Thomas Pearl and Dr. Carlton Osburn. They helped out and provided insight into my research. Their advice helped to steer me in the directions I needed to go.

The Nemanich group has always been like a small army, and as such its members are numerous. Nevertheless, there are a few who I feel deserve special thanks. I would like to thank Dr. Jaehwan Oh, for introducing me to STM and for teaching me how to operate the Small System. I would also like to thank Dr. Matt Zeman, for always being willing to talk about research and for putting up with the entropy that surrounded my desk when we shared an office. I would also like to thank Dr. Brian Rodriguez for guidance pertaining to AFM and research in general. A thank you goes to Dr. Anderson Sunda-Meya for his advice during the heteroepitaxy meetings. A quick thank you also goes to Dr. Jamie Perkins for being willing to talk about just about physics or research, which helped to pass the time, particularly during long experiments.

I count the other members of the Nemanich group, past and present as good friends and I thank them for that friendship. To that end, I would like to thank (in no particular order, more or less in order of their offices) Dr. Woochul Yang, Chethan Pandarinath, Dr. Phil

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When I first arrived at NC State in 2001, someone else in the department from outside the Nemanich group (I don't remember who, it may have even been a faculty member) told me that the Nemanich group was like a clique. It's not hard to see how one would come to that conclusion. During my graduate career, the Nemanich group always had at least a dozen members (and usually more) and we spent much of our time around each other doing research, and not out around other members of the graduate school. This wasn't a universal truth, but I found that it was pretty close to one. Therefore, the vast majority of friends I gained at NC State came from within the Nemanich group. However, there are a few friends that came from outside the group. I count Veda Bharath, Nancy Santagata, Matt Walker, Sharon Kiesel, Matt Lewis, Dave Baker, Brian Davis, Franklin DuBose, Bev Clark, and Dr. Simon Lappi among my friends from outside the group. I'm sure that I have forgotten several other people that I consider friends. Please don't take it personally. I thank each one of you.

There are several other people who made things click during my graduate career. Cecilia Upchurch, followed by CJ Hathorne, handled the administrative matters of the Nemanich group with deft ease. Administrative matters that I found difficult they took care of, and were able to help and answer questions. Operations tended to slow down when they

weren't around for whatever reason. I would also like to thank Jenny Allen for helping coordinate matters with the graduate department and make sure I had all my ducks in a row. She was also one of the nicest people.

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I'm sure that there are many others who I should be thanking who I have left of this list. Believe me when I say that it is not an intentional insult. So, to all of you, thank you.

And last, but by no means least, I would like to thank God, who managed to find time to watch over and guide me, despite having a very busy schedule of taking care of the universe and helping sports teams win games.

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Chapter 1:

Introduction

1.1. Motivation

In 1965, Gordon Moore of Fairchild Semiconductor made the bold prediction that the number of transistors that could be put on a microchip would double approximately every two years [1]. This exponential increase would lead to increases in processor speed and memory capacity, as well as decreases in overall device size. His prediction was born of his observations of the state of the semiconductor device industry to that point. Nevertheless, looking back over the years, his prediction has held up remarkably well. However, the trend that Moore predicted may be nearing an end.

The trend has been facilitated by ever-smaller transistors that allow for ever-faster processor designs. The basic structure and composition of these transistors has remained essentially the same. As a result, there are problems that may arise with the current technology long before reaching the absolute physical limits imposed by quantum mechanics. [2]. Silicon-based integrated circuits are rapidly approaching operational limits because of issues with heat dissipation, power density requirements, and current leakage. In order to solve these problems, the semiconductor industry is moving in the direction of using conventional device architecture in a new way, as opposed to redesigning the architecture to take advantage of new device structures [3].

The International Technology Roadmap for Semiconductors (ITRS) has predicted that the current device structure will endure and that decreases in size and advances in speed will continue into the future [4]. Nevertheless, research is being performed to investigate the possibility of utilizing new device structures in order to take advantage of previously-inaccessible physical phenomena. One such area of research into new device structures is research into single-electron devices [5-7].

Single electron devices will most likely utilize nanostructures as their base components because nanostructures offer a variety of advantages, from their ability to self-assemble and be used in "bottom-up" device construction [8] to their novel electrical properties. Self-assembly and nanostructure dynamics have been studied extensively [9-12], but in order to fully incorporate nanostructures into future device structures, the electrical characteristics must be studied further. In order to accurately study the characteristics of single nanostructures, a technique must be used that is capable of probing on a scale of several nanometers. This suggests that scanning probe microscopy will be an ideal technique.

There are many types of scanning probe microscopies available; however, the ones that may be most applicable to this area of research are those that allow for recording current-voltage (I-V) curves from individual nanostructures. For these purposes, scanning tunneling microscopy (STM) and conducting atomic force microscopy (*c*-AFM) appear to be the most relevant techniques. Therefore, in this dissertation, data will be presented that was obtained through the use of STM and *c*-AFM. $CoSi_2$ islands have been be grown on Si(111) and Si(100) surfaces in UHV. Standard thermionic emission theory has been used to calculate the Schotky barrier heights and ideality factor of these islands as a function of temperature. The variable temperature Schottky barrier heights of $CoSi_2$ islands will help elucidate the

transport processes occurring at the nanoscale $CoSi_2$/Si interface. Furthermore, an investigation into variable temperature single electron tunneling (SET) from $TiSi_2$ nanoislands will be presented. Together with the Schottky barrier height study, the variable temperature SET investigation will deepen the understanding of the electrical characteristics of these silicide nanostructures.

1.2. Scope of the Dissertation

This dissertation has been organized to follow a logical progression from beginning to end. An effort was made for this dissertation to build from an initial level, introduce the experimental studies, and draw conclusions from those studies.

As is the case for any experimental study, it is supported by the theoretical information arrayed throughout the literature. Chapter 2 takes this vast array and condenses it into a more reasonable form. It contains the necessary background information to understand the experimental work presented later in the dissertation. The review includes the theory behind the relevant experimental techniques of scanning probe microscopy, spectroscopy, and surface analysis. It also presents an introduction to the theory behind the phenomena presented in later chapters. To that end, the review presents only the barest information regarding silicide nanostructure growth, instead focusing on electrical characterization.

Whereas Chapter 2 introduces the theoretical background for the dissertation, Chapter 3 introduces the experimental facilities used during the studies that will follow. In addition to covering the details of the three experimental chambers used to perform growth and electrical characterization of nanostructures, Chapter 3 also presents the basic procedures used in those studies for sample preparation and characterization.

Chapter 4 presents the investigation concerning variable temperature electrical characterization of $CoSi_2$ islands. Schottky barrier heights and ideality factors are presented for $CoSi_2$ islands grown via self-assembly on Si(111) and Si(100) substrates. The barrier heights and ideality factors were calculated from I-V curves measured at room temperatures and below. The data gathered from these islands is presented, and the temperature dependence allows for a thorough examination of the current transport phenomena occurring in the $CoSi_2$ islands.

Chapter 5 presents the investigation of SET in $TiSi_2$ nanoislands grown on Si(111) and Si(100) substrates. The study presented in Chapter 5 differs from previous studies of SET in $TiSi_2$ nanoislands because it contains a variable temperature component, whereas previous investigations of SET in $TiSi_2$ nanoislands were only performed at room temperature [13-14]. I-V and $\left(\frac{dI}{dV}\right)-V$ curves are presented, along with the analysis of them that confirms the presence of SET. SET was not observed as often as expected, and Chapter 5 also contains an analysis of the reasons for this lack of observed SET.

Chapter 6 presents a summary of the studies presented in the preceding two chapters. The data as well as the explanations of what they mean are summarized and presented in a more concise manner. Chapter 7 contains directions for future research to continue in the area of electrical characterization of silicide nanostructures. Specific recommendations are also made for future research projects as they relate to this dissertation.

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Chapter 2:

Theoretical Background

2.1. Introduction

Experimental physics does not exist in a vacuum. While physical phenomena are often discovered experimentally before the theories that explain them are developed, experiment and theory are nevertheless intimately intertwined. Well-conceived experiments tend to have a rigorous theoretical underpinning. The studies undertaken in this dissertation are no different. The following sections of this chapter contain the theoretical background necessary to interpret and understand the experimental results remainder of this dissertation.

2.2. Scanning Probe Microscopy

Most microscopes are used in the far-field regime, where the spacing between the microscope objective and the sample is greater than the wavelength λ of the interaction being studied. When the spacing is this large, the spatial resolution is governed by the diffraction limit of the wavelength λ. However, there is a class of microscopes known as scanning probe microscopes that overcomes this limit to spatial resolution by operating in the regime where the spacing between the microscope probe and the sample is kept microscopically small and is less than the characteristic wavelength of the interaction being studied. Operating in this regime lends the advantage that the spatial resolution is determined by the effective radius of curvature of the probe and not by the diffraction limit of the wavelength [1]. Therefore, it is possible to use a range of different probe-sample interactions, while raster scanning over the

surface of interest, to collect data with a spatial resolution beyond the diffraction limit. It is this combination of raster scanning and utilizing a probe-sample interaction in the near-field regime, which lies at the center of scanning probe microscopy.

Scanning probe microscopy is used in many fields of study, but it is the electrical characterization of nanostructures that is the focus of this dissertation. In this dissertation, scanning tunneling microscopy (STM), as well as atomic force microscopy (AFM) and its derivative technique, conducting atomic force microscopy (*c*-AFM), are used to probe the electrical properties of transition metal silicide nanostructures.

2.2.1. Scanning Tunneling Microscopy

First invented in 1981 by Gerd Binnig and Heinrich Rohrer of IBM Zurich [2-5], the scanning tunneling microscope (STM) relies on quantum mechanical tunneling of electrons to study the material in question, with the potential to image with atomic scale resolution. The STM utilizes a sharpened metal tip positioned several Å above the sample under inspection. The mechanism used to probe the sample is quantum mechanical tunneling. The only true requirement is that the tip and the sample both be made of conductive material, because a tunneling current must be established between them when they are brought close together. A simple schematic of an STM [6] is shown in Figure 2.1. Several books and numerous review articles have been published related to STM [7-11].

2.2.1.1. Tunneling Tip

The key to realizing atomic resolution begins with the tunneling tip. The STM tip is made of metal and is sharpened. Any metal can be used to fabricate an STM tip, however, the electrical characteristics of the tip cannot be ignored when considering the material. For this

reason transition metals may be superior choices for use as STM tips due to the fact that their d-band electron orbitals are more pointed than the s-, p-, or f-band orbitals [9,12]. In addition to the electrical characteristics of the metal, considerations must be made as to the environment that the tip will encounter, whether that environment will be ultrahigh vacuum (UHV) conditions, ambient conditions, or somewhere in between the two. In UHV conditions, tungsten tends to be the material of choice; however, tungsten readily oxidizes in air and would form an oxide layer, WO_3, that would prevent tunneling and STM. For this reason, platinum-iridium (and not tungsten) is often used in ambient STM because platinum does not oxidize readily. The presence of the iridium in the alloy provides strength to allow the tip to maintain its shape. The lack of rigidity is the primary reason why softer metals, such as pure platinum and gold, do not make good STM tips even though they do not readily oxidize [13].

Metal tips can be prepared in a number of ways [14-17], with two of the most common being mechanical cutting and electrochemical etching. With mechanical cutting, a piece of metal wire is manually cut with a pair of wire cutters to form a sharpened end. With electrochemical etching, the wire is partially submerged in some electrolyte and is biased. Though a wide variety of aqueous solutions can be used as the electrolyte [15], studies in this dissertation utilized 0.5 M KOH. During the electrochemical etching process, the wire functions as the cathode and an electrical current is generated at the interface between the wire and the electrolyte. A feedback loop monitors this current, which decreases as the wire cross-section is etched away and the diameter of the wire decreases. In DC etching, when the wire has thinned sufficiently, it will break off and fall into the solution, shutting off the bias. Using this method, either the top or bottom end of the wire may be used as a tunneling tip;

however, it has been observed that the bottom end that fell into the solution is sometimes the better tip [8]. Using the AC self-terminating method, the tip is inserted into the electrolyte and biased, generating a current that is constantly monitored by the feedback loop. In this method, the wire material is completely etched away from the bottom end of the wire up to the wire-electrolyte interface. As the wire cross-section is etched away, the current decreases until it reaches a pre-set value, at which time the bias is removed and etching presumably stops. It has been shown, however, that if the tip is left in contact with the electrolyte following etching, there is residual etching of the tip (and tip blunting), even without bias being applied [17].

Once the tip has been etched and is loaded into the STM, a bias voltage is applied to it while the sample is grounded or vice versa. Regardless of where the bias is applied, the voltage differential creates an electric field, which causes electrons to quantum mechanically tunnel either from the sample to the tip (if the tip is biased positively) or from the tip to the sample (if the tip is biased negatively). The direction of tunneling is reversed if the bias voltage is applied to the sample. These tunneling electrons generate a current, which is known as the tunneling current. However, the electrons must satisfy Schrödinger's equation as they tunnel across the tip-sample gap, whether it be in vacuum or ambient conditions. Thus,

$$\Psi(z) = \Psi_0 e^{-\kappa z}, \tag{2.2.1}$$

where z is the width of the tunneling barrier, in this case the width of the gap (or the tip-sample distance) and

$$\kappa = \frac{\sqrt{2m(V-E)}}{\hbar}, \tag{2.2.2}$$

where m is the mass of the electron, V is the potential across the gap (the applied bias), and E is the energy of the electron. The probability of the electrons successfully crossing the gap becomes known as the tunneling current and is proportional to the tip-sample distance,

$$I \sim e^{-2\kappa z}. \tag{2.2.3}$$

What this equation effectively means for STM is that because for most tip materials $\kappa \sim 1$, the tunneling current increases (decreases) by about an order of magnitude for every decrease (increase) of the tip-sample distance by 1 Å. This exponential dependence on distance allows for precise vertical measurements. Additionally, precise lateral measurements are possible as well. Due to the fact that [8]

$$I(x) = I_0 \exp\left(\frac{-2\kappa x^2}{2R}\right), \tag{2.2.4}$$

where R is the radius of curvature of the tip, for tip radii on the atomic scale, the lateral resolution is well under 1 Å. Coupled with the fact that ~90% of the tunneling current passes between the two atoms of the tip and sample that are in closest proximity, and for a reasonably sharp tip, atomic resolution is attainable. This theory has been simplified by Tersoff and Hamann [18-19] by assuming that the tunneling tip is composed entirely of s-wave states, and in this case, the tunneling current is found to be proportional to the surface local density of states at the tip Fermi level. In other words, the lateral resolution Δx can be found using the equation,

$$\Delta x \sim \sqrt{2(R+z)}\ \text{Å}, \tag{2.2.5}$$

where R and z are the same as in Eqs. 2.2.4 and 2.2.1, respectively.

This theoretical treatment simplifies matters greatly, but it is not unreasonable. In fact, it underestimates the abilities of STM by being too conservative, particularly concerning

lateral resolution [8]. However, to more fully understand the relationship between the tip and the technique, one must first begin by reassessing the barrier through which the electrons tunnel. Eq. 2.2.3 is the solution for a symmetric barrier, however, in reality, the barrier would become asymmetric due to the presence of image forces in the sample as the tip approached it. The image force would generate a more rounded barrier, and the expression for tunneling current would become

$$I(z) \sim p_t p_s \exp\left(z\sqrt{\kappa}\right), \tag{2.2.6}$$

Where p_t is the electronic structure of the tip and p_s is the electronic structure of the sample [20]. With this correction, however, the vertical behavior of the tunneling current remains the same.

The computer software controlling the approach process continuously monitors the tunneling current. Once it has reached a pre-set value, known as the tunneling setpoint, the tip stops approaching. The distance that the tip is removed from the sample surface once it stops moving is dependent on the setpoint, the applied bias, and the sample (whether it be metal or semiconductor), however, for a setpoint on the order of 1 nA, the tip-sample distance is typically less than 1 nm.

STM images can be attained in either constant current mode or constant height mode. In constant current mode, the feedback loop attempts to maintain the tunneling current at the setpoint value by changing the tip-sample distance as the tip is scanned across the surface. The feedback loop has a gain associated with it that determines how quickly the feedback loop can adjust to changes in the surface topography. The feedback loop is disengaged in constant height mode, because the tip is rastered over the surface at a constant height. As the tip-sample distance increases and decreases, the tunneling current will decrease and increase

accordingly, but the tip will remain constant relative to its starting position. This mode carries with it the inherent danger that the tip could crash into a large feature because its height is greater than the tip-sample distance.

2.2.1.2. Sample

At this point it is appropriate to discuss the role that the sample plays in STM. As stated above, the sample must be conductive, so as to be able to generate a tunneling current between it and the tip when a bias is applied. Furthermore, in order to have atomic resolution, it is necessary to have a sample with flat areas. The surface of the sample may contain steps, such as the steps on silicon or gold surfaces. Regardless of the steps, the area between the steps must be flat in order to afford the best opportunity for achieving atomic resolution. Once the tunneling tip is positioned above the sample and the feedback loop is engaged, the height above will be adjusted in order to maintain the tunneling current near the tunneling setpoint and the tip is rastered back and forth over the sample. Because of this consideration, it may seem that atomic resolution cannot be achieved on a surface with many closely spaced terraces because the tip will constantly be in motion relative to the surface as it adjusts its height above the sample; however, this is not the case, as shown in Figure 2.2 [21].

As the sample is scanned, the tunneling current is proportional to the local density of states of either the sample or the tip, depending on the direction of the voltage gradient. If the gradient from tip to sample is positive, the image recorded will be of the filled states on the surface as electrons will tunnel from the sample to the tip and if the gradient from tip to sample is negative, the image recorded will be of the empty states of the sample because electrons will tunnel from the tip to the sample.

2.2.1.3. Other Considerations

Also essential for achieving atomic resolution is a high quality vibration isolation system [8-9]. Initially, vibration isolation was achieved using magnetic levitation of a superconducting bowl cooled by liquid helium [22]. This method of levitation is no longer used, having been replaced by other methods, such as spring suspension and rare earth magnet eddy current damping. An alternate method of vibration isolation that was developed in the early days of STM was the stack plate-elastomer system, which consists of a stack of metal plates separated by viton rubber pieces [8]. The main advantage of the stacked plate-elastomer system is that it requires very little space, and reasonable vibration isolation can be achieved in a volume of ~1000 cm^3. The main disadvantage of this type of vibration isolation system is that it is only effective for frequencies exceeding ~50 Hz [8]. For low-frequency vibrations, such as those due to building vibrations [23], it is necessary to employ an additional spring suspension system for further vibration isolation. The vibration isolation systems employed in the studies presented in this dissertation are discussed in Chapter 3.

2.2.2. Atomic Force Microscopy

Following their invention of the STM, Binnig and Rohrer proceeded to invent atomic force microscopy (AFM) in 1986 [24]. Initially, the AFM was viewed as a poor alternative STM due to its inability to generate true atomic resolution; ironically, however, it is now viewed as being far more versatile than STM [25]. The enhanced versatility is due to the fact that there are no limitations to the materials that may be studied using AFM, whereas STM is fundamentally limited to studying objects capable of conduction due to the necessity of generating a tunneling current. Furthermore, AFM is capable of probing a wider-range of tip-

sample interactions than STM. The basic operating principle of the AFM is shown in Figure 2.3(a). Numerous books and review articles have been written that discuss atomic force microscopy [10,26-30].

2.2.2.1. Contact Mode Atomic Force Microscopy

All AFM techniques can be separated into one of two primary modes: contact mode and noncontact mode. Noncontact mode AFM was not used during this study, and thus, will not be reviewed. In contact mode AFM, however, the cantilever, usually made from either silicon or silicon nitride, is brought into contact with the surface, where it senses the van der Waals forces, electrostatic forces, and magnetic forces from the surface atoms and is deflected [30]. As the cantilever is rastered across the surface, it is constantly deflected by these forces of the atoms and bends moves up and down. A laser is reflected off the back surface of the cantilever (generally, a reflective coating is deposited on the back surface to enhance the reflectivity of the cantilever) and on to a photodetector. A computer monitors the movements of the reflected laser spot, which are related to the deflections of the cantilever. From these movements, a contour map of the atomic positions can be determined.

Typically the forces present in AFM are small at tip-sample separations of 10 – 100 nm [27], but the basic fact that allows contact mode AFM to respond to these forces and create a profile of the surface atoms is that the force constant, k, of the AFM cantilever is small, generally 0.01 – 10 N/m [26]. The value of k is related to the stiffness of the cantilever and the small value of the force constant allows the cantilever to bend and sense these forces. The cantilever operates under the basic tenets of Hooke's Law, where the displacement of the cantilever, Δz is related to the applied force, F, by the equation

$$F = k\Delta z, \tag{2.2.7}$$

and the resonant frequency of the cantilever, f_r, is,

$$f_r = 2\pi\sqrt{\frac{k}{m}}, \tag{2.2.8}$$

where m is the mass of the cantilever.

True atomic resolution is not typically obtained in contact mode AFM because the tip is in contact with multiple atoms at once and under those conditions it is impossible to image single atoms. If the dimensions of the tip were on the order of a single atom, the attractive forces would lead to pressures of ~GPa and cause plastic deformation of the tip and sample in order to increase the contact area and reduce the pressure [30]. Regardless, an estimate of the contact diameter R_{cd} can be made using,

$$R_{cd} = 2\left\{\sqrt[3]{\left[\left(\frac{1-\nu_t^{\,2}}{E_t}\right)+\left(\frac{1-\nu_s^{\,2}}{E_s}\right)\right]RF}\right\}, \tag{2.2.9}$$

where R is the radius of the tip, F is the applied force, υ_t and υ_s are the Young's moduli of the probe tip and the sample, and E_t and E_s are the Poisson ratios of the probe tip and the sample. In ambient conditions, R_{cd} ~ 2 – 10 nm, while in UHV conditions, R_{cd} ~1 – 4 nm [30]. This lateral resolution is obviously too large to image atoms because atomic dimensions are ~0.2 nm).

All sub-techniques that rely on contact between the cantilever and the surface, are based upon this basic contact mode behavior. Conducting atomic force microscopy (*c*-AFM) is the only sub-technique of AFM utilized during this study, and it will be discussed in more detail later.

2.2.2.2. Conducting Atomic Force Microscopy

Conducting atomic force microscopy (*c*-AFM) is a descendant of contact mode atomic force microscopy and utilizes a conducting cantilever to measure the electrical characteristics of the surfaces with which it comes in contact. The basic principle behind *c*-AFM is identical to standard contact mode AFM, however the key difference between standard contact mode AFM and *c*-AFM lies in the utility of the conductive cantilever. Any cantilever that is conductive can be used in *c*-AFM. There are several different possibilities for conductive cantilevers that will work for *c*-AFM, ranging from doped silicon cantilevers to metal-coated cantilevers to doped diamond-coated cantilevers. Aside from being conductive, there are other considerations that must be made when considering the nature of the cantilever.

As noted in Section 2.2.2.1, the force constant, *k*, of the cantilever is a measure of its stiffness, and when comparing two cantilevers with different *k* values, the cantilever with the higher *k* value can have more force applied to it. The practical importance of this fact for *c*-AFM is that the stiffer cantilever (the cantilever with the higher value of *k*) can be pushed into the sample under study with more force. This is particularly important if attempting to measure the electrical characteristics of objects with an oxide coating because a higher force must be used in order to "push" through the oxide layer. Such force would not be needed in ordinary contact mode AFM because no electrical data was being gathered. If the sample under study was under vacuum, or were a noble metal, there would be no oxide layer to penetrate, thus less force can be used effectively. Whether or not a cantilever with a lower force constant could be used is something that must be considered, because previous research

[23] indicated that between two cantilevers that differ only in the value of *k*, the stiffer cantilever more accurately reflected electrical characteristics measured using a macroscopic tungsten probe. The cantilevers used in the previous study that exhibited accurate electrical characteristics had *k* values of 17 N/m [23]. The cantilevers used in the study presented in Chapter 4 have *k* values of 42 N/m. A diagram representing the apparatus used in the studies presented in Chapter 4 is shown in Figure 2.3(b).

The other factor that must be considered for *c*-AFM cantilevers is one of durability. While a standard AFM cantilever can be effective until its tip is blunt (and perhaps even long after that if high resolution is not required), a conducting cantilever is useless for *c*-AFM measurements after its conductive coating is worn away. The length of time required for this wear to occur depends on the composition of the conductive material and the force with which the cantilever is scanned across the surface. By scanning with a higher normal force, the frictional force on the cantilever will be greater and the wear on the conductive coating will be greater. Similarly, if high forces will be applied to the cantilever while stationary, such as to penetrate an oxide layer, then the frictional force, and corresponding wear, on the conductive layer will be greater. Therefore, if the experiment under consideration called for electrical characterization of oxidized surfaces, a highly durable cantilever would be preferred, to avoid quickly wearing off the conductive layer and blunting the tip. It is worth noting that with a doped silicon cantilever, the entire cantilever itself is conductive, and there is no layer to wear away. In principle, the useful life of this type of cantilever in *c*-AFM would be until it became too blunt to image appropriately [31]. However, in the studies presented in this dissertation, a silicon cantilever coated with a layer of doped diamond-like carbon (DDESP) was used due to its wear resistance and also because of the use of similar

cantilevers in previous studies [23]. Silicon cantilevers coated with a layer of doped diamond (CDT) were also tried and were found to be as effective as doped diamond-like carbon cantilevers. The DDESP cantilevers were chosen over the CDT cantilevers because the DDESP cantilevers delivered electrical characteristics of a series of large area platinum contact pads that more closely matched results from a macroscopic tungsten probe. Doped silicon cantilevers were also tried, but were not found to be effective in studying the electrical characteristics of the islands studied in this dissertation.

2.3. Additional Surface Analysis Techniques

Several methods of surface analysis exist in addition to scanning probe microscopy, many of which significantly pre-date the invention of the STM. Each method is predicated on analyzing the behavior of the surface and the electrons associated with that surface in order to learn information about the electrical, chemical, and topographical properties of that surface. Three surface analysis methods (beyond those explained above) were utilized in this study, Scanning Tunneling Spectroscopy (STS), Auger Electron Spectroscopy (AES), and Low Energy Electron Diffraction (LEED).

2.3.1. Scanning Tunneling Spectroscopy

The technique of scanning tunneling spectroscopy (STS) exists side-by-side with STM because, in addition to gathering topographical data of the surface using STM, STS can be used to gather information regarding the electronic states and energy spectra of the surface under investigation [32]. STS has the added advantage of being able to acquire electronic information simultaneously with topographical data, allowing the topography and the electrical characteristics of the surface to be directly compared to each other. STS has been

used to study the features of the surface density of states and it has been found that the normalized differential conductance curve is largely the same as the bulk band structure of the material [33]. Additionally, by using STS, shifts in the position of the Fermi level as a function of doping may be ascertained as well as the difference between the bulk band gap and surface band gap of silicon [34]. Furthermore, surface chemical reactivity has been studied by STS [35-36], as has the conductivity of nanostructures [37-40], and single electron effects [41]. Several review articles and books [1,9,11,42-44] have been published with extensive information about the technique, however, what follows is a brief summary of the relevant points.

At its core, STS is a simple technique. The feedback loop of the STM is temporarily disabled, meaning that the tunneling tip is held at a fixed point a constant distance away from the sample surface. While the tip is at a constant height, the bias voltage is varied through a range (usually of a few volts), and the current generated by the bias voltage is recorded. This procedure generates a current-voltage (I-V) curve, from which a great deal of information can be gathered. The I-V curve can be manipulated in order to generate the differential conductance curve, $\left(\frac{dI}{dV}\right)-V$, as well as the normalized differential conductance curves, $\left[\frac{\left(\frac{dI}{dV}\right)}{\left(\frac{I}{V}\right)}\right]-V$, both of which can be used to glean more electronic information regarding the surface under investigation.

When the bias voltage range is lower than the work functions of the tip and sample, the structure in the $\left(\frac{dI}{dV}\right)-V$ curves can be correlated with the surface density of states. Thus, at low voltages, STS is generally an effective means of surface state spectroscopy [10]. However, care must be taken because structure in the surface density of states may be due to true surface states or from critical points in the surface-projected bulk band structure. Regardless, interpretation of the low-voltage differential conductance curves is based on the WKB approximation for the tunneling current (with eV > 0 for positive bias and eV < 0 for negative bias),

$$\mathrm{I(V)} = \int_0^{eV} \rho_s(r,E)\rho_t(r,-eV+E)T(E,eV,r)dE\,, \tag{2.3.1}$$

where $p_s(r,E)$ is the electronic structure of the sample at position r and energy E and $p_t(r,-eV+E)$ is the electronic structure of the tip at position r and energy E relative to the Fermi level. The transmission probability T(E,eV,r) is,

$$\mathrm{T(E,eV)} = \exp\left(-\frac{2z\sqrt{2m}}{\hbar}\sqrt{\frac{\varphi_s+\varphi_t}{2}+\frac{eV}{2}-E}\right), \tag{2.3.2}$$

Where z is the tip-sample distance and φ_s and φ_t are the work functions of the sample and tip, respectively. Eq. 2.2.8. can be differentiated to give,

$$\frac{dI}{dV} = \rho_s(r,eV)\rho_t(r,0)T(eV,eV,r) + \int_0^{eV}\rho_s(r,E)\rho_t(r,E-eV)\frac{dT(E,eV,r)}{dV}dE\,. \tag{2.3.3}$$

From the preceding equations, it becomes evident that the tunneling probability is greatest for electrons that are the Fermi level of the electrode that is negatively biased [10].

Despite the fact that the transmission probability is generally unknown, the WKB

approximation gives a monotonically increasing function of applied voltage [10] that acts as a smooth background on to which spectroscopic information is applied. Thus, any structure in the $\left(\frac{dI}{dV}\right)-V$ curve can be ascribed to changes in the surface state density. Therefore, the differential conductance measurements provide a measure of the density of states at a particular location as a function of energy. A representative sample of I-V and $\left(\frac{dI}{dV}\right)-V$ curves is shown in Figure 2.4.

2.3.1.1. Current Imaging Tunneling Spectroscopy (CITS)

As stated above, STS can be used to determine the density of states as a function of energy and I-V curves can be recorded simultaneously with topography. Current imaging tunneling spectroscopy (CITS) is a method of STS that takes advantage of both of these facts to generate an image of the density of states by recording an I-V curve at every raster point in the image. This allows for a complete map of the electronic structure of the sample under study. By recording I-V data at every raster point, this data could be compiled in a manner to create a series of images of the tunneling current at a series of voltages, allowing the surface states to be seen. In fact, CITS was used to study the Si(111):7×7 surface and revealed the atomic location and geometric origin of the surface states [45-46], as shown in Figure 2.5. The differences in electronic structure between different atomic terraces have also been determined using CITS [47].

CITS is frequently used to study defect sites and surface states on semiconductor surfaces, however, it is a very subtle technique and often the energy-dependent transmission probability is ignored [48]. Furthermore, it must be remembered that even though the

feedback loop is disabled and the tip ideally remains at a constant height, the stabilization voltage may change slightly, leading to small variations in the tip-sample distance [48]. If care is taken to account for these possibilities, and with careful examination of $\left(\frac{dI}{dV}\right) - V$ curves and images, CITS can reveal a wealth of information regarding the density of states and surface conductances of the sample [49].

CITS is immensely useful, however, it is time consuming and leaves users with a tremendous amount of data to sift through, i.e. an image composed of 256 lines and 256 rows contains 65,536 raster points, meaning that a CITS scan of such an image would generate 65,536 independent I-V curves.

For the purposes of the single electron tunneling studies pursued in this dissertation, a variant of CITS was developed where an I-V curve was recorded at every fourth point on every fourth line (the image size used in that study was 400 lines by 400 rows). Doing this shortened the time required for data collection by a factor of four, and it still allowed for a dense array of points to be collected from each nanostructure, as shown in Figure 2.6.

2.3.2. Auger Electron Spectroscopy

Auger electron spectroscopy (AES) a surface characterization method based on the Auger effect that was discovered in 1925 [50-51]. The Auger process of electron emission begins by bombarding a sample with an electron beam that has an incident energy of several keV. The incident electrons cause one of the core electrons to be excited, leaving behind a core hole. An electron from a higher orbital drops down to fill the core hole, and emits the excess energy, which is transferred to another electron. This second electron is excited to a

higher level or out of the sample completely.

The primary electrons exit the sample after losing their energies in a well-defined event. AES is performed by collecting this spectrum of emitted electrons N(E). The spectrum of N(E) is then differentiated and a series of peaks is revealed. The positions of the sharp features in the differentiated signal reveal the chemical identity of the sample because the differentiated spectrum of each particular element is unique. By comparing the collected spectrum with spectra recorded in the literature [52], it is possible to determine what is present on the surface. It is also worth noting that the intensity of the AES signal is related to the quality of the sample surface; a very smooth sample surface will produce a larger AES signal than a rough sample surface [52].

It is also possible to do quantitative analysis of the surface using AES. The AES spectra will change depending on the amount of material present on the surface. By carefully measuring the AES spectra and deposition amounts, it is possible to correlate changes in the shape and intensity of the peaks in an AES spectrum with the amount of material on the surface [56]. Additionally, it is possible to determine atomic concentrations by utilizing known Auger sensitivity factors and comparing the peak amplitudes to known standards [52].

2.3.3. Low Energy Electron Diffraction

In 1927, Davisson and Germer discovered that if a beam of electrons is directed at a crystalline surface, that the electrons will be diffracted in the same way that light is diffracted by a grating [54-55]. Low energy electron diffraction (LEED) is a diffraction technique that is based on this phenomenon. Electrons in the energy range of 10 – 1000 eV are incident on the surface and diffract off the atoms, forming an image of the reciprocal space equivalent of

the atomic lattice on the surface. Furthermore, by using 60 – 100 eV incident electrons, the electrons sample the surface atoms and do not penetrate into the bulk. This is due to the fact that the mean free path of the electron is shortest in this energy range [56]. A retarding potential is applied to the grids of the LEED apparatus to ensure that only the elastically scattered electrons reach the screen.

The electrons are scattered in such a way that they satisfy the interference condition due to the crystal periodicity,

$$d\sin\theta = n\lambda, \tag{2.3.4}$$

which is the typical Bragg condition. Due to this requirement, a sample that does not have a well-defined periodic surface will not exhibit a well-defined LEED pattern. For this reason, oxidized samples will generally not exhibit a LEED pattern, and samples with contamination (whether intentional or unintentional) will typically exhibit a different LEED pattern than would the same uncontaminated surface. For example, when the Si(111):7×7 surface is hydrogen passivated, the LEED pattern changes from a (111):7×7 pattern to a (111):1×1 pattern [57].

LEED cannot reveal information about the chemical composition of the surface directly. However, it can be used to determine information about the surface coverage of any deposited layers. Typically, when a full monolayer of material is deposited on to a clean surface, the diffraction pattern will disappear as the long-range order of the surface is destroyed. Upon annealing, if the diffraction pattern reappears, it is taken to mean that the monolayer has coalesced into nanostructures, revealing the underlying substrate. It is also possible that if the nanostructures are dense enough, the resulting LEED pattern can be indicative of the crystalline order of the nanostructures and not the substrate [58]. It is also

sometimes possible to determine information about the thickness of the coverage, depending on the material, as is the case with Ti on Si [53].

2.4. Summary of Relevant Transition Metal Silicides

Entire books and review articles have been written on the rich subject of the physical and electrical characteristics of silicides [59-64], and any attempt to cover the width and breadth of the subject here would be needless. Furthermore, due to their technological importance, articles have been written that have focused on all aspects of cobalt silicide and titanium silicide [65-66]. Therefore, the following information will be a brief summary of the details of cobalt silicide and titanium silicide most relevant to the studies in this dissertation.

2.4.1. Cobalt

The form of cobalt silicide studied here, $CoSi_2$, has a cubic CaF_2 (fluorite) crystal structure, a -1.2% lattice mismatch with silicon, a low chemical resistivity, and a resistivity of 10 – 20 μm-cm [59-65]. For these reasons (among others), it is the form of cobalt silicide most often used by the semiconductor industry [65,67]. This is the primary reason why $CoSi_2$ was studied here, as opposed to one of the cobalt rich phases of cobalt silicide. However, in exploring the mechanism behind the formation of $CoSi_2$, it is essential to discuss these other phases of cobalt silicide.

2.4.1.1. Formation of $CoSi_2$

The specifics of the resulting cobalt silicide formation depend on the specifics of the cobalt deposition and its subsequent annealing. In general, when a layer of cobalt is deposited on silicon at room temperature and annealed to ~250°C, the cobalt reacts with the silicon and

forms Co_2Si. Upon further annealing to 350°C, the film becomes CoSi, and then at 650°C, $CoSi_2$. Furthermore, once above 500°C, the film begins to break up and form islands, and the epitaxial quality of the film increases with increasing temperature [68-69]. By 700°C, the $CoSi_2$ film has completely broken up to form crystallographically oriented islands [70].

There is one type of interface known to form between $CoSi_2$ and Si(100) [59.71], while there are four primary types of interfaces that form between $CoSi_2$ and Si(111), and they are known as type-A, type-B, type-C, and type-D [68-70]. Type-A $CoSi_2$ films have the same orientation as the silicon substrate, whereas type-B $CoSi_2$ films are rotated by 180° about the <111> axis normal to the substrate [78]. Furthermore, the epitaxial relationships between type-C $CoSi_2$ and silicon are $(001)CoSi_2||(111)Si$ and $[-110]CoSi_2||[-110]Si$ [78]. Type-D $CoSi_2$ is a bulk-like termination similar in structure to type-A $CoSi_2$ [73]. All four types of $CoSi_2$ are grown through cobalt deposition followed by annealing. Also, while type-C $CoSi_2$ was once thought to be the result of surface contamination during growth when it was first discovered [72], it has since been reported by other researchers [70]. Type-A and type-B interfaces typically have a high density of pinholes in the surface if the $CoSi_2$ is grown through deposition of cobalt on silicon followed by annealing, while co-deposition of cobalt and silicon avoids this problem [59]. Islands of $CoSi_2$ annealed to 800°C and above have been found to have fully coherent type-B interfaces [73]. Because of this fact, the remainder of the discussion about $CoSi_2$ on Si(111) will focus on the type-B interface.

2.4.1.2. Interfacial Coordination

The coordination of the interface between $CoSi_2$ and Si(111) is a very relevant parameter for determination of the Schottky barrier height because of differences in the

surface states for different coordinations [63,74]. Reports have been presented of five-fold coordinated, seven-fold coordinated, and eight-fold coordinated interface structures [61,63,71]. The coordination number of the interface refers to the number of nearest neighbor atoms for the cobalt atoms in the first layer at the interface. Theoretical analyses of the different type-B interfaces have indicated that the five-fold coordinated interface has an extremely high interfacial energy as compared to the seven-fold and eight-fold coordinated interfaces, and would most likely not form naturally [75]. It has been suggested that a seven-fold coordinated interface would exhibit a Schottky barrier of ~0.40 eV, while an eight-fold coordinated interface would exhibit a barrier height of 0.65 – 0.70 eV [71].

There is less ambiguity concerning the interface between $CoSi_2$ and Si(111). That interface has been shown to be six-fold coordinated, with no other known interfacial structures [75]. This interface is associated with the reported range of barrier heights of $CoSi_2$/Si(100) of 0.68 – 0.80 eV [76].

2.4.2. Titanium

$TiSi_2$, the titanium silicide studied in this dissertation, has two phases, C49 and C54, which have significantly differing properties [63,65]. The type of $TiSi_2$ that ultimately formed is not known, thus both forms will be discussed. Furthermore, in discussing the formation mechanism of C54 $TiSi_2$, the more titanium rich phases of titanium silicide will be discussed, in much the same way that the other phases of cobalt silicide were discussed in Section 4.1.

2.4.2.1. Formation of $TiSi_2$

The reaction pathway between the deposition of titanium on silicon and the formation of a stable $TiSi_2$ phase is complicated [77]. Following titanium deposition, upon annealing to 200 - 300°C, interdiffusion of the silicon into the titanium begins with agglomeration at the grain boundaries. The interdiffusion continues with annealing to 400°C. At 500°C, pockets of silicon and TiO form within the region of mixed titanium and silicon and at 600°C, metastable C49 phase $TiSi_2$ forms. For films with thicknesses below 10 nm, the C49 phase is stable until 800°C, when the C54 phase of $TiSi_2$ begins to form [78].

Both the C49 and the C54 phases of $TiSi_2$ have an orthorhombic crystal structure [65]. The C49 phase is metastable and has a resistivity of 60 μm-cm, while the C54 phase is the more stable high-temperature phase, and has a resistivity of 15 μm-cm [65]. The C49 phase is characterized by a rough interface between the $TiSi_2$ film and the silicon surface, while the C54 phase of $TiSi_2$ it is characterized by a smoother interface than the C49 phase [78]. Nanostructures of $TiSi_2$ have been reported to be both phases [79-80]. It was suggested that the nanostructures of different phases do not differ greatly in their physical and chemical properties [79], but, this was not related to the electrical characteristics of nanostructures with differing phases.

2.5. Metal-Semiconductor Interfaces

Contacts made between metals and semiconductors define many of the modern electronic devices in use today. Layers of theory envelop these contacts, both rectifying and ohmic, and in order to understand the theory, one must begin by understanding the surfaces themselves.

2.5.1. Basic Characteristics of Metal and Semiconductor Surfaces

Metal surfaces and semiconductor surfaces both have a wide range of physics associated with them, independent of the other. Before venturing into understanding the theory behind what happens at the interface between a metal and a semiconductor, it is necessary to understand the basic characteristics of both types of surfaces. A band diagram of a metal-semiconductor interface is shown in Figure 2.7, and each of the relevant quantities is indicated in the diagram.

The metal surface is described by the work function of the metal, φ_M. The work function is the amount of energy necessary to raise an electron from the Fermi level to the vacuum level. The work function is determined from a combination of volume contributions and surface contributions. The volume contribution to the work function is the energy of the electron due to the crystalline lattice of the metal and the interaction of the electron with other electrons. The surface contribution takes into account dipole layers at the metal surface. The dipole layers often exist because the charge distribution around atoms at the metal surface is not symmetric and centers of positive and negative charge do not coincide, resulting in a dipole layer. Additionally surface reconstructions or relaxations can lead to the formation of surface dipoles. Any change in the electron charge distribution on the surface will change the work function, thus, different crystallographic faces of the same crystal have varying work functions due to varying magnitudes of their dipole layers [81].

The semiconductor is defined by the presence of the band gap in the density of states. The width of the band gap, E_g, separates the valence band maximum (VBM) from the conduction band minimum (CBM). The VBM is the highest level with occupied electronic states at T = 0 K, whereas the CBM is the lowest level with unoccupied states. The interval

between the CBM and the energy of the vacuum level (E_{vac}) is also known as the electron affinity, χ_S, which is the difference in energy between an electron at the CBM and an electron at rest outside the surface of the semiconductor. For any non-zero temperature, there is a finite probability that electrons will be able to be excited into the conduction band. If states within the conduction band are occupied, then conduction is possible.

2.5.2. Schottky Barrier

Once the metal and semiconductor surfaces are brought into intimate contact, the electric fields in the two materials cause a transfer of electrons across the interface, leading to an alignment of the Fermi levels of the metal and semiconductor. While this has no significant effect on the electronic structure of the metal, the same cannot be said for the semiconductor. When the semiconductor Fermi level aligns with the Fermi level of the metal, the band structure shifts due to internal electrical fields causing the bands to bend up or down, depending on the doping type of the semiconductor and its relationship to the Fermi level of the metal, as shown in Figure 2.7(c). This band bending leads to a barrier to tunneling across the interface, known as the Schottky barrier. The band bending also leads to the formation of a region of uncompensated donors (or acceptors in p-type semiconductors) next to the metal because N_D (or N_A) is many orders of magnitude less than the density of electrons in the metal. This region of uncompensated donors (or acceptors) is known as the depletion region and it has a width, W [81].

The Schottky barrier height, the height of the tunneling barrier, is often described in terms of the Schottky-Mott model (for an n-type semiconductor) as the difference between the work function of the metal and the electron affinity of the semiconductor [82-83],

$$\Phi_{Bn} = \varphi_M - \chi_S. \quad (2.5.1)$$

Similarly, for a p-type semiconductor,

$$\Phi_{Bp} = (E_g + \chi_S) - \varphi_M. \quad (2.5.2)$$

However, the only substrates used in the studies presented in this dissertation were n-type silicon, therefore, for the remainder of this discussion, only the n-type barrier height will be considered. Thus, from this point, $\Phi_{Bn} = \Phi_B$.

2.5.2.1. Models of Schottky Barrier Formation

While the basic physics describing the formation of the Schottky barrier are presented above, several different models have been created to further explain the formation and behavior of the Schottky barrier, particularly as it relates to the full range of materials.

2.5.2.1.1. Schottky-Mott Model

The Schottky-Mott model is conceptually the simplest of the Schottky barrier models, stating that electronic states at either the metal or the semiconductor surface do not influence the barrier to tunneling. Whether this is due to an absolute lack of surface states, or due to a density of surface states that is too low to influence the electronic properties of the interface is immaterial. Regardless of the reason, when the metal and the semiconductor are brought together, the interface is perfectly intimate and the barrier height is expressed by either Eq. 2.5.1 or Eq. 2.5.2. As a result of the lack of surface states, according to the Schottky-Mott model, the barrier height for a series of metals on a particular semiconductor is linearly correlated to the metallic work function. The band diagram in Figure 2.7(c) is indicative of the predictions of the Schottky-Mott model.

2.5.2.1.2. Metal-Induced Gap States (MIGS) Model

The Metal-Induced Gap States (MIGS) model was developed by Heine in the 1960's [87]. The MIGS model states that the electronic wave functions of the metal atoms do not simply cease to exist at the surface of the metal. Rather, they exponentially decay as predicted by quantum mechanics. However, when the metal is brought into contact with the semiconductor, the metallic wave functions do not simply decay into free space, they penetrate into the semiconductor as far as the Thomas-Fermi screening length. In the semiconductor, the tails of the metallic wave functions induce electronic states in the band gap at energies below the Fermi level.

The induced electronic states form a continuum with a charge neutrality level (CNL), E_{CNL}, which pins the Fermi level if the density of gap states is high enough. It has been shown that this is not the case and the screening potential of the MIGS continuum is limited [99].A semi-empirical formula has been derived for the Schottky barrier height that accounts for this limited screening (for an n-type semiconductor) [85-86],

$$\Phi_B = (E_C - E_{CNL}) + S(\varphi_M - \Phi_{CNL}), \tag{2.5.3}$$

where φ_M is the metallic work function, Φ_{CNL} is the energy location of the CNL (E_{CNL}) from the vacuum level, and S is the slope factor,

$$S = \frac{1}{1 + \frac{q^2}{\varepsilon_i \varepsilon_0} D_{MIGS}(E_{CNL})\delta_i}, \tag{2.5.4}$$

where ε_0 is the permittivity of the vacuum, ε_i is the relative permittivity of the interface, q is the electronic charge, $D_{MIGS}(E_{CNL})$ is the density of the MIGS at E_{CNL}, and δ_i is the thickness of the interface dipole layer.

2.5.2.1.3. Schottky Barrier Inhomogeneity Model

The Schottky Barrier Height Inhomogeneity model was created by Tung and his associates at Bell Laboratories in the mid-1980's [87]. While it predicts the behavior of the barrier at the interface, the model is, in some ways, more general than the preceding models. The Schottky Barrier Inhomogeneity model states that the interface is not composed of a single uniform barrier of height Φ_B, but rather it is composed of a series of regions, or "patches," with a distribution of barrier heights. The model does not specify the origin of the inhomogeneity, only that it is present. Later researchers have added some specificity, stating that the inhomogeneity is most likely due to atomic inhomogeneity at the interface [88-89]. The original model, however, demands no such specificity.

According to the model, if the size of the low-barrier region is smaller than a critical size [87], the potential field of the interface creates a saddle point around the low barrier region that effectively screens it, "pinching it off", and ensuring that it does not affect the barrier of the interface. If the size of the low barrier region is larger than that critical size, then the potential of the interface does not "pinch it off." In this case, the potential of the interface approaches that of a uniform interface with a lower barrier height [88]. In this context, the term "pinch off" refers to that fact that electrons originating outside the depletion region must overcome a potential barrier higher than the band-edge position at the interface in order to reach the interface due to the creation of a saddle point potential [90], as shown in Figure 2.8.

The barrier height inhomogeneity model also states that the distribution of barrier heights at the interface resembles a Gaussian distribution [87]. While the model does not specify a number of patches, numerical simulations that have been performed typically have

a distribution of patches that has a minimum number of ~100 regions [88]. Therefore, the barrier height inhomogeneity model is consistent with macroscopic contacts because the size of the contacts is several orders of magnitude larger than the region size. However, for the case of nanoscale contacts, particularly on moderately doped samples, the size of the contact is not significantly larger than the critical size for low barrier regions discussed above. There is always the possibility that the low barrier region could exist near the edge of the diode [88], in which case it would be less likely to be "pinched off." Regardless, the barrier height inhomogeneity model, while it may be important for macroscopic contacts, it appears to not be as applicable to the case of nanoscale islands. Nevertheless, the model could still explain part of the barrier lowering in islands, but most likely just a minor part.

2.5.3. Current Transport across the Schottky Barrier

Regardless of the model of Schottky barrier formation, they share the common trait of explaining the formation of a rectifying contact. However, they do not explain the flow of current through that rectifying contact. For that, there are three regimes of current transport through the barrier: thermionic emission, thermionic field emission, and field emission. While all three may occur in any given sample, the dominant means of transport is determined by the efficiency of tunneling in the semiconductor, E_{00}, and how E_{00} compares to the available thermal energy, kT. The formula for E_{00} was developed by Padovani and Stratton [91] and is given by the equation

$$E_{00} = \frac{q\hbar}{2}\sqrt{\frac{N_D}{\varepsilon_s m^*}}, \tag{2.5.5}$$

where q is the electron charge, N_D is the doping concentration for a n-type semiconductor, ε_s

is the dielectric constant of the semiconductor and m^* is the effective mass of the electron. Note that the semiconductor will be assumed to be n-type for the remainder of this theoretical discussion because the substrates used in the studies presented in this dissertation are all n-type substrates. However, the same analysis may be performed for p-type semiconductors, with the appropriate changes to account for holes and acceptors.

There are also two other processes that allow current transport in a Schottky diode, recombination in the depletion region and hole injection. Both of these processes, and the three emission processes, are shown in Figure 2.9.

2.5.3.1. Thermionic Emission

When $E_{00} << kT$, tunneling in the semiconductor is highly inefficient, and electrons are elevated to a state in the conduction band that is above the Schottky barrier. There they are emitted over the Schottky barrier to the metal. Current transport of this form is known as thermionic emission and is the dominant form of transport when $N < 10^{17}$ cm^{-3}. The studies presented in this dissertation take place in the thermionic emission regime.

It is simplest to begin by discussing thermionic emission theory [81,90] with regard to an interface with a uniform Schottky barrier height. In this case, the total current I(V) is the sum of the currents in the forward and backward directions, therefore,

$$I(V) = I_{forward} + I_{reverse} = AA^*T^2\exp\left(-\frac{q\Phi_B}{kT}\right)\left[\exp\left(\frac{qV}{kT}\right)-1\right]. \quad (2.5.6)$$

where A is the contact area of the diode, A* is the Richardson's constant for the semiconductor, T is the temperature, Φ_B is the Schottky barrier height, q is the electron charge, V is the applied bias voltage, and k is Boltzmann's constant. This can be written in the familiar way,

$$I(V) = I_S \exp\left(\frac{qV}{kT}\right). \tag{2.5.7}$$

Therefore, when a measured I-V curve is plotted on a semi-logarithmic scale, the curve will have a linear region with a slope α and an intercept with the current axis of I_S. From these parameters, the ideality factor, n, and the Schottky barrier height, Φ_B, of the contact can be calculated, as follows,

$$n = \frac{q}{kT}\frac{d(\ln(I))}{dV} = \frac{q}{kT}\alpha \tag{2.5.8}$$

and

$$\Phi_B = \frac{kT}{q}\ln\left(-\frac{I_S}{AA^*T^2}\right) = \frac{kT}{q}\ln\left(\frac{AA^*T^2}{I_S}\right) = \Phi_B{}^0. \tag{2.5.9}$$

Φ_B is also known as $\Phi_B{}^0$ because there is a correction to Φ_B that takes into account image force lowering. The physical process behind image force lowering is simple to understand. When an electron leaves the metal, the exchange hole it leaves behind acts in a similar manner to the classical image charge [90]. The image force correction, δΦ, is given by

$$\delta\Phi = \sqrt[4]{\frac{q^3 N_D V_{bb}}{8\pi^2 \varepsilon_s^3}}, \tag{2.5.10}$$

where V_{bb} is the total band bending, defined as

$$eV_{bb} = \Phi_B{}^0 - kT\left[\ln\left(\frac{N_D}{n_i}\right)\right] - qV, \tag{2.5.11}$$

with $\Phi_B{}^0$ being the uncorrected Schottky barrier height and n_i is the intrinsic carrier concentration. Considering that the doping concentrations of the silicon substrates used for

the Schottky barrier height study in this dissertation are ~10^{15} cm^{-3}, it is evident from Eqs. 5.4.11 and 5.4.12 that $\delta\Phi \sim 0.0005$ eV and can be neglected.

2.5.3.2. Thermionic Field Emission (TFE)

When $E_{00} \sim kT$, then tunneling is more efficient than in the thermionic emission regime, but electrons will still tunnel through a portion of the Schottky barrier. However, due to the decreased efficiency of tunneling, thermal energy will cause the electrons to be elevated to a higher part of the conduction band, where the barrier to tunneling is lower. In this case, the Schottky contact is in the thermionic field emission regime (TFE) [81,90]. TFE is the dominant mode of current transport when the doping level is moderate-to-high, N ~ $10^{18} - 10^{19}$ cm^{-3}. It has been suggested that thermionic field emission will become the dominant mode of current transport when the semiconductor is doped at N ~ 10^{17} cm^{-3}, but only when the temperature is low [92]. TFE has also been suggested as occurring at the facets of nanostructures due to field enhancement [93-94]. This possibility will be addressed in Chapter 4.

For these semiconductors that exhibit thermionic field emission, the transition to TFE is approximately equivalent to a lowering of the barrier height corresponding to a decrease in the transmission probability of $\frac{1}{e}$. Specifically, this means that the amount of barrier lowering will be

$$\Delta\Phi \approx \left(\frac{3}{2}\right)^{2/3} (E_{00})^{2/3} (V_d)^{1/3}, \tag{2.5.12}$$

where V_d is the diffusion potential

$$V_d = \Phi_B - (E_{CBM} - E_F) - V. \tag{2.5.13}$$

Furthermore, the total current in the TFE regime has been calculated to be

$$I = I_S \exp\left(\frac{V}{E_{00}}\right)\left[1 - \exp\left(-\frac{qV}{kT}\right)\right], \tag{2.5.14}$$

where

$$E_0 = E_{00} \coth\left(\frac{E_{00}}{kT}\right). \tag{2.5.15}$$

2.5.3.3. Field Emission

If tunneling is highly efficient in the semiconductor, $E_{00} >> kT$. If this is the case, then tunneling will be efficient enough that the significant majority of electrons will tunnel through the depletion region. When the dominant mode of current transport is via tunneling, the Schottky contact is in the field emission regime. Field emission tends to be the dominant mode of current transport when the doping level of the semiconductor is very high, $N > 10^{19}$ cm^{-3}. The same equations that describe TFE can be used to describe field emission because they are both instances of direct tunneling through the Schottky barrier [81].

2.5.3.4. Recombination in the Depletion Region

Recombination of charge carriers in depletion region is thought to happen due to electronic states near the center of the band gap and has been shown to be correlated with non-ideality in Schottky diodes [81,95]. The current due to recombination can be written as

$$I_r = \left(\frac{qn_iW}{2\tau_r}\right)\exp\left(\frac{qV}{2kT}\right)\left[1 - \exp\left(-\frac{qV}{kT}\right)\right], \tag{2.5.16}$$

where W is the width of the depletion region and τ_c is the carrier lifetime within the depletion region [81]. Furthermore, recombination tends to be most important in materials with high barriers, low lifetimes, and at low bias and temperature.

Recombination in the depletion region has been shown to lead to ideality factors of up to 2 [96] and the temperature variation of the forward current will reveal two different activation energies, that is, two different temperature dependences with the form $\exp\left(-\frac{E_a}{kT}\right)$ [81]. Despite these facts, recombination is typically overlooked in the literature as a reason for small variations in the ideality of Schottky contacts because it is assumed that recombination will only lead to ideality factors of ~2.

2.5.3.5. Hole Injection

When $\Phi_B > E_i$, as is the case, for example, with typical $TiSi_2$ and $CoSi_2$ contacts on n-type silicon, the depletion region effectively becomes p-type due to a high density of holes [81]. Though the example of $CoSi_2$ and $TiSi_2$ on silicon is used, the effect whereby the depletion region effectively switches type is generally applicable. The holes diffuse into the neutral region of the semiconductor and are injected into the metal contact. There are two regimes of hole injection, hole injection in planar contacts and hole injection in point contacts. In planar contacts, hole injection is negligible [81]. However, for point contacts, γ_h can be large and approach unity. This behavior has been observed experimentally [97] and demonstrated theoretically [98-99]. It has been suggested that under these conditions, the hole current is determined by the transport processes in the neutral region, as opposed to the contact itself [98]. Furthermore, it has demonstrated that the hole diffusion rate will increase

due to accentuation of the hole current [99].

2.6. Single Electron Tunneling (SET)

SET is a phenomenon that occurs in systems of multiple tunnel-coupled junctions as a direct result of the quantization of the charge of the electron. The theory has always stated that SET can occur in a system containing any number of tunnel-coupled electrodes greater than two [100]. However, there is little advantage to analyzing a system with more than three electrodes and two tunnel barriers because the theory is simply generalized from this simple case of the double barrier tunnel junction (DBTJ). The primary reason for this is that the physics is essentially the same as the number of tunnel junctions increases, thus, for simplicity, it is best to focus on two barriers. Furthermore, the data presented in Chapter 5 is based on the DBTJ. Thus, for these reasons, the remainder of the discussion will focus on the physics of SET in DBTJs.

The theory of SET results from the interplay between the continuous nature of electrons within an electrode and the discrete nature of electrons while they tunnel through the barrier [101]. The first tenet of the theory is based on the fact that all objects have a self-capacitance, and with this self-capacitance comes a charging energy, E_C. The charging energy is the energy necessary to have one electron tunnel on to an object and increase the charge of that object by *e*. For macroscopic objects, the value of the self-capacitance is typically greater than 10^{-12} F. The self-capacitance is related to the charging energy by

$$E_C = \frac{e^2}{2C}, \tag{2.6.1}$$

therefore, it is quickly evident that the charging energy for macroscopic objects tends to be

extremely low. However, to see the manner in which this affects SET, it is necessary to understand where the charging energy originates.

In order to transfer an electron from one electrode to another, it is necessary to transfer the charge Δq (for the time being ignoring the fact that q = *e*) to the second electrode, increasing its charge from q, to q + Δq [102]. This costs the system an amount of work in the ΔW, given by ΔW = ΔqΔV. Because

$$\Delta V = \frac{\Delta q}{C}, \tag{2.6.2}$$

it follows that, because Δq = |*e*|,

$$\Delta W = \Delta q \frac{q}{C} \Rightarrow \int_0^W dW = \int_0^e \frac{q}{C} dq \Rightarrow W = \frac{e^2}{2C}. \tag{2.6.3}$$

Therefore, the act of one electron tunneling from one electrode to another costs the system energy in the amount of $\frac{e^2}{2C}$, while the energy of the electrode is increased by the amount $\frac{e}{C}$.

Returning to Eq. 2.6.5 and the discussion that preceded it, it is evident that not only will E_C be extremely low for a macroscopic object, but the increase in energy caused by a tunneling electron will be correspondingly low. This is important as it relates to the first criteria for observing SET. In order to observe SET in a DBTJ, it is necessary that the increase in energy be less than the energy available in ambient thermal fluctuations, kT. In other words,

$$\frac{e}{C_\Sigma} \gg kT, \tag{2.6.4}$$

Where C_Σ is the combined capacitance of the electrode from which the electron originated, C_0, and the central electrode, C_1, and it is given by the equation,

$$C_\Sigma = C_0 + C_1. \tag{2.6.5}$$

Alternately, Eq. 2.6.8 can be formulated in the following way,

$$\frac{e^2}{2C_\Sigma} \gg kT. \tag{2.6.6}$$

The reason for requiring Eq. 2.6.4 (or Eq. 2.6.6, alternately) to be satisfied lies in the knowledge of what SET means.

SET in a DBTJ is defined as the controlled transfer of single electrons between two outer electrodes through a central electrode. If the charging energy (related to the change in energy, as stated previously) of the central electrode is high, then it will require a correspondingly high amount of applied energy to cause one electron to tunnel from one electrode on to the central electrode. However, if the value of the charging energy is low, and Eq. 2.6.6. is not satisfied, then the energy available in ambient thermal fluctuations will be sufficient to cause electrons to spontaneously tunnel. Put another way, when Eq. 2.6.6 is satisfied, electron tunneling through the central electrode is suppressed until sufficient energy is applied to system to make tunneling energetically favorable [102]. Tunneling is energetically favorable when

$$eV + kT \gg \frac{e^2}{2C_\Sigma}, \tag{2.6.7}$$

or (in the alternate form)

$$eV + kT \gg \frac{e}{C_\Sigma}, \tag{2.6.7a}$$

where V is the applied bias.

Returning to the previous example of electron charging in macroscopic objects, consider satisfying Eq. 2.6.6 for a 33 pF. If a 33 pF capacitor were wired into a DBTJ, and the capacitance of the leads were ignored (difficult in practice [101]), the temperature of the system would have to be lowered to ~50 μK in order to observe SET using a 33 pF capacitor. Even if a 1 pF capacitor were used, the system temperature would still need to be lowered to less than 2 mK. From these examples, it is evident that it is not practical to observe SET in macroscopic objects.

It is possible, however, to determine an approximate size for which it is possible to observe SET by using Eq. 2.6.10. This equation can be manipulated to reveal that

$$C \ll \frac{e^2}{2kT}. \tag{2.6.8}$$

By knowing the equation for C, it is possible to determine a maximum size for observing SET. For example, the self-capacitance of a sphere is a medium (considering the other capacitances in the system to be negligible for simplicity) is

$$C = 2\pi\varepsilon_0\varepsilon_r d, \tag{2.6.9}$$

Where ε_0 is the permittivity of the vacuum, ε_r is the dielectric constant of the medium, and d is the diameter of the sphere. For a sphere in vacuum ($\varepsilon_r = 1$), the maximum diameter sphere is $\sim\frac{1.67\times10^{-5}}{T}$ m, while for a sphere embedded in a dielectric such as silicon ($\varepsilon_r = 11.9$ [103]), the maximum diameter sphere is $\sim\frac{1.41\times10^{-5}}{T}$ m, where T is the temperature in degrees Kelvin. For room temperature, these values are ~57 nm and ~4.8 nm, respectively, while for 4.2 K, the values are ~4 μm and ~330 nm, respectively. From these simple

calculations, it becomes clear that the first criterion for observing SET will only be satisfied for nanostructures at all but the lowest temperatures.

In addition to Eq. 2.6.8, there is another criterion that must be satisfied for SET to be observed, that both of the tunnel barriers are opaque enough to tunneling to localize the electron on the central electrode. To sufficiently localize the electron on the central electrode, the tunneling time must exceed the quantum of resistance, $R_Q = \frac{h}{e^2} = 25.813\ k\Omega$. In other words,

$$R_T \gg 25.813\ k\Omega. \tag{2.6.10}$$

Eq. 2.6.14 must hold true for both tunnel junctions. If either value of $R_T < 25.8\ k\Omega$, multiple conduction channels will be available to the electron and it will tunnel on to and/or off of the central electrode too quickly to be measured. An alternate way to think about this is that if Eq. 2.6.14 is not satisfied then the electron wave functions are extended and the electrons cannot be treated as classical, localized particles [104].

By satisfying the criteria embodied in Eqs. 2.6.6 and 2.6.10, it can be determined if it is possible to observe SET in the particular system under investigation. To know what to expect for the SET, however, requires knowledge of the resistance and capacitance of each tunnel junction, and how the RC products relate to each other. The reason for this is that a tunnel junction can be thought of as a parallel combination of a resistor and a capacitor, as shown in Figure 2.10(a) [105]. By determining the RC products of both tunnel junctions, it can be determined whether the Coulomb blockade or the Coulomb staircase is expected. For the discussion in the following sections, it will be assumed that the aforementioned two

criteria must also be satisfied in addition to any other criteria discussed in the relevant section.

2.6.1 Coulomb Blockade

Charge transport through the central electrode of a DBTJ is always suppressed when the charging energy of the electrode is high. However, when the RC products of the tunneling barriers are equal ($R_1C_1 = R_2C_2$) either because the barriers are made of the same substance or are quantitatively similar, then the Coulomb blockade of tunneling is the only discernible SET effect [106]. The Coulomb blockade occurs because charge quantization during tunneling results in a gap of width $\frac{2e^2}{C_\Sigma}$ to form in the states available for tunneling [107]. The gap in the density of states prevents electron from tunneling on to or off of the central electrode until a sufficient bias voltage has been applied and Eq. 2.6.7 has been satisfied. The Coulomb blockade is manifested as a space of zero current in the I-V curve centered on zero bias, as shown in Figure 2.11(ai). By differentiating the I-V curve, the Coulomb blockade is further revealed by the presence of a space of zero conductance, as shown in Figure 2.11(aii). It is worth noting that the presence of the zero conductance gap, when using metal electrodes, is sufficient to confirm SET. However, if one of the electrodes is a semiconductor, as shown in Figures 2.10(b) and 2.10(c), then the zero conductance gap alone is not sufficient proof of SET due to the semiconductor's band gap.

As shown in Figure 2.11(ai), once $V > \left|\frac{e}{C_\Sigma}\right|$, conduction becomes ohmic and follows the predictions of Ohm's Law. The reason for this lies in the fact that $R_1C_1 = R_2C_2$. The RC product determines the time of tunneling events in the barrier, i.e. $\tau_R = RC$. Therefore, if the

two RC products are equal, then tunneling events in both barriers will require the same amount of time and occur simultaneously. Because this is the case, as soon as the energy barrier is surpassed, the electron on the central electrode will tunnel off of the electrode and be replaced immediately by another electron tunneling on to the electrode. Furthermore, because the energy barrier has already been overcome, there are states available to which to tunnel, and tunneling proceeds as normal. Because the barriers are equal, there is no lag between the time an electron tunnels on to the electrode and the time the electron is able to tunnel off of the electrode. Thus, conduction becomes ohmic.

2.6.2. Coulomb Staircase

When the tunnel barriers are asymmetric ($R_1C_1 > R_2C_2$ or vice versa), the current through the central electrode increases in a stepwise fashion at regular intervals as the bias is increased [132]. The manifestation of this asymmetry is known as the Coulomb staircase because the I-V curve takes on a staircase shape due to a correlated set of tunneling processes that occur when one electron tunnels on to or off of the central electrode.

Consider a DBTJ such as that shown in Figure 2.11(a). An electron cannot tunnel through the top tunnel junction until there is an accessible state on the central electrode into which to tunnel. Once this tunneling process occurs, the Fermi level of the central electrode is changed to the point that there are no longer any accessible states for electron tunneling in the central electrode. The electron then tunnels through the bottom tunnel junction, lowering the Fermi energy, and creating a state that allows another electron to tunnel from the top electrode. However, due to the asymmetry, these two tunneling events do not occur simultaneously, and there is a short interval between tunneling events. Nevertheless, once the

electron is able to tunnel on to the central electrode through the top electrode, the process repeats itself, with the voltage increasing by $\frac{e}{C_{\Sigma}}$ each time the electron is able to tunnel through the bottom junction. With the asymmetry causing transport to be blocked during the interval between tunneling events, the current is essentially constant and only increases when the voltage increases. Thus, the I-V curve takes on the appearance of a staircase, as shown in Figure 2.11(bi). By differentiating the I-V curve, a series of peaks becomes apparent in the $\left(\frac{dI}{dV}\right) - V$ curve, as shown in Figure 2.11(bii). In a real I-V curve, the current increases would not be instantaneous and there would be some spread to the peaks, however, in the simplified curve shown in Figure 2.11(bi), the current increases are perfectly instantaneous, leading to perfect delta function peaks in the curve shown in Figure 2.11(bii).

As noted in the previous section, the Coulomb blockade alone is insufficient to confirm SET if one of the electrodes is a semiconductor. The Coulomb staircase is sufficient proof of SET, regardless of the composition of the electrodes. Care must be taken to ensure that the staircase appearance is not due to gaps in the density of states of any of the electrodes, contamination, or electrical noise [108]. However, if these problems are eliminated, then the Coulomb staircase is genuine proof of SET.

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Figures

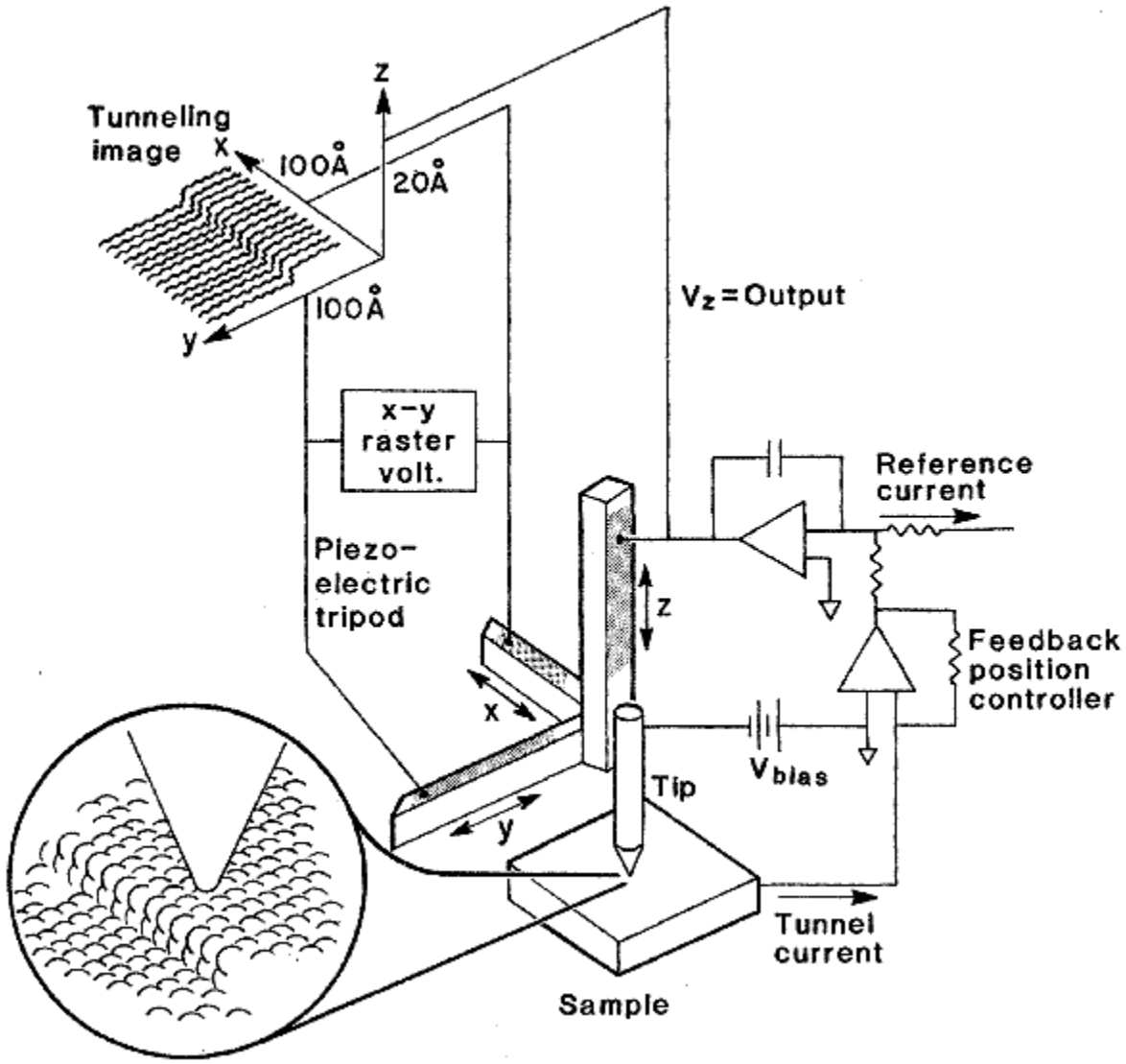

Figure 2.1: Simplified schematic view of an STM [6].

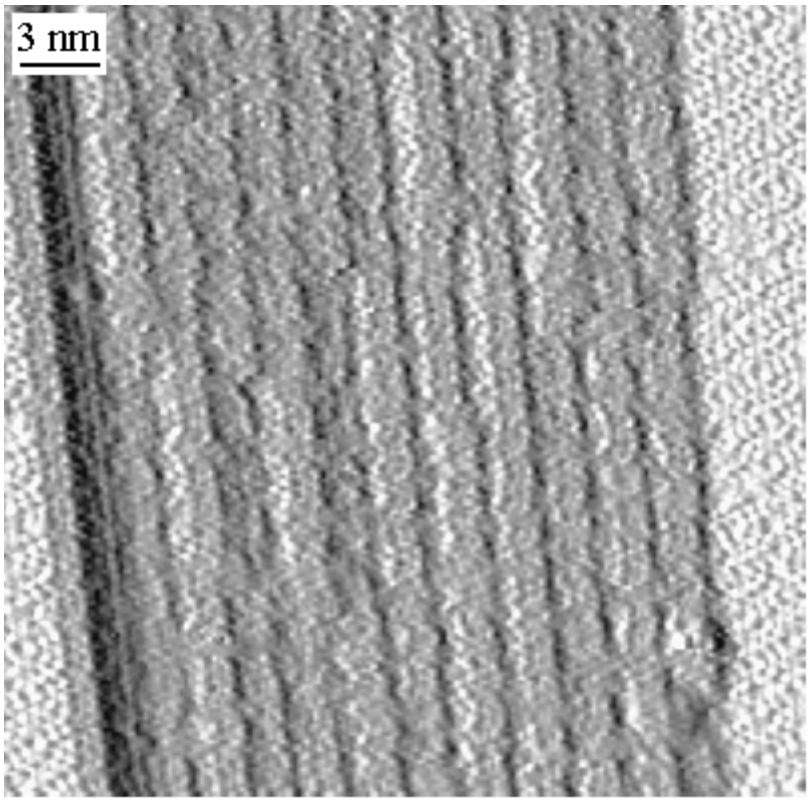

Figure 2.2: STM error signal image of a Si(111):7×7 surface that exhibits step bunching. Scan size: 30 nm × 30 nm. Note that there is evidence of atomic resolution in the individual steps within the step bunch [21].

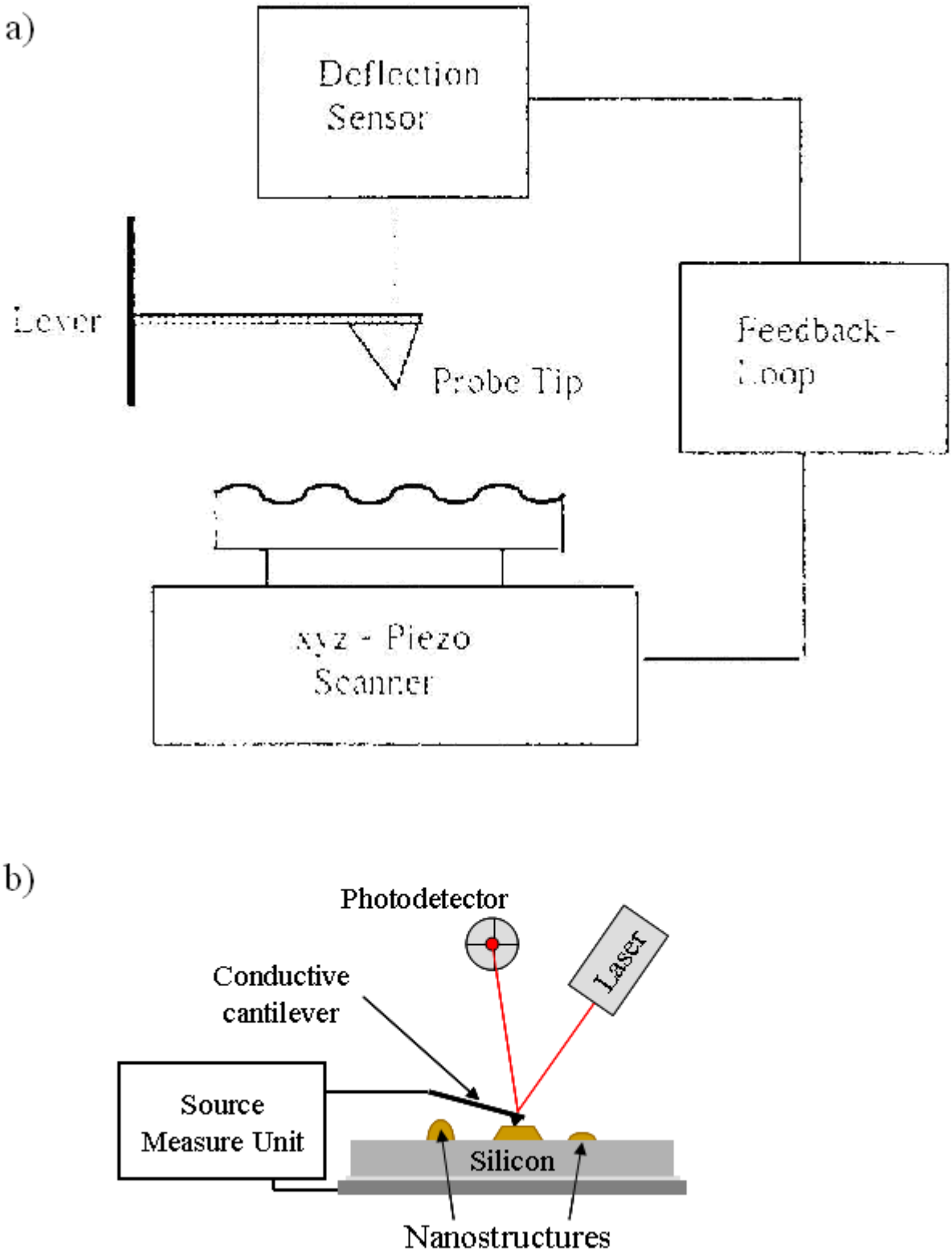

Figure 2.3: (a) Basic operational principle of the AFM [26]. (b) Basic schematic of *c*-AFM measurements presented in Chapter 4.

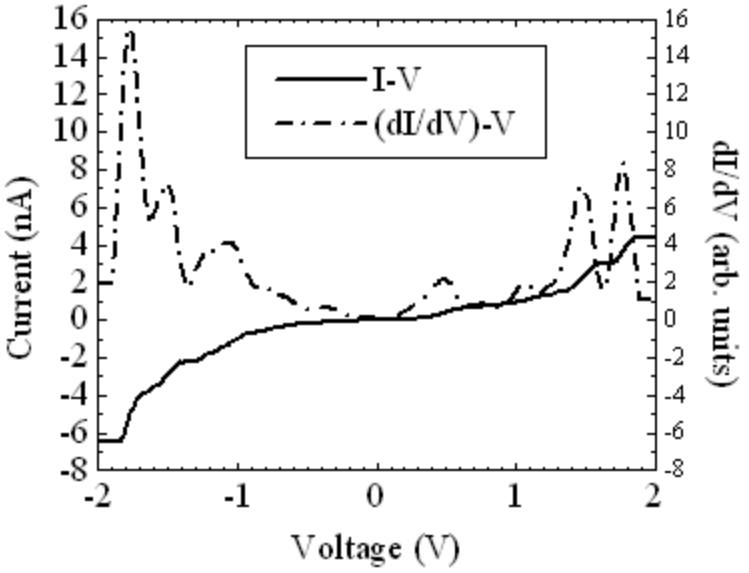

Figure 2.4: STS data recorded on a $TiSi_2$ nanoisland grown on Si(111). Note that small changes in the structure of the I-V curve can lead to pronounced peaks in the $\left(\frac{dI}{dV}\right)-V$ curve.

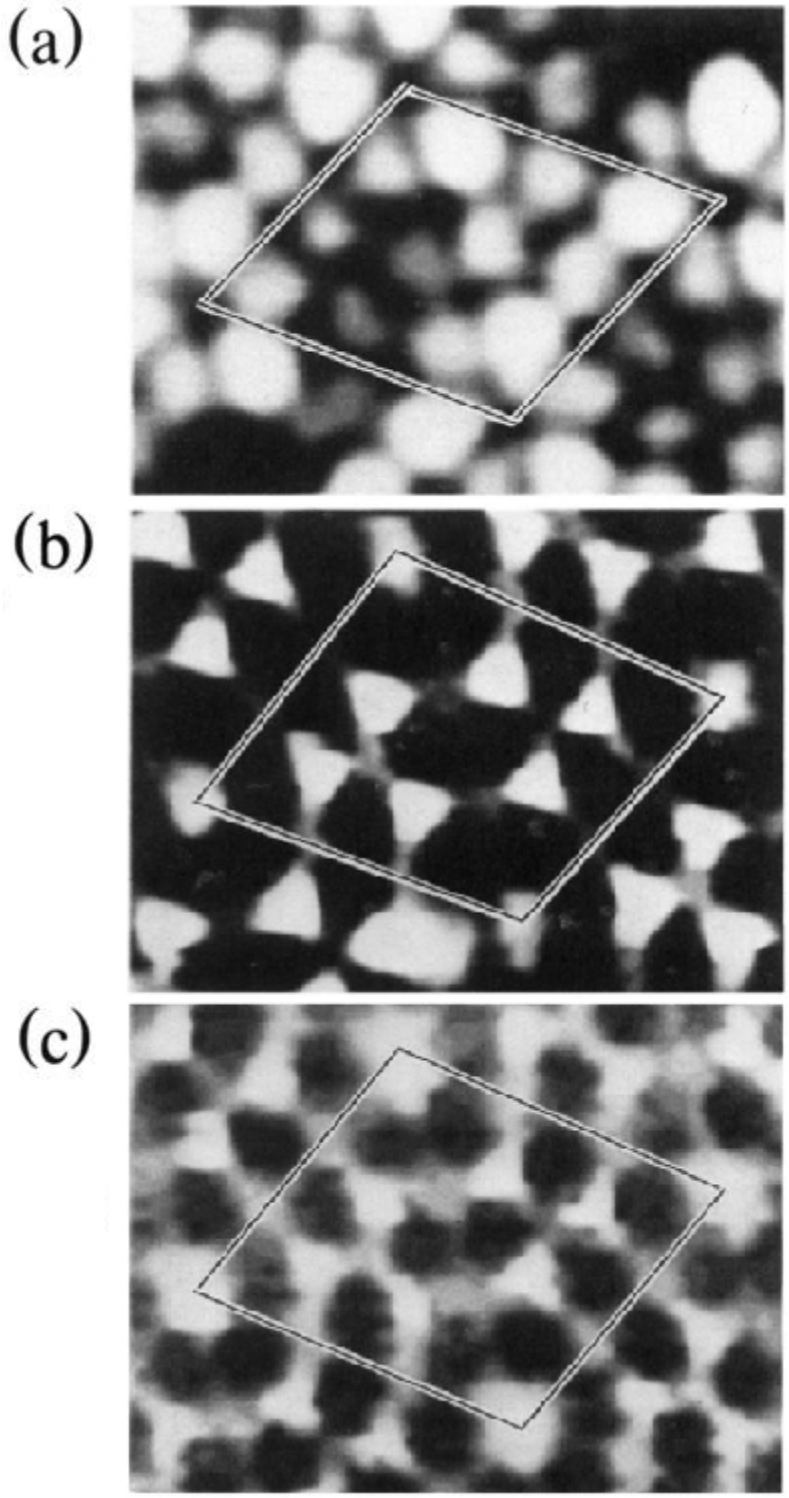

Figure 2.5: CITS images of occupied Si(111):7×7 surface states. (a) Adatom state at -0.35 V, (b) dangling bond state at -0.80 V, (c) backbond state at -1.7 V [49].

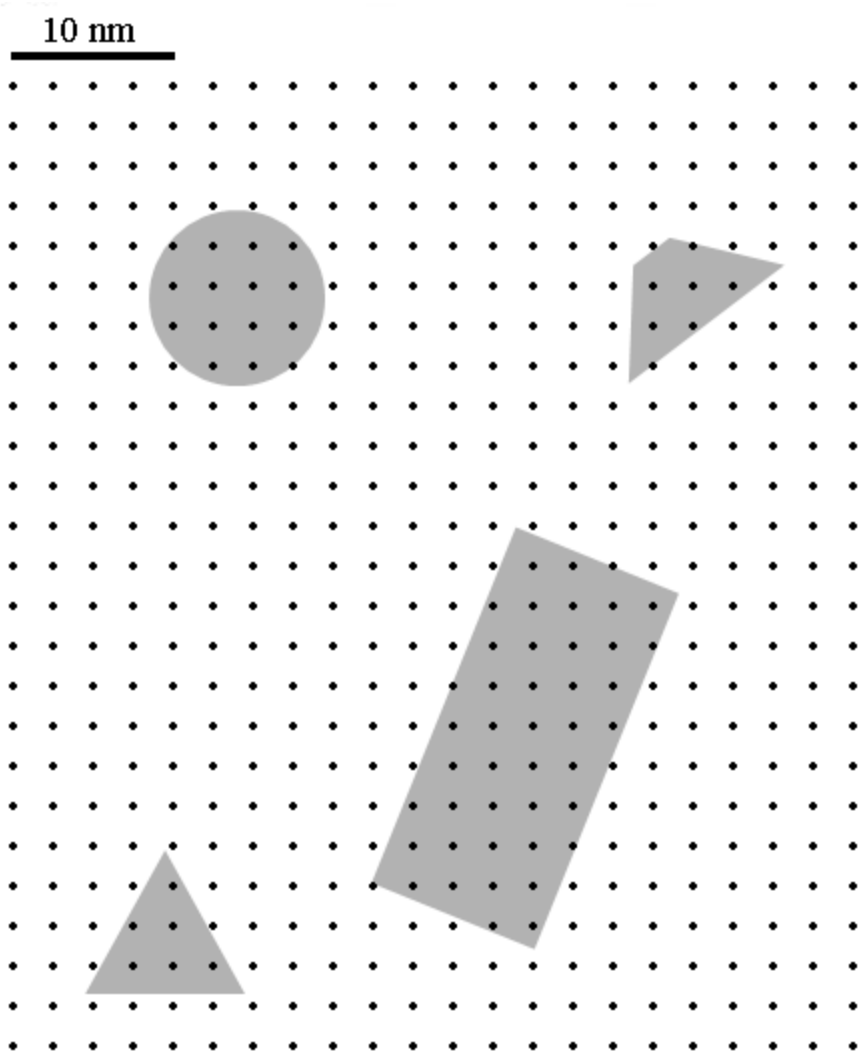

Figure 2.6: Representation of modified CITS. The points on the grid shows the locations of recorded I-V curves in a 50 nm scan area if the I-V curves were recorded every 2.5 nm. This is the point distribution in a 50 nm × 50 nm region of a 100 nm scan composed of 400 lines and 400 rows where an I-V curve is recorded at every fourth point of every fourth row. The gray shapes are arbitrary island shapes and they demonstrate that several I-V curves would be recorded on each island using the modified CITS method.

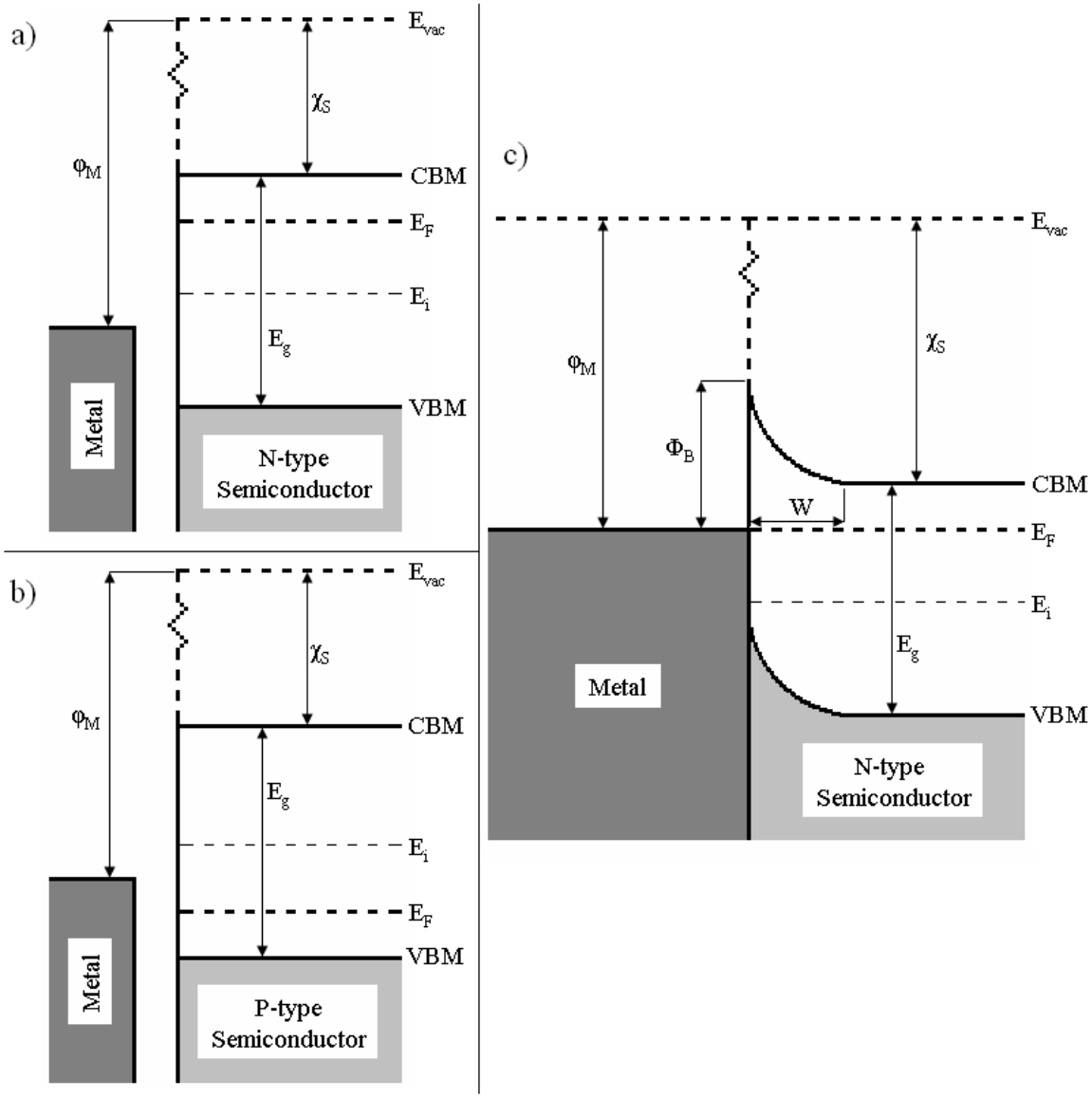

Figure 2.7: Metal-semiconductor heterojunction characteristics. Symbols and abbreviations are defined within the text of Sections 2.5.1 and 2.5.3. (a) A metal surface and an n-type semiconductor surface separated by a large distance. (b) A metal surface and a p-type semiconductor surface separated by a large distance. (c) A metal surface and an n-type semiconductor surface in intimate contact, forming a Schottky barrier. Note that for a metal in intimate contact with a p-type semiconductor, the bands would bend downward.

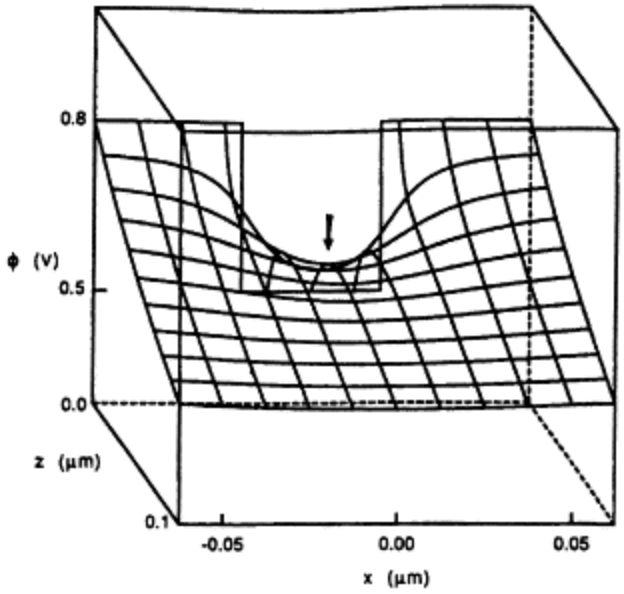

Figure 2.8: Saddle point potential due to Schottky barrier height inhomogeneity model [108].

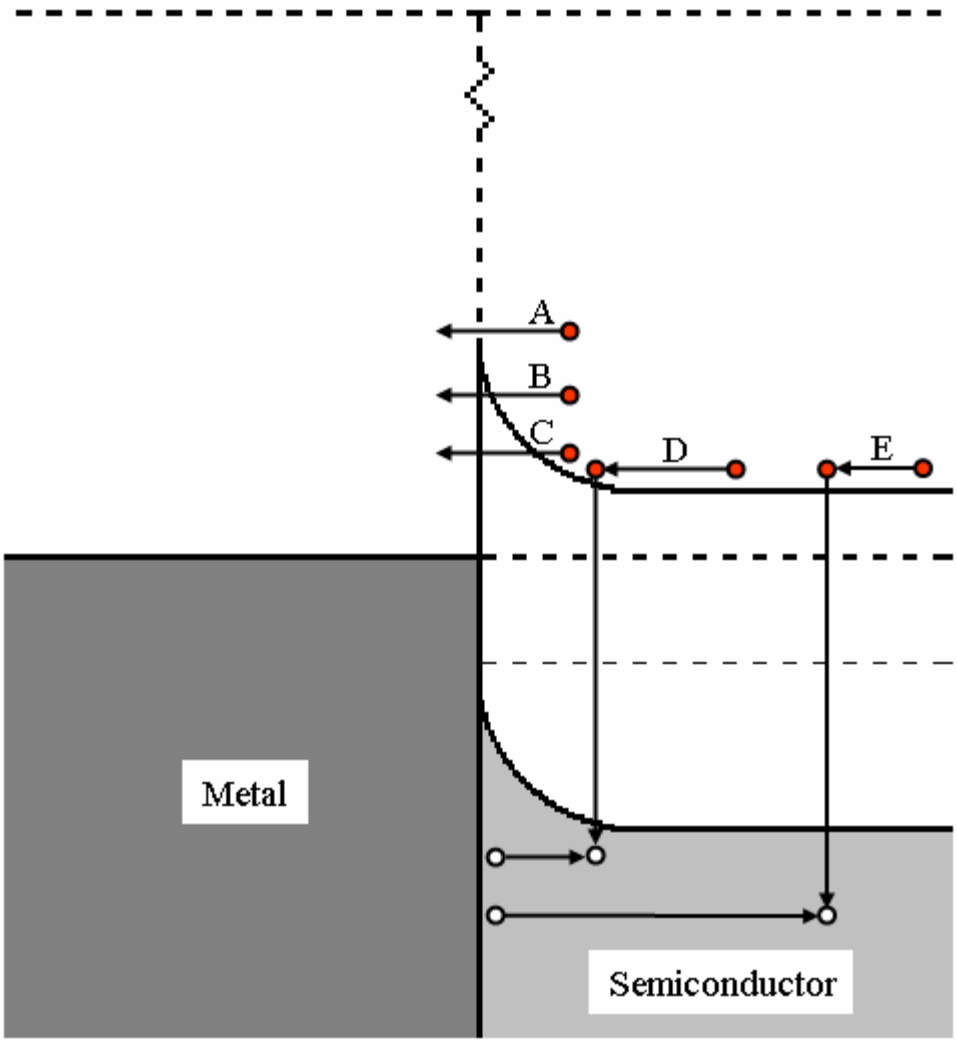

Figure 2.9: Current transport processes across a Schottky barrier between a metal and an n-type semiconductor. “A” represents thermionic emission, “B” represents thermionic field emission, and “C” represents field emission. “D” represents recombination in the depletion region and “E” represents hole injection. In all cases, filled circles represent electrons, while empty circles represent holes.

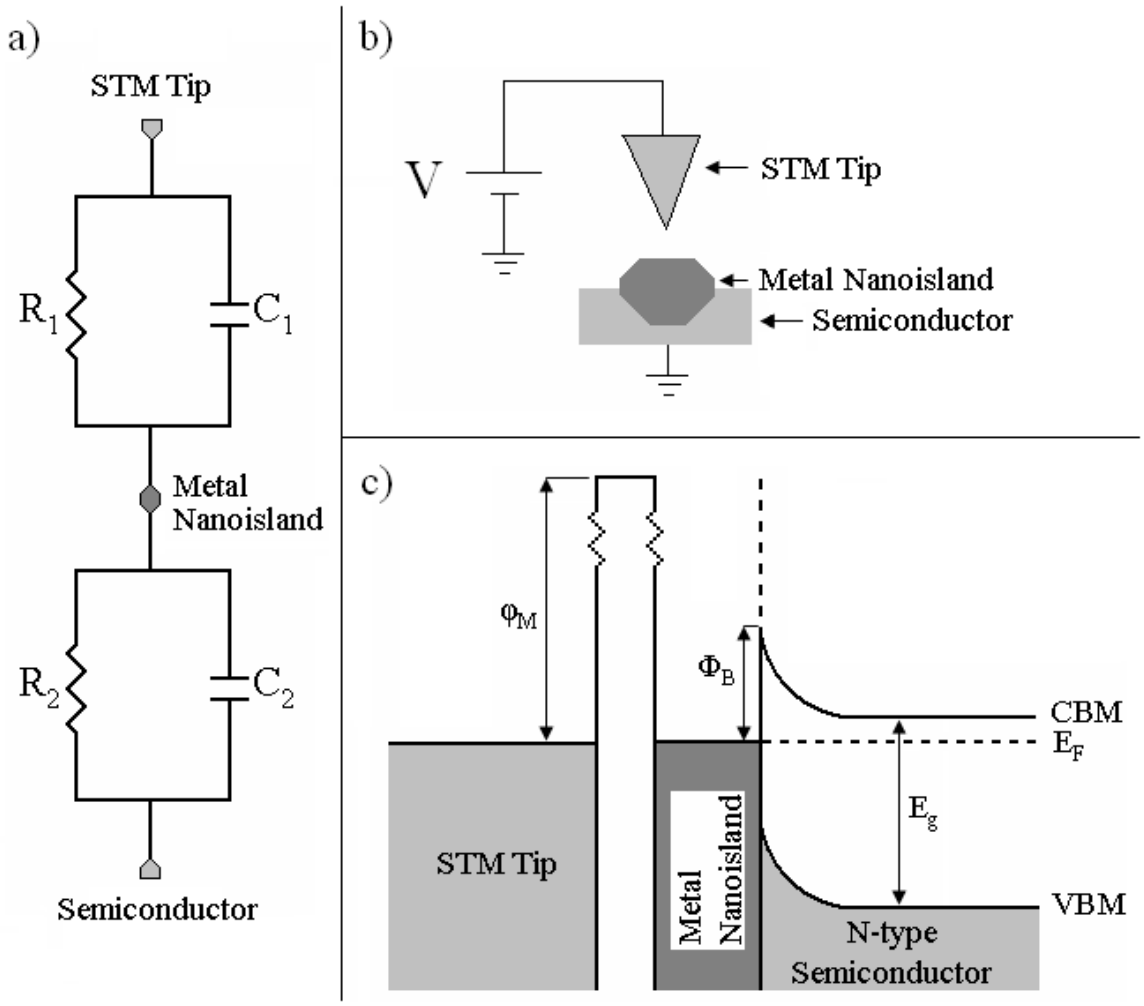

Figure 2.10: STM tip-metal nanoisland-semiconducting substrate double barrier tunnel junction (DBTJ). (a) Circuit diagram of the DBTJ with the electrodes labeled. (b) Schematic of the DBTJ. (c) Band diagram of the DBTJ. Note that the example band diagram shows features an n-type semiconductor, however, the theory would be successful with a p-type semiconductor, as well.

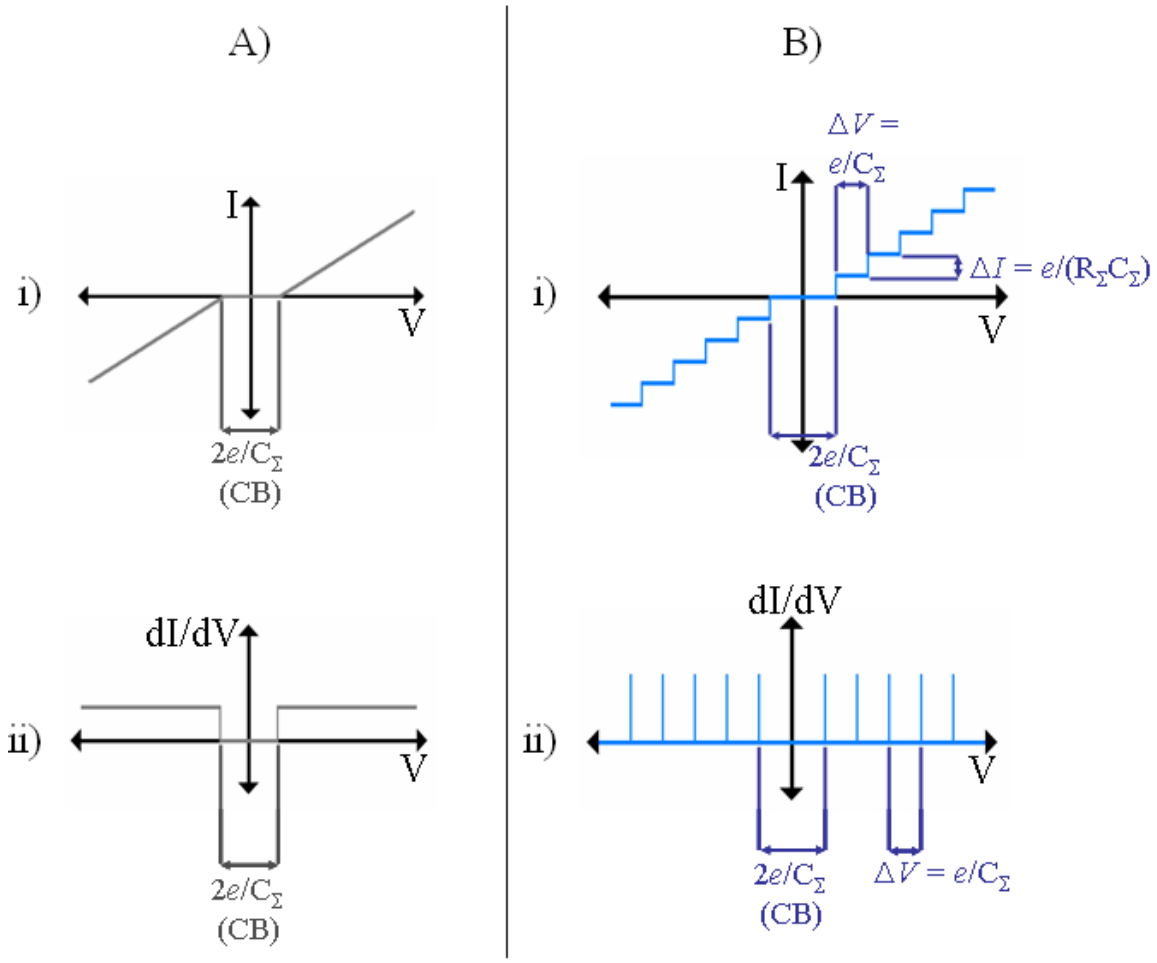

Figure 2.11: Simplified diagrams of I-V and $\left(\frac{dI}{dV}\right)-V$ curves that demonstrate SET signatures. (a) Simplified (i) I-V curve and (ii) $\left(\frac{dI}{dV}\right)-V$ curve for the Coulomb blockade. (b) Simplified (i) I-V curve and (ii) $\left(\frac{dI}{dV}\right)-V$ curve for the Coulomb staircase.

Chapter 3:

Experimental Facilities and Procedures

3.1. Introduction

The field of physics has always thrived on the co-existence of theorists and experimentalists, who together, through numerous theoretical and experimental studies, have shaped the field into what we know today. While modern theoretical studies can be accomplished with some combination of computer technology and ingenuity, experimental studies feature an additional requirement: equipment with which to perform sample preparation and analysis. The pieces of experimental equipment featured in this study fall into two distinct categories: ultrahigh vacuum (UHV) systems and ambient systems.

3.2. UHV Systems

The accurate study of the electrical properties of silicide nanostructures on silicon substrates requires that the interface between the nanostructures and the substrate be clean to eliminate the effects of contaminants on these properties. For instance, it has been suggested that the existence of an oxide layer at the nanostructure-substrate interface would increase the Schottky barrier height by increasing the amount of trapped surface charge [1]. Carbon contamination at the interface would negatively affect the electrical properties in other ways, such as causing the formation of a different compound than the intended silicide.

To ensure that the sample remains nominally free of contamination during the course of the experiment, it is essential that the study be performed in ultrahigh vacuum (UHV) conditions, both during sample preparation and examination. The facilities used in the studies presented in this dissertation, the Multiprobe P Surface Science System, the Small System, and the Integrated Surface Analysis and Growth System (ISAGS), are all UHV systems capable of *in situ* sample preparation, which allowed for the studies of the electrical characteristics to be performed without fear of contamination.

3.2.1. Multiprobe P Surface Science System

The Multiprobe P Surface Science System, shown in Figure 3.1, is a custom-designed commercial UHV system for sample preparation and analysis built by Omicron Nanotechnology GmbH. It is comprised of two UHV chambers, known as the preparation chamber and the analysis chamber, and a fast entry loadlock to allow samples (as well as tips and cantilevers) to be introduced and exchanged relatively quickly without the need to vent the entire system. The Mulitprobe P is built into its own table, with integrated heating assemblies for bakeouts and gas lines for venting the loadlock and the chambers, as well as for supplying the inlet gas for sputtering. The table is hollow, as shown in Figure 3.2, and contains a space for ion pumps for both chambers, as well as heating elements to bake the ion pumps. The Multiprobe P is also equipped with a stainless steel bakeout cover that completely encloses the system during bakeout, as shown in Figure 3.3, allowing for highly efficient heating and short bakeout times. Bakeouts are controlled automatically using the integrated System Controller, which allows users to set the bakeout temperature, temperature ramping speed, and bakeout time. Typically, a twenty-four bakeout is all that is necessary to

achieve pressures in the 10^{-11} torr range. However, if the chamber has been contaminated or has been left at pressures greater than 10^{-10} torr for extended periods of time, bakeouts of several days may be required, and these longer bakeouts can also be controlled automatically via the System Controller.

A VAT UHV gate valve separates the loadlock and the preparation chamber and an identical gate valve separates the preparation and analysis chambers. Transfers between the chambers are accomplished by using magnetic probes, which are indicated by arrows in Figure 3.1. The preparation chamber is pumped by a VacIon Plus 150 ion pump, allowing it to reach a base pressure of 7×10^{-11} torr, and the analysis chamber is pumped with a VacIon 300 ion pump, allowing it to reach a base pressure of 1.5×10^{-11} torr at room temperature. The loadlock is pumped by a Pfeiffer TMU 261 turbomolecular drag pump backed by an Edwards RV3 roughing pump. This pumping combination is capable of reaching pressures in the 10^{-8} torr range within 45 minutes of startup and has an attainable final pressure of 4×10^{-10} torr [2]. The TMU 261 is equipped with a fan for air cooling and a venting valve (Pfeiffer TVF 005) for automatic venting during turbopump shutdown. The turbopump and roughing pump are both controlled remotely through the TC 600 electronic control unit. Pressures in both chambers are monitored using nude ion gauges with thoriated iridium filaments, capable of monitoring pressures from the $10^{-4} – 10^{-12}$ torr [3]. Both chambers contain sample manipulators that allow for radiative and direct resistive heating of samples and sample cartridges. Radiative heating of sample cartridges is accomplished by using a pyrolitic boron nitride (PBN) heater embedded within the manipulator, while samples can be resistively or radiatively heated within the sample cartridges owing to a system of electrical contacts built into the manipulator. Both chambers are equipped with a Vacuum Generators ST22 titanium

sublimation pump (TSP). The configuration of both TSPs is identical. Each TSP is mounted horizontally on a 2.75" conflat flange and has three 2.0 mm diameter TiMo alloy filaments that can individually sublime a film of titanium on to a stainless steel plate situated directly above the filaments [4]. This titanium film acts as an effective gettering agent for oxygen, hydrogen, carbon monoxide, and other non-noble gases, with room temperature pumping speeds of up to ~9 $Ls^{-1}cm^{-2}$ [4]. The TSPs can be configured to operate either manually or automatically evaporating titanium at pre-determined intervals.

The preparation chamber is equipped with a sputter ion source (ISE 10) and two electron beam evaporators (EFM 3T and EFM 3). These devices allow for *in situ* sample preparation via sputter cleaning and deposition. The ISE 10 is connected to a gas line integrated into the Microprobe P table that is baked during a standard bakeout, allowing for sputtering gases to remain uncontaminated. The ion beam can also be focused manually, allowing for a beam diameter ranging from 3 – 12 mm [5]. The EFM 3T contains three cells for evaporant sources in the form of rods or crucibles, depending on the material to be deposited. Currently, the three sources in the evaporator are pieces of a 1 mm diameter cobalt rod (Johnson Matthey Grade 1) in a custom-made molybdenum crucible (shown in Figure 3.4(a)), a 3.175 mm × 3.175 mm gold slug (Alfa Aesar 99.995% purity) in a commercially-available molybdenum crucible with a Al_2O_3 liner (shown in Figure 3.4(b)), and a 2 mm diameter titanium rod (Goodfellow 99.99% purity). A 2 mm diameter silicon road (Goodfellow 99.999% purity) and a 1.5 mm diameter dysprosium rod (Rare Earth Metall Limited 99.9% purity) have also been used as deposition sources. The EFM 3 is a single source evaporator that currently holds a 3.125 mm diameter Pt rod (Goodfellow 99.99% purity) with a piece of 0.25 mm diameter tungsten wire (Alfa Aesar 99.95% purity) wound

around it for added stability during evaporation. This EFM 3 has been factory-modified to allow for the repeatable deposition of platinum contact pads for use in lateral transport measurements of nanostructures. A custom extension was added to reduce the nozzle-to-sample distance, and the exit apertures are interchangeable upon removal from the preparation chamber, allowing for the deposition of different sizes of contact pads. The custom extension adds 50 mm to the total travel distance of the evaporator nozzle, and is stable when fully extended, allowing for controllable, repeatable deposition of uniform contact pads. Deposition with either evaporator is controlled using one of two EVC 300 power supplies (having two power supplies allows simultaneous deposition of two materials [6]). Both evaporators are water-cooled to maintain overall chamber cleanliness by preventing heating of evaporator components other than the deposition source during evaporation. Water-cooling allows the evaporators to operate in the 10^{-10} torr range during deposition of all but the most refractory metals [6]. In addition to sample preparation facilities, there are eight additional ports on the preparation chamber (two 4.5” ports and six 2.75” ports), allowing users to expand the capabilities of the Multiprobe P. A residual gas analyzer (Stanford Research Systems RGA 100) is currently mounted on one 2.75” port, allowing for monitoring of the cleanliness of the system, and a UHV leak valve is mounted on another 2.75” port.

The analysis chamber is actually the moniker of two chambers connected via an open 8” flange. The first chamber contains facilities for low energy electron diffraction (LEED), Auger electron spectroscopy (AES), and the sample manipulator. The sample manipulator has been described previously. The LEED system (Omicron SpectaLEED rear view LEED) is an analytical instrument designed to allow for observation of diffraction patterns from a

crystalline sample. The LEED consists of an electron source with a thoriated tungsten filament encased in a mu metal shielded cylinder and set in front of a fluorescent screen. The screen is configured in such a way that the diffraction pattern can be viewed from both in front of the screen as well as from behind (i.e. rear view). The LEED also contains an external rotary drive that actuates an internal retraction mechanism, allowing the LEED screen to be moved relative to the sample to allow for additional room for sample manipulation as well as optimization of the LEED pattern. The integral electron source of the LEED allows for electron energies up to 3.5 keV, thus, the LEED can be adapted for use in retarding field Auger analysis without the need to provide an external excitation source for AES [7]. The LEED optics are controlled via the NG LEED power supply and control unit, allowing for control of the settings of the electrical supplies for the LEED optics. The high voltage for the screen can be set from 0 – 7 kV, the suppressor grid voltage can be set to optimize the suppression of secondary electrons, and the filament current can be manually set from 0 – 1.7 A [8]. The electron energy is adjustable from 0 – 999.9 eV, while the voltage settings on the internal grids can be adjusted to optimize the diffraction pattern on the screen. There is no way to adjust the electron spot size. However, the diameter is ~1.8 mm [7]. While some LEED systems have a devoted CCD camera for viewing diffraction patterns [9], the LEED on the Multiprobe P currently has no camera devoted to recording patterns. However, there are plans to add a camera mount to the chamber, which would allow multiple cameras to be interchangeably mounted for pattern recording [10].

The other analytical component in the analysis chamber, the AES system (CMA 150) consists of two coaxial cylinders acting as a bandpass electron energy filter, channeling the electrons (from the electron gun capable of generating an electron beam of 0 – 5000 V) into a

channel electron multiplier (Channeltron CEM) for electron detection. The CEM can be operated in either analog or pulse counting (digital) mode, depending on the beam currents needed. Analog mode allows for primary beam currents of 500 nA – 1 uA, while the digital mode allows for a high signal-to-noise ratio when using low beam currents of 1 – 500 nA [11]. It is possible to switch between the two modes through an exchange of preamplifiers and by changing settings within the control electronics. The CMA 150 system also contains an integrated lock-in oscillator (LIO), with a sensitivity range of 300 μV – 1 V, an oscillator amplitude range of 0 – 10 V, a time constant range of 3 ms – 10 s and a phase that can be set through a full 360º. The lock-in can be operated either in low drift mode, for high stability, or high dynamic reserve mode, which has a high overload capability [12]. The electronics and the LIO can be remotely controlled using the program DATAuger, allowing for automated scanning through an energy range of 0 – 3500 eV, and either 4.75 kHz or 9.5 kHz can be used as the reference frequency, for LEED or AES, respectively. The software can be configured to recognize either f or 2f (double the aforementioned frequencies) as the reference frequency of the LIO. The DATAuger program saves scans in a tab-delimited ASCII format and contains facilities for simple data processing, such as smoothing through 3- or 5-point adjacent averaging.

The second chamber contains the microscope stage, as shown in Figure 3.5. The vibration isolation system on the microscope stage consists of four soft springs, each surrounded by a stainless steel column for protection, yielding a resonant frequency of the spring suspension system of 2 Hz [13]. Other vibrations are intercepted by a ring of copper plates situated between permanent magnets that comprise the nearly non-periodic eddy current damping mechanism and successfully damp vibrational excursions in all directions

[13]. The microscope also contains a cryostat that will be discussed in detail later. However, it utilizes a highly flexible copper braid for the thermal connection, and to minimize vibrations from this braid, it is mechanically decoupled from the microscope stage at a special copper braid decoupling stage [13]. The vibration isolation system is effective by itself and does not require that the system table be suspended on pneumatic legs. In fact, due to the efficacy of the vibration isolation system, it is possible to achieve and maintain atomic resolution in STM mode with both the turbopump and the loadlock roughing pump running at full speed. The microscope stage can be locked, neutralizing the vibration isolation system, for purposes of sample/tip/cantilever transfer, spring adjustment, or other purposes using a push-pull motion drive (PPM).

Omicron has developed an innovative sample transfer mechanism for transfers within the analysis chamber. Such transfers are performed with the wobblestick instead of a standard magnetic probe. The wobblestick is a specially-designed double-action pincer grip manipulator, and is indicated in Figure 3.5. By squeezing the trigger outside the analysis chamber, both jaws can be opened and closed. The jaws securely grab and hold on to the tab of the sample cartridge, indicated in Figure 3.6. With the sample cartridge held by the wobblestick, it can be maneuvered into the sample storage carousel or into the microscope stage, both indicated in Figure 3.5. Once transferred to the microscope stage, however, additional care must be taken because three molybdenum clips are positioned within the microscope stage. The clips serve to ground flat sample plates and securely hold sample cartridges. If these clips are bent, sample cartridges will become loose, and a vibration can be induced in the images obtained by the microscope [14].

Though the microscope is known as the VT AFM, it is capable of operating as either a scanning tunneling microscope (STM) or an atomic force microscope (AFM), requiring only that the tunneling tip be exchanged for a cantilever or vice versa and the software be switched from one mode to another. While contact mode AFM and non-contact modes AFM are the only modes explicitly available given the current configuration of the electronics and software, it is also possible to use the VT AFM to perform conducting tip atomic force microscopy (*c*-AFM), electrostatic force microscopy (EFM), and lateral force microscopy (LFM) measurements. The system is equipped with a separate controller, the Kelvin control unit (KCU) to allow users to perform Scanning Kelvin Probe Microscopy (SKPM) measurements.

The VT AFM is also equipped with a second motorized probe custom-designed for this system by Omicron. The motorized probe is designed to be brought into contact with the platinum contact pad, which would function as the second contact for lateral transport measurements of nanostructures touching the pad. It has two axes of motion, being able to move along the z-axis and laterally along an axis oriented 45º relative to the x-axis. It is composed of spring-hardened copper beryllium alloy ($CuBe_2$) and is connected directly to a shielded high-voltage male BNC connector on the exterior of the analysis chamber. It is important to note that the second contact will only be fully effective if sample cartridges are used with a custom-designed ceramic top plate that has embedded electrical contacts.

The VT AFM is a variable temperature system, meaning that it can actively scan in any of the modes continuously throughout the temperature range of 25 K – 750 K. The microscope is able to scan continuously due to the design of the sample stage and the scanner. The scanner is equipped with a built-in heat shield that prevents the scanner tube

from being gradually heated or cooled by the sample, preventing long-term drift [13]. Furthermore, the sample stage is designed in such a way that the surface sample is the reference plane for thermal expansion or contraction [13]. This design keeps the tip-sample distance essentially constant during heating or cooling, allowing continuous scanning. For cooling, temperatures below room temperatures are achieved by use of a liquid helium cryostat. Cryogenic liquid, either liquid helium or liquid nitrogen (provided that a vertical withdrawal dewar is used), is pulled through the heat exchanger of the cryostat using an Edwards RV3 roughing pump. The transfer of thermal energy is accomplished via a flexible copper braid that is in contact with a gold clamping block that is lowered into contact with the bottom of the sample cartridge during cooling (the sample cartridge is inverted prior to loading into the microscope stage). The clamping block serves to ensure that the sample is cooled while the rest of the microscope, including the tip/cantilever, remains at near room temperature. Heating is accomplished by using electrical contacts to send current directly through the sample, using the direct current sample cartridges, shown in Figures 3.6(d) – 3.6(f), or through the PBN heater in the resistive heating sample cartridge, shown in Figure 3.6(c).

The temperature sensor is embedded in the clamping block, which allows for monitoring of the sample temperature using a Lakeshore 331 Temperature Controller. The Temperature Controller is configured to have a useful temperature range of 1.4 K – 475 K, and outside of this temperature range, it will not report a numerical value [15]. However, because the temperature sensor closest to the sample is in the clamping block and not at the sample, there is an offset between the temperature reported at the controller and the real temperature of the sample due to thermal losses by the sample cartridge, so that the real

temperature is lower (higher) than the value reported by the controller when above (below) room temperature. The low temperature offset has been measured by Omicron, and values of the offset at several temperatures are recorded in the system documentation. For sample temperatures above room temperature, electrical contacts in the microscope stage allow for direct resistive heating or radiative heating of the sample, depending on the type of sample cartridge used. Unfortunately, the high temperature offset is not reported by Omicron. However, an optical pyrometer is a reliable way to measure the sample temperature in the high temperature regime [16].

3.2.2. Small System

The Small System, described previously (in whole or in part) by Hyeontag Jeon [17], Hoon Ham [18], and Jaehwan Oh [19], is a home-built UHV system, shown in Figure 3.7, that has a base pressure of 5×10^{-11} torr. The Small System is installed on an optical table, with legs that can be pressurized with dry nitrogen to "float" during measurements requiring vibration dampening. There are three chambers, the metallization chamber, the analysis chamber, and the microscopy chamber, that are directly connected to each other, pumped by a 230 L/s ion pump (Varian StarCell VacIon Model 919-0105) located directly beneath the analysis chamber, and a fast entry loadlock to facilitate sample introduction. The loadlock is pumped by the combination of a turbomolecular drag pump (Pfeiffer TMU071P) backed by an oil-free diaphragm pump (Pfeiffer MVP 035-2). Samples are moved throughout the Small System using magnetic transfer probes that are electrically isolated from the chamber. The magnetic transfer probe that moves samples between the metallization chamber and analysis chamber contains an electrical lead, allowing for electrical contact with samples for the

purposes of LEED and AES. There is also a small storage rod in between the analysis and metallization chambers, allowing a sample to be kept in UHV conditions, even while tips are being exchanged. The Small System utilizes a series of eight interlocked heating tapes that are wrapped around the chambers and covered with aluminum foil during bakeouts.

The metallization chamber contains a single crucible electron beam evaporator (Thermionics) for deposition of metals. The crucible is water-cooled, with a fluid flow switch (Proteus Industries Standard Series) serving as the interlock for the Thermionics power supply used during deposition. Metal deposition is controlled using a Thermionics remote control and deposition is monitored using a quartz crystal rate monitor (Sycon STM-100/MF). The chamber also contains a heater for radiative heating of samples during deposition. The heater consists of a coiled tungsten wire wrapped in a circle at the bottom of a stainless steel tube with pyrolitic boron nitride for heat isolation. A type-C thermocouple is mounted in the center of the circle of wire and it extends below the plane of the wire. The heater is mounted on a vertical extension system that allows the heater to be moved up and down and the thermocouple can be brought into contact with the sample in order to more accurately measure the temperature that the sample has reached. The heater is controlled remotely via a Eurotherm 818 Controller/Programmer.

The analysis chamber contains a mechanism for direct heating of samples, as well as an electron gun for studies utilizing LEED and AES. The commercial LEED system (Princeton Review Instruments) contains a mu-metal cylinder for radiation shielding and is controlled by the Perkin-Elmer PHI Model 11-020 LEED electronics control unit. The LEED electron gun is used for AES studies, and the AES system is coming known as a Retarding

Field Analyzer AES (RFA AES). Despite not having a dedicated system for AES, there is a separate controller for AES (Perkin-Elmer PHI Model 11-500A AES System Control).

The microscopy chamber contains a commercial room temperature STM (Park Scientific Instruments Autoprobe VP2). Park Scientific Instruments (PSI) no longer exists, as it has merged with several companies over the years (PSI merged with TM Microscopes, who then merged with Digital Instruments to form Thermomicroscopes, who then merged with Veeco). Unfortunately, Veeco no longer supports the Autoprobe VP2 and no one associated with the development of the Autoprobe VP2 is currently employed by Veeco [20]. Therefore, maintenance and troubleshooting of the VP2 are the sole responsibility of the user(s).

In addition to room temperature STM measurements, The Autoprobe VP2 is configured for contact mode and non-contact mode AFM measurements. While STM measurements can be made using any metal tip (the shaft of the tip must have a maximum diameter of 0.5 mm), AFM measurements must be made using PSI Piezolevers [21]. In addition to AFM and STM modes, the VP2 can also be used to image the conductance of the sample (the ratio of the change in tunneling current to the change of the applied bias voltage generating that current) using the pre-amplifier, the interface module, and a lock-in amplifier [22]. Conductance and topographical images are recorded simultaneously to enable comparisons between the surface topography and the surface electronic properties [22].

As currently configured, the VP2, shown in Figure 3.8, is capable of movement in the x and z directions and the translation stage has a total horizontal range of 8 mm and total vertical range of 14 mm [21]. During scanning, the piezoelectric tube has a lateral range of 10 μm and a vertical range of 2.5 μm [21]. The sample stage has been modified to accept 1”

diameter wafers in a circular sample ring, which is indicated in Fig 8. The sample ring is made of Macor, a machineable ceramic, and is mounted to the sample stage using Torr-Seal, a UHV-compatible epoxy developed by Varian Vacuum Products. The sample ring acts as a large thermal mass to dissipate heat and reduce the levels of thermal drift following sample heating. The sample ring is capable of accepting standard puck-shaped 1" sample holder, shown in Figures 3.9(a) and 3.9(b), as well as a custom-designed sample holder, shown in Figures 3.9(c) and 3.9(d), built to allow direct current heating of samples in the small system.

In addition to the optical table, the Autoprobe VP2 also has an internal vibration isolation system consisting of a dual stage spring suspension system, indicated in Figure 3.8, consisting of two rings of four stainless steel springs each, with the inner ring suspended from the outer ring, as well as an eddy current damping system of copper plates between rare earth magnets. The vibration isolation system was always more efficient at night, when ambient activity was reduced, however, it is sufficient to allow for atomic resolution, as shown in Figures 3.10(a) and 3.10(b). A tip carousel, indicated in Figure 3.8, is available to hold up to six tunneling tips or cantilevers, allowing tips to be stored for future use. A tip transfer mechanism, shown in Figure 3.11, was constructed to allow for the exchange of tunneling tips and Piezolevers through the loadlock in order to avoid venting the entire system. The Autoprobe VP2 is also equipped with a filament made from 0.127 mm diameter molybdenum wire (Alfa Aesar 99.95% purity) that is used for *in situ* cleaning of tunneling tips by electron bombardment. The filament can also be used to test the tips for suitability for atomic resolution using field emission. By reverse biasing the tip, the filament can be used to detect the field emission current from the tip, if such a current is measurable. It has been

suggested that a measurable field emission current indicates that a tunneling tip can generate atomic resolution [23].

3.2.3. Integrated Surface Analysis and Growth System (ISAGS)

The Integrated Surface Analysis and Growth System (ISAGS), otherwise known as the UHV transfer line, is a home-built system of fourteen stainless steel chambers (with room available for a fifteenth chamber), each designed to house a different system for sample growth and/or sample analysis. The ISAGS is commonly known as the transfer line due to the nearly 59 foot long segmented stainless steel tube to which each chamber is connected, that is held at a base pressure in the low 10^{-9} – mid 10^{-10} torr range due to five Cryo-Torr 8 cryopumps, stationed at equal distances along the length of the line.

The ISAGS has been described in detail by Kieran Tracy [24] and Franz Köck [25], however, there have been changes made in the years since those description was written, the most notable change being that the system has been moved to a longer room specially designed for it [26]. Moving the ISAGS to a longer room ensured that several chambers did not have to be mounted in "piggyback" fashion, as shown in Figure 3.12, but could be mounted individually on to the transfer line, as shown in Figure 3.13. The custom-designed cart used for transporting samples and the standard puck-shaped sample holders described by Tracy [24] are both still the same now as they were in 2000. The sample holders used in the ISAGS are the same as those shown in Figures 3.9(a) and 3.9(b).

As shown in Figure 3.13, there are three molecular beam epitaxy (MBE) chambers: a gas source MBE (GSMBE) chamber, a solid source MBE (SSMBE or Si-Ge MBE) chamber, and an oxide MBE chamber. Tow chambers are also present for ultraviolet photoelectron

spectroscopy (UPS) and x-ray photoelectron spectroscopy (XPS), as well as angle-resolved ultraviolet photoelectron spectroscopy (ARUPS). There are four chemical vapor deposition (CVD) systems: the ECR CVD, the diamond CVD reactor, the hydrogen remote plasma-enchanced CVD (H_2 RPECVD, also known as H_2 plasma), and the oxygen RPECVD (also known as the O_2 plasma). Also present are three chambers used for different emission experiments, the thermionic emission chamber, the field emission chamber, and the ITO chamber. The ITO chamber is so-named because the window is coated with a film of indium tin oxide for use during emission experiments [27]. A metallization chamber is also present, and it was the primary ISAGS chamber used during this study.

The metallization chamber is a 6" six-way stainless steel cross connected to a 10" six-way stainless steel cross. Both six-way crosses are double-walled for the purposes of water-cooling the chamber. The metallization chamber is pumped by a Cryo-Torr 8 cryopump, which provides a base pressure below 1.5×10^{-10} torr. The cryopump, in tandem with water cooling during evaporation, ensures that pressure in the chamber during evaporation typically does not rise above the high 10^{-9} torr range. The metallization chamber is equipped with a five-pocket crucible, with each pocket containing one of the deposition sources. The crucible is located on a linear motion feedthrough, which allows the desired source to be moved into the optimal deposition position in front of the filament. Electrons from the filament are directed magnetically toward the source and evaporate material on to the sample located directly over the crucible. The sample cup contains a tungsten filament, allowing samples to be heated during deposition. Deposition amounts are measured using a quartz crystal oscillator connected to a Sycon rate monitor capable of measuring deposition amounts in increments of 0.1 A. To ensure that the material evaporated from the source is pure during

deposition, a screen is mounted on a linear feedthrough that is moved in front of the sample to prevent material from being deposited on the sample before the evaporant stream is pure. A second linear feedthrough is equipped with a mask that is used for deposition of large area contact pads on to the sample. The mask can be positioned in front of the sample cup while the screen is still in place, assuring that there is no additional deposition on the sample other than the contact pads.

3.3. Ambient Systems

At times, it becomes necessary to remove a sample from the UHV chamber it has been in and expose it to atmospheric conditions. Once this is done, an oxide layer will rapidly form on its exposed surfaces. There are several reasons necessitating removing a sample to atmosphere and thus contaminating it with an oxide film, such as the need to utilize an analytical technique not available in the current UHV chamber (such as atomic force microscopy) or for the sample to undergo some chemical process (such as wet etching).

There are techniques used to avoid oxidation of a sample's surface, such as hydrogen passivation. In ambient conditions, a sample can be passivated by exposing it to a liquid containing hydrogen, such as hydrofluoric acid (HF) or ammonium fluoride (NH_4F). In UHV conditions, where it would be impractical to expose the sample to a liquid, hydrogen passivation is typically accomplished by exposing a clean surface to atomic hydrogen, such as in a hydrogen plasma. In either case, the hydrogen atoms bond to the dangling bonds on the clean surface, leaving no available sites for oxygen atoms to bond later. These layers of hydrogen passivation are not permanent and will typically only last for several minutes [28], although some reports suggest that it is possible to create a stable hydrogen-terminated

surface for times ranging from several hours [29-31] to several days [32]. Another method to forestall oxidation is to deposit a thin layer of gold on the surface. Gold will not oxidize in air, and a thin film of no more than a few monolayers will typically mimic the surface features beneath the film. It is also possible to deposit large contact pads of gold for study of large scale surface or bulk electrical properties. Depositing large gold contact pads on top of arrays of nanostructures allows for the study of the electrical properties of those nanostructures, although the values determined in this manner would correspond to the entire set of nanostructures under the contact pad as a whole, not to the individual nanostructures.

3.3.1. Atomic Force Microscopy (AFM) Systems

There are two ambient AFM systems utilized in this study, the Thermomicroscopes Autoprobe CP-Research (CP-R) and the Park Scientific Instruments (PSI) Autoprobe M5 (M5). They are discussed in further detail below.

3.3.1.1. Autoprobe CP-Research

The Thermomicroscopes Autoprobe CP-Research (CP-R) is an ambient AFM with a high resolution scanner that has been equipped with electrical connections in order to perform piezoelectric force microscopy (PFM), EFM, SKPM, *c*-AFM, and other AFM techniques requiring the sourcing of voltage to the cantilever. However, the AFM has a series of attachments that can be added to enable users to perform additional measurements. For example, the CP-R has an attachment known as the “liquid cell” allowing for AFM measurements to be performed in liquid environments, which is invaluable for AFM of biological molecules. The CP-R also has several switches that allow it to be automatically

switched between several different microscopy modes, such as contact AFM mode, non-contact AFM mode, a mode for LFM, as well as a mode for STM measurements [33].

The CP-R consists of two components: the probe head and the sample stage. The probe head contains a deflection sensor, consisting of a laser diode, a mirror, and a position-sensitive photodetector (PSPD). The probe head also holds a probe cartridge that contains a removable chip carrier with an AFM cantilever mounted to it. The probe cartridge slides along side rails and locks into place to bring the chip carrier into a precisely-defined position. The laser is maneuvered so that it illuminates the end of the cantilever and is reflected on to the mirror and then on to the PSPD. When the laser spot is illuminating the center of the PSPD, it is in the optimal position and will generate the strongest signal. The probe head also contains an X-Y translation stage for moving the cantilever in the x and y directions, as well as a Z stage for moving the probe head up and down. The Z stage is controlled by the ProScan control software.

The sample stage of the CP-R is directly below the probe head and consists of a circular disk with a magnet in the center for holding samples during scanning. If the samples being scanned are non-magnetic, they must be fixed to a metallic sample plate. The stage rests on top of the scanner, a piezoelectric ceramic tube, which rasters the sample holder back and forth, while the cantilever is held stationary, thus generating the image. ProScan, the software controlling the Autoprobe CP-R, acquires the image and then stops acquiring, though the scanner is constantly in motion unless it is instructed to stop, ensuring that the scanner tube remains “warm”. If the scanner is held motionless for a long period of time, such as, if the software was shut down, then the scanner would experience scanner creep until it was warm again. Scanner creep is manifested by the scanner gradually extending

during a scan and then not retracting, effectively requiring it to be retracted and the sample re-approached. It is important to note that there are two interchangeable scanners, one with a maximum scan size of 100 μm, while the other scanner has a maximum scan size of 5 μm.

3.3.1.2. Autoprobe M5

The Park Scientific Instruments Autoprobe M5 (M5) is an ambient microscope that is typically used for piezoelectric force microscopy (PFM), scanning Kelvin probe microscopy (SKPM), and other AFM techniques requiring that voltage be sourced to the cantilever. It is usually not used for standard AFM because the resolution is not as high as the Autoprobe CP-R. However, the M5 has the distinct advantage of being equipped with a camera with a high-power zoom lens, allowing for the cantilever to be accurately localized on particular target features. For example, if a scratch was made on the sample to identify a domain boundary, that scratch could be found and the cantilever could be set to scan a particular area relative to the scratch, and this process could be performed accurately and repeatedly. It is impossible to perform this procedure with the same precision using the CP-R. Further detailed information regarding the Autoprobe M5 can be found in the description written by Brian Rodriguez [34].

The M5 uses a ceramic chip carrier to hold the cantilever in the scanning head. Any standard commercial cantilever that can be mounted to the ceramic chip carrier can be used in the M5 [35]. In fact, electrical measurements are made in the M5 by securing a conductive cantilever to a chip with epoxy, and also mounting a metal wire with an Amphenol connector to the chip using conductive epoxy. Silver paint is used to make electrical contact between

the cantilever and the wire, ensuring that electrical signals can travel between the electrical devices (source measure units, lock-in amplifiers, etc.) and the sample.

3.3.2. Testing Station

The Testing Station is a home-built system capable of making current-voltage (I-V) and capacitance-voltage (C-V) measurements of large scale contacts. The heart of the Testing Station is a Rucker and Kolls Model 260 Probe Station. The sample stage of the probe station is a nickel plate with built-in elements for heating and vacuum components to secure large samples during testing. The stage has two probe arms with a full range of motion along the x-, y-, and z-axes. The probe arms (Quater Research & Development P/N A-20235) are secured via magnets to a metal ring above the sample stage, and they can be fitted with any type of test probe. While many measurements of thin films and delicate materials are performed using spring-loaded probes with a gold-coated (to avoid oxidation that would prevent electrical contact with the sample) ball-shaped end (to avoid puncturing thin films), none such probes are currently available. The test probes that are available are suitable for the measurements that have historically been performed using the Testing Station, and are standard tungsten probes manufactured by American Test Probe & Technologies, Micromanipulator, Pacific Instruments, Quater Research & Development, and Terra Universal. There are several different types of sharpened tungsten needle probes available for use, with tip radii ranging from 1 μm to 25.4 μm. There are also probes consisting of tungsten shafts with a 25.4 μm diameter tungsten wire attached to them for use in high vibration and delicate in-circuit measurements.

The system is equipped with electrical connections and electronic controls for performing both current-voltage (I-V) and capacitance-voltage (C-V) measurements, and the station can be converted from one method to the other by reconfiguring the electrical connections and turning on the appropriate control unit. The electronic control units and the computer are connected via an IEEE-488 GPIB cable with stackable connectors. The testing station is set inside a cubical (~22" per side) black metal enclosure. The front face of the enclosure in hinged and opens to allow access to the probe station. The black metal enclosure serves a dual purpose, acting as a Farday cage, and preventing stray light from interfering with measurements when the door is closed.

I-V measurements are performed using either a Keithley 236 Source Measure Unit (SMU) or a Keithley 237 High Voltage SMU to apply the bias voltage to the test probe. The Model 236 SMU is capable of sourcing voltage in the range of ±100 μV – ±110 V, while the Model 237 SMU has an extra source range, enabling it to source up to ±1100 V [36]. At the same time, both SMUs are capable of measuring current in the range of ±10 fA – ±100 mA (if using the extra source range of the Model 237 SMU, the upper limit of the range is ±10 mA) [36]. Both SMUs have user-configurable compliance limits to ensure that the external circuits or devices under test are not damaged due to excessive current. Both SMUs are also capable of sourcing current, while measuring voltage, however, that was not done during this study. I-V data is collected via a Testpoint program that automatically controls the sourcing and ramping of voltage and the data is output in a tab-delimited ASCII file.

C-V measurements are performed using a Keithley Model 250 CV Analyzer, a Keithley Model 595 Quasistatic CV Meter, and a Keithley Model 230 Programmable Voltage Source. C-V data is collected using a Testpoint program and the data is output in a

tab-delimeted ASCII file. The C-V capabilities of the Testing Station were not used during this study.

3.4. Experimental Procedures

3.4.1. Sample Preparation Procedures

Different procedures were used to prepare the silicon wafers for use in the experiments depending on the particular type of study being undertaken. The different procedures were intended to take advantage of the specific circumstances involved in each study.

3.4.1.1. Substrates for room temperature *c*-AFM study

For samples of silicide islands on silicon that would be studied at room temperature only, the initial cleaning procedure that was followed was a variation of the cleaning procedure used by Morgan Ware [37]. Silicon wafers 25.4 mm in diameter were first rinsed in a steady stream of de-ionized water for two minutes while being held with stainless steel tweezers. Wafers were blown dry using research grade nitrogen and were subjected to a UV ozone treatment for five minutes. The UV ozone system utilized did not have its own oxygen supply, therefore, atmospheric oxygen was used. Following the UV ozone treatment, the sample was immediately submerged in 10:1 HF (J.T. Baker), while being held by fluoroware tweezers. While submerged in the HF, the wafers were in constant motion. After one minute, the wafers were removed from the solution and the hydrophobicity of the silicon surface was checked. If the HF ran off the surface, it was assumed that the native oxide had been removed because hydrogen-terminated silicon is hydrophobic, while silicon dioxide is hydrophilic [38]. The wafers were then loaded into the UV ozone system for five minutes,

followed immediately by a one minute HF dip. This process was repeated once more before the wafers were mounted to a standard puck-shaped sample holder using 0.25 mm diameter molybdenum wire. The wire was fixed to ensure that the wafers would not move when mounted, even if the sample holder was shaken.

Wafers were then loaded into the ISAGS loadlock and when the pressure in the loadlock was in the high 10^{-7} torr range, the wafers were transferred on to the cart, and then moved to the metallization chamber, where they were heated radiatively at ~600ºC for ~1 hour before being heated radiatively to ~950ºC for 15 minutes. 0.3 – 1.0 nm of cobalt were then deposited at room temperature and annealed at 880ºC – 900ºC for 25 minutes.

After the samples were removed from the ISAGS, they were imaged with the CP-R to ensure that heteroepitaxial nanostructures had formed. Nanostructures were thought to be heteroepitaxial if their shapes matched those that had been reported in the literature. For example, triangular and hexagonal $CoSi_2$ nanoislands on Si(111) wafers were considered epitaxial [39-40], whereas round $CoSi_2$ nanoislands on Si(111) were assumed to be non-epitaxial and most likely a result of contamination. If the nanoislands were judged to be appropriate for further study, then the wafers were prepared for deposition of the backside ohmic contact. Measurements of the Schottky barrier height are impossible without the backside contact, because without it, the backside will act as a reverse-biased diode. If the underside of the wafer is acting as a reverse-biased diode, the current transport through the actual Schottky diode (the island-silicon interface) will be degraded to the point that measured barrier heights will be inaccurate. Even if the backside film was composed of a metal that would ordinarily form a Schottky barrier with silicon, it was expected that if the

area covered by the film was significantly larger than the area of the frontside Schottky contacts, then the film would act as an ohmic contact due to defects.

The backsides of the wafers were swabbed with 10:1 HF for one minute and the samples were returned to the metallization chamber, where a titanium film was deposited to act as the backside Ohmic contact. A 100 nm thick film was found, during a preliminary study, to be sufficiently thick to create a high quality ohmic contact, one that did not experience voltage breakdown until beyond the range measured, -10 V, and increasing the thickness to 200 nm did not significantly improve the ohmic quality of the backside contact.

3.4.1.2. Substrates for variable temperature *c*-AFM study

Variable temperature *c*-AFM studies of nanostructures could only be undertaken in the Multiprobe P, which necessitated that the 25.4 mm diameter silicon wafers be diced into smaller pieces with sizes of 2 – 3 mm × 9 – 11 mm. Prior to dicing, a metal layer had to be deposited on the backside of the wafer to act as the backside Ohmic contact during I-V measurements. Owing to the fact that the top surfaces of the wafers would be cleaned by direct current heating once in the analysis chamber of the Omicron, the cleaning procedures followed did not focus on the top surfaces, rather they focused on cleaning the backsides of the wafers.

The wafers were held by one corner of the wafer, backside facing up, with stainless steel tweezers (considered more stable for this process than fluoroware tweezers) under a steady stream of deionized water for two minutes. The wafers were then placed backside up in the UV ozone for five minutes. To protect the top surfaces of the wafers, while in the UV ozone enclosure, they were laid on a piece of lint-free delicate task wiper (Kimtech Science

Kimwipes EX-L). After removing the wafers from the UV ozone system, they were submerged in 10:1 HF (J.T. Baker) for one minute. Once removed from the HF, the hydrophobicity of the backside was used to judge whether the oxide had been removed. A five minute UV ozone cycle followed by a one minute HF dip was repeated twice more before wafers were mounted, backside up, on puck-shaped sample holders and secured with 0.25 mm diameter molybdenum wire (Alfa Aesar 99.95% purity).

Wafers were immediately loaded into the ISAGS loadlock and once the pressure had reached the high 10^{-7} torr range, wafers were transferred to the cart, where they were moved directly into the metallization chamber. A 200 nm thick layer of cobalt was evaporated on to the backside of the wafer while it was at room temperature. This layer was intended to act as the backside Ohmic contact instead of a titanium because it was assumed that a titanium film would evaporate during flash annealing to 1100ºC, while a similar cobalt film was likely to be more robust and withstand the flash annealing process [41-42]. Another reason that cobalt was chosen over titanium was that cobalt is much less susceptible than titanium to etching in HF. This was critical because one of the portions of this study called for sample surfaces to be hydrogen-passivated prior to formation of $CoSi_2$ islands. An HF dip would result in a hydrogen-passivated surface, but if the titanium film was removed from the backside, there would be no backside Ohmic contact. Though this portion of the study was not undertaken, the cobalt film was still used.

Following deposition of the cobalt film, wafers were inspected visually to ensure film deposition, and then were removed from the ISAGS. Wafers were diced into pieces with sizes of 2 – 3 mm × 9 – 11 mm using a diamond-tipped scribe, and a number was lightly scratched into one side to aid in identification later. The wafers were mounted on sample

cartridges designed for direct current heating. The sample cartridges were modified slightly in that a small piece of tantalum foil was fixed to each contact foil (also made of tantalum), to extend the contacts to ensure that the cobalt film would be in electrical contact with the contacts on the sample cartridge even if it partially evaporated or coalesced. The modified sample cartridge is shown in Figure 3.6(e). Following a pumpdown time of ~40 minutes, the sample cartridges were transferred to the analysis chamber, where they were outgassed for ~4 – 8 hours using the radiative heater embedded in the sample manipulator. This step acted to clean the sample cartridges to prevent heavy outgassing during flash annealing. The samples were then held at ~600ºC for at least 12 hours (generally overnight) prior to flash annealing at ~1100 – 1125ºC. The flash annealing was performed by heating in short 3 – 5 second bursts, steadily increasing the temperature with each burst by ~25 – 75ºC, depending on the sample, until reaching 1100ºC. Once at 1100ºC, samples were held at this temperature for 30 seconds before rapidly cooling to 900ºC, and then slowly cooling back to room temperature. Samples were held at room temperature for a period of 30 seconds before the temperature was raised to 1100ºC again. This procedure of quickly raising the sample temperature to 1100ºC for 30 seconds, quickly cooling to 900ºC, slowly cooling to room temperature, and waiting 30 seconds before raising the temperature again, was performed from 2 – 4 times, mimicking the procedure used by Jaehwan Oh [19,43].

Following flashing, LEED was used to confirm the surface reconstruction, Si(111):7×7 or Si(100):2×1. STM was then performed AES to check that the surface was free of contamination, and AES scans were made to provide a baseline of the quality of the surface for comparison with the surface following deposition. ~1.0 nm of cobalt was deposited while the Si(111) samples were held at room temperature and while the Si(100)

samples were held at 700ºC. Following deposition, AES scans were used to confirm that cobalt was deposited. The samples were annealed for 20 – 30 minutes at 900ºC and then LEED was performed to ensure that nanostructures had formed on the sample surface. STM was used to gauge the relative epitaxial quality of the nanostructures and how they compared to those reported in the literature [39-40].

3.4.1.3. Substrates for SET study

There was no need for an Ohmic backside contact for studies regarding single electron tunneling (SET). The reason for not needing an ohmic backside contact was because the double barrier tunnel junction (DBTJ) formed by the STM tip-metal island-silicon system is unaffected by the rectifying quality of the back of the wafer. Therefore there was no *ex situ* processing performed for the SET studies as compared to *c*-AFM studies. SET studies were performed in the Mutliprobe P with samples mounted in the direct current heating sample cartridges (shown in Figure 3.6(f)), thus, the 25.4 mm diameter wafers were diced into pieces with sizes of 2 – 3 mm × 9 – 11 mm using a diamond-tipped scribe. Samples were handled with either fluoroware, ceramic, or molybdenum tweezers because handling the samples with stainless steel tweezers would lead to nickel contamination that would cause a higher density of vacancies and surface defects [44-45], which was found to be particularly visible on Si(100) surfaces as compared to Si(111) surfaces, as shown in Figure 3.14. Sample pieces were mounted and loaded into the loadlock and, after ~40 minutes, were transferred into the analysis chamber where the samples were heat cleaned using the same procedure discussed in Section 3.4.1.2, except that the maximum flashing temperature was ~1150ºC.

Following flashing, LEED was used to confirm the surface reconstruction, Si(111):7×7 or Si(100):2×1. STM was then performed to check that the surface was free of contamination, and AES scans were made to provide a baseline of the quality of the surface for comparison with the surface following deposition. 0.1 – 0.2 nm of titanium were deposited while the samples were held at room temperature and then AES scans were performed to confirm that titanium was deposited. The samples were annealed for 1 minute at 800ºC and then LEED was performed to ensure that $TiSi_2$ was formed on the sample surface. Post-anneal observation of LEED spots is typically used to indicate nanostructure formation because once the continuous titanium film formed nanostructures, the underlying substrate would be exposed and the LEED spots could be seen [46].

3.4.2. STM/AFM Procedures

3.4.2.1. Room temperature *c*-AFM study

Once nanostructures had been formed and a titanium layer had been deposited on the backside of the wafer, the samples were ready for study. These samples were removed from the ISAGS and mounted on a stainless steel disk using fast drying silver paint (Ted Pella, Inc. Product No. 16040-30). The sample was loaded into the Autoprobe CP-R and scanned with a doped diamond-like carbon cantilever (Veeco DDESP). Scan sizes of 8 – 10 μm were used to identify nanostructures on which to perform I-V measurements. When appropriate nanostructures were identified, the scanner was stopped and the cantilever was positioned on top of that nanostructure and the I-V curve was acquired using the same type of Testpoint program written for the Testing Station. Several I-V curves were acquired on the same nanostructure to ensure that each measurement was consistent.

3.4.2.2. Variable temperature *c*-AFM study

Once nanostructures had been formed, the samples were transferred into the microscope stage, where they were scanned with a Veeco DDESP cantilever. Large scans of 5 – 8 μm were used to identify nanostructures suitable for I-V measurements. When appropriate nanostructures were identified, multiple I-V curves were recorded on each nanostructure to ensure consistency between each measurement. I-V curves were acquired from -1.0 – 0.5 V because the VT AFM pre-amp saturates at ~333 nA, and it was found that I-V curves would yield ideality factors near unity if they reached 333 nA prior to 0.5 V.

Liquid helium was used to lower the temperature of the sample to allow for studying the temperature dependence of the I-V curves. A slow cool down was utilized to avoid excessively fast thermal drift, which would make following the identified nanostructures more difficult. Multiple I-V curves were recorded at regular temperature intervals. While efforts were made to keep the temperature essentially constant between the measurements on a single island, temperature differences of ~1 K tended to occur. The flow of cryogenic liquid was altered to control the temperature in between the measurements on separate nanostructures, which kept the total temperature fluctuations across the entire scan to typically within a 2 K range. The roughing pump was not turned off during the measurements because the swift rise of the I-V curves to saturation, and the large current values near saturation were significantly greater than the vibrational noise caused by the pump. It is worth noting that the vibrational noise was significant near zero volts and in the reverse bias range, where the current was low, particularly at low temperatures. However, the data in the

low voltage range was not used to calculate either the Schottky barrier height or the ideality factor.

3.4.2.3. SET study

After confirming that nanostructures were formed, the samples were transferred to the microscope stage and scanned with an electrochemically etched tungsten STM tip. Initial scan sizes of 500 nm were utilized to find appropriate areas that harbored the possibility of finding nanostructures small enough to experience SET. Once these nanostructures were found, scanning tunneling spectroscopy was employed to record I-V curves from -2.5 – +2.5 V and inspect the I-V curves for the step-like structure known as the Coulomb staircase, which is evidence of SET in a DBTJ system, such as those studied here. Once nanostructures exhibiting SET were identified, several large area scans (2 – 4 um) were recorded to aid in identifying the nanostructures once the temperature was lowered.

To study the temperature dependence of SET in these nanostructures, liquid helium or liquid nitrogen was used to lower the temperature of the sample, which was continuously monitored using the Lakeshore temperature controller. A slow cool down was used to prevent excessively fast thermal drift, which would prevent the identified nanostructures from being easily followed. I-V curves were recorded from these nanostructures at regular intervals as the temperature was decreased; however, I-V curves were only recorded once the temperature was stable. Temperature stability was important because the turbopump drawing the cryogenic liquid through the heat exchanger was turned off during recording of I-V curves to prevent the recorded I-V curves from being excessively noisy. The necessity of turning off the turbopump was discovered after early low temperature STM measurements

were found to be noisy enough to obscure SET signatures. However, it was found that a temperature gradient of ~1 K/hr was stable enough to allow turbopump to be turned off for a period of ~20 minutes.

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Figures

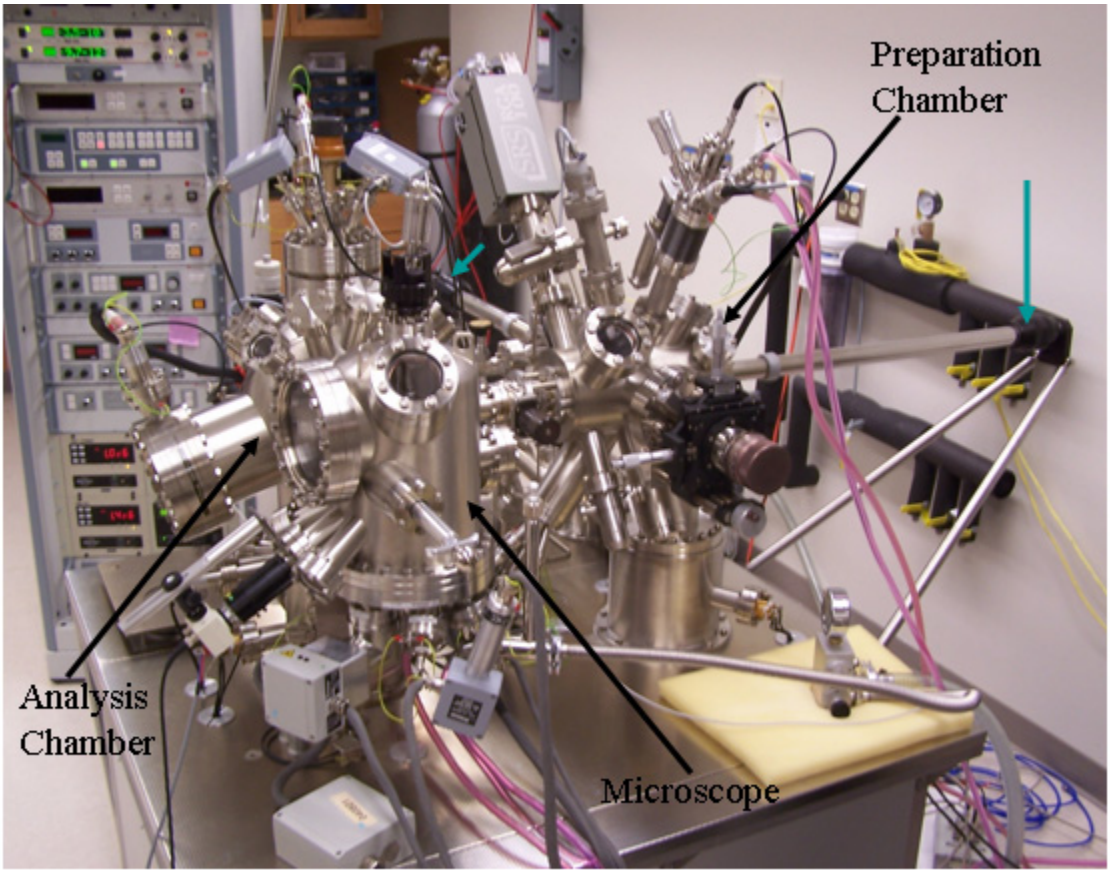

Figure 3.1: Multiprobe P Surface Science System. Labeled arrows identify the three main UHV chambers, the preparation and analysis chambers, as well as the chamber housing the microscope. The unlabeled arrows indicate the magnetic probes used to transfer samples and tip carriers between chambers.

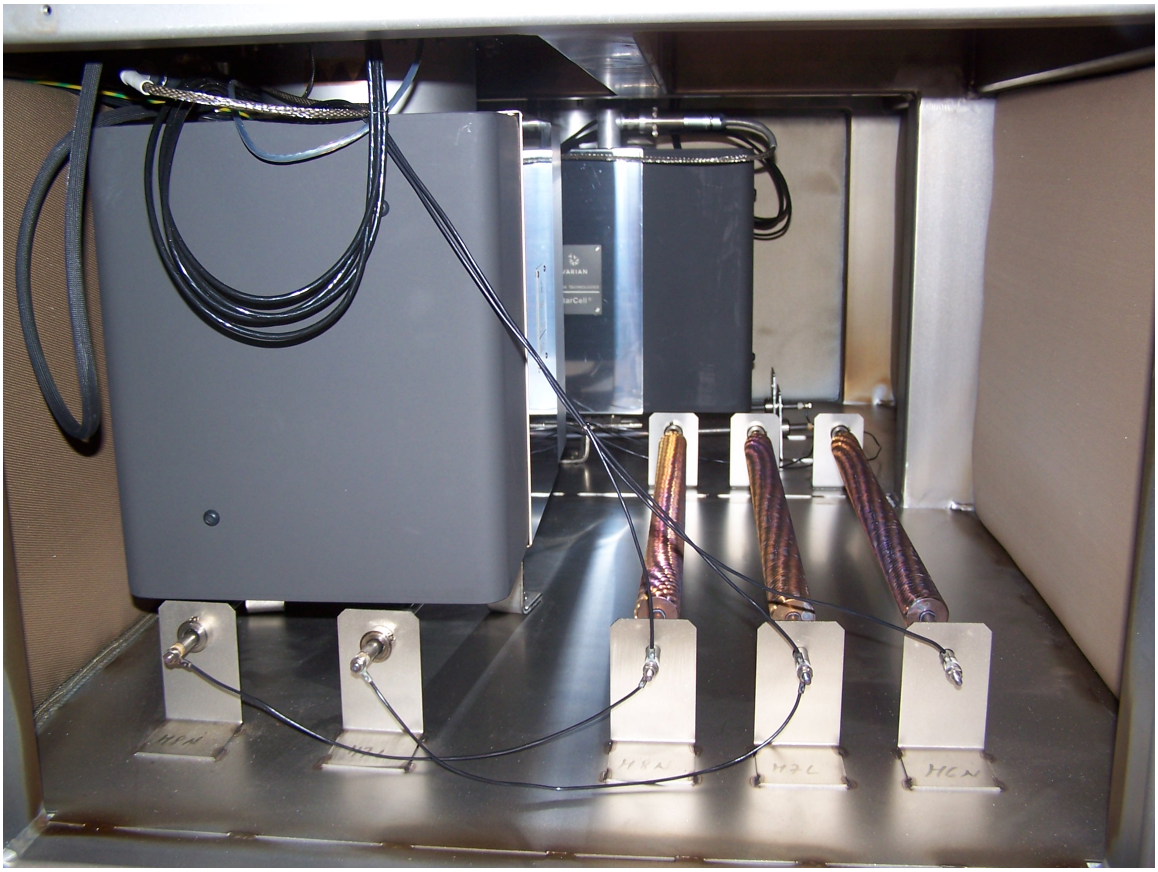

Figure 3.2: Space underneath the Multiprobe P containing the ion pumps. The ion pump in the foreground is for the analysis chamber while the far ion pump is for the preparation chamber. To the right of the analysis chamber ion pump and each ion pump are heating coils used during bakeouts.

Figure 3.3: Multiprobe P bakeout cover in place. Note that the transfer arm is covered with its own custom insulated cover, indicated by an arrow, because it extends outside of the confines of the bakeout cover. A similar insulated cover is placed on the other transfer arm (with the magnetic probes removed), allowing the transfer arms to be baked with the rest of the chamber.

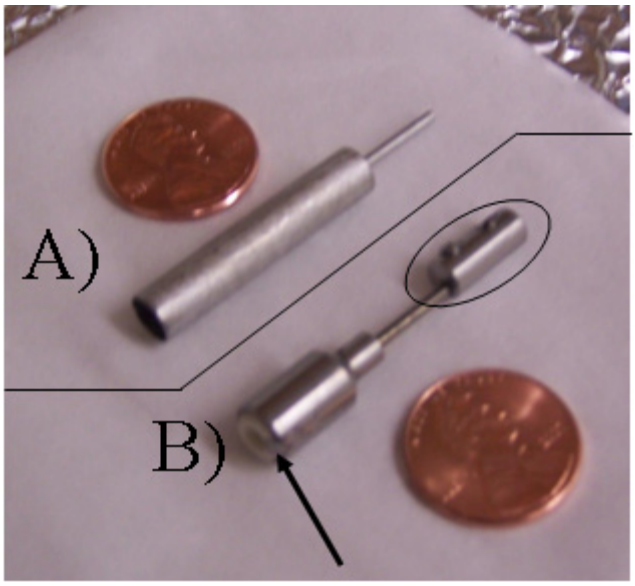

Figure 3.4: Crucibles used in the EFM 3T. (a) Custom-made molybdenum crucible used for the evaporation of cobalt. (b) Commercial crucible, manufactured by Focus, used for evaporating gold. Note that the arrow indicates a small piece of molybdenum that is designed to prevent the ceramic liner from charging while the gold source is bombarded with electrons during evaporation. The component that is circled is the barrel connector used for mounting the crucible inside the EFM 3T.

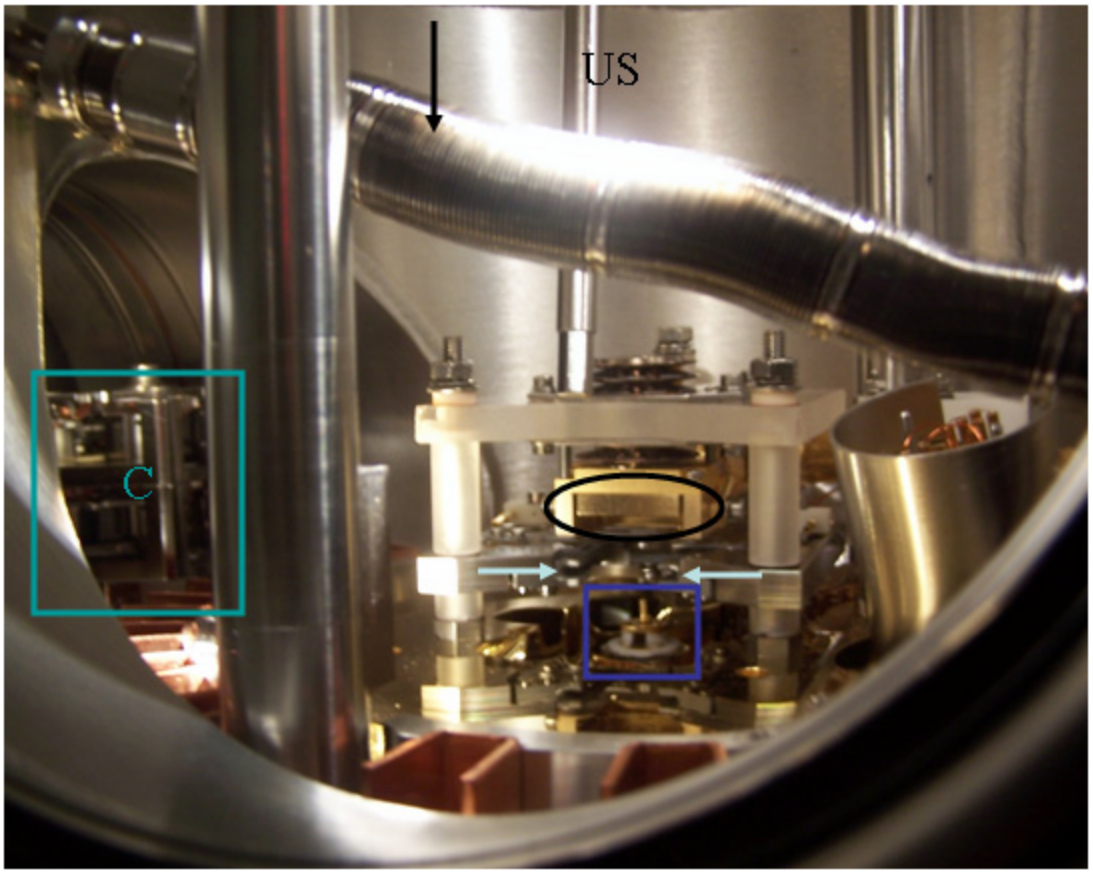

Figure 3.5: The microscopy half of the analysis chamber. Note that the wobblestick is indicated by an arrow near the top of the chamber while the clamping block is circled. The UHV screwdriver that is used to lower the clamping block into place is marked by the label "US". An STM tip, indicated by a box, is on top of the scanner tube directly beneath the clamping block. The place in the stage where a sample would be inserted is identified by double arrows. On the left side of the chamber, the storage carousel is outlined by a box and marked with a 'C'. The long column in the foreground contains one of the vibration isolation springs and the copper pieces beside the column are part of the eddy current damping system. The magnets between the copper plates are not visible.

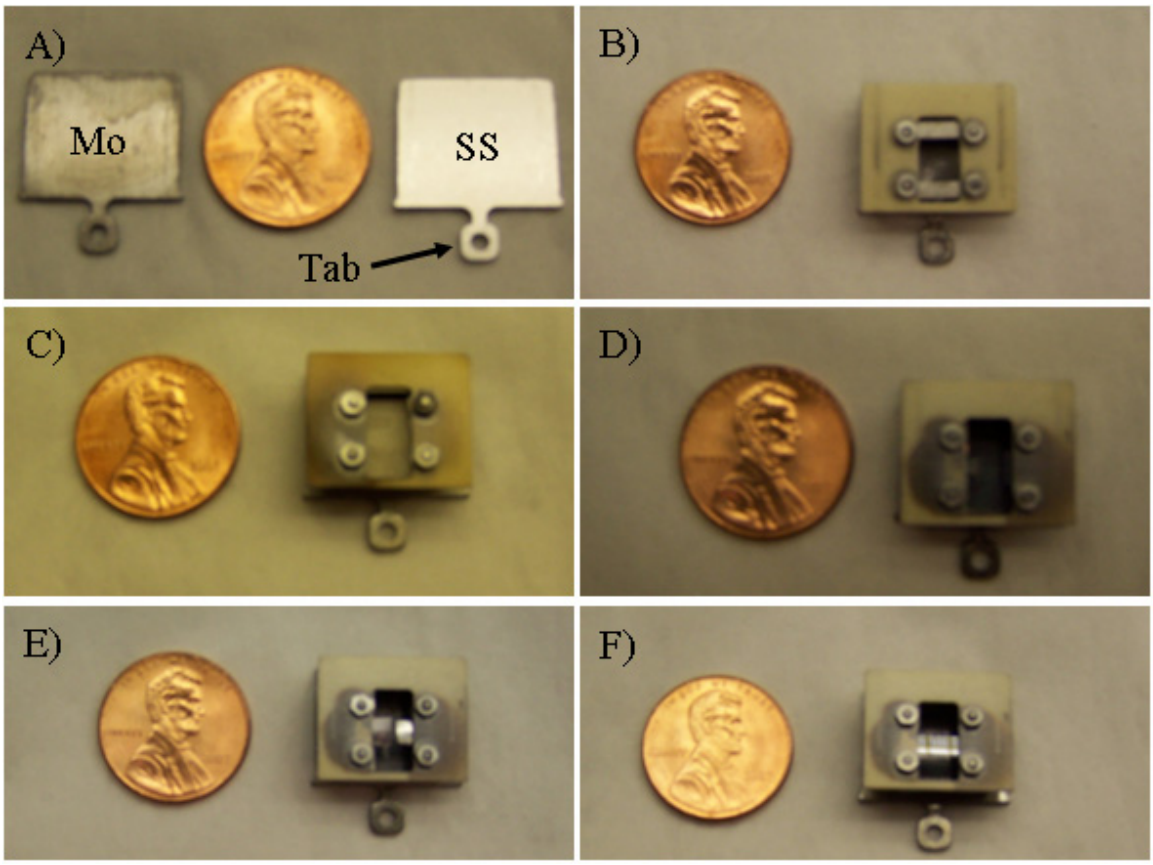

Figure 3.6: Sample cartidges for use with the Multiprobe P Surface Science System. The tab used for maneuvering samples with the wobblestick is indicated on the stainless steel sample plate and is the same for all sample cartridges. Note that some ceramic top plates are discolored due to extreme heat during annealing. a) Sample plate. There are two types of flat metal samples plates: molybdenum and stainless steel. b) Cooling sample cartridge. This type of sample cartridge has no electrical contacts in order to minimize thermal losses, but can only operate at either room temperature or ~25 K because samples cannot be counter-heated without electrical contacts. c) Resistive heating sample cartridge. This type of sample cartridge, despite its name, contains a PBN heater for radiatively heating samples. d) Direct current heating sample cartridge. e) Direct current heating sample cartridge with additional tantalum foil pieces for *c*-AFM studies. The tantalum pieces are typically separated by ~1 mm during use. f) Direct current heating sample cartridge with a silicon wafer piece mounted.

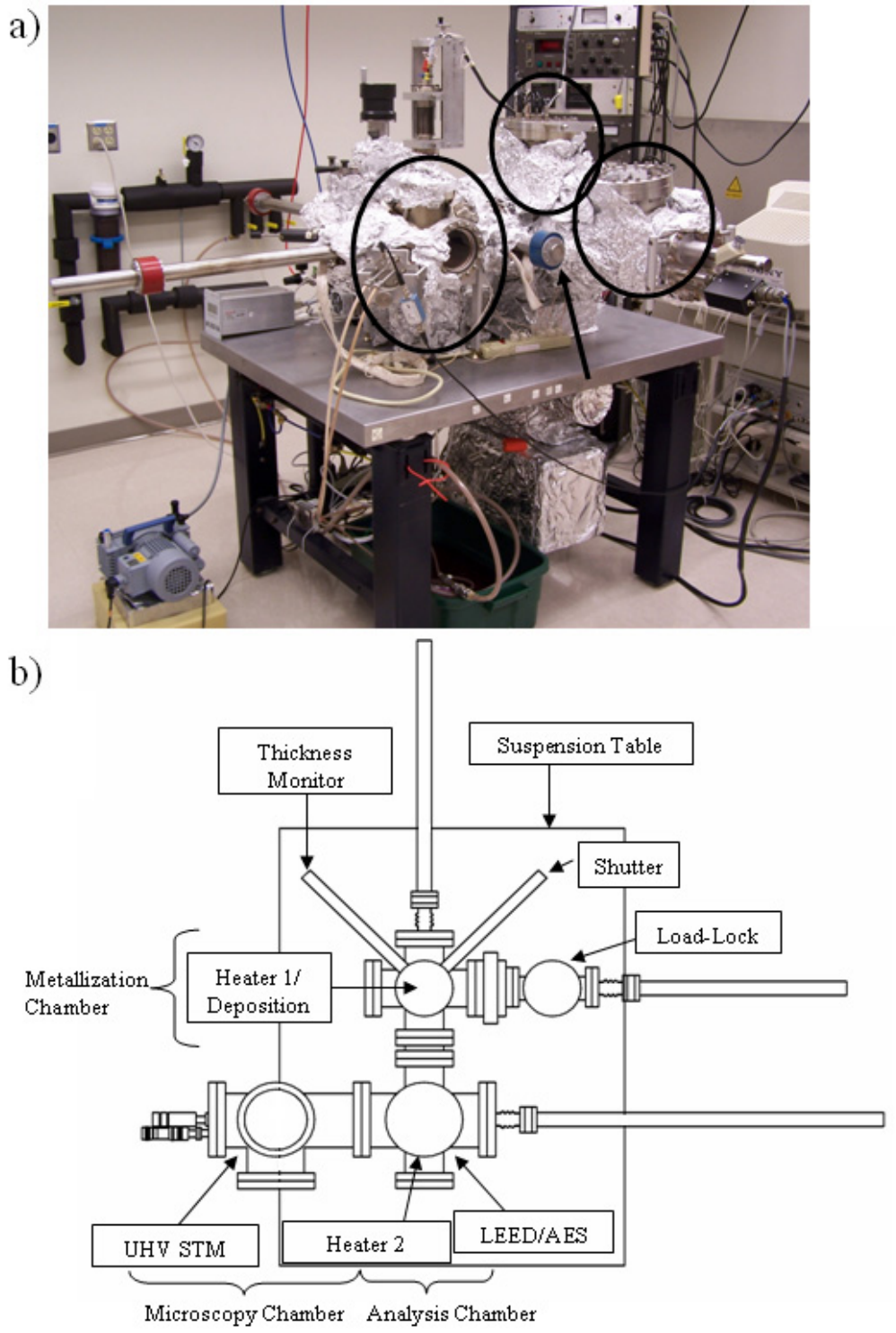

Figure 3.7: The Small System. (a) Image of the small system with the three chambers circled and the central storage rod indicated by an arrow. (b) Schematic of the small system. The three chambers are identified and the central storage rod is not included in the schematic.

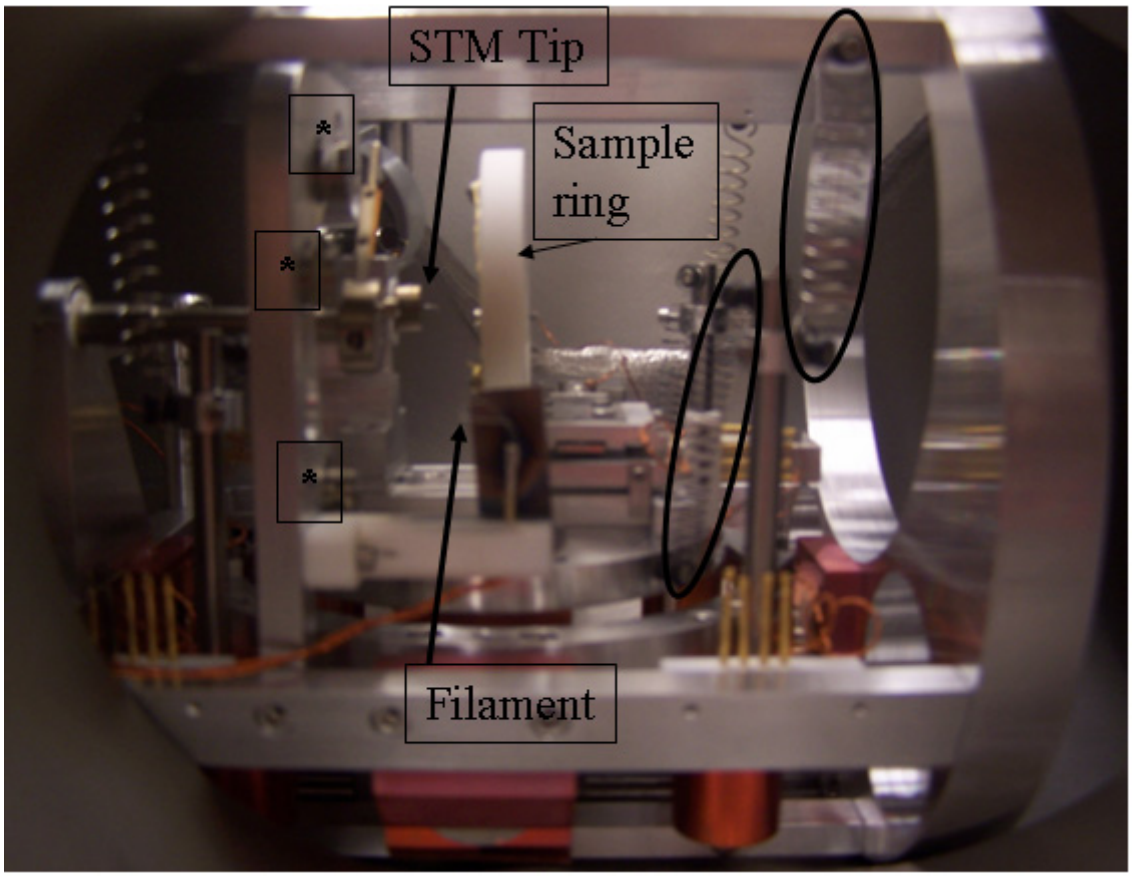

Figure 3.8: Autoprobe VP2 within the microscopy chamber of the Small System. The STM tip, the Macor sample ring, and the filament for tip annealing are labeled and indicated with arrows. A sample is not loaded in the sample ring in this image. Not shown is the metal pin on the sample ring that ensures electrical contact between the sample holder and the STM electronics. The carousel is indicated by the asterisks (*) marking the position of the spare STM tips (here, only three of the possible five extra tips are present in the carousel). One set of the double-spring suspension system springs is indicated with circles.

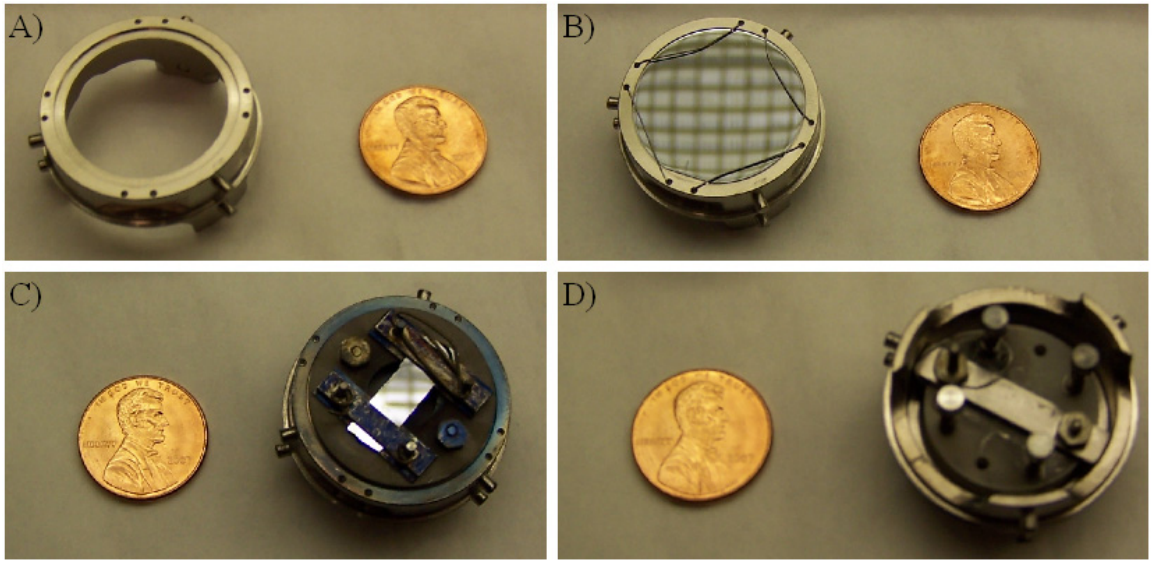

Figure 3.9: Sample holders for use in the Small System. (a) Standard 1” puck-shaped sample holder. (b) Standard 1” puck-shaped sample holder with 1” silicon wafer mounted. (c) Sample holder for direct current heating with piece of silicon mounted. Note that contact for heating is made to the left bottom stud (the stud closest to the penny), while the upper studs act as the floating ground. (d) Underside of sample holder for direct current heating. Note the loop of tungsten wire between the central screw and one of the studs. This wire is responsible for grounding the floating ground.

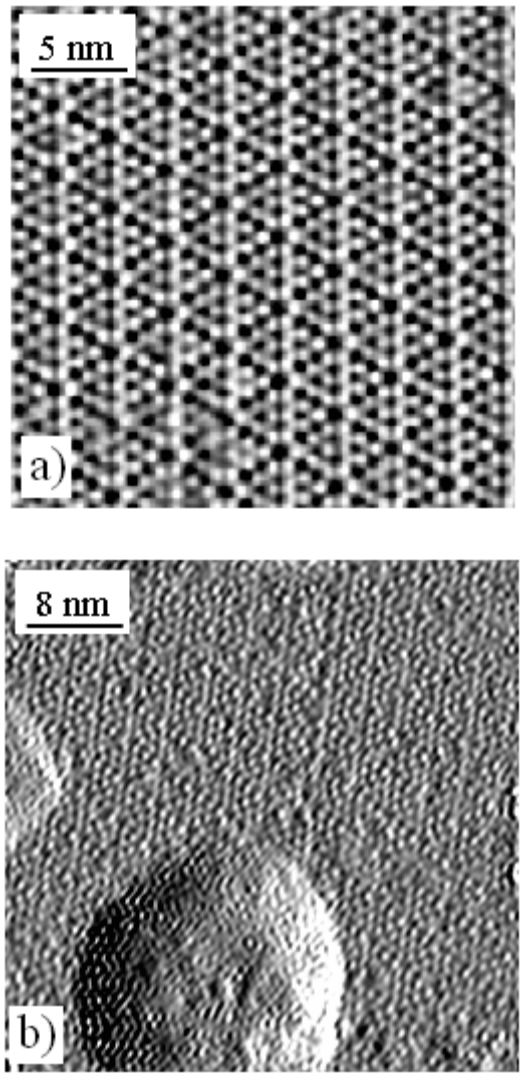

Figure 3.10: (a) STM image of Si(111):7×7 [19]. Scan size: 25 nm. (b) STM image of $TiSi_2$ islands grown on Si(111):7×7. Scan size: 40 nm. Tip bias: +1.2 V. Tunneling setpoint: 0.2 nA. The pixilation of the top surface of the nanoisland is due to image processing to remove noise and clarify the 7×7 unit cell.

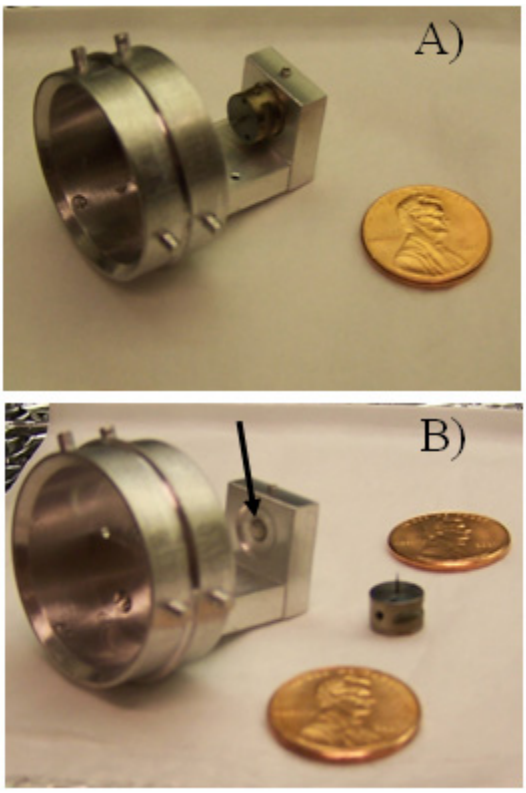

Figure 3.11: *In situ* tip transfer mechanism for the Autoprobe VP2. (a) Transfer mechanism with an STM tip mounted for transfer. (b) Transfer mechanism with the STM tip removed. The magnet used for holding tips during transfer is indicated.

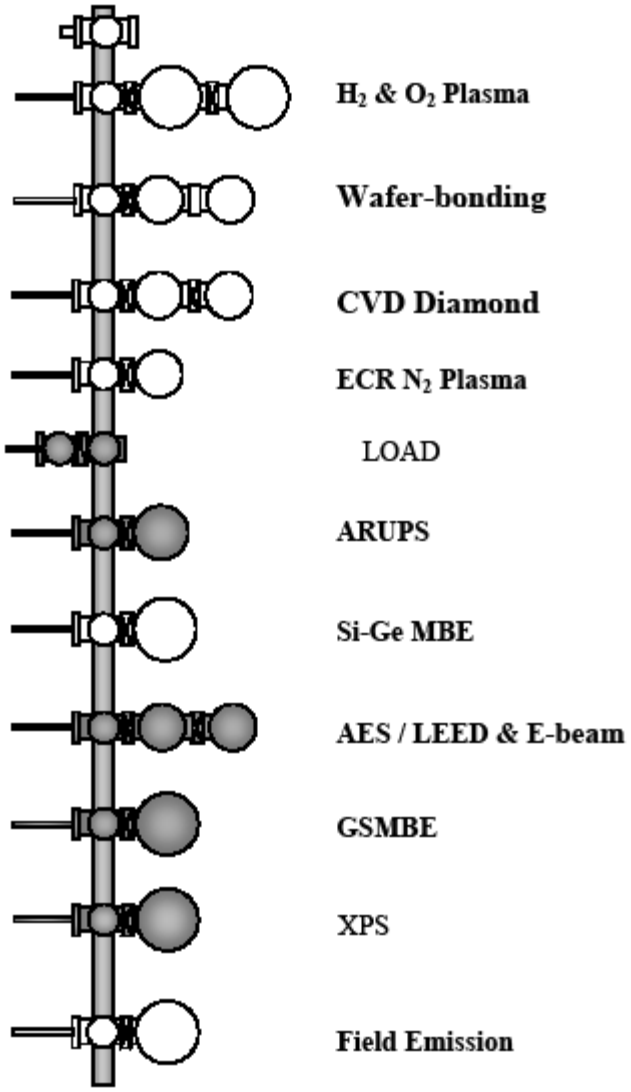

Figure 3.12: Configuration of the ISAGS in 2000 [24]. Note that double chambers are piggy-backed and transferring to the second chamber from the transfer line required transferring through the first chamber.

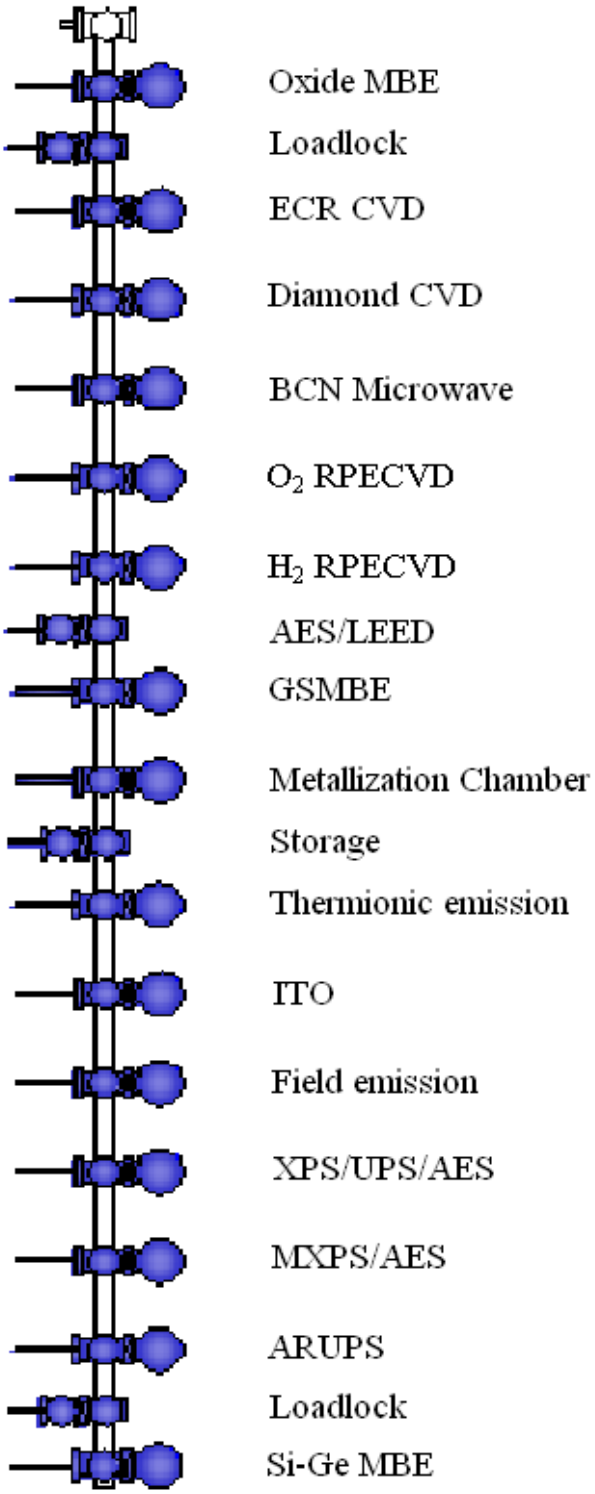

Figure 3.13: Current configuration of the ISAGS. Note that chambers with slashes (i.e. AES/LEED) are not piggy-backed, but have multiple functionalities. Also, the BCN Microwave chamber is currently not present, but is included in the plans for the ISAGS.

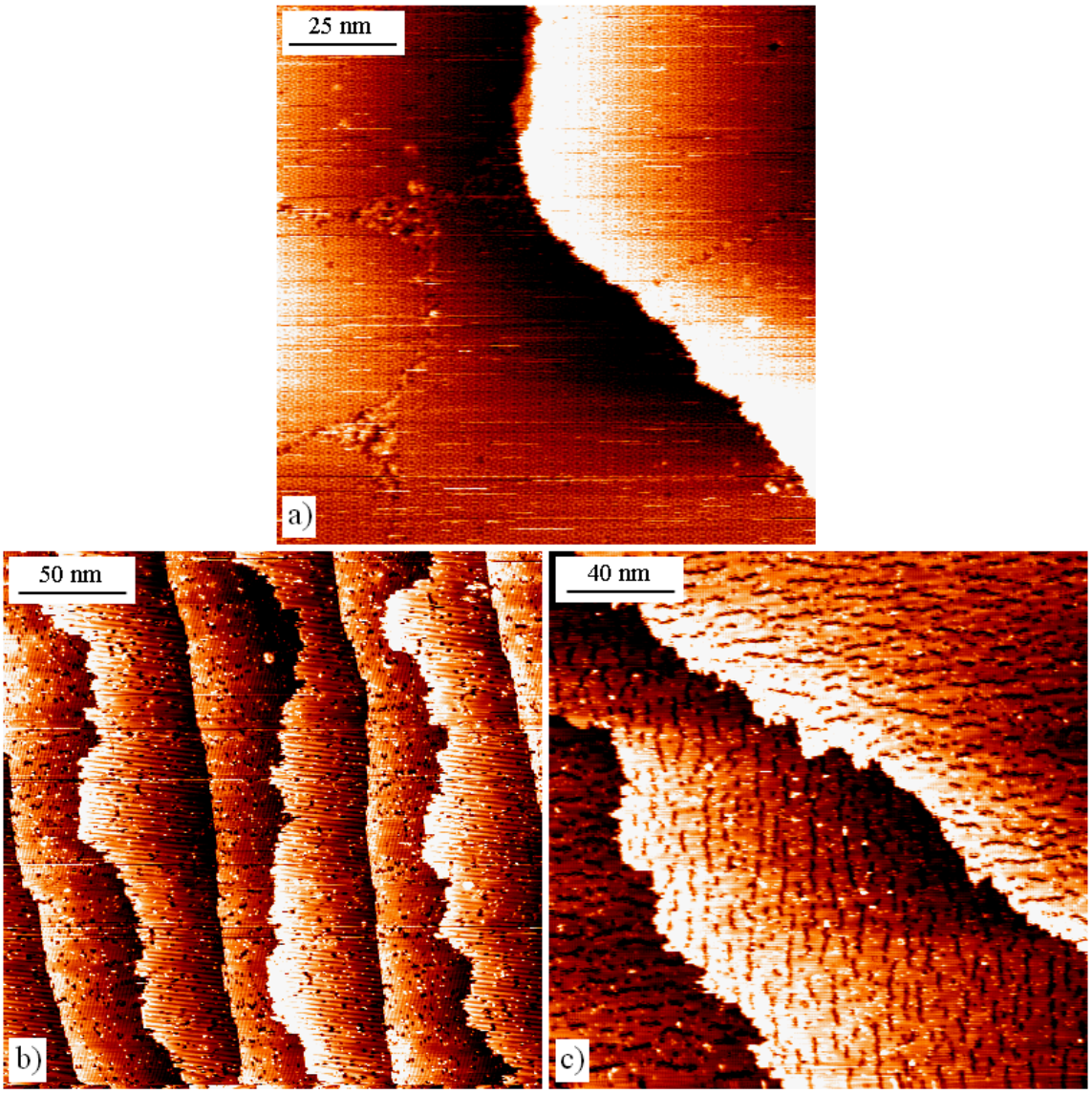

Figure 3.14: a) STM image of Si(111):7×7 surface handled with stainless steel tweezers. Scan size: 125 nm. Tip bias: +1.0 V. Tunneling setpoint: 1.0 nA. b) STM image of Si(100):2×1 surface handled with ceramic tweezers. Scan size: 250 nm. Tip bias: +1.0 V. Tunneling setpoint: 1.0 nA. c) STM image of Si(100): 2×1 surface handled with stainless steel tweezers. Scan size: 200 nm. Tip bias: +1.5 V. Tunneling setpoint: 1.0 nA. The ordered lines of vacancies on the Si(100) surface have been attributed to nickel contamination from the stainless steel tweezers.

Chapter 4:

Current-Voltage Measurements of Cobalt Disilicide Islands using Conducting Atomic Force Microscopy

4.1 Abstract

Cobalt disilicide islands have been formed by the deposition of thin films (~0.1-0.3 nm) of cobalt on clean Si(111) and Si(100) substrates in ultrahigh vacuum (UHV) followed by annealing to ~880 – 900ºC. Conducting atomic force microscopy (*c*-AFM) has been performed on these islands to characterize and measure their current-voltage characteristics. Current-voltage (I-V) curves were analyzed using standard thermionic emission theory to obtain the Schottky barrier heights between the silicide islands and the silicon substrates. Current-voltage measurements were also obtained at several temperatures, allowing the Schottky barrier heights of islands to be followed as the temperature is varied. Measured Schottky barrier heights are compared for islands of different shapes and with reported barrier heights. There appears to be no systematic difference between the barrier heights of islands with different shapes on the same substrate, which is attributed to these islands having similar epitaxial relationships to the substrate. The barrier heights measured from islands on clean surfaces in UHV conditions are found to be ~0.2 – 0.3 eV below corresponding barrier heights measured from islands on air-exposed surfaces. This shift is attributed to Fermi level pinning by non-passivated surface states of the clean surface in

UHV. Differences in the barrier heights are found between islands grown on clean Si(111) and Si(100) surfaces. Hole injection and generation-recombination are also identified as causes of non-ideality in the Schottky contacts through temperature-dependent current-voltage (I-V-T) measurements. The same I-V-T measurements also eliminate the possibility of enhanced thermionic field emission due to interfacial faceting as a source of non-ideal behavior.

4.2. Introduction

The Schottky barrier at the interface between a metal island and a semiconducting substrate will play an important role in the functionality of the next generation of electronic devices. The Schottky barrier will allow nanowires to act as effective interconnects in nanoelectronic devices by keeping the nanowires electrically isolated from the substrates [1] and has also been shown to be effective as a tunnel barrier in single electron tunneling devices [2]. Regardless of the specific means of implementation, a full understanding of the Schottky barrier is required for island-based devices.

One of the factors impeding a full understanding of the Schottky barrier in these islands is that the barrier height is known to be related to the quality and morphology of the interface [3-4], which can influence the barrier height in a number of ways, ranging from barrier height inhomogeneity [5-6] to Fermi level pinning due to defects [7-9] to differences in barrier height due to changes in interfacial orientation [10-11]. This last effect is perhaps most important when considering the differences in the morphology of the interfaces of islands of different shapes. In fact, the relationship between the barrier height and the island shape is one aspect that has not been well investigated.

$CoSi_2$ has a small lattice mismatch with silicon, -1.2% [12], meaning that it forms high quality epitaxial contacts with silicon [13-14]. Additionally, $CoSi_2$ is observed to form islands with several shapes that can be controlled through processing [15-18]. These are two requirements that are significant when studying the effect of island shape on barrier height. Therefore, $CoSi_2$ is an ideal candidate for a shape-dependent Schottky barrier height study. Furthermore, $CoSi_2$ has the added advantage that it is widely used in the semiconductor industry [19-21], offering the potential for a transition from the current device architecture to an island-based device architecture.

In this study, $CoSi_2$ islands have been grown on silicon substrates and studied using conducting atomic force microscopy (*c*-AFM). Using thermionic emission theory, the Schottky barrier height has been calculated from the recorded current-voltage (I-V) curves. The barrier heights of islands with different shapes are compared to determine systematic differences in the barrier heights as the island shape varies. The morphology of the interface has also been studied, and results are related to the differences in the barrier heights of the islands as their shapes change.

4.3. Experimental

Measurements were made in ambient conditions of $CoSi_2$ islands on air-exposed silicon surfaces as well as clean surfaces in UHV conditions. Samples were prepared using 25.4 mm diameter n-type silicon wafers with thicknesses of 0.25 – 0.28 mm and doping concentrations of $\sim 1 \times 10^{15} - 6 \times 10^{15}$ cm^{-3}. Both sets of samples were processed in UHV conditions, however, the details of processing and measurements were different. In both

cases, standard thermionic emission theory [22-23] was used to calculate the Schottky barrier height, Φ_B, and the ideality factor, n, from the measured I-V curves.

4.3.1. Air-exposed surfaces

The silicon wafers were cleaned *ex situ* by first rinsing them in flowing deionized water for 2 minutes to remove large particulates from the surface. Following this rinse, the wafers were subjected to an ultraviolet ozone (UV ozone) treatment for 5 minutes to remove hydrocarbons from their surfaces and densify the native oxide. This oxide layer, along with any residual contaminants embedded in it, was then removed with a 1 minute dip into room temperature 10:1 hydrofluoric acid (HF). The UV ozone and HF dip steps were repeated twice prior to the samples being mounted to molybdenum samples holders and secured with pieces of 0.125 mm tantalum wire. The sample holders were then loaded into the metallization chamber of the Integrated Surface Analysis and Growth System (ISAGS; see Chapter 3) for heat cleaning and deposition. The base pressure of this UHV chamber is 1.5×10^{-10} torr.

Once under UHV conditions, the wafers were heated radiatively and held at a sample temperature of ~675ºC for 1 hour. Then, the wafers were heated to ~950ºC and held at that temperature for 15 minutes. The sample was allowed to cool to room temperature for ~30 minutes before 0.3 nm cobalt was deposited at a rate of 0.02 nm/s. Following deposition, the sample was annealed at 880ºC for 25 minutes. A Thermionics 150-0030 e-beam evaporation system was used for the deposition.

Samples were then removed from UHV and a commercial ambient atomic force microscope (ThermoMicroscopes Autoprobe CP-Research AFM) was used to confirm

suitable island formation (i.e. islands of different shapes separated from each other by distances at least on the order of the island size). Following confirmation of island growth, the wafer backsides were swabbed with HF before being reintroduced into the UHV chamber where a layer of titanium ~100 – 200 nm thick was deposited at room temperature to form the backside ohmic contact.

Samples were then transferred to the same ambient AFM that was used to confirm island formation for topographical scanning and recording current-voltage (I-V) measurements. The cantilevers used with this AFM were standard n-type silicon cantilevers coated with a 100 nm thick layer of doped diamond-like carbon on the front side and a 50 nm thick layer of aluminum on the back side (Veeco DDESP cantilevers). I-V curves were recorded from 0 – 2.0 V in 0.02 V increments and only those curves where the current exceeded 10 μA at 2.0 V were processed. This was found to be the minimum level of conduction necessary to obtain consistency between measurements. Not all I-V curves recorded were useable for determining barrier heights because the current values were significantly less than 10 μA. Whether this was due to a highly resistive cantilever-island contact, irregularities within the island, or other reasons is unknown at this time. However, the contact resistance of the cantilevers used was measured on a sample of freshly-cleaved, highly oriented pyrolitic graphite (HOPG) using forces comparable to those used during the experiment, and was measured to be on the order of several kΩ. To account for the added voltage drop due to the contact resistance, R_c was assumed to be constant and was applied to the original I-V data using the equation [4]

$$V = V_0 - V_c = V_0 - IR_c. \tag{4.3.1}$$

When the modified I-V curves were plotted, it was found that the subtraction of the extra voltage due to the contact resistance did not significantly affect either the calculated Schottky barrier heights or the ideality factors. The negligible effect is reasonable given that at low forward bias (the region of the I-V curves utilized in the calculations), the currents passing between the cantilever and the islands are on the order of a few nA, which leads to an additional voltage, V_c, on the order of only a few μV.

After I-V curves were measured, the samples were removed from the AFM and submerged in 10:1 HF for 3 minutes to etch away the $CoSi_2$ islands from the Si(111) surface. It was assumed that the $CoSi_2$ would etch faster than the surrounding silicon and that significant etch pits in the silicon would correspond to the former locations of islands. The samples were then returned to the same ambient AFM for topographical scanning.

4.3.2. Clean surfaces

Measurements of islands on clean silicon surfaces while varying the temperature offer insights into current transport at metal-semiconductor interfaces that room temperature measurements alone cannot provide. In order to perform these measurements in this study, a variable temperature AFM was used. To prepare the samples for the variable temperature measurements, *ex situ* cleaning of the backsides of the silicon wafers using the same procedure described in Section 4.3.1. The reason for this difference was that the samples would be heat-cleaned in the UHV chamber prior to variable temperature AFM measurements; therefore no prior chemical cleaning of the frontsides of the wafers was necessary. A metal layer would be deposited on to the wafer backsides to act as an ohmic

contact, therefore it was necessary to perform the *ex situ* clean of the wafer backsides to ensure intimate contact between the metal film and the wafer.

In order to deposit the backside metal layer, the wafers were mounted in a similar manner as discussed for previous samples and loaded into the same UHV chamber that was used for the previous sample preparations. A 200 nm thick cobalt layer was deposited on to the backsides of the wafers and the wafers were then removed and sectioned into pieces ~2.5 × 10 mm^2 using a diamond-tipped scribe. The pieces were loaded into another UHV scanning probe system without additional *ex situ* chemical cleaning. The UHV system consisted of two interconnected chambers: a preparation chamber (base pressure: 7×10^{-11} torr) equipped with a triple-cell electron beam evaporator (EFM 3T), a custom single-cell electron beam evaporator (EFM 3), and an argon ion sputter gun (ISE 10), as well as an analysis chamber (base pressure: 1.5×10^{-11} torr) equipped with a commercially-available variable temperature scanning tunneling microscope/atomic force microscope (Omicron VT AFM), and facilities for Auger electron spectroscopy (AES) and low energy electron diffraction (LEED).

To avoid significant outgassing during heat cleaning, the sample holders were radiatively heated for ~ 4 hours at a temperature of ~200-300ºC. Following this, samples were resistively heated and held at ~600ºC for at least 12 hours (typically overnight). Once the initial heat cleaning had been performed, samples were flashed using quick 3 – 4 second pulses at increasingly higher temperatures until the sample temperatures reached ~1125ºC, which was maintained for 30 seconds 2 – 3 times before quickly cooling to 900ºC and then slowly cooling to room temperature. The final flashing step was repeated 2 – 3 times.

Scanning tunneling microscopy (STM) was performed to ensure that the surface was nominally free of defects other than atomic steps while LEED and AES were performed to

determine the long-range crystalline reconstruction of the surface, and to ensure that the surface was clean of contaminants, respectively. Once the surface was confirmed to be reasonably clean and ordered, ~0.1 – 0.2 nm of cobalt was deposited from a molybdenum crucible while the sample was held at room temperature, for Si(111) samples, or at 700ºC, for Si(100) samples. Following deposition, AES was performed to determine that cobalt was deposited and that the surface did not show a significant increase in contamination (most notably, in this case, carbon, oxygen, molybdenum, and tantalum). If cobalt was detected, LEED was used to gauge the surface coverage (absence of a diffraction pattern indicated full coverage) and the sample was then annealed at ~880 – 900ºC for 15 – 30 minutes. LEED was used again, and if a diffraction pattern was observed, it was assumed that the blanket cobalt film had formed into cobalt silicide islands, exposing the underlying silicon.

Samples were then transferred in UHV to the microscope stage for conducting atomic force microscopy (*c*-AFM) measurements. Current-voltage (I-V) curves were recorded at room temperature first to locate and select islands that demonstrated high conduction at low voltages (I > 333 nA at V = 0.5 V) and rectifying behavior at reverse biases (I ~ 10 nA at V > 1.0 V). Even though the preamplifier saturated at 333 nA, it was sensitive to ~10^{-12} nA, providing sufficient range to obtain a fit to the linear region of the I-V curve. Once such islands were identified, liquid helium was used to slowly lower the sample temperature while I-V curves were recorded on the identified islands at several temperatures between room temperature and ~75 K.

4.4. Results

4.4.1. $CoSi_2$/Si(111)

Two sets of $CoSi_2$/Si(111) samples were prepared. The samples prepared according the procedure of Section 4.3.1 were labeled air-exposed samples, while the samples prepared according to the procedure of Section 4.3.2 were labeled clean Si(111) (CS111). Despite the fact that two sets of samples were prepared in different UHV chambers using different preparation procedures, both $CoSi_2$ films formed epitaxial islands upon annealing to 880 – 900ºC that have similar appearances. Both sets of islands have been categorized into two types: triangular and non-triangular islands. As shown in Figures 4.1(a) and 4.1(b), both triangular and non-triangular islands formed together in nearby regions of the same surface. Additionally, it is notable that while most of the non-triangular islands were irregular partial triangles, there were some non-triangular islands with other distinct shapes, as shown in Figures 4.1(c) and 4.1(d). The primary difference between the two sets of islands is that the island density on the second set of samples was lower, as shown in Figure 4.2, when compared to the density of the islands shown in Figure 4.1. Regardless, the islands shown in both Figures 4.1 and 4.2 are similar to those reported elsewhere in the literature [13,15,17,24].

4.4.1.1 Electrical Characteristics of Air-Exposed Islands

Values of Φ_B calculated from those I-V curves measured from islands on air-exposed surfaces were found to range from 0.52 – 0.63 eV, with two outliers at ~0.45, with a linear correlation to the ideality factor, n, as has been reported by numerous other studies of Schottky contacts [4,25-30]. This relationship is shown in Figure 4.3. The data in Figure 4.3

is divided between triangular islands and non-triangular islands, as previously defined. There is neither an apparent systematic difference between the values of Φ_B for the different island shapes nor is there an apparent systematic difference between the relationship between Φ_B and n for the different shapes of islands, as shown in Figure 4.3.

The relationships between barrier height and island area is shown in Figure 4.4(a), while the relationship between ideality factor and island area is shown in Figure 4.4(b). Figure 4.4(a) shows that, excluding two outliers, there is a slight negative correlation between barrier height and island area, while Figure 4.4(b) shows that there is no apparent correlation between the ideality factor and the island area. As in Figure 4.3, the data points in Figures 4.4(a) and 4.4(b) are divided between triangular and non-triangular islands. Figure 4.4(a) shows no apparent systematic difference between the barrier heights of differently shaped islands of different sizes, while Figure 4.4(b) shows no apparent systematic difference between the ideality factors of differently shaped islands of different sizes.

4.4.1.2. Interfacial Structure of Air-Exposed Islands

The islands on air-exposed surfaces were successfully etched away using a 3 minute HF dip. When air-exposed samples were imaged following etching, etch pits were discovered that were mostly pyramidal in profile, as shown in Figure 4.5. However, the outlines of the etch pits were triangular and partially-triangular in shape, as shown in Figure 4.5. Based on these facts, it was assumed that the shapes of the etch pits corresponded to the shape of the interfaces of the islands that had been present there prior to etching. It must be noted that the regions shown in Figure 4.5 are not assumed to be same as the either the region shown in Figures 4.1(a) and 4.1(b) or the region shown in Figures 4.1(c) and 4.1(d). It is assumed that

the regions shown in Figure 4.5 were similar to those regions shown in Figure 4.1 prior to etching.

As shown in Figure 4.5, the etch pits have no consistent shape, either in outline or in profile. Some of the etch pits appear to be inverted triangular pyramids while other etch pits appear to be inverted truncated triangular pyramids. There are other etch pits that appear to be mostly flat. The etch pits with different profiles all exist in nearby areas, suggesting that the reasons for the different profiles is independent of islands' original surroundings.

4.4.1.3. Electrical Characteristics of CS111 Islands

The values of Φ_B calculated from the I-V curves measured on islands from CS111 ranged from 0.302 – 0.452 eV with values of the ideality factor ranging from 1.095 – 1.828. In addition to the anomalously low barrier heights, there is no apparent correlation between the barrier height and the ideality factor at room temperature, as indicted in Figure 4.6. This is unlike the result presented in Section 4.4.1.1, however, a similar result has been demonstrated in a previous study [8]. Furthermore, there is no apparent difference between the barrier height-ideality factor relationships of islands of different shapes at room temperature, also shown in Figure 4.6. Also, the room-temperature relationships between barrier height and island area and ideality factor and island area, as shown in Figures 4.7(a) and 4.7(b), do not indicate a systematic difference between different triangular and non-triangular islands.

Three plots that can be constructed from the collected I-V-T data are the barrier height and ideality factor as a function of temperature, shown in Figures 4.8(a) and 4.8(b) and Figures 4.9(a) and 4.9(b), respectively, and the activation energy plot, shown in Figures

4.10(a) and 4.10(b). As shown in Figures 4.8(a) and 4.8(b), the Schottky barrier heights tend to decrease with decreasing temperature, whereas the ideality factors tend to increase with decreasing temperature, as shown in Figures 4.9(a) and 4.9(b). The activation energy plots, as shown in Figures 4.10(a) and 4.10(b), tend toward linearity at high temperature, but diverge from linearity at low temperature. The degree to which the plots diverge from linearity does not appear to be related to either island shape or size. The reasons for the non-linearity at low temperature will be discussed later.

4.4.2. $CoSi_2$/Si(100)

The only $CoSi_2$/Si(100) samples prepared for this study were prepared using the procedure of Section 4.3.2. Therefore, using the naming convention established in Section 4.4.1, these samples are labeled clean Si(100) (CS100). As shown in Figure 4.11, the islands grown on CS100 are typically long rectangular islands, similar to those islands previously reported [16,18,31]. There were no comparisons between islands of different shapes, because the non-rectangular islands were found to be too small for reliable electrical contact with the cantilever and thus were not measured. Room temperature values of Schottky barrier height for these large islands range from 0.39 – 0.46 eV with corresponding values of the ideality factor ranging from 1.06 – 1.40, as shown in Figure 4.12. Furthermore, the negative correlation between barrier height and island area is barely evident in Figure 4.13(a), unlike in Figure 4.7(a). However, this effect could be related to the larger sizes of the islands grown on Si(100) than of the islands grown on Si(111). Regardless, as shown in Figure 4.13(b), the islands grown on Si(100), like the islands grown on Si(111) do not exhibit an identifiable correlation between ideality factor and island area.

In a similar manner as the CS111 islands, the Schottky barrier heights of the CS100 islands tend to decrease with decreasing temperature, as shown in Figure 4.14(a), and the ideality factors tend to increase with decreasing temperature, as shown in Figure 4.14(b). The activation energy plot, shown in Figure 4.15, tends toward linearity at high temperature, but diverges from linearity at low temperature in a similar manner to the air-exposed surface and CS111 islands.

4.5. Discussion

The three sets of samples, air-exposed islands, CS111, and CS100 each demonstrate different physical phenomena pertaining to current transport across the Schottky barrier. The phenomena unique to each sample will be discussed individually. However, there are common traits that affect the current transport through each sample. These common traits will be discussed below.

4.5.1. Common Phenomena

The most evident commonality between the three sets of samples is that the doping concentrations of the substrates are ~10^{15} cm^{-3}. This fact indicates that the current transport in each sample is in the thermionic emission regime. Therefore, effects due to thermionic field emission (TFE) or field emission should not be significant at any temperature range [32-34]. Additionally, because of the moderate doping density, image force lowering is a negligible effect because $\Delta\Phi_B < 0.005$ eV [35]. Previous studies performed using similar substrates have reached the same conclusions [30,36].

Additionally, all three sets of samples exhibit a correlation between barrier height and island area, as shown in Figures 4.4(a), 4.7(a), and 4.13(a). Furthermore, there appears to be

a correlation for all three sets of samples between barrier height and the ratio of island periphery-to-island area, as shown in Figure 4.17. A correlation between this ratio and the barrier height is indicative of increased hole injection and recombination for smaller islands. Increased hole injection and generation-recombination as a function of decreasing island size is one possible explanantion of the common trend of decreasing barrier height with decreasing island area.

It must be noted, however, that it is also possible that the trend is due to an increase in the effect of spreading resistance in the smaller islands. In circular contacts, the spreading resistance is inversely proportional to the radius of the contact [37-38]. While the islands in this study are not circular, the smaller islands will most likely experience a significantly increased spreading resistance relative to that of the larger islands. Additionally, the increased spreading resistance would be revealed by a suppression of the current in the high-voltage range of the I-V curves measured on smaller islands. Such suppression would artificially increase the saturation current, thus lowering the barrier height. If spreading resistance were causing this effect, it would lead to lower measured barrier heights, which would create an apparent trend toward lower barrier heights with decreasing island area.

Hole injection and generation-recombination are two factors typically cited as related to non-ideality in Schottky contacts [30]. The trends shown in Figures 4.4(a), 4.7(a), 4.13(a), and 4.17 indicate that there is a strong possibility that these phenomena are occurring and may be significant factors in the barrier height lowering. There is also evidence for recombination that is specific to CS111 and CS100 that will be discussed later.

The sizes of the islands in each of the samples are all of similar orders of magnitude, with average island areas of $\sim 10^5$ nm^2, as indicated in Figures 4.4, 4.7, and 4.13. This value is

important to know from the standpoint of Schottky barrier height inhomogeneity because according to the barrier height inhomogeneity model [5] the interface is composed on a distribution of regions with different barrier heights instead of one uniform barrier height. Furthermore, there exists a critical size at which a low barrier region will not affect the measured barrier height of the contact. However, if the total contact area is significantly greater than this critical size, then it is possible that a large area (i.e. greater than the critical size) low barrier region could exist. If this happens, then the potential distribution at the interface will approach that of a uniform interface with a low barrier height [39]. For doping densities of 10^{15} nm^2, the critical size for a low barrier region is ~5.0×10^4 nm^2. While the area of many of islands exceeds this value, some of the islands have areas below this value, yet they still exhibit significant barrier height lowering. Therefore, while effects due to Schottky barrier height inhomogeneity may be present, they appear to not be universal among all islands and are most likely not a significant cause of the barrier height lowering.

4.5.1.1. Sources of Schottky Barrier Height Inhomogeneity

Although it is suggested by the preceding analysis regarding island size that barrier height inhomogeneity is a minor effect, it is still worthwhile to explore the origins of any inhomogeneity that may be present. It has been suggested that a likely cause of the barrier height inhomogeneity is atomic inhomogeneity at the interface [40] such as from barriers that are composed of differing materials [41] or those with a mixed interface [42-43], as well as from an irregular interface [40,44]. Each of these cases will be considered individually.

Schottky contacts composed of different materials, also known as parallel contacts, are known to exhibit Schottky barrier lowering [25,41]. Sometimes, structures are purposely

designed with parallel contacts to allow for tailoring of the barrier height [41], which is not the case in this study. However, it is also possible that such contacts would form accidentally due to metallurgical reactions during growth [43]. In this study, however, the only materials present on the samples are cobalt and silicon. Thus, the islands are most likely only one species of silicide (cobalt silicide), thus eliminating inhomogeneity due to parallel contacts of different silicides. Furthermore, the details of the annealing ensure that the islands are entirely $CoSi_2$ [13,16,435An interface containing multiple grains with different interfacial orientations could lead to barrier height inhomogeneity. If an interface contains grains with different types of interfaces, and the interfaces have different barrier heights, then the overall barrier height will be lowered due to this inhomogeneity. $CoSi_2$ is known to form epitaxial films with a high degree of crystalline perfection at the interface [13-14]. Therefore, it is unlikely that multiple grains are the source of the inhomogeneity.

Additionally, it has been found that islands are likely to have faceted interfaces [18,31,46-48] and a faceted interface would most likely have points of locally high electric field relative to the rest of the interface due to the decreased radii of curvature of the facets [30,36,49-50]. It has been suggested that the locally higher electric field leads to a lowering of the local barrier height [51-52]. The differences between the electric fields would cause a redistribution of space charge in the silicon until a local equilibrium was reached [41] and if this happened, the barrier height would be lowered locally, which would result in the barrier height of the entire island appearing lower as the low barrier regions would dominate conduction [49,53]. Islands with smaller contact areas would be more likely to be affected by an interfacial region with a locally lower barrier height due to a higher electric field and enhanced conduction [25,41], leading to smaller islands being more likely to have a lower

barrier height. This correlation between decreasing island size and increased influence of low barrier regions would also help to explain the decreased barrier heights for smaller islands, as shown in Figures 4.4(a), 4.7(a), and 4.13(a).

4.5.2. Air-Exposed Islands

4.5.2.1. Island Shape and Interfacial Structure

As noted earlier, both triangular and non-triangular islands form in close proximity to each other. Furthermore, most of the non-triangular islands are hexagonal or partially triangular is shape. These shape are consistent with the three-fold symmetry of the Si(111) surface. Furthermore, they are consistent with islands that were in the process of transforming into fully triangular islands. A similar growth process occurs for epitaxial islands of $DySi_2$ on Si(111), in which irregular islands grow into stable faceted triangular islands [54]. Given the possibility of this process occurring, it is unclear if the highly irregular islands such as those in Figures 4.1(c) and 4.1(d) would eventually grow into faceted triangular islands with continued annealing or would decay away at the expense of the other, more regular, islands.

Non-triangular islands transforming into triangular islands could be considered more likely if the epitaxial relationdship between the substrate and the differently shaped islands was similar. Judging from Figure 4.5, there is no apparent systematic relationship between the shape of the island and the interfacial shape. This fact suggests that the epitaxial relationship between the silicon and differently shaped islands is the same. A similar epitaxial relationship would also explain the lack of differences between the electrical

characteristics of islands of different shapes, as discussed above, and shown in Figures 4.3 and 4.4.

4.5.2.2. Schottky Barrier Height Relationships

The barrier heights exhibit a linear negative correlation with ideality factor, as shown in Figure 4.3. The linear correlation between the barrier height and ideality factor can be related to the fact that the ideality factor reflects the quality of interface [4]. It should be noted that by fitting the data shown in Figure 4.3 to a straight line (while excluding the two outliers) [4] the intercept with n = 1.0 is found to be 0.687 eV, which is very close to the value of 0.69 reported in the literature for macroscopic $CoSi_2$/Si Schottky junctions [55]. Even by including the two outliers, the n = 1 intercept is 0.64 eV, which is still within the range of barrier heights reported in the literature for macroscopic $CoSi_2$/Si contacts [44,55-57].

A previous study [58] suggested that the non-ideality of the interface is related to a bias-dependent barrier height. The mechanisms responsible for a bias-dependent barrier height include image force lowering, interface states, hole injection, generation-recombination in the depletion region, and enhanced TFE [30].

Image force lowering has already been established to be negligible in these contacts, and hole injection and generation-recombination has been shown to most likely be occurring. Therefore, effects due to the interface states and enhanced TFE must now be considered. It is likely that interface states are not a significant factor because pre-deposition AES scans of the surfaces show no evidence of oxygen peaks.

TFE is ordinarily not a factor in Schottky contacts on moderately doped substrates, however, previous studies have suggested that field enhancement due to island faceting leads

to TFE, particularly at the island edges. [30,36,59]. It is difficult to eliminate enchanced TFE as a conduction mechanism in the air-exposed samples because to do so requires data recorded at several different temperatures.

The ideality factor increases as the island area decreases, as shown in Figure 4.4(b). This is reasonable given the linear relationship between barrier height and ideality factor. Because the ideality increases as the barrier height decreases, and the barrier height decreases with island area, it follows that the ideality factor would increase with decreasing island area.

4.5.3. Clean Surface Samples

4.5.3.1. Room Temperature Barrier Height Relationships for CS111

The range of measured barrier heights for CS111, 0.302 – 0.452 eV, is significantly lower than that typically reported [44,55-57]. However, barrier heights of 0.45 eV have been reported for $CoSi_2$ films on n-type Si(111) surfaces [55]. These anomalous barrier heights were attributed to non-uniform interfaces and Schottky barrier height inhomogeneities [55]. The issue of barrier height inhomogeneities has already been addressed and they were considered to be a minor effect. This suggests that a non-uniform interface may be the reason for the anomalously low barrier heights. If that is the case, it may also explain the lack of correlation between the barrier height and the ideality factor. Because the ideality factor is related to the interfacial quality [4], then if all islands possessed a non-uniform interface, a comparably lower ideality factor might not indicate that one interface was lower quality than another.

Alternately, the possibility of a bias dependent barrier height still exists. The mechanisms for introducing a bias dependent barrier height discussed in the previous section

still apply to CS111. However, it is possible to examine enhanced TFE in more detail now that I-V-T curves have collected for these islands. Additionally, it is possible that surface states play a significant role in barrier height lowering, which will be discussed later.

4.5.3.2. Room Temperature Barrier Height Relationships for CS100

The room temperature barrier heights measured from CS100, 0.39 – 0.46 eV, lie consistently 0.2 – 0.3 eV below the bulk range. One mechanism that has been suggested to cause such barrier height lowering is the presence of a thin oxide layer. It has been suggested that 2 – 3 monolayers of silicon oxide on Si(100) can lead to a decrease in the barrier height of more than 0.1 eV [60]. However, pre-deposition AES scans do not show the presence of oxygen peaks, suggesting that the amount of oxygen on the surface is significantly less than the 2 – 3 monolayers necessary for barrier lowering to occur.

Alternately, it is possible that a non-uniform interface with Si(100) would lead to similarly low Schottky barrier heights, in an analogous manner to the case of non-uniform interfaces between $CoSi_2$ and Si(111) [55]. However, it is interesting to note that the barrier heights and ideality factors of $CoSi_2$ islands on CS100 are, on average, more uniform than the corresponding values for islands on air-exposed samples and CS111. This suggests that the interfaces on CS100 were more uniform than the CS111 interfaces.

4.5.3.3. Fermi Level Pinning

While the barrier heights measured from islands on air-exposed surfaces match similar previously published studies of nanoscale islands [30], it is evident that the barrier heights measured from islands on clean surfaces behave differently. Specifically, the rangeof barrier heights reported is 0.2 – 0.3 eV below the bulk values and is centered around ~0.4 eV,

as shown in Figures 4.6 and Figures 4.12, as compared to Figure 4.3. This shift can be attributed to surface states of the clean surface that pin the Fermi level of the silicon surface. Due to this Fermi level pinning, the barrier is unable to reach the typical values reported in the literature [44,55-57].

Previous photoemission studies have found differences that the Fermi level is pinned at ~0.4 – 0.46 eV, depending on the step density of the surface [61], or at ~0.55 eV [62]. In either case, these values for the pinned Fermi level correspond well with the values of the barrier height measured on islands on CS111 and CS100. The fact that the correspondence is so close suggests that the surface states on the clean surfaces are not passivated and are pinning the Fermi level. This is the most likely reason for the 0.2 – 0.3 eV shift in the barrier heights for CS111 and CS100 as opposed to barrier heights measured on the air-exposed surfaces.

4.5.3.4. Temperature Dependent Analysis

The activation energy plots shown in Figure 4.9 exhibit non-linearity at low temperatures. Non-linearity in the activation energy plot is typically an indication of recombination in the depletion region [22]. This supports the suggestion in Section 4.5.1 that decreases in the barrier height with decreasing island area-to-periphery ratios indicate recombination. The fact that the non-linearity is more pronounced at low temperatures is also reasonable, given that recombination is generally more pronounced when the sample temperature is lowered [22]. The same analysis can be applied to CS100 using Figure 4.15.

The manner of current transport through the islands on CS111 can be determined by plotting nkT vs. kT, as shown in Figure 4.16(a), and fitting a curve through the data points. If

TFE is occurring, the fit of the nkT vs. kT plot will become non-linear and approach a constant value at low temperature [50,59]. As shown in Figure 4.16(a), the fit is essentially linear through 75 K, suggesting that TFE is not occurring in this study. This statement would also appear to eliminate the possibility that enhanced electric fields at the edges of the islands are high enough to cause TFE.

The nkT vs. kT plot, however, does suggest that there may be another mechanism at work known as the T_0 anomaly, which is the phenomenon where the recorded data can be made to match the predictions of thermionic emission theory by using the equation

$$n = 1 + \frac{T_0}{T}. \tag{4.5.1}$$

The physical origin of the T_0 anomaly has been related to doping at the interface [44], surface states at the interface [5,63], the temperature dependence of the silicide work function [59], TFE [39-40], Schottky barrier inhomogeneity [5,39], as well as deformation of the Schottky barrier under applied bias [49]. T_0 is not a constant for the curve shown in Figure 4.16(a), as would be expected from previous studies [63-64], however, the temperature dependence of T_0 presented here is attributed to fringing fields from the islands edges causing thermionic emission to occur [59]. The same analysis and conclusions can be applied to CS100 using Figure 4.16(b).

4.5.3.5. Interfacial coordination

There are four known interfacial types for the $CoSi_2$/Si(111) system (known as type-A, type-B, type-C, and type-D) [14,43,65]. $CoSi_2$ islands formed on Si(111) in the manner used in this study are known to form type-B interfaces only [13]. The preceding study that discovered this fact is unclear about the coordination of the $CoSi_2$/Si(111) interface because,

although it is a fully epitaxial, type-B interface, it is not specified whether the interface is 7-fold or 8-fold coordinated. This is an important question because the 8-fold coordinated interface is reported to have a barrier height of 0.67 eV, while the 7-fold coordinated interface is reported to have a barrier height of 0.4 eV [56]. Judging from the data presented in Figure 4.6, it is possible that the CS111 interface is characteristic of the 7-fold coordinated interface. Given this fact, it is interesting that the data presented in Figure 4.3 suggests that the interfaces of islands on air-exposed surfaces were characteristic of 8-fold coordinated interfaces.

The $CoSi_2$/Si(100) interface is reported to have only a 6-fold coordination [66]. While this eliminates barrier height inhomogeneity due to a mixed interface from causing barrier lowering in CS100, it leads to additional problems. The foremost problem is that the barrier heights for this interface are reported to range from 0.68 – 0.80 eV [55], and there are no other reported interface coordinations to account for the anomalously low barrier heights measured in this study. However, as stated in Section 4.5.3.3, the non-passivated surface states of the clean silicon surface can cause a negative shift in the barrier height of 0.2 – 0.3 eV. By accounting for this negative shift, the barrier heights presented in Figure 4.12 are consistent with the model of the 6-fold coordinated interface.

4.6. Conclusion

$CoSi_2$ islands were grown on Si(100) and Si(111) substrates and I-V measurements were performed using *c*-AFM, both at and below room temperature. In air-exposed samples, the range of barrier heights measured approached the range of barrier heights typically reported in the literature. Furthermore, a negative linear correlation was found between

decreasing Schottky barrier height and increasing ideality factor, as well as a slight correlation between barrier height and island area. In measurements performed on clean surfaces, no such correlation was found between barrier height and ideality factor at room temperature, however the same correlation between barrier height and island area was found. Furthermore, the range of barrier heights measured was ~0.2 – 0.3 eV below the range reported in the literature for these contacts. The measured Schottky barrier heights of CS111 suggested that the CS111 interface was characteristic of either a non-uniform or a 7-fold coordinated interface. Fermi level pinning by the non-passivated surface states of the clean surface can account for the anomalously low barrier heights of both the CS111 and the CS100 samples. Using I-V-T measurements, the temperature dependent electrical characteristics of the islands were investigated and it was found that the barrier heights decreased with decreasing temperature while the ideality factors increased with decreasing temperature. The I-V-T measurements allowed a fuller assessment of the reasons for these correlations than would be possible at room temperature. It was found that hole injection and recombination in the depletion region were the most likely sources of non-ideal behavior. Barrier height inhomogeneity was also considered, but it was concluded to be a minor effect due to the small size of the islands. Additionally, enchanced TFE due to island facets was eliminated as a possibility due to the I-V-T measurements, which showed that TFE was not occurring in either CS111 or CS100 throughout the temperature range investigated.

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Figures

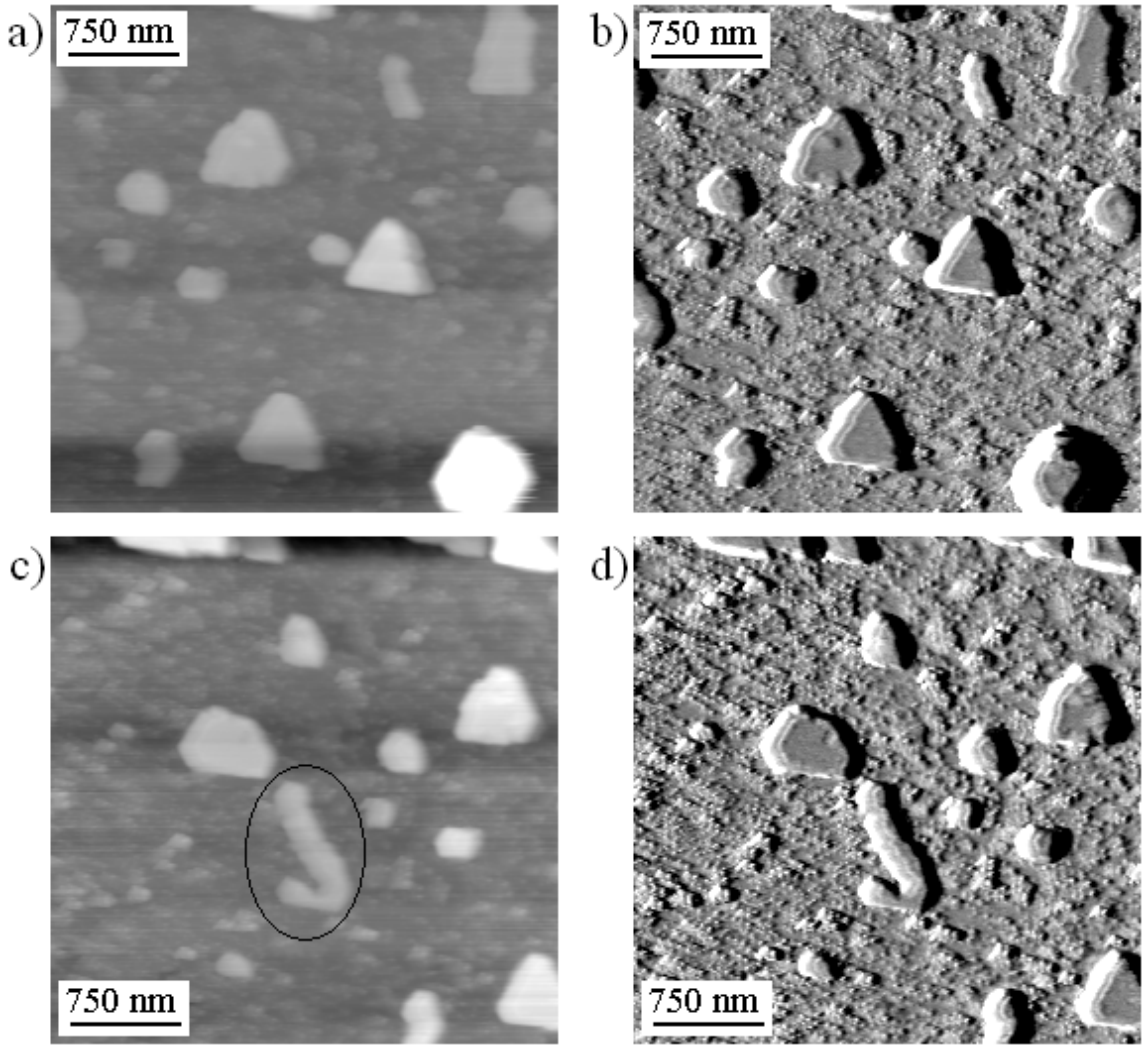

Figure 4.1: AFM image of $CoSi_2$/Si(111) islands from air-exposed samples. (a) AFM topographical scan. Scan size: 3.0 μm. Note that triangular and non-triangular islands grow in the vicinity of each other, however, the majority of non-triangular islands appear to have irregular hexagonal shapes. (b) Error signal of the scan shown in (a). (c) AFM topographical scan. Scan size: 3.0 μm. Note that there are non-triangular islands that are not hexagonal in shape, such as the circled island. (d) Error signal of the scan shown in (c).

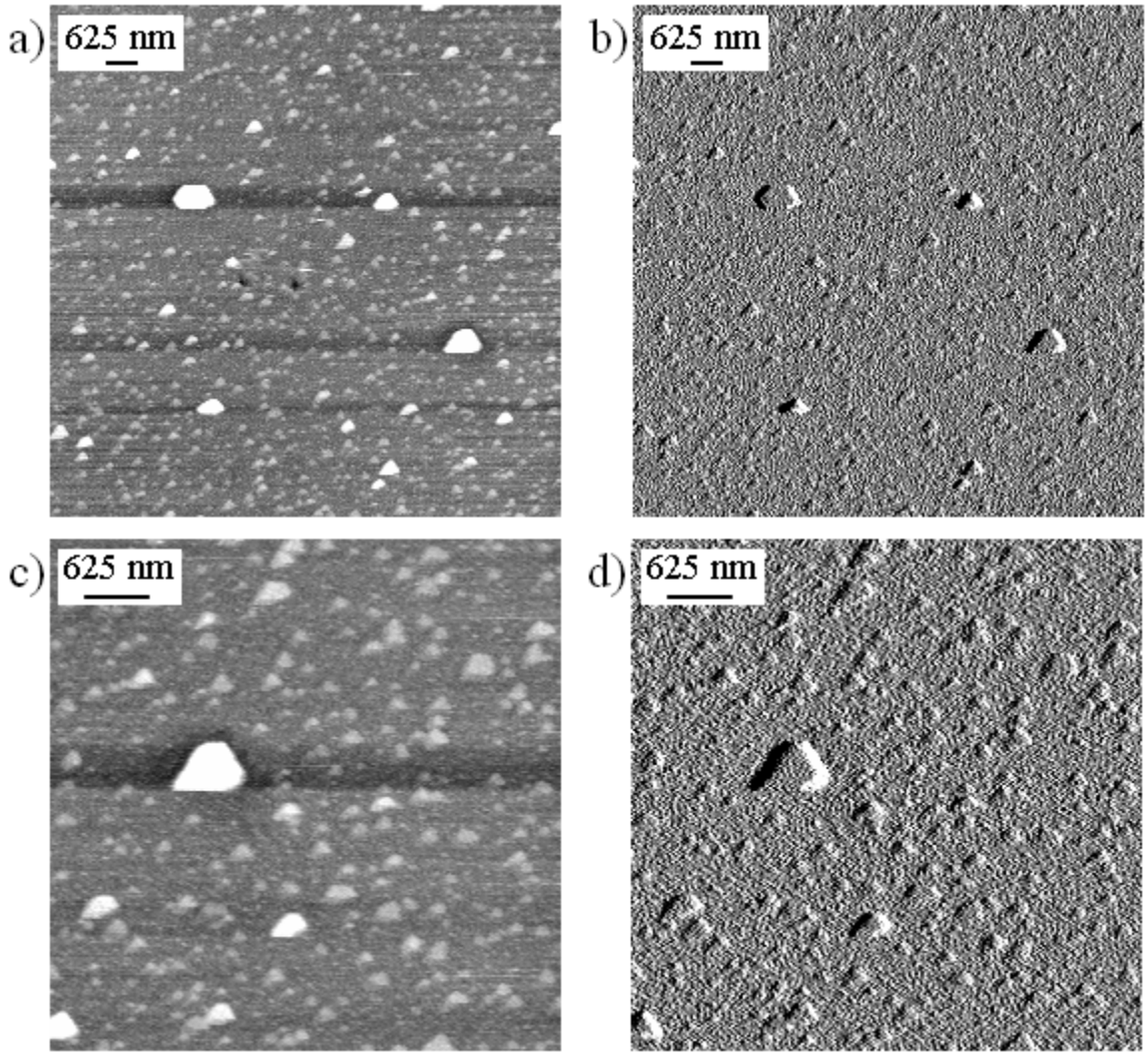

Figure 4.2: $CoSi_2$/Si(111) islands from CS111. (a) AFM topographical scan. Scan size: 10.0 μm. (b) Error signal of the scan in (a). (c) AFM topographical scan of a close-in image of the lower right region of the scan in (a). Scan size: 3.0 μm. (d) Error signal of the scan in (c).

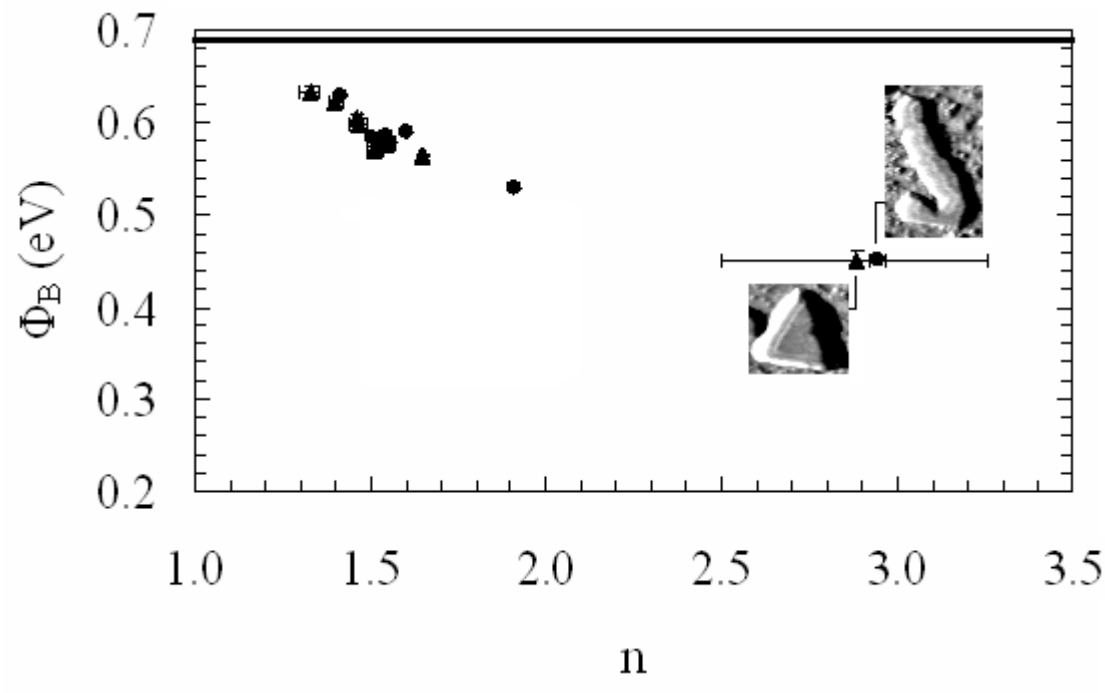

Figure 4.3: The relationship between Schottky barrier height, Φ_B, and ideality factor, n, for $CoSi_2$ islands on air-exposed samples. The data points are divided between those islands that are triangular in shape (▲) and those that are non-triangular in shape (●). A thick line (—) marks the value of Φ_B reported in the literature for bulk $CoSi_2$/n-Si(111) [53]. The two islands that are outliers are indicated with AFM error signal scans to indicate their appearances.

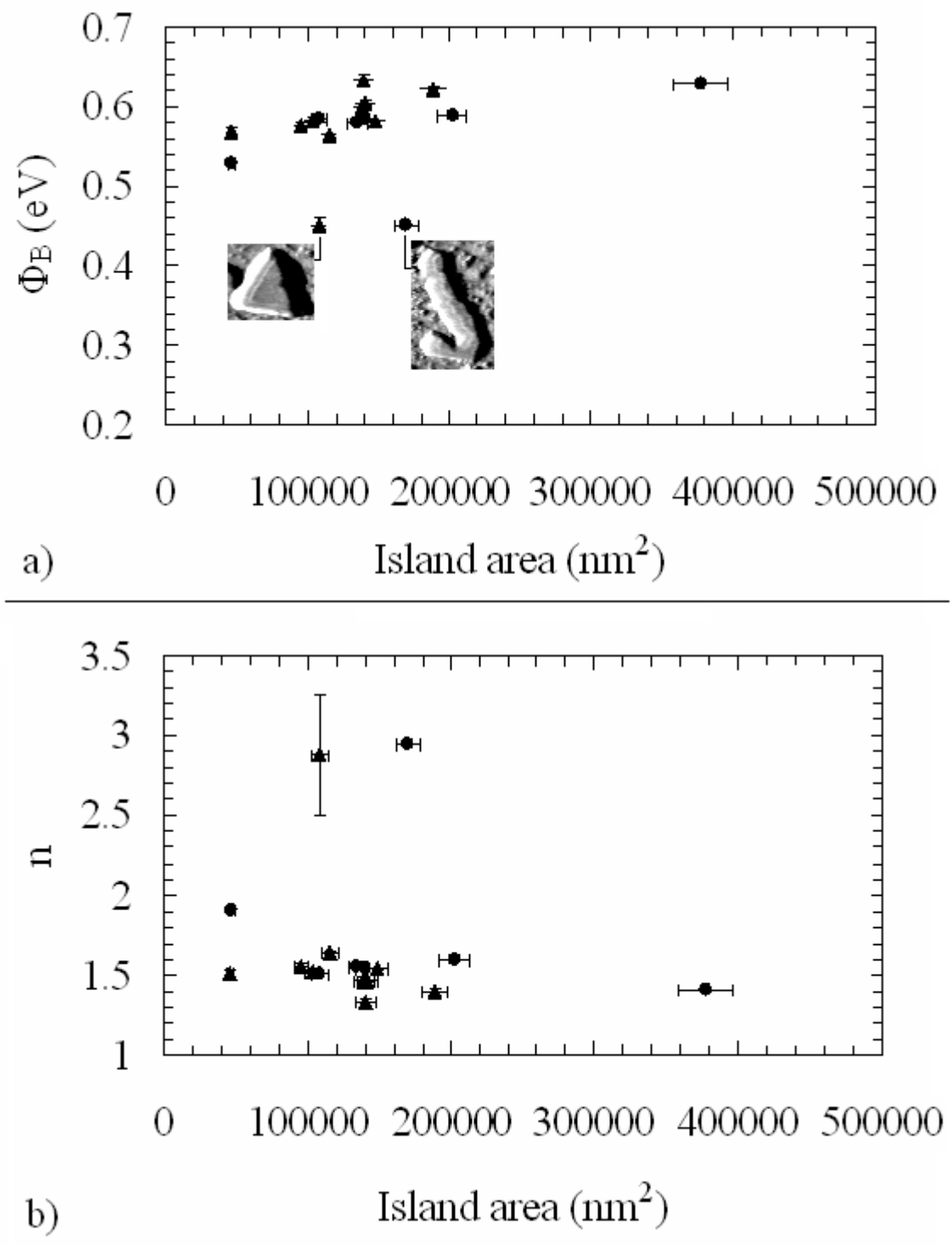

Figure 4.4: Areal relationships for $CoSi_2$ islands on air-exposed samples. (a) Φ_B as related to island area. (b) n as related to island area. The data points for both (a) and (b) are divided between those islands that are triangular in shape (▲) and those that are non-triangular in shape (●). The two outliers in both (a) and (b) are the islands that are shown in (a).

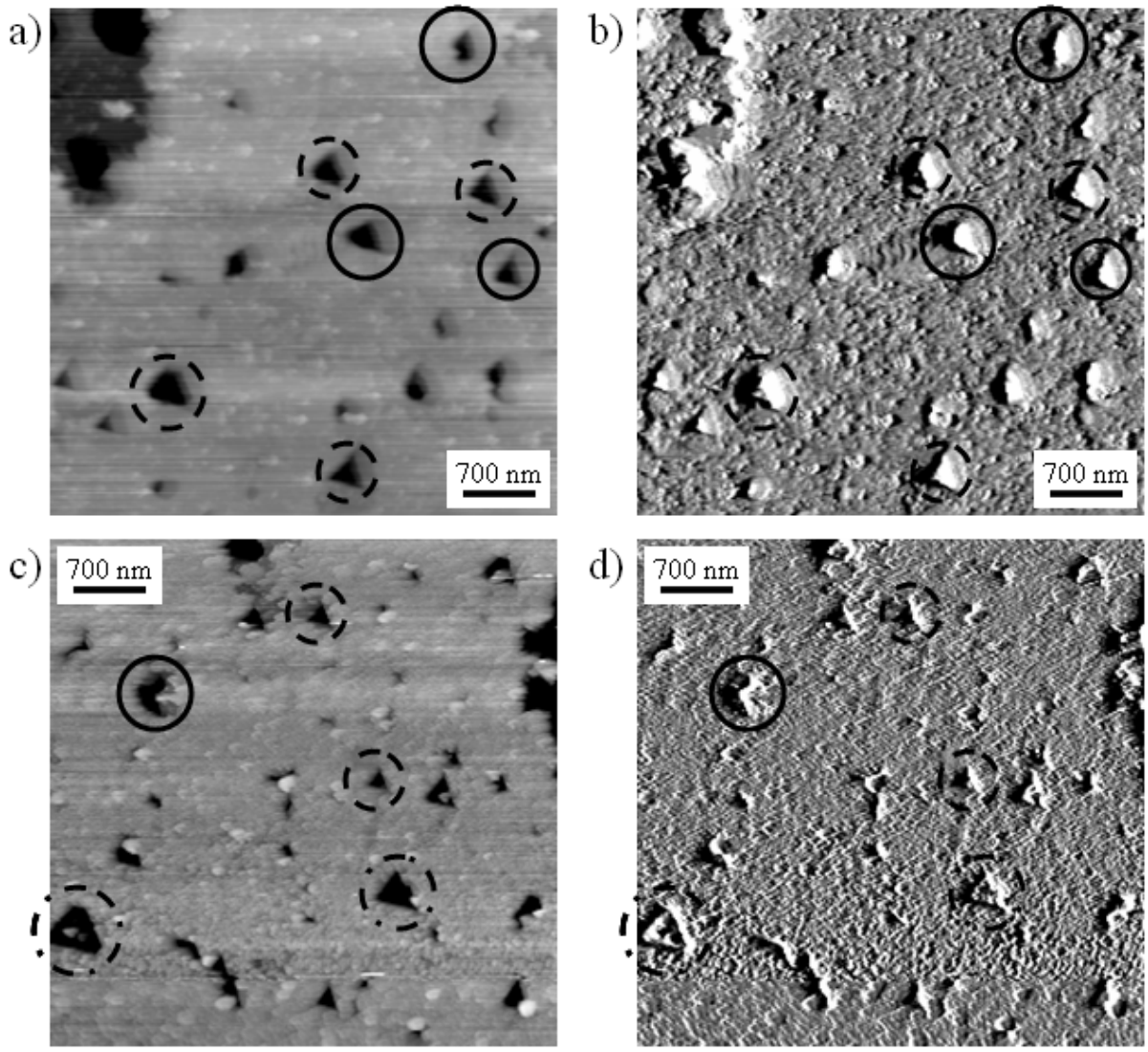

Figure 4.5: AFM scans of etch pits on air-exposed samples following etching. All scan sizes are 5.0 μm. Etch pits surrounded by full circles are fully inverted pyramidal. Etch pits surrounded by dashed circles are truncated inverted pyramidal. Etch pits surrounded by dashed and dotted circles are mostly flat. (a) and (c) are AFM topographical scans while (b) and (d) are the error signals of the scans shown in (a) and (c), respectively. It must be noted that darker colors in the topographical scans (and brighter colors in the error signals) indicate the surface is recessed into the substrate.

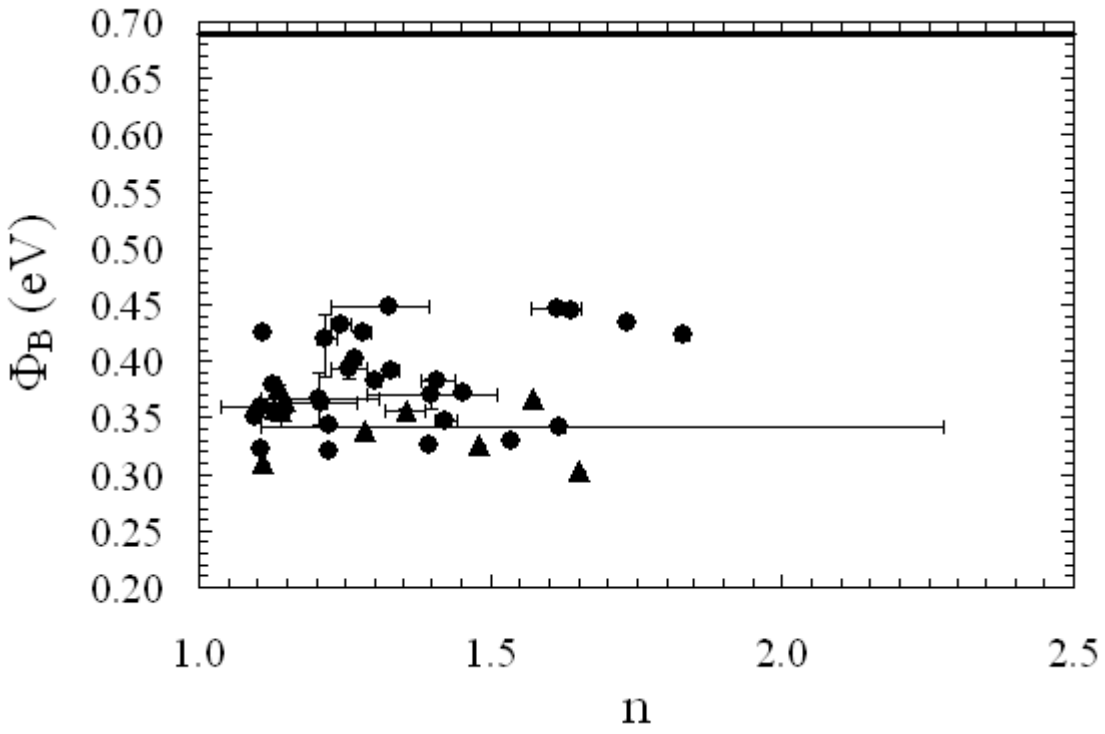

Figure 4.6: Room temperature Schottky barrier height and ideality factor for $CoSi_2$ islands on CS111. As in Figure 4.3, the data points are divided between those islands that are triangular in shape (▲) and those that are non-triangular in shape (●).

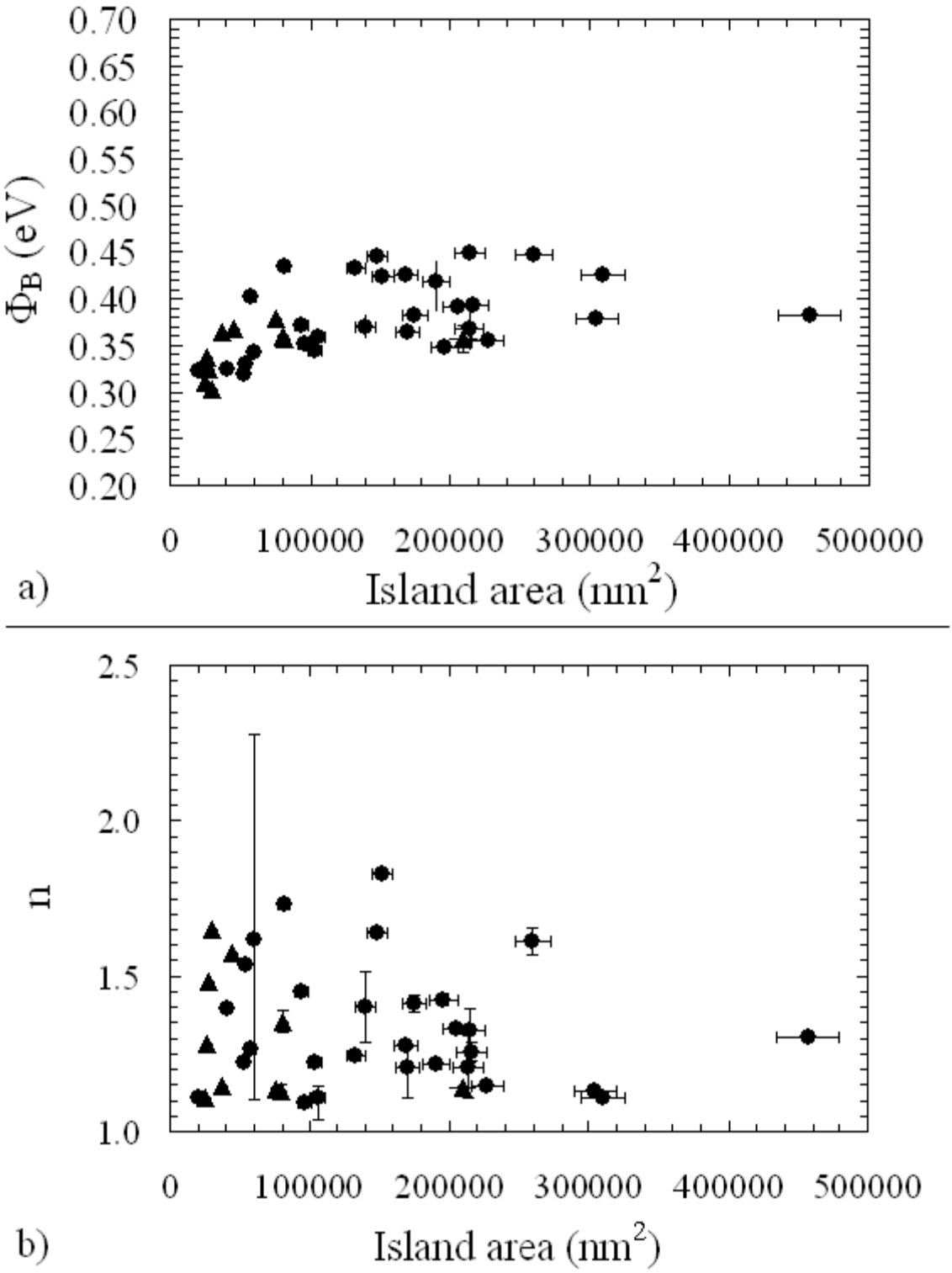

Figure 4.7: Room temperature areal relationships for $CoSi_2$ islands on CS111. (a) Φ_B as related to island area and (b) n as related to island area. The data points for both (a) and (b) are divided between those islands that are triangular in shape (▲) and those that are non-triangular in shape (●).

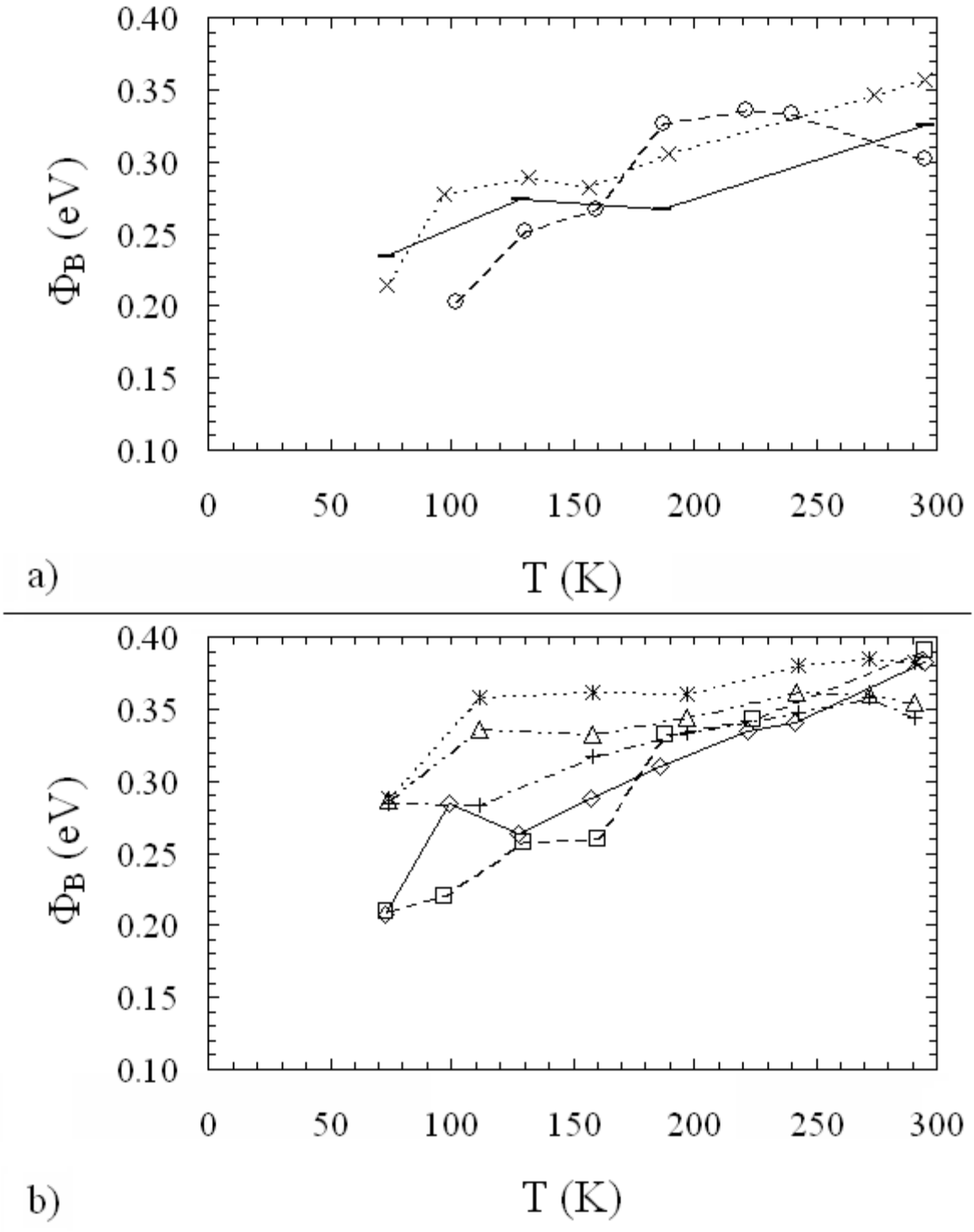

Figure 4.8: Φ_B as a function of temperature for $CoSi_2$ islands on CS111. (a) $\Phi_B(T)$ for triangular islands and (b) $\Phi_B(T)$ for non-triangular islands.

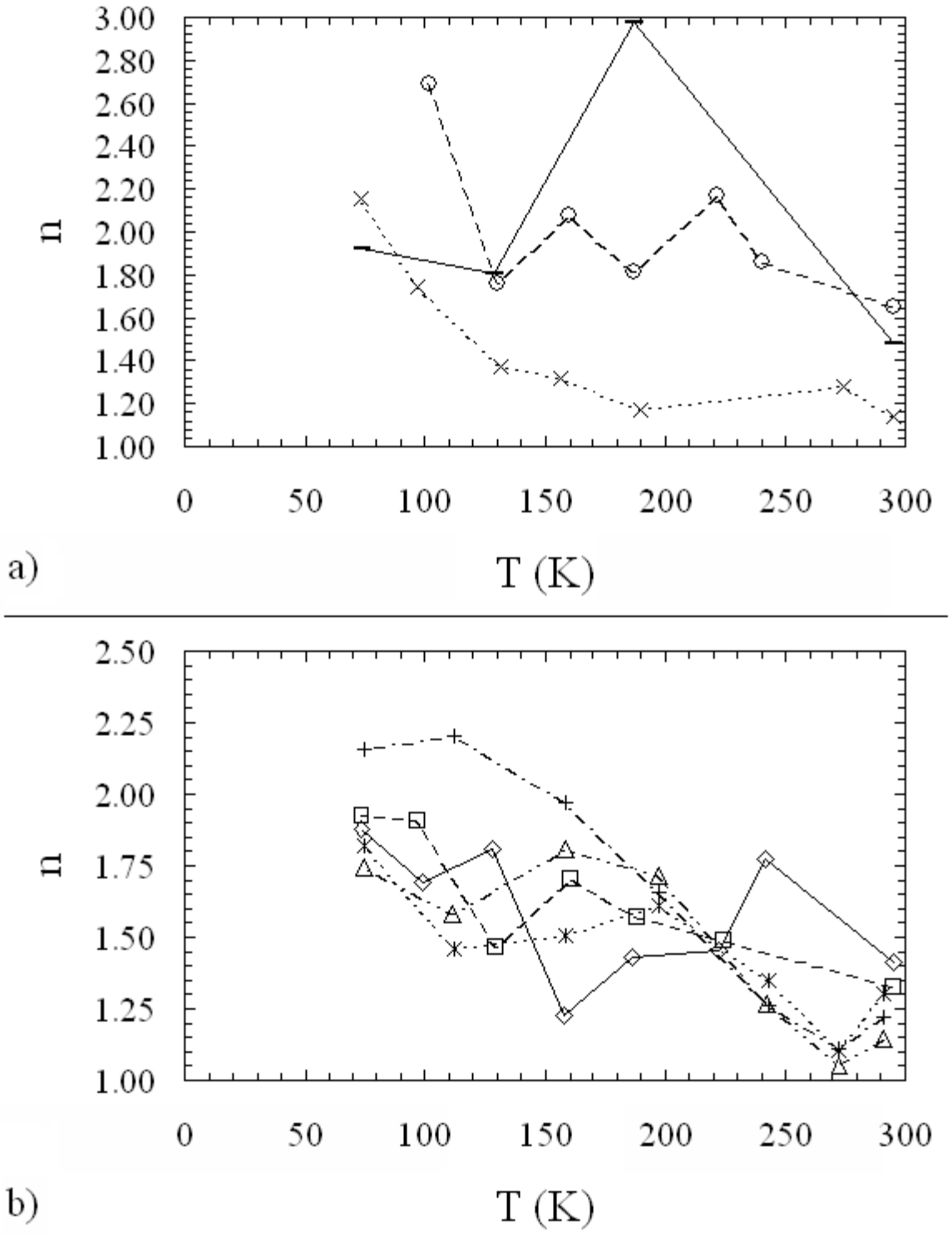

Figure 4.9: Ideality factor as a function of temperature for $CoSi_2$ islands for CS111. (a) n(T) for triangular islands and (b) n(T) for non-triangular islands.

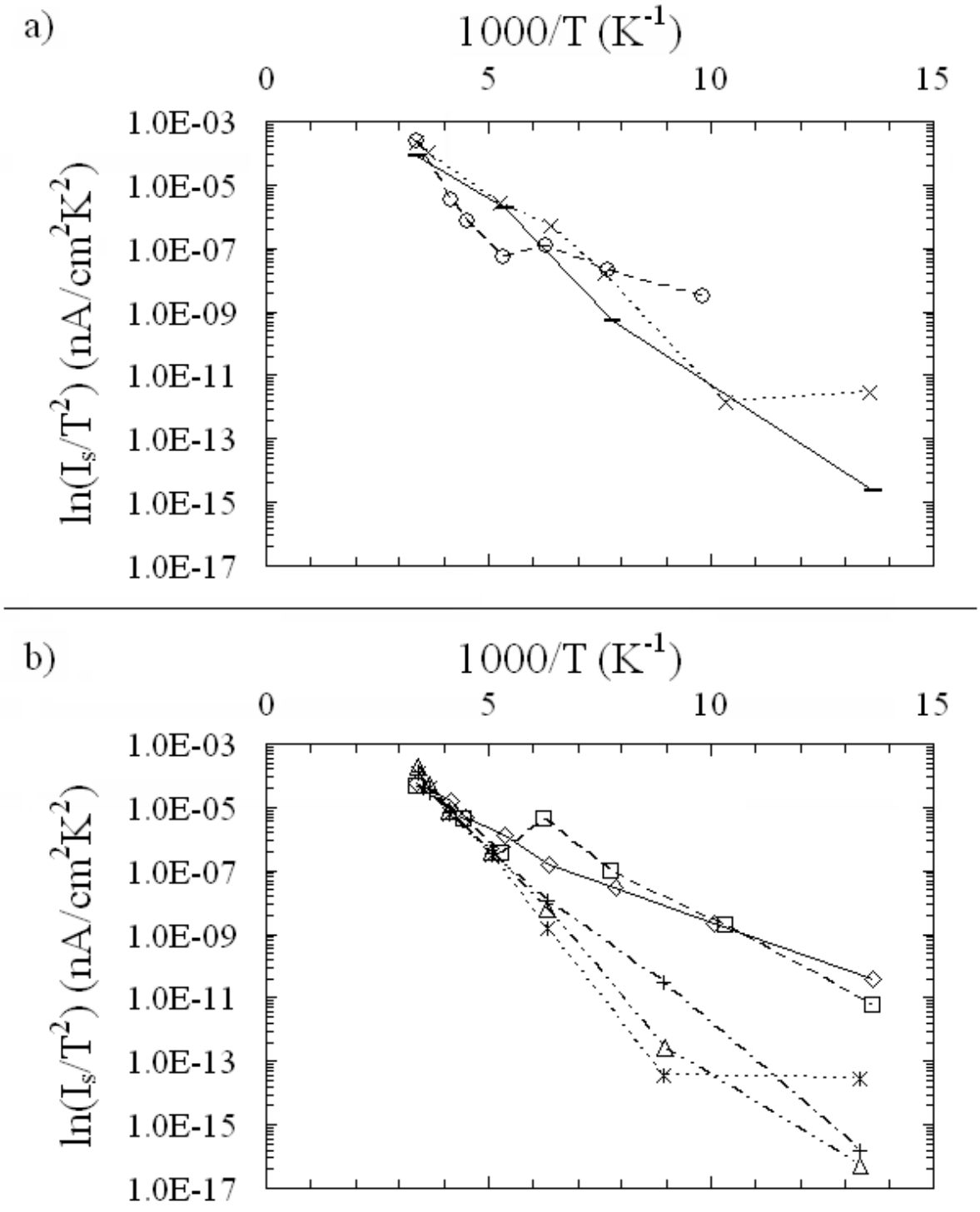

Figure 4.10: Activation energy plot for $CoSi_2$ islands on CS111. (a) Activation energy plot for triangular islands. (b) Activation energy plot for non-triangular islands.

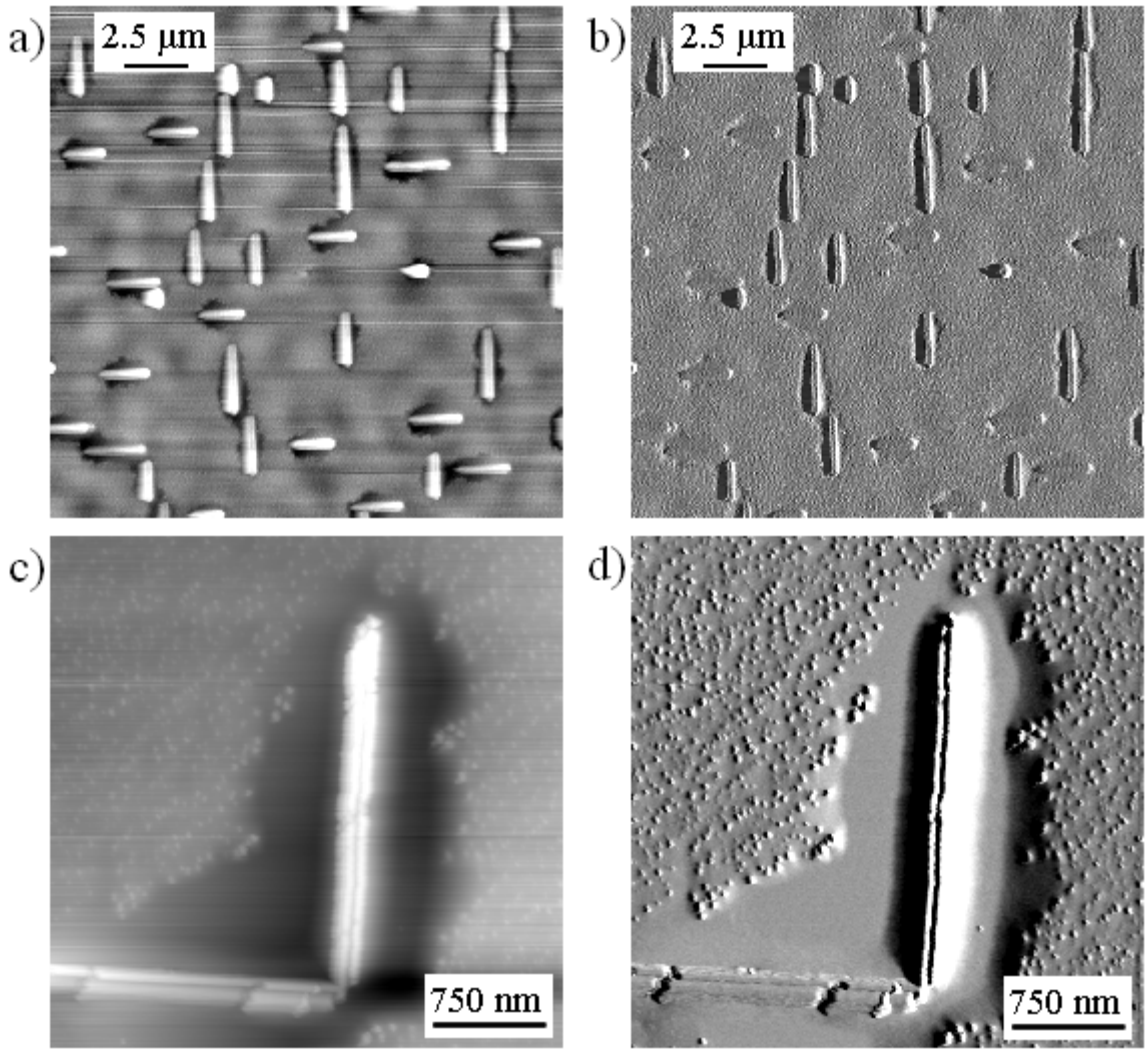

Figure 4.11: $CoSi_2$ islands on CS100. (a) AFM topographical scan of the islands. Scan size: 20.0 µm. Note that the islands are rectangular and the tapered appearance of some of the islands is an image processing artifact. (b) Error signal of the image shown in (a). (c) Detail of rectangular islands. Scan size: 3.0 µm. Note that these islands do not appear in (a). (d) Error signal of the image shown in (c).

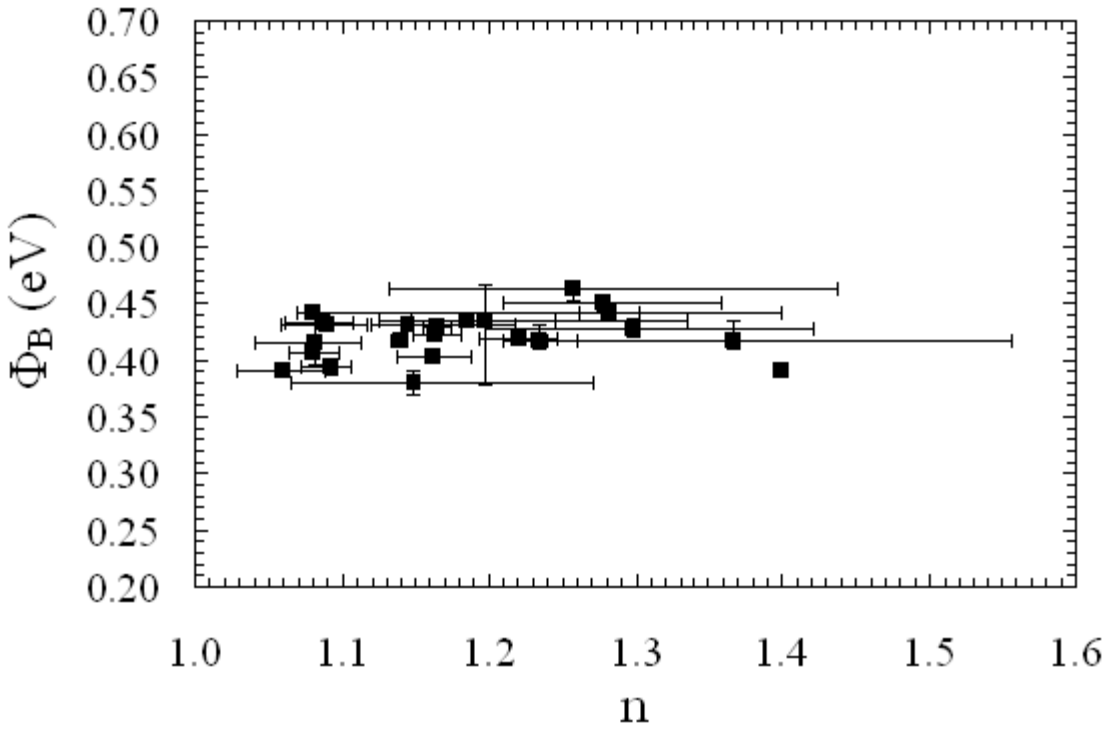

Figure 4.12: Room-temperature Schottky barrier height and ideality factor for $CoSi_2$ islands on CS100.

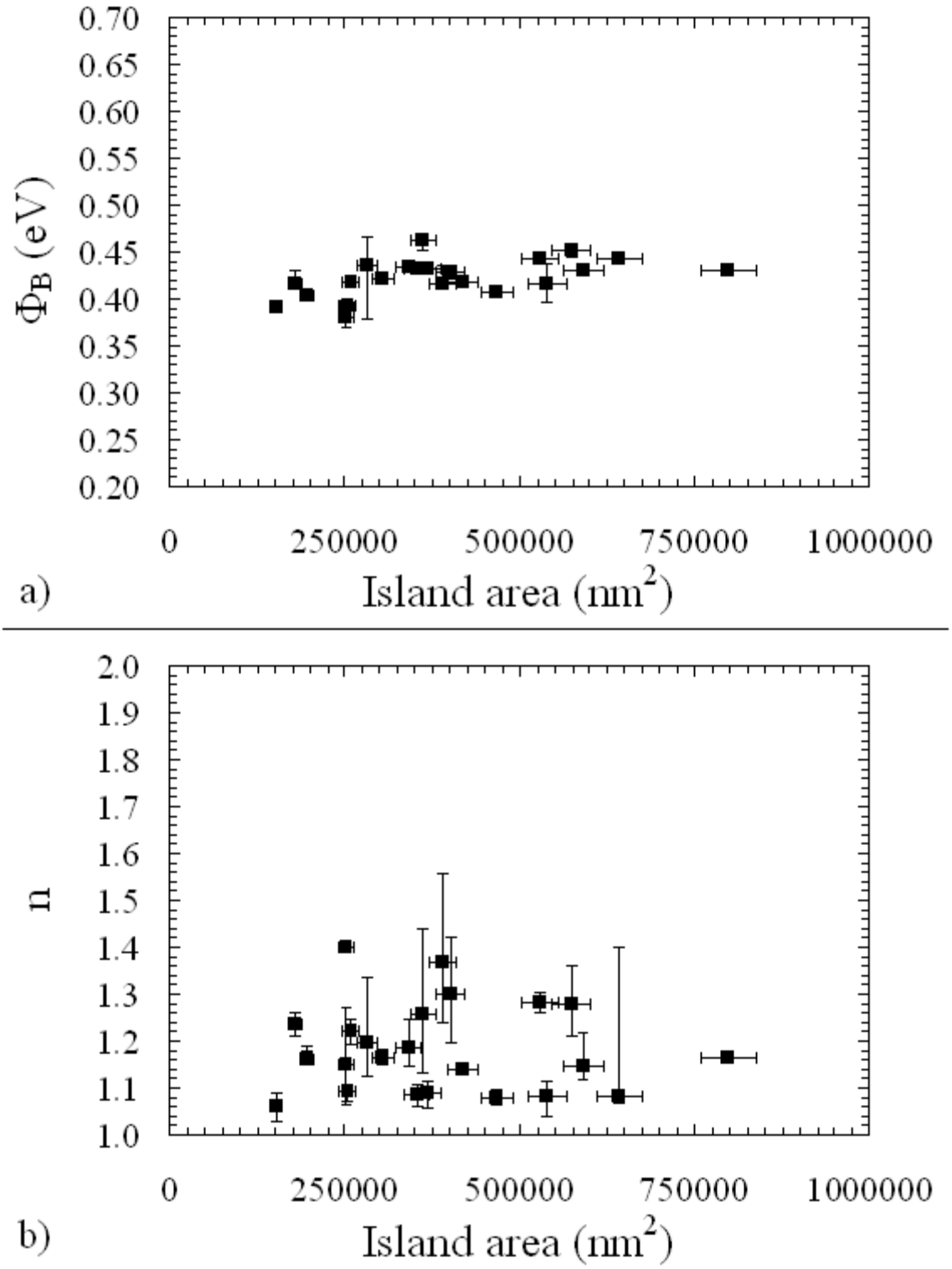

Figure 4.13: Room temperature areal relationships for $CoSi_2$ islands on CS100. (a) Φ_B as related to island area and (b) n as related to island area.

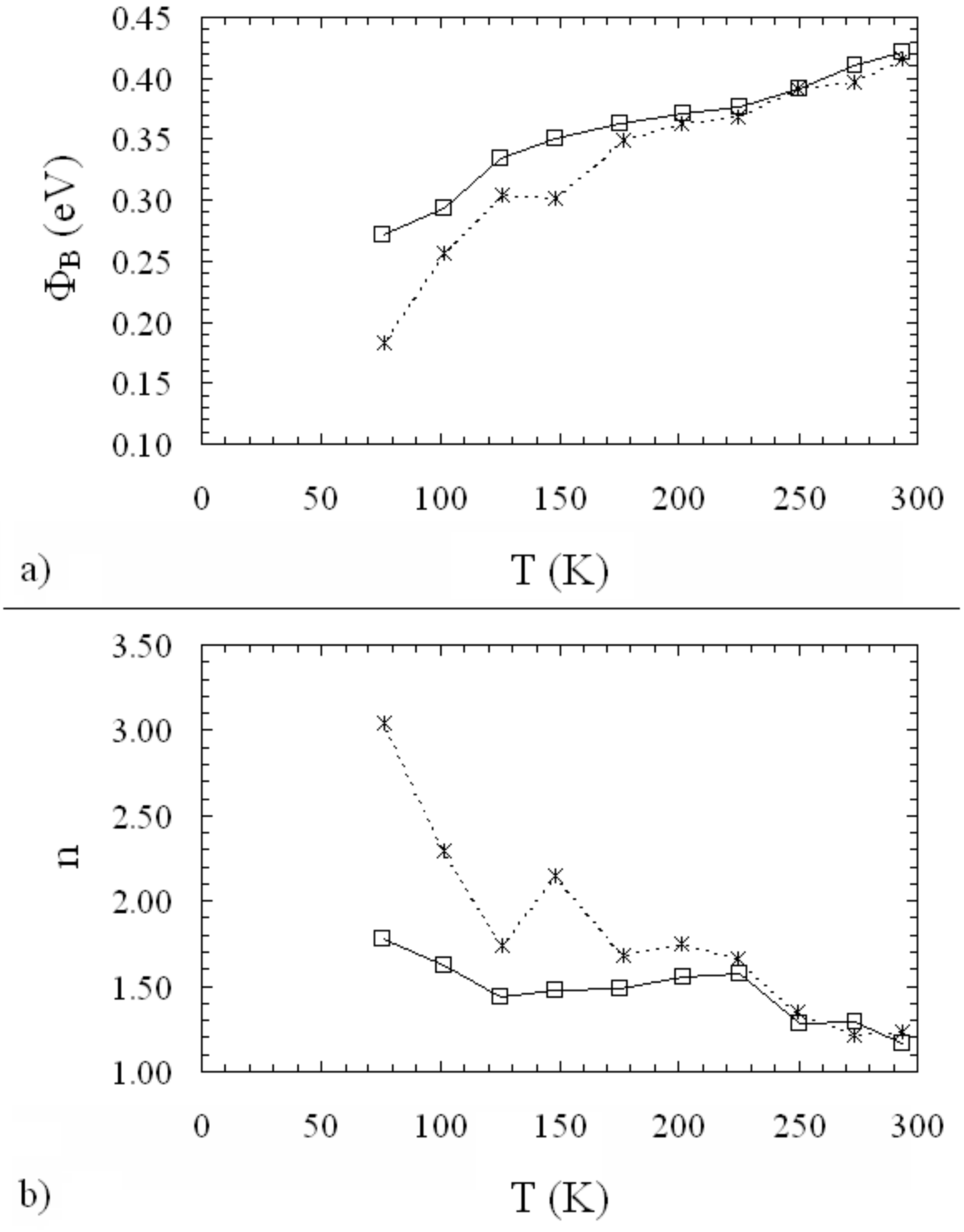

Figure 4.14: Temperature dependent electrical characteristics of $CoSi_2$ islands on CS100. (a) Φ_B(T) measurements and (b) n(T) measurements.

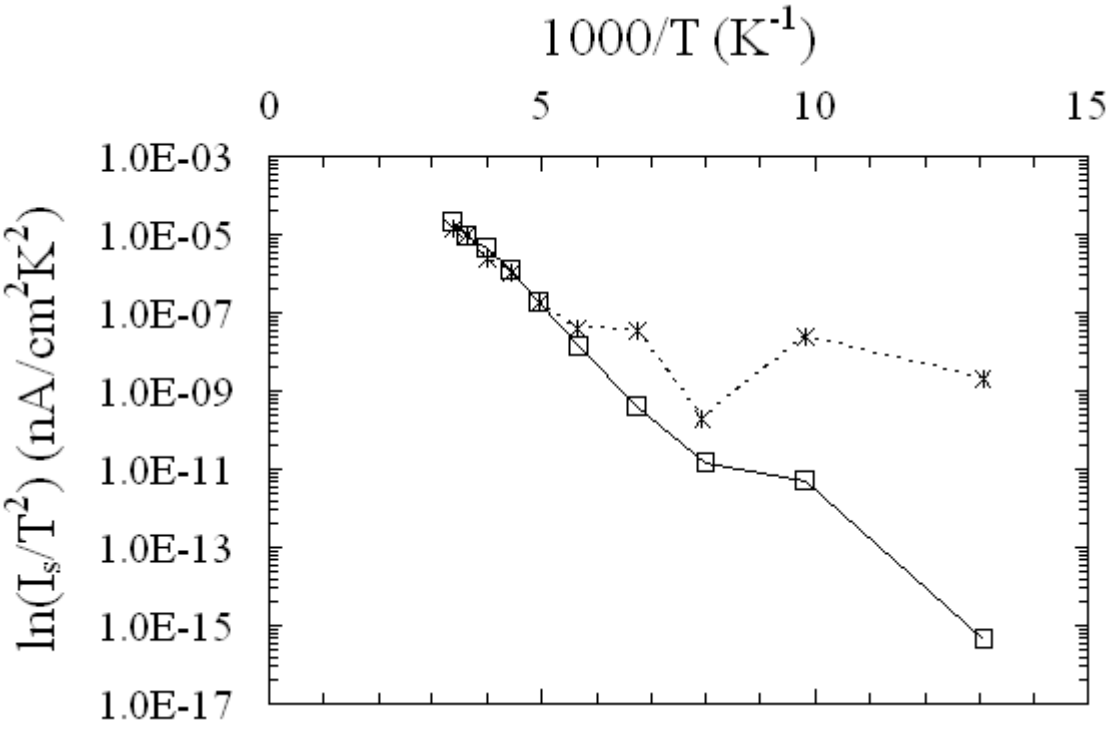

Figure 4.15: Activation energy plot for $CoSi_2$ islands on CS100.

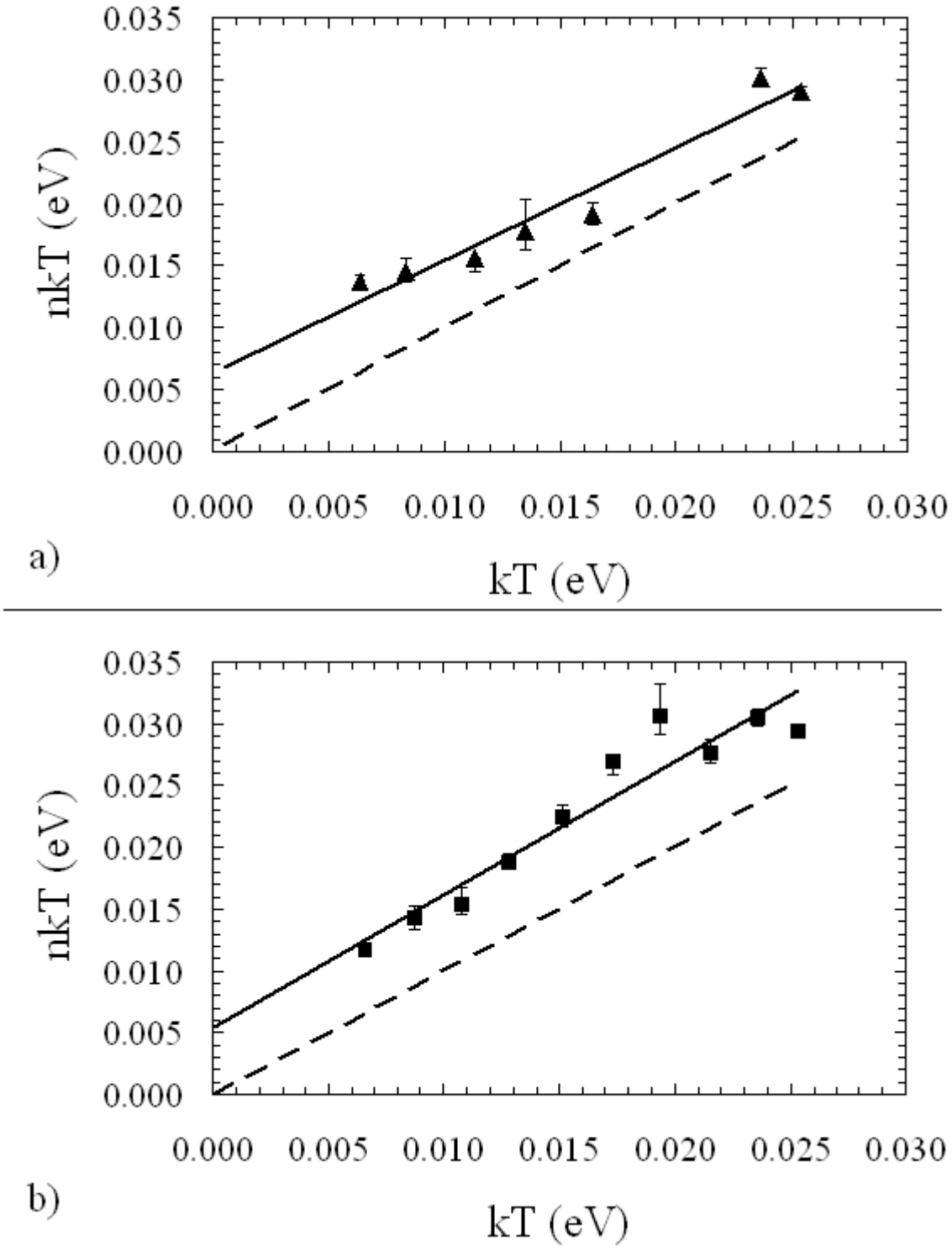

Figure 4.16: nkT vs. kT plots for $CoSi_2$ islands. The dashed curves in both (a) and (b) are curves for n = 1. (a) nkT vs. kT for CS111. (b) nkT vs. kT for CS100.

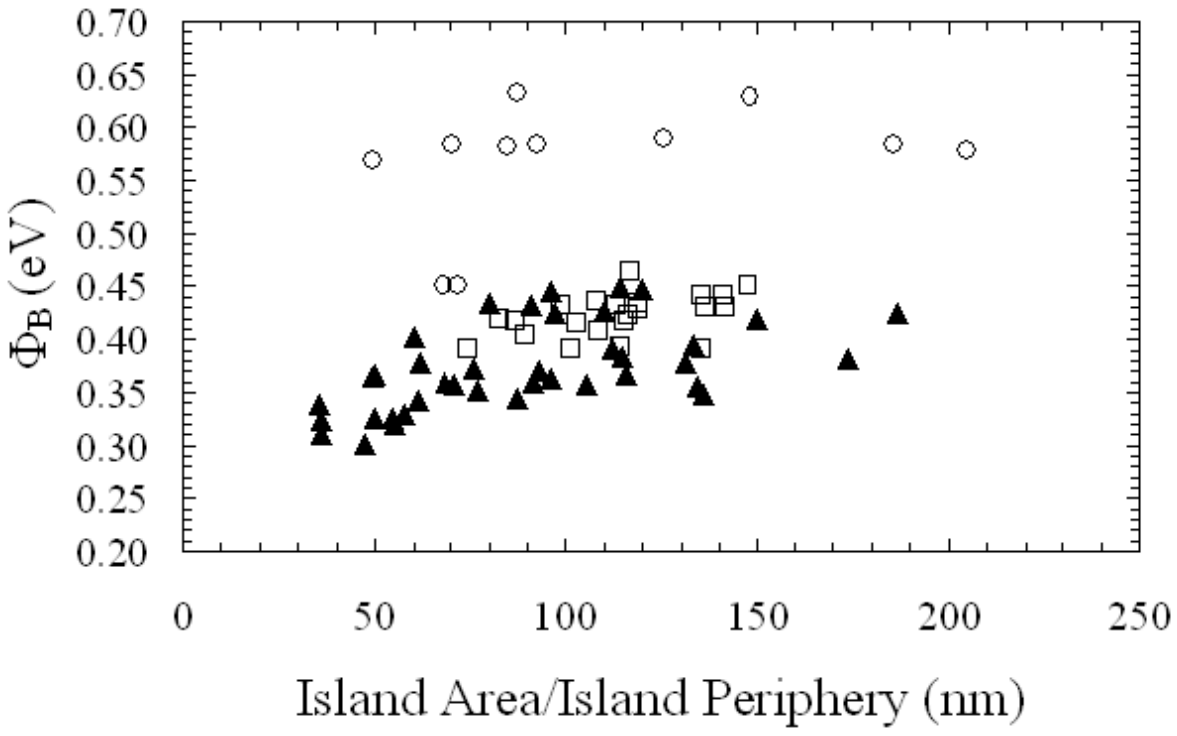

Figure 4.17: Schottky barrier heights as related to the area-to-periphery ratios for $CoSi_2$ islands. The plot is divided between islands on air-exposed surfaces (□), islands on CS111 (▲), and islands on CS100 (○).

Chapter 5:

Variable Temperature Scanning Tunneling Microscopy and Spectroscopy of Titanium Silicide on Si(100) and Si(111)

5.1 Abstract

Titanium silicide islands have been formed by the ultrahigh vacuum (UHV) deposition of thin films of titanium (< 1 nm) on clean Si(100) and Si(111) surfaces followed by annealing to ~800ºC. Scanning tunneling microscopy (STM), scanning tunneling spectroscopy (STS), and a variant of current imaging tunneling spectroscopy (CITS) have been performed on these islands to demonstrate single electron tunneling (SET). Evidence of SET has been identified in current-voltage (I-V) curves recorded from islands at room temperature and compared to the predictions of the orthodox model were found to agree with those predictions. The I-V scans were also analyzed within the framework of the orthodox model of SET and were found to be consistent with that model, except for slight discrepancies of the shape of the I-V curves at current steps. The tunneling spectra of individual islands were also recorded as the temperature was varied, unfortunately, no evidence of SET was identified. In addition to these islands, many other islands that were grown that were expected to exhibit SET did not do so, and the potential reasons for this absence of SET, at both room and low temperatures, were evaluated. Schottky barrier lowering due to interfacial faceting and Fermi level pinning were identified as the most likely

reasons for the absence of SET. The results establish that a Schottky barrier can be used as an effective tunnel junction in a double barrier tunnel junction (DBTJ) structure, which could form the basis of future nanoelectronic devices. However, unless the reasons for the absence of SET are dealt with, islands may prove to be too unreliable for use in future nanoelectronic devices.

5.2. Introduction

With the continued advancement of semiconductor integrated circuit technology, device architectures are reaching the limit where quantum mechanical effects will restrict the performance of conventional device structures [1]. New devices, so-called nanoelectronics, take advantage of physical effects accessible only when the devices dimensions approach the scale of nanometers. One such effect that has shown potential is single electron tunneling (SET). In fact, it has been proposed that SET could form the basis of a digital technology based on single electron devices [2-3].

When a nanoscale metal island of appropriate size is placed between two tunnel barriers, it has the potential to exhibit SET effects. For SET to occur, two criteria must be satisfied. First, the tunnel barriers must have resistances greater than the quantum of resistance, i.e. $R_T > \frac{h}{e^2} \sim 25.8\ k\Omega$. If the resistances of the tunnel barriers are less than this value, the tunneling time, t_τ, will be too short for the electrons to be localized on the island. Second, the charging energy, E_c, associated with a island must be greater than kT. The charging energy is characterized as $\frac{e^2}{2C}$ (where C is the capacitance of the island), and electron transport through the island will be suppressed if this energy is greater than kT. For

the second criteria to be satisfied at room temperature, the diameter of the metallic island must be ~10 nm or less [4].

In these double barrier tunnel junction (DBTJ) structures, tunnel junctions can be described in terms of parallel combinations of R and C connected in series [5]. When the two tunnel junctions are symmetric ($R_1C_1 = R_2C_2$), and the above criteria are satisfied, the Coulomb blockade is the only discernible single electron effect [4]. The Coulomb blockade occurs because charge quantization results in a gap of width $\frac{2e}{C}$ to form in the states available for tunneling [6]. Outside of this gap, the I-V takes on an ohmic appearance because tunneling events occur simultaneously.

However, when the tunnel barriers are asymmetric ($R_1C_1 > R_2C_2$ or vice versa), the current increases in a stepwise fashion at regular intervals as the bias voltage is increased [5]. This is known as the Coulomb staircase because the I-V curve takes on a staircase shape due to a correlated set of tunneling processes occurring when one electron tunnels into and out of the island.

While SET has been studied in several systems, such as metallic particles [4, 7-30], semiconducting islands [31-33], thin films [34-35], and organic molecules [36-37], there have been fewer reports of the efficacy of a Schottky barrier as one of the tunnel junctions [14-18, 20-21, 23, 25-26, 29]. It is important from a technological standpoint to establish if the Schottky barrier can be used effectively in this fashion because metal islands are known to self-assemble on semiconductor substrates [38-41], and the ability to use the Schottky barrier as an effective tunnel junction could minimize the number of processing steps necessary to form nanodevices. Furthermore, nanodevices composed of metallic islands

could be made much smaller than devices composed of semiconducting islands because the electron density in metals is much higher ($n \sim 10^{15}$ cm^{-3} – 10^{19} cm^{-3} for semiconductors versus $n \sim 10^{22}$ cm^{-3} for metals), allowing small islands to have large charging energies and operate at temperatures above 4.2 K [19]. For example, a $TiSi_2$ island 15 nm in diameter would have a charging energy of ~18.2 meV, allowing operation up to ~210 K.

While SET has been proposed for several metal nanocluster systems, such as Au nanoclusters on organic self-assembled monolayers (SAMs) [13, 22], metal particles encased in polymer shells [26, 35], and Ag and Au islands on semiconducting surfaces [14-18, 20-21, 23], each of these materials systems would have difficulty withstanding the temperatures and processing necessary for device fabrication.

Given the considerations of both functionality and stability, titanium silicide ($TiSi_2$) on silicon may prove to be an ideal foundation for future nanoelectronic devices. $TiSi_2$ is already used in current integrated circuit technology [42], and the $TiSi_2$/Si system is capable of withstanding the high temperatures used in device fabrication. Furthermore, measurements have indicated SET characteristics in self-assembled $TiSi_2$ islands [25, 29], but only at room temperature. One method of establishing that features in the I-V curves recorded on an island are due to SET effects is to examine those curves over a range of temperatures. According to the orthodox model for SET [49-52], as the temperature changes, there should be no significant change to the Coulomb staircase, except that as the temperature rises, the steps should become less pronounced as the available thermal energy approaches the charging energy of the island. The other features of the staircase, such as the spacing of the steps, should remain unchanged. Few studies have established SET at multiple temperatures [11, 14, 22, 35-36], and even fewer investigations of SET in similar islands at multiple

temperatures have been reported [14, 22]. This current study would be one of the first to not only investigate SET in a single island across a range of temperatures, but also do so using a metal already commonly used by the integrated circuit industry.

In this study, $TiSi_2$ islands have been formed on Si(100) and Si(111) surfaces and scanning tunneling microscopy (STM) images, as well as the I-V and $\left(\frac{dI}{dV}\right)-V$ characteristics of the islands, have been recorded. A simplified drawing of the tip-island-substrate structure used in these experiments is shown in Figure 5.1(a), while its accompanying DBTJ band structure is shown in Figure 5.1(b). A variant of current imaging tunneling spectroscopy (CITS) has been used to compare the tunneling spectra from different parts of the same island. By obtaining SET signatures at several temperatures, and on different regions of the same island, it can be established that SET has occurred. For those SET signatures demonstrated at only one temperature, comparing the curve with theoretical predictions can establish that the SET is genuine. Furthermore, evidence of genuine SET would suggest that it is possible to use a Schottky barrier as a tunnel barrier in SET-based nanoelectronic devices.

5.3. Experimental

The experiments were performed with an Omicron VT AFM system. The system includes an analysis chamber equipped with a variable temperature ultrahigh vacuum (UHV) STM, low energy electron diffraction (LEED), and Auger electron spectroscopy (AES), as well as a preparation chamber with a triple-cell electron beam deposition source (EFM 3T). The base pressure in the preparation chamber was ~7.0×10^{-11} torr, and the base pressure in the analysis chamber was ~1.5×10^{-11} torr.

Both the (111) and (100) substrates were cut from 25.4 mm diameter, n-type (phosphorus-doped) silicon wafers with a thickness of 0.25 mm ± 0.025 mm and doping concentration of ~10^{17} cm^{-3} (ρ = 0.05 – 0.1 Ω-cm). A diamond-tipped scribe was used to section the wafers into strips ~2 × 10 mm^2 and the same sample preparation procedure was used regardless of substrate orientation. These wafer sections were mounted on to sample cartridges and loaded into vacuum without an *ex situ* chemical clean. To avoid significant outgassing during flashing, the sample cartridge was degassed for several hours in ultrahigh vacuum (UHV) at ~500°C. After this initial heat treatment, direct current heating was used to hold the sample at ~650°C for ~12 hours (overnight). A clean surface was then obtained by flashing the sample in short 2-5 second increments at steadily increasing temperatures, culminating with 2-4 flashes at ~1150°C, each lasting 30 seconds. The temperature was measured using an Ultimax optical pyrometer with the emissivity, ε, set at 0.65 [43]. During flashing, the pressure remained below 1.5 × 10^{-9} torr. Following flashing, LEED was used to confirm the 2×1 or 7×7 reconstruction, for Si(100) or (111) substrates, respectively. After observing the reconstructed LEED pattern, STM and STS were used to characterize the state of the surface. The surface was considered suitable for island formation if it was clean, flat, nominally free of defects, and showed atomic terraces with widths > 10 nm. The STM and STS measurements were performed using electrochemically etched tungsten tips.

Once the surfaces were confirmed to be clean and flat, the samples were transferred to the preparation chamber for deposition. The deposition source was a 2 mm diameter titanium rod of 99.99% purity (Goodfellow). Titanium layers, 0.2 nm to 0.5 nm thick, were deposited with the sample at room temperature. The deposition rate was calibrated by depositing a thick layer of titanium while maintaining a constant flux and then measuring the

resulting layer thickness using an ambient atomic force microscope (AFM). During deposition, the pressure in the preparation chamber did not rise above 1.5×10^{-9} torr and was generally lower. After deposition, AES was used to confirm the presence of titanium and detect carbon and oxygen, which was generally measured at or near the detection limit of the AES instrumentation. After confirming the titanium deposition, samples were annealed at ~800°C for 60 seconds, and LEED was performed. If a diffraction pattern was detected, it was presumed that the titanium had formed into $TiSi_2$ islands, exposing the underlying silicon substrate.

Samples were then transferred into the STM for scanning and STS. The STM scans were recorded with a tip bias between +1.0 V and +2.5 V and a tunneling setpoint of between 0.75 nA and 1.0 nA. The I-V curves were recorded from -2.5 V to +2.5 V and 10,000 I-V curves were recorded per scan, and were analyzed both individually and by averaging several curves obtained on an individual island. Acquiring several I-V curves on the same island also allowed for comparison between I-V curves from different areas of the same $TiSi_2$ island. There are several types of artifacts that can mimic the appearance of steps in an I-V curve. Comparing the I-V curves from different positions on a single island, and finding agreement between those curves, supports the validity of the SET analysis. The I-V curves were numerically differentiated to obtain $\left(\frac{dI}{dV}\right) - V$ curves.

Once I-V curves were recorded at room temperature, liquid nitrogen or liquid helium was used to lower the temperature of the sample. The system is equipped with a cryostat that cools the sample, while the rest of the microscope is held at near room temperature, with the sample temperature monitored by a Lakeshore 331 temperature controller. The I-V scans

were recorded only after the temperature of the sample was nominally stable, i.e. the temperature varied by less than 1°/hr. Generally, the rate of temperature change while recording I-V curves was lower than this value.

5.4. Results

5.4.1. Tunneling spectra of $TiSi_2$ islands and confirmation of SET

$TiSi_2$ islands are known to grow in several shapes on Si(100) [53-54] and Si(111) surfaces [25,44-45,47,55-56]. In this study, however, the islands grown on Si(100) surfaces were predominantly circular, as shown in Figure 5.2(a), while the islands grown on Si(111) surfaces were predominantly circular and triangular, as shown in Figure 5.2(b). The triangular and circular islands grown on Si(111) surfaces tended to have flat top surfaces.

Prior to examining SET signatures from $TiSi_2$ islands, it is necessary to establish that the step-like I-V curves are actually due to SET and not artifacts. Using a tungsten tip and $TiSi_2$ islands eliminates oscillations in the density of states of either the tip or the islands from being the origin of step-like features in the I-V curves. Additionally, while silicon does have a band gap and surface states, these would not contribute to regularly-spaced step-like features in the I-V curves. To eliminate tip contamination as the source of the step-like features, I-V curves were recorded on islands near those islands exhibiting step-like features. One such I-V curve is shown in Figure 5.4(c) and does not exhibit regular step-like structures. Current oscillations, the oscillations caused by partial reflection and interference of the electron wave as the electron tunnels [48], cannot be conclusively ruled out; however, they are not likely to be the source of the step-like structure in the I-V curves for two reasons. First, larger islands near those shown in Figure 5.3(a) do not exhibit step-like structures in I-

V curves recorded on them, as shown in Figure 5.4(c), which appears to indicate that there are no current oscillations. Furthermore, current oscillations are known to increase proportionally with increases in the current [23] and this does not happen here, as shown in Figures 5.4(a) and 5.4(b). Having established that the step-like I-V curves are due to SET and not due to artifacts, the SET signatures in the I-V curves can be identified and analyzed in detail.

Tunneling spectra from several dozen islands were recorded, both singly and using the modified CITS procedure discussed previously. The size distribution of the islands is displayed in Figures 5.5(a) and 5.5(b). As shown in Figures 5.5(a) and 5.5(b), most of the islands are large and would not be expected to exhibit SET, however, there were islands grown that were of a size where the orthodox model predicts SET. Islands that were not round in shape were excluded from the histogram due to the difficulty of determining reasonable approximations to use for calculating their self-capacitances. This exclusion does not affect statistics regarding observation of SET, because no non-round islands measured in this study exhibited SET. The fact that there was not a higher incidence of SET observed in the measured I-V curves will be discussed later.

5.4.2. Coulomb staircase at room temperature

Figure 5.3(a) shows an array of $TiSi_2$ islands grown on an n-type Si(100) surface and imaged at room temperature. STS was used to record I-V spectra from several islands in the scan area. The size of most of the islands is greater than the maximum size predicted to allow observation of SET at room temperature [4], however, the islands indicated in Figure 5.3(a) with the numbers “2” and “5” have radii of 7.0 ± 0.25 nm and 3.0 ± 0.325 nm, respectively,

both of which are small enough to expect to observe SET at room temperature [4]. The line scans shown in Figures 5.3(b) and 5.3(c) demonstrate that the features indicated are indeed islands.

As shown in Figures 5.4(a) and 5.4(b), the I-V curves demonstrate a series of regular steps and the $\left(\frac{dI}{dV}\right)-V$ curves exhibits regular peaks. Peaks in the $\left(\frac{dI}{dV}\right)-V$ curves indicate incidents of increased conduction, which is a sign of SET. Furthermore, the fact that the conductance increases are more pronounced for voltages greater than zero than for voltages less than zero is consistent with SET observed from islands on n-type substrates [25]. The tunneling spectra shown in Figures 5.4(a) and 5.4(b) will be analyzed in further detail later.

5.5. Discussion

5.5.1. Analysis via the orthodox model

According to the orthodox model [49-52], the steps in the Coulomb staircase should have the width,

$$\Delta V = \frac{e}{C_\Sigma}, \tag{5.5.1}$$

where $C_\Sigma = C_T + C_I$, where C_T is the tip-island capacitance and C_I is the island-substrate capacitance [57-59]. Before continuing to evaluate these values for the specific nanostructures, it is necessary to develop the models used to approximate both capacitances. C_I can be approximated by considering the nanostructure to be a metal sphere of diameter d surrounded by a material with permittivity ε_r,

$$C_I = 2\pi\varepsilon_r\varepsilon_0 d, \tag{5.5.2}$$

where ε_0 is the permittivity of free space. This approximation is commonly used in the literature, where the sphere is said to be in vacuum ($\varepsilon_r = 1$) [4,11,25,60]. The approximation for C_T uses the method of images to calculate the capacitance of two spheres of diameters d_1 and d_2 separated by a distance *s* in a material of permittivity ε_r [25,61]. Assuming that higher order terms are negligible,

$$C_T \approx \frac{\pi \varepsilon_r \varepsilon_0 d_1 d_2}{s}. \tag{5.5.3}$$

Utilizing Eq. 1 and the tunneling spectra from Figures 5.4(a) and 5.4(b), the C_Σ values for the nanostructures shown in Figures 5.4(a) and 5.4(c), respectively, can be determined and compared to the theoretical values predicted using Eqs. 5.5.2 and 5.5.3.

Considering first the island labeled "2" in Figure 5.3(a), from the tunneling spectra shown in Figure 5.4(a), ΔV is determined to be 0.33 ± 0.02 V. Therefore, according to Eq. 5.5.1, the C_Σ value for this island is expected to be $4.85 \times 10^{-19} \pm 0.29 \times 10^{-19}$ F. From the line scan shown in Figure 5.3(b), the diameter of island "2" is 7.0 ± 0.25 nm. Using Eqs. 5.5.2 and 5.5.3, and taking the tip diameter, d_1, to be 0.15 nm (a reasonable approximation given that the radius of a tungsten atom is ~0.141 nm [62]) and the distance s to be 0.5 nm, $C_\Sigma \approx 5.06 \times 10^{-19} \pm 0.18 \times 10^{-19}$ F. By using this value in Eq. 5.5.1, the predicted value of ΔV is 0.317 ± 0.01 eV. The remarkable agreement between the theoretical values and experimentally-determined values of C_Σ and ΔV suggests that the Coulomb staircase shown in Figure 5.4(a) is genuine and fits the predictions of the orthodox model.

Considering next the island labeled "5" in Figure 5.3(a), ΔV is determined to be ~0.63 ± 0.02 V from the tunneling spectra shown in Figure 5.4(b). Therefore, according to Eq. 1, the C_Σ value for these nanostructures, from Eq. 5.5.1, is expected to be $\sim 2.54 \times 10^{-19} \pm$

0.09×10^{-19} F. From the STM line scan shown in Figure 5.3(c), the diameter of the indicated nanostructure is determined to be 3.0 ± 0.325 nm. Using the same process as above, $C_\Sigma \approx 2.17 \times 10^{-19} \pm 0.25 \times 10^{-19}$ F and the predicted value of ΔV is 0.739 ± 0.08 eV. The theoretical values of C_Σ and ΔV are close to the actual values calculated from the tunneling spectra shown in Figure 5.4(b), especially given the crude approximations used, suggesting that the Coulomb staircase shown in Figure 5.4(b) is also genuine.

5.5.2. Discrepancies with predictions of the orthodox model

There are several features in the recorded I-V curves exhibiting SET that differ from the predictions of the orthodox model. These features include: uneven step heights, asymmetric current increases at positive and negative voltages, and rounding of the top edge of the steps. The orthodox model predicts steps in the I-V curve that are equidistant, as shown by Eq. 5.5.1, and step heights that are also equivalent, except for the first step, which is half the height of subsequent steps [5]. Due to these equal step heights, the heights of successive peaks in the $\left(\frac{dI}{dV}\right) - V$ curve are also predicted to be equal. However, in the recorded I-V curves, the peaks are not equal, and their intensity is more pronounced on one side of zero bias than on the other. Each of the non-orthodox features described can be explained by the fact that the tunneling processes in this study are more complicated than those considered in the original orthodox model.

In the STM tip-metal island-semiconductor substrate DBTJ system studied here, non-linear current transport occurs via thermionic emission over the barrier at the $TiSi_2$/Si interface [19], which is non-linear because the effective barrier height at the $TiSi_2$/Si

interface is voltage-dependent. The height of the effective barrier at the $TiSi_2$/Si interface is based on the width of the depletion zone, which varies due to the amount of band bending as the interface is biased [63]. As the amount of band bending changes, the width of the barrier to tunneling will change, causing the tunneling rate to vary in a non-linear manner. Furthermore, while the barrier to tunneling decreases with increasing voltage when the interface is forward biased, the barrier height remains nearly constant when the interface is reverse-biased [25]. Both of these facts explain the uneven step heights and the asymmetry in differential conductance peak heights between positive and negative voltage. The step heights are uneven because the increase in current between tunneling events is non-linear due to non-linear changes in the effective barrier height. Furthermore, such non-linear increases in the effective barrier height lead to differential conductance peaks that are more pronounced when the interface is forward-biased. For n-type substrates, such as those used in this study, the interface is forward-biased when the bias applied to the tip is positive, which explains why the peaks in the $\left(\frac{dI}{dV}\right)-V$ curves shown in Figures 5.4(a) and 5.4(b) are more pronounced for positive tip voltage than for negative tip voltage. The voltage-based asymmetry in barrier height changes is also the source of the asymmetry in the positive and negative current increases. As shown in Figures 5.4(a) and 5.4(b), the value of the current at positive bias is greater than the value of the current at negative bias. This asymmetry is due to the fact that as the barrier height decreases with increasing positive bias, the tunneling rate increases, and the amount of current transported across the interface increases for corresponding voltage increases, while the barrier height does not change significantly with

increasing negative bias, leading to a tunneling rate that does not change significantly, and a current that does not increase as quickly with increasing voltage as it did for positive bias.

Of the stated non-orthodox features, the only one not explained by the voltage-dependent effective barrier height at the $TiSi_2$/Si interface is the rounding of the steps in the I-V curves. According to the orthodox model, the increases in current occur when the applied voltage supplies enough energy to exceed the charging energy of a island and tunnel onto it. The electron tunnels through the barrier onto the island in the characteristic time t_τ, which is on the order of 10^{-15} s [7]. Such a short time interval leads to the current increase appearing constant in I-V curve with a sharp step edge. In this study, however, the edges of the steps appear rounded, as shown in Figures 5.4(a) and 5.4(b). This rounding is likely due to thermal activation of tunneling processes [24]. As the temperature is increased, states above the Fermi energy are populated and states below the Fermi energy are emptied [5]. As more states appear below the Fermi level, there are more states available for electrons to tunnel into, leading to a gradual rounding of the top edge of the steps as the temperature increases [7]. Furthermore, the steps naturally become dull as the bias increases [23], independent of temperature.

5.5.3. Absence of SET

In this study, few islands appear to exhibit SET. Sometimes, the reason for the lack of SET is obvious because the islands are very large and their charging energy is much less than kT and the available thermal energy provides sufficient energy to overcome to allow electrons to overcome the tunneling barriers. This explanation, however, does not explain why numerous islands that meet the requirement $E_C > kT$ do not exhibit SET. Additionally,

while it is possible that the SET signatures of some islands measured at low temperature could be obscured by vibrations in the I-V curves generated by the cryogenic liquid, such vibrations are absent at room temperature, and thus, the explanation cannot explain the lack of SET in many islands measured at room temperature. An alternate suggestion that the quantum electromagnetic fluctuations could be preventing the occurrence of SET effects is invalid because, while such electromagnetic fluctuations would wash out SET in a single tunnel junction [64], they would not do so in a DBTJ [65] system.

An alternate explanation to the lack of SET is suggested by other studies that claim that SET can only occur in islands on semiconductor surfaces if the islands are very close together [16, 37]. Those studies claimed that lateral electric conduction through a common space charge region was the origin of SET. However, in these studies, the islands were within a few angstroms of each other, and that is not the case in the present study nor was it the case in previous studies [15,17,25]. Furthermore, some islands have been grown that were close together, as shown in Figure 5.6(a), but did not exhibit SET, as shown in Figures 5.6(b) – 5.6(d). Therefore, a lack of lateral conduction is not the explanation for the lack of SET in those islands from which it would be expected.

The possibility that surface contamination may have caused SET to not be observed must be considered. It is possible that a level of surface contamination existed and that during annealing, the contaminants were either absorbed by the silicide islands, thus changing their properties, or they coalesced into contaminant islands. This explanation would offer a chance of explaining why some of the islands did not exhibit SET, but it does not appear to be a valid explanation for the lack of SET in well-formed, apparently epitaxial islands on an otherwise-clean surface.

Theoretical studies have been performed to suggest that the Coulomb staircase can only be observed when both the resistance and capacitance of one junction is greater than the resistance and capacitance of the second junction (i.e. $R_1 > R_2$ and $C_1 > C_2$), but not if $R_1 > R_2$ and $C_1 < C_2$ [5]. The islands studied here would seem to fit the second category, because the resistance of the vacuum gap between the STM tip and island is greater than the resistance between the island and the silicon substrate, while, according to Eqs. 5.5.2 and 5.5.3, the tip-island capacitance is less than the island-substrate capacitance. However, the study also suggests that while the Coulomb staircase would not be observed, the Coulomb blockade would still be visible [5]. In the islands where no SET is observed, neither the Coulomb staircase nor the Coulomb blockade is observed. Furthermore, the islands that do exhibit SET conform to the same relationship between the resistance and capacitance as do the islands that do not. The fact that the islands indicated in Figure 5.3(a) exhibit SET, as well as the islands in a previous study [25], would appear to suggest that the explanation for the lack of SET is different. To investigate the importance of this effect and its impact on SET, a temperature dependent study would be necessary. If tunneling spectra of a island were successfully recorded across a wide range of temperatures, it would not only confirm that the SET was genuine, it would also allow this theory to be tested because SET signatures would become more evident as the temperature decreased.

Of the requirements for SET, the only one that has not been addressed is the requirement that the resistances of both tunnel barriers exceed the resistance quantum, ~25.8 kΩ. The resistance of the vacuum gap is on the order of several hundred MΩ, judging by the values of the current at high voltage in the recorded I-V curves. If the resistance of the vacuum gap changed significantly, that would cause a significant increase in the current at

high voltage in the I-V curves, which is not observed. As for the tunnel barrier at the $TiSi_2$/Si interface, a previous study found the resistance of this junction to be ~10 MΩ when the substrate doping concentration was ~10^{15} cm^{-3} [66]. While this value is significantly greater than the quantum of resistance, it is possible that the resistance of the junction is significantly less when the substrate doping is ~10^{17} cm^{-3}, as was the case here. Furthermore, prior studies have suggested that the Schottky barrier height, and thus the resistance of the junction, can be lowered significantly for islands [60,66]. It has been suggested that faceting of the island could lead to a locally enhanced electric field, which could substantially decrease the barrier height in the region of the facet. Prior research suggests that ~50% of $TiSi_2$ islands grown at 800ºC form some degree of faceting at the interface [67]. If the islands formed sharp enough facets, the radius of curvature could be small enough that it would cause a significant increase in the field density around the facet. Coupled with a lower value of the junction resistance, this increased field density could potentially lower the barrier height enough that the junction resistance is of the same order as the resistance quantum. Therefore, the lower resistance of the substrate coupled with interfacial faceting could explain the lack of observable SET.

To investigate this possibility further one of two methods could be employed: cross-sectional transmission electron microscopy (X-TEM) or atomic force microscopy (AFM). For the latter technique to be successful, the $TiSi_2$ islands would need to first be etched off the surface using HF. However, AFM has the advantage over X-TEM of providing the shape of the whole interface as opposed to a single cross-section of the interface. Both techniques, however, are beyond the scope of the present study. A temperature-dependent study would

also aid in the investigation of the role of field enhancement because field enhancement is constant across all temperatures.

Related to the low resistance of the substrate is the fact that the Schottky barrier of the islands is likely lowered by Fermi level pinning of the surface states of the silicon surface. It has been found in previous photoemission studies that the Schottky barrier height can be pinned by ~0.4 – 0.55 eV depending on the step density and the condition of the surface [68-69]. The Schottky barrier height of $TiSi_2$/Si system is typically measured to be 0.6 eV [70], however, if the barrier height is pinned 0.2 eV below this value, the barrier height will be correspondingly lower, especially for the small islands necessary to observe SET. With the barrier height of the island's Schottky barrier pinned by the surface states, the resistance of the tunnel junction could be of the order of the quantum of resistance. Thus, the electron will not be localized on the island and SET will not be observed. The fact that SET is observed in a few islands suggests that those islands that the barrier heights of those islands are not pinned for some reason. This possibility can be tested by forming small $TiSi_2$ islands on passivated surfaces. The surface passivation should eliminate the effect of the surface states, thus preventing the barrier height of the $TiSi_2$ island from being reduced due to pinning.

Regardless of the reason for the absence of observed SET, it still remains that out of 651 islands measured throughout the SET study, SET was only observed twice. Of the islands measured, 290 islands had diameters less than 10 nm, yielding a success rate of 0.69% of observing SET. This low success rate implies that before $TiSi_2$ islands can be used in SET devices, their reliability must be improved.

5.6. Conclusion

$TiSi_2$ islands have been formed on Si(100) and Si(111). I-V curves recorded on these islands at room temperatures have shown evidence for SET and the steps in the Coulomb staircases were analyzed and were found to agree with the structure predicted by the orthodox model. There were discrepancies between the shape of the recorded I-V curves and those predicted by the model, however, these were attributed to non-linear current transport over the Schottky barrier at the $TiSi_2$/Si interface and thermally activated tunneling processes. The fact that fewer islands than predicted by the orthodox model exhibited SET was also investigated. Several reasons for the lack of observable SET from other studies were examined and most were disregarded as being invalid under the present circumstances given the recorded data. Schottky barrier lowering due to island interfacial faceting and Fermi level pinning were identified as the most likely reasons for the lack of observable SET. The results indicating the genuine nature of the SET suggest that the Schottky barrier may be used as one of the tunnel junctions, and by extension, that islands may be used as a basis for future nanoelectronic devices. However, the results also indicate that many islands that are expected to exhibit SET do not exhibit observable SET and unless this problem is addressed, islands may be too unreliable to be used as the basis for nanoelectronic devices.

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Figures

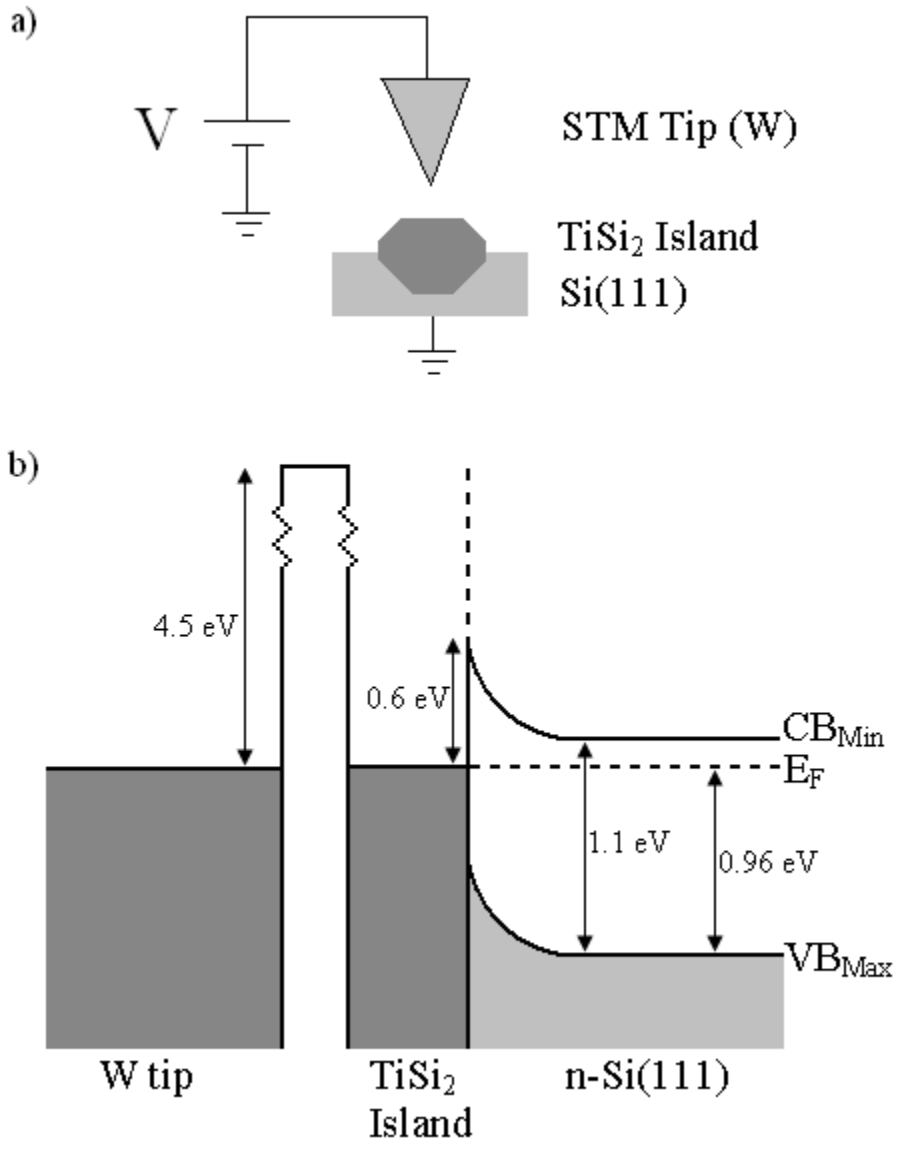

Figure 5.1: a) Simplified drawing of DBTJ in these experiments. b) Diagram of the band structure associated with the DBTJ structure shown above. Note that this represents the band structure for the equilibrium case (V=0) when $N_D \sim 10^{17}$ cm^{-3}.

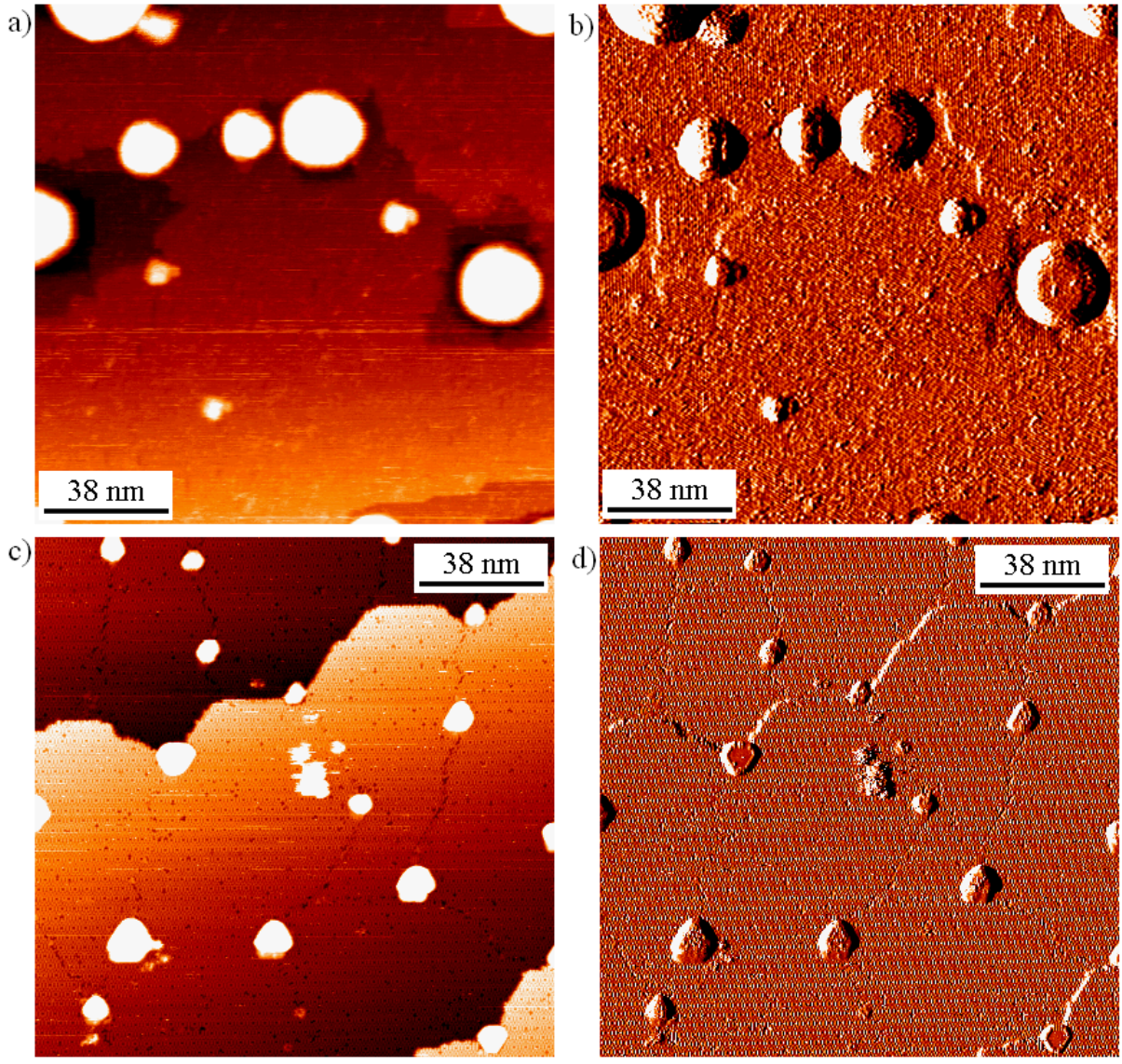

Figure 5.2: $TiSi_2$ islands grown on silicon surfaces. (a) STM image of $TiSi_2$ islands on a Si(100) surface. Scan size: 150 nm. Tip bias: +1.0 V. Tunneling setpoint: 1.0 nA. (b) STM error signal image of $TiSi_2$ islands shown in (a). (c) STM image of $TiSi_2$ on a Si(111) surface. Scan size: 150 nm. Tip bias: +1.0 V. Tunneling setpoint: 1.0 nA. (d) STM error signal image of $TiSi_2$ islands shown in (c).

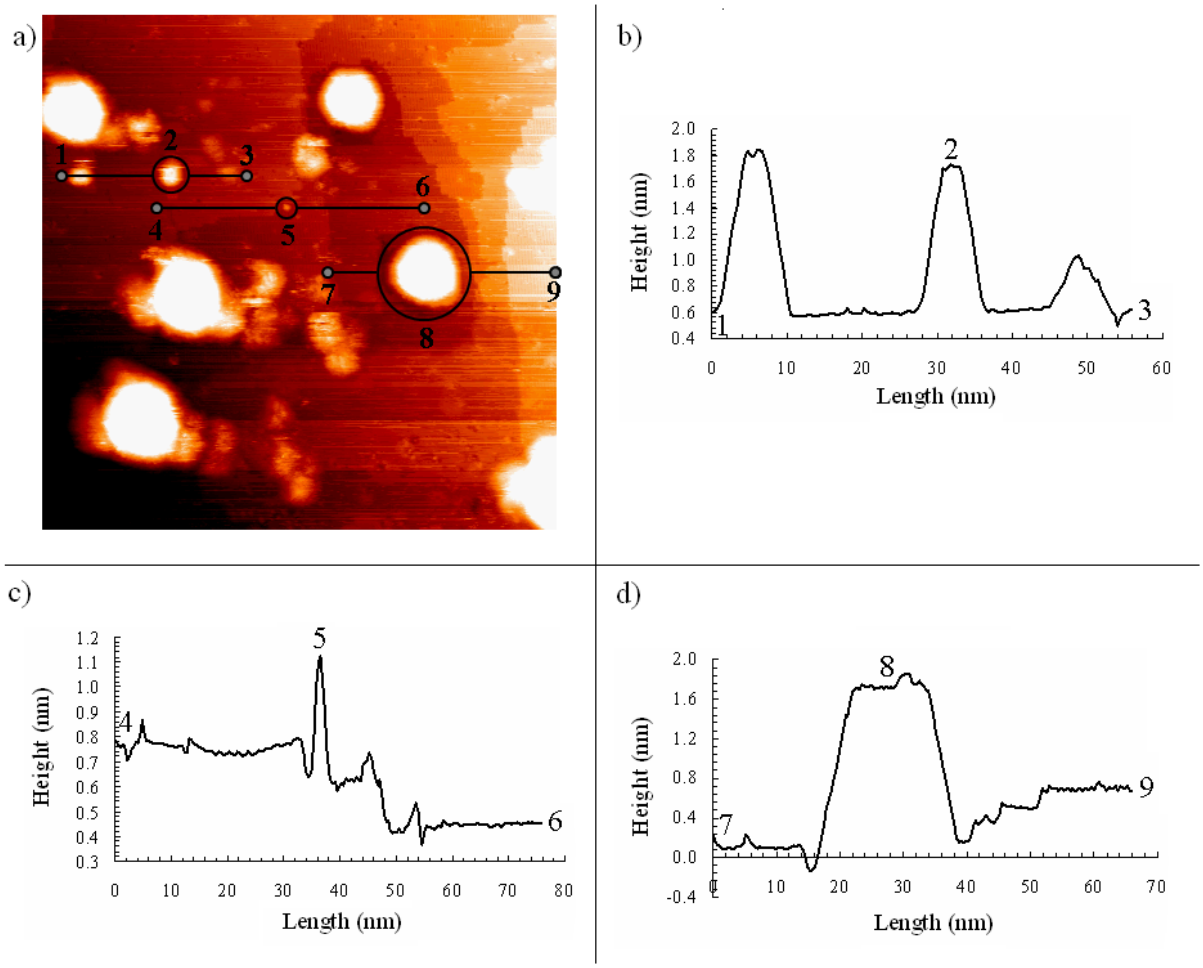

Figure 5.3: Image and line scans of $TiSi_2$ islands on Si(100). (a) STM image of $TiSi_2$ islands on n-type Si(100):2×1. Scan size: 150 nm. Tip bias: +1.0 V. Tunneling setpoint: 1.0 nA. (b) Line scan of island labeled by numbers 1 – 3. (c) Line scan of island labeled by numbers 4 – 6. (d) Line scan of island labeled by numbers 7 – 9.

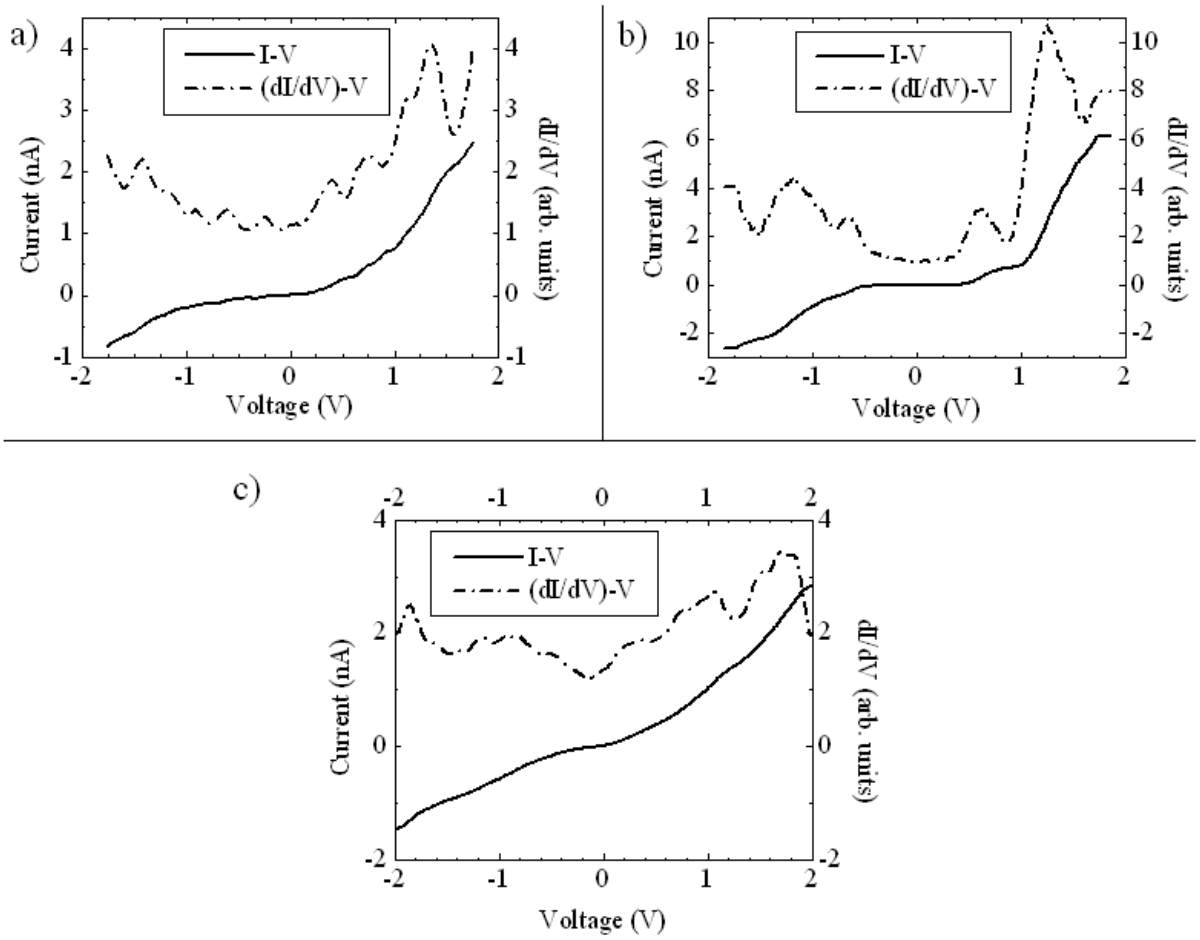

Figure 5.4: (a) I-V and $\left(\frac{dI}{dV}\right)-V$ curves of the island labeled "2" in Figure 5.3(b). (b) I-V and $\left(\frac{dI}{dV}\right)-V$ curves of the island labeled "5" in Figure 5.3(c). (c) I-V and $\left(\frac{dI}{dV}\right)-V$ curves of the island labeled "8" in Figure 5.3(d).

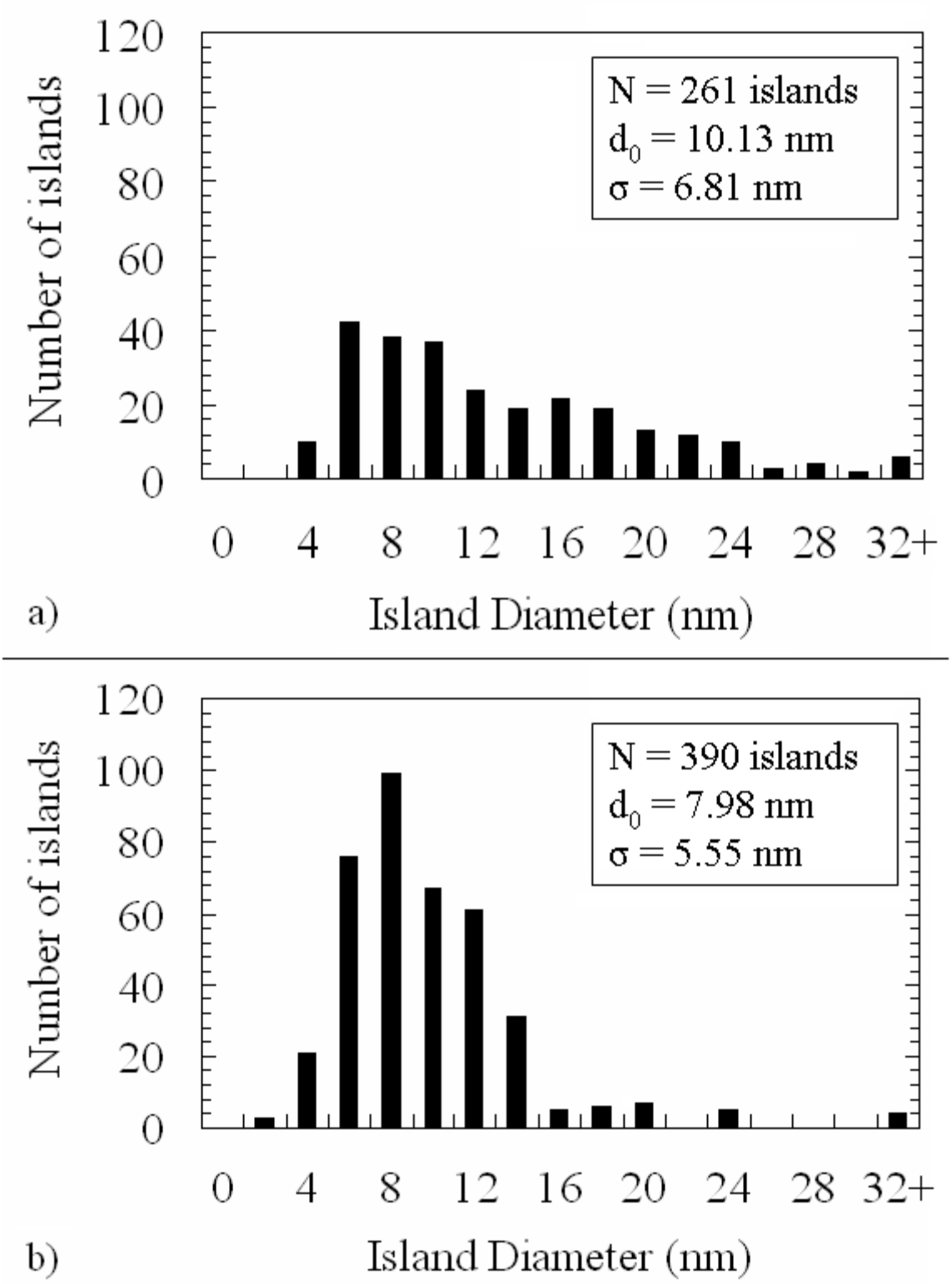

Figure 5.5: Distribution of islands sizes for round islands grown on (a) Si(100) surfaces and (b) Si(111) surfaces.

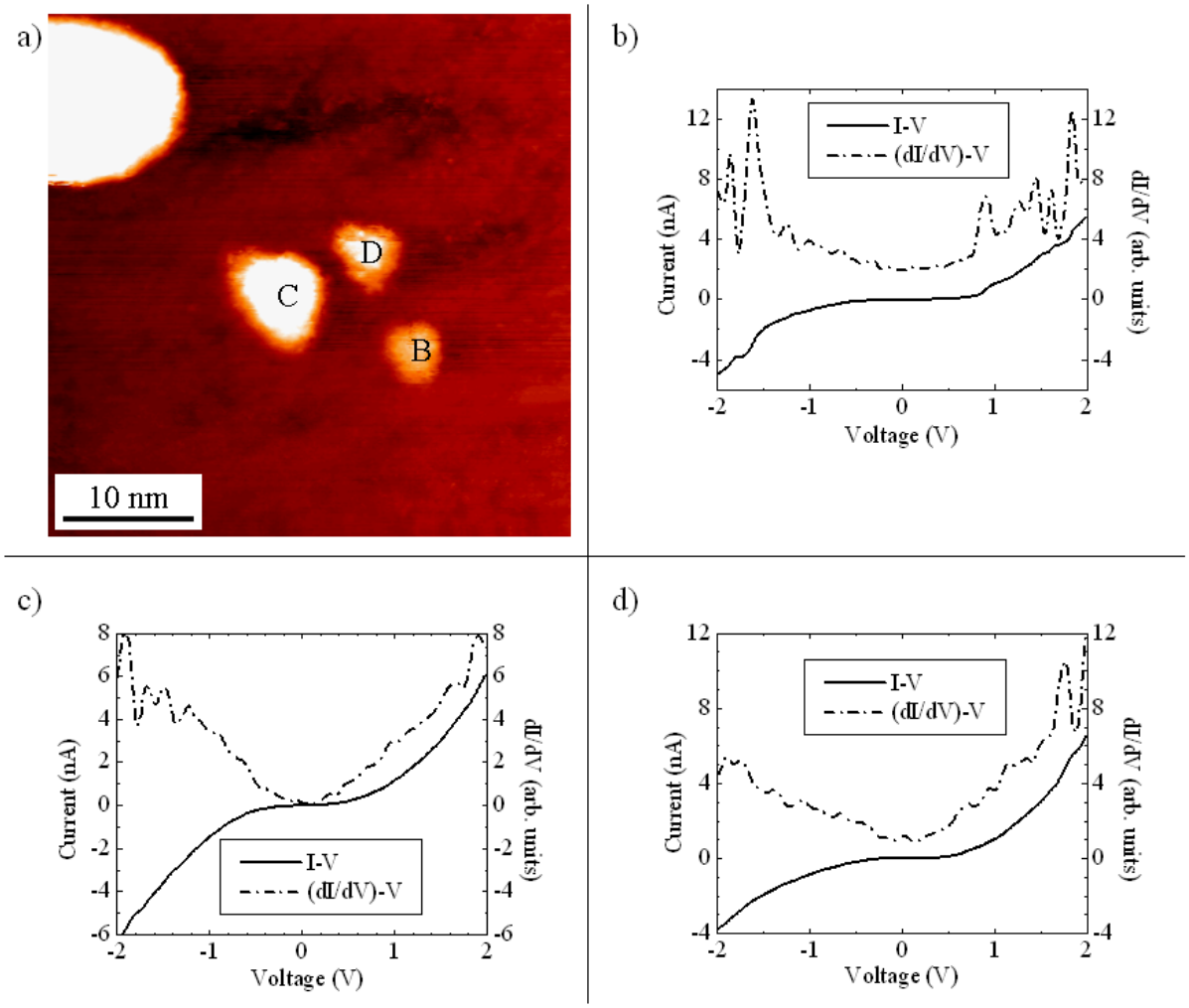

Figure 5.6: (a) STM image of $TiSi_2$ islands close together. Scan size: 40 nm. Tip bias: +1.0 V. Tunneling setpoint: 1.0 nA. The distance between islands 1 and 2 is ~2.5 nm while the distance between islands 2 and 3 is ~1.3 nm. (b) I-V and $\left(\frac{dI}{dV}\right)-V$ curves recorded from islands in (a) that do not exhibit SET.

Chapter 6:

Summary

6.1. Introduction

The design of integrated circuit devices, as stated in Chapter 1, is quickly reaching its physical limits, and new solutions need to be devised if the desire for the continued development of smaller and faster electronic devices. When these new solutions are envisioned, they will undoubtedly require either new materials or existing materials in new forms. Cobalt silicide ($CoSi_2$) and titanium silicide ($TiSi_2$) are two transition metal silicides that are used quite often in the modern semiconductor industry in integrated circuit design [1-4] and are familiar to experts in the field. As such, if the decision was made to begin investigating materials for use in the next generation of electronic device components—or the devices themselves, if they could be made small enough—$CoSi_2$ and $TiSi_2$ would most likely be among the first materials considered by industry researchers. As an additional bonus, though they are currently used in devices as blanket thin films [1-2,5], both silicides have the added functionality of being able to self-assemble into a variety of nanostructures, as has been the subject of numerous studies [6-26]. Thus, both silicides have access to the phenomena that occur at the quantum level, and would allow the semiconductor industry to take advantage of these novel features in future electronic devices. With that end as an ultimate future goal, the studies presented in this dissertation were undertaken to examine the electrical characteristics of these silicide nanostructures.

6.2. Conclusions of work concerning $CoSi_2$

Variable temperature electrical characterization was performed on $CoSi_2$ islands grown on both Si(111) and Si(100) surfaces using conducting atomic force microscopy (*c*-AFM), as was presented in Chapter 4. Though the $CoSi_2$ samples were prepared specifically for this study, the specifics of the self-assembly of the $CoSi_2$ islands were only considered when they would potentially influence the electrical characteristics of the islands. The reasoning here was that although heteroepitaxy and island formation are admittedly rich subjects, this study should maintain electrical characterization as its focus. To that end, two types of samples were grown on Si(111), air-exposed samples and clean surface samples, while only clean surface samples were grown on Si(100).

A summary of the results of the current-voltage (I-V) measurements performed on all three types of samples is presented in Table 6.1. The most evident difference between the three types of samples was in the range of room temperature barrier heights measured from each sample. The barrier heights measured on the air-exposed samples approached the range of values reported in the literature [9,21,24,27-29], while the barrier heights measured on the clean surface samples were within the range 0.30 – 0.46 eV. For the Si(111) samples, these anomalously low barrier heights suggest either a non-uniform interface [29] or a 7-fold coordinated interface [28]. Additionally, a possibility that may ultimately explain the low barrier heights of the islands on the clean surface samples is Fermi level pinning. As stated in Chapter 4, the Fermi level has been found to be pinned on clean silicon surfaces at ~0.4 – 0.55 eV depending on the condition of the surface [30-31]. If the Fermi level is pinned, this

would potentially influence the barrier height of the islands, and it would explain the 0.2 – 0.3 eV downward shift in the barrier heights of the islands on the clean surfaces.

A linear correlation between decreasing barrier height and increasing ideality factor was observed for the air-exposed samples. The ideality factor is associated with the quality of the interface [32-33], enabling a correlation to be made between a reduced barrier height and a non-ideal interface. There was no apparent correlation between barrier height and ideality factor for the other sets of samples. This suggested that the room temperature barrier heights measured on the clean surface samples were not as closely linked to the quality of the interface as the barrier heights measured from the air-exposed samples.

It was identified that there was a correlation between barrier height and island area, suggesting that there was a size-dependent effect occurring. This size-dependent effect may have been the cause of the lack of a correlation between barrier heights and ideality factors in the Si(111) and Si(100) samples. The same correlation was noted in the room temperature Si(111) samples, however it was not as pronounced. That the correlation was less pronounced suggested that the air-exposed sample barrier heights were more closely associated with the atomic structure of that interface and not as closely correlated to the electrical properties (i.e. hole injection, recombination, and field enhancement) that affected the clean surface samples. Furthermore, the apparent lack of correlation between ideality factor and island area further strengthens the argument that the cause of the barrier height lowering is not closely tied to atomic interfacial quality. It should be noted that this trend may have been due to the effects of increased spreading resistance in smaller islands.

By examining the I-V-T data for both Si(111) and Si(100) samples, it is evident that there were clear trends of decreasing barrier height and increasing ideality factor with

decreasing temperature. These trends indicated that the reasons for barrier height lowering are associated with effects that are more pronounced at low temperatures. The non-linearity in the activation energy plots, coupled with the correlation between barrier height and island area, suggests that hole injection and recombination in the depletion region are the most likely sources of barrier height lowering.

The possibility of barrier height inhomogeneity [34] as a source of barrier height lowering was also assessed. By comparing the island areas (average contact area ~10^5 nm^2) to the critical area necessary for low barrier regions to affect the measured barrier height (~10^4 nm^2), it was shown that it was possible that barrier height inhomogeneity could affect the measured barrier heights of the islands because the island areas were greater than the critical area stated above. It must be noted that islands with contact areas less than the critical area were found to still exhibit significant barrier lowering, suggesting that barrier height inhomogeneity, while it may be present in some samples, is not the dominant effect. The most likely source of the low barrier regions, if present, was thought to be regions with a locally higher electric field due to field enhancement at facets in the island interfaces.

Additionally, the dependence of island shape on the measured barrier height was examined. There was found to be no systematic difference between islands of different shapes grown on the same substrate, but there were differences between islands grown on substrates with different orientations. The lack of a difference between samples on the same substrate suggested that the epitaxial relationships between different islands are essentially the same, whereas the epitaxial relationships between islands on different substrates is understandably different.

Overall, while interfacial quality was found to play a role in the barrier height lowering, the primary mechanism behind barrier height lowering in the clean surface samples was apparently not related to the atomic quality of the interface. By utilizing I-V-T data, it was concluded that the primary reasons for barrier height lowering of the clean surface samples were most likely hole injection and recombination in the depletion region of the silicon. Barrier height inhomogeneity was considered as a possible agent of barrier height lowering due to the size of the islands, and the origin of the inhomogeneity was thought to be higher electric fields at the facets of the $CoSi_2$ islands. However, due to the presence of significant barrier lowering in the smallest islands, it was concluded that hole injection and recombination were more significant than barrier height inhomogeneity.

6.3. Conclusions of work concerning $TiSi_2$

Single electron tunneling (SET) effects have been predicted and observed in double barrier tunnel junction (DBTJ) structures. These effects are manifested as either the Coulomb blockade or the Coulomb staircase, depending on the relationship between the tunnel barriers. The outer electrodes are tunnel coupled to the center electrode and both outer electrodes are electrically isolated from the other electrode, therefore, the relationship discussed here is the relationship between the RC products of the junctions, R_1C_1 and R_2C_2. The RC product of a tunnel junction determines the rate of tunneling through the junction, and comparing the tunneling rates through both junctions indicates whether the Coulomb blockade or the Coulomb staircase will be observed.

If the tunneling rates are essentially equivalent, which typically means that the tunnel junctions are composed of the same material or are nearly quantitatively identical, then SET

will be manifested as the Coulomb blockade. In the Coulomb blockade, the charging energy of the center electrode is large enough that electrons are prevented from tunneling onto the electrode because the barrier to tunneling is too high. As an increasing amount of bias voltage is applied, the amount of energy available to the electrons increases and eventually they are able to tunnel on to the center electrode. Furthermore, since the tunneling rates are equal, once an electron tunnels off the electrode, it is immediately followed by another electron. At this point, conduction becomes ohmic and the only sign that the Coulomb blockade exists is a region of zero conductance in the I-V curve.

If the tunneling rates are significantly different, tunneling on-to and off-of the center electrode will be asymmetric. Electrons will be prevented from tunneling onto the electrode until the applied bias is high enough, however, due to asymmetric tunneling, electrons tunneling on to and off of the electrode will not occur simultaneously. Therefore, as the bias is increased, a series of plateaus will appear in the I-V curve, giving the curve the appearance of a staircase.

The $TiSi_2$ islands grown on Si(111) and Si(100) were expected to exhibit a Coulomb staircase due to the difference between the tunneling rates of the two tunnel junctions. The vacuum gap between the tip and islands has a resistance that exceeds several hundred MΩ, while the resistance of the Schottky barrier between the island and the silicon substrate is significantly less than 10 MΩ [35]. As expected, I-V curves from two $TiSi_2$ islands exhibited step-like structures in their I-V curves. These were identified as Coulomb staircases, confirming that SET effects were detected in the $TiSi_2$ islands, as was presented in Chapter 5.

A problem arose at this point because over one thousand I-V curves were measured from $TiSi_2$ islands on a variety of substrates and only two exhibited SET. When applied to

the range of I-V curves, the orthodox model of SET predicted that 290 of the islands should exhibit SET. This range was determined by counting the islands with diameters below 10 nm. Therefore, it became necessary to assess why more islands did not exhibit a Coulomb staircase. There are possibilities why more islands did not exhibit SET, and these possibilities were presented in Chapter 5. Ultimately, the analysis indicated that the most likely sources of the lack of SET effects to be Schottky barrier lowering. The former possibility was related to the reasons for Schottky barrier lowering that were presented in Chapter 4. The doping concentration of the substrate was also considered to be a possible contributing factor to the lack of SET observations due to the potentially low resistance of the substrate. Fermi level pinning by the surface states of the clean silicon surface was also considered as a possible contributing factor to the absence of SET because of the barrier height lowering that such pinning would cause.

The analysis of the SET from the $TiSi_2$ islands demonstrates that the Schottky barrier can act effectively as one of the tunneling barriers in an SET-based nanoelectronic device. Therefore, $TiSi_2$ islands could, in principle, be incorporated into SET-based electronic devices at some future date. However, the absence of SET from the vast majority of islands that were predicted to exhibit it indicates a need to determine the reason why SET was not more common. While it is evident that $TiSi_2$ islands have the potential to be effective in an SET-based device, with a success rate of less than 1%, $TiSi_2$ islands appear to be too unreliable to use in a future nanoelectronic devices. However, if it could be determined what was causing the absence of SET, it could potentially be corrected, and $TiSi_2$ islands could be used reliably as components in future electronic and nanoelectronic devices.

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Tables

Table 6.1: Summary of Schottky barrier heights and ideality factors calculated from I-V measurements on all three classes of $CoSi_2$ samples.

Growth Chamber	Substrate Orientation	Φ_B (eV)	n	T (K)	Comments
ISAGS	Si(111)	0.520 – 0.633 0.450 – 0.633	1.329 – 1.910 1.329 – 2.943	295	Linear correlation between Φ_B and n; Two outliers at $\Phi_B \sim$ 0.45 eV with n > 2
Multiprobe P	Si(111)	0.302 – 0.452	1.095 – 1.828	295	No correlation between Φ_B and n
		0.202 – 0.391	1.055 – 2.983	73 – 295	Decreasing in Φ_B with decreasing T; Increasing n with decreasing T
	Si(100)	0.390 – 0.463	1.060 – 1.402	295	No correlation between Φ_B and n
		0.183 – 0.422	1.165 – 3.502	76 – 294	Decreasing in Φ_B with decreasing T; Increasing n with decreasing T

Chapter 7:

Future Research

7.1. Introduction

The studies presented in this dissertation, while they have advanced the knowledge in the field of nanoscale electrical characterization, have left ample room for future research related to them. In fact, there are still open questions that must be answered. What follows in this chapter are directions identified for future research.

7.2. Schottky Barrier Height Measurements

To begin with, the obvious recommendation for a future direction is to simply expand the work presented in Chapter 4 to other materials. There are many other silicides which self-assemble into interesting forms and that have practical applications for which a deeper knowledge of their Schottky barrier would prove useful. However, the question of the temperature dependence of the electrical characteristics of titanium silicide (or some other silicide) is not the open question that immediately comes to mind in relation to this dissertation. Indeed, there are two questions that arise out of the work presented in this dissertation that would advance the knowledge in the field.

7.2.1. Interfacial Structure of a Nanocontact and Its Ideality Factor

As has been stated numerous times within this dissertation, the ideality factor is related to the quality of the interface [1-2]. By that logic, there should be a connection

between the interfacial structure of a nanoisland and the ideality factor of that same nanoisland. Cross-sectional transmission electron microscopy (X-TEM) images have been presented throughout the literature to relate the interfacial structure of macroscopic contacts and thin films to their ideality factors [3-10]. However, similar attempts to directly correlate the interfacial structure of a nanocontact with its ideality factor have not been as abundant and such research is necessary to provide a more conclusive link between ideality factor and interfacial structure. In fact, work in this area can begin with the subjects in this dissertation, by directly correlating the ideality factors of the $CoSi_2$ islands with their interfacial structures.

7.2.2. Impact of Surface States

Beyond the structure of the interface, another factor related to the interface is the effect that surface states have on the Schottky barrier. This specific question pertaining to nanoscale Schottky contacts was first raised about the conducting atomic force microscopy (*c*-AFM) study that preceded and inspired part of this dissertation [11]. In that study, the effect of surface states was ruled out because the smallest $TiSi_2$ islands had barrier heights that approached the value of the barrier height for bulk $TiSi_2$.

This current study has the advantage of the ability to vary the sample temperature, whereas the previous study was performed at room temperature only. Variable temperature measurements are important in sorting out the true barrier height mechanisms. Furthermore, in light of the data presented in Chapter 4 that suggests possible effects due to surface states, it is important to learn what the full effects of these surface states are.

Passivation studies have been performed concerning the electrical characteristics of several metal-semiconductor (MS) systems [12-20]. These studies have found a variety of effects present due to the passivation layer. These effects range from significant changes in barrier height [14,18] to mixed-phase interfaces [13] to changes in the metal-semiconductor interaction [15,19] to the formation of a surface dipole [20]. One study even found that the Schottky barrier was only weakly affected by the passivation [17]. However, these studies have been performed using large area Schottky contacts. Any study undertaken to investigate the effect of surface states in nanoscale Schottky contacts, such as the $CoSi_2$ and $TiSi_2$ islands in this dissertation, will advance the level of understanding about the full effects of surface states.

7.3. Single Electron Tunneling Measurements

The SET presented in Chapter 5 is most notable, perhaps, for its scant nature. The reasons for the lack of SET signatures from the $TiSi_2$ nanoislands are described in Chapter 5, and the primary open questions left from that study revolve around the absence of SET.

7.3.1. Effect of Doping Concentration on SET

As mentioned in Chapter 5, the doping concentration of the substrates used was 10^{17} cm^{-3}. These substrates could have had a lower resistance than was expected, especially given the possibility of interfacial faceting. While preliminary measurements were performed on 58 islands that were grown on silicon with $N_A \sim 10^{15}$ cm^{-3}, none of those islands exhibited SET. Furthermore, the number of total nanoislands measured was significantly less than in the study presented in Chapter 5 (58 nanoislands compared to 651 nanoislands in the Chapter 5 study). Therefore, it would be interesting to perform a proper study of the dependence of

SET on the doping concentration of the silicon substrates. Such a study would have the added benefit of establishing the necessary substrate parameters for future SET studies.

7.3.2. Interfacial Effects on SET

As stated in Chapter 5, the effects of the interface between the silicide nanoislands and the silicon substrate must be considered when investigating SET in these nanoislands. The primary concerns about the interface that were raised in Chapter 5 are the effects of interfacial faceting on SET and the possibility of Schottky barrier lowering and its effect on SET. AFM and X-TEM will allow for a study of the shape of the interface and the amount of faceting. By determining the amount of faceting, modeling can be performed to determine an estimate of the electric field at any facets that are present and how those elevated electric fields affect current transport across the interface.

The possibility that the Fermi level pinning of the clean silicon surface by surface states was also proposed as a means of barrier lowering in both Chapters 4 and 5. Passivation studies have been proposed in Section 7.2.2 to investigate the effect that surface states have on the Schottky barrier height. However, such studies could also be applied to SET measurements. If small islands were grown on passivated surfaces, the effects of Fermi level pinning, and subsequent pinning on the barrier height, would be eliminated. Passivation studies should be undertaken to assess the full effects that the surface states have on SET.

A conflict between the tunneling time and the increases in current between tunneling events (represented by $R_T > R_I$ while $C_T < C_I$, as defined in Chapter 5) and how it possibly affects SET in the STM tip-metal island-semiconductor system must be assessed [21]. If this conflict is occurring, the Coulomb staircase will be suppressed, however, the Coulomb

blockade will still be visible. At lower temperatures, the thermal noise will be reduced, and that should enable a more accurate determination of whether or not an I-V curve contains the signature of the Coulomb blockade. By measuring I-V curves from nanoislands across a range of temperatures and comparing those curves to I-V curves recorded from the bare silicon surface, it should be possible to confirm if the portions of the I-V curves that exhibit zero conductance are due to the Coulomb blockade. If the Coulomb blockade is indeed occurring, that would confirm that the conflict between tunneling times and current increases is taking place. A previous study found that the addition of an epitaxial intrinsic silicon interlayer prior to titanium deposition and $TiSi_2$ island formation led to more pronounced SET measurements [22]. The use of such an interlayer, combined with X-TEM, could allow for further testing of the conflict.

7.3.3. Temperature Dependence of SET

One of the original intentions of the SET study presented in Chapter 5 was to investigate the temperature dependence of SET in the $TiSi_2$ nanoislands. There is little explicit temperature dependence in the orthodox theory of SET [23-26] aside from the requirement that the charging energy of the nanoisland exceed the energy of ambient thermal fluctuations, kT. However, in addition to the SET being more easily accessible at low temperature, the steps in the Coulomb staircase should appear to become sharper as the temperature decreases. Therefore, it is reasonable to study the temperature dependence of the SET through the nanoislands and watch the shape of the I-V curves as the temperature changes. Not only would the presence of SET across a range of temperature confirm that the SET is genuine, it would also allow for a study of how the discrepancies between SET in MS

systems and the predictions of the orthodox model change with temperature. By studying the discrepancies with the orthodox model across a range of temperatures, it will enable a fuller understanding of the SET process within the MS double barrier tunnel junction, and any corrections that must be taken into account due to the presence of the Schottky barrier. It must be noted that this study would most likely be made simpler once the interfacial effects on SET (see Section 7.3.2) are resolved.

7.4. Linear Transport Properties of Nanowires

When considering electrical characterization of nanostructures, it is important to consider their form and function. Nanoislands can range from zero-dimensional quantum dots to three-dimensional islands, however, this refers to the size of the nanoislands relative to the size of the charge carrier. The nomenclature has no direct bearing on how the island would be used in a nanodevice. For the most part, islands tend to be thought of vertically, that is, current will pass between two electrodes and go directly through the island. Nanowires, on the other hand, while they may range from one-dimensional to three-dimensional wires, however, they have the added flexibility of being able to conduct charge carriers laterally. Therefore, they can be used as interconnects between electrodes spaced at distances much greater than the diameter of a single island.

In order to take advantage of the lateral transport properties of nanowires, they must be fully understood. Characterization of the electrical properties of single nanowires revolves around two different categories of measurements: two-terminal measurements and four-terminal measurements. There are three basic methods used to make these measurements. It is possible to use multiple moveable contacts, such as a multi-tip SPM, to make contact to

different parts of a single nanowire [27]. This allows the possibility of making four-terminal measurement if four probes are available. Alternately, multiple contact pads could be deposited to allow for four-terminal or two-terminal measurements [28-31]. A third method is to evaporate a single contact pad, using gold or platinum, on top of an array of nanowires and then use an AFM cantilever to make contact with a single nanowire that is in contact with the metal pad [32]. The third method allows for two-terminal measurements, but four-terminal measurements are nearly impossible.

The procedure that could be utilized in the Multiprobe P, given the configuration discussed in Chapter 3, is the third method. An array of nanowires could be grown and a platinum contact pad could be deposited and the second motorized probe used to make contact with the pad. An AFM cantilever would then provide the second contact that would allow two-terminal lateral transport measurements to be made. A schematic of this method is shown in Figure 7.1. There are two research areas related to lateral transport that are intriguing that would be possible using this approach: conductance quantization and size-dependent electrical characteristics.

7.4.1. Conductance Quantization

There are three conductance regimes that apply to lateral transport through nanowires, depending on the width of the nanowire: the macroscopic regime, the mesoscopic regime, and the nanoscopic regime. In the macroscopic regime, the dimensions of the nanowire are significantly greater than the mean free path of the electron. As a result, current transport is diffusive [33] and background scattering mechanisms dominate conduction. In the mesoscopic regime, the nanowire dimensions are on the order of the mean free path of

electron, and scattering from the nanowire surfaces becomes the dominant scattering process [34-35].

While the physics in the macroscopic and mesoscopic regimes are rich, once the nanowire dimensions are on the order of the Fermi wavelength of the electron in the material and the nanowire length is less than the mean free path, the nanowire is operating in the nanoscopic regime. In this regime, the electron is confined along the short axes and the nanowire is essentially one-dimensional, making current transport ballistic [33]. Once in this regime, conductance is quantized in steps of $G_0 = 2ne^2/h$ (for non-magnetic nanowires), where n refers to the number of available conduction channels [36], which are discrete sub-bands in the one-dimensional density of states [37-38].

Conductance quantization is the one-dimensional analog of SET because with quantized conductance, the current will increase in regular steps as the bias is increased, and the I-V curve will be shaped like a staircase. The difficulty in obtaining conductance quantization is growing a nanowire with a width less than the Fermi wavelength of the electron within it. This is difficult with metals, because the Fermi wavelength of electrons in the metal is typically below 1.0 nm and most nanowires are wider than 1.0 nm. However, it is possible, at least in principle. $DySi_2$ has a Fermi wavelength calculated to be 0.84 nm, while the narrowest $DySi_2$ wire that has been measured was 0.77 nm [39].

7.4.2. Size Dependence of Nanowire Electrical Characteristics

As stated above, there are three regimes for current transport in nanowires. In general terms, in the macroscopic regime, the resistivity, ρ, is proportional to the inverse of the relaxation time, τ^{-1}. In the mesoscopic and nanoscopic regimes, the resistivity increases as the

nanowire width decreases [32,40-41]. These simple definitions do not address how the resistivity of the nanowire is related to the corresponding thin film resistivity.

Several studies have been performed on different species of silicide nanowires and have measured the resistivities and resistances of the nanowires [27-32,42-46]. The studies have found that the resistivities of the nanowires do not have a universal relationship to the corresponding thin film resistivities. The studies have found nanowires where $\rho_{wire} \gg \rho_{film}$ [32,42-43], $\rho_{wire} > \rho_{film}$ [27,29-31], $\rho_{wire} \approx \rho_{film}$ [28,44,46], and $\rho_{wire} < \rho_{film}$ [45]. It is an open question if there are different regimes of size that lead to these different relationships between the nanowire resistivities and the thin film resistivities. Furthermore, if there are not different size regimes, then what is the cause of the widely varying relationships? Research performed to answer these questions will undoubtedly prove valuable to the field of nanowire electrical characterization.

7.5. Conclusion

As shown in the preceding sections, there are a number of directions in which future researchers can proceed using this dissertation as a starting point. The primary advantage to these possible research areas is their versatility. The research can be performed using several different materials systems. For instance, temperature dependent Schottky barrier measurements can be performed on any combination of metal islands and semiconductor surfaces. Furthermore, the necessity of correlating barrier height and ideality factor to the interfacial structure of a nanocontact is a question that extends to these other materials systems. SET can likewise be studied on any system where nanoscale islands can be formed, either through self-assembly or lithography. If the conflict discussed in Chapter 5 and Section

3.1 of this chapter is found to be true for $TiSi_2$ nanoislands, it would be of interest to extend the research to other materials system to determine if there is an STM tip-metal island-semiconductor system that does not suffer from that conflict. Additionally, a study of the interfacial structure and its relation to SET would be of interest regardless of the materials system involved. The same statement can be extended to nanowires, as well. Nanowires form from several different types of silicides, and silicon nanowires [47] and molecular wires [48-50] also exist. Conductance quantization and size dependence studies could be undertaken on these other nanowires as well. In fact, the non-metal nanowires could prove quite interesting as they would be influenced by different physical phenomena (for example, the highest occupied molecular orbital-lowest unoccupied molecular orbital (HOMO-LUMO) gap in molecular wires). Ultimately, regardless of the particular materials system chosen, the research proposed in this chapter can be applied to enhance the knowledge in the field of nanophysics. Furthermore, if these avenues of research are pursued, it would enable a full characterization of the nanostructures that might be used as the components and interconnects in future nanoelectronic devices.

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Figures

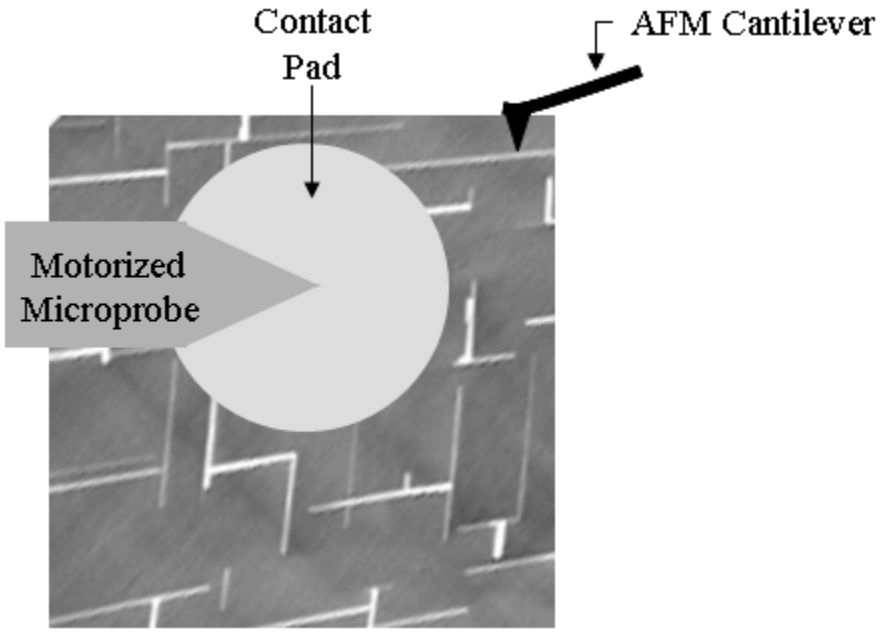

Figure 7.1: Schematic for performing lateral transport measurements of nanowires using the Multiprobe P. In this example, the contact pad is platinum and is deposited directly on top of the nanowire array. Any conductive AFM cantilever may be used.