



US006861330B2

(12) **United States Patent**
Basceri et al.

(10) **Patent No.:** US 6,861,330 B2
(45) **Date of Patent:** Mar. 1, 2005

(54) **STRUCTURES AND METHODS FOR ENHANCING CAPACITORS IN INTEGRATED CIRCUITS**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/232,217**

(22) Filed: **Aug. 29, 2002**

(65) **Prior Publication Data**

US 2003/0001187 A1 Jan. 2, 2003

Related U.S. Application Data

(62) Division of application No. 09/533,433, filed on Mar. 23, 2000, now Pat. No. 6,476,432.

(51) **Int. Cl.⁷** **H01L 21/20**

(52) **U.S. Cl.** **438/387; 438/396; 257/303; 257/306**

(58) **Field of Search** **438/244, 253, 438/256, 387, 396, 696, 700, 702, 703, 763; 257/301, 303, 304, 306**

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(57) **ABSTRACT**

Systems, devices, structures, and methods are described that inhibit dielectric degradation in the presence of contaminants. An enhanced capacitor in a dynamic random access memory cell is discussed. The enhanced capacitor includes a first electrode, a dielectric coupled to the first electrode, a second electrode coupled to the dielectric, and at least one inhibiting layer that couples to the first electrode, the dielectric, and the second electrode. The inhibiting layer defines a chamber that encloses the capacitor and renders the capacitor impervious to disturbance in its physical or chemical forces in the presence of contaminants. The inhibiting layer includes a nitride compound, an oxynitride compound, and an oxide compound. In one embodiment, the nitride compound includes Si_xN_y . In another embodiment, the oxynitride compound includes SiO_xN_y . In another embodiment, the oxide compound includes Al_2O_3 and $(\text{SrRu})\text{O}_3$. The variables x and y are indicative of a desired number of atoms. The dielectric includes an oxide compound. In one embodiment, the oxide compound includes barium strontium titanate.

30 Claims, 16 Drawing Sheets

