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(54) **METHOD OF FORMING A LAYER COMPRISING EPITAXIAL SILICON AND A FIELD EFFECT TRANSISTOR**

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See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,758,531	A	7/1988	Beyer et al.	
5,250,837	A	10/1993	Sparks	
5,753,555	A	5/1998	Hada	
5,763,305	A	6/1998	Chao	
6,060,746	A	5/2000	Bertin et al.	
6,064,081	A	5/2000	Robinson et al.	
6,437,375	B1	8/2002	Beaman	
6,448,129	B1	9/2002	Cho et al.	
6,518,609	B1	2/2003	Ramesh	
6,617,226	B1	9/2003	Surguro et al.	
6,624,032	B1	9/2003	Alavi et al.	
6,642,539	B1	11/2003	Ramesh et al.	
6,703,290	B1	3/2004	Boydston et al.	
6,713,378	B1	3/2004	Drynan	
6,716,687	B1	4/2004	Wang et al.	
6,716,719	B1	4/2004	Clampitt et al.	
6,746,923	B1	6/2004	Skotnicki et al.	
6,878,592	B1 *	4/2005	Besser et al.	438/285
6,885,069	B1 *	4/2005	Ohguro	257/369
2001/0010962	A1	8/2001	Chen et al.	
2001/0017392	A1	8/2001	Comfort et al.	
2001/0025985	A1	10/2001	Noble	
2002/0081861	A1	6/2002	Robinson et al.	
2003/0027406	A1 *	2/2003	Malone	438/471
2003/0153155	A1	8/2003	Wang et al.	
2003/0211712	A1 *	11/2003	Chen et al.	438/481
2004/0241460	A1	12/2004	Bodell et al.	

OTHER PUBLICATIONS

U.S. Appl. No. 11/035,298, filed Jan. 12, 2005, Blomiley et al.
Bashir et al., *Characterization and modeling of sidewall defects in selective epitaxial growth of silicon*, J. Vac. Sci. Technol. B 13(3), pp. 928-935 (May/Jun. 1995).
U.S. Appl. No. 10/932,151, filed Sep. 1, 2004, Ramaswamy et al.
U.S. Appl. No. 10/931,924, filed Sep. 1, 2004, Ramaswamy et al.

* cited by examiner

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(57) **ABSTRACT**

This invention includes methods of forming layers comprising epitaxial silicon, and field effect transistors. In one implementation, a method of forming a layer comprising epitaxial silicon comprises epitaxially growing a silicon-comprising layer from an exposed monocrystalline material. The epitaxially grown silicon comprises at least one of carbon, germanium, and oxygen present at a total concentration of no greater than 1 atomic percent. In one implementation, the layer comprises a silicon germanium alloy comprising at least 1 atomic percent germanium, and further comprises at least one of carbon and oxygen at a total concentration of no greater than 1 atomic percent. Other aspects and implementations are contemplated.

91 Claims, 2 Drawing Sheets