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[54] **INTEGRATED CIRCUITS HAVING COOPERATIVE RING OSCILLATOR CLOCK CIRCUITS THEREIN TO MINIMIZE CLOCK SKEW**

[75] Inventors: **Lester Crossman Hall; S Mark Clements**, both of Raleigh; **Wentai Liu, Cary; Griff L. Bilbro**, Raleigh, all of N.C.

[73] Assignee: **North Carolina State University**, Raleigh, N.C.

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Related U.S. Application Data

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[52] **U.S. Cl.** **331/56**; 327/294; 327/565; 331/45; 331/57; 331/74

[58] **Field of Search** 331/45, 46, 56, 331/57, 74; 327/294, 295, 565

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Primary Examiner—Siegfried H. Grimm
Attorney, Agent, or Firm—Myers Bigel Sibley & Sajovec

[57] **ABSTRACT**

Integrated circuits having cooperative ring oscillator clock circuits therein include a plurality of synchronous and asynchronous active devices on the substrate and a plurality of “cooperative” ring oscillators (CRO) electrically coupled in parallel at respective clock nodes, interspersed on the substrate as a mesh, for example. The ring oscillators, which may have a predetermined number of stages but possibly different size in terms of clock driving capability, are preferably interspersed among the synchronous active devices on the surface of the substrate to provide a “local” clock signal which is constrained in terms of skew and jitter by the presence of the other parallel-connected ring oscillators at other locations on the substrate. Multiple replications of a ring-oscillator containing three serially connected inverters may result in the formation of a two-dimensional hexagonal network of clock nodes of different phases (e.g., ϕ_1 , ϕ_2 and ϕ_3). Connection of the inverters as a hexagonal network also causes “aggregation” because the arrangement of the inverters in the net places the inverters in parallel. Whenever inverters are connected in parallel, an “aggregated” inverter is formed having an effective width equal to the arithmetic sum of the widths of the all the individual inverters of the same phase. This “aggregation” compensates for process variations because the “faster” and “slower” inverters tend to cancel each other out during signal transitions. The benefits of aggregation are also independent of the size of the IC so efficient scaling can be readily achieved. Ring oscillators of larger size (e.g., widths) can also be placed in close proximity to those portions of the circuit which have high load synchronous active devices therein, to inhibit local variations in skew and jitter.

13 Claims, 4 Drawing Sheets

