

ABSTRACT

GOVINDARAJ, ARVIND. Design and Characterization of Various Circuit Topologies for Battery/Ultracapacitor Hybrid Energy Storage Systems. (Under the direction of Dr. Srdjan M. Lukic).

There is a good possibility that plug-in hybrid and fully electric vehicles will have an increasing role in the future. One of the key limiting factors in the performance of such vehicles is the performance of the energy source. A single battery technology which can meet the complete range of requirements (high instantaneous power and high energy density) is ideal; but such an ideal battery does not exist yet.

A hybrid power pack consisting of batteries and ultracapacitors has the advantage of combining high energy capability (batteries) with high power capability (ultracapacitor). The objective of this thesis is to design and characterize topologies for effectively combining batteries (focused on Li-Ion technology) and ultracapacitors. Existing circuit topologies have been characterized; new variants and a new topology have been proposed.

Hybrid Energy Storage System (HESS) topologies have been classified as passive and active types. Performance of passive HESS topologies (direct paralleling and paralleling with an inductance) have been characterized. Active HESS topologies; primarily the classic buck-boost converter and variants (Battery Facing Load and Ultracapacitor Facing Load) are analyzed and a design method is presented. A novel contribution of this work has been defining clearly the 2 major variants of this converter and discussing their merits and demerits. An interleaved version of the buck-boost converter is proposed. An experimental platform was constructed to verify performance of these topologies.

A new topology which attempts to improve performance over the existing topologies and makes efficient use of the ultracapacitor in the HESS has been presented. The design of a new battery management system which was required for HESS experiments and research on battery modeling has also been presented in this thesis.

Design and Characterization of Various Circuit Topologies for
Battery/Ultracapacitor Hybrid Energy Storage Systems

by
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A thesis submitted to the Graduate Faculty of
North Carolina State University
in partial fulfillment of the
requirements for the Degree of
Master of Science

Electrical Engineering

Raleigh, North Carolina

2010

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BIOGRAPHY

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ACKNOWLEDGMENTS

To my advisor Dr. Srdjan M. Lukic for giving me direction in my research work, the many hours spent in discussions, for the critical reviews and above all for providing an ideal environment for learning and conducting research.

I would also like to express my gratitude to my committee members Dr. Subhashish Bhattacharya who was responsible for creating a good understanding of power electronics through his courses and for motivating creativity and Dr. Mo-yuen Chow for demonstrating rigorousness in research and for the many discussions on batteries. Many thanks to Dr. Alex Huang, Director of the FREEDM Systems Center.

To my parents for their love and support all through my life. To my grandpa and grandma for all their teachings and affection.

To my friends for the engaging discussions, all the help and the fun times that I will cherish in my memory for ever, my special thanks to Siddharth Ballal, Edward VanBrunt, Shashank Bodhankar, Shane Hutchinson, Zeljko Pantic, Katarina Pantic, Hesam Mirzaee, Mathew King, Arun Kadavelugu, Misha Kumar, Urvir Singh, Daniel, Shanzhong Bai and Hoosein Hooshyar. To my childhood friends Ashwin Kumar and Vinay Shivakumar; I would be lost without your friendship.

To my wife Sangeetha for all the love, encouragement and sacrifices. This degree would not have been possible without you.

Many thanks to all those who made this possible.

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1

Introduction

1.1 Perspective

Ever since the industrial revolution, mankind's consumption of energy has increased dramatically. Fossil fuels provided a ready solution to the burgeoning energy demand and continue to do so; producing nearly 85% (Oil: 37%, Coal: 25%, Gas 23%) [1] of the world's total energy supply. In the U.S., transportation accounts for nearly 2/3 of the total oil consumption [2]- about 40 million barrels a day! However burning of fossil fuels has several detrimental impacts on the environment; important among those is the release of green house gases into the atmosphere which have been attributed to global warming and climate change [3]. This has led to a strong drive to decrease the carbon footprint (the total set of greenhouse gas (GHG) emissions caused by an organization, event or product) and to create more efficient vehicles. Several solutions have been proposed to achieve these goals; some of the significant methods [4] are listed below:

- Using alternate fuels (BioDiesel, Ethanol, Propane, Natural gas) in modified internal combustion engines.
- Using electricity to completely power or assist vehicle propulsion (using electric motors) - this includes hybrid, fully electric and plug-in hybrid electric vehicles. The energy is stored on board the vehicle using batteries.
- Using hydrogen powered vehicles - hydrogen fuel cell is used to produce electricity which drives the vehicle's electric motor.

The recent past has seen a surge in interest in Plug-In Hybrid Electric Vehicles (PHEV) and fully Electric Vehicles (EV) [5, 6]. These technologies enable the possibility of utilizing renewable energy and other clean energy sources thereby decreasing the carbon footprint. Studies conducted by Electric Power Research Institute (EPRI), National Renewable Energy Laboratory (NREL) and MIT Sloan Automotive Laboratory on the environmental impact of PHEVs are shown in Table 1.1 (reproduced from [7]). The EPRI study compares the CO_2 emissions of traditional ICE with hybrids and PHEVs (driven 20 miles a day) and powered by electricity from various sources (old and new coal plants, Nuclear plants and renewable sources) and the reduction in emissions are evident. The NREL study presents similar information; the emissions when the PHEVs are charged during off-peak hours (of the electricity grid) and when they are continuously charged is presented. The MIT study presents information on a 30 mile/day PHEV cycle and an all-electric vehicle. Although there are variations in the predicted numbers, all the above mentioned studies show the same trend.

Table 1.1: Estimated CO_2 emissions in grams/mile for ICE, PHEV and EV

Electric Power Research Institute [8]					
ICE-only	Hybrid	PHEV20	PHEV20	PHEV20	PHEV20
		2010 Coal	2035 Coal	Nuclear	Renewables
450 g	295 g	325 g	305 g	150 g	150 g
National Renewable Energy Laboratory [9]					
ICE-only	Hybrid	PHEV20	Off-peak charging	PHEV20	Continuous charging
410 g	299 g		247 g		221 g
MIT Sloan Automotive Laboratory [10]					
ICE-only	Hybrid	PHEV30		Electric-only	
477 g	140 g	138 g		185 g	
Note: ICE emissions correspond to the average of 2007 U.S. vehicles					

These benefits combined with the drive to reduce dependence on oil, has led to the increased research focus in PHEV and EV technology. The energy storage systems (batteries) used in PHEV's and EV's are an important factor to ensure their successful adoption. The focus

of this work is on improving the energy storage systems (ESS) to make them more efficient and improve their lifetime.

1.2 Why a Hybrid Energy Storage System ?

1.2.1 Power Profile of an Electric Vehicle

A power profile of an electrically powered vehicle is required to understand the demands on the energy storage system. A simple model of a vehicle as described in [11] is used to determine the forces acting on the vehicle and to estimate the power required to overcome the opposing forces and provide the acceleration the driver demands. The forces modeled are described in Table 1.2. The vehicle is simulated using the Urban Dynamometer

Table 1.2: Forces Modeled

Force	Equation	Terms
Acceleration	$M_v a^2$	M_v - Vehicle mass, a - Acceleration
Rolling Resistance	$M_v g f_r$	g - Standard Gravity, f_r - Rolling Resistance Coeff
Air Resistance	$\frac{1}{2} \rho A_f C_D V^2$	ρ - Air Density, A_f - Frontal area, C_D - Drag Coeff

Driving Schedule (UDDS)[12], which is representative of the city drive cycle we want to optimize the energy storage system for. The parameters used for the model vehicle are $M_v = 1756kg$, $A_f = 1.88m^2$, $C_D = 0.4$, $f_r = 0.02$; fitted with a 56.25 kW motor and a gear system. The energy source is a 300V battery pack. The power profile obtained by simulation is shown in Fig. 1.1, the negative power indicates regenerative energy.

1.2.2 Inferences from the Power Profile

It can be observed that the power profile contains many peaks (which correspond to acceleration and deceleration); the average power is much lower than the peak power. Due to the nature of the application (traction) and driving requirements, the ESS needs to be capable of providing high power pulses to the vehicle (accelerating) as well as sustained power over longer intervals (cruising). In addition the power source also needs to be capable of the accepting high power pulses regenerated from the vehicle (braking). This high peak-

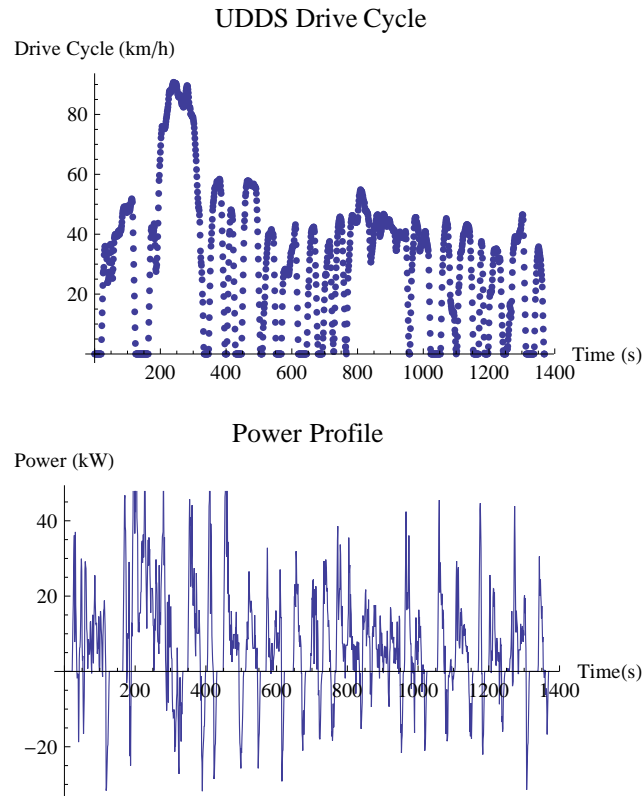


Figure 1.1: Graph showing UDDS and Power Profile of the Vehicle Model

to-average power ratio creates several implementation issues because the ESS has to be dimensioned to be able to provide peak power as well as store enough energy to provide driving range. While a single battery technology which can meet the complete range of requirements (instantaneous power and energy) is ideal, such an ideal battery does not exist. Hence there has been considerable research effort into combining batteries with other power sources to improve performance. Ultracapacitors are often considered for use in such hybrid power systems because of their high instantaneous power delivery capability which complement the high energy storage capabilities of the batteries. The Ragone plot in Fig 1.2 (Delphi Automotive Systems, DOE workshop, 2001) shows the energy/power capabilities of different sources and it can be seen that there is scope to combine high energy Li-Ion's with high power ultracapacitors. The characteristics of 3 energy sources used in this work are superimposed on Fig 1.2; 1. High Power Li-Ion (A123, 28650) - Yellow dot, 2. High

Energy Li-Ion (Kokam, LiPo) - Green dot and 3. Ultracapacitor (Maxwell, BCAP 350) - Blue dot. It can be observed that current battery and UC technology match the projections of the Ragone plot.

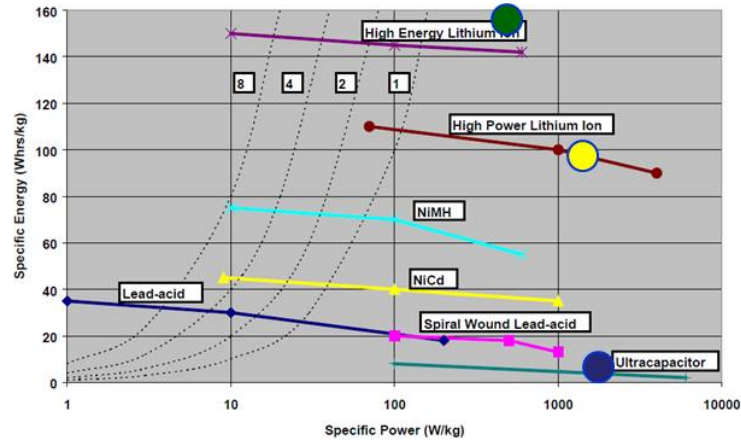


Figure 1.2: Ragone Plot showing Energy/Power Capabilities of Batteries and UCs

1.2.3 System Level Simulations

Several system level simulations have been performed and strengthen the notion that hybrid energy storage solutions incorporating batteries and ultracapacitors (UC) could potentially lead to extended range and increased lifetime.

In [13], the performance of hybrid energy storage (Lithium battery and UC) is analyzed for PHEV applications. A storage system combining batteries and UCs (with a DC/DC converter) is simulated over various driving cycles (FUDDS, Fed Highway, US06). It has been shown that there is an increase in fuel economy and decreased stress on the battery. Further, UCs allow the use of batteries with a wide range of power characteristics.

In [14], the authors have built an hybrid battery pack (lead-acid and UCs) for an electric vehicle. It has been measured from drive tests that the effective driving range of the vehicle improved when the hybrid system was used.

1.3 Review of Current Battery Technology

Several battery chemistries have been developed over the years, with each type having varied performance characteristics. The target for battery packs (shown in Table 1.3, reproduced from [15]) to be used in PHEV's have been defined by several bodies, including USABC, MIT and EPRI. These target values are used to find the best battery chemistry to meet these requirements (also applicable to EV energy sources).

Table 1.3: Battery Pack Requirements for PHEV performance goals

		USABC		MIT	EPRI	
	Units	AE-10	AE-40	B-30	AE-20	AE-60
Power						
Peak power	kW	50	46	44	54	99
Peak power density	W/kg	833	383	733	340	328
Energy						
Total energy capacity	kWh	5.6	17.0	8.0	5.8	17.9
Total energy density	Wh/kg	93	142	133	37	59
Life						
Calendar life	years	15	15	15	10	10
CD cycle life	cycles	5,000	5,000	2,500	2,400	1,400
CS cycle life	cycles	300,000	300,000	175,000	200,000	200,000
Cost						
OEM priced	\$	\$1,700	\$3,400	\$2,560	-	-
OEM price/total kWh	\$/kWh	\$300	\$200	\$320	-	-

AE - All Electric, B - Blended

The major contenders for this application are Nickel-Metal hydride (NiMH) batteries (which are used in most of the current HEV's) and Lithium-Ion (Li-Ion) batteries. It has been shown in [16] that Li-Ion appears to be the only technology capable of meeting the goals. Hence a lithium secondary cell is considered the most likely candidate for this class of applications.

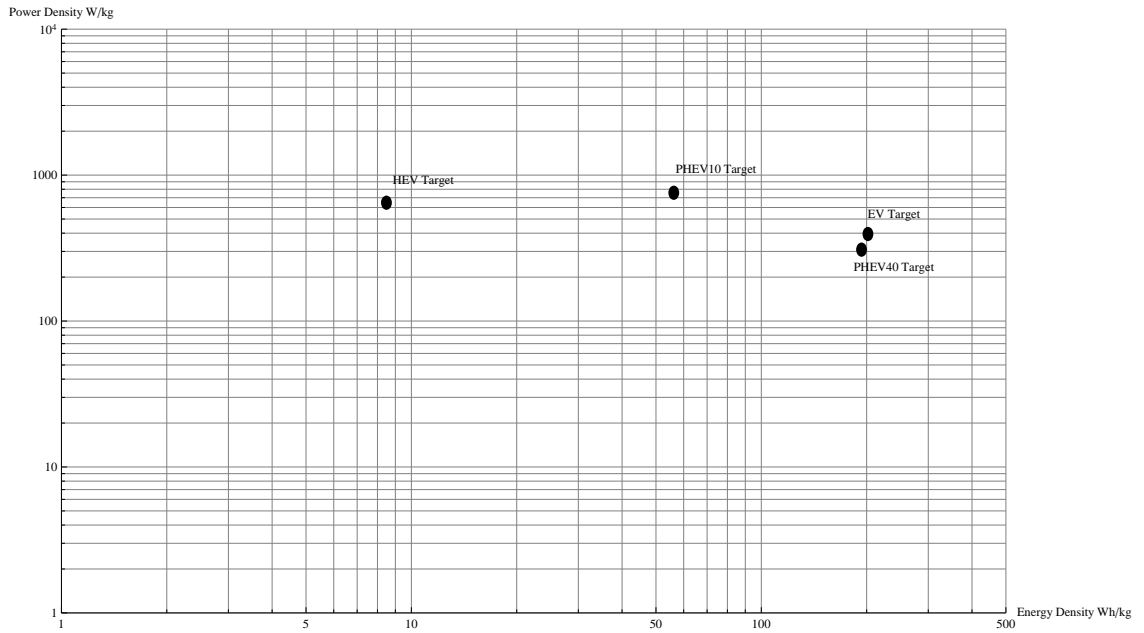


Figure 1.3: Ragone Plot Showing USABC Battery Targets

1.3.1 Li-Ion Technology

Lithium is the lightest metal and has a high standard electrode potential, which gives Li a theoretical specific capacity of 3860 Ah/kg compared with 820 Ah/kg for zinc and 260 Ah/kg for lead [17]. The main elements of a Li-Ion cell are the anode, cathode and the electrolyte. During charging, the lithium is extracted from the cathode and inserted into the anode and the reverse happens during the discharging process. The primary performance indicators of a Li-Ion battery are:

- Energy Density
- Power Density
- Life Time
- Cost
- Safety

Table 1.4: Performance Indicators of current Li-Ion chemistries

Name	Description	Electrodes: Positive (Negative)	Power	Energy	Safety	Life	Cost
LCO	Lithium cobalt oxide	LiCoO ₂ (Graphite)	Good	Good	Low	Low	Poor
NCA	Lithium nickel, cobalt and aluminum	Li(Ni _{0.85} Co _{0.1} Al _{0.05})O ₂ (Graphite)	Good	Good	Mod	Good	Mod
LFP	Lithium iron phosphate	LiFePO ₄ (Graphite)	Good	Mod	Mod	Good	Mod
NCM	Lithium nickel, cobalt and manganese	Li(Ni _{1/3} Co _{1/3} Mn _{1/3})O ₂ (Graphite)	Mod	Mod	Mod	Poor	Mod
LMS	Lithium manganese spinel	LiMnO ₂ or LiMn ₂ O ₄ (Li ₄ Ti ₅ O ₁₂)	Mod	Poor	Excel	Excel	Mod
LTO	Lithium titanium	LiMnO ₂ (LiTiO ₂)	Poor	Poor	Good	Good	Poor
MNS	Manganese titanium	LiMn _{1.5} Ni _{0.5} O ₄ (Li ₄ Ti ₅ O ₁₂)	Good	Mod	Excel		Mod
MN	Manganese titanium	Li _{1.2} Mn _{0.6} Ni _{0.2} O ₂ (Graphite)	Excel	Excel	Excel		Mod

The performance of the Li-Ion batteries depend on the choice of materials for the anode and cathode. An overview of current Li-Ion chemistries which are being considered for PHEV/EV applications is shown in Table 1.4 (reproduced from [16]); the interplay between the performance indicators is evident. Typical Li-Ion batteries used for this class of application (automotive), are projected to have energy densities in the range of 200-300 Wh/kg [13].

1.3.2 Issues with Li-Ion Technology

Peukert's Law: Batteries exhibit a reduction in usable capacity when discharged at higher rates. This effect was first modeled by W.Peukert, using a simple equation $C_p = I^k t$, where C_p is the capacity of the battery, I is the discharge current, k is the Peukert constant and t is time. Though it has been shown in [18] that using the Peukert's equation results in a error in estimation capacity, the effect is still observed. This effect becomes important to PHEV/EV applications because the batteries are cycled at high discharge rates. The discharge curves of a Kokam, 7.5Ah Li-Ion battery is shown in Fig.1.4 - the loss in capacity at high discharge rates can be observed.

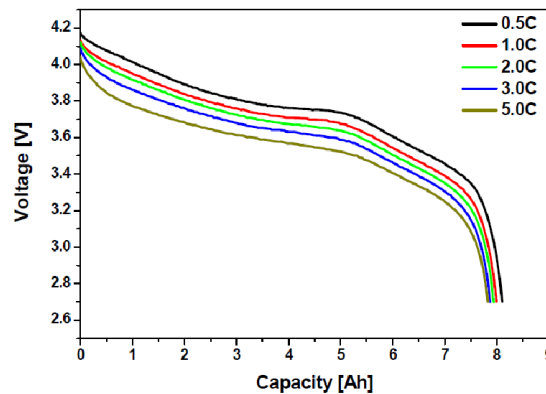


Figure 1.4: Graph showing Capacity Loss at High Discharge Rates

Capacity Fade: It has been observed that there is a loss of capacity in Li-Ion batteries when cycled (charge/discharge) over a number of cycles. The reason for this capacity fade has been attributed to loss of primary, secondary material and the difference of rate capability when quantified [19]. It has also been observed that the loss of capacity is a

function of the energy processed by the battery, it has also been shown that capacity fade is accelerated when cycled at higher rates (like in a vehicle application)[20].

In summary, fast discharging or charging events reduce the lifetime and performance of batteries and hence must be oversized to supply the high current(power) bursts demanded by the load as shown in Section 1.2. This adds additional mass and cost to the system.

1.4 Review of Ultra Capacitor Technology

Ultra Capacitors (UC) unlike batteries (energy is stored via redox reactions in the bulk electrode - high energy density - slow kinetics) store energy by electrostatic storage of charge at the electrode surface. This leads to fast charge and discharge capability (but low energy density) [21].

Ultracapacitor Internals UC construction resembles batteries, with the exception that the mechanisms of charge storage are different. Typically they consist of two electrodes which are immersed in an electrolyte, with a separator between the electrodes. The electrodes are fabricated from extremely porous material and extremely large surface area. Energy is stored in double-layer capacitor as charge separation in the double-layer, formed at the interface between the solid electrode material surface and the liquid electrolyte in the micro pores of the electrodes. An exhaustive review of different UC charge storage mechanisms is out of scope of this work. Listed in Table 1.5 (reproduced from [22]) are some of the newest UC technologies and their capabilities.

1.5 Summary

In summary, it can be seen that UC's have high power capability and low energy storage capability. Since the internal resistance of UC's are potentially lower than batteries, their efficiency during high power pulses are better than batteries. This also implies that a Hybrid ESS (HESS) could lead to lower battery pack temperatures (the net power dissipated in the HESS system is lower because of reduced battery currents); this can lead to denser packing. Low temperature performance is also improved with a HESS because the UC performance is not impacted to a great degree.

Table 1.5: Technology for development of high energy density UC's

Technology type	Electrode materials	Energy storage mechanisms	Cell voltages	Energy density Wh/kg	Power density kW/kg
Double-layer	Activated carbon	Charge separation	2.5-3	5-7	1-3
Advanced carbon	Graphite carbon	Charge transfer	3-3.5	8-12	1-2
Advanced carbon	Nanotube forest	Charge separation	2.5-3	not known	not known
Pseudo-capacitive	Metal oxides	Redox charge transfer	2-3.5	10-15	1-2
Hybrid	Carbon or metal oxide	Double-layer or Charge transfer	2-3.3	10-15	1-2
Hybrid	Carbon or lead oxide	Double-layer or faradaic	1.5-2.2	10-12	1-2

1.6 Scope of this Thesis

The objective of this thesis is to design and characterize topologies for effectively combining batteries (focused on Li-Ion technology) and ultracapacitors. Existing circuit topologies have been characterized; new variants and a new topology have been proposed.

1.7 Glossary of Terms

- ESS - Energy Storage System
- HESS - Hybrid Energy Storage System
- PHEV - Plug-In Hybrid Electric Vehicle
- HEV - Hybrid Electric Vehicle

- EV - Electric Vehicle
- SOC - State Of Charge
- BFL - Battery Facing Load
- UCFL - Ultra capacitor Facing Load
- BMS - Battery Management System

2

Review of Circuit Topologies for Hybrid Storage

Several circuit topologies (reviewed in [23, 24]) have been proposed, to combine batteries and UC's effectively in a hybrid storage system. The primary objective of the circuit is to reduce the bursts of high power seen by the battery, which is detrimental to the performance of the battery. The ideal circuit combined with a suitable control scheme will utilize UC's to provide the bursts of power, while utilizing the battery to provide the energy for the system at a lower, steadier (without current transients) discharge rate. Popular methods to achieve this performance have been presented in this chapter.

2.1 Direct Parallel Connection

The direct parallel connection (Fig 2.1) between batteries and UC's is the simplest way to connect the 2 systems together. The system works by utilizing the differences in the internal resistances and hence the performance of this system depends on the characteristics of the battery and UC.

Advantages:

- Can filter high current transients to battery.
- Simplicity.
- Robustness.

Disadvantages:

- Poor utilization of UC's because the voltage swing and hence the utilization of the energy stored in the UC is limited by the nature of the discharge pulse and the resistances in the system.

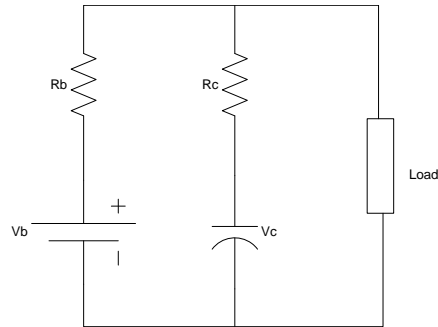


Figure 2.1: Direct Parallel Connection

Studies have been conducted on the performance improvement obtained by direct paralleling.

The paralleling of a modern high energy Li-Ion battery (MP 176065) with a UC (BCAP0310 P250) was simulated in [25]. The number of UC units paralleled with the battery was varied and the performance of the system (for constant power and pulsed power discharge) evaluated by using Ragone plots. It has been shown that for certain load profiles, the hybrid pack performs better than state-of-the-art power Li-Ion batteries.

Experimental results from testing the parallel combination, has been presented in [26] for pulsed loads. It is shown that there is an increase in energy available from the Li-Ion battery, when the duty cycle (of pulsed load) decreases. Also it is shown that there is no benefit on a mass basis and the authors recommend adding power electronics in the system, to improve utilization of the UCs.

A theoretical analysis of the parallel combination is presented in [27]; and shows improvement in peak power capability, smaller internal losses and greater discharge life.

2.2 Combining using a Power converter

In order to overcome the limitations of a direct parallel connection, a power converter can be inserted between the battery and UC as shown in Fig 2.2. The main goal of inserting the power converter is to be able to control battery current and hence control the stress applied to the battery. It also has the advantage of being able to utilize the UC by discharging it to a lower voltage than possible by just using a simple parallel connection.

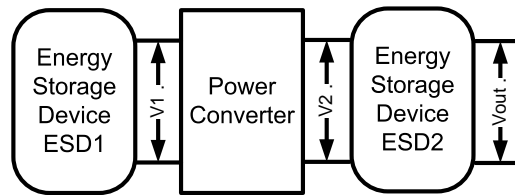


Figure 2.2: Hybrid system with a Power Converter

2.2.1 Circuit Topologies

Several topologies (buck-boost, Cuk, Sepic etc) can be used for implementing the power converter. Each of these topologies have their merits and demerits with respect to circuit complexity, component count, switch ratings and control scheme. A comparison of the various topologies has been presented in [28]. The buck-boost (half bridge) converter is the most popular topology owing to its simplicity and robustness. Hence the buck-boost converter is reviewed in detail below and the design of buck-boost variants is presented in Chapter 4.

2.2.2 Buck-Boost Converter

It must be noted that the power converter has to be bi-directional. This is to support both charge and discharge sequences. Though a number of converter configurations are possible, the buck-boost configuration (Fig 2.3) is the most popular option [29, 14]. There are 2 different configurations possible, battery connected to the bus or the UC connected to the bus [30]. In the former, the battery voltage becomes the bus voltage and hence is relatively stable (Li-Ion terminal voltage stays relatively flat while delivering most of its energy) ; in the latter, the bus voltage would vary with UC State of Charge (SOC). However

with the battery connected to the bus, there is no direct control on battery current, which is the advantage of the other method. The disadvantage of having the UC bank supporting the bus voltage is because of the fact that UC's have low cell voltages (2.5V, typical) and hence a lot of individual cells are needed to attain high bus voltages (which is preferable) from a system perspective.

Although buck-boost converters are popular, almost all published work consider the case of the battery connected to the bus. Hence one of the major objectives of this work is to clearly define the 2 variants, characterize their performance and evolve a design methodology for using them (Chapter 4).

2.2.3 Control Strategy

The goal of the control strategy is to source current from the UC, when there is a high power demand, accept high current pulses (like during regenerative braking). The challenge, is to maintain the UC SOC dynamically, so as to perform the above task and in order to perform this, there has to be energy transfer between the battery and UC. All the control strategies reviewed in this section apply to the buck-boost topology with the battery connected to the load.

In [14], the control strategy is implemented in the form of a rule based system (rule for UC SOC and battery current limits) which is implemented using a Artificial Neural Network (ANN). The performance of this approach is measured by using an electric vehicle on a urban drive cycle. In the authors opinion this is not a reliable measure; the reason being that the performance of the system is highly dependent on the ANN tuning, the drive cycle, drive style etc.

In [29] and [31], traditional small-signal modeling approach is applied to PWM buck-boost converters. A transfer function for UC current to duty cycle is obtained and this transfer function is then used to design a standard PI (Proportional Integral) controller for the system. Both the referred works do not include a vehicle level control strategy.

Some other control techniques employed include a digital polynomial control strategy (RST); presented in [32] and a wavelet based control scheme presented in [33].

Advantages:

- Independent battery and UC voltages.

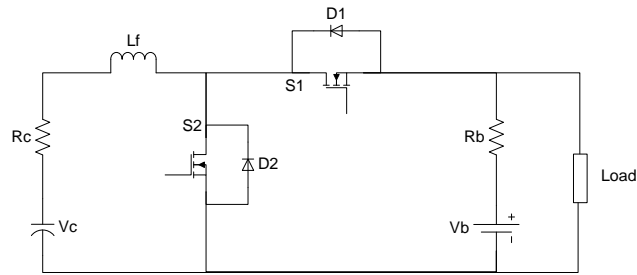


Figure 2.3: Buck-Boost Power Converter used to combine Battery and UC

- Better utilization of UC.
- Battery Current control possible (if UC is connected to the bus).

Disadvantages:

- Bus voltage control not possible.
- Power losses in the converter.
- Increased Component count.

2.3 Multi Input Converters

Multi input converters have the advantage of combining sources with different characteristics. A typical multi-input converter which is commonly found in literature [34, 35] is shown in Fig 2.4 (reproduced from [34]). The topology essentially works like multiple buck-boost converters in parallel.

Control:

It is possible to control the independent converters in either voltage mode or current mode. The goal of the control is to be able to operate each of the power sources which are connected to the converter, on the basis of their characteristics. A control system for a multi-input converter combining UC, battery and fuel-cell generator is presented in [36].

Advantages:

- Flexibility in combining multiple sources.

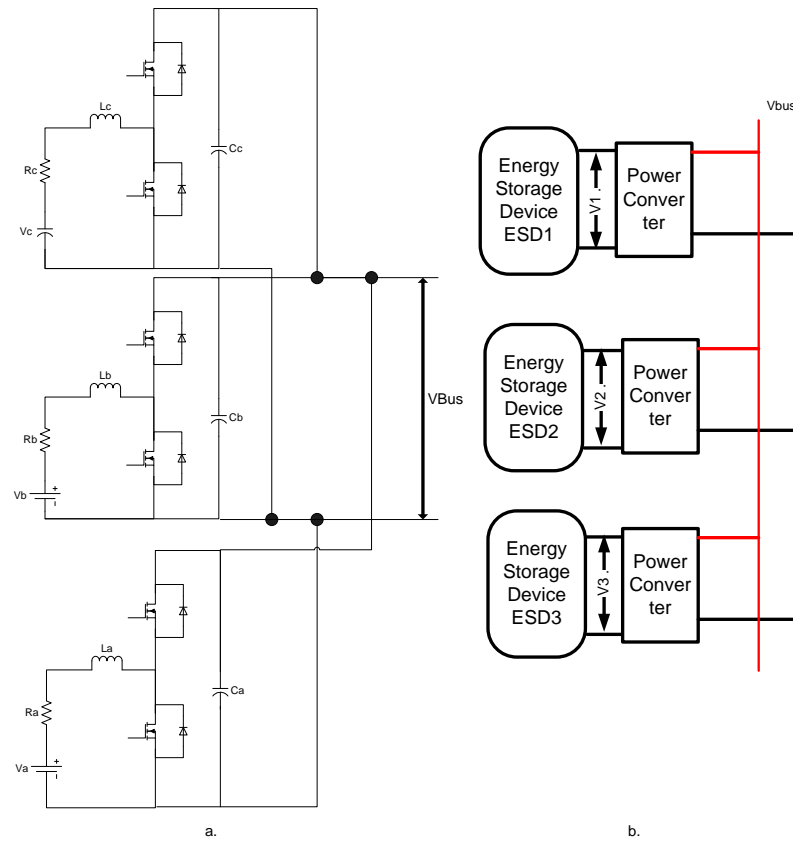


Figure 2.4: a. Multi-Input Converter b. General structure

- Bus voltage control possible.

Disadvantages:

- Increased number of system elements.
- Decreased efficiency.
- Complex control.

2.4 Source Swapping

This is a novel topology [37], which allows simple source selection between batteries and UC's (shown in Fig 2.5). Switch S1 or S2 is switched on and allows either the battery

or UC to directly drive the load. There is a low power DC/DC converter in the circuit implemented by switches M1, M2 and inductance L. This converter (working in buck or boost modes) allows for charge transfer between the battery and UC, and current injection to the load. There are many possible modes of operation which can be implemented with this system.

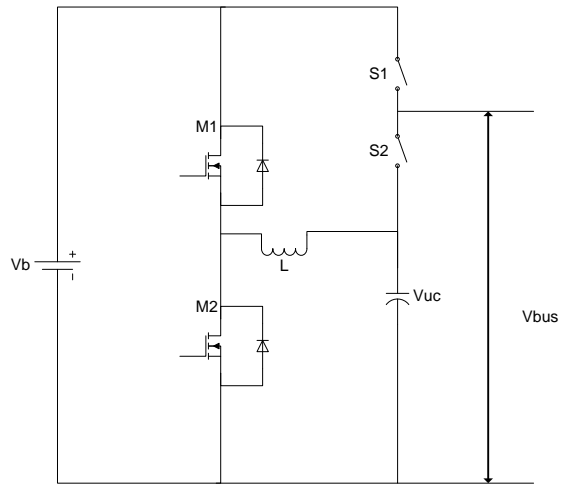


Figure 2.5: Novel Topology for Hybrid Storage

Advantages:

- Simple hardware.
- Several modes of operation are possible.

Disadvantages:

- No bus voltage control.
- Wide bus voltage swing.
- High control complexity.
- System efficiency could be impacted.

2.5 Summary

A number of topologies for combining batteries and UCs to form a hybrid energy storage system (HESS) have been reviewed. These can be broadly classified as passive topologies (which do not employ power converters) and active topologies (which employ at least 1 power converter). Although there are many publications dealing with HESS topologies, there is a dearth of information about the relative performance characterization of these various topologies. This information could serve as a design guide for selecting a suitable topology for a target application. As mentioned in Chapter 1, the primary objective of this work is to address this lack of information.

3

Performance Characterization of Passive Hybrid ESS

It is essential to quantify the performance benefits of different circuit topologies for combining batteries and UC's. This will establish a metric for evaluating the performance of new topologies as well as providing a basis to select a certain topology and design the hybrid ESS optimized for a target application. The following are used as performance measures in this work:

- Reduction in peak battery current.
- Battery and UC RMS currents (can be used to calculate system losses and efficiency improvement).

The performance improvements are measured by employing analytical techniques. The analytical method presented in [38] (performance evaluation of direct parallel connection) is employed in this work, and has been extended to evaluate paralleling of battery and UC with an inductor. The following topologies are evaluated:

- Direct parallel connection.
- Paralleling with an inductor between battery and UC.

Since performance is dependent on the load power profile of the application, a standard load power profile is used as reference. The load for this analysis is assumed to be

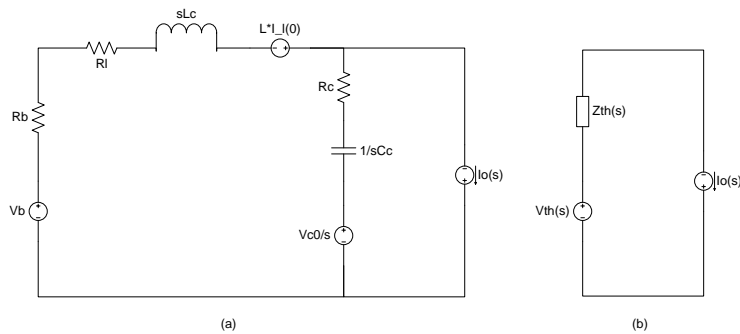


Figure 3.1: (a) Complete Frequency domain circuit (b) Thevenin equivalent circuit

a pulsed current load of a certain duty cycle d , frequency f and magnitude I_o . A similar analysis has been presented in [39], but lacks mathematical analysis of the paralleling with an inductor system.

3.1 Analytical Model for Direct Parallel and Paralleling with an Inductor

3.1.1 Circuit Model

Frequency domain Thevenin model of the circuit is used to compute the performance of the hybrid ESS. A simple model of the battery (voltage source, with a series resistance) and UC (capacitor, with a series resistance) are used. This helps in reducing the complexity of the model while still allowing us to quantify performance (with approximations) and visualize the working of the system and its potential benefits. The circuit used to model direct paralleling and paralleling with an inductor is shown in Fig 3.1.

The Thevenin voltage and impedance of the system are described by equations 3.1 and 3.2 respectively. Where $V_{th}[s]$ is the Thevenin voltage and $Z_{th}[s]$ is the Thevenin resistance. C_c and L_c denote the UC and the inductance (in the paralleling with inductor case) and R_b , R_c and R_l are the internal resistances of the battery, capacitor and inductor respectively. The initial conditions of the UC voltage and inductor current are denoted by V_{c0} and I_{l0} respectively.

$$\begin{aligned}
V_{thc1}[s] &= \frac{V_b}{s} \cdot \frac{R_c + \frac{1}{s \cdot C_c}}{R_b + R_l + s \cdot L_c + R_c + \frac{1}{s \cdot C_c}} \\
V_{thc2}[s] &= \frac{V_{c0}}{s} \cdot \frac{s \cdot L_c + R_l + R_b}{\frac{1}{s \cdot C_c} + R_c + s \cdot L_c + R_l + R_b} \\
V_{thc3}[s] &= L_c \cdot I_{l0} \cdot \frac{R_c + \frac{1}{s \cdot C_c}}{R_b + R_l + s \cdot L_c + R_c + \frac{1}{s \cdot C_c}} \\
V_{th}[s] &= V_{thc1}[s] + V_{thc2}[s] + V_{thc3}[s]
\end{aligned} \tag{3.1}$$

$$Z_{th}[s] = \left(\left(R_c + \frac{1}{s \cdot C_c} \right)^{-1} + (R_b + R_l + s \cdot L_c)^{-1} \right)^{-1} \tag{3.2}$$

3.1.2 Modeling the load

The load is modeled by pulsed current of frequency f , duty cycle d and peak magnitude of I_o . The time and frequency domain equations are described in 3.3 and 3.4.

$$i_o[t] = I_o \cdot \sum_{k=0}^{N-1} (u(t - kT) - u(t - (k + d)T)) \tag{3.3}$$

$$i_o[s] = I_o \cdot \sum_{k=0}^{N-1} \frac{e^{-kT \cdot s}}{s} - \frac{e^{-(k+d)T \cdot s}}{s} \tag{3.4}$$

3.1.3 Branch currents and terminal voltages

The internal drop in the complete system is obtained in equation 3.5. Using this value, the output voltage and the branch currents can be computed, as shown in equations 3.6 to 3.7. Where $V_o[s]$ is the output voltage, $I_b[s]$ and $I_c[s]$ are the battery and UC currents respectively.

$$V_{drop}[s] = Z_{th}[s] \cdot I_o[s]$$

$$V_o[s] = V_{th}[s] - V_{drop}[s] \tag{3.5}$$

$$I_b[s] = (R_b + s \cdot L_c + R_l)^{-1} \cdot \left(\frac{V_b}{s} - V_o[s] \right) \tag{3.6}$$

$$I_c[s] = I_o[s] - I_b[s] \tag{3.7}$$

3.2 Electric Scooter Testbed

An electric scooter has been used as a testbed in this work. The reason to choose a scooter as the testbed, was the relative simplicity of the system (as compared to a 4 wheeler) with respect to its control system and drive electronics. The scooter consumes about 1kW - 1.5 kW during operation and the load profile closely resembles a 4 wheeled application.

The battery pack used to power the system consists of Kokam (SLPB75106100) 7.5Ah energy Li-Ion battery cells which are modeled by a 3.7V voltage source and an internal resistance of 5.3mOhm/cell.

A Maxwell 350F, 2.5V UC (BCAP0350 E250) is used in the UC pack and is modeled as a 350F capacitor with an ESR of 3.2mOhm/cell.

The bus voltage is 50V and the peak current is 30A. This needs a series connected battery string with 14 cells and a UC series connected string with 20 cells. The system frequency is assumed to be $f = \frac{1}{(Rb+Rc) \cdot Cc} = 0.425Hz$. The system parameters are summarized as $Vb = 50V$, $Rb = 74m\Omega$, $Rc = 60m\Omega$, $Cc = 17.5F$. The electric scooter, the battery pack and the UC pack are shown in Fig 3.2. All the HESS topologies discussed in this work use the same battery pack and UC pack, in order to enable a fair comparison.

These parameters are used to provide numerical examples in the following analysis. *However it must be noted that the analysis technique itself is generic.*

3.3 Analysis: Direct paralleling of battery and UC

Fig 3.3 shows the battery, UC current and output voltage in time domain (obtained by Inverse Laplace Transform) at a pulsed load current (30A) frequency of 0.425Hz (2.3s) and 10% duty cycle. It can be observed that the battery peak current is reduced to about 20A. Fig 3.4 shows the performance of the system, at 10 times the system frequency and 50% duty cycle. It can be observed that the system has not attained steady state yet, the battery current keeps increasing and hence the performance of the hybrid ESS, varies from cycle to cycle. Considering the nature of the load, it is meaningful to evaluate the performance of the system in two separate cases,1. Single Pulse Performance 2. Steady State Performance.

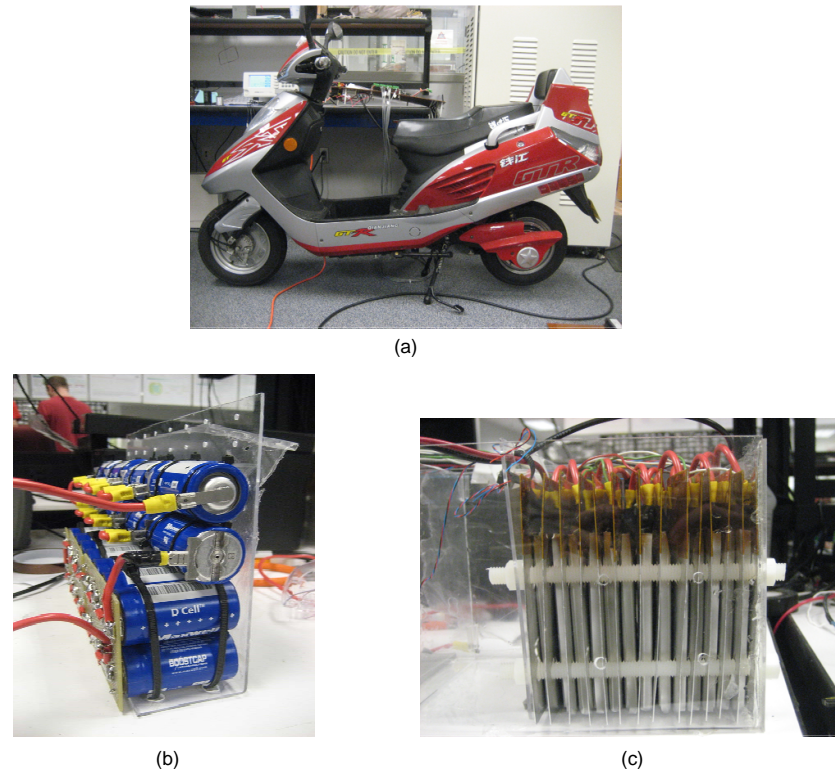


Figure 3.2: (a). Electric Scooter testbed (b). UC pack (c). Battery pack

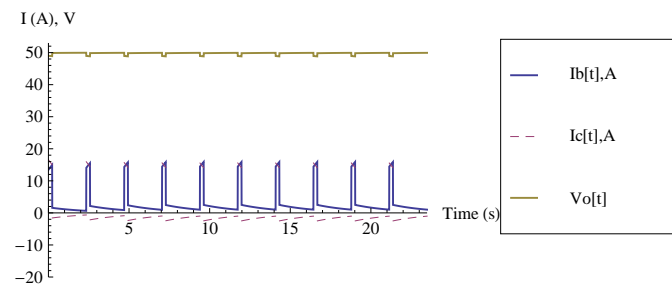


Figure 3.3: Direct parallel HESS with pulsed load: $I_o = 30A$, $f = 0.425Hz$, $Duty = 10\%$

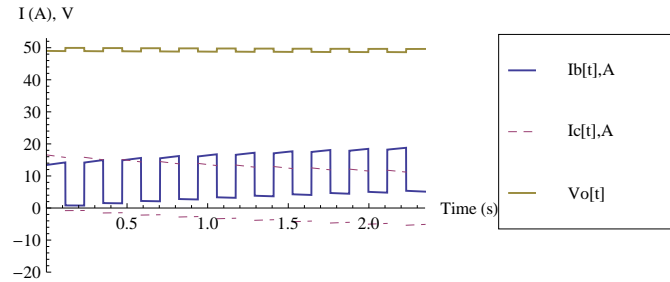


Figure 3.4: Direct parallel HESS with pulsed load: $I_o = 30A$, $f = 4.25Hz$, $Duty = 50\%$

3.3.1 Single pulse performance characterization

Peak Current Reduction: In this analysis, the system is assumed to have been at rest until complete charge distribution between battery and UC has taken place (i.e $V_b = V_c = 50V$). The battery current factor shown in Eq 3.8 is plotted (Fig 3.5) for different pulse width's and it can be observed that as pulse width gets larger, the benefit from the hybrid pack decreases and the battery current factor saturates at 1.

$$I_{cf} = \frac{I_o}{Max[Ib]} \quad (3.8)$$

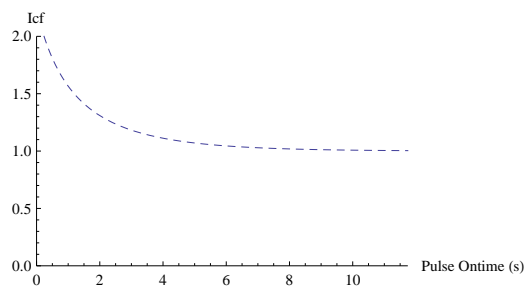


Figure 3.5: Battery current reduction factor for different pulse widths

Time to Recovery: Time to Recovery (TR) is defined as the time taken for complete redistribution of charge between the battery and UC. This aids in determining the load pulse frequency which can be applied to the system with the desired single pulse performance. TR can be obtained by setting the battery current to zero (implies UC is fully charged) or to some finite value $I_{b_{min}}$ (because the exponential charging characteristic leads to a large

time to zero current) as denoted by Eq 3.9. Because the equation for Ib (Eq 3.6) is not algebraic a numerical root finding technique has to be used to find the solution. Example, for a pulse width of duration 1 second and $Ib_{min} = 1A$, a period of 4.26 seconds is required after the end of the pulse; for Ib to reach 1A. Fig 3.6 shows the recovery time for different pulse widths and as expected it can be seen that it saturates for larger pulse widths; this is due to the limited role the UC can play for larger pulse widths.

$$Ib[Tpulse + TR] = Ib_{min} \quad (3.9)$$

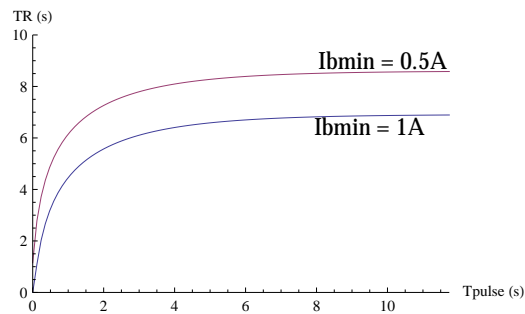


Figure 3.6: Time to Recovery for different pulse widths and Ib_{min}

RMS currents and Loss Analysis: RMS battery and UC current during the application of the load pulse and the subsequent recharge phase, and the total loss in the system can be calculated and hence the efficiency improvement can be quantified. The time considered for the RMS measurement includes the load pulse duration and the charge redistribution phase after. Currents (per pulse) in a battery only system and the hybrid ESS for various pulse widths are show in Fig 3.7. An example for the case of pulse width of duration 1 second and $Ib_{min} = 1A$ is considered. Power dissipated (per pulse) in a battery only system and the hybrid ESS are compared in equations 3.10 and 3.11 respectively.

$$Ib_{RMS} = 10.35A$$

$$TotalLoss = Ib_{RMS}^2 \cdot Rb = 7.9W \quad (3.10)$$

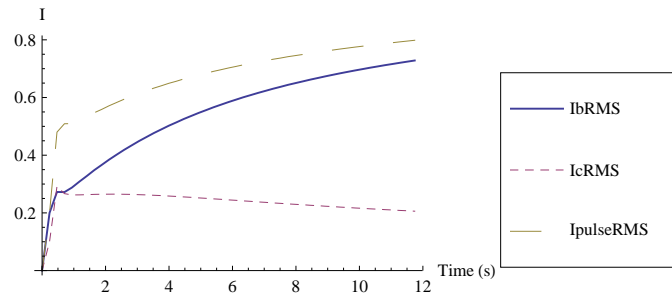


Figure 3.7: Normalized RMS currents for varying pulse widths

$$I_{C_{RMS}} = 5.26A$$

$$I_{b_{RMS}} = 8.14A$$

$$TotalLoss = I_{b_{RMS}}^2 \cdot R_b + I_{c_{RMS}}^2 \cdot R_c = 6.58W \quad (3.11)$$

3.3.2 Steady State pulse performance characterization

Condition for Steady State: In a battery - UC direct parallel connection, the state of the capacitor voltage is an indication of the steady state condition. By the principle of charge balance, the charge into and out of the UC, during a load current pulse, should be the same in steady state. This also implies that the UC voltage at the start and finish of the load current pulse should be the same. When the initial voltage of the UC V_{c0} is initialized to this voltage, the system enters steady state condition immediately. This value of initial capacitor voltage is obtained by using numerical methods to solve Eq 3.12 (where T_{cy} is the pulse width of the load current pulse). Applying this technique to the system as described in Fig 3.4, the value of $V_{c0} = 48.26$ is obtained. When the system is simulated with this initial condition for the UC voltage, it is found to be in steady state as shown in Fig 3.8.

$$V_{c0} = V_o[T_{cy}, V_{c0}] - I_b[T_{cy}, V_{c0}] \cdot R_c \quad (3.12)$$

Peak Current Reduction: The steady state condition for V_{c0} is inserted into the time domain simulation, and the battery current factor (as defined earlier) is plotted in Fig 3.9.

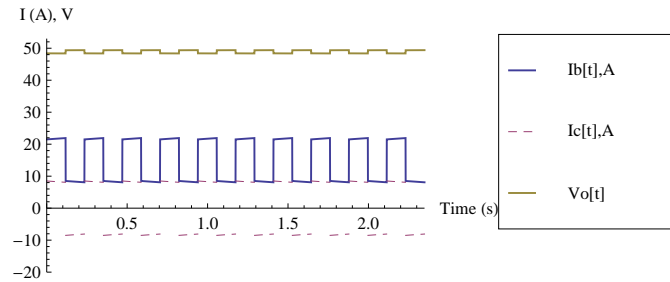


Figure 3.8: Direct parallel HESS with pulsed load: $I_o = 30A$, $f = 4.25Hz$, $Duty = 50\%$, $V_{c0} = 48.9148$

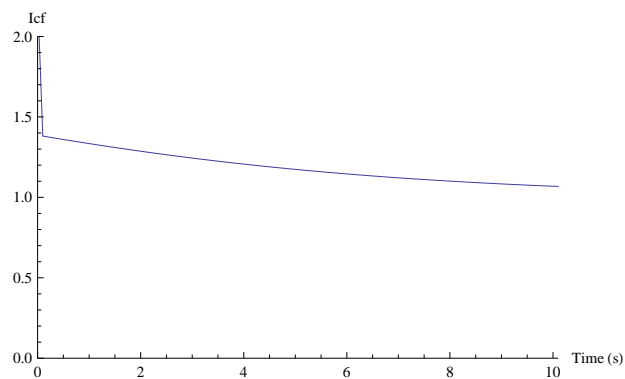


Figure 3.9: Battery current reduction factor for different load current widths ($dutycycle = 0.5$)

RMS currents and Loss Analysis: The steady state condition for V_{c0} is inserted into the time domain simulation, and the RMS battery and UC currents are calculated over 1 cycle. The RMS currents in the system for varying load pulse widths ($dutycycle = 0.5$) are computed from this steady state condition and are shown in Fig 3.10. An example for the case of pulse period of duration 1 second is considered. Power dissipated (per pulse) in a battery only system and the hybrid ESS are compared in equations 3.13 and 3.14 respectively.

$$I_{b_{RMS}} = 21A$$

$$TotalLoss = I_{b_{RMS}}^2 \cdot R_b = 33.02W \quad (3.13)$$

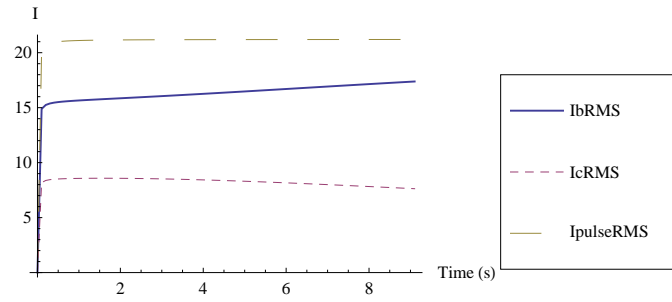


Figure 3.10: Normalized RMS Currents in a Steady State System with varying pulse periods

$$\begin{aligned}
 I_{C_{RMS}} &= 8.46A \\
 I_{b_{RMS}} &= 16.3A \\
 TotalLoss &= I_{b_{RMS}}^2 \cdot R_b + I_{c_{RMS}}^2 \cdot R_c = 24.04W
 \end{aligned} \tag{3.14}$$

3.4 Analysis: Paralleling of battery and UC with an inductor

The rationale behind adding an inductance in the system is that it can provide a method to alter (tune) the system to be effective for load power pulses of a certain frequency and duty cycle. Designing the inductor (potentially cheaper than altering the UC bank) suitably can also allow for better utilization of UC by increasing the impedance of the battery current path. An example showing battery and UC currents for a pulsed load current (30A) frequency of 0.425Hz (2.3s), 10% duty cycle paralleled with a 200mH inductor is shown in Fig 3.11 and in comparison with Fig 3.3, it is evident that there is a reduction in battery current.

3.4.1 Single pulse performance characterization

Peak Current Reduction: The same procedure discussed in section 3.3.1 is used. The battery current factor ($I_{cf} = \frac{I_o}{Max[I_b]}$) is plotted for different pulse width's as a fraction of $T = 11s$. A 3-D plot is generated for values of inductances ranging from 1mH to 1H and is shown in Fig 3.12. It can be observed that significant improvement is obtained for pulse widths of up to 5 seconds. This figure can also be used as a aid for sizing the optimal

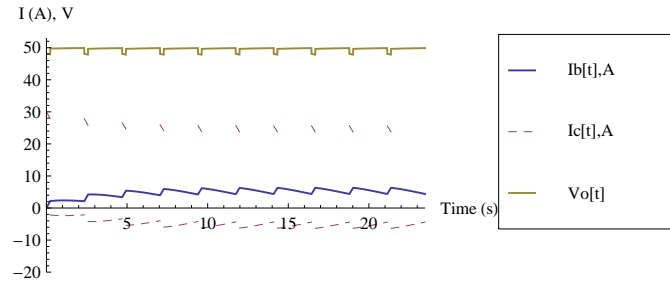


Figure 3.11: Paralleling with inductor HESS with pulsed load: $I_o = 30A$, $f = 0.425Hz$, $Duty = 10\%$, $L_c = 200mH$

inductance.

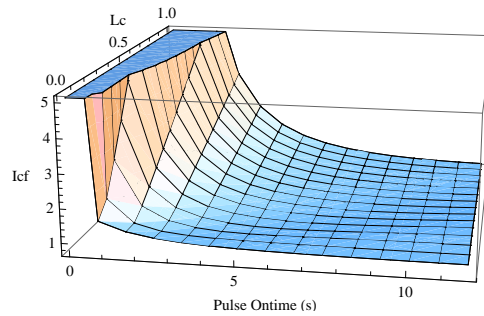


Figure 3.12: I_{cf} for different pulse widths and inductances (1mH-1H)

Time to Recovery: It can be computed using the same procedure detailed in the previous section. Fig 3.13 shows the recovery time for various load pulse widths and $I_{b_{min}}$. A 200mH inductance is considered. It can be observed that the TR decreases above certain pulse widths; the reason for this behavior is because for longer time periods, the UC is recharged even before the end of the load current pulse.

RMS currents and Loss Analysis: The procedure similar to the one presented in the previous section is used. The time considered for the RMS measurement includes the load pulse duration and the charge redistribution phase after. The RMS currents in the system for varying load pulse widths are computed from this steady state condition and are shown in Fig 3.14.

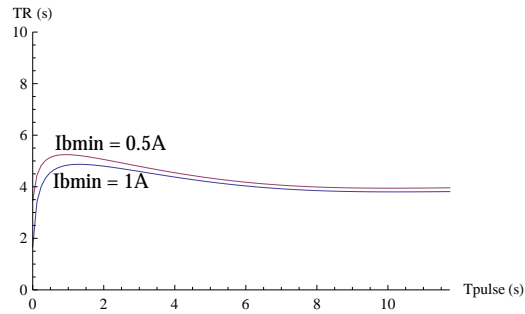


Figure 3.13: Time to Recovery for different pulse widths and I_{bmin} ($L = 200mH$)

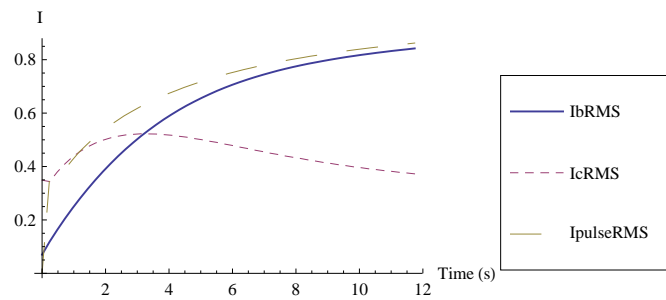


Figure 3.14: Normalized RMS currents for varying pulse widths

3.4.2 Steady State pulse performance characterization

Condition for Steady State: Since there are two state variables in the system, the technique applied to the direct parallel HESS cannot be applied. Hence an approximate technique is utilized, where it is assumed that the ripple in inductor current and UC voltage is much smaller compared to their respective average values. This is the same technique called the “small-ripple approximation” introduced in [40]. In steady state, the inductor volt-second and capacitor - charge balance have to be zero over the load current pulse - if this condition is not met, the inductor current and UC voltage will ramp up to infinity which is impossible in a practical system with losses. Using these approximations, it can be shown that the average inductor current and hence the battery current is $I_b = Duty * I_o$; where $Duty$ and I_o are the duty cycle and amplitude of the load pulse respectively. The larger the inductance, the better the approximation.

3.5 Inductor Sizing for the HESS

Choosing an optimal size of the inductor will help determine if it is feasible for implementation (of the hybrid ESS) or if it is necessary to choose another implementation technique - for example using a power converter.

Method 1: If the system is expected to be used with an application which resembles the single pulse performance characteristics, Fig 3.12 can be used to choose an inductor optimized for a certain pulse load current timing.

Method 2: For this analysis it is assumed that the pulse duty cycle is 50%. This is a reasonable assumption because for pulse widths greater than 50% the impact of the UC is decreased, and sizing an inductor for this case, ensures performance for all lower duty cycles. A Fourier analysis of the square wave reveals that the even harmonics are absent and the maximum power is present in the fundamental frequency. Good performance improvement is obtained if the inductor is sized such that battery impedance for the fundamental frequency of the load power pulse is greater than 10 times the UC internal resistance ($Z_b > 10.R_c$) (A higher or lower factor can be used for design, this factor directly impacts inductor value and dimensions). This would ensure that the UC shares the majority of the peak current.

3.6 Conclusion

It can be concluded from this analysis that the benefit from this system is highly coupled with the nature of the load pulse. This analysis method provides a tool to model the system performance for an stream of pulses or a single pulse and can be extended to any arbitrary waveform by considering them as a sequence of pulses.

Using the analysis presented in this chapter, an estimation of the performance of the passive HESS systems can be obtained. It can be inferred from Fig 3.5 and from Fig 3.9 that for the width of load pulses in this application, there is only marginal improvement in battery peak current reduction. The improvement decreases as the width of the load current pulse increases. The same observation holds good with the RMS current reduction (and hence the losses).

It can also be inferred that passive HESS are not very effective with the state of the art Li-Ion batteries and UC's. The reason being that the performance of the passive HESS

systems is a major function of internal impedance (ESR) and the ESR's of the battery and UC are in the same order of magnitude. Also the UC utilization is very low. The voltage swing on the UC is a measure of the energy delivered by the UC and it can be observed that the UC voltage swing is very low. Hence active HESS topologies are required to extract greater benefit from the addition of UCs to the system.

4

Design and Evaluation of Buck-Boost Converter Variants

4.1 Introduction

Several active HESS topologies for combining batteries and UC's have been reviewed in Chapter 2. The bi-directional Buck-Boost converter is one of the most popular topologies to build HESS; because of the simplicity and robustness it offers. Hence this topology has been selected for implementation in this work.

Although there are several publications dealing with the different aspects of implementing the buck-boost topology, there are some shortcomings. In the opinion of the author, the performance measures found in literature are ambiguous, because of tests being performed with different load profiles and control techniques (i.e. there is a lack of a reference technique to measure performance).

The objective of this work, is to design buck-boost converter variants; develop a common control scheme and evaluate performance of HESS with a standard load profile. This approach provides an objective means of evaluating the relative performance of the various topologies tested. It can also serve as a reference technique for evaluating other HESS circuit topologies. The following variants of the buck-boost converter are designed and evaluated in this work:

- Buck-Boost Converter - Battery facing Load (BFL)

- Buck-Boost Converter - Ultra Capacitor facing Load (UCFL)
- Interleaved Buck-Boost Converter

All the variants are designed for the electric scooter system which has been described in Section 3.2. *Evaluating the relative benefits of the “Battery Facing Load” and the “UC Facing Load” variants (Fig 4.1) is the novel contribution of this work.*

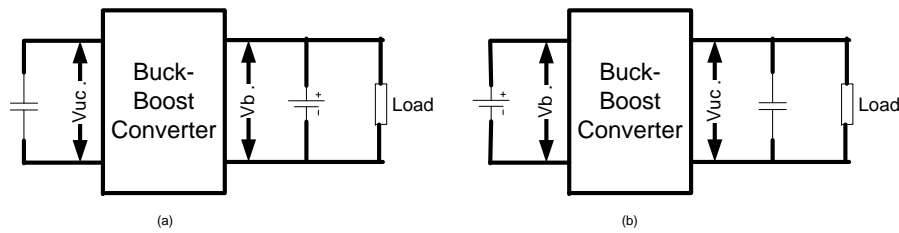


Figure 4.1: (a). Battery Facing Load (BFL) variant (b). UC Facing Load (UCFL) variant

4.2 Load Profile

A standard load profile (power-time demand) is required for the purpose of evaluating HESS topologies. The load profile needs to be representative of the real-world loads experienced by automobiles. UDDS (Urban Dynamometer Driving Schedule) or the FUDS (Federal Urban Driving Schedule) based load profiles, are too complex for a simple control scheme to be effective. Hence a simplified load profile, based on the FUDS load profile is chosen. This profile is described in the USABC “Electric Vehicle Battery Test Procedures” manual and is shown in Fig 4.2.

Since the profile defines percentage power, 100% is defined as 1.5kW for the electric scooter application.

4.3 Test System Description

The test system which is used for simulations and experimental validation of the various HESS topologies under consideration is shown in Fig 4.3. All the HESS topologies evaluated are optimized (component dimensioning and control optimization) for the EV DST load profile; this enables a fair performance comparison.

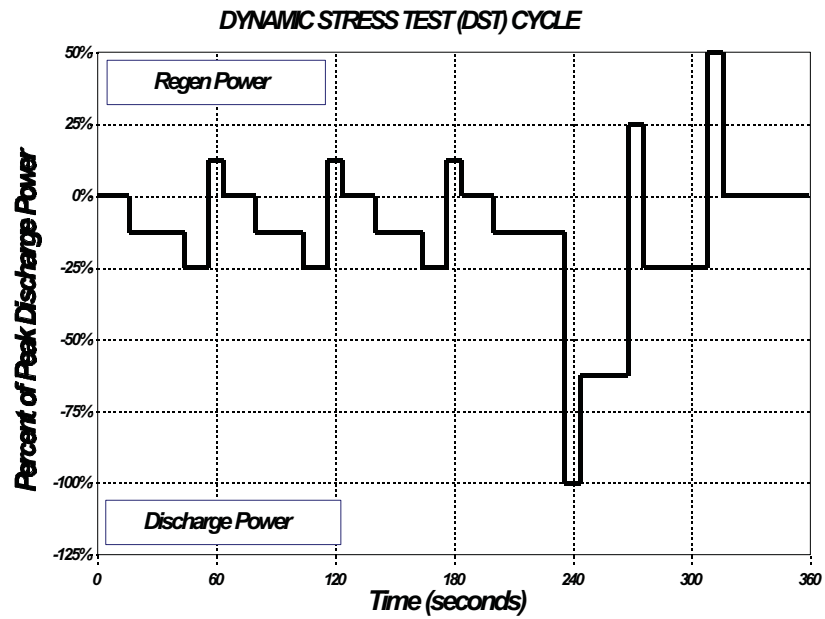


Figure 4.2: EV DST load profile (reproduced from USABC test manual)

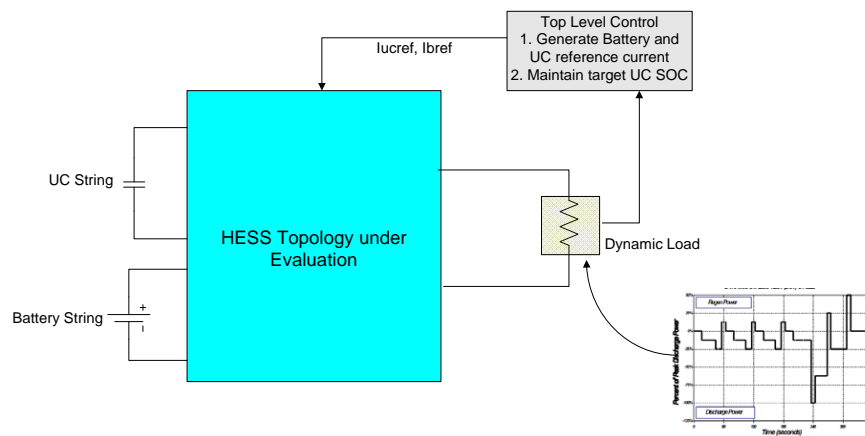


Figure 4.3: Block diagram of the test system

4.4 Control Scheme

The control scheme is responsible for governing the operation of the HESS topology. In the case of the buck-boost converter the controller is responsible for controlling the battery/UC currents and to maintain the UC State of Charge (SOC). Several control schemes have been proposed in literature (reviewed in Section 2.2.3). Complex control schemes have the disadvantage of being tough to characterize - their performance is a strong function of their design, tuning and load profile (for example the performance of a neural network control scheme depends on its design and tuning). The control scheme for this task (evaluating HESS topologies), needs to be simple and provide repeatable performance. Developing an optimal control scheme is beyond the scope of this work. Hence the control scheme used in this work, is developed based on [41]; the method involves the use of simple filters and provides repeatable performance. It can be tuned for desired performance and is also capable of maintaining UC SOC. The control scheme is optimized for the EV DST load profile. The control scheme as shown in Fig 4.4 is divided into 2 parts.

Top Level Control: The function of this block is to generate the target current output command to the DC/DC converter, based on the power demand and vehicle speed. The top level control also has to ensure that the UC SOC is maintained within predefined boundaries - this function is achieved by modifying the current command sent to the DC/DC converter as a function of UC SOC.

DC/DC Control: The function of this block is to cause the DC/DC converter's current output to track the reference generated by the top level control. The DC/DC converter can be thought of as a current source assisting the primary supply. The implementation of this block is presented along with converter design in a following section.

4.4.1 Top Level Control Implementation

The two functions of the top level control are 1. To generate a reference current to the DC/DC converter and 2. To maintain UC SOC above a minimum defined level. The reference current is generated by sensing the load current demand and applying a filter to it. Since there is no direct way to control UC SOC, it is controlled by modifying the reference current to the DC/DC converter. The top level controller is different for the 2 topology variants (i.e. Battery facing Load and UC facing load) and is shown in Fig 4.5.

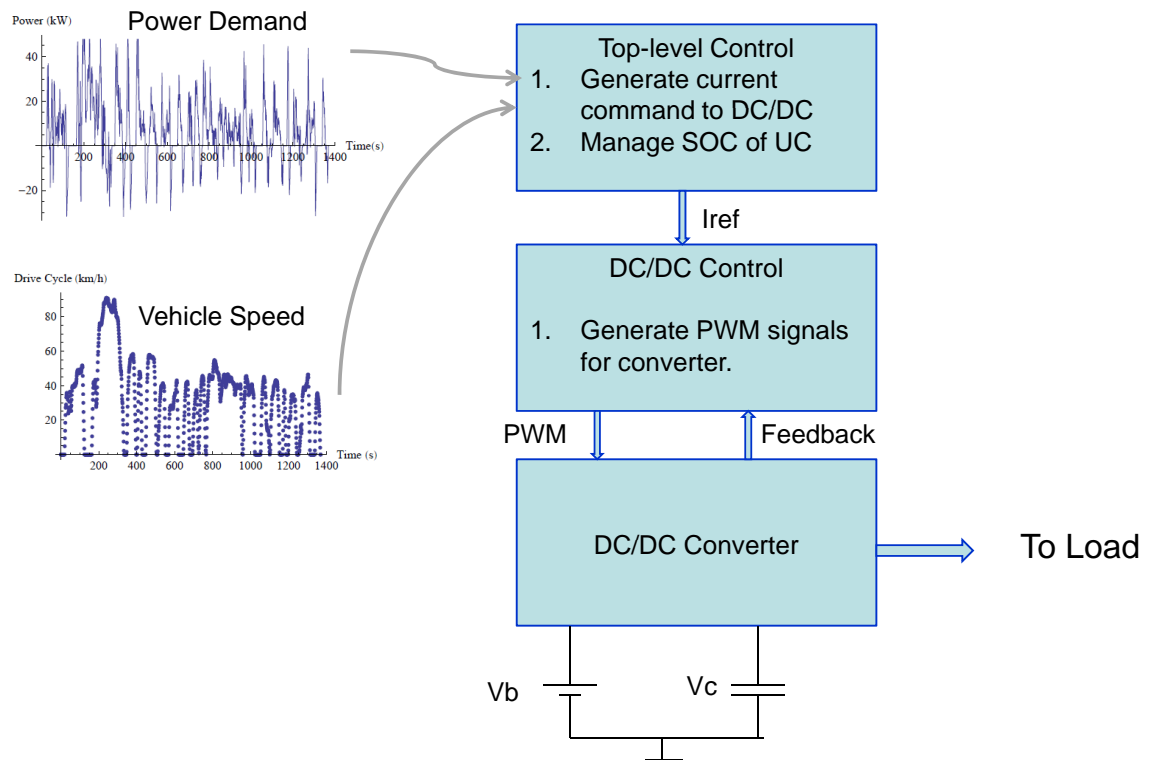


Figure 4.4: Overview of the control scheme

All simulations are performed using PSpice.

Reference Current Generator

In the BFL variant, the reference current is generated using a feed-forward scheme, where load current is sensed and passed through a High Pass Filter (HPF). Subjectively, the job of the DC/DC converter in this case (sourced by the UC) is to supply the spikes in current demand and regenerated current - thereby reducing battery stress. The battery supplies the average load demand. The filter time constant can be adjusted to get the desired load sharing between the battery and the UC. Similarly in the UCFL variant, a Low Pass Filter (LPF) is used to generate the current reference - the goal is for the DC/DC converter (sourced by the battery) to supply the average current demanded by the load and for the UC connected to the bus to supply the spikes in current demand. It is also possible to sense the driver demand instead of load current demand, which will improve performance

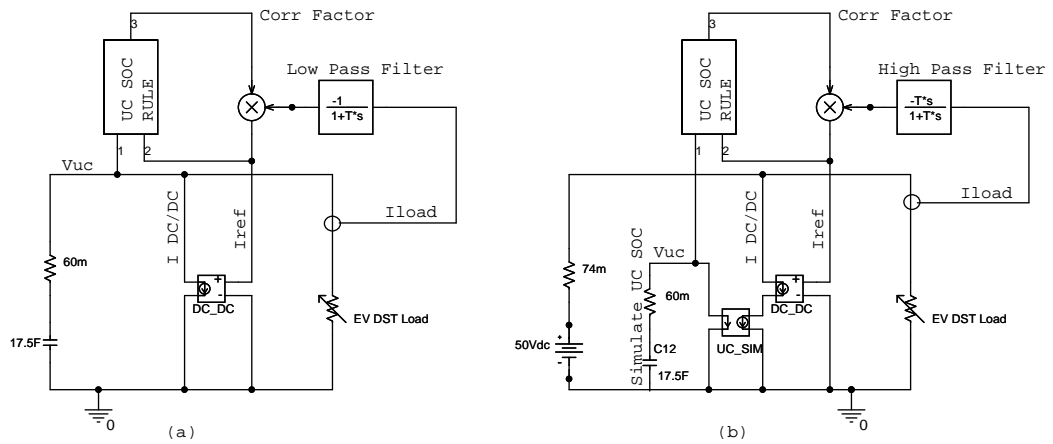


Figure 4.5: Top Control Implementation (a). UC facing Load (b). Battery facing Load

in real applications.

UC SOC Control

In both the topology variants, there is the need for maintaining the UC SOC between a predefined range ($V_{max} - V_{min}$). For example in the BFL variant, the DC/DC converter has a defined minimum input voltage, and the UC voltage must not be allowed to drop below this level. In the UCFL variant, the target application defines the minimum input voltage (for e.g. the electric scooter drive has a defined minimum voltage of 38V). The UC SOC is controlled by modifying the current reference to the DC/DC converter, by multiplying the reference current to the DC/DC (I_{ref}) by a correction factor ($CorrFactor$). The correction factor is generated by an exponential function (which models capacitor, charge-discharge characteristics), which reduces the current demand to the DC/DC in the BFL variant and by increasing the current demand to the DC/DC in the UCFL variant. The UC SOC control rules are shown in equation 4.1 for BFL variant and equation 4.2 for the UCFL variant. I_{ref} is negative when sourcing current (discharging) and positive when sinking current (charging). Where V_{max} and V_{min} are the maximum and minimum allowed UC voltages, V_{sf} is the scaling factor which controls the behavior of the scaling function and can be tuned for desired performance.

$$\begin{aligned} \text{CorrFactor} &= e^{-(V_{max}-V_{uc})/V_{sf}}; \text{ for } I_{ref} < 0 \\ \text{CorrFactor} &= e^{-(V_{uc}-V_{min})/V_{sf}}; \text{ for } I_{ref} > 0 \end{aligned} \quad (4.1)$$

$$\begin{aligned} \text{CorrFactor} &= 1 - e^{-(V_{max}-V_{uc})/V_{sf}}; \text{ for } I_{ref} < 0 \\ \text{CorrFactor} &= 1 - e^{-(V_{uc}-V_{min})/V_{sf}}; \text{ for } I_{ref} > 0 \end{aligned} \quad (4.2)$$

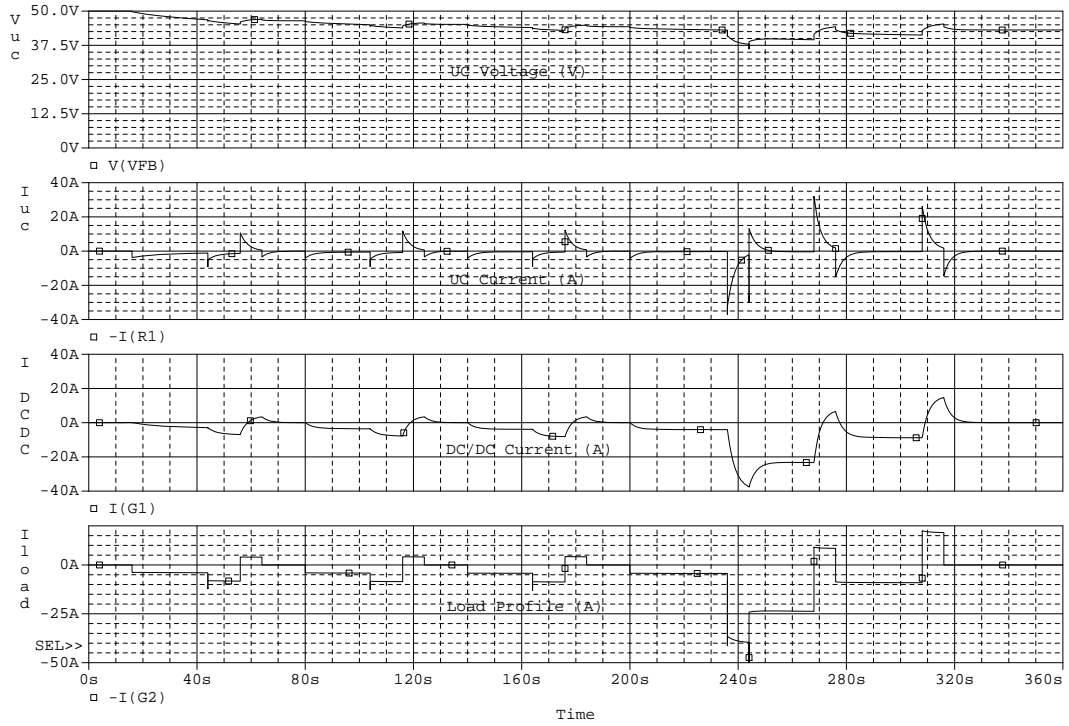


Figure 4.6: Top Level Control performance - UCFL variant

4.4.2 Performance of Control Algorithm

The control algorithm has been tuned for the electric scooter application and with the EV DST load profile. In order to enable a fair comparison, the no of battery and UC cells are kept constant for the BFL and UCFL variants. The system specifications are the same

as those used in Chapter 3. The battery used in the analysis is a Kokam (SLPB75106100) 7.5Ah energy Li-Ion battery which is modeled by a 3.7V voltage source (nominal voltage) and an internal resistance of 5.3mOhm/cell. A Maxwell 350F, 2.5V UC (BCAP0350 E250) is used and is modeled with a 350F capacitor with a ESR of 3.2mOhm/cell. 14 battery cells and 20 UC cells are used in all the variants evaluated in this work.

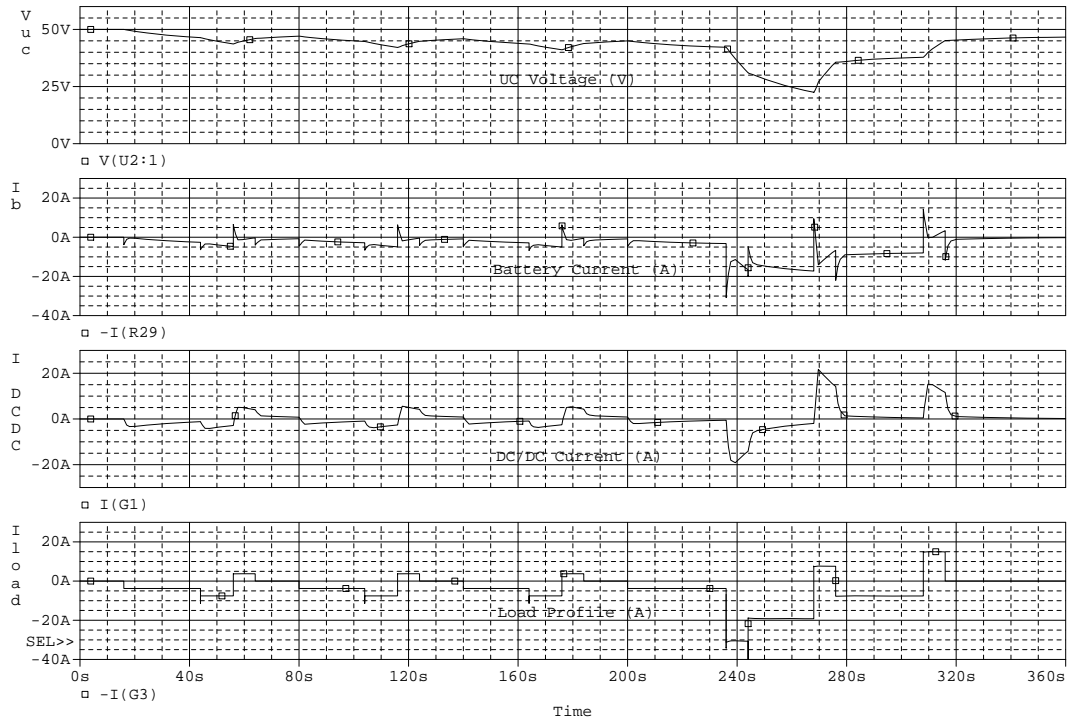


Figure 4.7: Top Level Control performance - BFL variant

UCFL Variant: UC string consists of 20 cells in series with a ESR of $60m\Omega$, battery string consists of 2 parallel strings of 7 cells each with a supply voltage of 25V (ESR $35m\Omega$). The buck-boost topology, limits the source voltage to be lower than the load voltage and hence batteries are in parallel. The operating voltage of the electric scooter is between 38V-50V ($V_{min}-V_{max}$) and hence the UC's are pre-charged to 50V before starting the vehicle. The LPF used to generate (I_{ref}) has a time constant of 2.2 seconds and the voltage scaling factor (V_{sf}) for UC SOC control is chosen to be 2.5. These values were chosen to minimize RMS battery current and to maintain UC voltage between the limits 38V-50V. The performance of this control scheme is shown in Fig 4.6. $I_{b_{rms}} = 13.1A$; $I_{c_{rms}} = 4.30A$; $I_{o_{rms}} = 9.96A$.

BFL Variant: Battery string consists of 14 cells in series and connected to the load (ESR $70m\Omega$). The UC string consists of 20 cells connected in series (ESR $60m\Omega$) and is allowed a voltage swing of 25V-50V ($V_{min}-V_{max}$). As in the previous case, the control loop is tuned to lower battery RMS current and to maintain UC voltage bounds. A time constant of 25 seconds is used for the HPF and a voltage scaling factor (V_{sf}) of 50 for UC SOC control. The performance of this control scheme is shown in Fig 4.7. $I_{b_{rms}} = 5.94A$; $I_{c_{rms}} = 6.49A$; $I_{o_{rms}} = 8.23A$.

Tuning Equivalence: Since the BFL and UCFL topologies have different bounds on the UC SOC, battery RMS current was chosen as the equivalence criterion for tuning the filter. Battery RMS current for the BFL variant is approximately 6A and for the UCFL variant is approximately 13A (twice the current as the BFL variant; because the UCFL battery pack consists of 2 parallel strings with a supply voltage of 25V). This provides a fair basis for comparing the two topologies.

4.5 Design of BFL and UCFL variants

The buck-boost converter topology is identical for the BFL and UCFL variants (Fig 4.1), barring the position of the battery and UC strings. A brief overview of the converter operation is presented below.

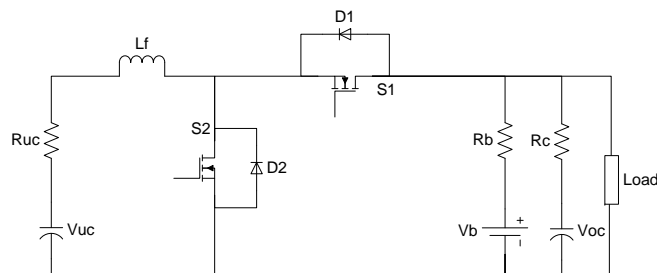


Figure 4.8: Buck-Boost converter (BFL variant)

4.5.1 Overview of Converter Operation

The buck-boost converter as shown in Fig 4.8, works in the boost mode when transferring energy from the UC to battery and buck mode when the energy flow is reversed.

This imposes a limitation that the voltage of the UC bank has to be always lower than the battery bank. Although it is possible to build a converter capable of buck/boost operating mode in both directions of energy transfer, this would add 2 switches and lead to increased losses. The role of the converter (both variants) is to serve as a current source delivering current pulses to the load. Hence the converter is always operated in current limited mode of operation, where the inductor current is directly controlled (using traditional PWM techniques or a hysteresis controller).

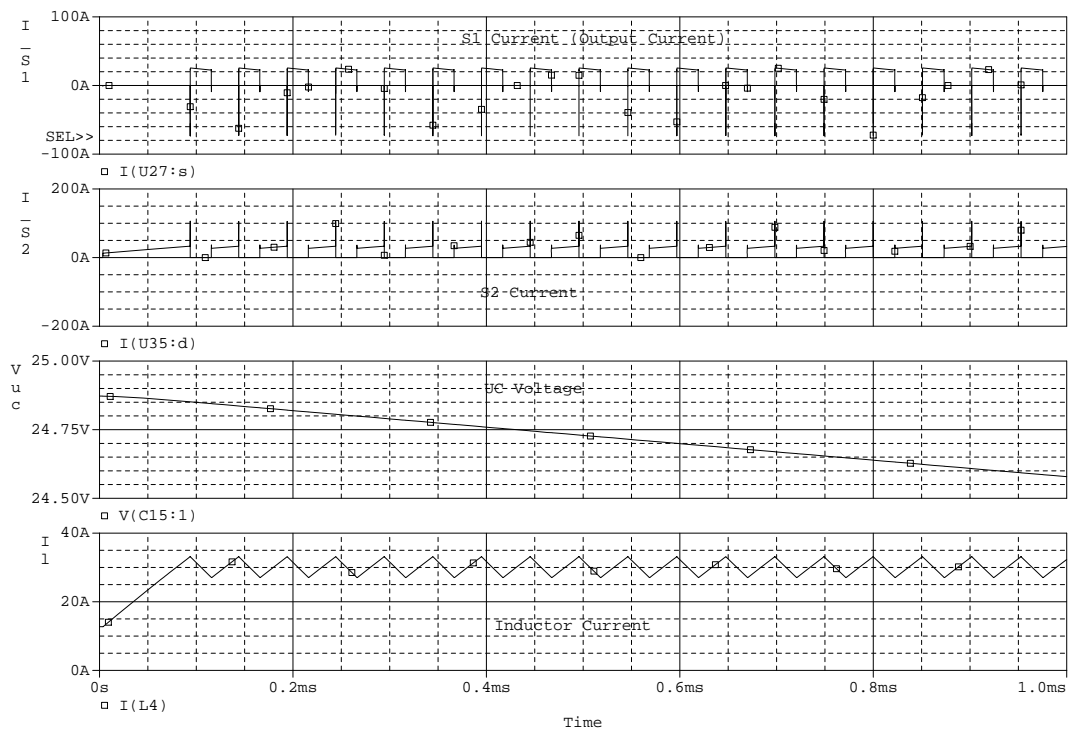


Figure 4.9: Boost Mode of Operation

Boost Operating Mode: In the boost mode of operation, when switch S2 is ON (S1:OFF), current builds up in the inductor (sourced by the UC) and when S1 is On (S2:OFF) the inductor current is delivered to the load. Turning ON S1 during the current delivery to the load, reduces the diode losses. It should be noted the input current (UC current) is continuous, while the output current is discontinuous. The RMS equivalent of the pulsating output current, is given by Eq 4.3; where *Duty* is the duty cycle of the switching sequence, I_l and dI_l are average and ripple inductor currents respectively.

$$I_{dc}c_{rms} = I\sqrt{(1 - \text{Duty})}\sqrt{\left(1 + \frac{1}{3}\left(\frac{dI}{I}\right)^2\right)} \quad (4.3)$$

The critical current and voltage waveforms in this mode of operation are shown in Fig 4.9. The regulated inductor current can be observed, also note that the UC voltage decreases as it delivers energy to the load. The currents through the two switches during the switching sequence are also shown in the figure.

Buck Operating Mode: In the buck mode of operation, when switch S1 is ON (S2:OFF), current builds up in the inductor (sourced by the battery) and when S2 is ON (S1:OFF) the current is delivered to the UC, charging it up. In the buck mode, input current is discontinuous while the output current is continuous. The critical current and voltage waveforms in this mode of operation are shown in Fig 4.10. The regulated inductor current can be observed it is negative to indicate that the current flows in the opposite direction to the boost mode, also note that the UC voltage increases. The currents through the two switches during the switching sequence are also shown in the figure.

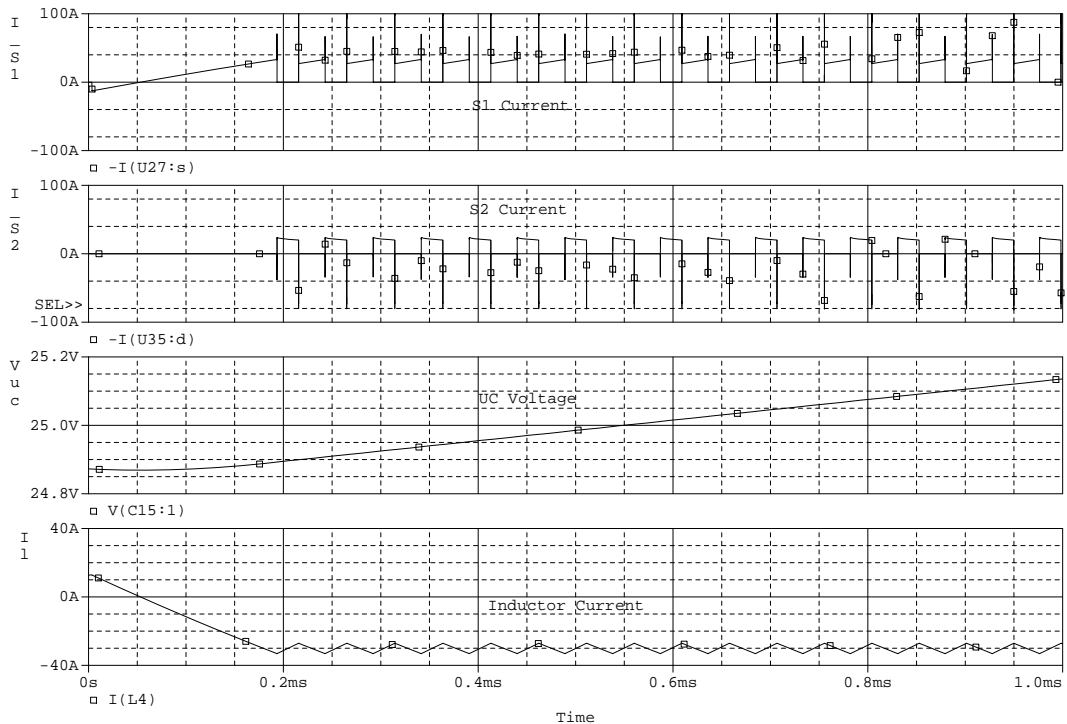


Figure 4.10: Buck Mode of Operation

Thus the 2 modes of operation of the buck-boost converter are presented. Although the operation has been described with respect to the BFL variant, it applies to the UCFL variant as well, except that the battery and UC bank positions are swapped.

4.5.2 Converter Design Notes - BFL and UCFL variants

Several design criterion are influenced by the two topology variants - some of the most important are discussed in Table 4.1.

Table 4.1: Converter Design BFL Vs UCFL

S.No	BFL Variant	UCFL Variant
1	Designed for transient power delivery.	Designed for average power delivery.
2	Fast Transient response required.	Slower transient response.
3	Smaller UC bank possible. Has to be sized to provide worst case transient power demand.	Larger UC bank required - has to support bus voltage and also maintain output voltage between certain bounds.
4	MOSFET/Diode and thermal solution - dimensioned for intermittent operation	MOSFET/Diode and thermal solution dimensioned for continuous operation.
5	Inductor Design - Higher operating currents - higher core saturation flux capacity.	Lower operating currents - lower core saturation flux capacity.
6	Higher switching frequency and smaller inductor for better dynamic response	Lower switching frequency.
7	Poor regen performance.	Better regen performance.

The circuit diagram of the buck-boost topology BFL variant is shown in Fig 4.8, the UCFL variant has the battery and UC string positions swapped. For the purpose of performance characterization, the converter is designed to work in both BFL and UCFL

variants; the inductor design however is different. This allows using the same hardware to test both the topology variants and also the interleaved converter (as shown in a following section). *The components are dimensioned using the boost operation as reference, because this is the mode of operation, the converter spends most of its operating time in.*

4.5.3 Steady State Model

The steady state model is built by applying the small ripple approximation, described in [40]. The steady state analysis helps to select and dimension the components of the buck-boost converter. The Boost mode of operation is considered (Fig 4.8). The voltage across the inductance during the 2 states of the switching cycle (i.e. State1 - SW2:ON,SW1:OFF; State2 - SW1:OFF,SW2:ON) are described in equations 4.4 and 4.5 respectively. Where R_l , R_{uc} , R_b , R_{oc} are the ESRs of the inductor, UC, battery and output capacitance respectively; R_{on} is the 'On' resistance of the MOSFET. V_{uc} and V_b are the voltages of the UC and battery string respectively. I_l is the average inductor current and I_{load} the average load current. Applying the inductor volt-second balance (Eq 4.6), the solution for I_l is obtained (Eq 4.7); where Duty is the dutycycle of the converter.

$$V_{l_{S2OFF}} = V_{uc} - I_l(R_{uc} + R_l + R_{on}) - \left(V_b - \frac{R_{oc}}{R_b + R_{oc}}(I_l - I_{load})R_b \right) \quad (4.4)$$

$$V_{l_{S2ON}} = V_{uc} - I_l(R_l + R_{on} + R_{uc}) \quad (4.5)$$

$$0 = \text{Duty } V_{l_{S2ON}} + (1 - \text{Duty}) V_{l_{S2OFF}} \quad (4.6)$$

$$I_l = \frac{(-1 + \text{Duty})I_{load}R_bR_{oc} + (R_b + R_{oc})((-1 + \text{Duty})V_b + V_{uc})}{R_{oc}(R_l + R_{on} + R_{uc}) + R_b(R_l + (-1 + \text{Duty})R_{oc} + R_{on} + R_{uc})} \quad (4.7)$$

The inductor ripple can be calculated as shown in equation 4.8; where T_s is the time period of the switching cycle, $V_{l_{S2ON}}$ is defined in Eq 4.5 and L is the inductance used. Using equations 4.7 and 4.8, the RMS current supplied by the DC/DC converter can be calculated from Eq 4.9. It must be noted that the output current in the boost converter mode is discontinuous hence the RMS current delivered by the converter, is a function of duty cycle, average inductor current and inductor current ripple. The converter is operated in CCM (Continuous Conduction Mode) during all modes of operation; DCM (Discontinuous Conduction Mode) has the disadvantage of generating higher EMI and stresses on the

switches (CCM and DCM are defined with respect to inductor current).

$$dIl = \frac{Vl_{S2ON}DutyTs}{2L} \quad (4.8)$$

$$Idcdc_{rms} = Il\sqrt{(1 - Duty)}\sqrt{\left(1 + \frac{1}{3}\left(\frac{dIl}{Il}\right)^2\right)} \quad (4.9)$$

Analysis: BFL variant

RMS Current Calculation: Using the model developed in this section, the RMS current which can be delivered by the BFL variant to the load can be calculated as a function of UC voltage and dutycycle (Fig 4.11). Output voltage is assumed to be constant (50V), since the battery string is connected to the rail. The following values are used for this analysis; $Ruc = 60m\Omega$, $Rb = Ruc = 70m\Omega$, $Rc = 6m\Omega$, $Ron = 25m\Omega$. The inductance is $100\mu H$ and switching frequency is $50kHz$. UC voltage is allowed to vary from $25V-50V$. Note that the figure only shows the DC/DC RMS current from $0A-40A$.

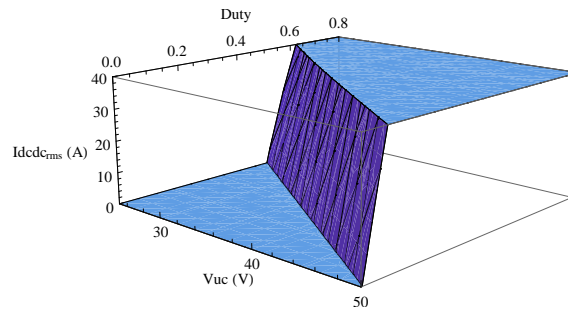


Figure 4.11: $Idcdc_{rms}$ as a function of Vuc and Duty Cycle (BFL variant)

Ripple Current Calculation: It is essential to calculate the maximum inductor ripple current (Eq 4.8), since this is an essential parameter for inductor design. However it should be noted that the DC/DC RMS current output is limited to $40A$. Fig 4.12 shows the inductor ripple current as a function of UC voltage and duty cycle (subject to the $40A$ RMS current limit) for an inductance of $100\mu H$ and switching frequency of $50kHz$. It can be observed that the maximum ripple is $< 1.5A$.

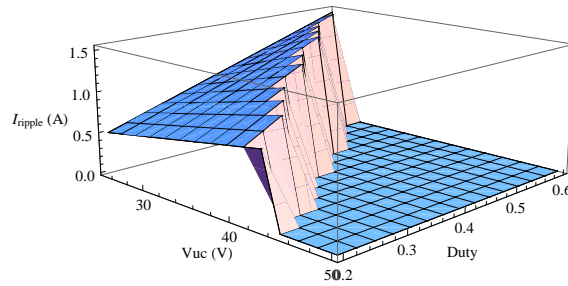


Figure 4.12: I_{ripple} as a function of Vuc and Duty Cycle (BFL variant)

Analysis: UCFL variant

RMS Current Calculation: Similar to the above analysis, the RMS current delivered by the UCFL variant, can be calculated as a function of output voltage and duty cycle (Fig 4.13). Input voltage is assumed constant since it is powered by a battery. Component values are the same except for battery voltage which is 25V (parallel connected string) and hence $R_b = 35m\Omega$. UC voltage (also output voltage) is allowed to vary between 38V-50V. Note that the figure only shows the DC/DC RMS current from 0A-40A.

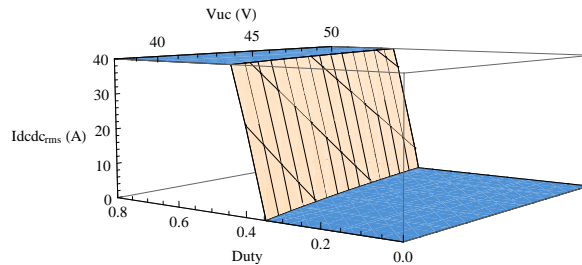


Figure 4.13: $I_{dc_{rms}}$ as a function of Vuc and Duty Cycle (BFL variant)

Ripple Current Calculation: Similar to the ripple current analysis for the BFL variant, Fig 4.14 shows the inductor ripple current as a function of UC voltage and duty cycle (subject to the 40A RMS current limit) for an inductance of $100\mu H$ and switching frequency of 50kHz. It can be observed that the maximum ripple is $< 1.5A$.

The analysis presented in this section can be used to dimension the power components (select voltage & current ratings and estimate losses), the inductance and the cooling solution.

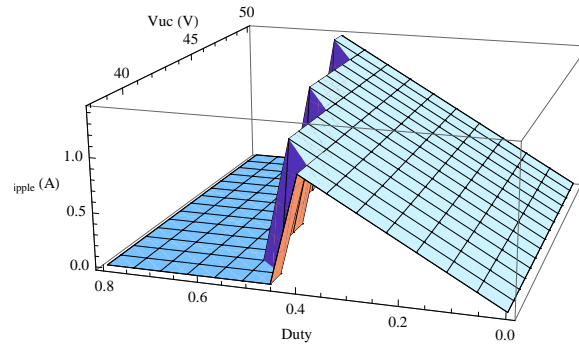


Figure 4.14: I_{ripple} as a function of V_{uc} and Duty Cycle (UCFL variant)

4.5.4 Hardware Design

Performance of the power converter is dependent on component characteristics. The converter design is intended for the electric scooter application and must support implementation of the BFL, UCFL and interleaved converter variants. Because of the need to have a common HW test platform; components are selected to support all variants. A brief description of the component selection process and impact on performance is given below. The complete schematics of the hardware implemented is shown in Appendix A.

MOSFET Selection: The switches S1 and S2 in the buck-boost converter (Fig 4.8) are implemented with MOSFETs. The voltage range in ideal for MOSFET implementation and also EV/PHEV battery pack voltages are around 300V which are suitable for MOSFET switches. MOSFETs provide better performance (switching frequency, losses) compared to IGBTs in this application. The following are the SOA (Safe Operating Area) requirements: $V_{br} > 70V$; $I_{dmax} > 30A$. The choice of MOSFET influences the conduction losses (function of R_{dsON}) and switching losses (function of gate charge and gate drive voltage). In order to allow for reduced switching losses at higher frequency operation, a Logic Level FET ($V_{gs(th)} < 2V@250\mu A$) is chosen. This allows for decreased switching losses in the MOSFET and decreased gate drive losses. Parameters of the selected MOSFET (IRL2910):

- $V_{br} = 100V$ (breakdown voltage)
- $I_{dmax} = 55A$
- Logic Level FET

- $Q_g = 140\text{nC}$ (gate charge)
- $R_{dsON} = 26\text{m}\Omega$ (ON resistance)

Diode Selection: The buck-boost converter is capable of synchronous rectification. However fast diodes are paralleled with MOSFETs in order to prevent overshoot and current ringing from the slow internal MOSFET body diodes. Since the diode does not carry the entire inductor current (the synchronous MOSFET turns ON (S1 or S2 depending on mode of operation), the diode can be sized to carry smaller currents. Parameters of the selected diode (V8P10):

- $I_{fAVG} = 10\text{A}$ (average forward current)
- $V_{RRM} = 100\text{V}$ (max repetitive reverse voltage)
- $V_f = 0.453$
- Fast recovery $< 500\text{ns}$

MOSFET Gate Driver: A standard push-pull driver is used for driving the low-side MOSFET (S2). For the high-side MOSFET (S1), a bootstrap driver is selected because of the need to support high frequency operation. Also since the performance of the system is being measured, the bootstrap driver is an efficient driver. Parameters of the selected gate driver (IR2301):

- High Side - Bootstrap drive
- Low side - Push-Pull drive
- V_{gs} from 5V to 20V - Allows using the LogicLevel FET

Current Sensing: Inductor and load current sensing are required for operating the converter. Both these currents are bi-directional. Hence the current sensing solution must be capable of detecting bipolar currents. A shunt resistor is chosen as the current measuring device; although Hall Effect sensors have the advantage of causing no power loss, resistive sensing was chosen because of its high bandwidth and low cost. However the currents must be measured in the presence of high common mode voltages, hence special high voltage current sensor amplifiers are required to amplify the voltage measured by the current sense

resistor. A $3m\Omega$ current shunt is used which dissipates a maximum of 3 Watts. Parameters of the selected amplifier (AD8210):

- -2V to +65V Common Mode Range
- Gain - 20
- Bandwidth - $450kHz$

Controller: The controller is entirely implemented in digital control. A DSP with special power control peripherals is chosen for this application. Parameters of the selected DSP (dsPIC30F2023):

- High Resolution PWM
- 10-bit ADC @ 2000 (ksps)
- Hardware comparators

Inductor Design: The inductor design is dependent on several factors, primarily:

- Average current
- Ripple current
- Switching frequency
- Core type

These factors can be traded off for size Vs losses Vs cost. Several different core materials are available and an exhaustive inductor design procedure is beyond the scope of this work. Powder cores provided by the company Magnetics were reviewed (Fig 4.15, reproduced from [42]) and are considered for this design. Only toroidal cores are considered. The selection procedure though not optimized provides a guideline for inductor design for the topology variants discussed (BFL, UCFL, interleaved).

Based on the core review and information presented in Table 4.1, the following design choices were made.

- High Flux Core type is selected for the BFL variant since this yields the lowest size and high efficiency for high saturation flux.

	MPP	High Flux	Kool Mu	XFlux
Permeability	14-550	14-160	26-125	60
Core Loss	Lowest	Moderate	Low	Moderate
Perm vs. DC Bias	Better	Best	Good	Best
Saturation (Bsat)	7.5 Kilogauss	15 Kilogauss	10.5 Kilogauss	16 Kilogauss
Nickel Content	80%	50%	0%	0%
Relative Cost	High	Medium	Low	Low

Figure 4.15: Review of powder core types

- MPP core is selected for UCFL variant since this yields lowest size and losses for moderate saturation flux requirements.

An inductance of 100uH is chosen for the design so that the ripple current magnitude is limited to 2A (Fig 4.12 and Fig 4.14). Switching frequency is 50kHz for the BFL and UCFL variants and 100kHz for the interleaved converter (presented in a later section). For the BFL variant, the maximum inductor current is limited to 30A, 20A for the UCFL variant and 15A for the interleaved converter. Based on the design constraints, the UCFL variant uses a MPP core (part no: 55548-A2) with overall wound dimensions of 1.65”x0.78” and the BFL variant uses a High Flux core (part no: 58907-A2) with overall wound dimensions of 3.47”x1.0”. The UCFL inductor is also used in the interleaved converter design, because current requirements are similar. Note that the current limitations imposed on the inductor are with respect to the experimental setup only.

4.5.5 Small Signal Modeling

The small signal model (or AC equivalent model) of the converter is a linearized model of the switching converter at a certain operating point. This model can be used to build a controller for the system. The DC/DC converters discussed in this chapter behave as current sources and hence the quantity to be controlled is the inductor current. Hence the transfer function of inductor current to duty cycle ($TF[s] = \frac{\hat{i}_L}{\hat{d}}$), where TF is the desired transfer function and \hat{i}_L and \hat{d} are small signal inductor current and duty cycle respectively. **Boost Mode:** Using the technique presented in [40] and equations 4.4 and 4.5 the small signal inductor voltage is obtained as shown in Eq 4.10. Where $V_L(t)$ and $I_L(t)$ are inductor voltage and current averaged over one switching cycle and $d(t)$ is the duty cycle. The time

varying quantities can be expressed as the sum of DC quantities and small AC variations as shown in equations 4.11 and 4.12. Where I_L and D are average inductor current and average duty cycle respectively.

$$V_L(t) = L \cdot \frac{d}{dt}(I_L(t)) = d(t) \cdot V_{l_{S2ON}} + (1 - d(t)) \cdot V_{l_{S2OFF}} \quad (4.10)$$

$$I_L(t) = I_L + \hat{i}_L \quad (4.11)$$

$$d(t) = D + \hat{d} \quad (4.12)$$

Using equations 4.10 to 4.12 and ignoring DC and nonlinear terms (product of \hat{i}_L and \hat{d}) the s-domain transfer function of inductor current to duty cycle is obtained as shown in Eq 4.13. Where $Rt = Ruc + Rl + Ron$. Eq 4.13 is defined for the BFL variant but also holds good for the UCFL variant (by replacing Vb with Vuc).

$$TF(s) = \frac{\frac{(-I_L + I_{load})Rb \cdot Roc}{Rb + Roc} + Vb}{-\frac{(-1 + D) \cdot Rb \cdot Roc}{Rb + Roc} - Rt - L \cdot s} \quad (4.13)$$

As expected, it is a single pole system because inductor current is directly controlled. The magnitude of the transfer function is plotted in Fig 4.16 for a BFL variant with $D = 0.5$; $Vb = 50V$; $I_L = 20A$; $I_{load} = 30A$; $L = 100\mu H$; $Ruc = 60m\Omega$; $Rb = 70m\Omega$; $Ron = 26m\Omega$.

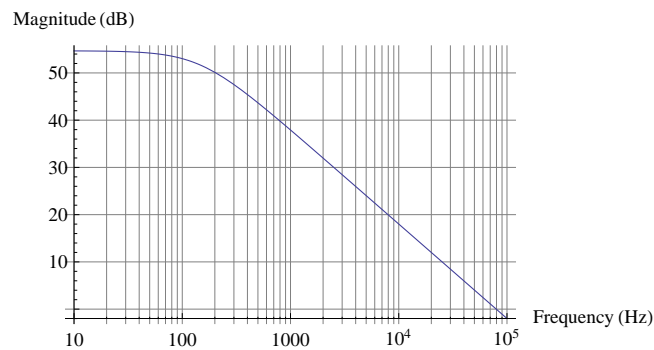


Figure 4.16: Transfer Function of BFL variant

Buck Mode: Using a similar procedure as used for the Boost mode, the transfer function is obtained as shown in Eq 4.14. All the terms have been defined earlier.

$$TF(s) = \frac{-Il \cdot (Rb + 2 \cdot Rt) + Vb}{Rt - D \cdot (Rb + 2Rt) - L \cdot s} \quad (4.14)$$

4.5.6 DC/DC Controller Design

The DC/DC controller is responsible for tracking the current demand generated by the Top Level control as described in Section 4.4. The block diagram of the DC/DC controller is shown in Fig 4.13. Two types of control schemes are proposed; 1. Classic PI control, 2. Hysteresis controller; each control type has its merits and demerits and are described in this section.

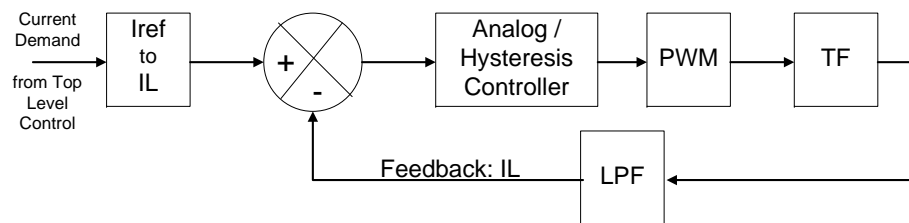


Figure 4.17: Block diagram of the control scheme

Analog Controller

The small signal inductor current to duty cycle transfer function developed previously is used to design the analog controller. The transfer function of the closed loop system with a analog controller is obtained in Eq 4.15. Where $H(s)$ is the current measuring function $TF_{conv}(s)$ and $TF_{cont}(s)$ are the transfer functions of the converter and controller respectively. $T(s)$ is the loop gain of the system and is shown in Eq 4.16 and V_m is the peak amplitude of the sawtooth/triangle wave used for PWM generation. A single pole low pass filter (LPF) is used to filter the inductor current. The controller can be tuned differently for the buck and boost modes of operation. There are no stability issues with this control scheme because the converter transfer function contains only a single pole. The controller has to be tuned such that the controller bandwidth is one-tenth the switching frequency.

$$\frac{\hat{i}_L}{\hat{d}} = \frac{1}{H(s)} \frac{T(s)}{1+T(s)} \quad (4.15)$$

$$T(s) = H(s) \cdot TF_{cont}(s) \cdot TF_{conv}(s) \cdot TF_{LPF}(s)/Vm \quad (4.16)$$

$$TF_{LPF}(s) = \frac{1}{1 + \tau \cdot s} \quad (4.17)$$

Some observations about this control approach are presented below:

- Fixed switching frequency.
- Ripple current amplitude is dependent on frequency.
- UC efficiency decreases with increase in ripple magnitude.
- Inductor has to be sized to keep ripple current within bounds - can be non-optimal.

Hysteresis Controller

This control technique works by limiting inductor current between a window defined by I_{high} and I_{low} . The switches S1 or S2 depending upon the mode of operation are controlled by the hysteresis converter. Hence the ripple current amplitude is always maintained constant at the expense of variable frequency switching. By using simple circuit equations, the switching frequency can be characterized for a certain inductor ripple current amplitude. Fig 4.18 shows switching frequency as a function of inductance and V_{uc} (for BFL) for a ripple amplitude of 2A and average inductor current of 30A. The ripple current restriction of 2A leads to optimal size for inductor design in this case.

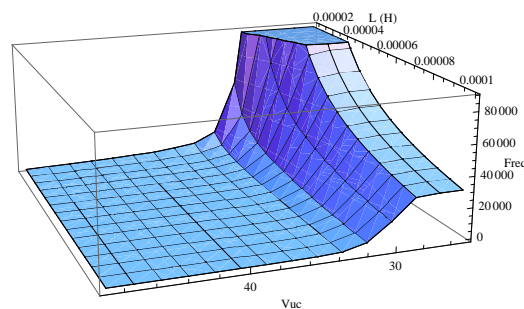


Figure 4.18: Switching frequency (Hz) Vs Inductance (H) and V_{uc} (V) (Ripple current =2A, Inductor Average Current =30A)

Some observations about this control approach are presented below:

- Variable switching frequency.
- Ripple current amplitude is fixed.
- UC efficiency is unaffected.
- Smaller inductor can be used - trade off with higher switching losses.

4.6 Converter Design - Interleaved Buck-Boost Converter

The interleaved converter variant of the buck-boost topology could potentially improve the performance of the BFL variant. Interleaved converters and application have been presented in detail in [43]. A 2-phase BFL interleaved converter is proposed in this work (Fig 4.19) and its performance characterized.

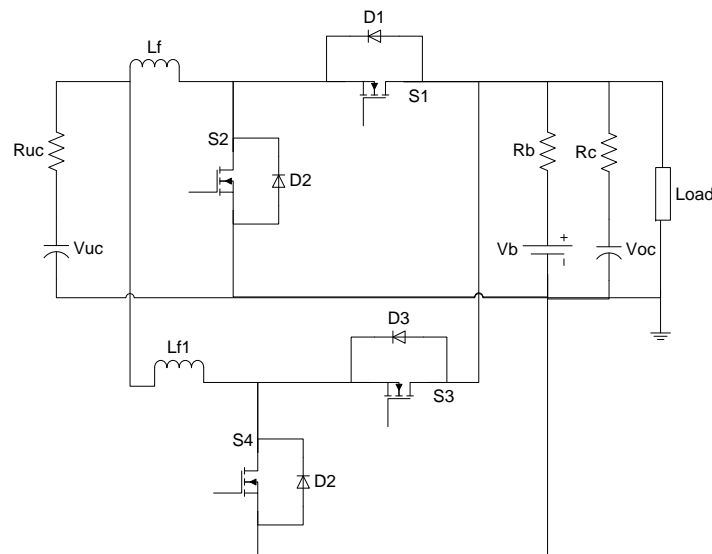


Figure 4.19: Interleaved 2-Phase Buck-Boost converter (BFL)

4.6.1 Overview of Converter Operation

The interleaved converter consists of 2 buck-boost converters (referred to as phases) connected in parallel but connected to the same sources as shown in Fig 4.19. The 2 phases

are identical with respect to their components. The difference arises from the switching sequence which is applied to the 2 parallel converters. Assuming that PWM signals are used to drive the converter, the carrier waveform (sawtooth or triangle) of the respective phases are phase shifted by a certain fixed angle. One of the most common techniques is to use a phase shift of 180° . This has several beneficial effects, primarily reducing the ripple content in the input and output currents. The operating waveforms of the interleaved converter are shown in Fig 4.20. The following can be observed from the figure; the sawtooth reference for the PWM generator is shifted by 180° , the current ripple in the inductor current (boost mode) is lower than the phase current ripple.

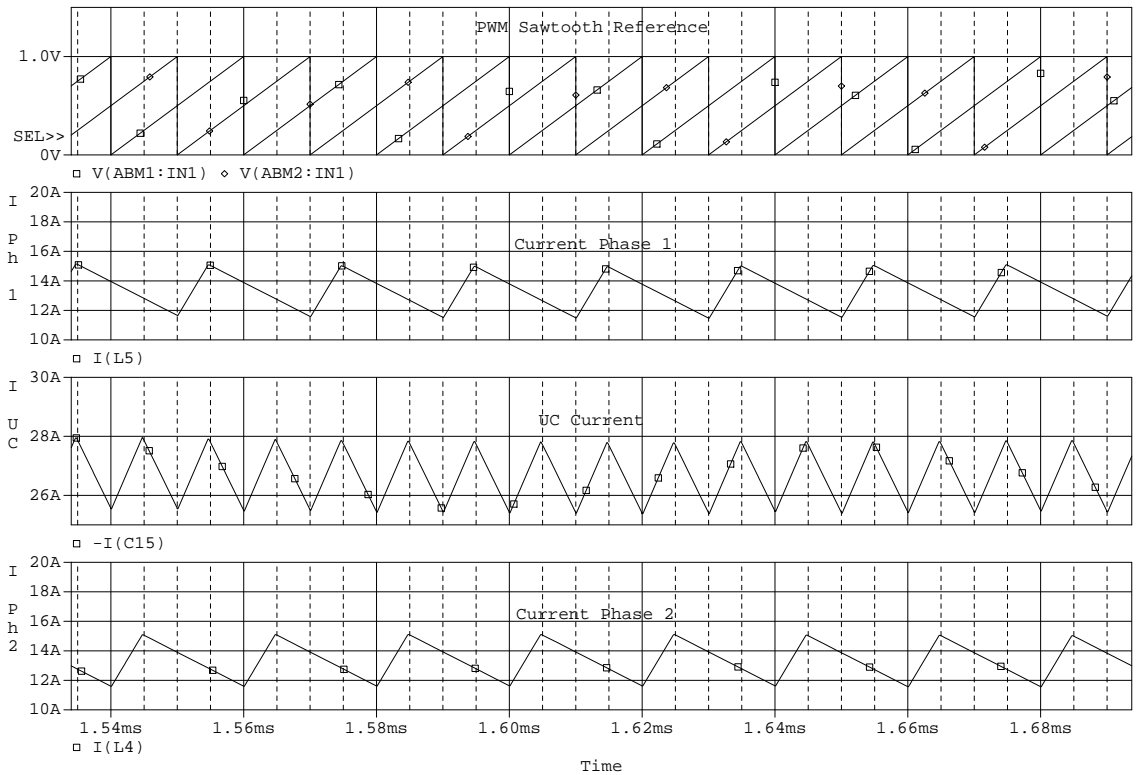


Figure 4.20: Interleaved Converter Operation (BFL)

4.6.2 Why interleaved converter?

There are several reasons why interleaved BFL variant can have better performance, these reasons are listed below:

1. Input Ripple reduction: UC's exhibit a loss of capacity when they are subject to ripple currents at high frequencies. This drop off in capacitance is due to the physical limitation of the charge storage process in the UC. The drop off in capacitance for the BCAP 350F UC used in this work is shown in Fig 4.21. Interleaved converters have lower input ripple when compared to non-interleaved converters - the input ripple current reduction factor (which is the reduction in ripple over a single phase converter) for a 2-phase interleaved converter is shown in Fig 4.22. Increase in number of phases to 3 will reduce the input ripple further (over certain duty cycle range) but increase circuit complexity and losses. So if the UC current is looked as a superposition of a DC component with AC ripple components, using an interleaved converter will lead to improved utilization of the UC. This is achieved due to reduction in ripple.

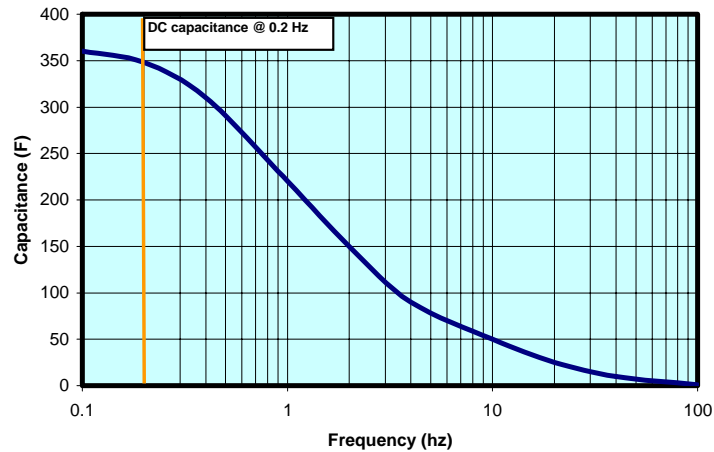


Figure 4.21: Capacitance Vs Frequency behavior (BCAP350), (reproduced from Maxwell UC Guide)

2. Improved efficiency at low power levels: Interleaved converters can improve light load efficiency by load shedding (i.e. one of the phases can be turned off at light load).

3. Improved Transient Response: Interleaved converters operate at higher frequencies than corresponding non-interleaved converters. Hence the transient response is improved. This is an important attribute for this class of applications.

4. Smaller Inductors: Inductor dimensioning is a function of ripple current and average current; interleaved converters have lower average and ripple current per phase and hence this can possibly lead to an overall reduction in inductance size. However two inductors are

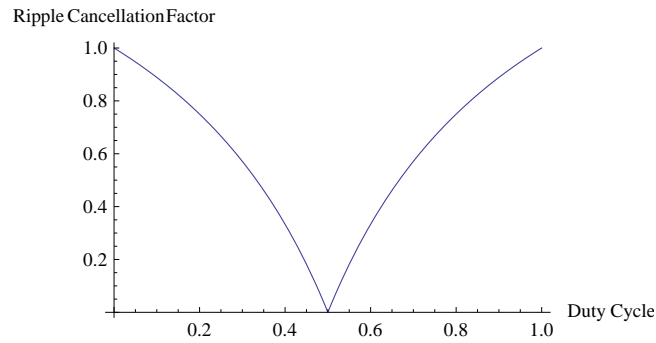


Figure 4.22: Input Current Ripple Reduction Factor, 2 Phase Boost Interleaved Converter

now required instead of one.

4.6.3 Hardware Design

The components selected for the BFL and UCFL variants are also used for constructing the interleaved converter. Although component selection can be optimized for the proposed 2-phase converter, the same hardware was selected to facilitate using a single experimental platform.

Inductor Selection: The inductor design process outlined in the previous section is also applicable for the 2-phase interleaved converter. The inductor selected for the UCFL variant (MPP core (part no: 55548-A2) with overall wound dimensions of 1.65" x 0.78") is reused for the interleaved converter.

4.6.4 Control

The top level control and DC/DC Controller remain the same as detailed in the previous sections (for BFL variant). The only difference is that there are 2 PWM modulators; one for each phase of the interleaved converter and the reference sawtooth waveform to these 2 PWM units are phase shifted by 180° .

The complete schematics of the experimental hardware platform used to verify operation of the interleaved converter (as well as the BFL and UCFL variants) is shown in Appendix A.

4.7 Simulation Results - DC/DC Performance

The goal of the design and testing process outlined in this chapter, is to be able to compare the performance (efficiency) of the converter variants presented. This efficiency information can then be perform a system level simulation. The necessity to employ this approach is because the load profile is 360 seconds in length and it is not feasible to run a full switching model (50-100 kHz) over this time period. The simulations were performed using PSpice in order to analyze the switching behavior of the converter. An example of an simulation model used is shown in Fig 4.23.

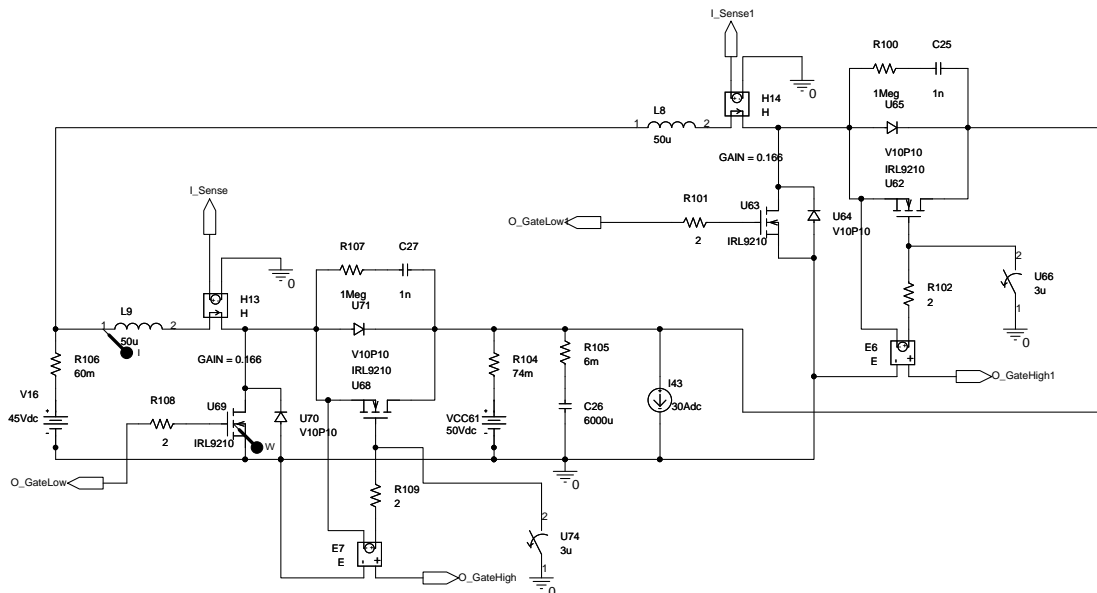


Figure 4.23: Orcad simulation model (BFL interleaved converter)

The efficiencies of the BFL, UCFL and interleaved converter variants and the split up of the losses is shown in Figures 4.24, 4.25 and 4.26 (as function of V_{UC} and I_{ref}) respectively. Inductor losses are not accounted in these simulations and hence a derated value for efficiency; 95% is used for all system level simulations.

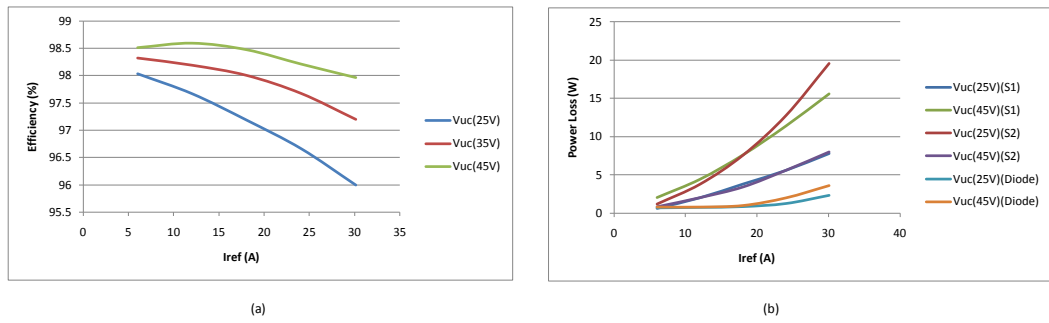


Figure 4.24: BFL variant (a). Efficiency (b) Loss breakdown

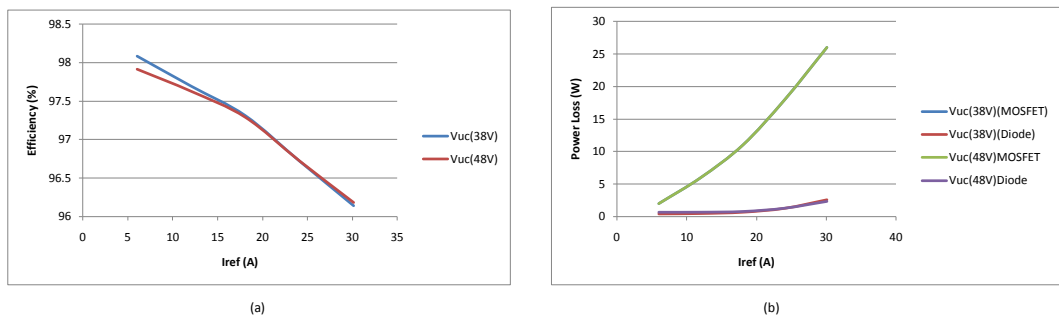


Figure 4.25: UCFL variant (a). Efficiency (b) Loss breakdown

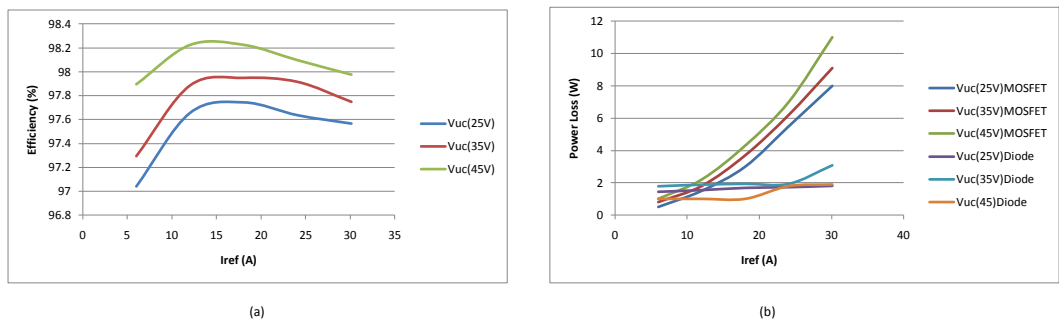


Figure 4.26: Interleaved variant (a). Efficiency (b) Loss breakdown

4.8 Simulation Results - System Level

System level simulations were also performed using PSpice, using a tuned top level controller presented in an earlier section and modeling the DC/DC converter as an controlled current source with an efficiency of 95 %. The performance of the BFL variant is shown in Fig 4.27; $DC/DC\text{Losses} = 14.74W$; $UCESR\text{Losses} = 2.82W$; $BatteryESR\text{Losses} = 2.33W$; $BatteryPeakCurrentReduction = 1.78$.

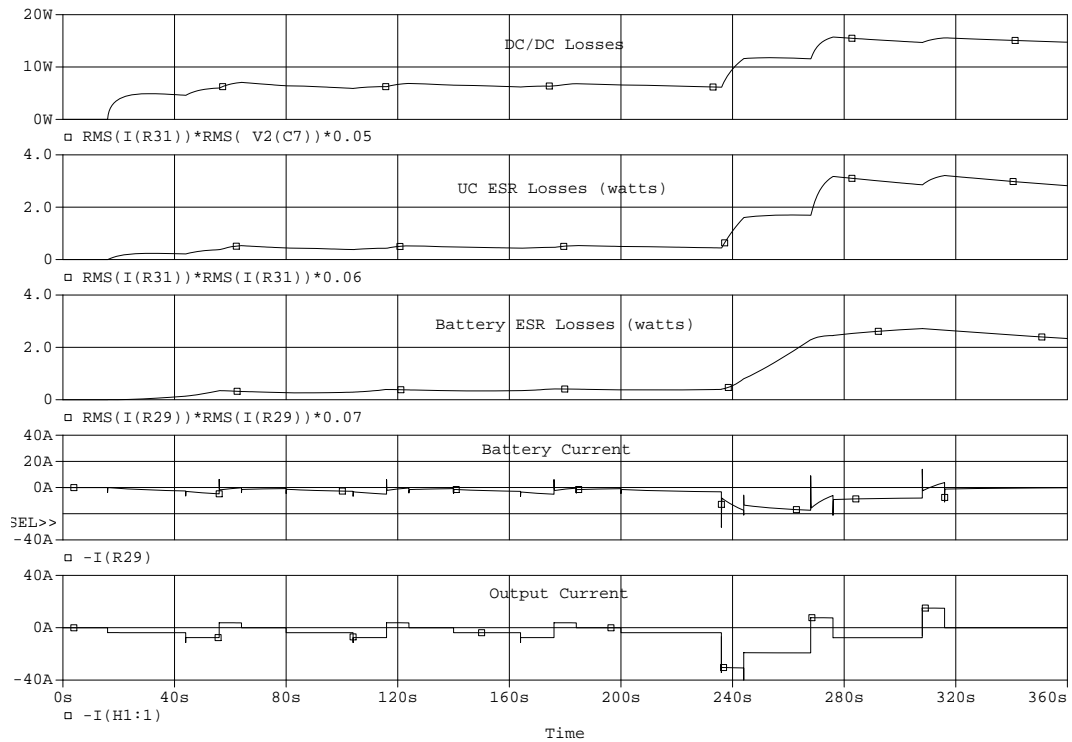


Figure 4.27: System Level Simulation (BFL Variant)

The performance of the UCFL variant is shown in Fig 4.28; $DC/DC\text{Losses} = 19.5W$; $UCESR\text{Losses} = 1W$; $BatteryESR\text{Losses} = 3W$; $BatteryPeakCurrentReduction = 1.33$.

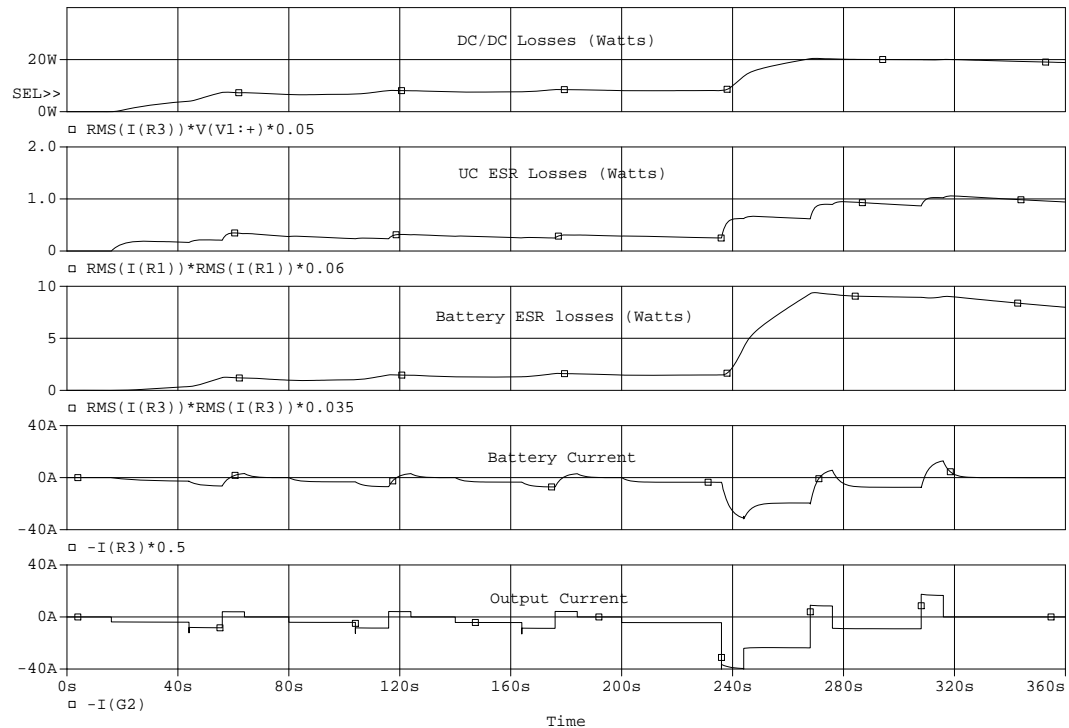


Figure 4.28: System Level Simulation (UCFL Variant)

4.9 Experimental Setup

The hardware setup built to verify proper operation of the converters designed in the chapter is shown below. The hardware is finally intended to be mounted inside the electric scooter, with a hybrid pack. Features of the hardware:

- Supports implementation of BFL, UCFL and 2-phase interleaved BFL variants.
- 16-bit DSP processor.
- Operating voltage from 18V 70V
- Current sensing of all inductor currents and load current. (3x Current Sense).
- Voltage sensing of all supplies.
- Supports logging of data via serial port.

- Off board inductor for flexibility in changing inductances.

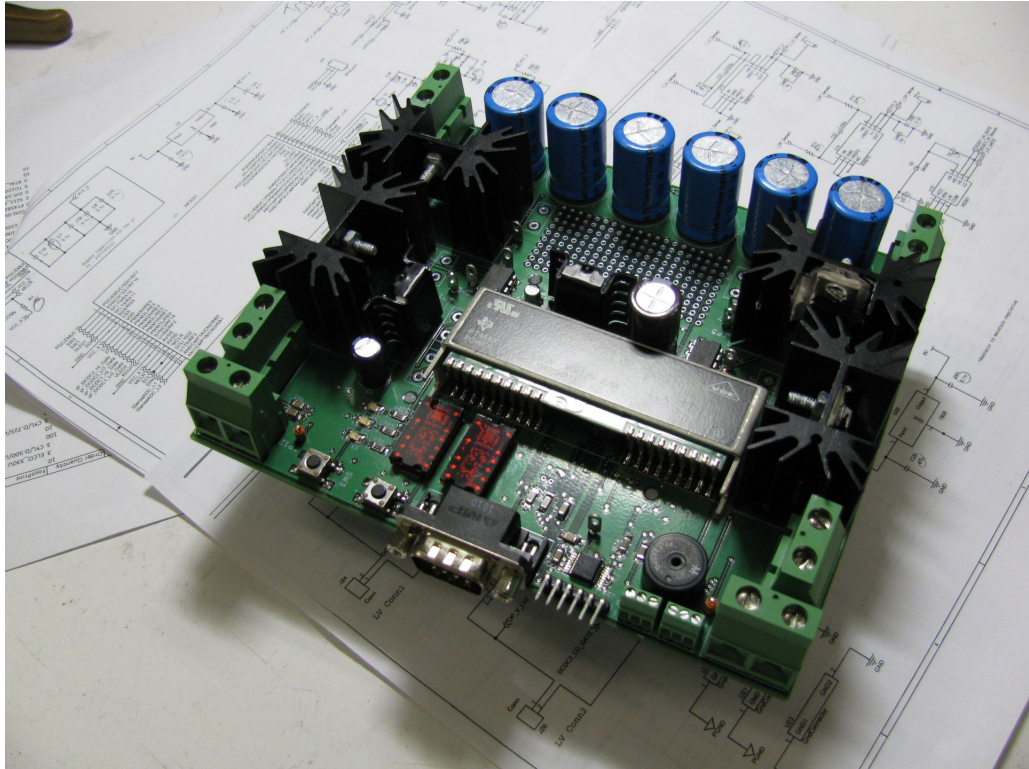


Figure 4.29: Experimental Hardware for verification of converter operation

A description of the experimental test setup and results from experiments are presented in [44].

4.10 Summary

A new test platform has been presented for performance characterization of active and passive HESS systems. The design and performance of 3 variants BFL, UCFL and interleaved converter were presented. Based on the material presented in this chapter, the following inferences can be made about the performance of the active HESS topologies discussed:

- Reduction in battery RMS currents is achieved.

- Reduction in battery peak currents is achieved.
- Better utilization of UC energy is achieved.
- The BFL variant has better performance over the UCFL variant.
- Performance of the DC/DC converter is the major deterrent for implementing active HESS topologies.

5

A Novel Scheme for Optimal Paralleling of Batteries and UCs

5.1 Introduction

Several HESS topologies have been presented in chapters 3 and 4 and their performance evaluated. The new HESS topology presented in this chapter attempts to combine batteries and UCs with a simple technique (which does not need high power DC/DC converter blocks) and finding new methods for utilizing the UC. The objective is to provide for robust operation (due to the decreased complexity), while at the same time utilizing the additional cost of the UC in an optimum fashion.

5.2 Review of Cell Balancing

Series connected battery cells exhibit variations because of manufacturing tolerances and operating conditions. The weakest cell in the pack can then limit the performance of the pack [45]. In order to fully utilize the capacity of series connected battery cells, it is desirable to keep them balanced at all times. A variety of methods has been reviewed in [46] and includes several dissipative and non-dissipative techniques. Of particular interest is a technique proposed in [47] which uses series connected string of capacitors to perform the balancing process (charge shuttling). Fig 5.1 shows the use of a capacitor to transfer charge between batteries B1 and B2. The same principle can be extended to a series battery string

containing multiple cells.

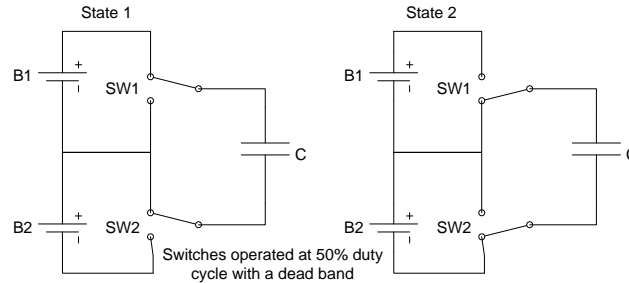


Figure 5.1: Cell Equalizing using a capacitor for Charge Shuttling

The balancing current is a function of the difference in voltage between the batteries, switching frequency (toggling frequency of SW1, SW2), the value of the capacitor and the resistances in the current path. The balancing time can then be calculated as show in Eq 5.1. Where %Difference is the difference in the stored charge between the batteries and $I_{balance}$ is the balance current.

$$BalanceTime(h) = \frac{\%Difference \cdot Capacity(A - h)}{I_{balance}} \quad (5.1)$$

5.3 Proposed Topology

Fig 5.2 shows a simplified block diagram of the system. A three battery system is used as an example (the length of the string can be extended) to explain the operation of the system. The system consists of a battery string and an UC string. B1, B2, B3 can either be independent battery cells or a set of cells. Similarly with UC1 and UC2 which are ultracapacitors with a voltage rating greater than the battery cells. For example if B1 is a 12V pack than UC1 is a 20V UC pack. There is a controller for the whole system.

The switches SW1-SW3, SW_Batt, SW_UC and SW_UC LO are controlled by the controller. The controller also measures the voltages across all the cell elements and also the currents through the inductor L1 - L2. These are used to make decisions regarding the operation of the circuitry. The batteries and the UC strings perform like two parallel strings but without the disadvantages of direct parallel connection (they can be decoupled by SW1-SW3 in middle position). The following modes of operation are possible with the

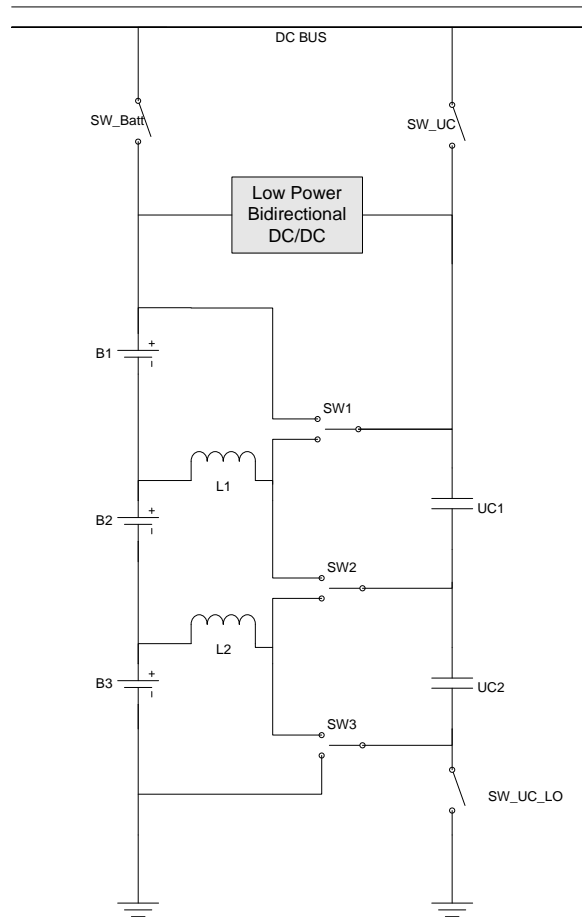


Figure 5.2: Proposed Battery/UC System

new system:

1. High speed dynamic cell balancing: A modified technique based on the capacitive charge shuttling approach is employed in this scheme. Switches SW1-SW3 are toggled between their two states to achieve this.
2. UC or Battery Source Selection: The scheme allows the UC, the battery or the parallel combination (of UC and battery) to be connected to the load. The three possible configurations are shown in Fig 5.3. SW1-SW3 are off.
3. Charge transfer to UC (Method 1): The equalization mechanism also leaves the UC's charged at close to battery voltages. Hence an equalization sequence can be initialized during normal operation of the system to charge up the UC's. In addition the inductors L1-L2

(which are also used for current limiting) are used to implement a boost converter, which allows the UC's to be charged to greater than battery voltages. More information on the operation of the boost converter is provided in the following section.

4. Bi-Directional Energy transfer between Battery and UC: The low power bi-directional DC/DC converter (refer Fig 5.2) allows for energy transfer from battery to UC and vice versa. This arrangement allows the State of Charge of the UC to be dynamically changed during operation and also allows for customized operations which could be useful for certain applications. For example recovering the stored energy in UC before a vehicle shuts down.

5. Diagnostics: The voltages of the batteries and UCs and the inductor currents measured during the equalization process, can be used to determine the State of Health of the individual cells or sub-packs in the battery pack. This allows the pack health to be dynamically monitored and weak cells/ sub-packs can be identified.

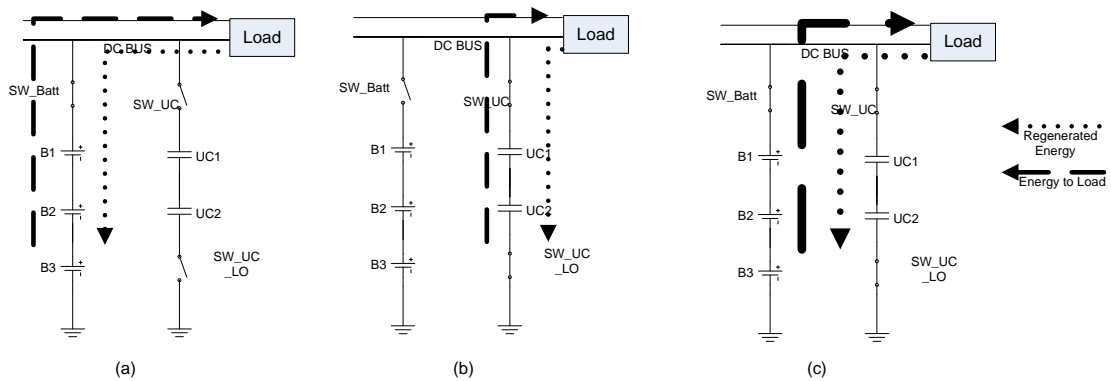


Figure 5.3: Proposed Battery/UC System

5.4 Some Implementation Specifics of the System

5.4.1 Suggested Switch Implementation

A proposed implementation of the system is shown in Fig 5.4. MOSFETs are suitable for switch implementation because of the low voltages involved (cell/pack voltages) and have the benefit of low cost. Also low voltage MOSFETs have lower on-state resistance (for a standard die size) and have low switching losses. The MOSFETs which are used for cell balancing can be rated for lower current and breakdown voltages. The MOSFETs

used to implement SW_Batt, SW_UC and SW_UC_LO should be high voltage MOSFETs (IGBTs can be considered for voltages higher than a few hundred volts).

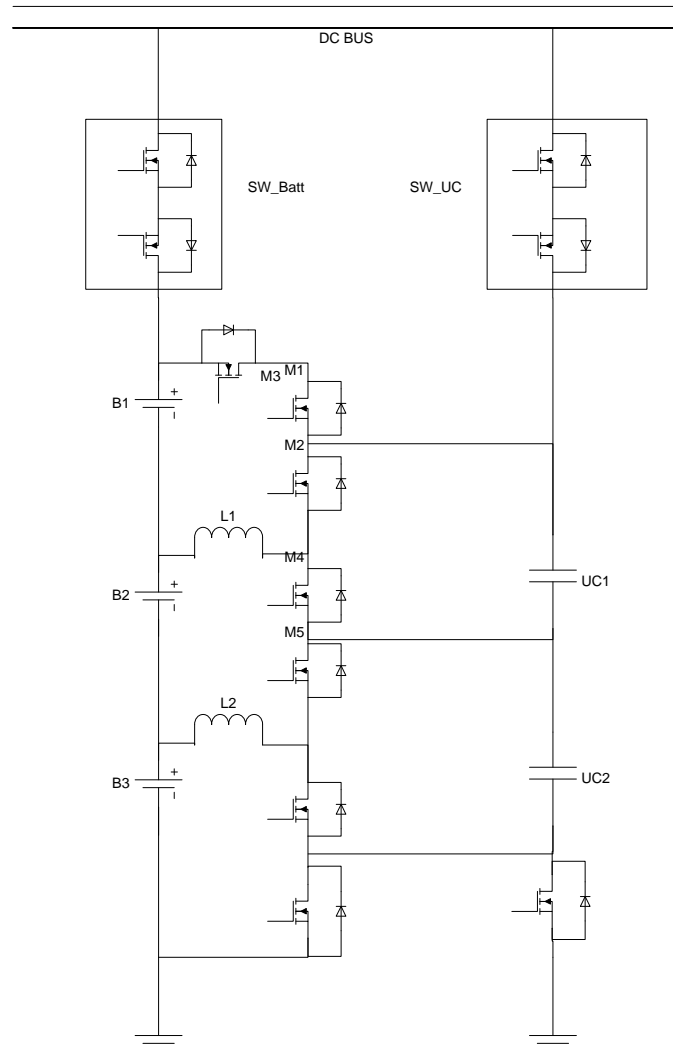


Figure 5.4: Suggested Switch Implementation

The MOSFETs M1 and M2 implement the cell equalization switch. M3 is required if the UC string voltage is higher than the battery pack voltage, it is required in every equalization circuit, where there is a possibility of the UC string voltage at each level exceeding the battery voltage at the corresponding level.

5.4.2 Cell equalization with the proposed structure

Cell equalization is performed by toggling between the top MOSFETs (M1, M4) of the equalization circuit and the bottom MOSFETs (M2, M5) with a dead band in between. The effectiveness of the capacitive charge balance technique [47] can be measured by the charge transported between the cells. The balance current can be shown to increase with increase in transfer capacitance (C_{eq}) as shown in Eq 5.2.

$$I_{balance} = C_{eq} \cdot \delta V \cdot f \quad (5.2)$$

Using ultracapacitors gives the advantage of faster balancing which can be performed during both charge and discharge phases. Fundamental to the use of UCs for charge equalization is to limit the inrush current into the UCs when they are connected across a nearly fully charged battery. This problem is addressed in the proposed solution by two methods:

Method 1: Using a current transfer inductance to limit current - inductors L1-L2 serve this purpose. The dead band between the two phases is used to dissipate the energy in the inductor. Fig ?? shows the action of the transfer choke and the inductor reset action.

Method 2: This involves charging up the UCs to a safe voltage value which then coupled with the ESRs of the batteries, UCs and the resistance of the switches limits the current to an acceptable value. The pre-charging can be performed with the low power DC/DC converter.

5.4.3 Modified bootstrap driver for driving equalization MOSFETs

Bootstrap drivers are best suited to drive the equalizing n channel MOSFETs for reasons of switching frequency and cost. A modified bootstrap driver is presented (Fig 5.6), which allows for recharging the bootstrap capacitor without high power dissipation in the recharge circuit. M1 and M2 are part of the modifications which effectively decouple the bootstrap capacitor C_{bst} from the source of the power MOSFET. This allows bootstrap drivers to be used for this application. In the regular case, the high voltage at the source of the MOSFET, prevents its usage.

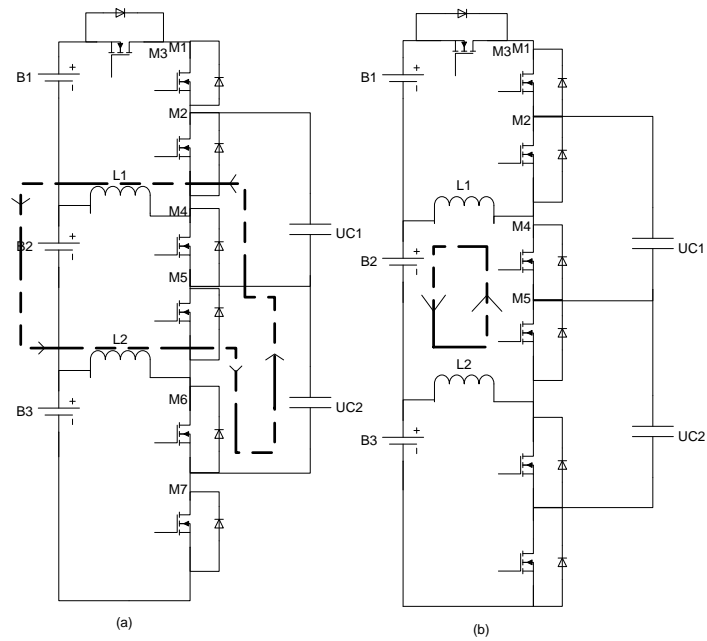


Figure 5.5: Transfer inductance action. (a) L1, L2 help limit inrush current (M4, M6: ON)
 (b) L1, L2 reset during dead band (M4, M6: OFF)

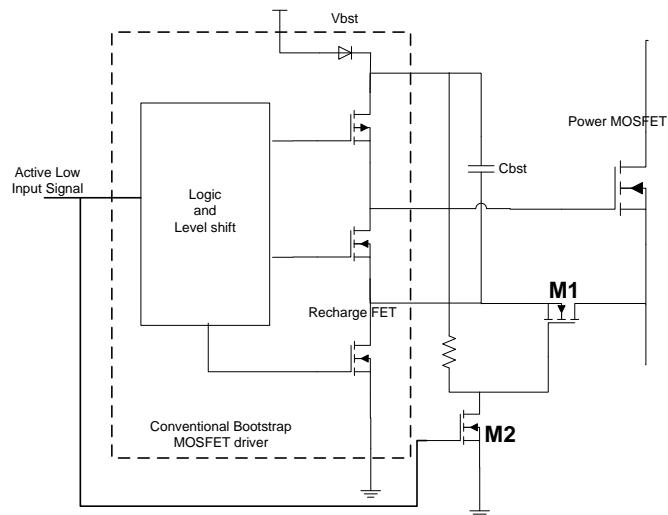


Figure 5.6: Modified Bootstrap MOSFET driver circuit

5.4.4 Boost converter utilizing the current limit inductors

A boost converter can be implemented at a cell level utilizing the current limit inductor. The feasibility of this converter depends on the value of the inductor used for current limit. The boost converter action is shown in Fig 5.7. Consecutive equalizing cells cannot be active as a boost converter at the same time.

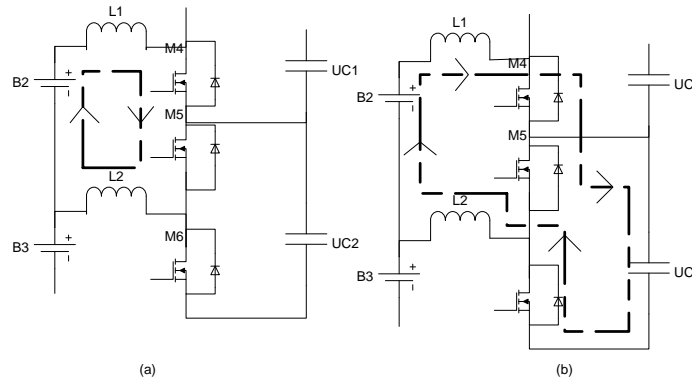


Figure 5.7: Boost converter operation. (a) L1,L2 charged (M4, M5 : ON) (b) L1,L2 discharged into UC2 (M4, M6 : ON)

5.4.5 Low Power Bi-Directional DC/DC converter

The bidirectional DC/DC converter allows charge transfer between the battery and the ultracapacitor. The architecture of the converter is shown in Fig 5.8. V_{batt} is the voltage across the battery string and V_{uc} is the ultracapacitor string voltage. A current control loop is used which limits the current across the inductor and also monitors the voltages to ensure desired levels are reached. The converter (bi-directional) functions as a buck converter when the source voltage is greater than the load voltage and switches to boost mode with the load voltage is greater than the source voltage. In a real application the DC/DC is sized taking into account the application demands (for power transfer). This converter is not intended for high power transfer.

5.4.6 Using the system in a traction application

The advantage of the system proposed is the simplicity of the architecture and the flexibility of directly accessing the battery and the ultracapacitor. An optimal algorithm

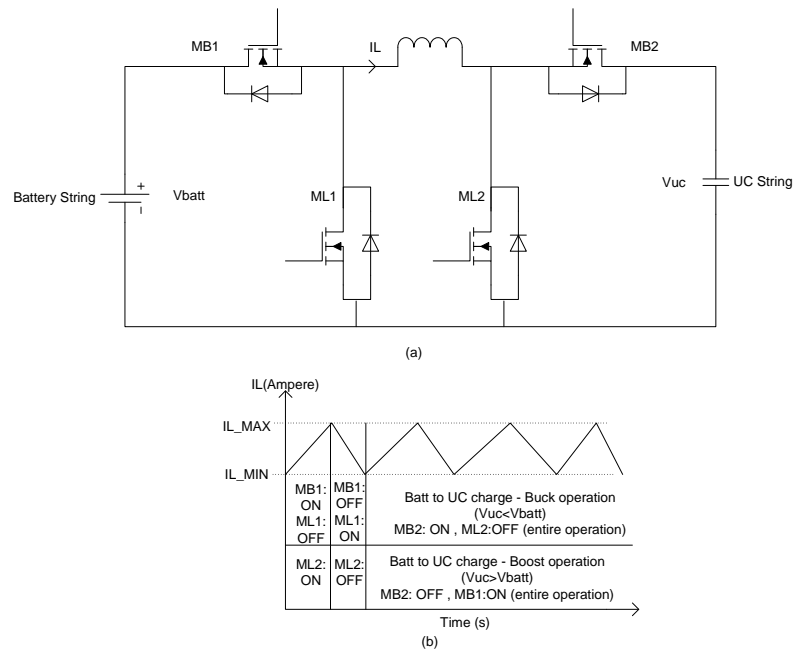


Figure 5.8: Bidirectional DC/DC converter. (a) Architecture of the converter (b) Current limited operation of the converter

has to swap the sources such that the battery handles the average power demand and the ultracapacitors handle the spikes in power demand and the State of Charge of the ultracapacitor is maintained by the regenerated pulses. Work on an optimal usage algorithm is currently in progress. The suggested operation of the system for a simple power profile is shown in Fig 5.9.

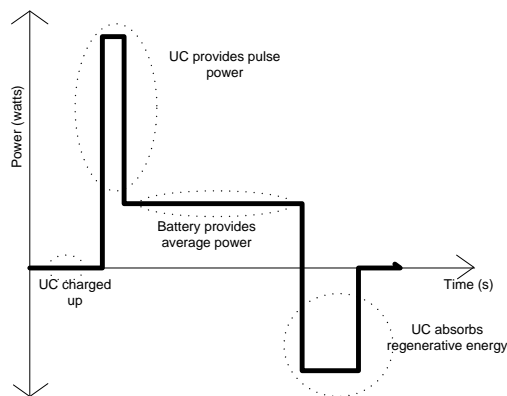


Figure 5.9: Suggested system operation for a simple power profile

5.5 Simulation Results

Matlab/Simulink and PSPICE simulations were used to verify if the circuit operation confirmed to design. Some of the important results are presented below.

5.5.1 Balancing process and effect of current limiting inductor

The circuit as shown in Fig 5.4 is simulated with the battery modeled as a 10F capacitor and the UC modeled as a 1F capacitor. The switching frequency for the equalizing process is 500 Hz. The internal resistances are modeled as equivalent series resistors with the total resistance of the path being 20 mOHM. VB1, VB2 and VB3 are the 3 batteries with starting voltages 3.6 V, 3.9 V and 3 V respectively. The UCs are precharged to 3.5 V. The transfer inductance is 50 uH. The results of the simulation are shown in figures 5.10 and 5.11.

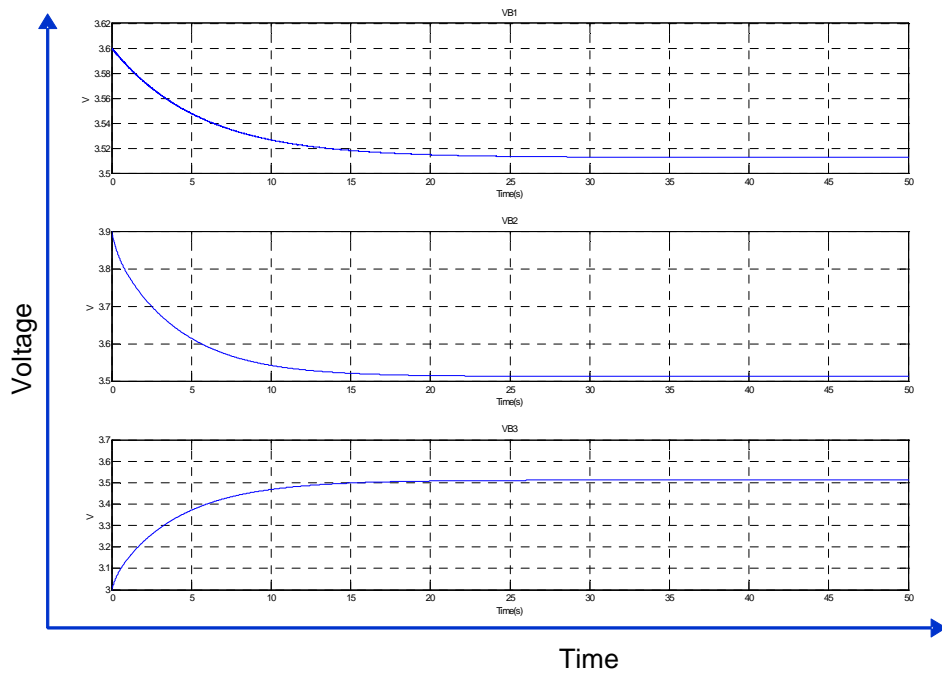


Figure 5.10: Battery voltages during cell balancing

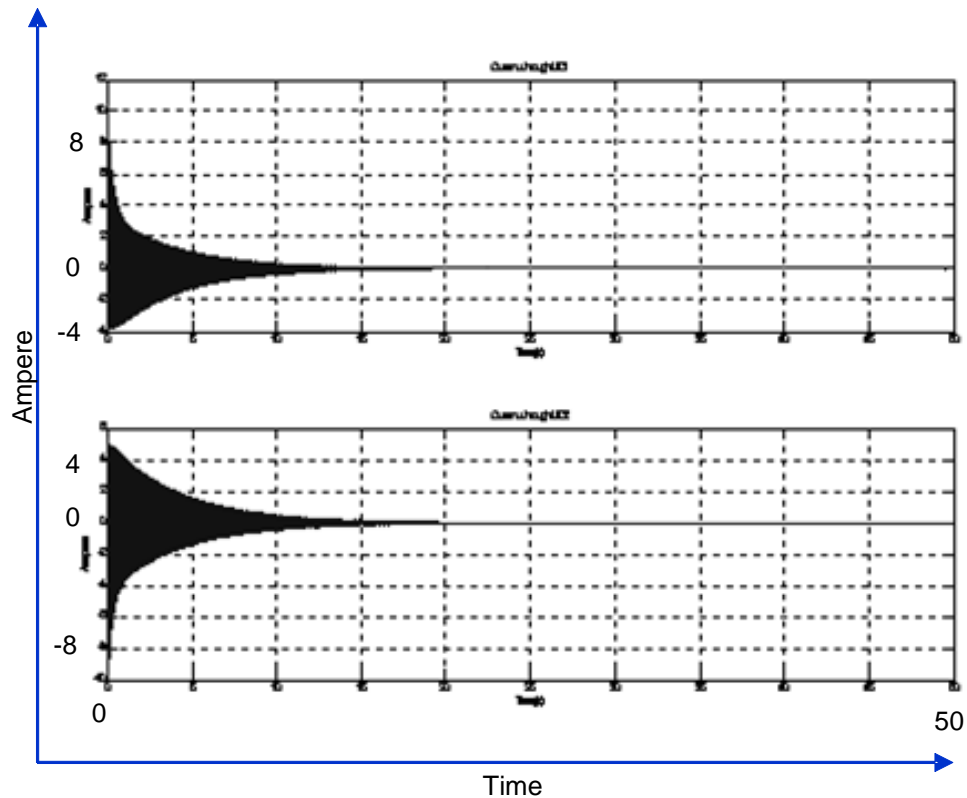


Figure 5.11: UC currents during cell balancing - effect of the inductor in limiting current

5.5.2 Performance of the modified bootstrap circuit

PSPICE was used to simulate a bootstrap driver with the proposed modifications. The power dissipated in the recharge MOSFET and current limit resistor is used as the index for comparison. Fig 5.12 shows the power dissipated in the bootstrap capacitor recharge circuit. All other circuit values remain the same.

5.5.3 Performance of the boost converter using current limit inductors

The method of utilizing current limit inductors as a boost converter (as shown in Fig 5.7) is simulated. The boost converter is current limited with hysteresis control on the inductor current. In this simulation the limits are between 10 A and 20A. The inductance value is 50uH. Results are shown in Fig 5.13

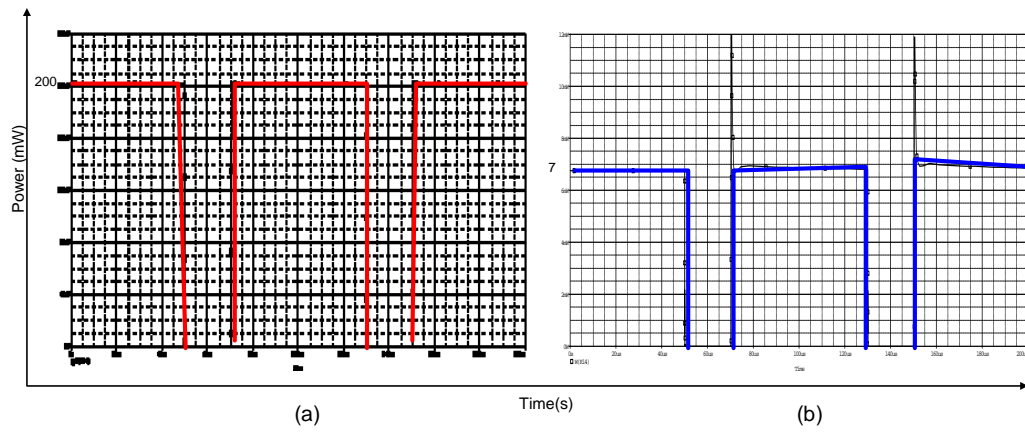


Figure 5.12: Power dissipated in the recharge circuit (a). 200mW (original Bootstrap driver) (b). 7mW (modified Bootstrap driver)

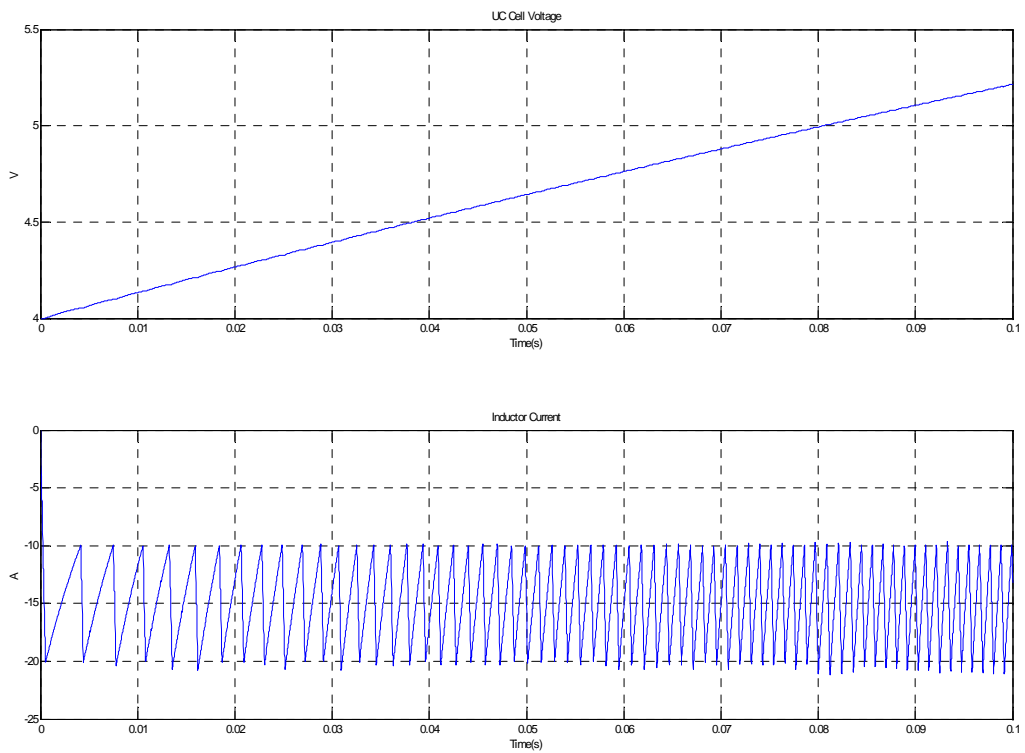


Figure 5.13: Boost Converter Operation

5.6 Conclusion

Several new techniques like using UC for cell equalization, a modified MOSFET bootstrap driver, boost converter with current limit inductor and a DC/DC converter topology have been presented. Further work on an optimal algorithm for driving the system for traction applications and dimensioning values for an optimal power pack are required to evaluate performance of this topology from a system perspective.

6

Design and Development of a Battery Management System

6.1 Introduction

A BMS (Battery Management System) is required for almost all applications using Li-Ion batteries. The most common functions performed by a BMS are listed below:

1. State Of Charge (SOC) monitoring.
2. Over/Under voltage protection.
3. Over current protection.
4. Over temperature protection.
5. Cell balancing

These functions are very critical for applications utilizing Li-Ion batteries; the chemistry being particularly sensitive to over/under voltage and over temperature. The block diagram of a typical BMS is shown in Fig 6.1 (reproduced from [48]).

A BMS system was designed to support the experiments on HESS and is presented in this chapter. This system [49] was jointly developed by the author and Mr. Mathew King.

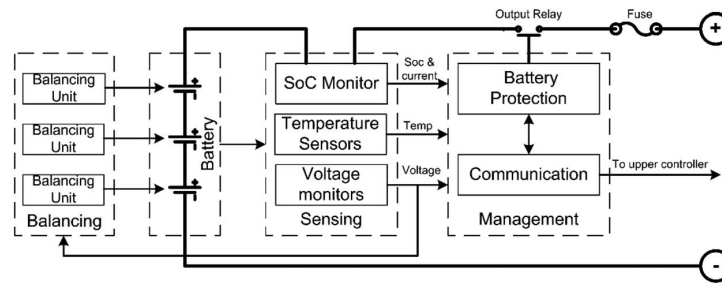


Figure 6.1: Typical BMS system

6.2 Design Specifications

The system overview of the battery pack, instrumented with the BMS is shown in Fig 6.2.

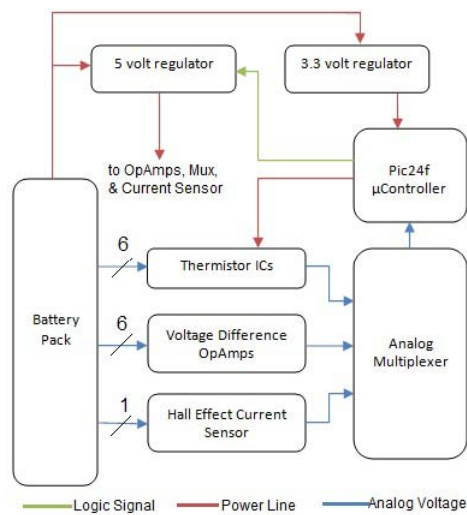


Figure 6.2: Battery pack interfaces with BMS

The specifications of the BMS system are listed below:

- Operating Voltage Range (powered by measured battery pack): 6V-30V.
- Average current consumption of <math><200\mu\text{A}</math> (comparable to self-discharge rate of battery pack).

- Differential Voltage Measurement (12-bit ADC) : 6 channels (can monitor 6 typical Li-Ion batteries).
- Current Measurement (+/- 100A, 12-bit ADC) : 1 channel.
- Temperature Measurement ($-40^{\circ}C$ to $+125^{\circ}C$) : 7 channels.
- Sampling Time: 20ms hours (for 1 set of samples of all channels).
- Storage : SD/MMC card.
- Communication interfaces:
 - 1 UART non-isolated, for direct data logging to the PC and for configuration.
 - 1 UART isolated, for chaining multiple BMS boards.
 - 1 I2C for multi-board systems.
- Real Time Clock and Calendar.
- Digital Outputs:
 - 2 configurable digital outputs for error detection/protection.
 - 2 configurable status LEDs.
 - 2 General Purpose IO (GPIO).
- Digital Inputs:
 - 2 configurable switches (e.g. for mode selection).
 - 2 General Purpose IO(GPIO).
- CPU: Must support SOC algorithm complexity and logging functions.

6.3 Hardware Design

The major challenge in the design of the BMS system is the quiescent power consumption requirements. One of the goals of the BMS is long term monitoring of the battery pack and hence the monitoring system should not significantly impact the SOC of the battery being monitored.

The low power consumption requirement is achieved by a combination of component selection, powering on/off peripherals selectively and using an intelligent software system. The block diagram of the hardware implementation is shown in Fig 6.3.

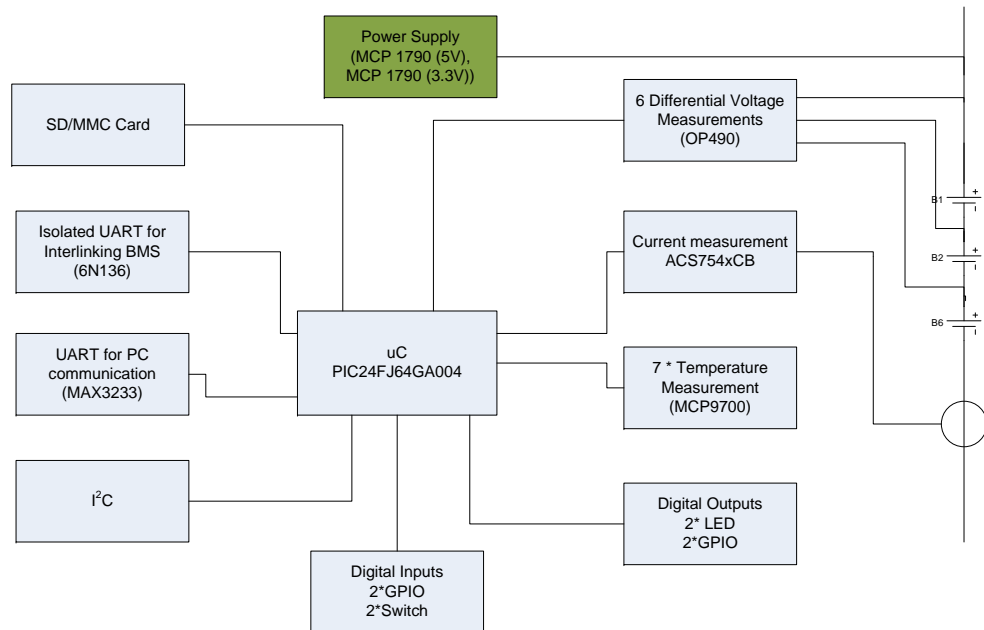


Figure 6.3: Battery pack interfaces with BMS

The BMS board developed is shown in Fig 6.4, the dimensions of the board are 3" x 3". The complete schematics of the hardware are shown in Appendix B.

6.4 Software Control

The highlights of the control strategy are listed below:

- A scheduler is used to implement the control strategy.
- All Non-Essential Hardware is turned off between samples when the board is in low power mode.
 - SD Card, Temperature Sensors, OpAmps, Current Sensor, UART line driver, and 5 volt accessory supply.

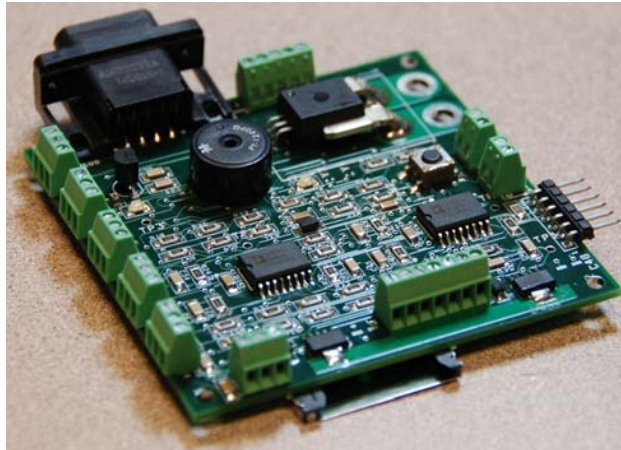


Figure 6.4: BMS system circuit board (3" x 3")

- Writes to the SD Card are limited and performed every 10 samples.
- During Sleep, all modules are powered off and the board draws 3.4 A.
- During Sampling, when modules are all modules are powered on, the board draws 2.2 mA.
- Dynamic sampling rate (based on rate of change of current) to increase samples when desired (e.g. transients) and also to conserve energy during static operation conditions.

The flowchart of the software implementation is shown in Fig 6.5 (reproduced from [49]).

6.5 Application Examples

The BMS system developed, has been used to instrument a Li-Ion battery pack containing 14 cells in series. This requires 3 BMS boards which are linked via the isolated optical communication interface. The instrumented battery pack is shown in Fig 6.6.

The BMS system was also used to monitor the electric scooter battery pack voltage and currents (Fig 6.7) ; this data was used to analyze the power demands of the scooter and to develop control strategies.

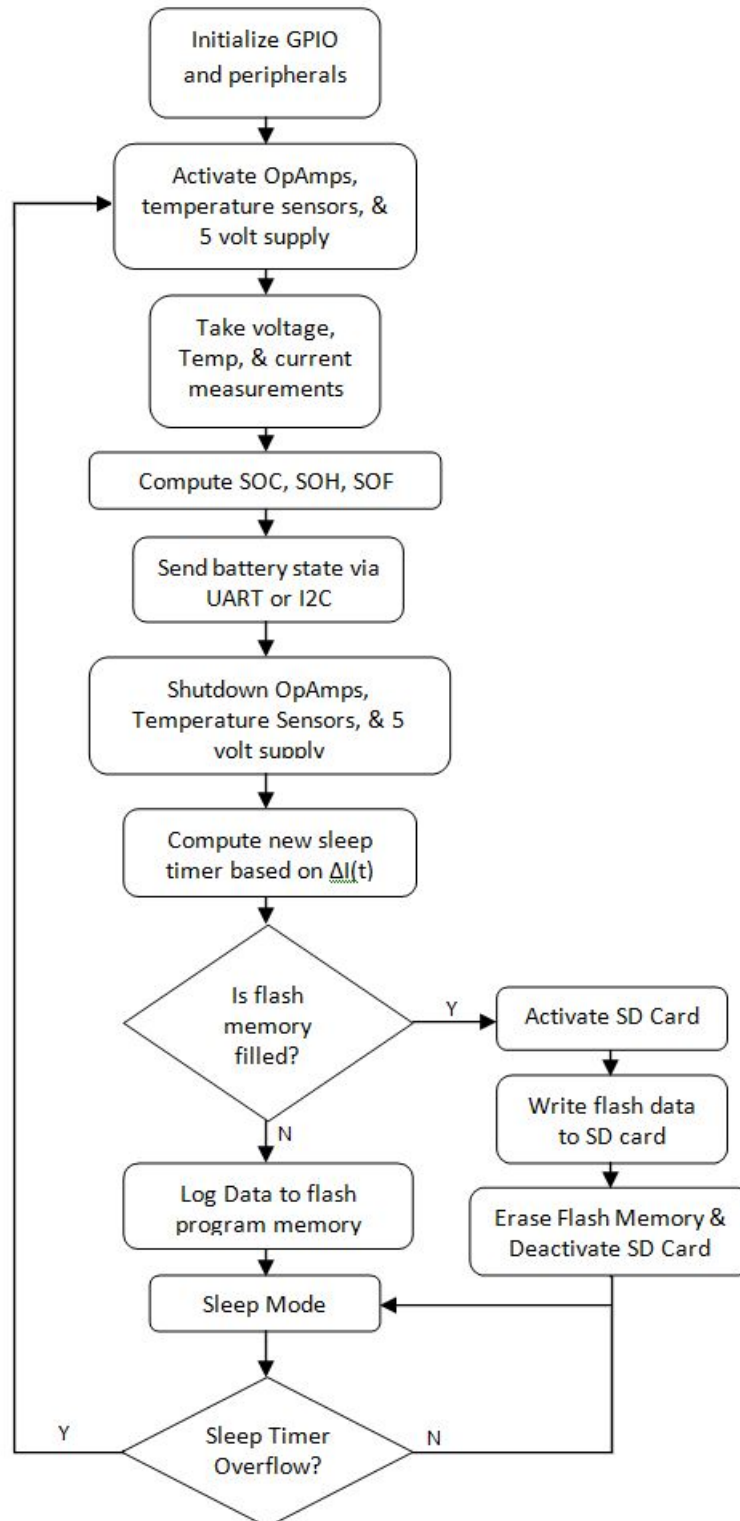


Figure 6.5: Flowchart of software implementation

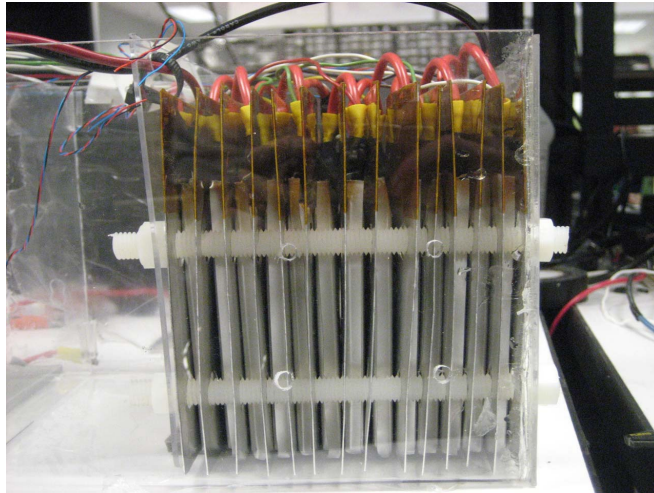


Figure 6.6: Li-Ion battery pack for the electric scooter, instrumented with 3 BMS boards

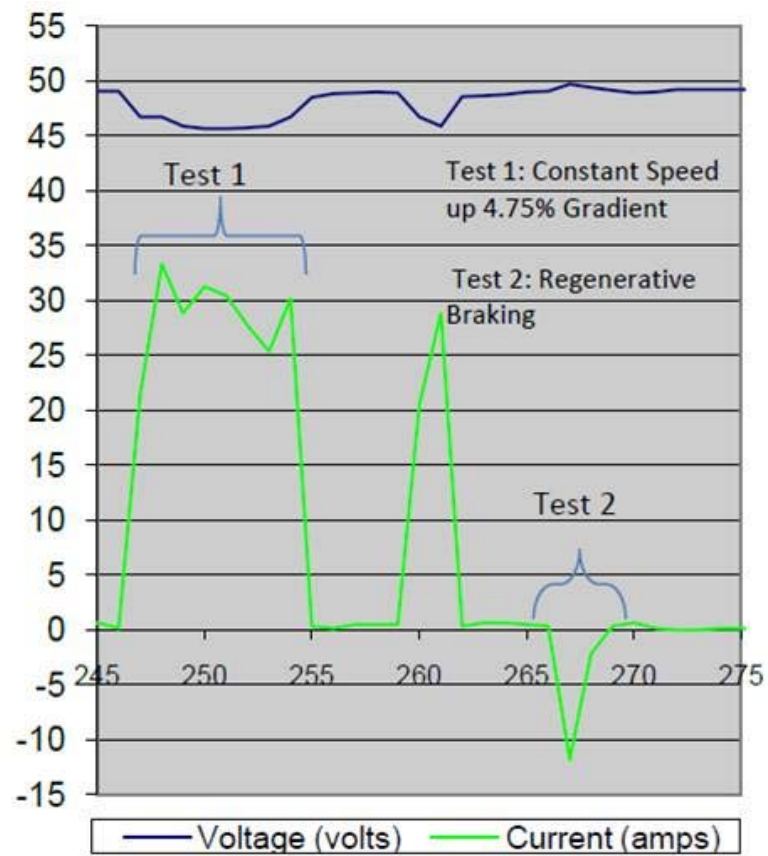


Figure 6.7: EV Scooter battery pack - Voltage and Current profiles

6.6 Conclusion

Thus a versatile tool has been developed to meet the research needs for implementing HESS systems as well as to facilitate battery modeling research. This BMS design provides a platform which can be used with a variety of applications and has scope for expansion.

7

Conclusion and Future Work

Several HESS topologies have been discussed in this work. The primary focus of this work was to analyze the merits and demerits of significant active and passive HESS topologies. New topology variants have also been proposed. This information can serve as design inputs in the selection and dimensioning of HESS topologies for a target application.

It has been demonstrated that passive HESS topologies (direct parallel and parallel with inductance) have limited scope with consideration to the recent generation of Li-Ion batteries and UCs because of their internal impedances being in the same order of magnitude. The UCs are poorly utilized.

The classic buck-boost converter provides a robust active HESS solution, its advantages being low-component count, flexibility and simple control. A novel contribution of this work (Chapter 4) has been defining clearly the 2 major variants (BFL and UCFL) of this converter and discussion their merits and demerits. Also a systematic method for dimensioning and control have been presented. Further performance improvements can be achieved by using interleaved buck-boost converter. A lot of scope for future work exists including characterizing the system level performance of the variants proposed (for e.g. system loss analysis of UCFL variant driving an AC induction motor) and to understand the impact of the HESS on the improvement in battery life and mass reduction. This work will be carried out in the near future.

A novel topology (Chapter 5) has been proposed which allows for the UCs to be used for balancing the battery pack in addition to serving as a source swapping type HESS. This approach to HESS implementation can have benefits for certain class of applications

and has the advantage of simplicity and hence reliability. Further research needs to be conducted to evolve an control strategy and to analyze system level performance (loss analysis, life time analysis etc).

A BMS system (Chapter 6) was required to perform experiments with HESS and also to assist research in battery modeling. Such a system was conceived, designed, built and used in several experiments. The platform can also be expanded to meet new requirements (for various battery pack requirements).

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Appendices

APPENDIX A

The schematics of the experimental board built to demonstrate operation and verify performance of the Buck-Boost and Interleaved Buck-Boost converter is presented in this appendix.

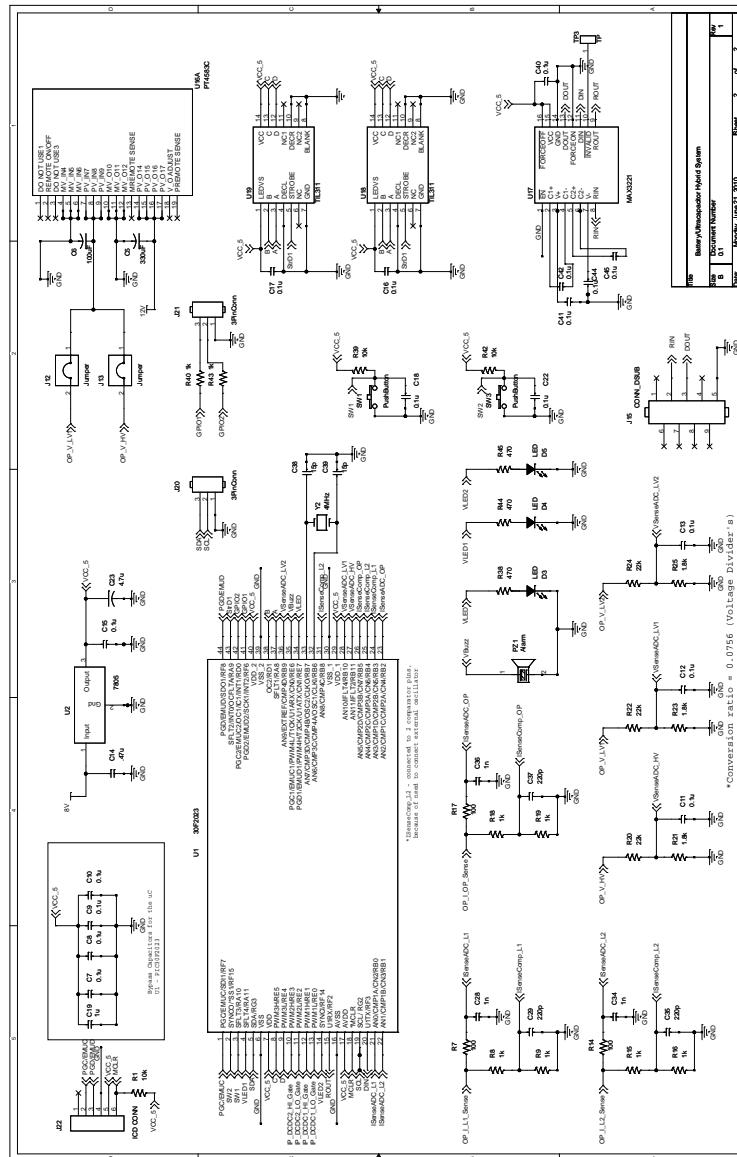


Figure .1: Schematics page Buck-Boost converter control and user interface

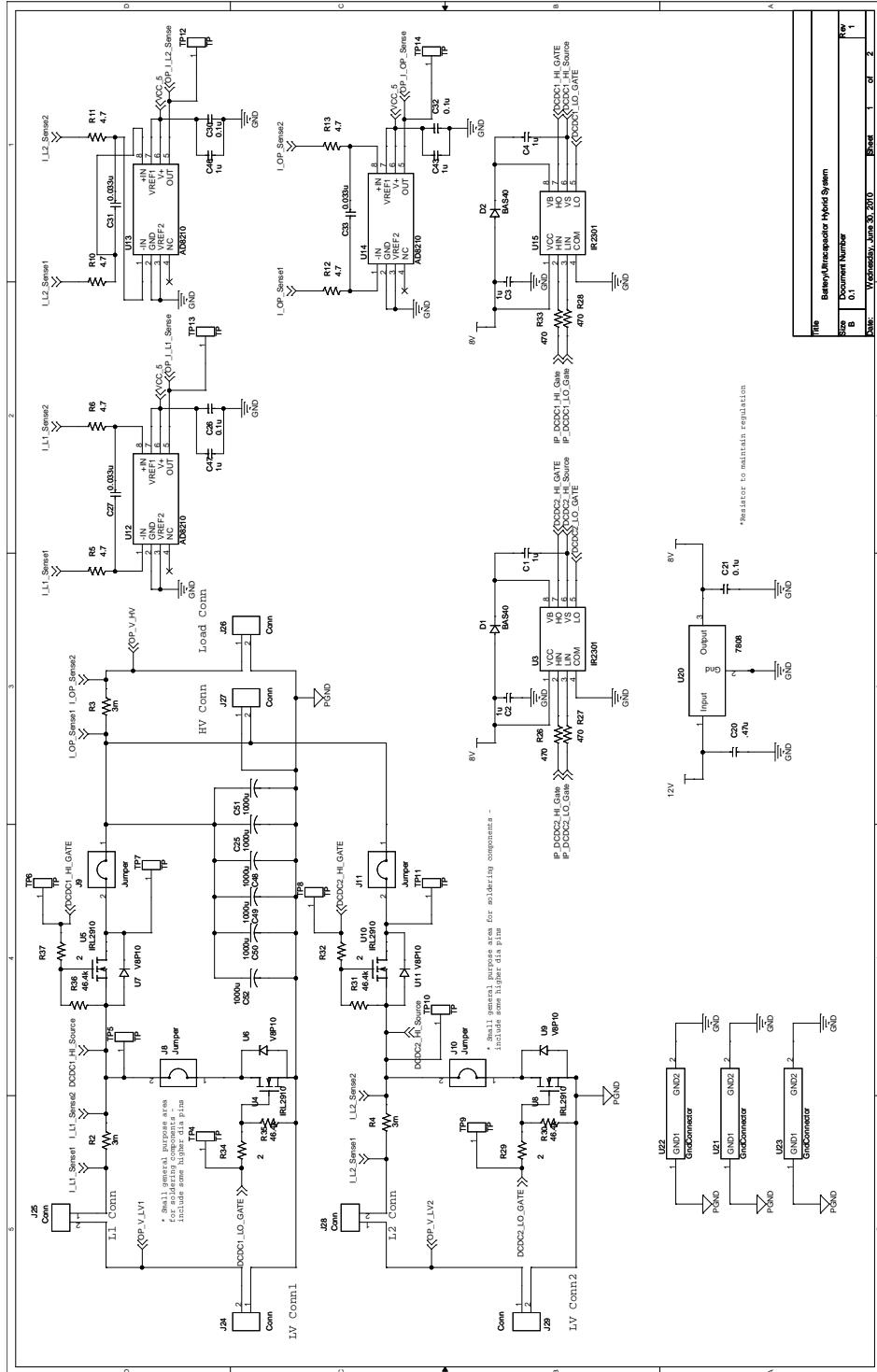


Figure .2: Schematics page Buck-Boost converter power and sensing

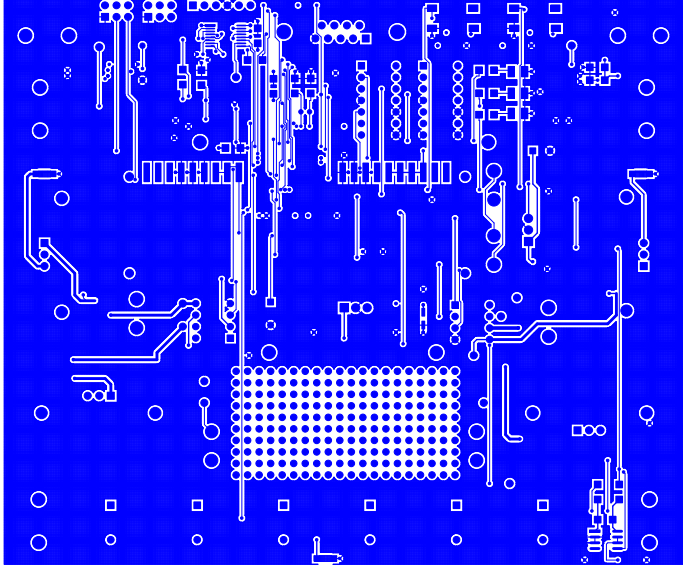


Figure .3: Buck-Boost converter Top Layer Layout

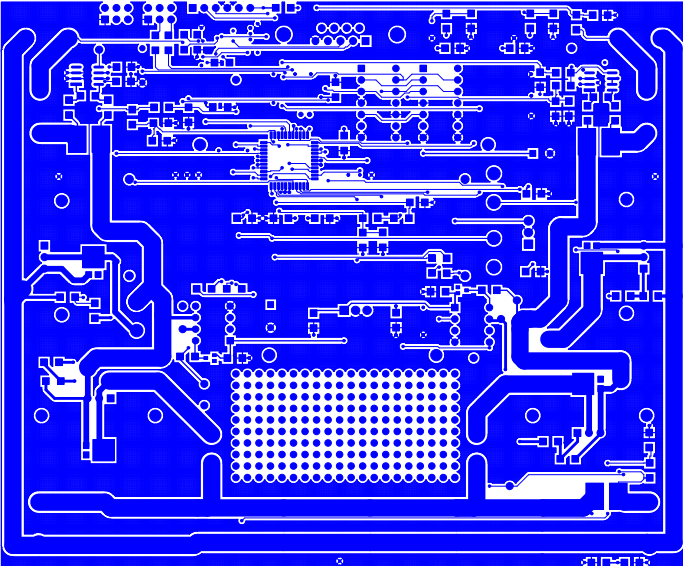


Figure .4: Buck-Boost converter Bottom Layer Layout

APPENDIX B

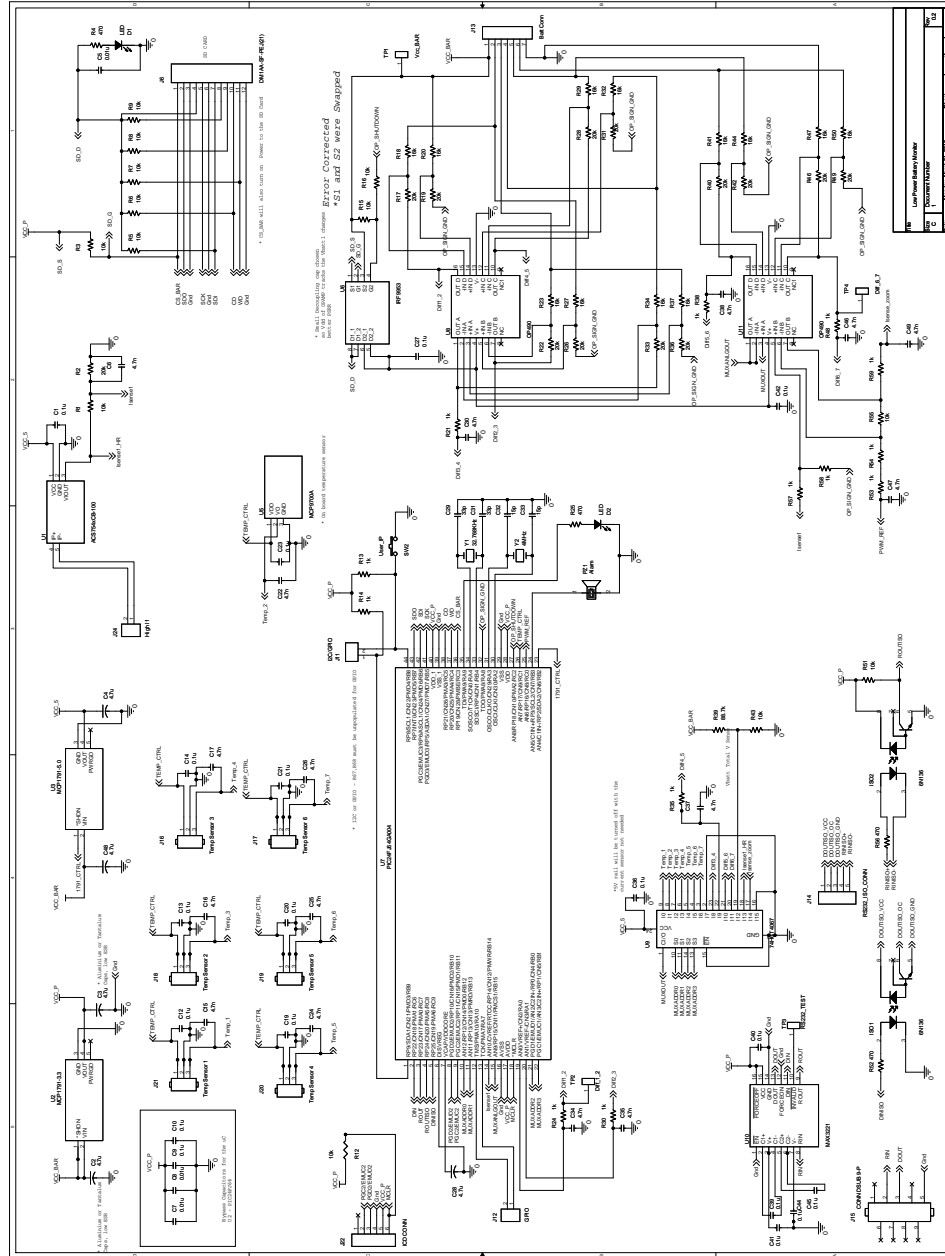


Figure .5: Complete BMS Schematic