

## ABSTRACT

SINGH, SHALEEN PRAKASH. Ge-MoS<sub>2</sub> PN Diodes for TFET Applications (Under the direction of Dr. Spyridon Pavlidis).

The performance of silicon-based CMOS integrated circuits has begun to stall due to physical scaling limits. In order to keep up with future demand for highly efficient and high-performance computing laid out by the International Technology Roadmap for Semiconductors (ITRS), it is imperative that both new semiconductor materials and new devices are studied. One candidate device is the tunneling field-effect transistor (TFET), which offers the advantage of steep-slope (<60 mV/dec) switching. Recent experimental studies have demonstrated such a device using bulk, p-type germanium (Ge) substrates and n-type 2D molybdenum disulfide (MoS<sub>2</sub>). The advantage of 2D materials lies in the promise of enhanced electrostatic control of the channel due to their inherently thin body. A major barrier for the Ge-MoS<sub>2</sub> TFET is the presence of a native and substoichiometric GeO<sub>x</sub> (germanium oxide) layer at the Ge-MoS<sub>2</sub> interface, which may degrade the subthreshold slope and reduce the drive current (I<sub>ON</sub>).

Hence, the goal of this thesis is to verify whether hydrobromic (HBr) and hydrochloric (HCl) acid treatment of the Ge surface will remove these defects and passivate the p-type Ge surface prior to the addition of n-type MoS<sub>2</sub>. The efficacy of this approach is assessed through the use of Ge-MoS<sub>2</sub> heterostructure PN junction diodes.

The electrical characterization results obtained from our Ge-MoS<sub>2</sub> devices deviate from expected results and any obvious trend in these characteristics was not found, suggesting the existence of some unknown non-idealities. Future studies that focus on these challenges are needed to realize ideal Ge-MoS<sub>2</sub> TFETs for beyond-CMOS computing systems.

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Ge-MoS<sub>2</sub> PN Diodes for TFET Applications

by  
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## **DEDICATION**

I dedicate this work to my friends, family and extended family; especially my parents Mr. Shri Prakash and Mrs. Poonam Singh, for their constant support, care and encouragement.

## **BIOGRAPHY**

Shaleen received his Bachelor of Engineering (B.E) degree in Electronics Engineering from University of Mumbai. While pursuing a B.E degree in electronics engineering, his early research interest involved study of novel semiconductor materials for electronic devices, for post-silicon era application; he got an opportunity to work as a research intern at Indian Institute of Technology Bombay to study electronic characteristics of Graphene Quantum Dots. To pursue his research interests further in the field on novel semiconductor electronic devices, Shaleen joined North Carolina State University in 2018 as a Master of Science student in Electrical Engineering, with specialization in nanoelectronics. Shaleen's masters research is on optimization of mixed-dimensional, 3D-2D (germanium-molybdenum disulfide) van der Waals heterostructure device interface, for ultra-low power TFET application. This masters research was in collaboration with imec, Belgium.

## ACKNOWLEDGMENTS

To work on this research project in collaboration with imec, Leuven, was an altogether unique experience for me, through which, I learnt a lot and developed significantly as a researcher. I consider myself fortunate enough that I got this opportunity to work at imec and really appreciate the time I spent here on my research. I express my sincere gratitude to my research advisors Dr. Spyridon Pavlidis at NCSU and Dr. Quentin Smets at imec, without the combined efforts of whom I could not have got this wonderful opportunity to work on this collaborative project, to begin with; not to mention, their constant support, encouragement and patience throughout this entire research project that has led to its successful completion. I would like to thank the Exploratory Devices group at imec for hosting and supporting my research, special thanks to my team members Yashwanth Balaji, Vivek Koladi Mootheri and Xiangyu Wu for their contribution to this project. I would like to thank Dr. Dennis van Dorp and Graniel Abrenica for their contribution to this project in helping the planning of wet-chemical treatment of the germanium substrate. I would like to thank Dr. Ginger Yu and Dr. Mehmet Ozturk for not only being a part of my committee but Dr. Yu for her constant guidance as the ADGP of ECE, helping me figure and chalk out the entire plan of work for my master's program; and Dr. Mehmet Ozturk, for actually introducing me to the field of TMDC semiconductor electronics, while I was still stuck at graphene. I would like to thank my colleagues at the LEADS group at NCSU for their invaluable feedback on my presentations for this research topic. I would like to thank the NCSU ECE department for sponsoring my travel, and, a part of my living expenses. Thanks to KU Leuven for allowing me access to the university resources as an International Scholar. Lastly, a special thanks to the OIS at NCSU and the international advisor Kelsey Stolzenbach for helping me figure out the entire graduate research abroad process from administrative perspective and their counselling during my research abroad.

## TABLE OF CONTENTS

LIST OF TABLES .....	vii
LIST OF FIGURES .....	viii
1 CHAPTER 1 INTRODUCTION .....	1
1.1 Integrated Circuits .....	1
1.2 TFET operation principle .....	2
1.2.1 Steep-Slope Devices .....	2
1.2.2 Band-To-Band TFETs as Steep-Slope devices .....	2
1.3 2D Materials for TFETs .....	4
1.4 TFETs Using the Ge-MoS <sub>2</sub> Heterostructure .....	5
1.5 Removal of GeO <sub>x</sub> .....	7
1.6 Interface optimization using diodes .....	9
1.6.1 Goal of thesis .....	9
1.6.2 Background of PN junction diodes .....	10
1.6.3 Simulations - Band diagram & Surface recombination velocity .....	12
1.7 Outline .....	15
2 CHAPTER 2 DESIGN AND FABRICATION OF Ge-MoS <sub>2</sub> DIODES .....	16
2.1 Introduction .....	16
2.2 Ge-MoS <sub>2</sub> PN Diode Designs .....	16
2.2.1 Devices with Isolation layer .....	16
2.2.2 Devices without Isolation layer .....	17
2.3 Ge-MoS <sub>2</sub> PN Diode Fabrication .....	19
2.3.1 Overview of Diode Fabrication .....	19
2.3.2 Substrate Doping .....	19
2.3.3 Removal of Ge's Native Oxide .....	22
2.3.4 Flake Transfer .....	23
2.3.5 Top-Contact Formation .....	25
2.4 Discussion .....	27
2.4.1 Comparison of device types .....	28
2.4.2 Comparison of flake transfer techniques .....	29
2.5 Conclusion .....	30
3 CHAPTER 3 RESULTS AND DISCUSSION .....	31
3.1 Introduction .....	31
3.2 MoS <sub>2</sub> Flake Thickness, Uniformity and Area Characterization .....	31

3.2.1	Uniformity Score .....	32
3.2.2	Dektak vs AFM for obtaining Flake Thickness .....	34
3.3	Electrical characterization results.....	36
3.4	Correlation between electrical and physical characteristics.....	36
3.5	Explaining deviations from expected trends .....	39
3.5.1	Additional TCAD simulations of non-idealities .....	39
3.5.2	Temperature-dependent measurements .....	39
3.5.3	Comparison with literature .....	40
3.5.4	Other possible sources of deviation .....	42
4	CHAPTER 4 CONCLUSIONS AND FUTURE WORK.....	44
4.1	Conclusions .....	44
4.2	Future Work .....	44
	REFERENCES .....	46
5	APPENDICES .....	49
	Appendix A – Non-ideality simulations .....	50
	Appendix B – Detailed Fabrication Flow .....	58

## LIST OF TABLES

**Table 1:** Pros and Cons of the 4 process flows as described in Figure 2-9. (++ means best)..... 30

## LIST OF FIGURES

<b>Figure 1-1:</b>	(a) Staggered Band alignment (b) Staggered band in OFF state [8] and (c) ON state enabling BTBT [8].	3
<b>Figure 1-2:</b>	Ge-MoS <sub>2</sub> TFET structure, showing vertical cross-section of the device [3].	6
<b>Figure 1-3:</b>	Energy band diagrams showing the staggered band alignment between bilayer MoS <sub>2</sub> and bulk Ge obtained by alignment of vacuum levels [3].	6
<b>Figure 1-4:</b>	Transmission electron microscopy (TEM) image of Ge-MoS <sub>2</sub> heterojunction showing presence of GeO <sub>x</sub> [3]. The scale bar (in black) is 2nm wide.	7
<b>Figure 1-5:</b>	(a) O 1s (Inset), showing the amount of oxide at the Ge surface for each type of treatment; Ge 3d showing characteristic peaks for Ge at 29.8 eV and 30.4 eV (b) Ge 2p <sub>3/2</sub> XPS spectrum showing slight amount of Ge-OH (Ge1+) after treatment with Halides [13].	8
<b>Figure 1-6:</b>	(a) near flat-band condition in Ge with as-is oxide (b) Band-bending after respective (HBr or HCl) halide treatment (+IPA dip) [13].	9
<b>Figure 1-7:</b>	(a) Band alignment for the Ge-MoS <sub>2</sub> diode setup used in the simulation under applied reverse bias of -1V and (b) the results of simulation for different recombination velocities.	13
<b>Figure 1-8:</b>	Effect of fixed charge density at the Ge-MoS <sub>2</sub> interface on (a) the band bending at Ge surface and (b) the I-V characteristics of the diodes.	14
<b>Figure 2-1:</b>	(a) Cross-section schematic diagram of a finished Ge-MoS <sub>2</sub> PN diode with isolation layer. (b) Top view after isolation layer etch, (c) after MoS <sub>2</sub> flake transfer and (d) the finished device after formation of metal contact.	18
<b>Figure 2-2:</b>	(a) Cross-section and (b) top view of Ge-MoS <sub>2</sub> PN diode without isolation layer.	19
<b>Figure 2-3:</b>	Process flow for fabrication of diodes with isolation layer (left) and diodes without isolation layer (right).	20
<b>Figure 2-4:</b>	Fabrication steps for diode with isolation layer: (a) Formation of opening in the SiO <sub>2</sub> after (b) Flake transfer to the opening and (c) Deposition of metal contact.	21
<b>Figure 2-5:</b>	Fabrication steps for diodes without isolation layer: (a) Flake transfer and (b) Formation of metal contact.	22
<b>Figure 2-6:</b>	Steps involved in needle flake transfer technique: (a) PMMA spin-coated and sliced-off to be used in transfer the flake, (b) PMMA transferred on top of the flake followed by bake, (c) Encapsulated flake is transferred onto the target substrate.	25

<b>Figure 2-7:</b>	Optical image of an identified good quality flake after scotch-tape transfer method under 50x microscope zoom, to be used for defining top-contact layer using “KLayout” CAD tool.....	26
<b>Figure 2-8:</b>	Top view of Contact formed via EBL.....	27
<b>Figure 2-9:</b>	Flow-chart showing the 4 types of devices possible as a combination of flake transfer techniques and dependence of contact size on the flake size.....	27
<b>Figure 3-1:</b>	(a) Flake scoring criterion and images of flakes with scores 10, 9, 8, 7, 6 and 3 (b) Histogram of flake score vs device count.....	33
<b>Figure 3-2:</b>	(a) Multiple Dektak scans required to extract the precise flake thickness (b) AFM scan of the flake, extracting complete flake profile from one scan (height profile extracted along lines “1” and “2” for comparison with Dektak) (c) Near-identical data is obtained from AFM and Dektak (all thicknesses are in nanometers) (d) Thickness data for all 18 measured flakes.....	35
<b>Figure 3-3:</b>	I-V characteristics of our Ge-MoS <sub>2</sub> diode devices with HCl treatment, HBr treatment and no treatment (as-is oxide).....	36
<b>Figure 3-4:</b>	(a) Median Flake thickness vs normalized current densities at 0.5 V (b) Normalized I-V characteristics color coded with the median flake thickness in the device.....	37
<b>Figure 3-5:</b>	Rectification ratio vs Uniformity Score of flakes. ....	38
<b>Figure 3-6:</b>	Uniformity Score distribution for normalized currents at 0.5 V. ....	39
<b>Figure 3-7:</b>	Temperature dependent I-V characteristics of Ge-MoS <sub>2</sub> diodes suggesting tunneling in reverse bias.....	40
<b>Figure 3-8:</b>	Doping concentration mapping of (a) monolayer MoS <sub>2</sub> Flake and (b) multilayer (85 layers) MoS <sub>2</sub> Flake obtained via KPFM [21].....	42
<b>Figure 5-1:</b>	(a) The band alignment and (b) corresponding I-V characteristics for different doping concentrations. ....	51
<b>Figure 5-2:</b>	(a) The band alignment and (b) corresponding I-V characteristics for different out-of-plane MoS <sub>2</sub> carrier mobilities. ....	51
<b>Figure 5-3:</b>	(a) The band alignment and (b) corresponding I-V characteristics for different MoS <sub>2</sub> flake thickness. ....	52
<b>Figure 5-4:</b>	(a) The band alignment and (b) corresponding I-V characteristics for different Schottky Barrier heights at MoS <sub>2</sub> -metal contact.....	53
<b>Figure 5-5:</b>	(a) The band alignment and (b) corresponding I-V characteristics for different out-of-plane tunneling mass of MoS <sub>2</sub> charge carriers.....	53
<b>Figure 5-6:</b>	(a) The band alignment and (b) corresponding I-V characteristics for different BTBT rates at the Ge-MoS <sub>2</sub> interface. ....	54
<b>Figure 5-7:</b>	Instead of a staggered band alignment, a straddled band alignment is obtained via application of transitivity principle and separately obtained valance band	

	offsets of MoS <sub>2</sub> and Ge from IPE on MoS <sub>2</sub> -SiO <sub>2</sub> and SiGe-SiO <sub>2</sub> . All values are in units of eV. ....	55
<b>Figure 5-8:</b>	(a) The band alignment and (b) corresponding I-V characteristics for straddled and staggered bands. ....	56
<b>Figure 5-9:</b>	(a) The band alignment and (b) corresponding I-V characteristics for straggled condition with different recombination velocities. ....	56
<b>Figure 5-10:</b>	(a) The band alignment and (b) corresponding I-V characteristics for straddled condition with different doping concentrations. ....	57

# CHAPTER 1

## INTRODUCTION

### 1.1 Integrated Circuits

Keeping up with Moore's Law [1] represents a significant challenge as we progress to newer VLSI technology nodes. The power dissipation in a CMOS IC presents a limit to the maximum number of transistors that can be crammed into a given area without causing damage to the IC due to overheating, also referred to as thermal bottleneck. The total power dissipation in a CMOS IC is a sum of dynamic, short circuit and static power losses [2]. Dynamic losses are attributed to switching transients and can be reduced by lowering the switching frequency and/or the supply voltage ( $V_{DD}$ ). Short circuit power loss is direct current (DC) leakage when both PMOS and NMOS transistors are in triode state at the same time during a switching event. This type of power loss can be reduced by minimizing the rise and fall times of the input signal since, during this transition, the power supply is essentially shorted to the ground. The ability to accomplish this, is, however, limited by the subthreshold swing (SS) of MOSFET devices, which differentiates MOSFETs from an ideal switch. The best subthreshold swing achievable in conventional MOSFET technology at room temperature is 60 mV/dec, which is due to thermionic emission [3]. This means for each 60 mV of additional gate bias, the drain current increases by a factor 10. If a smaller subthreshold swing could be reached, the ON current could be reached with a smaller supply voltage. This would significantly reduce dynamic power dissipation in CMOS technology, primarily. Secondly, the smaller the voltage swing window for transition from OFF to ON current, the smaller the short circuit power dissipation.

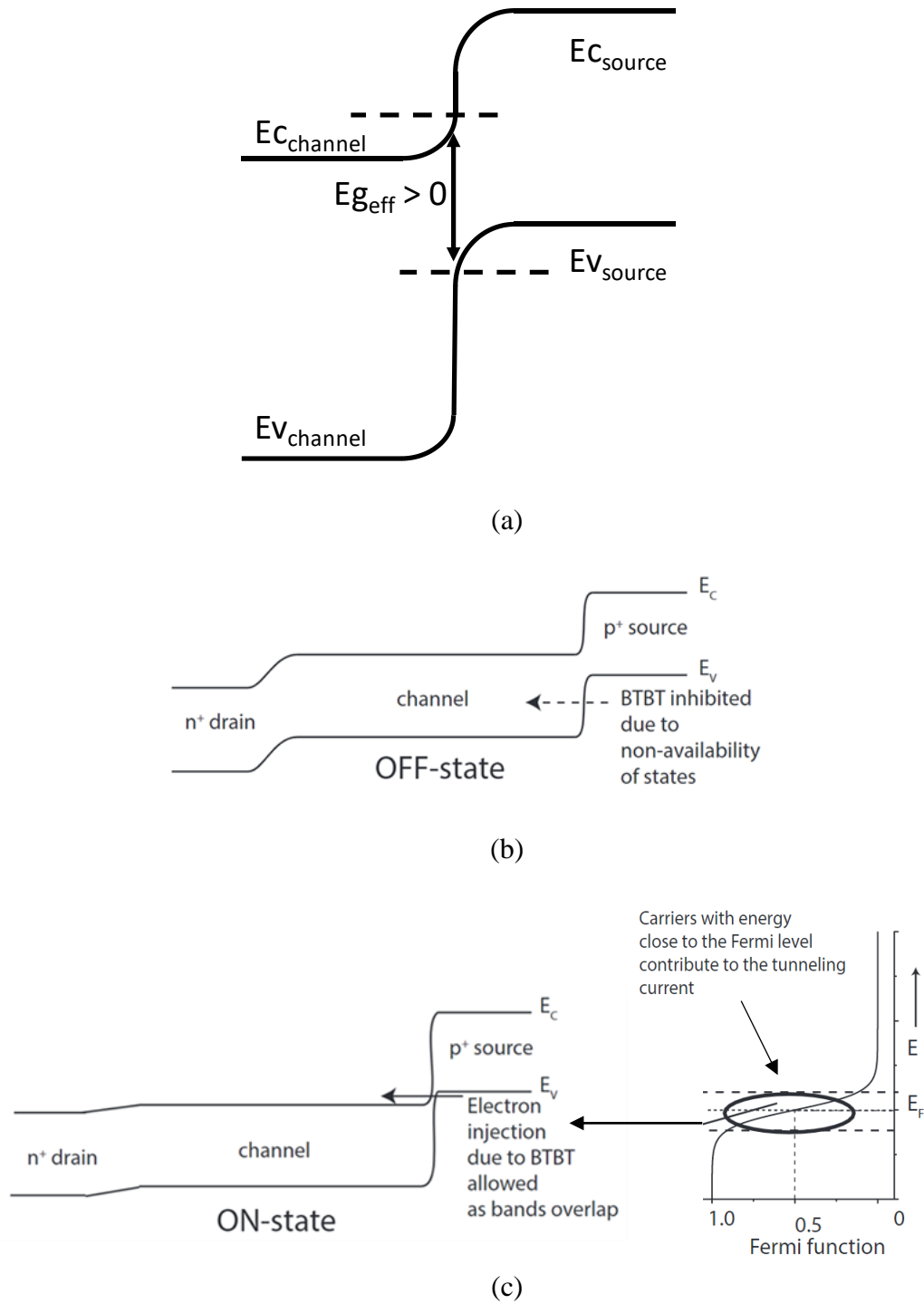
## 1.2 TFET operation principle

### 1.2.1 Steep-Slope Devices

To achieve steep subthreshold slopes of less than 60 mV/dec, new current flow mechanisms and/or technologies need to be implemented that are not limited by thermionic emission. Band-To-Band Tunneling (BTBT) [4], negative capacitance technology [5] and Metal-Insulator-Transition (MIT) transistors [6] are some such methodologies that enable a steeper subthreshold swing. BTBT, as pointed out by Seabaugh *et al.* [4], enables low voltage FET devices that do not have feedback delays which are inherent to other subthreshold mechanisms like impact ionization, ferroelectric dielectrics and mechanical gates. This makes BTB tunneling field effect transistors (TFETs) most suitable for voltage-scaling and high-speed IC applications.

### 1.2.2 Band-To-Band TFETs as Steep-Slope devices

In this section, the TFET design to achieve steep-slope devices is discussed. As can be seen from **Figure 1-1** that shows the band structure of a n-type TFET, the charge carriers from the high-energy Fermi tail that contribute to thermionic current of a MOSFET ( $SS > 60$  mV/dec) are filtered off in the TFET, and current is only due to tunneling of low-energy carriers ( $SS < 60$  mV/dec [3]). From the expression for the quantum tunneling probability of electrons through an energy barrier at a semiconductor interface [7], it is seen that a high  $I_{ON}$  can be achieved for lower effective mass and lower bandgap materials. Lower bandgap materials however also have higher source to drain and channel to drain leakage current. To overcome this issue, heterostructures that result in a staggered bandgap configuration (**Figure 1-1** (a)) can be used, where the effective bandgap for BTBT ( $E_{geff}$ ) is much lower than the bandgaps of the individual materials used on each side of the junction. This ensures lower BTBT and thermionic emission current in the off-state **Figure 1-1** (b), and a higher BTBT current in the on-state **Figure 1-1** (c).



**Figure 1-1:** (a) Staggered Band alignment (b) Staggered band in OFF state [8] and (c) ON state enabling BTBT [8].

### 1.3 2D Materials for TFETs

In order to obtain the best possible electrostatic control by the gate on the channel, it has been shown that a thinner channel is beneficial [3]. For example, 2D materials like monolayer molybdenum disulfide ( $\text{MoS}_2$ ) are exactly 3 atoms thick. In-plane, the atoms are covalently bonded to each other, and out-of-plane, the layers can be stacked on top of each other and held together by van der Waals bonds. The van der Waals force is a weak force as compared to the covalent bond force, hence this makes it easier to extract just one or just a very few  $\text{MoS}_2$  layers by simple techniques such as mechanical exfoliation. The ability to achieve atomic thickness limits in 2D channels enables better electrostatic control by the gate, and hence also provides steeper subthreshold slope as compared to 3D dimensional channels [9]. Also, the planar nature of 2D materials makes them easy to use in fabrication of devices as compared to 1D materials [3].

It is proposed, therefore, that a heterojunction formed by use of two 2D materials resulting in a staggered bandgap would be considered as the best choice of materials for building a TFET. This would allow better gate control over the channel material, and the heterojunction would be pristine as no dangling bonds will be present to form trap sites at the interface to reduce the  $I_{\text{ON}}$ .

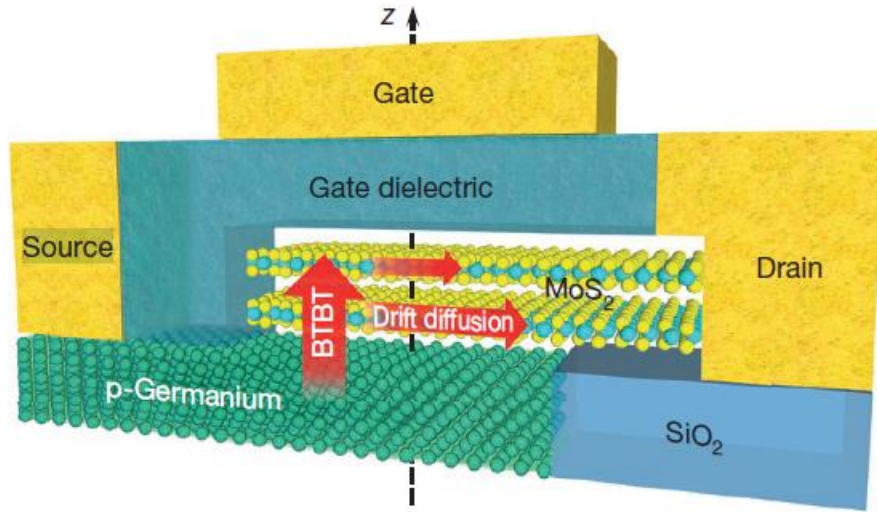
However, doping of 2D materials is still a significant challenge. Degenerate doping of the TFET source is typically used to fix its electrostatic potential, and only modulate the potential in the channel region to enable/disable BTBT. Since doping of 2D materials is not straightforward, the use of bulk materials at source has been investigated [3]. Bulk group IV and III-V semiconductors can be degenerately doped, and the use of a 2D material as the channel provides better gate control. The 3D-2D heterojunction, however, will have trap sites because of dangling bonds present at the surface of bulk material, which will reduce the  $I_{\text{ON}}$ . Hence, it will be of utmost

importance to passivate the trap sites in these 3D-2D heterojunctions to achieve a significant  $I_{ON}$ , making the TFET suitable for practical IC applications.

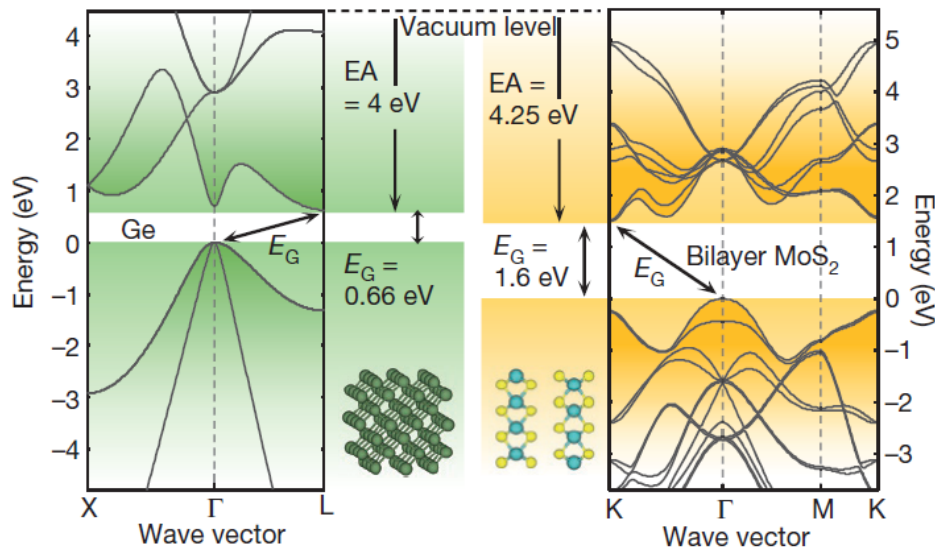
To summarize, for optimization of the TFET for a steep-subthreshold slope and a high  $I_{ON}$ , a heterostructure allowing for a staggered bandgap configuration with low-dimensional semiconducting material as channel and degenerately doped source material should be used. One of such material combinations is the Ge-MoS<sub>2</sub> heterostructure, as discussed in the next section.

#### **1.4 TFETs Using the Ge-MoS<sub>2</sub> Heterostructure**

A Ge-MoS<sub>2</sub> heterostructure TFET with steep-slope and high ON-current has been reported by Sarkar et. al. [3]. The device structure is shown in **Figure 1-2**, which shows the use of bilayer MoS<sub>2</sub> as the channel material and degenerately doped germanium as the p-type source material in a vertical configuration to maximize interface surface area in order to optimize the BTBT. The staggered bandgap alignment between the Ge-MoS<sub>2</sub> interface can be seen from **Figure 1-3**, the BTBT of electrons happens from the  $\Gamma$  wavevector symmetry point at the valance band edge of germanium to the K wavevector symmetry point at conduction band edge of MoS<sub>2</sub>, as in between these two points the energy-gap is minimum. The staggered band alignment is obtained here by the method of alignment of vacuum levels. However Internal Photoemission (IPE) [10], [11] studies show that the actual band alignment can vary significantly from the ones obtained by alignment of vacuum level (further discussed in Appendix A – Non-ideality simulations, Straddled band alignment)



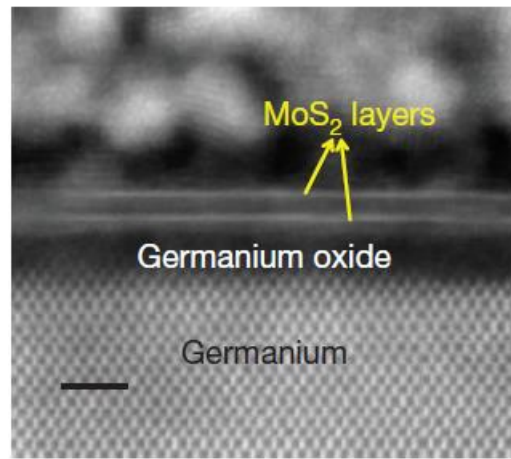
**Figure 1-2:** Ge-MoS<sub>2</sub> TFET structure, showing vertical cross-section of the device [3].



**Figure 1-3:** Energy band diagrams showing the staggered band alignment between bilayer MoS<sub>2</sub> and bulk Ge obtained by alignment of vacuum levels [3].

The device reported in this work has been shown to achieve a very steep subthreshold swing of 34.3 mV/dec for over four decades of current. The authors of this work also identified the presence of a 2 nm thick germanium Oxide (GeO<sub>x</sub>) at the Ge-MoS<sub>2</sub> interface (**Figure 1-4**). According to their analysis, this unwanted layer increases the tunneling resistance and renders the tunneling probability independent of applied bias. However it is known from other work [12] that

the defective interfaces at the tunneling junction typically introduce Shockley-Read-Hall (SRH) surface generation and recombination sites, which are expected to cause leakage current in the off-state, degrade the SS, screen the electric field and therefore reduce the ON current. At imec, Ge/MoS<sub>2</sub> TFETs have been fabricated but have poor performance, likely caused by a 5-10 nm thick GeO<sub>x</sub> layer at the interface (unpublished). With these numerous incentives to remove GeO<sub>x</sub> in mind, the focus of this thesis is to establish techniques to improve the Ge-MoS<sub>2</sub> heterostructure interface.

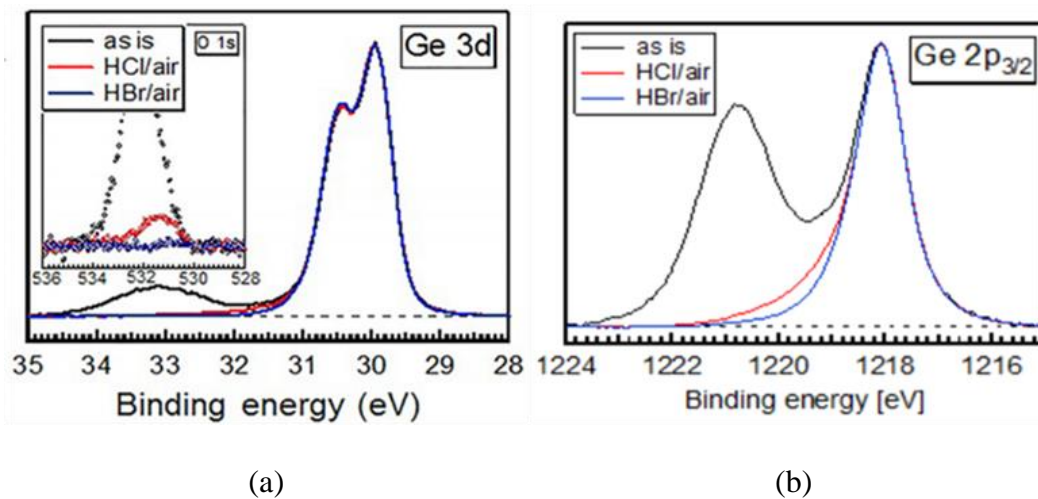


**Figure 1-4:** Transmission electron microscopy (TEM) image of Ge-MoS<sub>2</sub> heterojunction showing presence of GeO<sub>x</sub> [3]. The scale bar (in black) is 2nm wide.

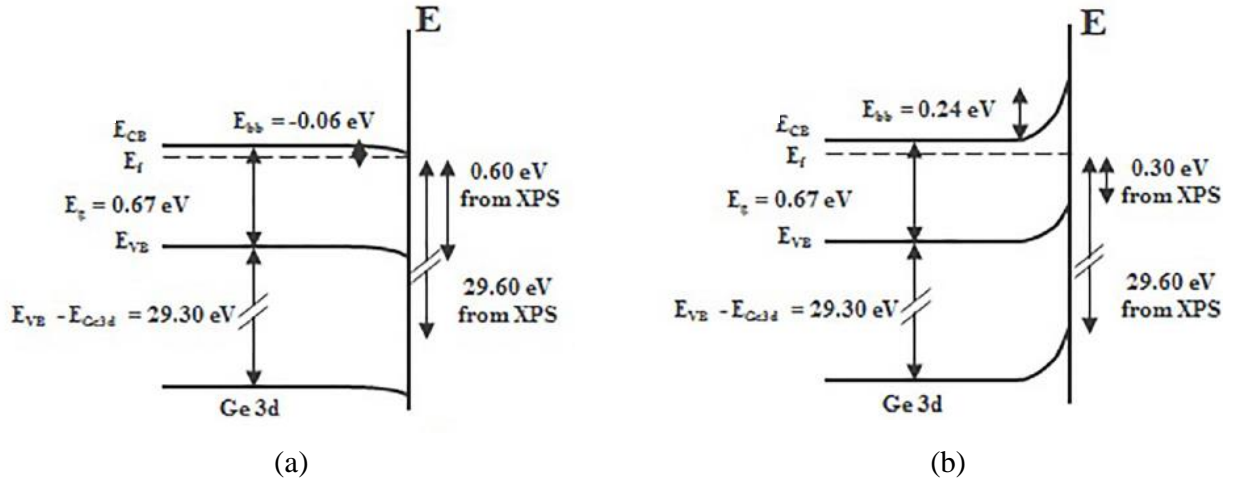
## 1.5 Removal of GeO<sub>x</sub>

To remove GeO<sub>x</sub>, Abrenica et. al. [12] used spectroscopic techniques of Time-Resolved Photoluminescence (TRPL) and X-Ray Photoelectron Spectroscopy (XPS) to compare the effectiveness of wet-chemical methods. It was found that wet-chemical bromination is the most effective and can be deployed in a simple and scalable manner. **Figure 1-5(a)** (inset) shows the O1s XPS spectra, which demonstrates that Hydrobromic acid (HBr) is more effective than Hydrochloric acid (HCl) for removal of oxide; the Ge3d XPS spectra shows typical Ge peaks and hence absence of Ge<sup>1+</sup>, Ge<sup>2+</sup>, Ge<sup>3+</sup> and Ge<sup>4+</sup> oxides. In **Figure 1-5(b)** the Ge2p<sub>3/2</sub> spectra shows

Ge-OH ( $\text{Ge}^{1+}$ ) being present in some amounts for both HBr and HCl treatment. The amount of Ge-OH on HBr-treated Ge was found to be  $0.22 \pm 0.05$  (Mega Langmuir) ML and that HCl treated Ge was  $0.42 \pm 0.05$  ML. The TRPL and XPS measurements by Abrenica et. al. show that HBr treated Ge surface should have less trap sites than the HCl treated Ge surface. One other thing to note in this work is that the negative ions ( $\text{Br}^-$  and  $\text{Cl}^-$ ) on the Ge surface from the respective treatments result in dipole formation at the Ge surface. The formation of a dipole results in band-bending at the surface of Ge, as shown in **Figure 1-6**. The amount of band-bending was obtained from XPS spectrum analysis.



**Figure 1-5:** (a) O 1s (Inset), showing the amount of oxide at the Ge surface for each type of treatment; Ge 3d showing characteristic peaks for Ge at 29.8 eV and 30.4 eV (b) Ge 2p<sub>3/2</sub> XPS spectrum showing slight amount of Ge-OH ( $\text{Ge}^{1+}$ ) after treatment with Halides [13].



**Figure 1-6:** (a) near flat-band condition in Ge with as-is oxide (b) Band-bending after respective (HBr or HCl) halide treatment (+IPA dip) [13].

In our work, the same surface treatment strategy is used and evaluated in terms of its impact on the electrical behavior of the Ge-MoS<sub>2</sub> interface. The goal of this thesis and chosen method of characterizing the Ge-MoS<sub>2</sub> interface for presence of GeO<sub>x</sub> is discussed in the next section 1.6. We expect that a halide-induced dipole at the Ge/MoS<sub>2</sub> interface will also cause band bending and possibly a different band alignment in our devices. In section 1.6.3 we perform semiclassical simulations of the Ge-MoS<sub>2</sub> diodes to acquire qualitative insight of the effects the band-bending would have for our diodes.

## 1.6 Interface optimization using diodes

### 1.6.1 Goal of thesis

The goal of this thesis is to effectively remove the germanium oxide layer present at the Ge-MoS<sub>2</sub> interface to enable the long-term development of heterostructure TFETs. In order to remove the GeO<sub>x</sub> layer, we follow the approach described in section 1.5 and performed wet-chemical bromination and chlorination of the Ge substrate using HBr and HCl, respectively. To characterize the treated interface, we fabricated Ge-MoS<sub>2</sub> diodes to be used as test structures for electrical characterization. Three types of Ge substrates are used in Ge-MoS<sub>2</sub> diodes for

comparison: i) Ge treated with HCl, ii) Ge treated with HBr and iii) Ge with as-grown GeO<sub>x</sub>. The Ge used in our devices is p-type and has a boron doping concentration either  $3.2 \times 10^{19} \text{ cm}^{-3}$  or  $5.7 \times 10^{19} \text{ cm}^{-3}$ . The MoS<sub>2</sub> flakes present in our diode devices must have a sufficiently low doping concentration in order to electrically observe the effects of GeO<sub>x</sub> as introducing reverse bias leakage current in the Ge-MoS<sub>2</sub> diodes (discussed in detail in the next section). The low n-type doping concentration in the MoS<sub>2</sub> flakes, obtained via scotch-tape exfoliation method, is present due to Sulfur vacancy defects [14], [15], [16] and [17]. The presence of GeO<sub>x</sub> at this abrupt PN junction diode introduces trap sites for carriers. These trap sites are expected to allow Shockley-Read-Hall (SRH) carrier recombination and generation [18] [19] that can be characterized as a leakage current in reverse bias, and increased ideality factor in forward bias (slope is higher than 60mV/dec at room temperature). Overall, additional trap sites reduce the rectification ratio in diode devices. The goal of this thesis is to verify whether chemical treatment will remove these defects and passivate the Ge surface to yield PN junction diodes with improved electrical characteristics in comparison to untreated diodes.

### **1.6.2 Background of PN junction diodes**

In this section, PN junctions are discussed, the ideal diode characteristics of homojunctions and heterojunctions, as well as possible deviations from ideal characteristics due to impurities at the junction interface. The Ge-MoS<sub>2</sub> heterostructure that is of interest in this work is then examined via simulation.

When a n-type semiconductor is brought in contact with a p-type semiconductor without externally applied biases, the PN junction reaches an equilibrium state after the drift and diffusion components of charge carrier transport cancel each other out. A depletion region is consequently created on both the n and p sides of the junction, the width of which is inversely dependent on the

respective doping concentrations. Generally, PN junctions are expected to exhibit rectifying behavior. The way a specific device responds electrically to an applied potential bias depends, however, on a number of factors, including 1) the magnitude and polarity of the voltage, 2) doping concentrations in each region, 3) the bandgap of the semiconductor(s) used, 4) the presence of defects that impact generation and recombination of carriers, and, if a heterojunction, 5) the band alignment (i.e. straddled, staggered or broken) between the materials used in the n- and p-regions, respectively.

For homojunction diodes, the P-doped and N-doped sides are made of the same semiconductor. In this case, the equal bandgap allows continuous band bending to take place. When impurities are present in the depletion region with defect energy levels in the bandgap, generation/recombination mechanisms (direct and/or indirect) occur and cause deviation from ideal diode characteristics; the leakage current in reverse bias is higher and the ideality factor in forward bias is also higher. In heterojunction devices, the band bending is discontinuous. The amount of discontinuity (given by Anderson's model [20]) and the type of heterojunction can result in unique band diagrams otherwise not possible in case of homojunctions. Our diodes are expected to have a staggered band alignment.

In our devices, only thick (>100 nm) MoS<sub>2</sub> flakes are intentionally chosen. In combination with their low doping concentration, this results in a wide depletion region and a low electric field. BTBT is not expected as the tunneling probability is low, and the I-V curves are expected to follow charge-injection characteristics via drift-diffusion mechanism. Having thick and lowly doped flakes helps in electrically characterizing the SRH trap sites, which are expected to show a characteristically large leakage current when GeO<sub>x</sub> is present. This leakage current would be

difficult to distinguish from BTBT dominant current in case of highly doped MoS<sub>2</sub> flakes, or in TFETs with a thin MoS<sub>2</sub> where strong BTBT is applied by a top gate.

### 1.6.3 Simulations - Band diagram & Surface recombination velocity

Ge-MoS<sub>2</sub> heterojunction diode simulations were carried out by Dr. Quentin Smets in order to predict ideal electrical characteristics, and to investigate the impact of trap sites at the heterojunction interface. The device was simulated in the Synopsys Sentaurus Device K-2015 TCAD tool. The p-type doping concentration of Ge was taken to be  $2 \times 10^{19} \text{ cm}^{-3}$  in accordance with the doping levels that were to be used in Ge substrates prepared for experiment. A n-type reference doping level of  $5 \times 10^{18} \text{ cm}^{-3}$  was assumed for MoS<sub>2</sub> based on Hall-effect measurements on thin-flake MoS<sub>2</sub> devices made at imec. An effective bandgap of 0.42 eV was taken between the valance band of Ge and the conduction band of MoS<sub>2</sub> based on publication by Sarkar *et al.* (see **Figure 1-3**) [3]. The simulations include a Schottky contact at the MoS<sub>2</sub>-metal interface, of with an electron barrier height of 0.5 eV as reference value. This was also taken from a previous result obtained by imec, in which the experimental behavior of a bilayer (CVD grown) MoS<sub>2</sub> transistor was compared to TCAD simulations (unpublished). **Figure 1-7(a)** shows the energy band diagram for the Ge-MoS<sub>2</sub> PN heterostructure with the staggered band alignment at the Ge/MoS<sub>2</sub> heterojunction and the Schottky barrier at the MoS<sub>2</sub>/metal contact.

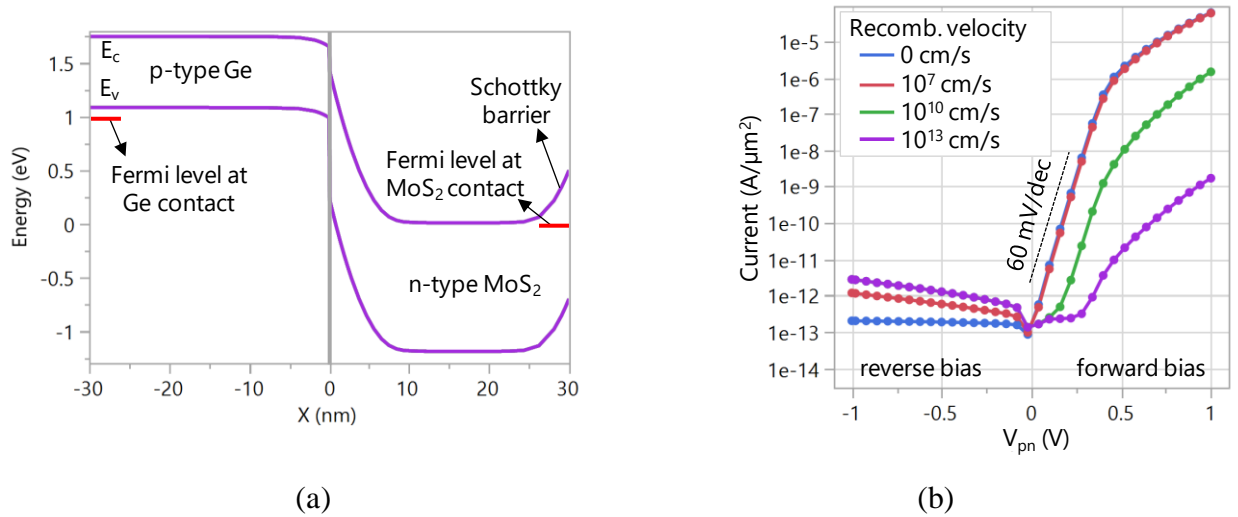
To mimic the effect of GeO<sub>x</sub>, surface SRH generation/recombination is defined at the heterointerface with a rate

$$R = \frac{n p - n_i^2}{(n + n_{\text{trap}})/s_n + (p + p_{\text{trap}})/s_p}$$

$$n_{\text{trap}} = n_i \exp\left(\frac{E_{\text{trap}} - E_i}{k_b T}\right)$$

$$p_{\text{trap}} = n_i \exp\left(\frac{E_i - E_{\text{trap}}}{k_b T}\right)$$

where  $n$  and  $p$  are the electron and hole concentrations,  $n_i$  is the intrinsic carrier concentration,  $E_{\text{trap}}$  is the trap energy level,  $E_i$  is the intrinsic energy level. We choose  $E_{\text{trap}} = E_i$  and different recombination velocities  $s_n = s_p$  are taken from 0 to  $10^{13}$  cm/s, to model different trap concentrations.

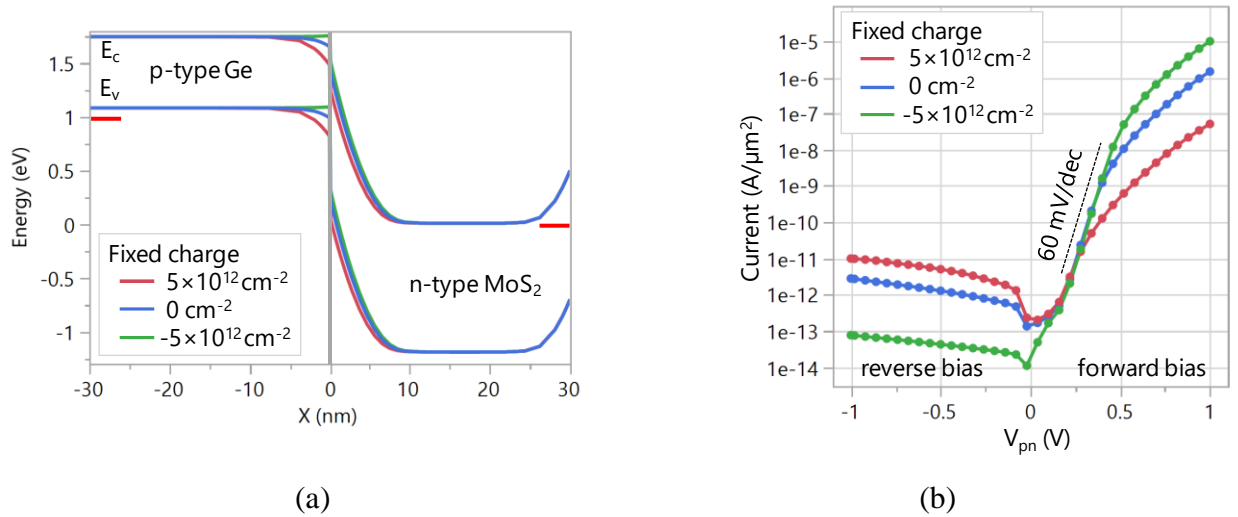


**Figure 1-7:** (a) Band alignment for the Ge-MoS<sub>2</sub> diode setup used in the simulation under applied reverse bias of -1V and (b) the results of simulation for different recombination velocities.

As can be seen from the simulation results in **Figure 1-7(b)**, for the case where no GeO<sub>x</sub> is present (represented by plot for case of 0 cm/s recombination velocity, in blue) the response is that of an ideal PN junction rectifier diode. On the other hand, a higher recombination velocity gives a lower forward bias current and a higher reverse-leakage current representing the devices that have GeO<sub>x</sub> at the interface. The recombination values used in the simulations are arbitrarily chosen to provide a quantitative understanding of the effect of trap sites. In chapter 3, diodes are treated with HCl, HBr, or left untreated, similar changes in electrical characteristics are expected.

During the writing of this thesis, a report was found mentioning that the doping levels in exfoliated MoS<sub>2</sub> flakes are lower for thicker flakes [21]. Since our experiments use thick MoS<sub>2</sub> flakes, the electric field at the Ge/MoS<sub>2</sub> heterojunction is expected to be lower than in **Figure**

**1-7(b).** There is also uncertainty on the Schottky barrier height for the thick MoS<sub>2</sub> flakes, compared to the bilayer flakes used for the calibration. Simulations however show that this change in barrier height for Multi-Layer MoS<sub>2</sub> can be considered negligible for the applied bias range in our experiments.



**Figure 1-8:** Effect of fixed charge density at the Ge-MoS<sub>2</sub> interface on (a) the band bending at Ge surface and (b) the I-V characteristics of the diodes.

**Figure 1-8** shows the band structure and the I-V results obtained from simulation of our devices for the case where band-bending takes place at the Ge surface due to the presence of fixed charge density. The use of Halides (HCl or HBr) for removal of GeO<sub>x</sub> and passivation of Ge surface results in a negative fixed charge density at the Ge surface due to halide ions (Section 1.5). In the simulation, effects of both positive and negative charge densities have been considered. The value of these fixed charge densities was loosely chosen based on the band diagrams in **Figure 1-6**, but also on trap densities observed in MoS<sub>2</sub> MOSFETs with SiO<sub>2</sub> back-gates fabricated at imec. Here, the trap density was found to be in the range of  $3 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$  to  $6 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ . Also, in this simulation in **Figure 1-8**, the recombination velocity of  $10^{10} \text{ cm/s}$  is considered to represent a small amount of GeO<sub>x</sub> at the Ge-MoS<sub>2</sub> interface. The values of charge densities and recombination

velocity are for qualitative purpose to obtain a general understanding of how these parameters will affect the I-V characteristics of our diode devices.

If no charge is present, the band bending at the Ge surface is not impacted by this, and the blue curves in **Figure 1-8** are the same as the green curves in **Figure 1-7**. If a negative fixed charge density is present at the p-type Ge substrate, this results in formation of an accumulation region at the Ge surface and hence an upwards band bending at the surface Ge interface (**Figure 1-8(a)**, in green). The accumulation of holes at the Ge interface leads to a higher forward bias current and a lower reverse bias current (**Figure 1-8 b**), in green). The presence of a positive charge density at the Ge surface results in formation of a longer depletion region and hence a downwards band bending at the Ge interface. This depletion region formed at the Ge interface causes lowering of forward bias current and an increased reverse bias current. From these simulations, a difference in electrical characteristics is also expected for the experimental results in chapter 3.

## 1.7 Outline

Having discussed the motivation, aim and methodology for our work in chapter 1, chapter 2 describes the Ge-MoS<sub>2</sub> diodes that were designed for this work, along with the details of their fabrication process. In chapter 3, the results of electrical characterization of the diodes are presented, accompanied by interpretation and discussion. Finally, chapter 4 summarizes the findings of this thesis and proposes future work related to Ge-MoS<sub>2</sub> heterostructure devices.

# CHAPTER 2

## DESIGN AND FABRICATION OF

### Ge-MoS<sub>2</sub> DIODES

#### 2.1 Introduction

In this chapter, the process to fabricate Ge-MoS<sub>2</sub> diode devices and the methodology to optimize this process are discussed in detail. Two device configurations are presented that trade off ease of production and diode geometry control. The steps to fabricate each are discussed. Efforts made to optimize each process flow ultimately motivated the decision to prioritize ease of fabrication in order to maximize the number of devices that could be studied.

#### 2.2 Ge-MoS<sub>2</sub> PN Diode Designs

Two different diode configurations were considered in order to realize Ge-MoS<sub>2</sub> PN diodes: one with an isolation layer in order to reproducibly define the Ge-MoS<sub>2</sub> interface area, and one without an isolation layer in order to simplify device fabrication.

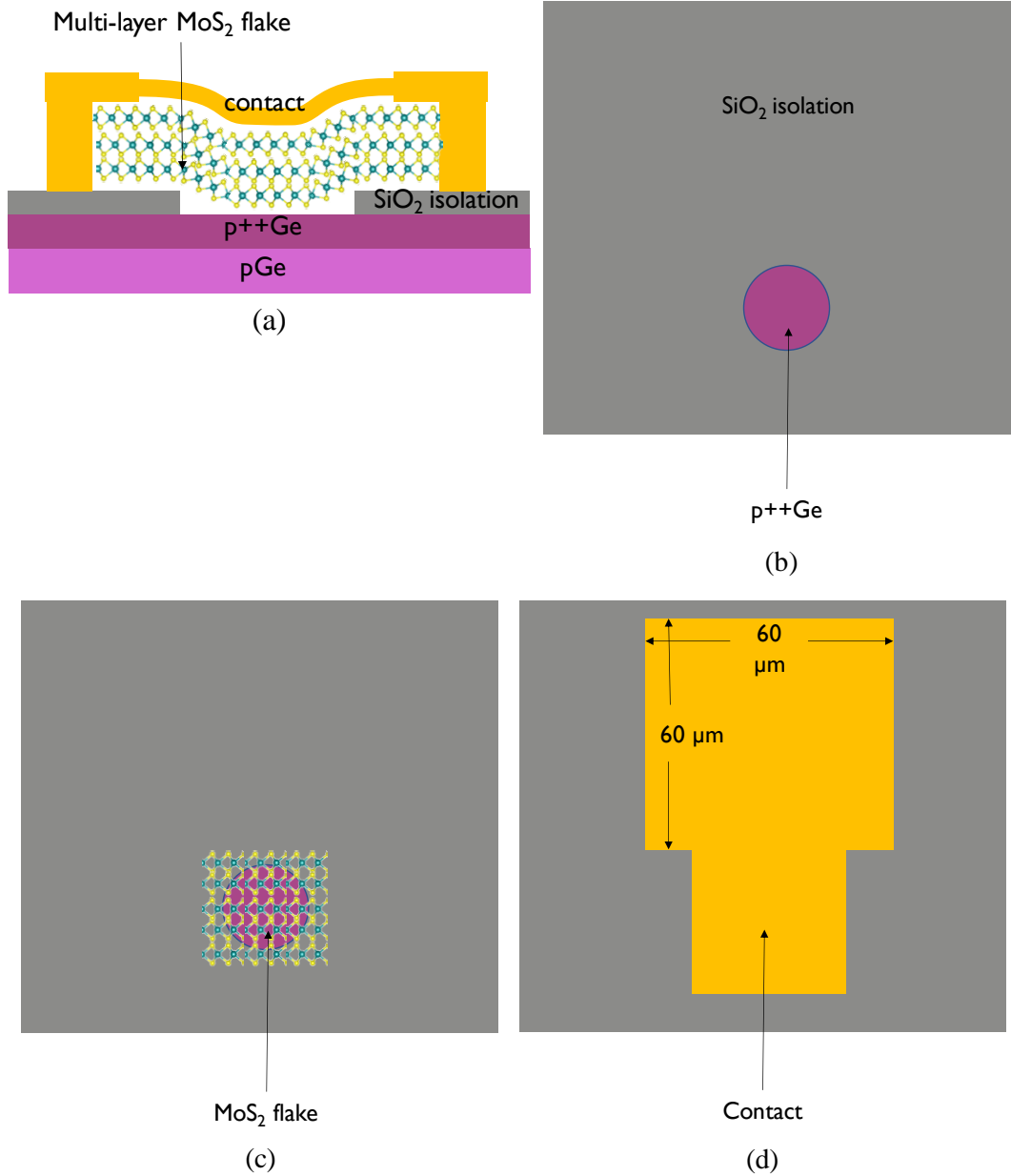
##### 2.2.1 Devices with Isolation layer

The ability to precisely produce a known device area is of utmost importance in any device technology. In this work, however, the MoS<sub>2</sub> layer was obtained through exfoliation of flakes whose size cannot be controlled and the flakes ranged from a few 10's of  $\mu\text{m}$  to 100's of  $\mu\text{m}$  in length (longest dimension). To avoid complications associated with mesa etching, a Silicon dioxide (SiO<sub>2</sub>) isolation layer with predefined openings with diameters 2 – 15  $\mu\text{m}$  was instead used, as shown in **Figure 2-1**. Devices of this type are henceforth referred to as “devices with isolation layer”. An additional advantage of these devices is that a standardized mask with fixed

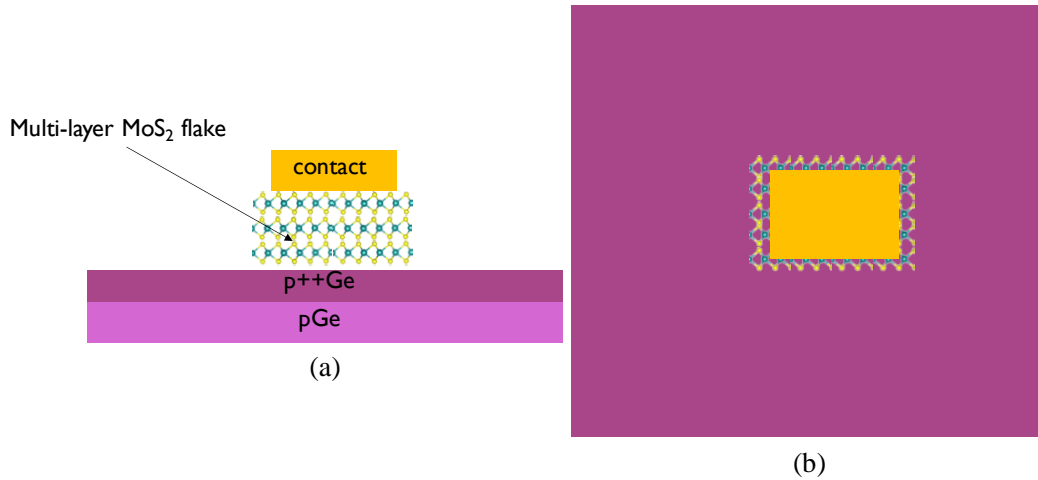
contact pad size ( $60 \times 60 \mu\text{m}^2$ ) that is easy to probe can be used, even if the exfoliated flake or diode area are smaller. Since the mask is identical for every sample, photolithography is used in this flow.

### **2.2.2 Devices without Isolation layer**

Two design considerations that compete with precision are ease and speed of fabrication. The latter were prioritized in the second type of device, depicted in **Figure 2-2**, which are referred to as “devices without isolation layer”. In such devices, an  $\text{SiO}_2$  isolation layer was not used, thereby eliminating  $\text{SiO}_2$  growth and etching steps. Flake transfer, as will be discussed below, was also facilitated to a great degree since diodes could be built wherever flakes were found rather than being restricted to flakes that aligned with the  $\text{SiO}_2$  opening. This approach also requires the top metal contact to be made on top of the  $\text{MoS}_2$  flake, and within its perimeter. Therefore, the possibility of using a mask with standardized top metal contact size and pitch for ease of probing is no longer available. Instead, a custom e-beam mask must be designed for every sample separately.



**Figure 2-1:** (a) Cross-section schematic diagram of a finished Ge-MoS<sub>2</sub> PN diode with isolation layer. (b) Top view after isolation layer etch, (c) after MoS<sub>2</sub> flake transfer and (d) the finished device after formation of metal contact.



**Figure 2-2:** (a) Cross-section and (b) top view of Ge-MoS<sub>2</sub> PN diode without isolation layer.

## 2.3 Ge-MoS<sub>2</sub> PN Diode Fabrication

In this section, an overview of the fabrication processes used to obtain each diode structure is provided. This is followed by a step-by-step description of the major fabrication steps, the detailed process flow can be found in Appendix B – Detailed Fabrication Flow.

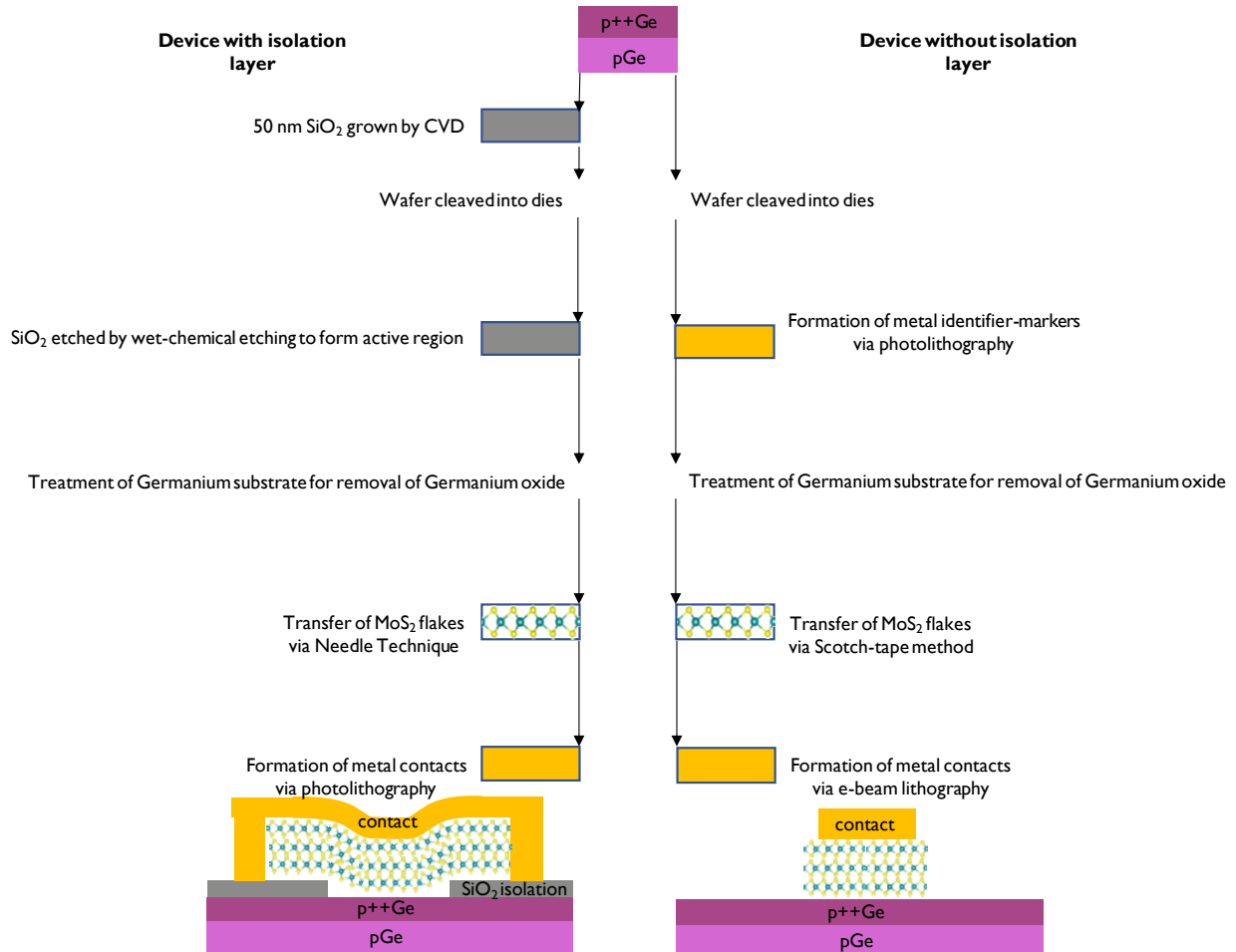
### 2.3.1 Overview of Diode Fabrication

**Figure 2-3** summarizes the fabrication steps involved in the two types of diode designs. Some steps are common, while others are unique to each design. Not having a SiO<sub>2</sub> isolation layer makes the process less complicated as development and control steps of SiO<sub>2</sub> etch are not present, hence reducing the fabrication time with the control over contact size being a trade-off. The details involved in each fabrication sequence are discussed below.

### 2.3.2 Substrate Doping

On 4-inch Ge substrates with (100) top surface orientation and p-type doping concentration  $5 \times 10^{17} \text{ cm}^{-3}$ , 100 nm of p-type germanium with Boron doping concentration either  $3.2 \times 10^{19} \text{ cm}^{-3}$  or  $5.7 \times 10^{19} \text{ cm}^{-3}$  was epitaxially grown using Chemical Vapor Deposition (CVD). The top layer doping concentration was confirmed by Hall effect measurement on separate substrates with n-

type doping concentration. The root mean square roughness of the top surface of the epitaxial layer was 0.2 nm confirmed by Atomic Force Microscopy (AFM). These wafers were then diced into dies of size 2.2 x 2.2 cm<sup>2</sup> using a saw blade with water cooling and rinse.

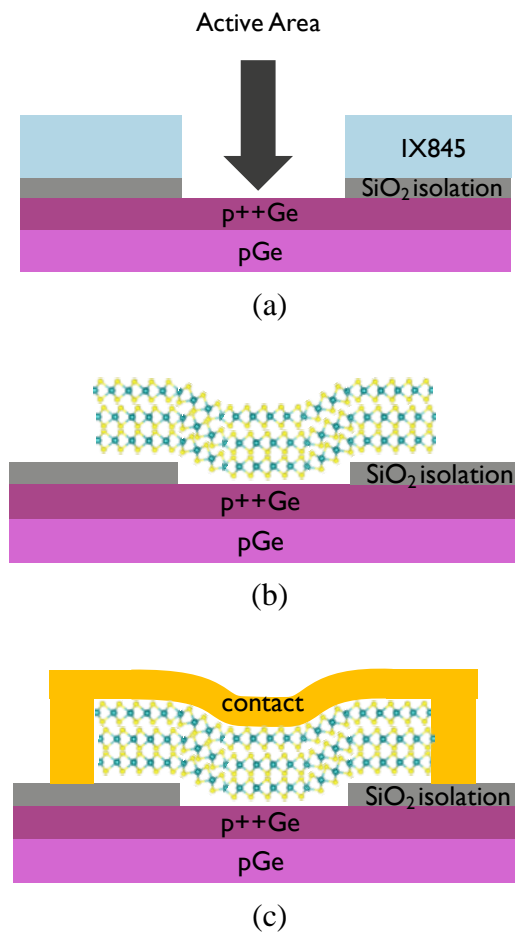


**Figure 2-3:** Process flow for fabrication of diodes with isolation layer (left) and diodes without isolation layer (right).

*i) Diodes with isolation layer*

The SiO<sub>2</sub> isolation layer was formed on top of the Ge substrate by Inductively Coupled Plasma Enhanced Chemical Vapor Deposition (ICPECVD). A thickness of 50 nm was chosen. This is sufficiently thin compared to the isolation layer opening of 1 – 15 μm, such that the transferred MoS<sub>2</sub> flakes make contact with the Ge substrate rather than being fully suspended. 50 nm is also sufficiently thick to have negligible parasitic current leakage from the Ge through

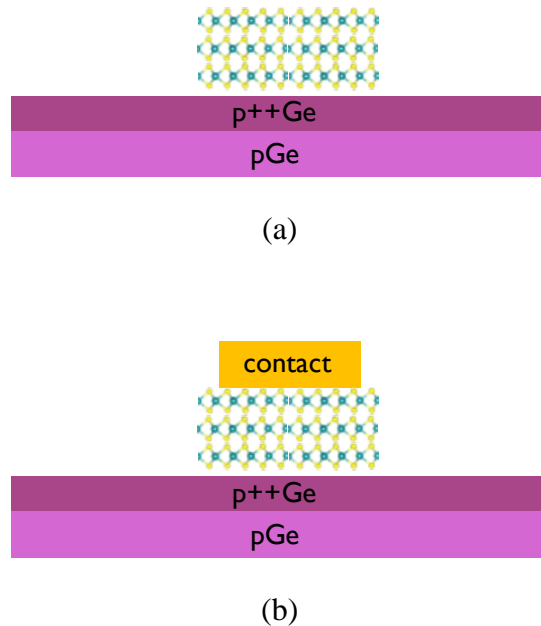
the SiO<sub>2</sub> isolation layer to the metal contact with a bias range of  $\pm 1$  V. Following photolithography to pattern a photoresist etch mask, the isolation layer was removed using buffered hydrofluoric (BHF) acid to expose the underlying substrate (**Figure 2-4** (a)). After the required treatment for removal of GeO<sub>x</sub>, the MoS<sub>2</sub> flake was then transferred on top of the exposed region (**Figure 2-4** (b)). More details regarding the flake transfer methods used are presented in Section 2.3.4. The top Nickel/Palladium (Ni/Pd: 10 nm/20 nm) metal contact was formed via metal evaporation and subsequent lift-off. By extending beyond the top of the MoS<sub>2</sub> flake and over the SiO<sub>2</sub> isolation layer region, a large probe pad can be made for easy probing (**Figure 2-4** c)), which is needed for electrical characterization of the diodes.



**Figure 2-4:** Fabrication steps for diode with isolation layer: (a) Formation of opening in the SiO<sub>2</sub> after (b) Flake transfer to the opening and (c) Deposition of metal contact.

ii) *Diodes without Isolation layer:*

In the non-isolated device structured, fabrication began with the immediate transfer of the exfoliated MoS<sub>2</sub> flake onto the Ge substrate. Using E-Beam Lithography (EBL), a custom contact pad can be defined in response to the arbitrary size and shape of the exfoliated flakes. After the required treatment for removal of germanium-oxide is done [Figure 2-5 a)], The metal deposited for these contacts was via evaporation of sputtered Nickel/Gold (Ni/Au: 10 nm/20 nm) (Figure 2-5 b)).



**Figure 2-5:** Fabrication steps for diodes without isolation layer: (a) Flake transfer and (b) Formation of metal contact.

### 2.3.3 Removal of Ge's Native Oxide

As noted previously, a key objective of this work was to study the effectiveness of different native oxide (GeO<sub>x</sub>) removal techniques in order to achieve a pristine Ge-MoS<sub>2</sub> interface. In the devices without an isolation layer, GeO<sub>x</sub> removal occurred after substrate dicing and right before MoS<sub>2</sub> flake transfer. In the devices with an isolation layer, by contrast, this procedure was carried

after SiO<sub>2</sub> etching and also right before MoS<sub>2</sub> flake transfer. GeO<sub>x</sub> removal was attempted by dipping the wafer in a halogen acid (HCl or HBr) for 10 minutes followed by an immediate dip in Isopropyl alcohol (IPA) for about 2 minutes to rinse the acid in a way that does not re-oxidize the surface. To further delay the re-growth of a GeO<sub>x</sub> layer, the samples were stored in a beaker of IPA for maximum 30 minutes, until the flakes were ready to be transferred onto the die. In this work, three different cases were considered: (1) samples treated with HCl, (2) samples treated with HBr, and (3) samples without surface treatment, where the native oxide is kept as-is.

#### **2.3.4 Flake Transfer**

As mentioned above, a critical step in the fabrication process involves the transfer of MoS<sub>2</sub> flakes from a bulk source crystal. This process is known as exfoliation, and is known to currently provide superior device performance compared to devices relying on CVD-grown films [22]. While exfoliation is a useful tool for basic studies, it is important to note that better scalability of the MoS<sub>2</sub> films is achievable via CVD growth [23] [24] [25]. Since for the characterization of GeO<sub>x</sub> in our Ge-MoS<sub>2</sub> diodes, it is essential to have low doping concentration in MoS<sub>2</sub> flakes, leading to a wide depletion region (Section 1.6.2), we need flakes thicker than the depletion region width in order to ensure proper functioning of the diode devices. We choose Flake exfoliation to obtain MoS<sub>2</sub> flakes from bulk sample as this is able to provide the thick MoS<sub>2</sub> flakes needed for our devices, as opposed to the CVD growth method available at imec, that currently allows a maximum thickness of 3 nm for MoS<sub>2</sub> flakes.

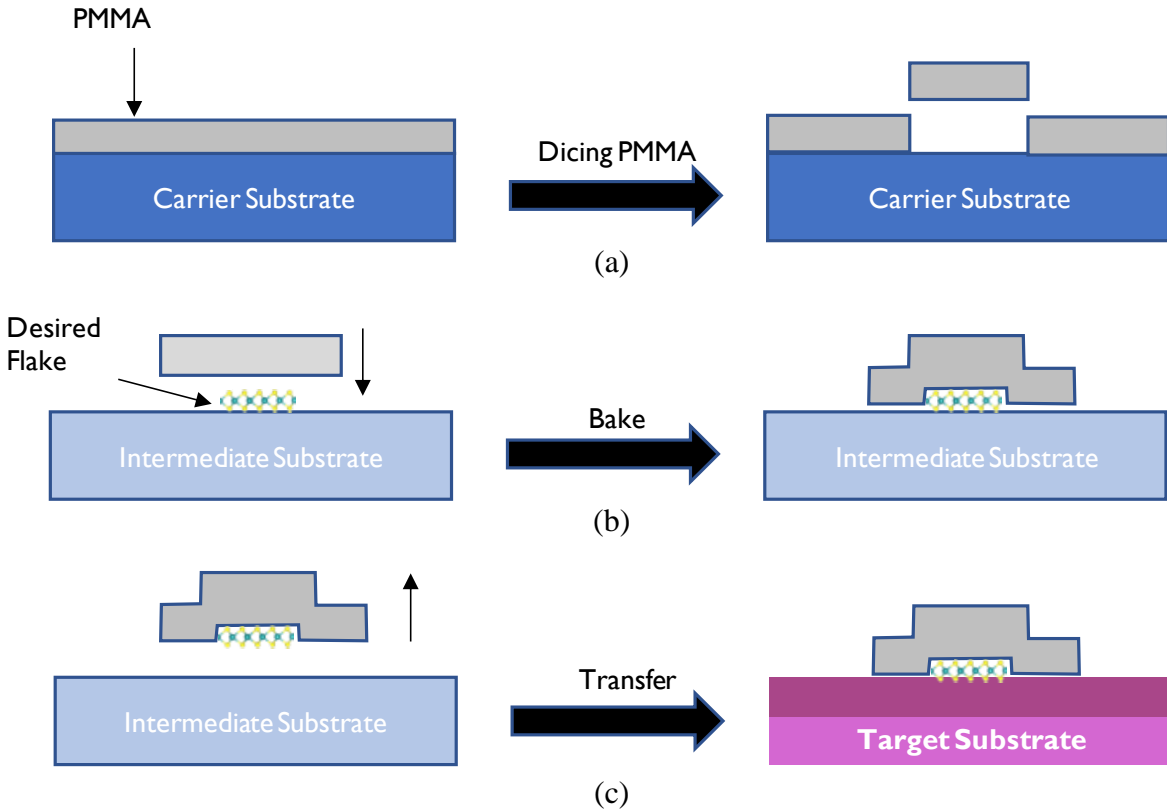
Two types of flake transfer techniques were evaluated: “direct scotch-tape transfer” and “needle transfer”.

*i) Scotch-Tape method of Flake Transfer:*

This technique is inspired by the Nobel Prize winning work conducted by the Manchester group [22]. The flakes were lifted-off from bulk MoS<sub>2</sub> using a piece of scotch-tape. Consequently, the tape was folded in half and the two ends pressed together repeatedly in order to perform a series of exfoliations that yielded flakes with a desired thickness. This step was executed in advance, so that once the substrates were chemically treated to remove surface GeO<sub>x</sub>, the tape could be pressed down onto the Ge substrate as quickly as possible to avoid oxide regrowth. The tape was then peeled off, leaving behind the MoS<sub>2</sub> flakes, which are held onto the substrate with help of van der Waals forces. Finally, tape residue was cleaned away by dipping the substrate in Dichloromethane (DCM) for 5-10 minutes.

*ii) Needle Transfer Technique:*

As shown **Figure 2-6 a)**, the first step of the needle transfer technique [26] was to spin-coat a layer of Poly(methyl methacrylate) (PMMA) on top of a carrier substrate. The PMMA was then manually sliced into pieces using a surgeon's scalpel to obtain a block that is large enough to encapsulate a desired flake, typically 20 x 20 μm<sup>2</sup>. A needle was then used to pick up the PMMA block and transfer it on top of MoS<sub>2</sub> flakes that had already been exfoliated onto an intermediate substrate using scotch-tape. The intermediate substrate was subsequently heated in order to reflow the PMMA and enable it to completely cover the underlying flake, as depicted in **Figure 2-6 b)**. With help of the needle again, the PMMA was gently poked on its sides until it was released from the substrate along with the target flake. Thus, the PMMA could be precisely (within 10 μm) positioned on top of the germanium substrate and lowered to transfer the flake. Finally, the PMMA was baked and allowed to cool down, followed by a dip in DCM for about 10 minutes to dissolve away the PMMA and leave the MoS<sub>2</sub> flake behind.



**Figure 2-6:** Steps involved in needle flake transfer technique: (a) PMMA spin-coated and sliced-off to be used in transfer the flake, (b) PMMA transferred on top of the flake followed by bake, (c) Encapsulated flake is transferred onto the target substrate.

### 2.3.5 Top-Contact Formation

In case of devices with isolation layer, the use of a standardized mask for formation of active regions also allowed for designing a standardized mask for top contact for each device. The top contact had to follow the same pre-defined co-ordinates as the active region (going on top of the active region), and also, the dimensions could be pre-defined (as this was not restricted by the flake shape and size). Photolithography enables pre-defining the top-contact size and its placement co-ordinates. After aligning the top-contact mask with the active region pattern, photolithography was performed to transfer the top-contact pattern onto the photoresist. The photoresist was then developed followed by deposition of top-contact metal deposition and lift-off to make top-contacts in case of devices with isolation layer.

In contrast, a more complicated process was required for flakes transferred onto a substrate lacking the isolation layer and hence with random flake placement. Firstly, the surface of the substrate was inspected with a microscope in order to identify candidate flakes, which were evaluated based on their size, average thickness and thickness uniformity. The results of this morphological characterization will be discussed in section 3.2. At locations where flakes of interest were identified, microscope images were saved (**Figure 2-7**) and imported into the “KLayout” CAD tool. This permitted the preparation of ad-hoc E-Beam Lithography (EBL) layouts for each flake. In general, the metal contact was designed well within the flake boundaries ( $\sim 10\ \mu\text{m}$  margin, seen in **Figure 2-8**) to avoid the metal contacting the germanium directly, hence forming a short circuit. After EBL exposure of PMMA and development, 20 nm Titanium/ 70 nm Gold (Ti/Au) was deposited on top of the flakes by evaporation and lifted off.



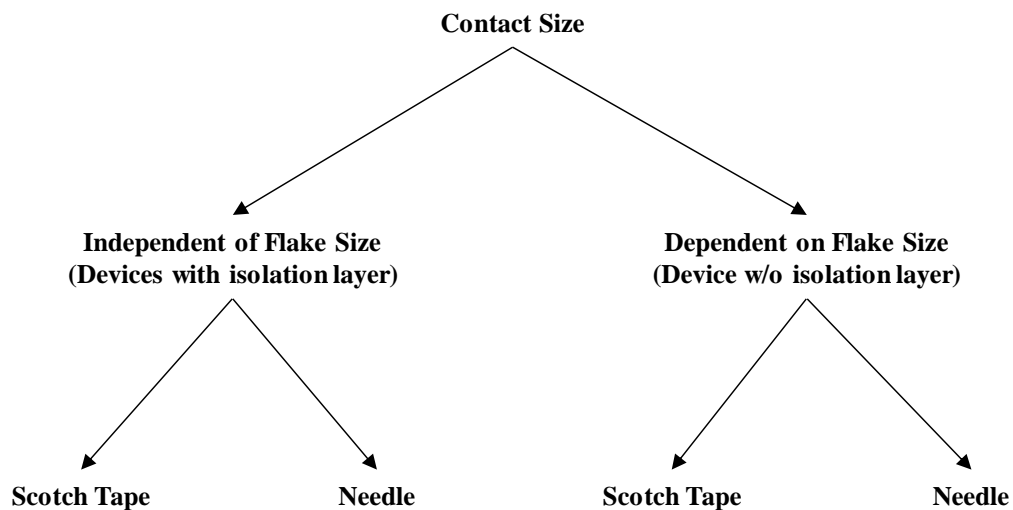
**Figure 2-7:** Optical image of an identified good quality flake after scotch-tape transfer method under 50x microscope zoom, to be used for defining top-contact layer using “KLayout” CAD tool.



**Figure 2-8:** Top view of Contact formed via EBL.

## 2.4 Discussion

The combination of the two possible device types (with or without isolation layer) and two possible flake transfer techniques (needle or scotch-tape) leads to 4 possible process flows to fabricate our Ge-MoS<sub>2</sub> diodes, shown in **Figure 2-9**. Since, ultimately, it is the entire process flow that matters, it is important to compare all the possible process flows that the different combinations of device types and fabrication steps provide, in order to decide which process flow would be the optimum for our study. In the next part, first, the comparison between the alternate device types and the alternate fabrication steps are discussed, then the entire process flows possible as a combination of these variations are compared.



**Figure 2-9:** Flow-chart showing the 4 types of devices possible as a combination of flake transfer techniques and dependence of contact size on the flake size.

### 2.4.1 Comparison of device types

Beginning with the dependence of metal contact size on the flake size, we had devices in which contact size is independent of the flake size (with isolation layer) and devices where the contact size was dependent on the flake size (without isolation layer). As already discussed in detail in sections 2.2.1 and 2.2.2, the advantage of diodes with isolation layer is that the contact size is standardized and pre-defined by photolithography. This has three knock-on advantages. First, the contacts are large enough for convenient probing during electrical characterizations. Second, the probe needles are placed on Ge/SiO<sub>2</sub>/metal stack, instead of Ge/MoS<sub>2</sub>/metal stack, avoiding any risk of MoS<sub>2</sub> flake getting punctured while probing. This is mechanically more robust than a stack with MoS<sub>2</sub>, which delaminates easily. Third, the regular contact spacing allows electrical measurements with automatic stepping. The disadvantage of devices with isolation layer, however, is that these devices require growth of a SiO<sub>2</sub> isolation layer followed by its etching to expose the Ge surface. It also requires alignment of the MoS<sub>2</sub> flakes on top of these exposed spots, during transfer process. Growth and etching of SiO<sub>2</sub> modify the Ge surface. They also add extra steps to diode fabrication, making this flow more complicated and longer to execute.

On the other hand, diodes without isolation layer do not require growth and etch of SiO<sub>2</sub>. However, since this allows us to make contacts only on top of the flakes, the size of contact might be too small at times due to randomness in flake sizes, making it difficult to probe the devices. To allow maximum contact area, the shape of contacts need to replicate the flake below with a narrow margin to avoid shorting with the Ge substrate. The flakes are of random shape and size and so the contact needs to be defined individually for each and every flake as described in detail in section 2.3.5. As described in the next section, with respect to the flake transfer method that works best

with each type of device, the devices without isolation layer have an advantage over the devices with isolation layer, in terms of Critical Timing Loop (CTL) to transfer the flakes.

#### 2.4.2 Comparison of flake transfer techniques

The advantage of the direct scotch-tape transfer method is that it allows a much faster transfer of many flakes at once on to the germanium substrate. Hence this is best to fabricate many devices on a sample, while keeping any re-growth of germanium Oxide to a minimum, having the shortest CTL. However, the flakes, which range in length from few 10's of  $\mu\text{m}$  to 100's of  $\mu\text{m}$ , are scattered randomly over the substrate. In the flow with isolation layer, the flakes need to be aligned to the openings in the isolation layer, hence the yield would be very low (only 3 devices were observed experimentally on a single sample). Therefore, the scotch-tape transfer method is most suitable for devices without an isolation layer (37 operational devices were measured on a single sample). The needle technique, on the other hand, allows very precise placement of the flakes; albeit at the cost of time and so have a longer CTL. Typically, 5-10 minutes are needed for this method. The ability to intentionally align a  $\text{MoS}_2$  flake to the  $\text{SiO}_2$  openings on the wafer makes it a highly suitable method for devices with an isolation layer. Having compared all the parallels in fabrication steps against one another, we discuss next the comparison of all the process flows that the different combinations of the parallel steps lead to. **Table 1** shows a concise comparison of the 4 possible process flows. After fabricating devices with and without the isolation layer and comparing the flake transfer techniques, it was found that scotch-tape method of flake transfer gave a high yield of large flake sizes, allowing us to form large enough contacts for convenient probing of devices during electrical characterization and most importantly shortest CTL to keep the re-growth of  $\text{GeO}_x$  to minimum. Since the scotch-tape technique of flake transfer is best suited for devices without isolation layer which do not require growth and etching away steps of  $\text{SiO}_2$ , it

was concluded that that the devices without isolation layer with scotch-tape flake transfer give us the most optimized process flow to fabricate Ge-MoS<sub>2</sub> diode devices in terms of both faster fabrication and convenient electrical characterization.

**Table 1:** Pros and Cons of the 4 process flows as described in Figure 2-9. (++ means best)

Process Flow	With isolation		Without isolation	
	scotch tape	needle	scotch tape	needle
Ease of probing during electrical measurements	+	+	-	-
Control of device dimensions	+	++	--	-
Limit GeO <sub>x</sub> regrowth (short CTL)	+	-	+	-
Device quality and variability	+	++	--	-
Number of devices per samples	--	+	++	+
Amount of processing steps	-	--	++	+
Time required to produce one sample	-	--	++	+
			chosen	

## 2.5 Conclusion

In this chapter we have explored two types of Ge-MoS<sub>2</sub> diode designs (with isolation versus without isolation layer) and two types of flake transfer techniques (direct scotch-tape versus needle technique). Of the 4 possible combinations, we established that the optimal process flow is without isolation layer and with direct scotch-tape transfer technique. These allow fastest fabrication, the shortest CTL between Ge passivation and MoS<sub>2</sub> transfer, and high yield of large sized flakes. The most important is the shortest CTL, as this allows the fastest flake transfer and hence minimum time window for re-growth of GeO<sub>x</sub>, which is the aim of our study.

# CHAPTER 3

## RESULTS AND DISCUSSION

### 3.1 Introduction

With the optimal process flow established in chapter 2, three different Ge passivation conditions were used (HCl-treated, HBr-treated, and no treatment) over 6 different samples, and in total 121 Ge-MoS<sub>2</sub> diode devices were fabricated. Then, physical characterization was performed, and section 3.2 shows combination of AFM and profilometry to estimate the MoS<sub>2</sub> flake thickness and uniformity. In section 3.3, the electrical characterization is presented and linked to the physical characterization for each individual device in section 3.4. Since clear trends with the different Ge passivation conditions are lacking, in section 3.5 the results are compared against those from additional TCAD simulations to incorporate additional non-idealities that might be present, compare to similar works in literature. Finally, other possible sources of deviation are suggested.

### 3.2 MoS<sub>2</sub> Flake Thickness, Uniformity and Area Characterization

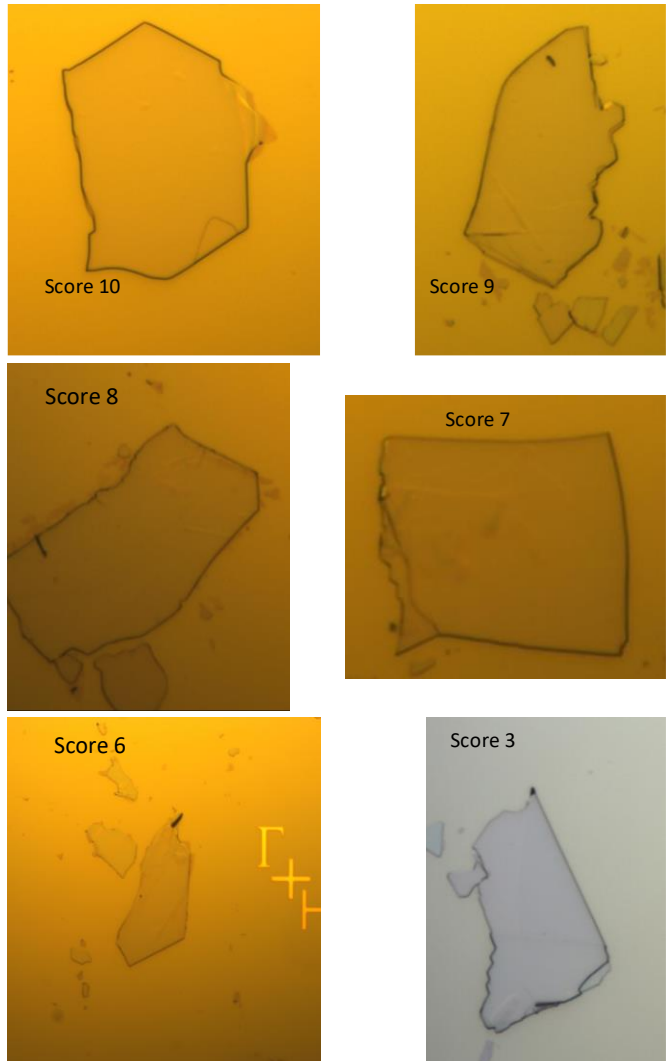
As discussed in chapter 2, it was decided that the exfoliated flake transfer method would be used to realize large numbers of Ge-MoS<sub>2</sub> PN diodes. Since the exfoliation process does not permit tight control over the produced flakes, it was critical to gather the following three parameters for each electrically measured device: uniformity score, thickness, and area of the MoS<sub>2</sub> flakes. The uniformity was characterized by optical microscope inspection. The thickness measurements were performed via a combination of atomic force microscopy (AFM) and contact profilometry; the latter will be hereafter referred to as “Dektak” in recognition of the instrument’s

manufacturer. The flake and contact areas were measured by importing the optical microscope images into KLayout. These three physical characterization methods are covered in the following sections.

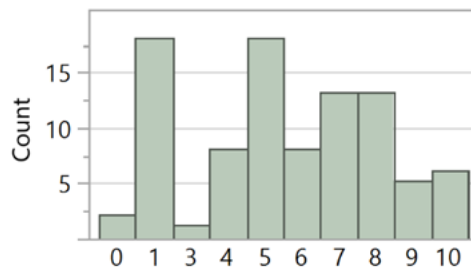
### 3.2.1 Uniformity Score

In anticipation that the MoS<sub>2</sub> quality would impact the electrical performance of the diodes, flakes were grouped according to their within-device thickness uniformity based on inspection via optical microscope. This is a very fast method, allowing all 121 electrically measured devices to be inspected. However, the thickness cannot be extracted quantitatively, and only large differences in thickness result in a difference in color and brightness. Thus, a score was assigned to every flake to group them by similar uniformity. This score is defined in table shown in **Figure 3-1** (a) and example images of flakes with different flake scores are presented on the right of this table. **Figure 3-1** (b), is the histogram of flake score vs number of devices representing each flake score. Electrical results of devices with a flake score of 5 and above were considered sufficiently high quality and included in electrical characterization.

SCORE	OPTICAL CHARACTERISTIC
10	100% Uniform.
9	Small region of slight variation in thickness.
8	Two regions with slight variation in thickness.
7	Two regions with large variation in thickness.
6	Many different of slight variation of thickness.
5	Large differences in thickness.
4	Tears present.
3	Large differences in thickness and tears.
0	Sort/Metal markers beneath the flakes.



(a)



(b)

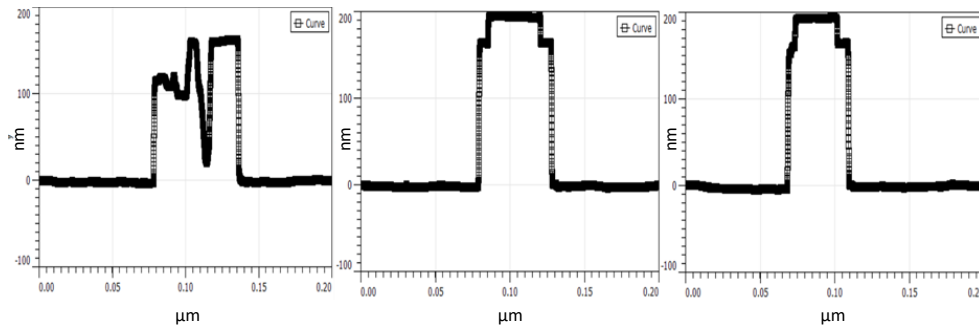
**Figure 3-1:** (a) Flake scoring criterion and images of flakes with scores 10, 9, 8, 7, 6 and 3 (b) Histogram of flake score vs device count.

### 3.2.2 Dektak vs AFM for obtaining Flake Thickness

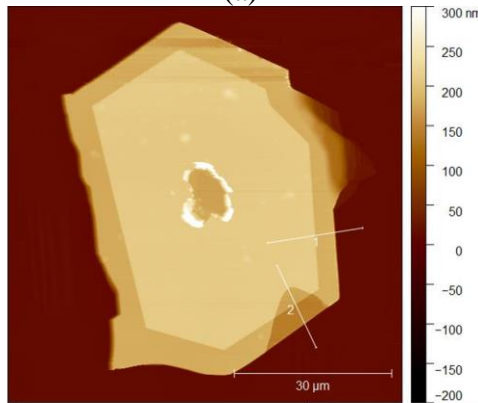
The flake thickness could be quantitatively extracted either via Dektak or AFM. Dektak is a faster method for extracting the thickness profile of flakes, albeit at the cost of being a 1D measurement with less precision compared to AFM scans. Since AFM scans map an entire region as compared to the single-line-scan of Dektak, AFM scans can extract more data. Additionally, since the sensitivity and resolution of AFM scans are higher as compared to Dektak, the results are more precise. **Figure 3-2** (a) and **Figure 3-2** (b) show three Dektak scans and a AFM scan respectively for a same flake. The AFM scan in **Figure 3-2** (b) shows the profiles of flake and the metal contact on top of the flake, a margin of about 10 nm was left when forming metal contact on top of the flake. The piercing seen on the metal contact is as a result of probing during electrical characterization. Only the metal contact was pierced and not the MoS<sub>2</sub> flake. The electrical characteristics of the Ge-MoS<sub>2</sub> devices were not affected due to this piercing of metal contact, as confirmed by repeating the electrical measurements multiple times before and after the piercing was formed.

Ideally, it might be best to scan the entire flake with more precision to get a real thickness profile of the flake. However, given that we had about 65 devices of flake score 5 and above, making AFM scans for each and every device was not feasible. To extract the thickness profile of all 65 flakes within a reasonable time frame, the flake thickness results from AFM and Dektak were compared for a few flakes to see how precise the results from Dektak are. As can be seen from the table in **Figure 3-2** (c), Dektak scans were found to be in good agreement with the AFM scans with an error of about 3%. With these results, it was concluded that Dektak scans are precise enough to extract flake thickness. **Figure 3-2** (d) shows the flake thickness obtained for 18 flakes

after assigning them with a flake score. All flakes are thicker than 50 nm, as intended, per requirement of flakes thicker than the depletion width for our devices (section 1.6.2).



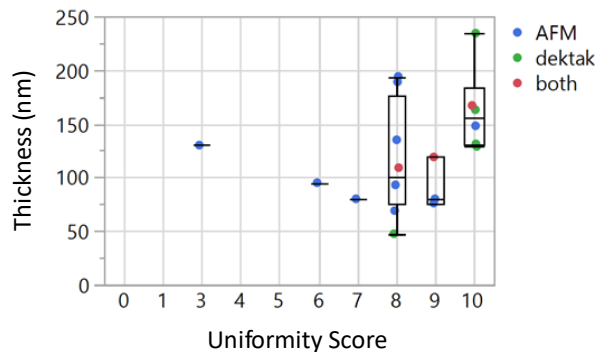
(a)



(b)

Flake Score	AFM max	AFM median	AFM min	Dektak max	Dektak median	Dektak min
10	167	167	125	169	160.8	157.2
9	119	119	119	121.1	114.1	111.4
8	109	109	90	107.5	102.2	89.2

(c)

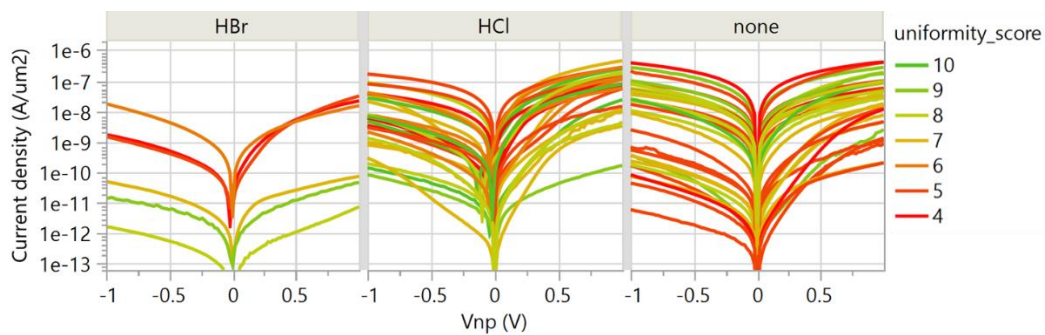


(d)

**Figure 3-2:** (a) Multiple Dektak scans required to extract the precise flake thickness (b) AFM scan of the flake, extracting complete flake profile from one scan (height profile extracted along lines “1” and “2” for comparison with Dektak) (c) Near-identical data is obtained from AFM and Dektak (all thicknesses are in nanometers) (d) Thickness data for all 18 measured flakes.

### 3.3 Electrical characterization results

The normalized I-V characteristics with respect to flake area from our Ge-MoS<sub>2</sub> diodes, treated with HCl, HBr, and with no interface treatment are shown in **Figure 3-3**. These exhibit reverse bias currents in ranges comparable to or higher than forward bias currents, which is not expected. The expected I-V characteristics have been discussed in section 1.6.3, with a higher current in forward bias than reverse bias. The highest rectification ratio was expected for the case of very low surface recombination velocity (GeOx removed and passivated with HCl and/or HBr). For the case of high surface recombination velocity (no treatment, native GeOx still present), the simulations predicted higher leakage current in reverse bias but still with rectifying behavior. The experiments do not show a clear trend with surface treatment, are not rectifying, and are therefore not in line with the simulations. Also, as can be seen from the experimental results, there is a very large device-to-device variability of current density of 3 to 4 decades, which appears to be random with respect to the color-coded flake scores.



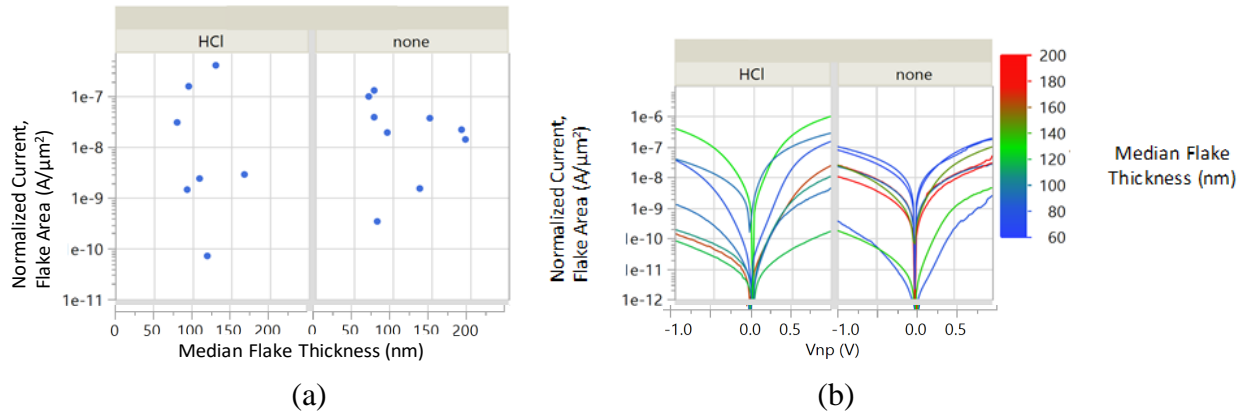
**Figure 3-3:** I-V characteristics of our Ge-MoS<sub>2</sub> diode devices with HCl treatment, HBr treatment and no treatment (as-is oxide).

### 3.4 Correlation between electrical and physical characteristics

In this section, an analysis of our results is presented to see if a trend between electrical and physical characteristics persists.

i) *Current density vs flake thickness:*

It has been reported in literature that thicker flakes could have a lower doping concentration than thin flakes. This will be discussed in more detail in section 3.5.3 ii). If true for our devices, a lower current density is expected for thicker flakes due to the poor electron injection at the MoS<sub>2</sub>/metal Schottky contact (Appendix A – Non-ideality simulations, a). This trend is expected to be seen in normalized I-V characteristics with respect to thickness of flakes. As can be seen from the **Figure 3-4**, no such systematic trend could be observed.

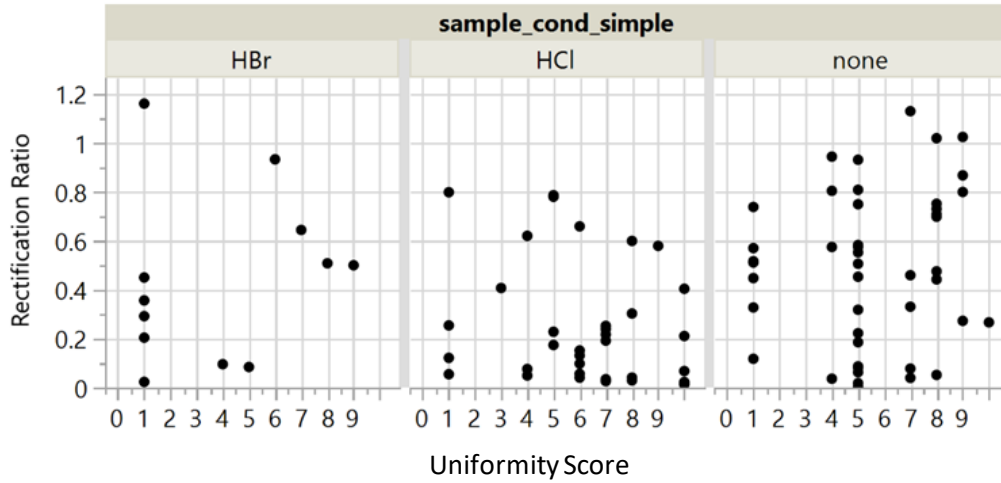


**Figure 3-4:** (a) Median Flake thickness vs normalized current densities at 0.5 V (b) Normalized I-V characteristics color coded with the median flake thickness in the device.

ii) *Rectification ratio vs uniformity score:*

The non-scaling behavior of the Ge-MoS<sub>2</sub> I-V characteristics with respect to the flake thickness could be because of poor quality flakes being considered for observing a trend. So, a trend in rectification ratio with respect to the flake scores was tested, to sort out flakes having poor rectification ratio. As can be seen from the plots in **Figure 3-5**, no consistency in rectification ratio

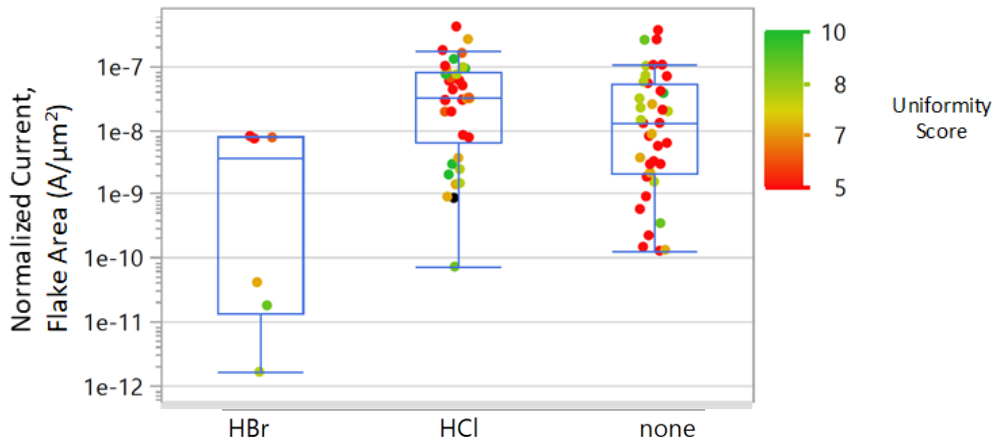
can be observed for any flake score. As noted before, most of the rectification ratios are between 0 and 1, which means the reverse bias current is higher than forward bias current.



**Figure 3-5:** Rectification ratio vs Uniformity Score of flakes.

iii) *Area-normalized forward current vs. Uniformity score:*

It was tested whether the area-normalized forward current shows some pattern with the uniformity scores for the flakes. However, as can be seen from the plots of **Figure 3-6**, the distribution of uniformity score with respect to the corresponding current in the device appears to be random.



**Figure 3-6:** Uniformity Score distribution for normalized currents at 0.5 V.

### 3.5 Explaining deviations from expected trends

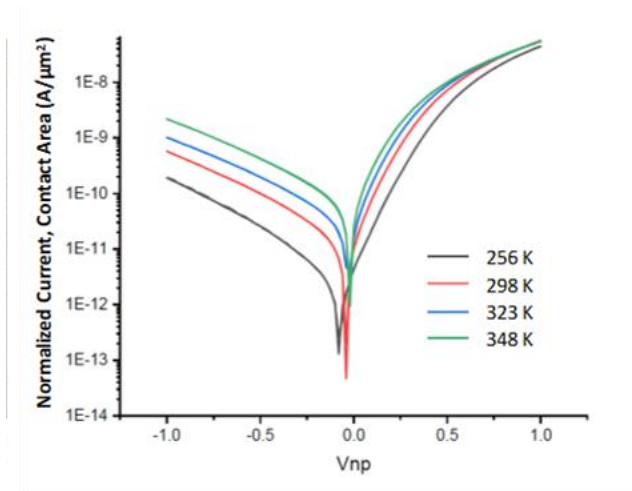
#### 3.5.1 Additional TCAD simulations of non-idealities

To investigate why there is a strong deviation between measured characteristics and the simulations in **Figure 1-7** (b), additional simulations were performed by Dr. Quentin Smets to verify the effect of various non-idealities: the impact of MoS<sub>2</sub> doping concentration, MoS<sub>2</sub> mobility, MoS<sub>2</sub> flake thickness, metal-MoS<sub>2</sub> Schottky barrier height and tunneling mass, BTBT rate, and Ge/MoS<sub>2</sub> band alignment. These simulations were run to see if they can qualitatively explain the deviation of I-V characteristics obtained from our fabricated Ge-MoS<sub>2</sub> devices. The simulation results can be found in Appendix A – Non-ideality simulations. The effects of non-idealities that could be causing deviation from the expected results are summarized there. Only when incorporating BTBT in the simulations, or with extremely low MoS<sub>2</sub> doping concentration, show nearly no rectification, which is more in line with the I-V characteristics of our devices.

#### 3.5.2 Temperature-dependent measurements

Temperature-dependent IV measurements are useful to test whether BTBT and/or TAT are the dominant current mechanisms in reverse bias, and responsible for the experimentally measured absence of rectification. Since BTBT is not thermally activated, the current is typically nearly

temperature independent. Therefore I-V characterization at different temperatures were performed for one of our devices, where the Ge substrate was treated with HCl. As can be seen from **Figure 3-7**, the reverse bias current appears to be relatively less temperature dependent than the forward bias current, suggesting that tunneling could be dominant in the reverse bias. As explained in section 1.6.2, direct BTBT is not expected in our devices with the consideration of low doping concentration of MoS<sub>2</sub> flakes and therefore long tunneling paths. Therefore, either the doping concentration of MoS<sub>2</sub> flakes is higher than expected, or we are observing TAT in our devices. Future efforts to extract activation energies for each of these processes would help confirm this interpretation. In the next section, we discuss examples from the literature that are related to our work suggesting TAT in Ge-MoS<sub>2</sub> devices, and variation of doping concentration in MoS<sub>2</sub> flakes.



**Figure 3-7:** Temperature dependent I-V characteristics of Ge-MoS<sub>2</sub> diodes suggesting tunneling in reverse bias.

### 3.5.3 Comparison with literature

#### i) *Trap-assisted tunneling at the Ge-MoS<sub>2</sub> interface*

To study the temperature dependent I-V characteristics of the Ge-MoS<sub>2</sub> heterostructure interface, similar Ge-MoS<sub>2</sub> diode devices were fabricated by Son *et al.* [27]. In their devices, the MoS<sub>2</sub> is only 3 layers (2.9 nm) thick, which is extremely thin compared to our work (average

thickness of MoS<sub>2</sub> flakes is 120 nm). Also, the doping level of Ge is 10<sup>17</sup> cm<sup>-3</sup> which is much lower than in our work. To remove the native oxide, the Ge surface was treated with dilute HF solution (H<sub>2</sub>O: HF = 100: 1). In the analysis done by the authors of this work, the current at high temperature (above 300 K) is shown to be dominated by thermionic emission. At lower temperatures (below 300 K), the current is shown to be due to TAT at low bias and due to Fowler-Nordheim tunneling (FNT) at higher bias.

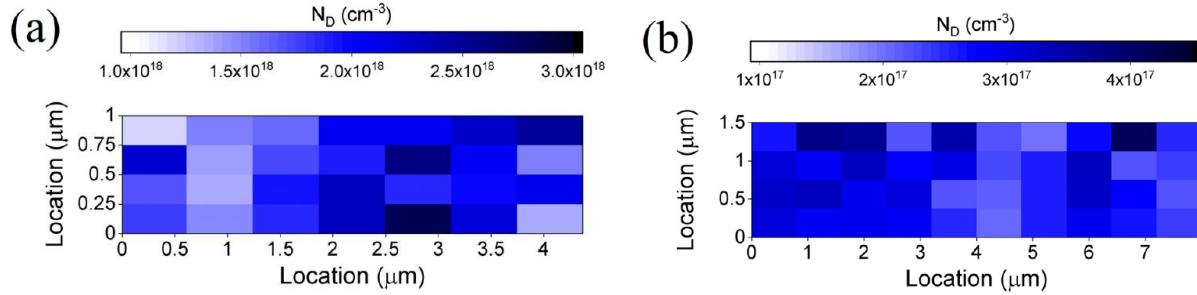
As discussed in the previous section, the temperature dependent I-V characteristics in our devices also suggest current due to some sort of tunneling mechanism in the reverse bias. In our devices, however, since an average thickness of MoS<sub>2</sub> flakes is 120 nm, compared to 2.9 nm thick in this work, FNT is not expected, only Tunneling in our devices could be TAT. If indeed, we observe similar TAT in our device where the Ge substrate was treated with HCl, either HCl treatment was ineffective, or the additional trap sites were introduced in our devices after HCl treatment. Re-introduction of trap sites could be due to prolonged dip in IPA causing an introduction of hydroxide (OH<sup>-</sup>) trap sites, or from hydrocarbons in the air. More temperature-dependent I-V tests for our devices in which the Ge substrate is either untreated or treated with HBr could help us observe effect of various levels of trap sites (higher for as-is case and lower for HBr) and figure out if TAT is indeed occurring.

ii) *Doping non-uniformity within the same device*

Dagan *et al.* [21] calculated the doping concentration in contacted MoS<sub>2</sub> flakes from the lateral electric field, obtained by Kelvin Probe Force Microscopy (KPFM), and from the measured current and mobility. They show that thick 85-layer flakes have a lower average doping concentration (2×10<sup>17</sup> cm<sup>-3</sup>) as compared to few layer and single layer flakes (2×10<sup>18</sup> cm<sup>-3</sup>). The doping concentration of multilayer MoS<sub>2</sub> flakes used in our simulations (5×10<sup>18</sup> cm<sup>-3</sup>), is an order

of magnitude higher than their result for thick flakes. For our Ge-MoS<sub>2</sub> devices, the simulation results in Appendix A – Non-ideality simulations show a lower doping concentration should result in lower current both in forward and reverse bias.

Dagan *et al.* [21] also show that the doping concentration might vary significantly across the same flake, as shown in **Figure 3-8**. The variation of doping level across a single flake might cause many parallel paths for current to flow from Ge to MoS<sub>2</sub> to the metal contact with varying energy barrier heights. This might explain the random variations in the I-V characteristics of our devices.



**Figure 3-8:** Doping concentration mapping of (a) monolayer MoS<sub>2</sub> Flake and (b) multilayer (85 layers) MoS<sub>2</sub> Flake obtained via KPFM [21]

### 3.5.4 Other possible sources of deviation

An uncertainty in band-alignment, possibly due to halide treatment (as discussed in section 1.5), and uncertainty in doping concentrations, are causes for deviation from the expected PN diode characteristics. A couple of situations can be discussed:

- i) Lower effective bandgap for BTBT: Due to an accumulation region at Ge surface from halide treatment (causing upward band-bending), the actual effective bandgap could be even less than 0.42eV, which is obtained by alignment of the vacuum levels. Then, BTBT might be dominant in reverse bias.

- ii) MoS<sub>2</sub> being p-doped: Another explanation for the observed I-V characteristics could be that MoS<sub>2</sub> is actually p-type. It should be noted that a literature review of p-type doping in MoS<sub>2</sub> indicates a very low likelihood of p-type behavior in unintentionally doped films. Instead, it is expected that p-type doping can only be achieved via intentional doping techniques [28], [29], [30] and [31]. In this situation, a high hole current (transport by majority carriers) is expected both in forward and reverse bias. At the heterojunction, there would be thermionic emission of holes over the potential barrier formed by the valence band offset at the heterojunction. Direct tunneling through the potential barrier would also be a contributing conduction mechanism.

# CHAPTER 4

## CONCLUSIONS AND FUTURE WORK

### 4.1 Conclusions

The aim of this work was to improve the Ge/MoS<sub>2</sub> interface quality by removing the native GeO<sub>x</sub>, passivate the Ge surface, fabricate Ge/MoS<sub>2</sub> PN diodes, and electrically characterize those diodes to identify the best passivation technique. Different types of device designs and flake transfer techniques have been compared to identify the most suitable approach for our work. As discussed in section 2.4, it was concluded that devices without isolation layer and direct scotch-tape transfer are optimal, offering both the shortest CTL and highest device yield.

However, the electrical characteristics show large deviations from the expected results from TCAD simulations. A higher reverse bias current than forward bias is obtained and a large device-to-device variability of 4 decades in current density is observed. Therefore, it is not possible to link the effects of wet-chemical halogen acid treatments for removal of GeO<sub>x</sub> and passivation of Ge to the electrical characteristics of the PN diodes. However, the analysis of this deviation has led to understanding of various non-idealities that might be present in the Ge-MoS<sub>2</sub> device like deviation in band-alignment and non-uniformity in MoS<sub>2</sub> doping concentration.

### 4.2 Future Work

Band bending at the Ge surface was observed by XPS in an earlier study, and it was predicted that this would reduce the effective BTBT barrier height at the Ge-MoS<sub>2</sub> interface in future TFETs. Our current I-V characterization results make it difficult to draw a conclusion about the effectiveness of this approach. To compare the effect of wet chemical halogen acid treatment

for improving the Ge-MoS<sub>2</sub> interface, it is first important to know the exact band-alignment of Ge-MoS<sub>2</sub> heterostructure, which can be obtained via Internal Photoemission (IPE) studies [10], [11].

Figuring out the doping of the MoS<sub>2</sub> flakes will be the next most important task. This will result in more accurate TCAD simulations to understand the band diagram and the exact transport mechanism in Ge-MoS<sub>2</sub> devices. Only with a fair understanding of expected I-V characteristics, a Ge-MoS<sub>2</sub> device can be designed that will help in electrically characterizing the effect of removal of GeO<sub>x</sub>, and also, ultimately realizing a TFET device.

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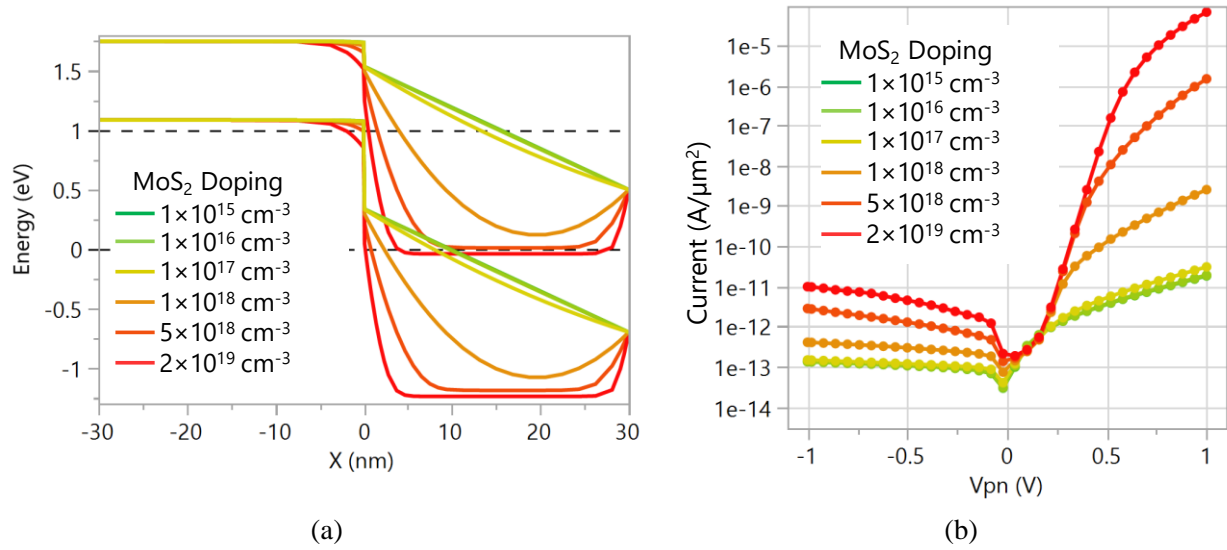
## APPENDICES

## Appendix A – Non-ideality simulations

To explain the trend of equal forward and reverse currents in our devices, simulations incorporating some non-idealities were run by Dr. Quentin Smets to see if any of these known non-idealities exhibit the similar trends.

### a. Doping concentration of MoS<sub>2</sub>

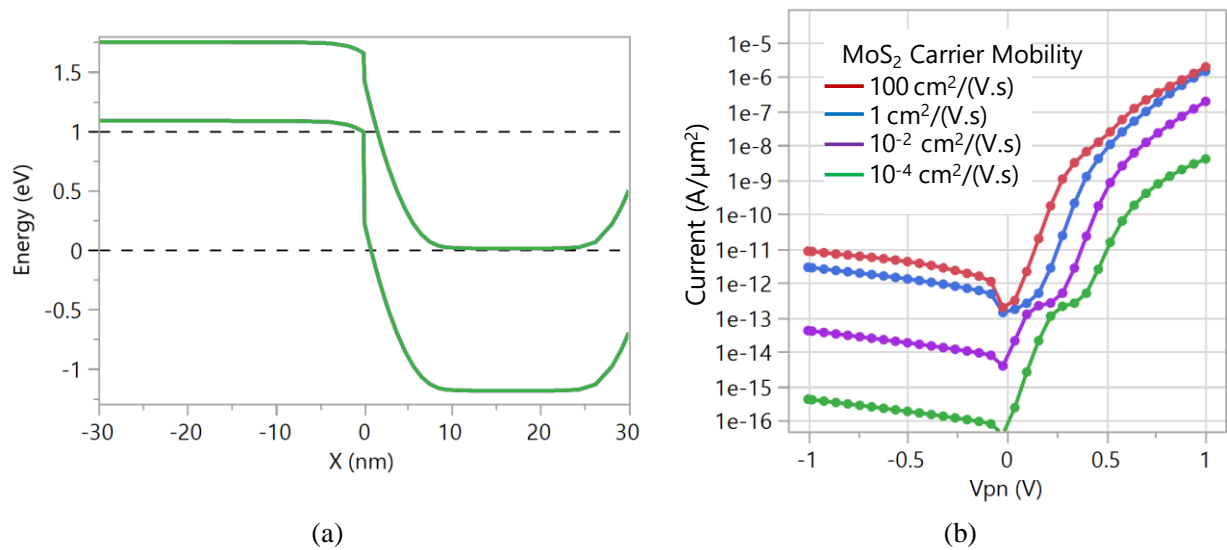
There always exists some unintentional doping in MoS<sub>2</sub> flakes, typically caused by uncontrolled Sulfur vacancies. These are present in bulk crystals and more might be created during processing of flakes for use in devices [21]. Since the doping concentration of our MoS<sub>2</sub> flakes is unknown – even the order of magnitude – simulations were performed to understand the effects of doping concentration in MoS<sub>2</sub> on the I-V characteristics. The band diagrams in **Figure 5-1** show a lower doping level leads to a large depletion region in MoS<sub>2</sub>. At the lowest doping levels ( $10^{15} \text{ cm}^{-3}$  and  $10^{16} \text{ cm}^{-3}$ ), the depletion regions from the Schottky barrier and from the PN junction merge, and the 30 nm thick flakes are fully depleted. This leads to very poor injection of electrons at the MoS<sub>2</sub>/metal Schottky barrier, and very poor forward bias current.



**Figure 5-1:** (a) The band alignment and (b) corresponding I-V characteristics for different doping concentrations.

b. Mobility of MoS<sub>2</sub>

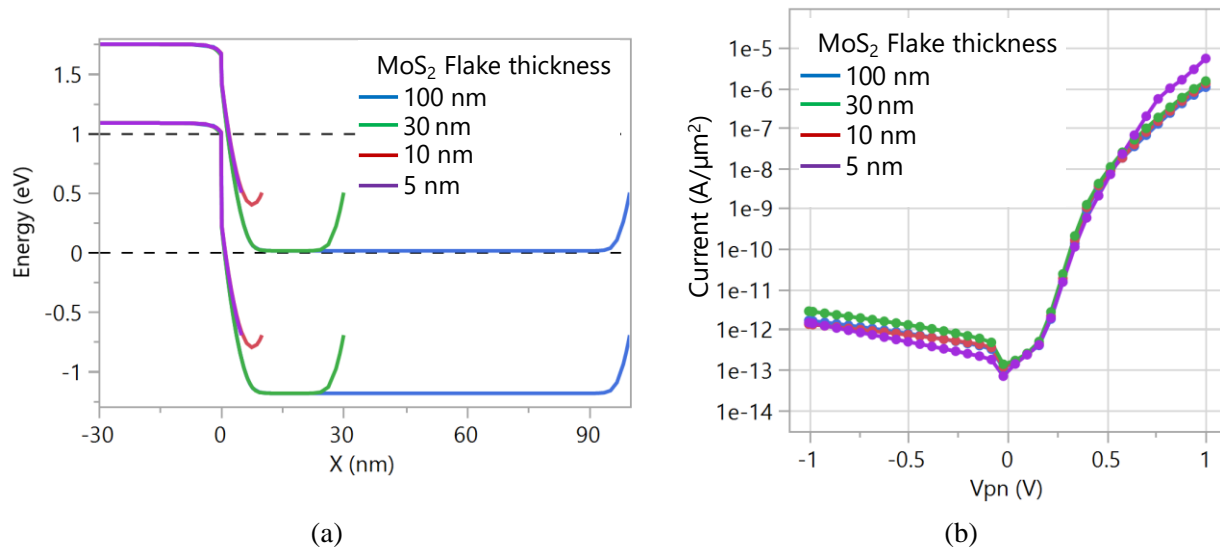
Simulations considering varying out-of-plane carrier mobilities were run, as can be seen from the results in **Figure 5-2**, lower mobility leads to an equally lower forward and reverse bias current.



**Figure 5-2:** (a) The band alignment and (b) corresponding I-V characteristics for different out-of-plane MoS<sub>2</sub> carrier mobilities.

c. Thickness of MoS<sub>2</sub>:

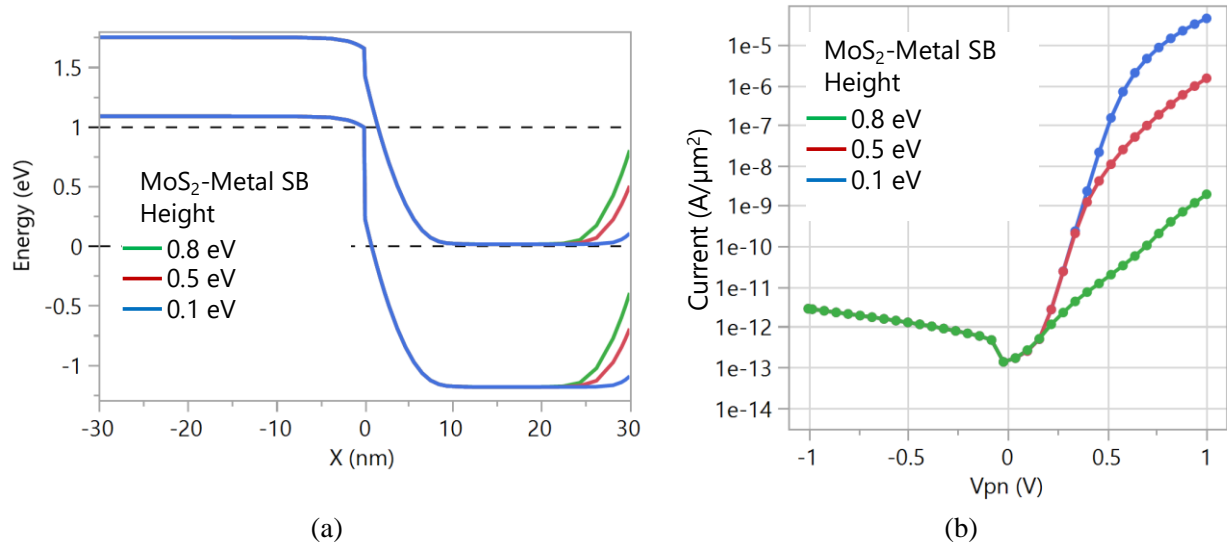
Flake thickness is a variable due to scotch-tape exfoliation. The simulation considers the effect of flake thickness with respect to the depletion width. As discussed in section 1.6.2, MoS<sub>2</sub> flakes need to be thicker than the depletion width in our devices. As can be seen from the simulation results in **Figure 5-3**, as long as flake is thicker than the depletion width, not much difference in I-V characteristics is expected. If the flake becomes thinner than the depletion width, the rectification can actually be due to Schottky junction formation in vertical heterostructure devices with vertical contacts [32], regardless, a high rectification ratio is expected.



**Figure 5-3:** (a) The band alignment and (b) corresponding I-V characteristics for different MoS<sub>2</sub> flake thickness.

d. Schottky barrier height at MoS<sub>2</sub>/metal contact:

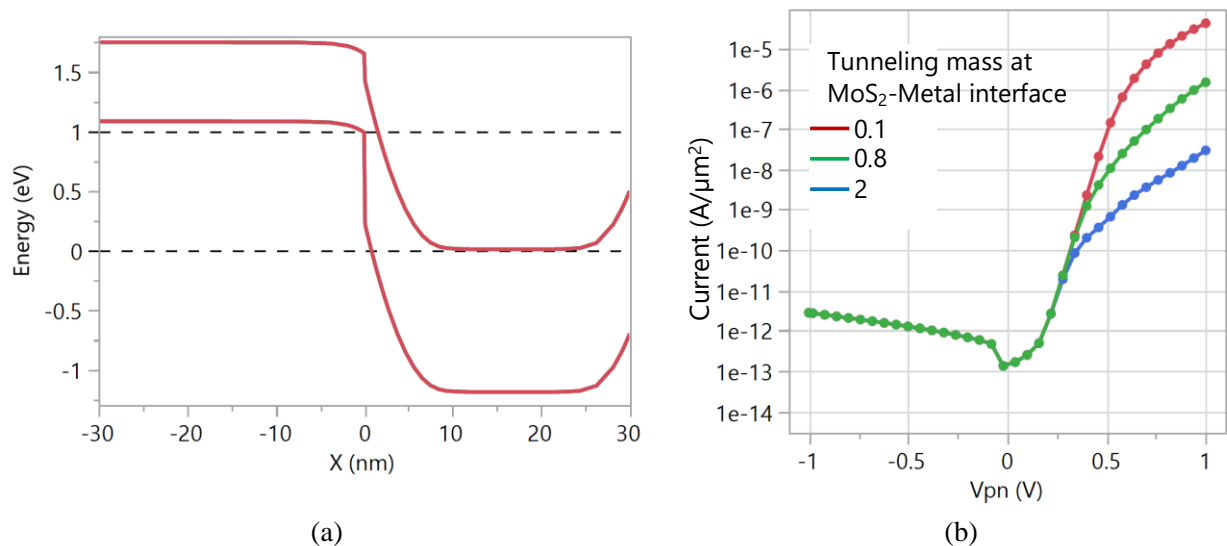
An uncertainty in Schottky barrier height also exists. As seen from the simulation results in **Figure 5-4**, if the Schottky barrier height at metal contact is higher, this will lead to a lower forward-bias current due to poor injection of electrons.



**Figure 5-4:** (a) The band alignment and (b) corresponding I-V characteristics for different Schottky Barrier heights at MoS<sub>2</sub>-metal contact.

e. Tunneling mass at MoS<sub>2</sub>/metal contact

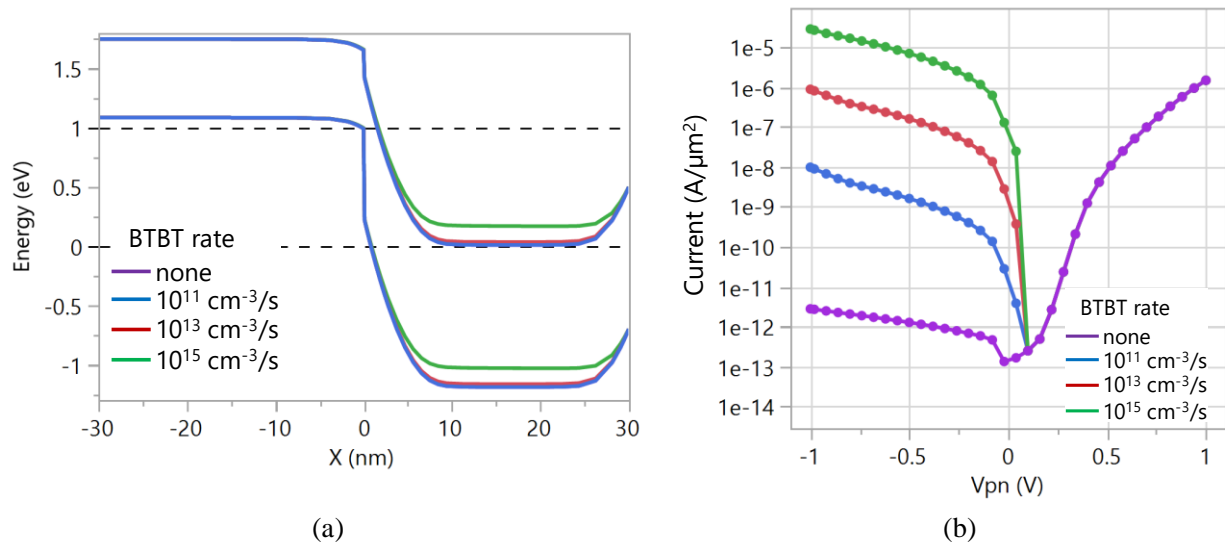
Simulations to investigate varying out-of-plane tunneling mass for MoS<sub>2</sub> carriers were run, as can be seen from the results in **Figure 5-5**, a higher tunneling mass leads to lower forward-bias current.



**Figure 5-5:** (a) The band alignment and (b) corresponding I-V characteristics for different out-of-plane tunneling mass of MoS<sub>2</sub> charge carriers.

f. Impact of BTBT from Ge to MoS<sub>2</sub>:

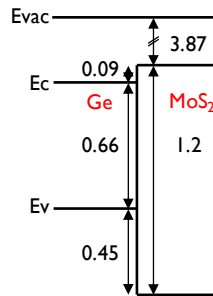
From the simulations with a reference MoS<sub>2</sub> doping concentration  $N_D=5\times 10^{18}\text{cm}^{-3}$ , tunnel path lengths of 2 nm – 10 nm at  $V_{np} = 1\text{V}$  are obtained (**Figure 5-6**), which is quite short. If the doping concentration of MoS<sub>2</sub> flakes is even higher than  $N_D=5\times 10^{18}\text{cm}^{-3}$ , the tunnel paths would be even shorter and BTBT and/or Trap-Assisted-Tunneling (TAT) might be observed. Also, IPE studies [10], [11] show that actual band-alignment might vary significantly, this could lead alignment of band-gaps such that the effective band-gap between valance of Ge and Conduction of MoS<sub>2</sub> might be lower than the reference 0.42eV, this, coupled with the accumulation region at the surface of Ge due to halide ions, and local variability in doping concentration of the flakes, could lead to TAT and/or BTBT. As seen from the simulation results, BTBT would severely increase the reverse bias current, and the current in reverse bias might be higher than in forward bias. Accurate models for BTBT in 3D/2D heterojunctions are not yet available, hence BTBT is only for qualitative insight.



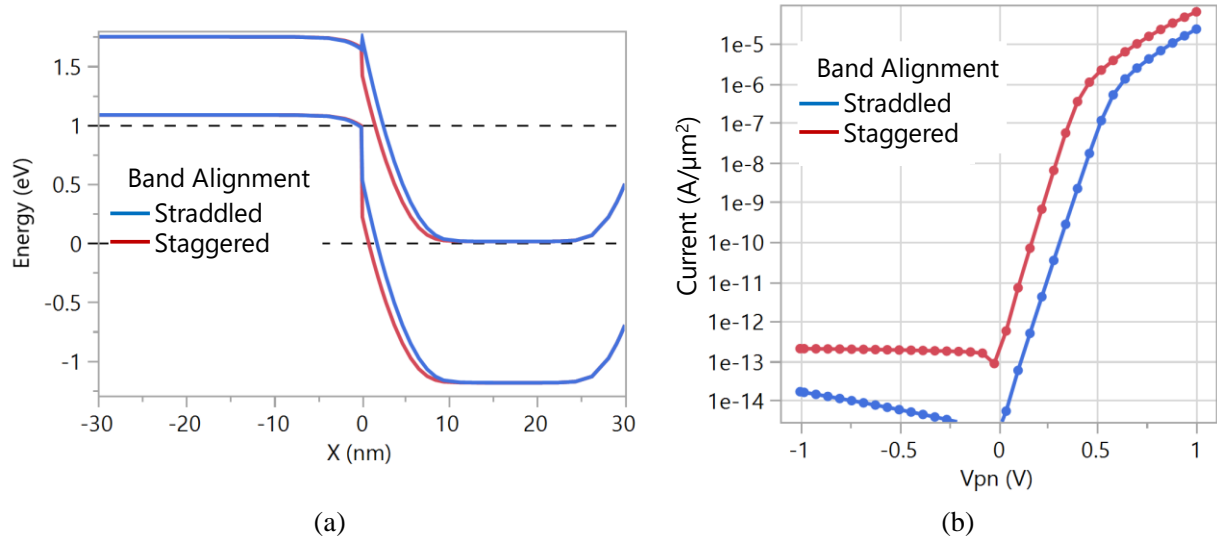
**Figure 5-6:** (a) The band alignment and (b) corresponding I-V characteristics for different BTBT rates at the Ge-MoS<sub>2</sub> interface.

g. Straddled band alignment

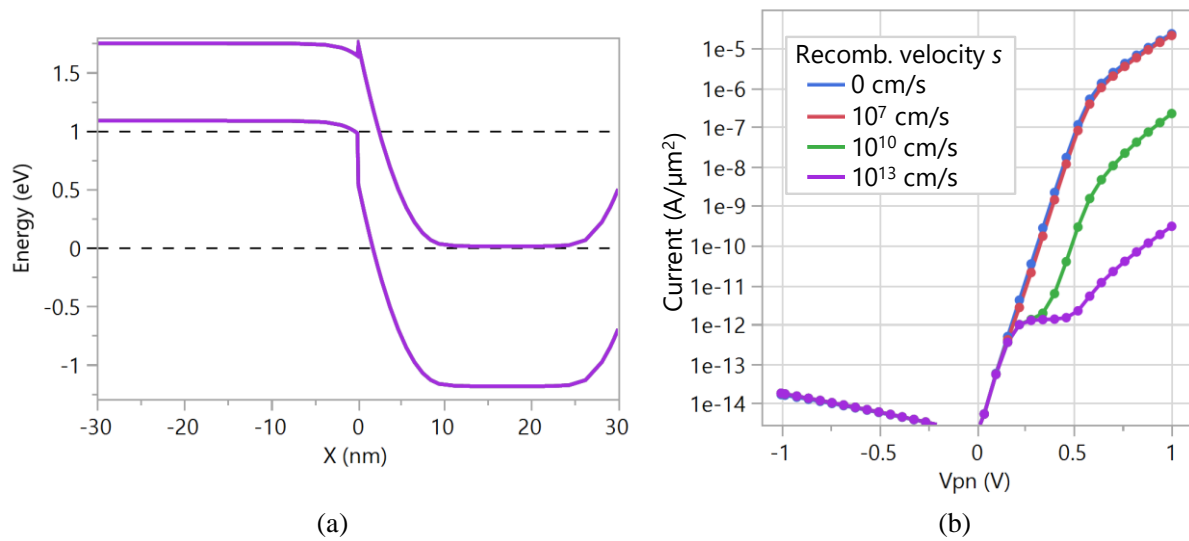
Although a staggered band-alignment is expected for Ge-MoS<sub>2</sub> devices by alignment of vacuum levels [3]. IPE measurements [10], [11] of the Ge/SiO<sub>2</sub> and MoS<sub>2</sub>/SiO<sub>2</sub> systems, in combination with the transitivity principle [10], suggest that the band alignment of Ge-MoS<sub>2</sub> heterostructure might actually be straddled rather than staggered, as shown in the **Figure 5-7**. **Figure 5-8** shows the simulation results for straddled (in blue) and staggered (in red) band-alignments, as can be seen that similar trend with respect to rectification ratio being high, is observed. **Figure 5-9** shows the effect of higher recombination velocities in I-V characteristics with straddled band-alignment, as can be seen the forward current reduces for increased recombination velocities. **Figure 5-10** shows the effect of reduced doping concentration of MoS<sub>2</sub> for straddled Ge-MoS<sub>2</sub> band-alignment, the forward bias current collapses for reduced doping concentration of MoS<sub>2</sub>



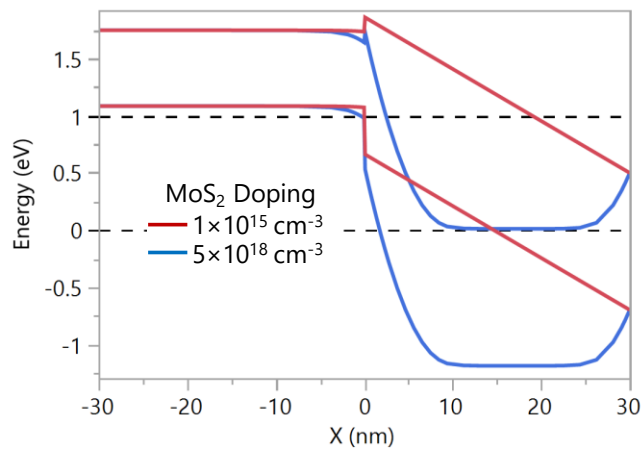
**Figure 5-7:** Instead of a staggered band alignment, a straddled band alignment is obtained via application of transitivity principle and separately obtained valance band offsets of MoS<sub>2</sub> and Ge from IPE on MoS<sub>2</sub>-SiO<sub>2</sub> and SiGe-SiO<sub>2</sub>. All values are in units of eV.



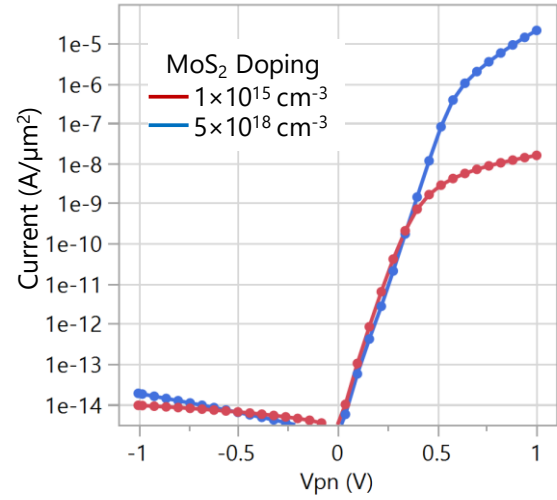
**Figure 5-8:** (a) The band alignment and (b) corresponding I-V characteristics for straddled and staggered bands.



**Figure 5-9:** (a) The band alignment and (b) corresponding I-V characteristics for straggled condition with different recombination velocities.



(a)



(b)

**Figure 5-10:** (a) The band alignment and (b) corresponding I-V characteristics for straddled condition with different doping concentrations.

## Appendix B – Detailed Fabrication Flow

### Diodes with isolation layer:

#### A) Formation of SiO<sub>2</sub> openings:

- i) 50 nm of SiO<sub>2</sub> was grown on the p<sup>++</sup> Ge surface via NOC CVD tool.
- ii) The die was mounted in Laurel spin-coater chuck.
- iii) Titanium prime, serving as resist adhesion promoter, was drop-casted on to the die and spun at 4000 rpm for 30 seconds.
- iv) The die was then baked at 120 °C for 2 minutes.
- v) The die was then again mounted on the vacuum chuck and IX845 photoresist was drop-casted on top of the die and spun at 4000 rpm for 30 seconds.
- vi) The die was then baked at 120 °C for 2 minutes.
- vii) The die was loaded on MA6 photolithography tool, for 2.4 seconds of exposure, to transfer the pattern for SiO<sub>2</sub> openings.
- viii) The die was developed for 90s under OPD5262 followed by microscope and Dektak profilometer inspection to confirm the developed resist profile.
- ix) The thin layer polymer residues in the developed areas was removed in a descum step by soft CCP O<sub>2</sub> plasma etch for 3 minutes.
- x) Dektak inspection was done to confirm removal of the polymer residues in the developed areas.
- xi) To form the openings in the isolation layer, the SiO<sub>2</sub> was etched in Buffered Hydrofluoric acid (BHF) for 33 seconds.
- xii) Dektak profilometer inspection was done to confirm the etch of SiO<sub>2</sub>.

- xiii) To strip away the remaining resist, the die was kept under hot acetone at 50 °C for 15 minutes followed by ultrasonication in acetone for 5 minutes, IPA at 50 °C for 5 minutes and then dried with N<sub>2</sub> gun.
- xiv) Microscope inspection was done to check for etch pattern.

**B) Flake Transfer:**

- i) The die is then treated with HCl or HBr for 10 mins for removal/passivation of GeO<sub>x</sub>, followed by Isopropyl alcohol (IPA) rinse.
- ii) Flakes were transferred onto scotch tape and kept ready to be transferred onto the die immediately after it was removed from IPA and blown with N<sub>2</sub> gun.
- iii) The die was then placed under Dichloromethane (DCM) for about 10 minutes to remove PMMA and the tape residues.
- iv) The flakes were then identified, and images were taken.

**C) Formation of Contacts:**

- i) The die was then again mounted on the spinner and IX845 photoresist was drop-casted on top of the die and spun at 4000 rpm for 30 seconds.
- ii) The die was then baked at 120 °C for 2 minutes.
- iii) The die was loaded on the MA6 mask aligner tool for 2.4 seconds of exposure to transfer pattern for contacts.
- iv) The die was developed for 90 seconds under OPD5262 followed by microscope and Dektak profilometer inspection to confirm development profile.
- v) 10 nm of Nickel and 20 nm of Palladium was deposited on the die by metal evaporation.

- vi) Lift-off was performed by placing the die under acetone at 50 °C for 30 minutes followed by IPA rinse and N<sub>2</sub> dry.

### **Diodes without isolation layer:**

#### **A) Formation of metal markers:**

In order to identify the flakes, metal markers were formed on germanium substrate. The steps involved are as follows:

- i) A die was mounted on Laurel spin-coater chuck.
- ii) LOR-1A was drop-casted on top of the die and spun at 4500 rpm for 30 seconds. LOR-1A was used to promote lift-off.
- iii) The die was then baked at 190 °C for 3 minutes.
- iv) The die was then again mounted on the vacuum chuck and IX845 photoresist was drop-casted on top of the die and spun at 4000 rpm for 45 seconds.
- v) The die was then baked at 120 °C for 2 minutes.
- vi) The die was loaded on MA6 tool for 2.4 seconds of exposure.
- vii) The die was developed for 90 seconds under OPD5262 followed by microscope inspection to confirm development profile.
- viii) 20 nm of Titanium and 70 nm of Gold was deposited on the die via evaporation.
- ix) For lift-off, the die was placed under Acetone for 30 minutes followed by IPA rinse and Nitrogen gun drying.
- x) The die was then again dipped in OPD5262 for around 8 seconds to remove LOR followed by water rinse, dip in NPA for 5 seconds and drying with Nitrogen gun.

**B) Flake Transfer:**

- i) The die is then treated with HCl or HBr for 10 mins for removal/passivation of  $\text{GeO}_x$  followed by IPA rinse.
- ii) Flakes were transferred onto scotch tape and kept ready to be transferred onto the die immediately after it was removed from IPA and blown with N<sub>2</sub> gun.
- iii) The die was then placed under DCM for about 10 minutes to remove the tape residues.
- iv) The flakes were then identified, and images were taken under 50x magnification for making contact polygons using “KLayout” CAD tool.

**C) Formation of Contacts:**

- i) The die with the flakes was then mounted again on the vacuum chuck of Laurel spin-coater tool.
- ii) LOR-1A was drop-casted on top of the die and spun at 4500 rpm for 45 seconds.
- iii) Post-bake at 190 °C for 3 minutes was performed.
- iv) PMMA 3C was spin coated on the die for 45 seconds at 4500 rpm.
- v) Post-bake at 165 °C for 3 minutes was performed.
- vi) e-beam exposure was performed on the die using contact layer mask made with KLayout.
- vii) The die was placed under 1:1 solution of Methyl isobutyl ketone (MIBK): Isopropyl alcohol (IPA) for around 50 seconds for development followed by 30 seconds of 1-Propanol rinse.
- viii) LOR was removed by placing the die under OPD5262 for 3 seconds followed by water rinse and NPA dip for 5 seconds.
- ix) 10 nm of Nickel and 20 nm of Gold was deposited on the die by evaporation.

- x) Lift-off was performed by placing the die under acetone at 50 °C for 30 minutes followed by IPA rinse and N<sub>2</sub> dry.
- xi) To remove LOR, the die was treated with OPD5262 for 8 seconds followed by water rinse and NPA dip for 5 seconds.