ABSTRACT

Mo, Hongxiang. Formation of Low-Resistivity Germanosilicide Contacts to Phosphorus Doped Silicon-Germanium Alloy Source/Drain Junctions for Nanoscale CMOS. (Under the direction of Mehmet C. Öztűrk)

Conventional source/drain junction and contact formation processes can not meet the stringent requirements of future nanoscale complimentary metal oxide silicon (CMOS) technologies. The selective $Si_{1-x}Ge_x$ source/drain technology was proposed in this laboratory as an alternative to conventional junction and contact schemes. The technology is based on selective chemical vapor deposition of in-situ boron or phosphorus doped $Si_{1-x}Ge_x$ alloys in source/drain areas. The fact that the dopant atoms occupy substitutional sites during growth make the high temperature activation anneals unnecessary virtually eliminating dopant diffusion to yield abrupt doping profiles. Furthermore, the smaller band gap of $Si_{1-x}Ge_x$ results in a smaller Schottky barrier height, which can translate into significant reductions in contact resistivity due to the exponential dependence of contact resistivity on barrier height. This study is focused on formation of self-aligned germanosilicide contacts to phosphorous-doped $Si_{1-x}Ge_x$ alloys. The experimental results obtained in this study indicate that self-aligned nickel germanosilicide ($NiSi_{1-x}Ge_x$) contacts can be formed on $Si_{1-x}Ge_x$ layers at temperatures as low as 350ºC. Contacts can yield a contact resistivity of 10^{-8} ohm-cm^2 with no sign of germanosilicide induced leakage. However, above a threshold temperature determined by the Ge concentration in the alloy, the $NiSi_{1-x}Ge_x/Si_{1-x}Ge_x$ interface begins to roughen, which affects the junction leakage. For phosphorus doped layers considered in this study, the threshold temperature was around 500ºC, which is roughly 100ºC higher than the threshold temperature for $NiSi_{1-x}Ge_x$ contacts formed on boron doped $Si_{1-x}Ge_x$ layers with

a Ge percentage of ~ 50%. Nickel and zirconium germanosilicides were also considered as contact candidates but they were found to result in a contact resistivity near 10^{-7} ohm-cm^2.

FORMATION OF LOW-RESISTIVITY GERMANOSILICIDE CONTACTS TO PHOSPHORUS DOPED SILICON-GERMANIUM ALLOY SOURCE/DRAIN JUNCTIONS FOR NANOSCALE CMOS

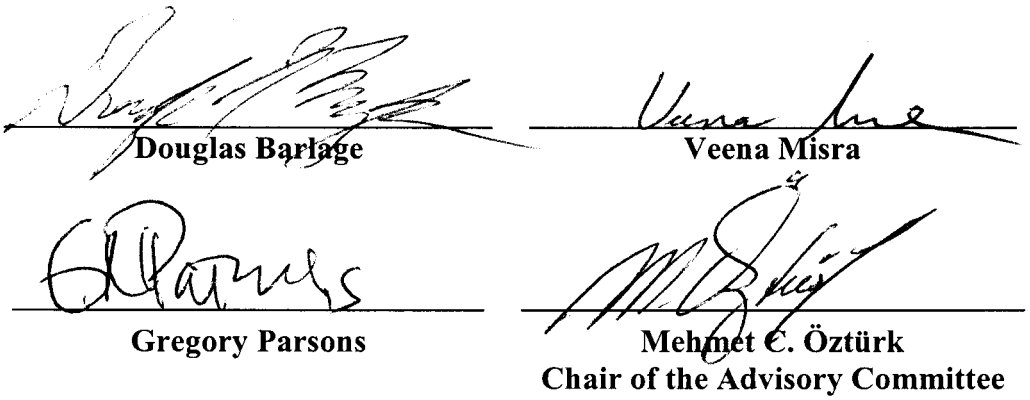
By Hongxiang Mo

A dissertation submitted in partial fulfillment of the requirements for the degree of

Doctor of Philosophy

Electrical and Computer Engineering

North Carolina State University



Biography

I was born in July 10th, 1973 in Guilin, China. I finished my elementary school, and high school in the town of Yongfu in Guangxi province. In the fall of 1991, I was admitted to Fudan University in Shanghai. I spent 8 years in Fudan University to complete my Bachelor of Science (B.S.) and Master of Science (M.S.) degrees in the department of electronic engineering. My advisor for my M.S. thesis was professor Bing-Zong Li. My thesis was on the formation of ternary silicide, $(NiCo)Si_2$. In the Fall of 1999, right after receiving my Master's degree, I came to Raleigh, North Carolina. I continued my graduate studies in the department of electrical and computer engineering at North Carolina State university for the direction of Dr. Mehmet C. Öztürk. The funding for my research was provided by Semiconductor Research Center (SRC) and SEMATECH.

Acknowledgments

I wish to express my deep gratitude to my advisor Dr. Mehmet C. Öztürk, who gave me great guidance and support during my Ph.D. studies. He led me to a treasure of knowledge and showed me what a scientist should be. The experience of doing research in Dr. Öztürk's group was invaluable to me.

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The majority of my research was done in the AEMP clean room. Without the continuous help from the staff members, my Ph.D. could not be possible. I would like to thank Joan O'Sullivan, Harold Morton, Henry Taylor, Dr. Ginger Yu, Tina McNulty, John Todd and Myrick Peacock. I would like to thank SRC/SEMATECH for providing funding for my Ph.D. research.

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I. Introduction

About half a century ago, Shockley, Bardeen and Brattain invented the first transistor. Since then, the semiconductor technologies advanced rapidly. After the invention of the integrated circuit, the number of transistors included in a chip increased according to Moore's law [1]. To achieve higher density, higher speed and lower power consumption both vertical and lateral device dimensions have been continually scaled. The Metal-Oxide-Silicon Field-Effect-Transistor (MOSFET) is currently entering the nanoscale regime through continuous improvements in processes and device design.

Fabrication of high quality shallow source/drain has always been an important branch of scaling efforts. With continuous scaling of device dimensions, IC performance is becoming more and more dependent upon the parasitic series resistance of the source/drain junctions and their contacts.

I.1 Contact Resistance Challenge for Nanoscale CMOS

To meet the international technology roadmap for semiconductors (ITRS) requirements, the total junction series resistance must be a small fraction of the channel 'on' resistance [2], as shown in Figure I-1. A key contributor to the parasitic resistance is the contact resistance of the junctions. Figure I-2 shows the maximum contact resistivity that can be tolerated assuming that the entire series resistance is due to the contact resistance. As shown, a contact resistivity of ~ 10^{-8} ohm-cm^2 will be required, which is an order of magnitude lower than the current state of art.

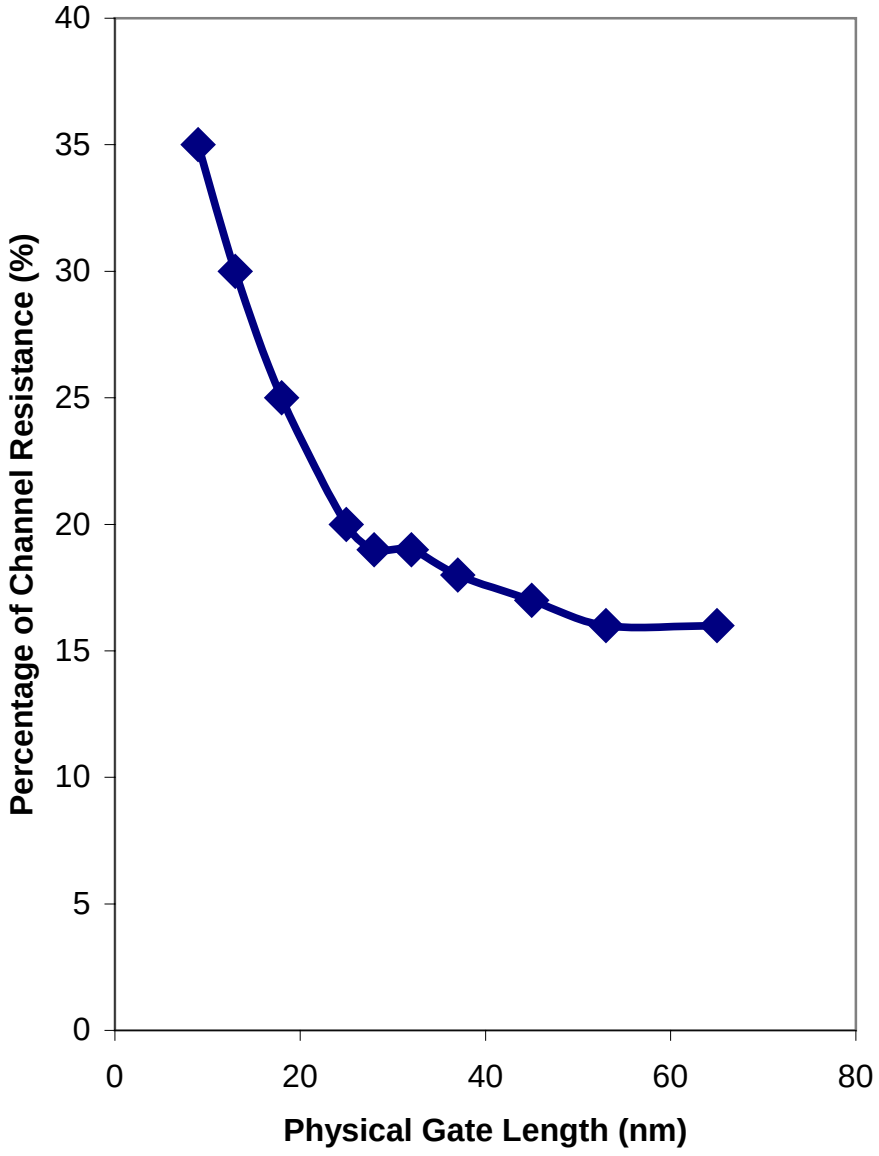

Figure I-1 Parasitic source/drain resistance as percentage of ITRS year channel resistance (V_{dd}/I_{dd}).

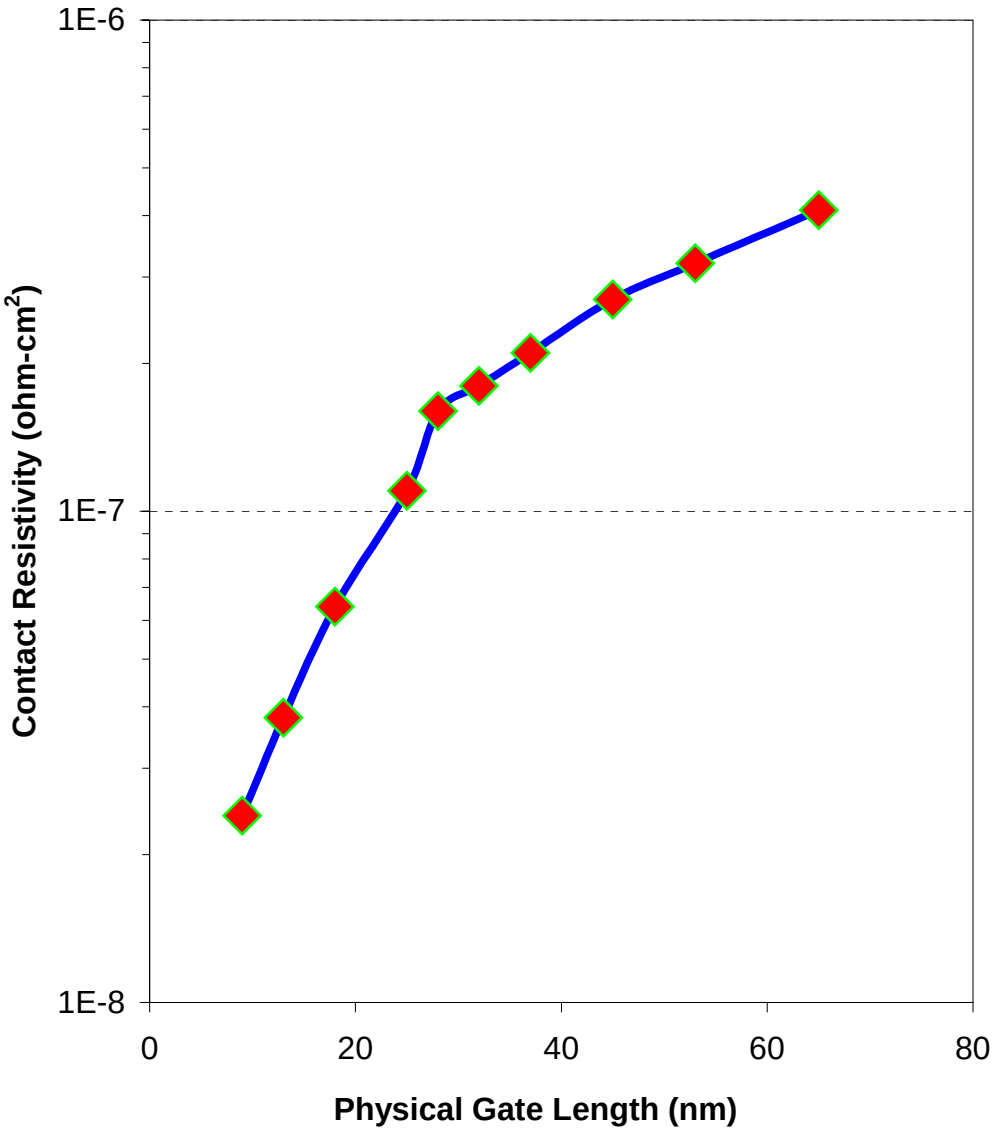

Figure I-2 The maximum specific contact resistance required by ITRS roadmap

The contact resistivity of a metal/semiconductor contact can be modeled by assuming field emission through the Schottky barrier as the dominant conduction mechanism. With this assumption, the contact resistivity can be expressed as [3]:

$$\rho_c(FE) = \rho_{c0} \exp\left(\frac{2\phi_B\sqrt{m^*\varepsilon_s}}{\hbar\sqrt{N_D}}\right)$$

In the above expression, ϕ_B is the Schottky barrier height, N_D is the doping level, ε_s is the dielectric permittivity of silicon, $\hbar$ is Planck's constant and ρ_{c0} is a function of N_D and T. Figure I-3 shows the contact resistivity plotted as a function of the Schottky barrier height and doping density immediately under the contact metal. One can conclude from this figure why the existing contact technologies cannot meet the contact resistivity requirements of future CMOS technologies. Presently, silicides are used as contacts to source/drain junctions. Most silicides have their Fermi levels near the Si midgap, which results in a Schottky barrier height of roughly half the Si bandgap or ~ 0.6 eV. Using this barrier height and ~ 10^{20} cm^{-3} as the maximum boron activation level in Si we obtain a contact resistivity of ~10^{-7} ohm-cm^2, which is too high for future CMOS technology nodes as demonstrated in Figure I-4.

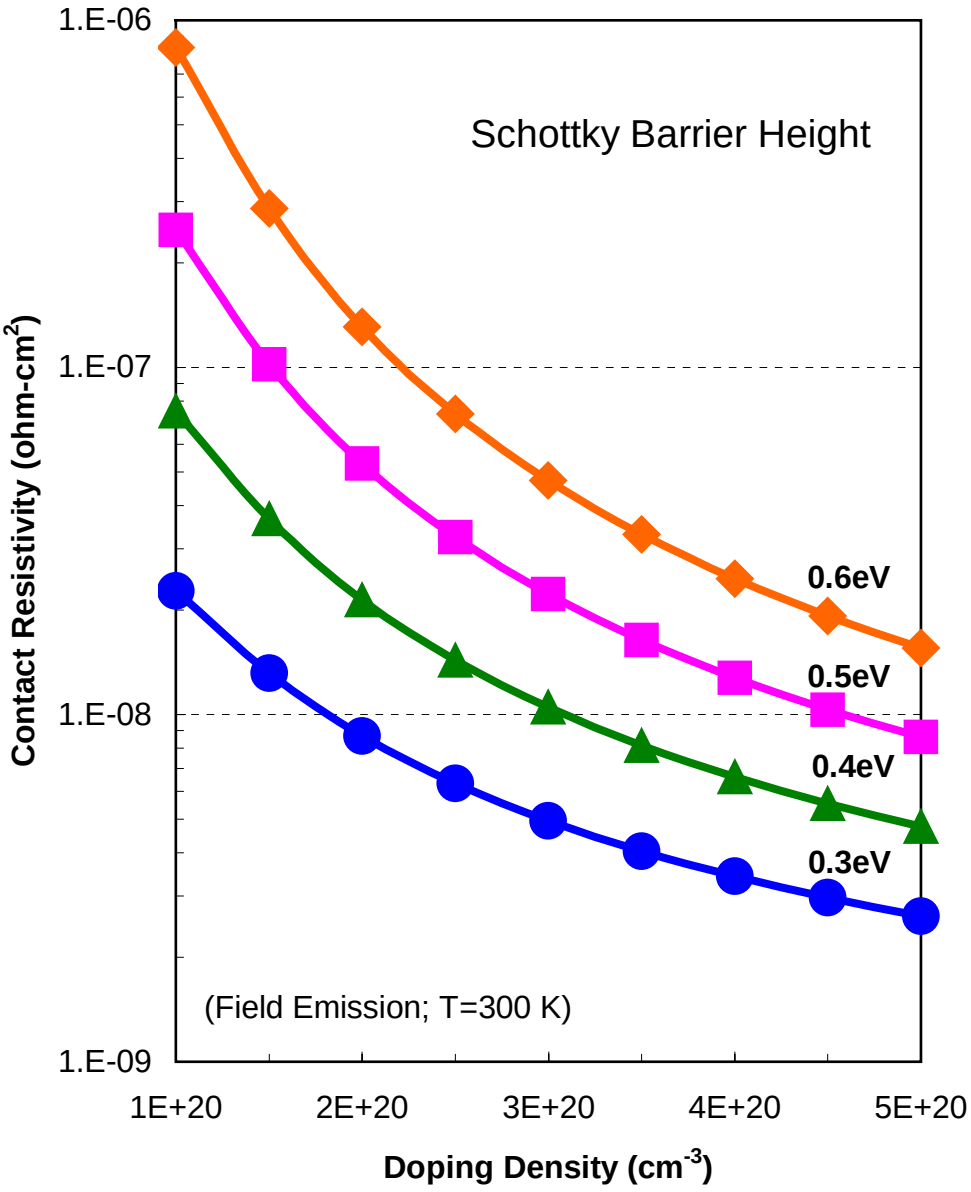

Figure I-3 The simulation curves of specific contact resistance as a function of substrate doping level and Schottky barrier height

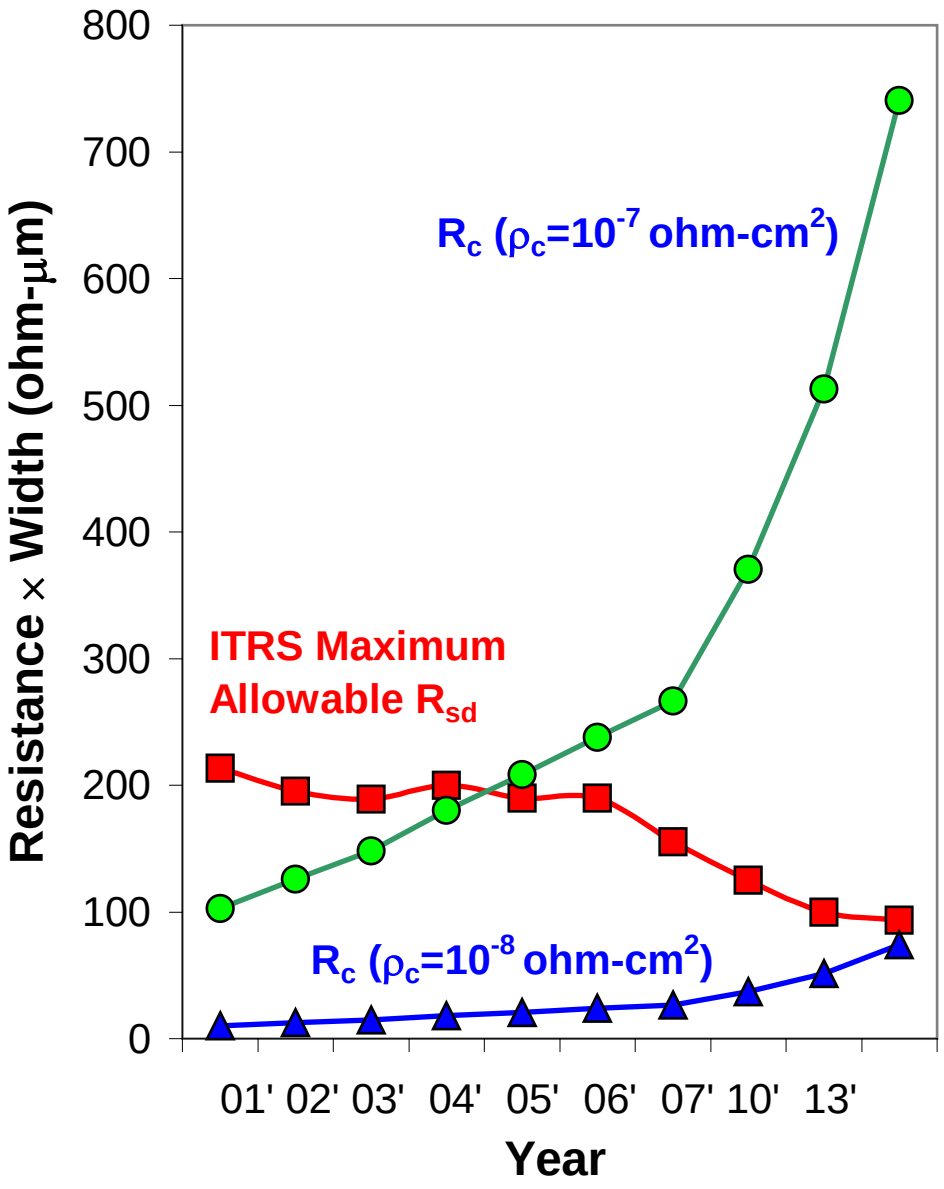

Figure I-4 Maximum allowable parasitic source/drain resistance (shown as -■-), contact resistance with ρ_c = 1 x 10^{-7} ohm-cm^2 (-●-) and ρ_c = 1 x 10^{-8} ohm-cm^2 (-▲-) plotted as functions of the technology year.

I.2 Selective Si_xGe_{1-x} Source/Drain Technology

A new ultra shallow junction technology was developed in this laboratory to meet the ITRS requirements for nanoscale CMOS. The technology is illustrated in Figure I-5. In this technology, in-situ boron doped $Si_{1-x}Ge_x$ layers are selectively deposited into recessed source/drain areas by chemical vapor deposition. By compensating the strain in the $Si_{1-x}Ge_x$ alloy using large concentrations of boron, very high boron activation levels are achieved at temperatures as low as 500°C. Another advantage of this technology is that $Si_{1-x}Ge_x$ has a lower bandgap, which results in a lower contact barrier height. Therefore, the new technology can provide a higher doping level as well as a low barrier height, which are both essential for reducing the contact resistivity. A detailed discussion of the new technology can be found in a PhD thesis by S. Gannavaram [4] and previous publications[5,6]. More recently, INTEL has announced the company's new 90 nm CMOS technology featuring the same $Si_{1-x}Ge_x$ junctions and claimed that the junctions introduced just the right amount of strain in the channel to boost the hole mobility.

In addition to the contact resistance advantage, the $Si_{1-x}Ge_x$ junctions are highly abrupt since a high temperature activation anneal is not required after epitaxy. Thus, the junctions can deliver a much lower spreading resistance than the junctions formed by ion-implantation. Finally, the junctions are deposited at T < 800ºC, which can be an advantage with advanced gate stack materials such as high-K dielectrics or metal gate electrodes.

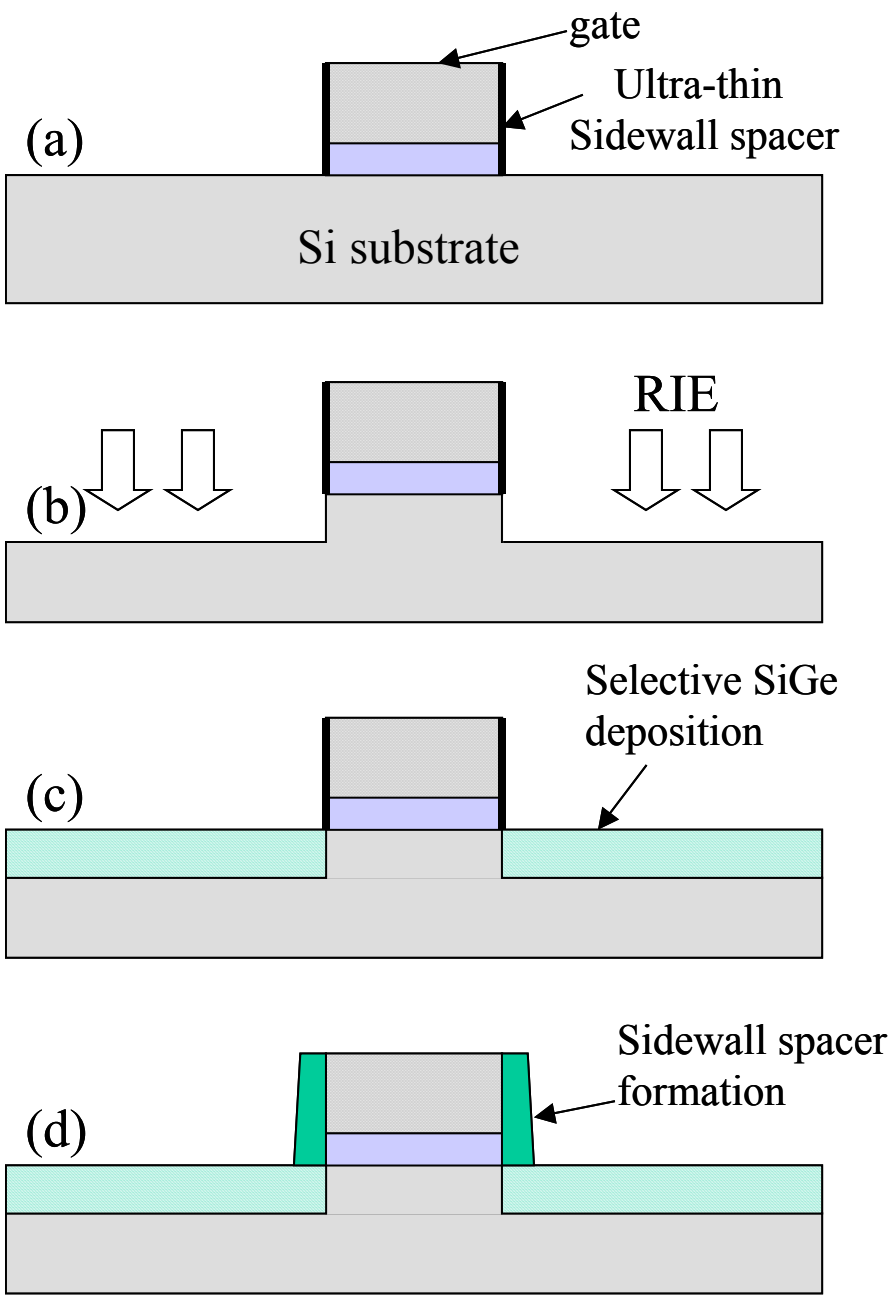

Figure I-5 Fabrication sequence of recessed $Si_{1-x}Ge_x$ source/drain junctions with selectively deposited $Si_{1-x}Ge_x$

Gannavaram's Ph.D. work on $Si_{1-x}Ge_x$ junctions was followed by I. Kang and N. Pesovic [7] and Jing Liu, who were also doctoral candidates working in the same laboratory. I. Kang worked on phosphorus doped $Si_{1-x}Ge_x$ alloys and the highlights of his work are summarized in the next section.

I.3 Deposition of In-Situ Phosphorous doped $Si_{1-x}Ge_x$

In this section, a brief summary of Inkuk Kang's work is given for reference purposes since the same layers were used to study metal $Si_{1-x}Ge_x$ reactions in this work.

To achieve the lowest contact resistivity possible, it is essential to use the highest Ge content possible to minimize the band gap and dope the material at least up to the solubility limit at the process temperature used. Unfortunately, I. Kang's work showed that phosphorous incorporation during CVD is not independent of the Ge content. This is demonstrated in Figure I-6, which shows the active Phosphorus concentration as a function of the Ge content in $Si_{1-x}Ge_x$ for films deposited in a temperature range of 670 – 810°C. The Ge content was obtained from XRD measurements. As shown in Figure I-6, phosphorus incorporation exhibits a maximum around 20 – 30 % Ge, which appears to change slightly with temperature. At the deposition temperature of 760°C, the highest phosphorous concentration is achieved when the Ge content is ~ 20%. At the lower temperatures of 720°C and 670°C, the highest phosphorous concentration is obtained with 30% Ge.

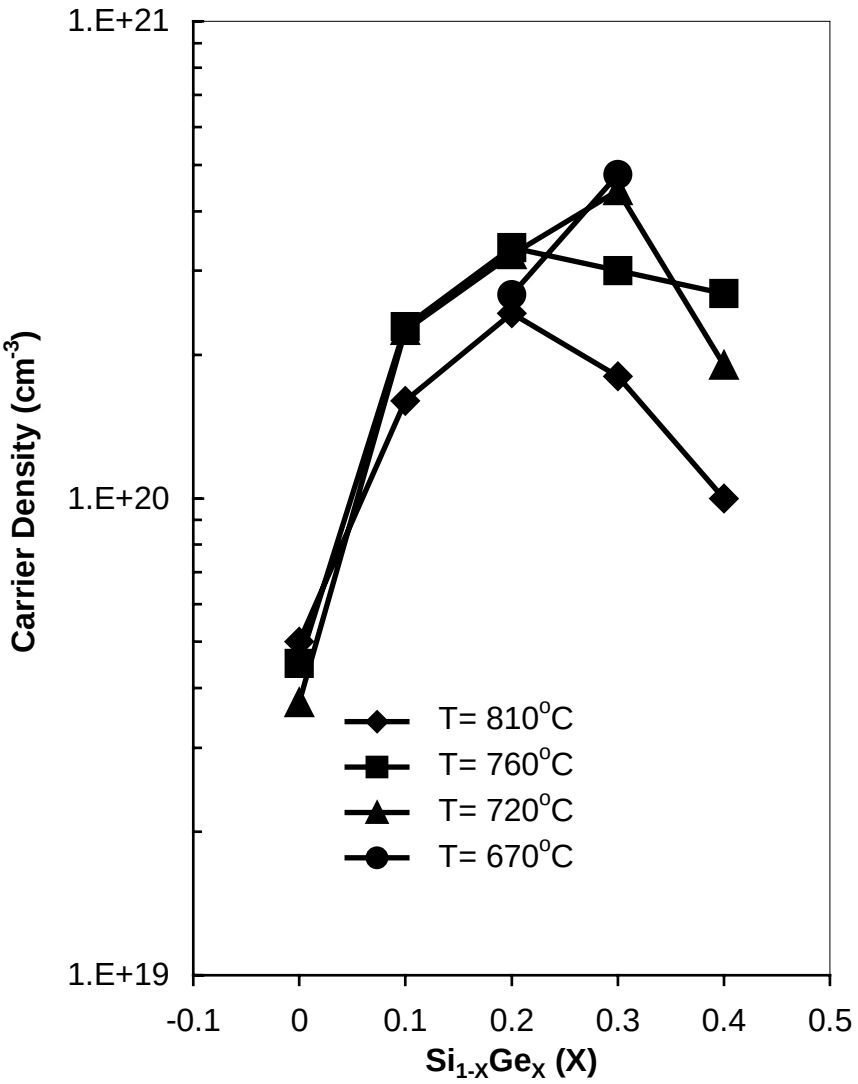

Figure I-6 Phosphorous density obtained at different temperatures for different Ge concentrations.

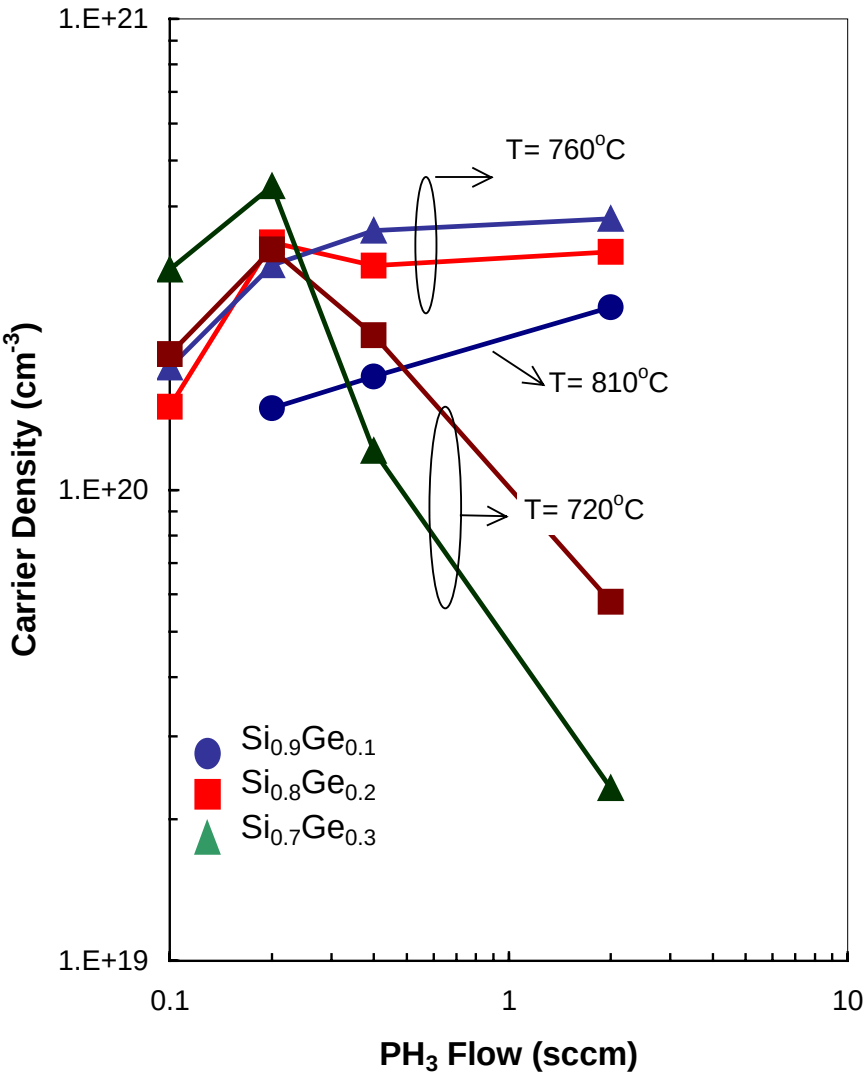

Figure I-7 Phosphorous density obtained at different temperatures using different PH_3 flows. Three different layers with different Ge concentrations were used.

The active carrier density is shown in Figure I-7 as a function of the PH_3 flow for different $Si_{1-x}Ge_x$ compositions. It can be seen that the phosphorus incorporation is a strong function of the PH_3 flow rate and the deposition temperature. At higher temperatures, phosphorus desorption from the surface reduces the phosphorus incorporation. At lower temperatures, phosphorus poisoning of the $Si_{1-x}Ge_x$ surface limits the incorporation process.

Based on the experimental data from I. Kang shown in Figure I-6 and Figure I-7 the films in this work were grown at 760°C with a Ge concentration of ~ 20% and a phosphorus concentration of $3 - 4 \times 10^{20}$ cm^{-3}. While the phosphorus concentration is less than desired for achieving a low contact resistance, we note that the numbers only represent average values obtained from Hall Effect measurements. In reality, I. Kang has noted that the phosphorus concentration in these layers is quite non-uniform due to phosphorus segregation at the surface during deposition. A typical atomic phosphorus profile obtained by SIMS is shown in Figure I-8, which demonstrates that the highest concentration exists at the surface, which is beneficial for low contact resistance. Relying on a Ge content within 20-30% is also not a big compromise due to the fact that strain compensation does not exist in these alloys as S. Gannavaram and J. Liu showed in their Ph.D. work for boron doped $Si_{1-x}Ge_x$. This means that the Ge content in these alloys could not be very high to keep the SiGe strained and to minimize the defects at the interface arising from the lattice mismatch.

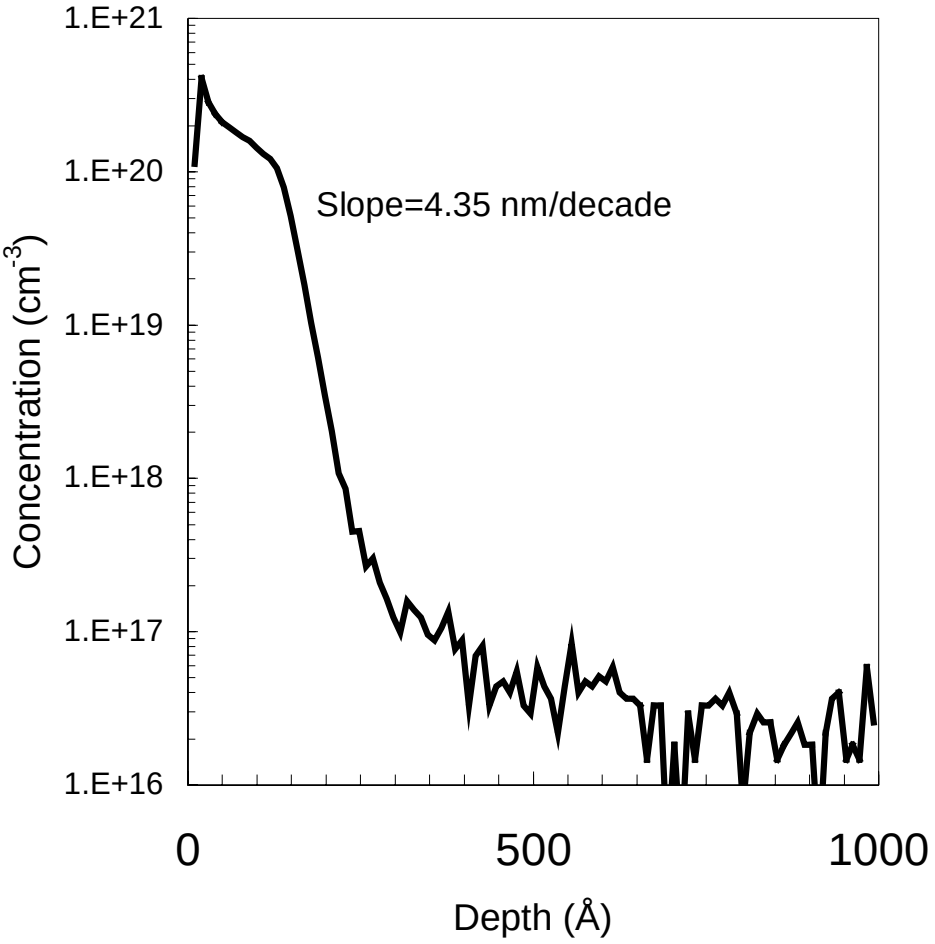

Figure I-8 A typical phosphorus profile obtained by SIMS in a $Si_{0.8}Ge_{0.2}$ layer deposited at 760°C.

I.4 Self-Aligned Germanosilicide Contacts to $Si_{1-x}Ge_x$ Alloys

$Si_{1-x}Ge_x$ alloys react with popular silicide metals forming germanosilicides. Similar to silicides, germanosilicides can be formed self-aligned to source/drain junctions. Unfortunately, metal-$Si_{1-x}Ge_x$ reactions are not as simple as the metal-Si reactions since germanosilicide is a ternary alloy.

I.4.1 Nickel Germanosilicide

Previous work on Ni-Ge reactions identified GeNi, Ge_3Ni_5, Ni_3Ge, $GeNi_2$, Ge_2Ni_5 and $Ge_{12}Ni_{19}$ as potential phases. NiSi and NiGe both have the orthorhombic structure with the lattice parameters given in Table I-1 [8]. As shown, the lattice constant of NiSi is smaller than that of NiGe. Therefore, we expect the lattice constant of $Ni(Si_{1-x}Ge_x)$ to be between that of NiSi and NiGe.

Table I-1 Lattice parameters of NiSi and NiGe

	A	B	C
NiSi	5.233	3.258	5.659
NiGe	5.381	3.428	5.811

$NiSi_{1-x}Ge_x$ was found to form at temperatures as low as 200°C in vacuum [9]. For annealing temperatures above 300°C, Ge out-diffusion from $Ni(Si_{1-x}Ge_x)$ was observed [9] and it was attributed to the large difference in the heats of formation of NiSi and NiGe (–45 and –32 KJ/mol) [10]. At higher temperatures, it was shown that Ge out-diffusion could result in formation of Ge rich $Si_{1-x}Ge_x$ islands between the NiSi grains.

The above mentioned instability was also observed for other metal-$Si_{1-x}Ge_x$ reactions. For example, $Co(Si_{1-x}Ge_x)$ is even less stable than $Ni(Si_{1-x}Ge_x)$ [11]. The heat of formation of CoSi and CoGe are –100.4 and –34.2 KJ/mol respectively, and the difference is higher than that of Ni.

I.4.2 Platinum Germanosilicide

The lattice parameters of PtSi and PtGe are compared in Table I-2 [8]. While PtSi and PtGe have the same orthorhombic lattice structure but the lattice constant of PtGe is about 2.4% larger than that of PtSi. H. K. Liou et al have studied the reactions between Pt and epitaxial $Si_{1-x}Ge_x$ films [12]. They showed that the germanosilicide could be formed at temperature as low as 350°C. Ge segregation was found at the surface and the surface Ge concentration increased with annealing temperature. The Schottky barrier height of Pt/n-$Si_{0.8}Ge_{0.2}$ was pinned at 0.68eV for different annealing temperatures. J.J. Peterson et al. have studied the reactions between Pt and $Si_{1-x-y}Ge_xC_y$ ($y<0.03$) layers [13]. X-ray diffraction data showed the formation of Pt_2(SiGeC) and Pt(SiGeC) after 600°C annealing. The contact resistivity of Pt($Si_{1-x}Ge_x$) to both n and p type $Si_{1-x-y}Ge_xC_y$ were determined to be 10^{-2} Ω*cm^2 for SiGeC doping level of 10^{18}cm^{-3}.

Table I-2 Lattice constants of PtSi and PtGe

	A	B	C
PtSi	5.94	5.60	3.60
PtGe	6.09	5.73	3.70

I.4.3 Previous Work on Germanosilicides at NC State University

The work on $Si_{1-x}Ge_x$ junctions in our laboratory was continued by Jing Liu who worked on formation of self-aligned germanosilicide contacts to boron doped $Si_{1-x}Ge_x$ junctions [14]. The main focus of his thesis was on nickel germanosilicide.

Figure I-9 shows the sheet resistance of $Ni(Si_{1-x}Ge_x)$ formed on undoped $Si_{0.5}Ge_{0.5}$ as a function of the annealing temperature. As shown, the thermal stability of Ni germanosilicide on undoped $Si_{1-x}Ge_x$ is very limited. For 10nm Ni, the maximum allowable temperature is less than 400°C. On the other hand, the thermal stability is much better on heavily boron doped $Si_{1-x}Ge_x$.

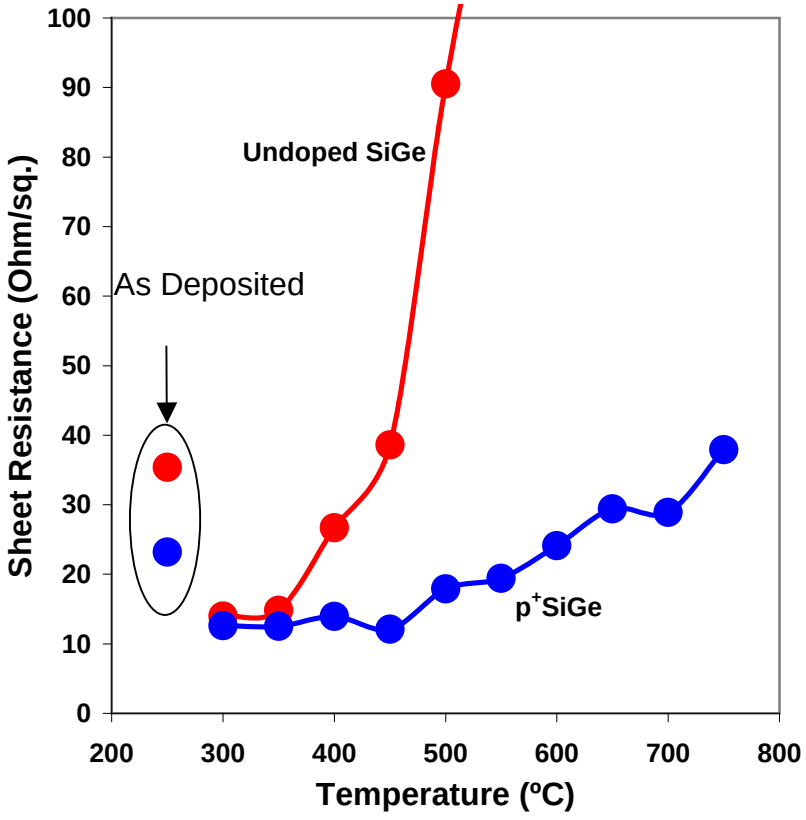

Figure I-9 Sheet resistance as a function of annealing temperature for 10 nm Ni on undoped and heavily boron doped $Si_{0.5}Ge_{0.5}$.

A cross-sectional TEM image of a Ni($Si_{1-x}Ge_x$) sample formed on boron doped $Si_{1-x}Ge_x$ at 400°C is shown in Figure I-10. No defects can be observed at the $Si_{1-x}Ge_x$/Si interface. The thickness of the original Ni and Ni($Si_{1-x}Ge_x$) are 10nm and 21 nm respectively and the thickness ratio of Ni($Si_{1-x}Ge_x$) to Ni is about 2.1, which is very close to that of NiSi. From these measurements, the resistivity of the Ni($Si_{1-x}Ge_x$) was determined to be 25μΩ-cm. Ni(SiGe) has low substrate consumption and low resistivity, which are both advantages for contacts to shallow junction.

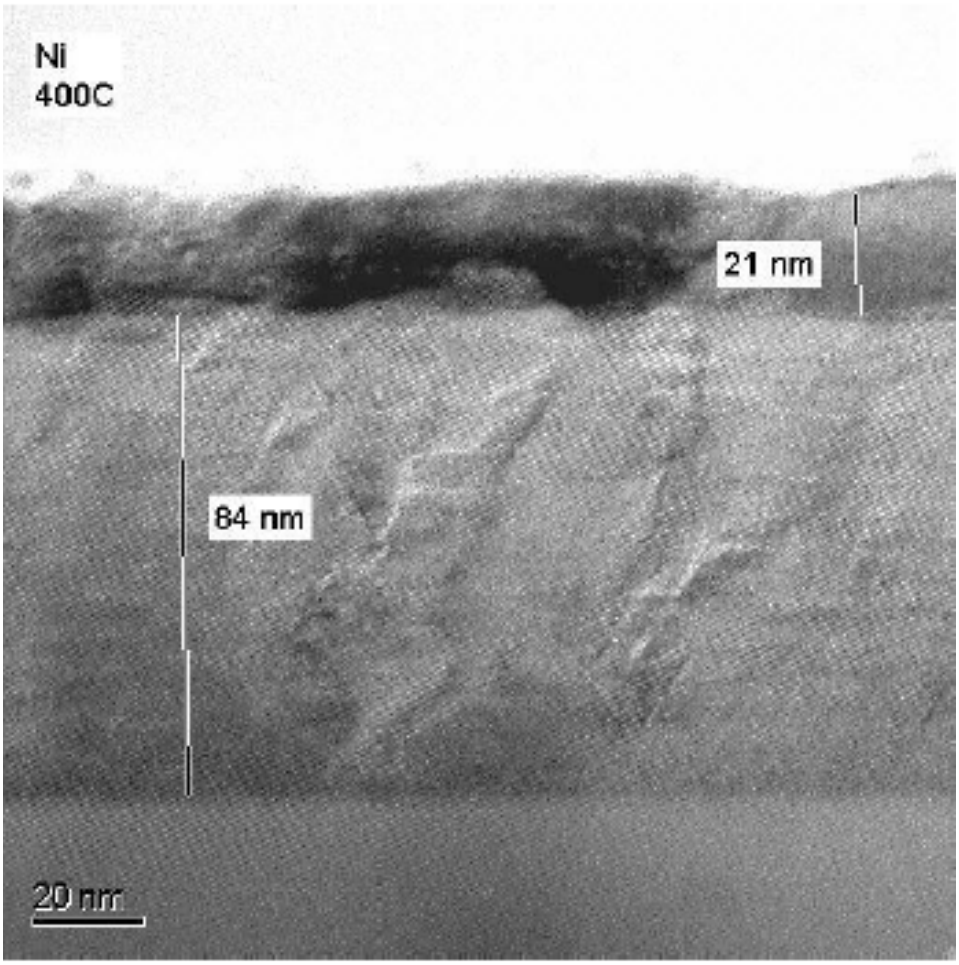

Figure I-10 Cross-sectional TEM image of Ni($Si_{1-x}Ge_x$) formed with 10nm Ni on P^+ $Si_{1-x}Ge_x$ at 400°C.

The leakage current of junctions with Ni($Si_{1-x}Ge_x$) contacts formed at different annealing temperatures are shown in Figure I-11. The diodes have the same active area of

600 x 600 μm^2 but three different contact areas. The junction leakage increases with the contact area for contacts formed at 500°C or higher, which indicates Ni($Si_{1-x}Ge_x$) induced junction leakage. On the other hand, the junction leakage of samples annealed at 400°C and below shows excellent leakage behavior.

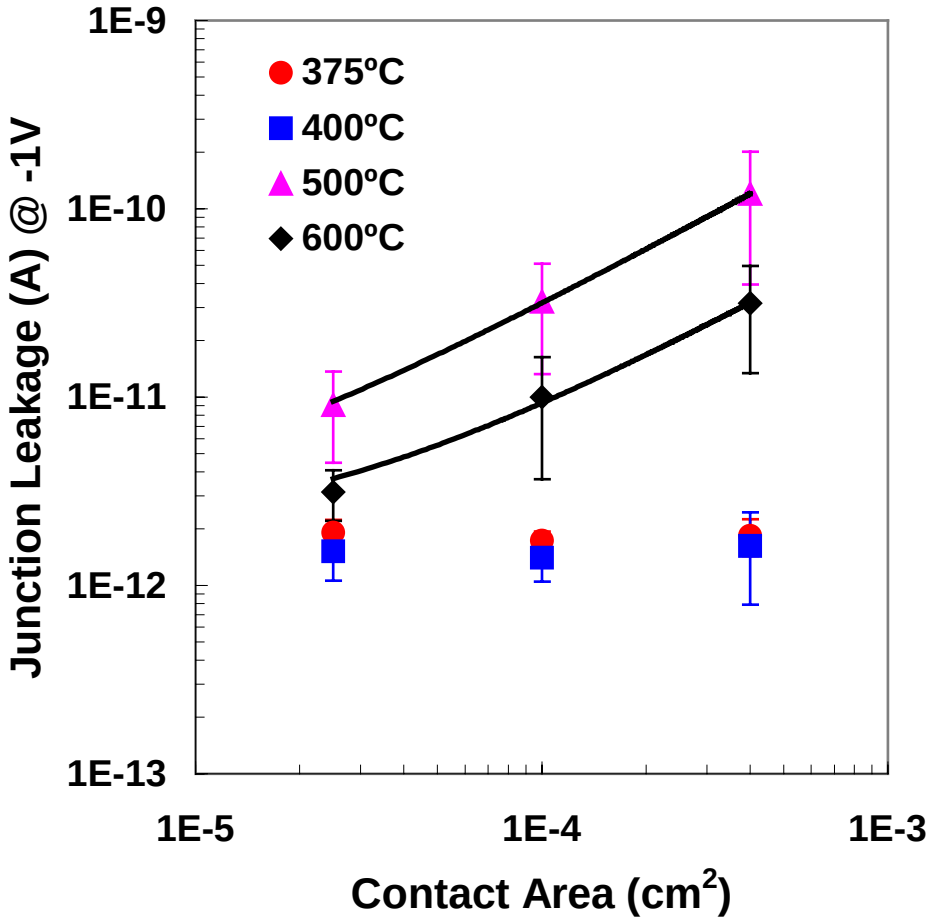

Figure I-11 Junction leakage at a reverse bias of -1V as a function of contact area for junctions with $NiSi_{1-x}Ge_x$ contacts formed at different temperatures.

Contact resistivity obtained Ni($Si_{1-x}Ge_x$) contacts on with $Si_{1-x}Ge_x$ with various boron concentrations and Ge percentage is shown in Figure I-12. As shown, the contact

resistivity is a function of the doping density as well as the germanium concentration. The two parameters can be optimized to reach a contact resistivity of ~10^{-8} Ω-cm^2.

Since the thermal stability of Ni($Si_{1-x}Ge_x$) on $Si_{1-x}Ge_x$ with 50% Ge content is poor, Jing Liu proposed using a Pt interlayer to improve the thermal stability of Ni($Si_{1-x}Ge_x$). As shown in Figure I-13, with a 1 nm Pt interlayer, the thermal stability of Ni($Si_{1-x}Ge_x$) formed on both undoped and P^+ $Si_{1-x}Ge_x$ are improved. Especially on boron doped $Si_{1-x}Ge_x$, the material appears to be stable at least up to 600°C.

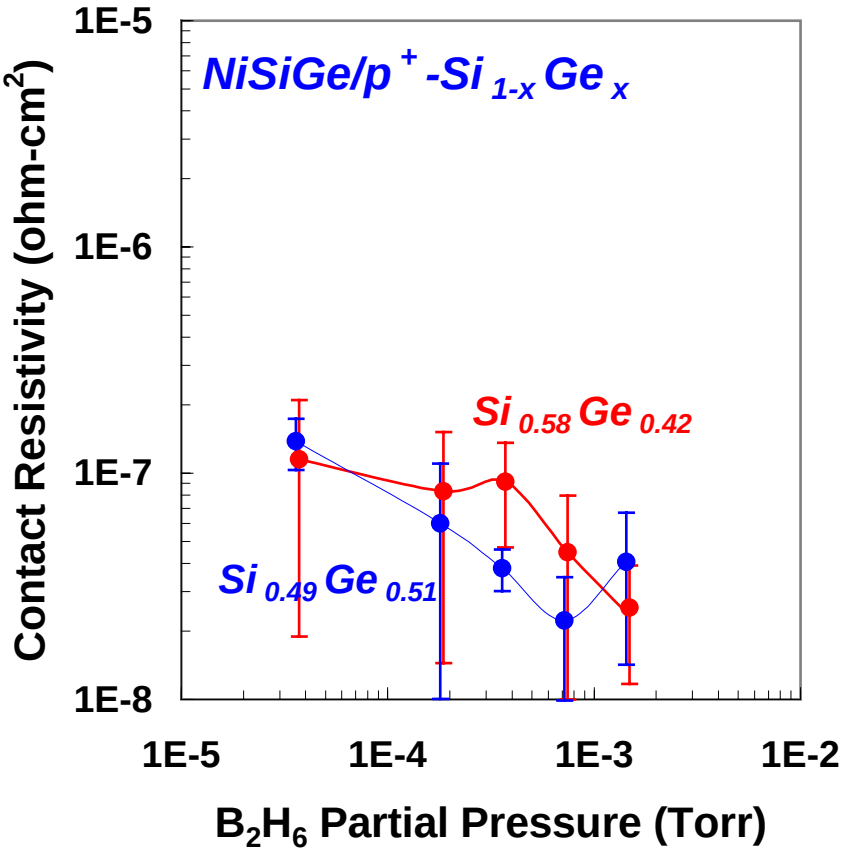

Figure I-12 Contact resistivity of Ni($Si_{1-x}Ge_x$) on P^+ $Si_{1-x}Ge_x$ with different doping concentrations and Ge contents.

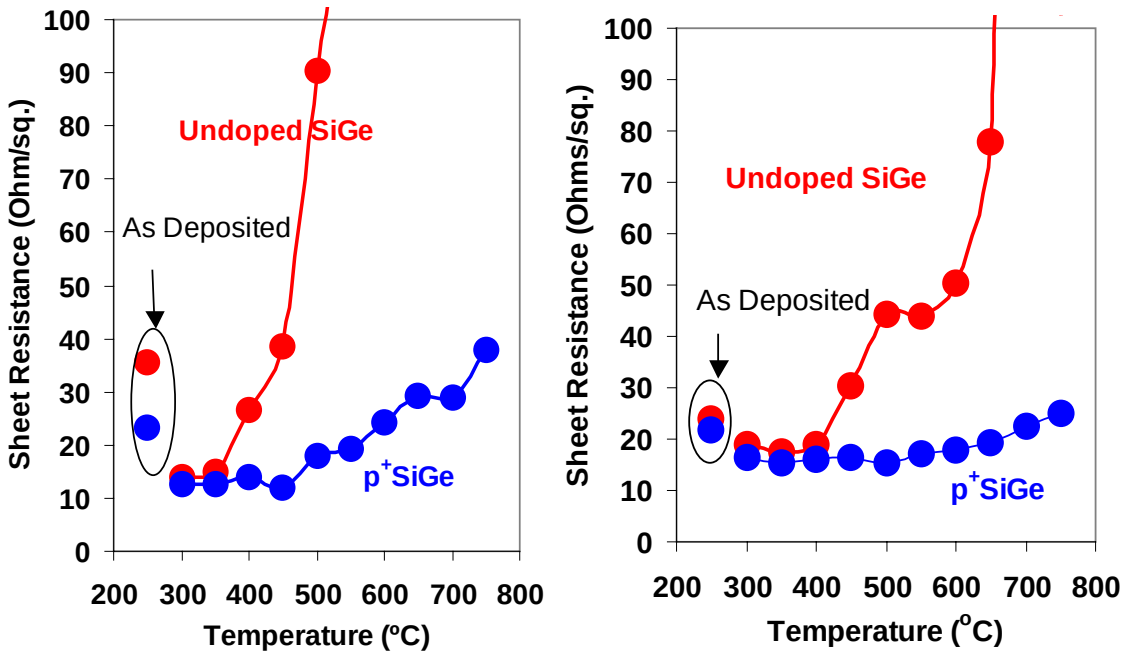

Figure I-13 Sheet resistance of Ni germanosilicide formed on undoped $Si_{1-x}Ge_x$ and boron doped $Si_{1-x}Ge_x$ with 10 nm Ni and a 1 nm Pt interlayer showing the thermal stability improvement.

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II. Sample Preparation

In this chapter, we present experimental conditions used in sample preparation. The deposition systems used to deposit $Si_{1-x}Ge_x$ and metal layers are also described.

II.1 UHV-RTCVD System

In this work, in-situ phosphorus doped Si and $Si_{1-x}Ge_x$ alloys were deposited in an Ultra-High Vacuum Rapid Thermal Chemical Vapor Deposition (UHV-RTCVD) reactor shown in Figure II-1. The system is capable of processing both 6" and 8" wafers. The system was designed and built at North Carolina State University. Construction of this system was accomplished by Dr. Nemanja Pesovic and Inkuk Kang, who were also graduate students in my research group. The system consists of three separate chambers: a load-lock (sample entry chamber), an intermediate chamber, and a main process chamber. The load lock is pumped by a dry molecular drag pump to a base pressure of 10^{-5} Torr. The intermediate chamber serves as a vacuum buffer between the sample entry and main process chambers and it is pumped by a cryopump to a base pressure of 10^{-9} Torr. Another cryopump maintains a base pressure of 10^{-9} Torr in the main chamber. During growth, a turbomolecular/molecular-drag combination pump is used to pump the process gasses. This pump is backed up by a dry mechanical pump. All pumps and gate valves on the system are oil-free to minimize the hydrocarbon contamination. The main

process chamber shown in Figure II-2 is a double walled (with oil circulation to heat the chamber if needed) stainless steel chamber with a quartz dome on top. Under the quartz dome, the seal consists of two O-rings with differential pumping. A small turbomolecular pump is used for this purpose and maintains a pressure of ~10^{-6} Torr between the O-rings. The wafer is heated through the quartz dome by tungsten-halogen lamps on top and around the dome. Two optical pyrometers (λ = 4.9 - 5.3 μm) focused at the edge and center of the wafer are used the measure the wafer temperature. The pyrometer focused at the wafer center is used in a closed-loop feedback control system. The wafer transfer mechanism is capable of loading four wafers into the intermediate chamber.

II.2 Surface Preparation Prior to $Si_{1-x}Ge_x$ Deposition

Wafers were cleaned *ex-situ* using a standard RCA clean with $SC_1(NH_4OH+H_2O_2+5H_2O)$ and $SC_2(HCl+H_2O_2+5H_2O)$. Immediately before loading into the system, the wafers were dipped in a 1 % HF solution for 30 seconds followed by a rinse in deionized water for 15 seconds. The purpose of the HF dip was to remove the protective oxide grown during the RCA clean. In addition, hydrogen passivates the dangling bonds and protects the surface against contamination.

After the HF dip, a wafer cassette containing four wafers is loaded into the load-lock. The procedure for transferring a wafer into the deposition chamber is as follows: Queue time before loading the wafer cassette into the vacuum chamber is about 10 – 15 min. After reaching a pressure of 10^{-5} Torr in the load-lock, the four-wafer cassette is

transferred into the intermediate chamber. After reaching 10^{-8} Torr in this chamber, one of the wafers from the cassette is transferred into the main chamber. The gate valve between the two chambers is closed and the main chamber is pumped to the base pressure by a dedicated UHV cryopump. Upon reaching the base pressure, the chamber is switched to the turbomolecular/molecular drag combination pump to pump the process gasses.

An *in-situ* vacuum bake was performed at 800°C for 10-15 seconds to remove any residual oxygen and carbon on the wafer surface. Previous studies in this laboratory by Mahesh Sanganeria and Muhsin Celik showed that annealing the wafer at 800ºC for 10 s in vacuum is sufficient to reduce the oxygen below the SIMS detection level and the carbon level below ~ 10^{18} cm^{-3} [1, 2]. Epitaxial growth is initiated by gas switching (i.e. by starting the gas flows while the wafer is at the process temperature) and terminated by temperature switching (i.e. by turning the lamps off while the process gases are still flowing). The gas flow into the chamber was terminated almost immediately after turning the heat lamps off. The cycle is illustrated in Figure II-3.

Precursors used in this work were 100% Si_2H_6, 10% GeH_4 mixed with H_2, 1% PH_3 mixed with H_2, and 100% H_2. Since the quartz bell jar is transparent to the infrared radiation, it remains relatively cold during the deposition process. However, long deposition periods can result in quartz heating, which can eventually result in deposition on the bell jar. Thus, the deposition times were limited to about 1 minute at 750ºC to avoid excessive heating of the bell jar.

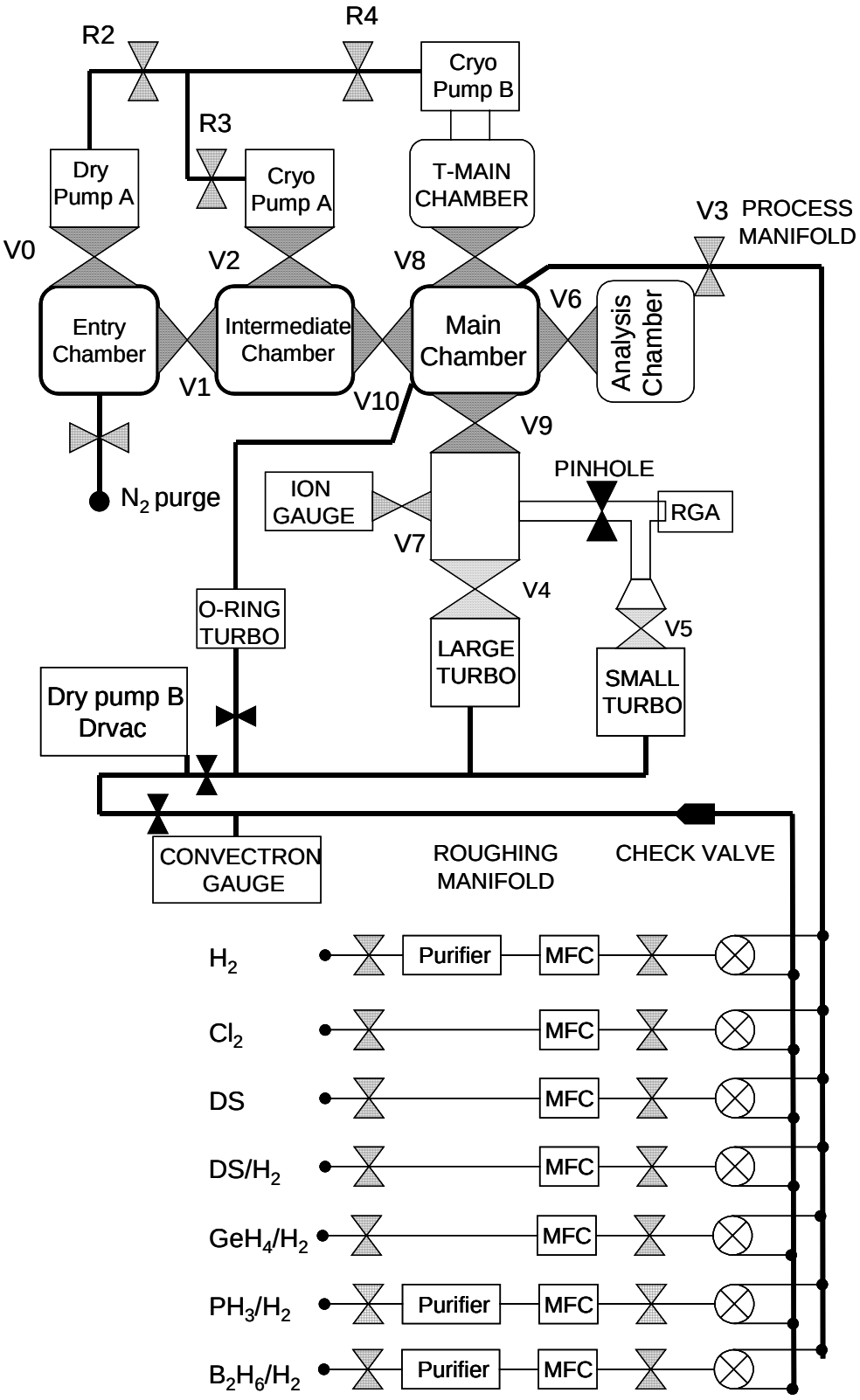

Figure II-1 Top view of the UHV-RTCVD System used in this work.

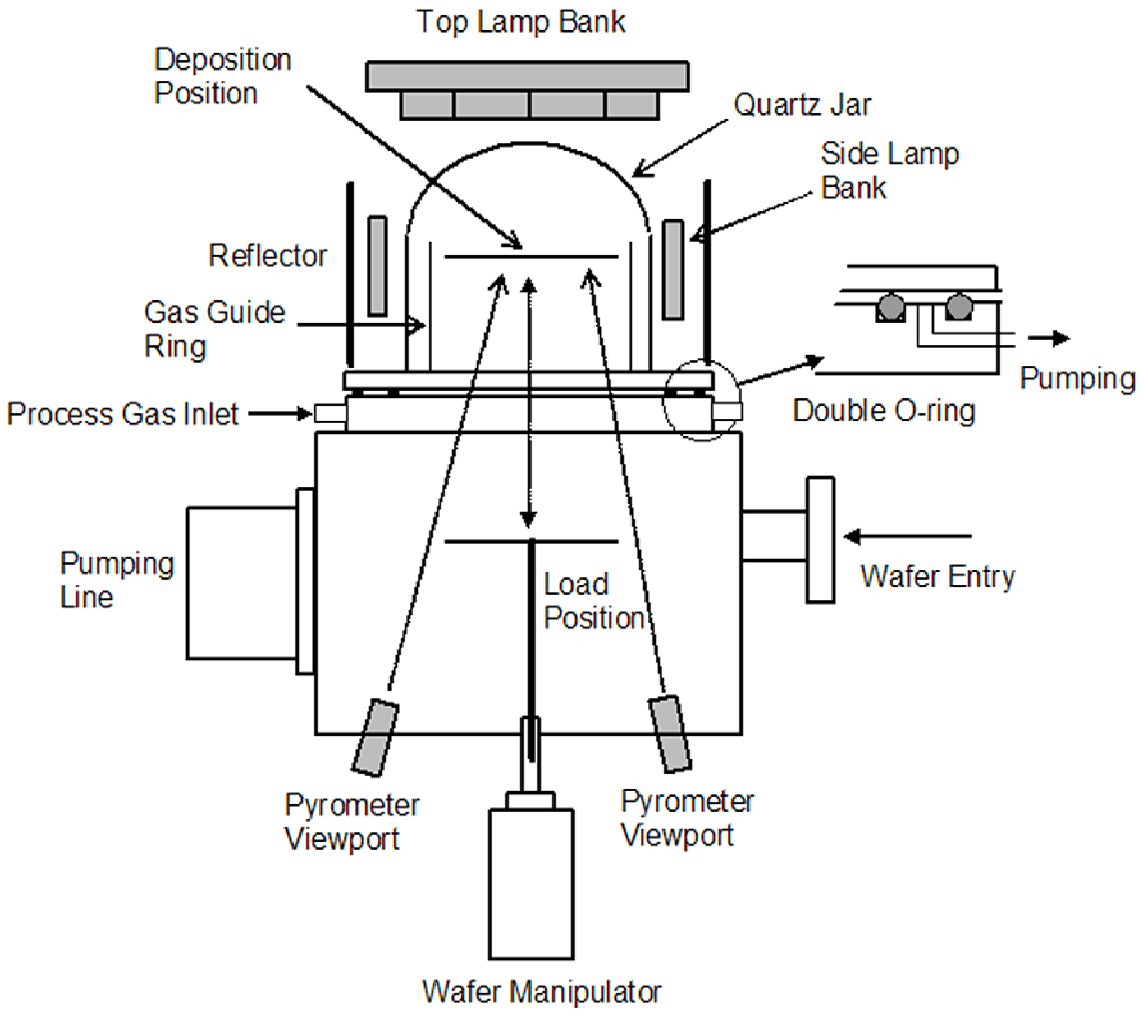

Figure II-2 Deposition Chamber of the UHV-RTCVD system consisting of a quartz dome with lamps on top of and around the dome.

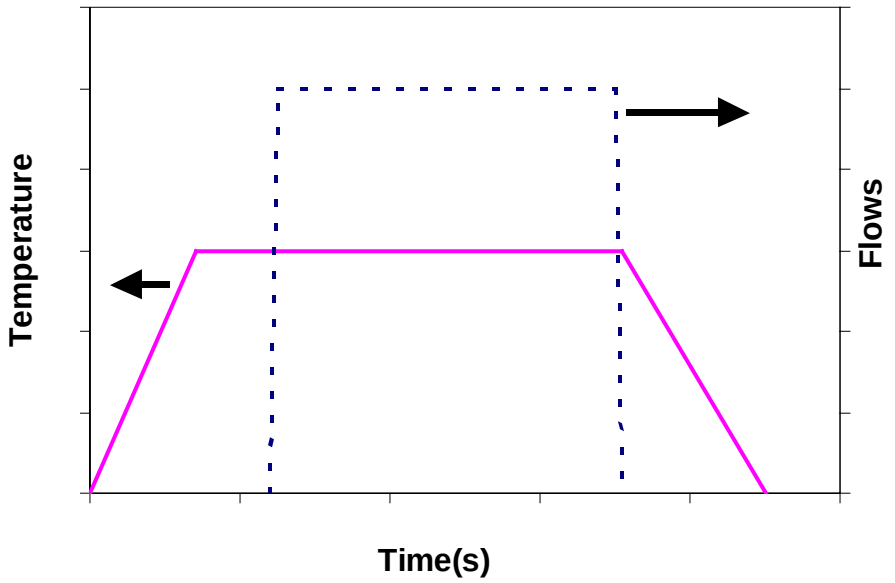

Figure II-3 Wafer temperature and gas flow versus processing time during a typical deposition cycle.

II.3 Phosphorus Doped $Si_{1-x}Ge_x$ Deposition

As shown in Chapter 1, the phosphorus and germanium concentrations can not be set independent of each other. To maximize the phosphorous incorporation, the films were deposited at 760ºC with a Ge percentage of ~20%. The standard gas flow rates used to deposit the layers are listed in Table II-1. The deposition pressure is ~ 132 mTorr.

Table II-1 Precursors and their flow rates used to deposit the $Si_{0.8}Ge_{0.2}$ layers.

Precursors	Si_2H_6	GeH_4	PH_3	H_2
Flow (sccm)	13.3	6.9	0.2	278

Shown in Figure II-4 is a typical XRD spectrum with a $Si_{1-x}Ge_x$ peak at the 2θ angle of 68.6º. The lattice constant of the $Si_{1-x}Ge_x$ can be calculated using the following equation:

$$d = \frac{\lambda}{2 \cdot \sin\theta}$$

where λ is the wavelength of the X-ray source and it is 0.15418nm. The Ge percentage can be obtained using the following expression,

$$Ge\% = \frac{d_{SiGe} - d_{Si}}{d_{Ge} - d_{Si}}$$

where d_{SiGe} and d_{Si} are the lattice constants of Ge and Si respectively. The Ge percentage of the film shown in Figure II-4 is ~ 20.6%. The measurement assumes that the SiGe is fully relaxed.

The surface morphology of a phosphorous doped $Si_{1-x}Ge_x$ layer selectively deposited in a window defined in SiO_2 is shown in Figure II-5. The surface roughness of the film is about 4 Å. The film is selectively deposited with a few nuclei on the oxide. A facet can be observed at the $Si_{1-x}Ge_x$/oxide interface.

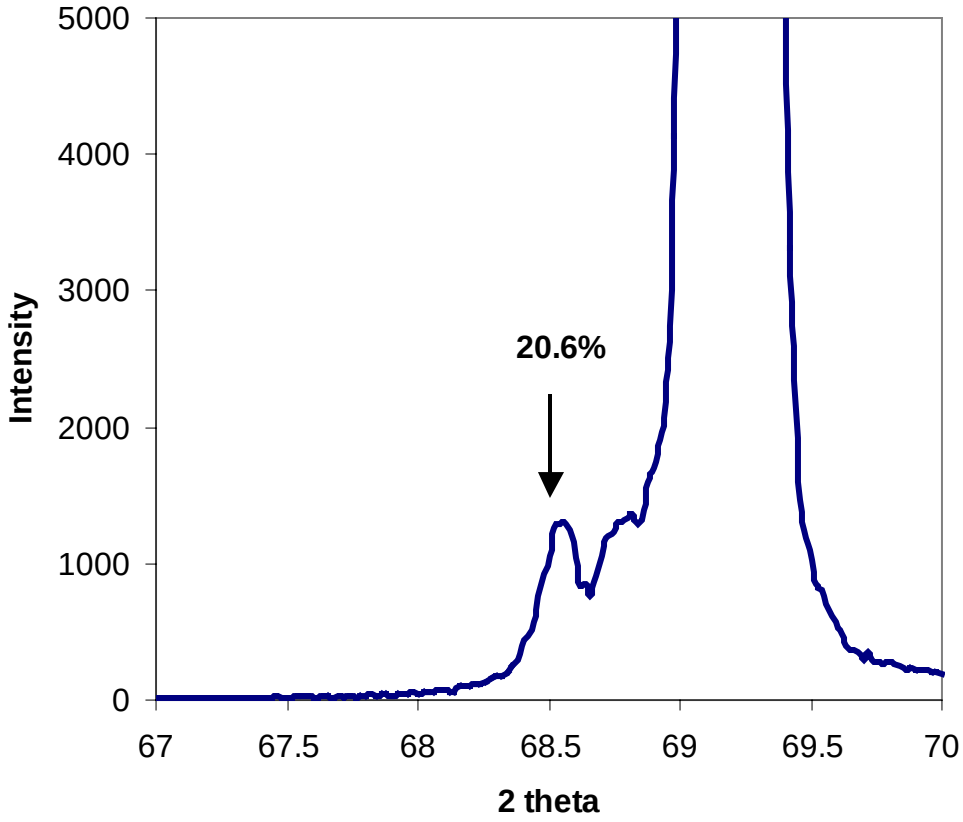

Figure II-4 X-Ray diffraction spectrum of a typical N^+ $Si_{1-x}Ge_x$ film used in this study. The $Si_{1-x}Ge_x$ peak locates at 2θ angle of 68.58 degree, which corresponds to ~20.6% Ge concentration.

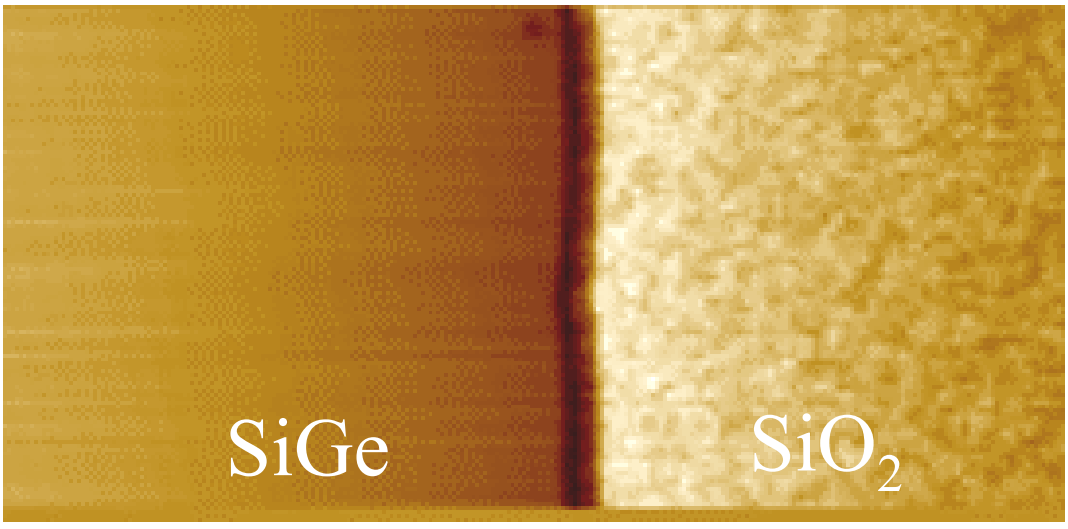

Figure II-5 AFM image of selective N^+ $Si_{1-x}Ge_x$ deposited on Si wafer with SiO_2 pattern.

II.4 UHV Sputter Deposition System

Ni and Pt depositions were carried out in a UHV sputtering system designed and constructed in this laboratory. The system can process both 6 and 8" wafers. The top view of the system is shown in Figure II-6. As shown, the system consists of two stainless-steel chambers, a load lock and a deposition chamber. The tool is equipped with 3 sputtering guns made by AJA international Inc. A diagram of the sputtering gun is shown in Figure II-7.

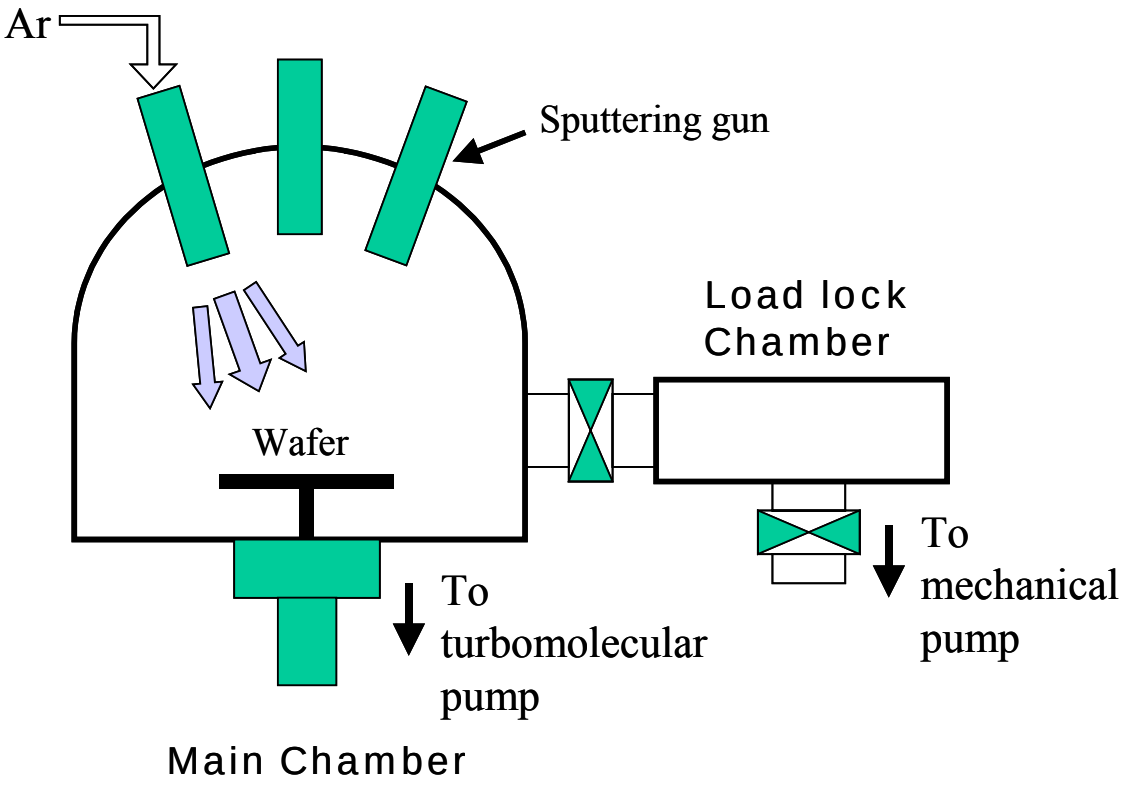

Figure II-6 A cross sectional view of the UHV sputtering system.

After loading a single wafer, the load lock is pumped until a base pressure of ~ $1x10^{-6}$ Torr is reached. The wafer is then transferred into the deposition chamber and placed on a rotating sample holder. The chamber is pumped until a base pressure of 10^{-8} Torr is reached for sputtering. During processing, the Ar pressure was set at 5.5 mTorr. The RF power used for sputtering ranged from 30 to 100 Watts depending on the material deposited and the desired deposition rate. The sputtering rate of Ni, Pt and Zr with 100 Watts' power is shown in Table II-2.

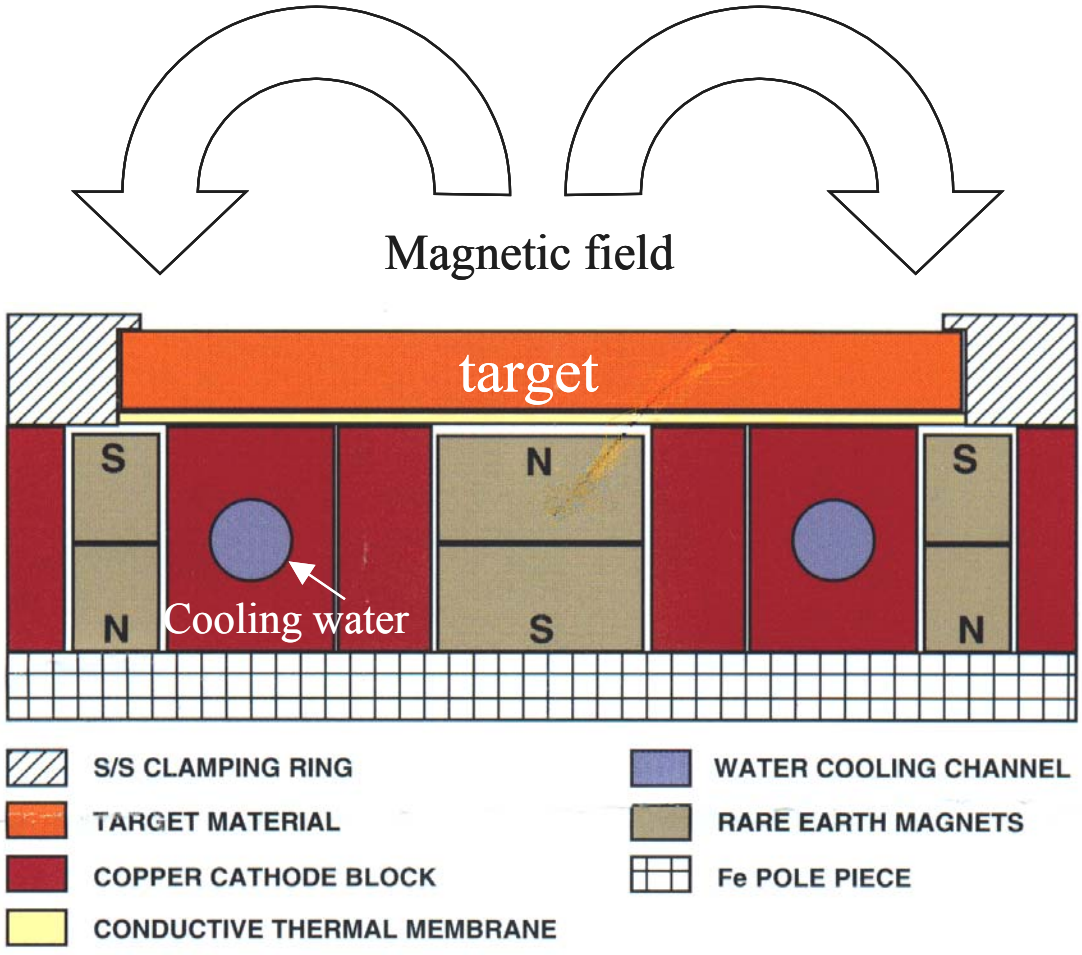

Figure II-7 Cross sectional view of the sputtering gun.

Table II-2 Sputtering rates at 100 Watts in the UHV sputtering system

	Pt	Ni	Zr
Sputtering Rate (Å/min.)	55	24	24

II.5 References

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III. Ni, Pt and Zr Germanosilicide Formation on Phosphorus Doped $Si_{1-x}Ge_x$ Alloys

III.1 Introduction

Previous work by Jing Liu in this laboratory showed that both Ni and Pt could be used to form low-resistivity germanosilicides on boron doped $Si_{1-x}Ge_x$ alloys [1]. Jing Liu showed that both germanosilicides formed on boron doped $Si_{1-x}Ge_x$ alloys could meet the contact resistivity requirements of future MOSFETs. It was also shown that the thermal stability of $NiSi_{1-x}Ge_x$ was limited to temperatures below 450ºC for a Ge concentration of ~ 50 % in the alloy. $PtSi_{1-x}Ge_x$ was found to be stable up to ~ 800ºC. The material with the best thermal stability was found to be $Zr(Si_{1-x}Ge_x)_2$, however, the contact resistivity with this material was demonstrated to be an order of magnitude higher than the best values for Ni and Pt germanosilicide. In this chapter, we present experimental results on germanosilicide formation with these Ni, Pt and Zr on phosphorus doped $Si_{1-x}Ge_x$ alloys.

III.2 Nickel Germanosilicide

Figure III-1 shows the sheet resistance of $NiSi_{1-x}Ge_x$ formed on phosphorus doped $Si_{1-x}Ge_x$ as a function of the annealing temperature. The sheet resistance values obtained on Si and undoped $Si_{1-x}Ge_x$ are also shown for comparison. The Ge concentrations are 20% for the $Si_{1-x}Ge_x$ films. The starting Ni and $Si_{1-x}Ge_x$ layers were 30 nm and 100 nm respectively. Annealing was performed in N_2 ambient for 30 seconds.

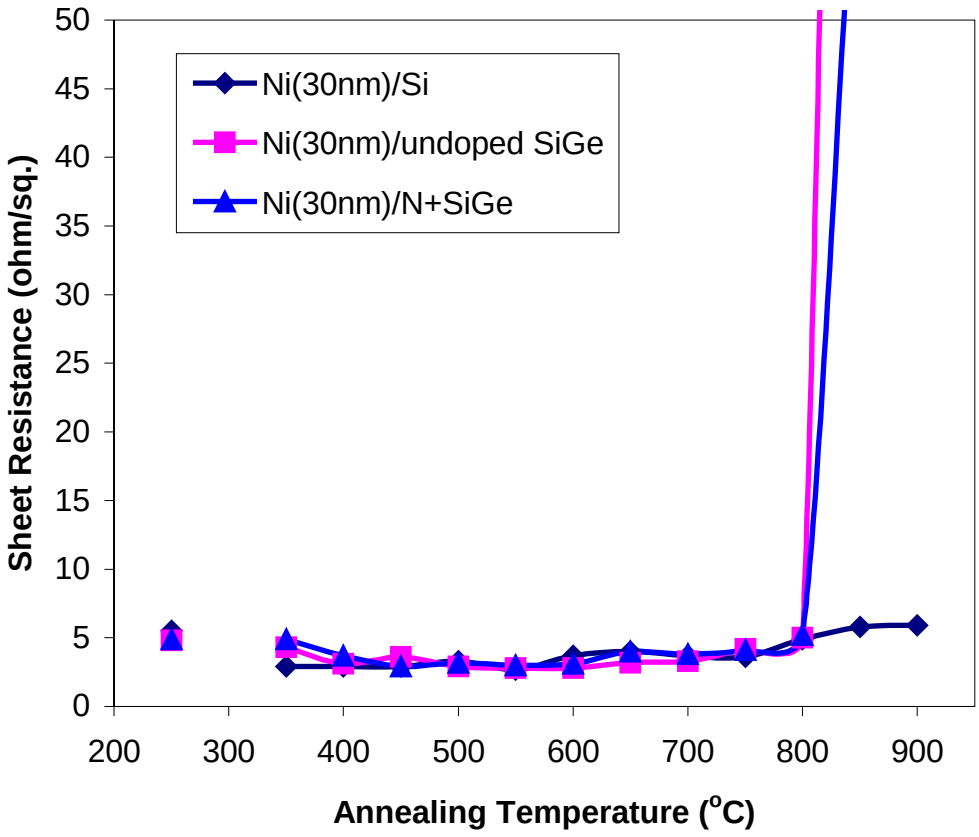

Figure III-1 Sheet resistance of $NiSi_{1-x}Ge_x$ plotted as a function of the germanosilicide formation temperature. The starting Ni thickness is 30 nm.

All three curves look very similar. The germanosilicide reaches the low resistivity phase below 400°C, which appears to be stable until 800°C, where the sheet resistance jumps to ~ 68ohm/square abruptly. On Si, this abrupt shift in sheet resistance is not observed indicative of a better thermal stability. We note that both doped and undoped $Si_{1-x}Ge_x$ layers exhibit a similar behavior. This contrasts the results obtained by Jing Liu in our laboratory on boron doped $Si_{1-x}Ge_x$. In his work, Jing Liu showed that boron improved the thermal stability of the germanosilicide possibly due to the strain compensation effect of small boron atoms. It is important to note however that as a much

larger atom, phosphorus provides little strain compensation. Furthermore, the phosphorus concentrations used in this work is far less than the boron levels used in Jing Liu's work.

It should also be noted that $NiSi_{1-x}Ge_x$ layers of Jing Liu formed on undoped $Si_{1-x}Ge_x$ was stable only up to ~ 450ºC whereas the sheet resistance of the $NiSi_{1-x}Ge_x$ shown in Figure III-1 is stable at least up to 800ºC. The main difference between the two experimental studies is that the $Si_{1-x}Ge_x$ layers used in Jing Liu's work was ~ 50% as opposed to 20-30% used in this study due to reasons discussed in the previous chapter. The impact of Ge concentration on $NiSi_{1-x}Ge_x$ thermal stability is demonstrated in Figure III-2. As shown, with 20% Ge, the sheet resistance is stable up to ~ 800°C. On the other hand, the sheet resistance begins to raise at a much lower temperature when the Ge content is raised to 50%. As discussed in the previous chapter, at temperatures above 450°C, the Ge atoms begin to leave the germanosilicide layer and accumulate at the grain boundaries[2].

XRD was used to identify the different germanosilicide phases forming at different temperatures and to study Ge out-diffusion. Figure III-3 shows the results of the XRD analysis on phosphorous doped samples for temperatures ranging from 350 to 700°C. After annealing at 350°C, Ni rich Ni_2Si silicide phase and $Ni(Si_{1-x}Ge_x)$ (020) and (211) phases co-exist in the material. At higher temperatures, we can observe the gradual shift of the (020) peak toward the higher 2θ values indicative of Ge loss from the germanosilicide. This shift was also observed for boron doped $Si_{1-x}Ge_x$ by J. Liu et al [3]. Interestingly, the sheet resistance of the germanosilicide layer formed on phosphorus dopes $Si_{1-x}Ge_x$ appears to be stable at least up to 800ºC. However, this may not necessarily provide a complete picture since the sheet resistance is expected to go up only

if the electric current flowing through the germanosilicide grains is obstructed. Therefore, it is possible that the sheet resistance of the layer may not be as sensitive to the subtle changes occurring in the film composition or the structure.

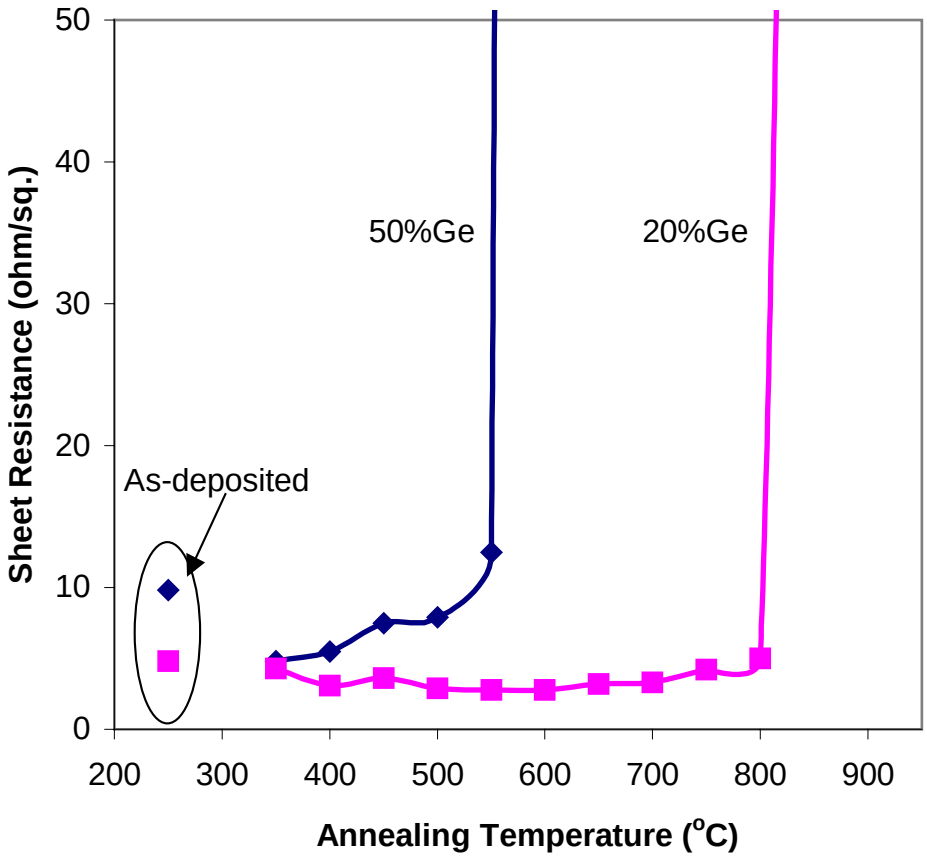

Figure III-2 Sheet resistance of $NiSi_{1-x}Ge_x$ formed on undoped $Si_{0.8}Ge_{0.2}$ and $Si_{0.5}Ge_{0.5}$. The starting metal thickness is 30 nm.

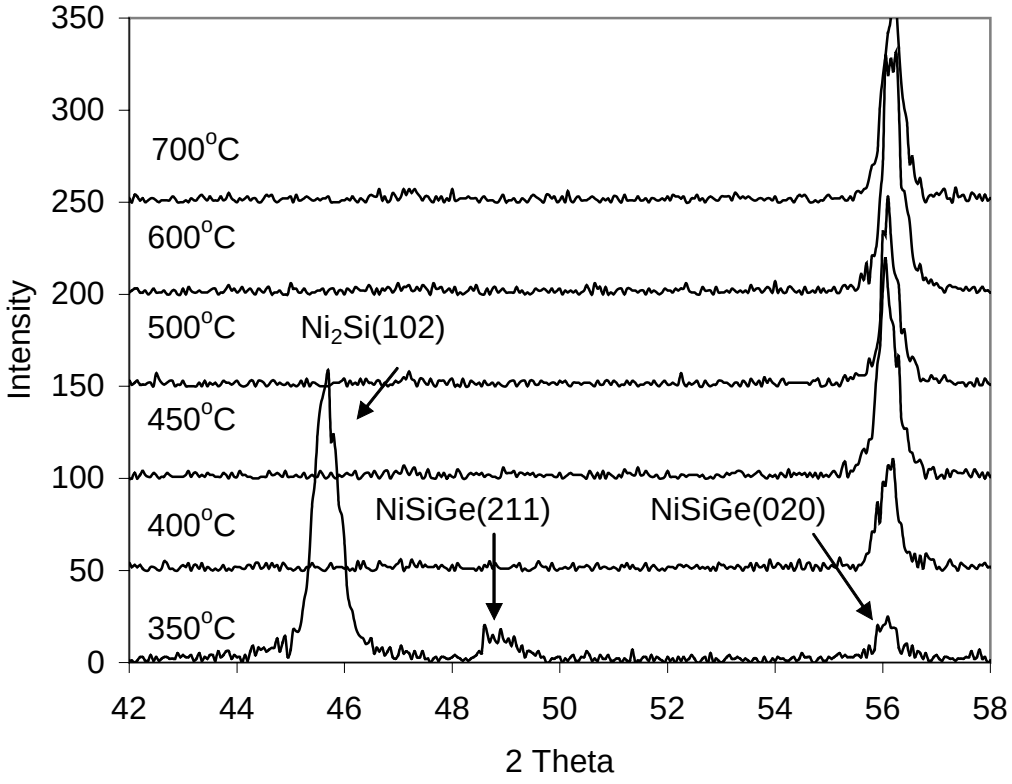

Figure III-3 XRD profiles of $NiSi_{1-x}Ge_x$ formed at different temperatures.

Figure III-1 shows that the NiSi sheet resistance increases from ~ 3Ω/sq to ~ 5Ω/sq at ~ 750°C, which is most likely due to formation of the $NiSi_2$ phase [4]. The formation of $NiSi_2$ is controlled by nucleation of $NiSi_2$, which starts at the NiSi/Si interface [5]. In Figure III-4, XRD shows $NiSi_2$ is formed at annealing temperature of 800°C on N^+ $Si_{1-x}Ge_x$ layer. When Ge atoms begin to accumulate at the grain boundaries, the $NiSi_{1-x}Ge_x$ layer slowly transforms into NiSi, which then converts to $NiSi_2$ around 800°C. This change may not only enhance phase separation but it may also promote agglomeration since $NiSi_2$ has a cubic structure while both NiSi and NiGe have the orthorhombic structure.

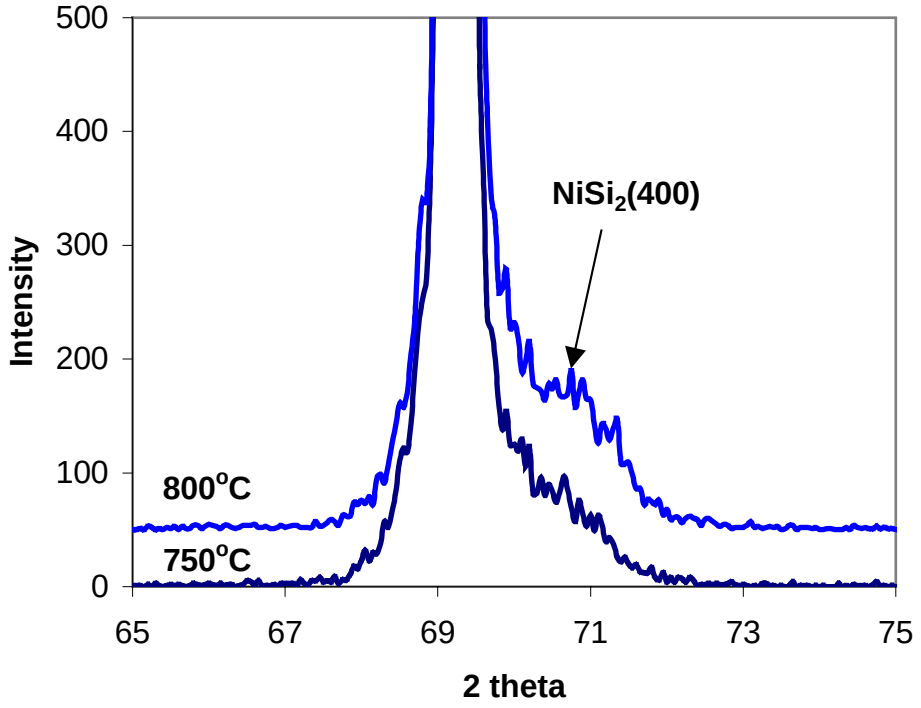

Figure III-4 XRD profiles of $NiSi_{1-x}Ge_x$ formed at 750 and 800°C.

It is well established that the film thickness may have a strong impact on the thermal stability of a silicide layer. Lavoie et. al. from IBM showed that thin NiSi layers can agglomerate before they convert into $NiSi_2$ [6]. They attributed this behavior to the different surface energies for the NiSi films. We observe a similar behavior in Figure III-5, which shows the sheet resistance of $NiSi_{1-x}Ge_x$ layers formed using 10, 15, 20 and 30 nm thick Ni layers. The data shows that the maximum allowable temperature decreases as the Ni layer gets thinner. With a Ni layer of 10 nm, the maximum temperature is close to 600°C, which is ~ 150°C higher than the 50% Ge case.

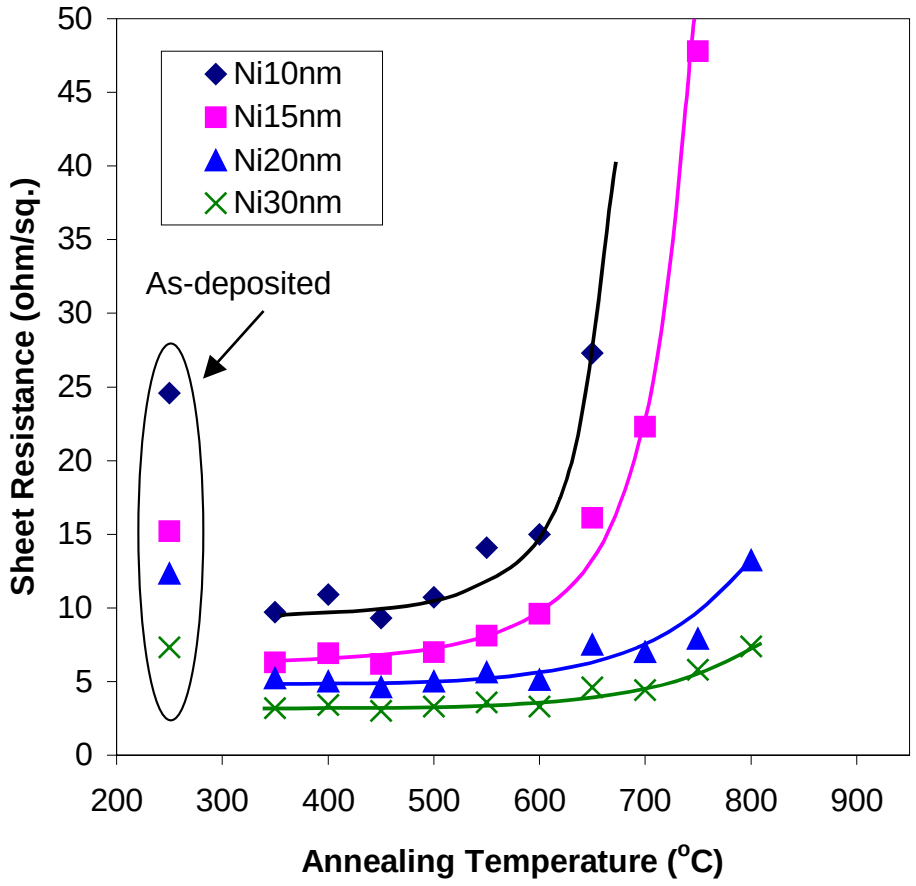

Figure III-5 Sheet resistance of $NiSi_{1-x}Ge_x$ formed using different starting Ni thicknesses plotted as a function of the formation temperature.

Secondary ion mass spectrometry (SIMS) was used to analyze the distribution of elements during $NiSi_{1-x}Ge_x$ formation. The depth profiles of Ni, P Si obtained from a germanosilicide layer formed at 500ºC on a $Si_{1-x}Ge_x$ with a Ge concentration of 20% are shown in Figure III-6. The analysis was performed using O_2 at an incident energy of 0.625 KeV. From the profiles, we can conclude that the thickness of the $NiSi_{1-x}Ge_x$ layer is about 60 nm. We note that the phosphorus concentration in the germanosilicide is lower, which may be due to a lower ion yield in the material. However, the phosphorus profile is also suggestive of phosphorus accumulation at the $NiSi_{1-x}Ge_x/Si_{1-x}Ge_x$ interface

and at the surface of the sample. The surface peak may well be coming from the original $Si_{1-x}Ge_x$ layer since phosphorus segregates at the surface during growth [7]. It is also true that SIMS is not yet capable of providing an accurate analysis of the sample surface. If there is indeed phosphorus pile-up at the interface, we expect the contact resistance of $NiSi_{1-x}Ge_x$ to decrease. Considering the distribution of phosphorus in $Si_{1-x}Ge_x$ without the germanosilicide in Figure II-8, we note that the phosphorous distribution is not uniform and it increases toward the surface. Therefore, the fact that we have an almost uniform P distribution in Figure III-6 hints that phosphorus atoms may have been pushed out of the germanosilicide increasing the phosphorus concentration in the underlying $Si_{1-x}Ge_x$ layer. Another interesting observation we can make from Figure III-1 is that the Ni profile has a tail extending into the Si substrate, which cannot be disregarded as a measurement error. We note that both Ge and P profiles are quite abrupt relative to the Ni profile, which is suggestive of Ni diffusion into the underlying semiconductor layers or a rough interface.

As shown in Figure III-1, the lowest sheet resistance obtained for $NiSi_{1-x}Ge_x$ is about 3.0 Ω/sq. For 30nm Ni, the NiSi thickness is expected to be around 60 nm [8], which yields a resistivity of 18 μΩ-cm. Figure III-6 suggests roughly the same thickness for $NiSi_{1-x}Ge_x$. In his work on boron doped $Si_{1-x}Ge_x$, J. Liu claimed that 2.1nm $NiSi_{1-x}Ge_x$ could be formed with 1 nm of Ni [1]. In his case, the Ge content of the $Si_{1-x}Ge_x$ layer was about 50%. Therefore, if the thicknesses of the $NiSi1_{-x}Ge_x$ and NiSi layers in Figure III-1 are indeed the same, we can conclude that $NiSi_{1-x}Ge_x$ should also have a resistivity of about 18 μΩ-cm, which is lower than the 25 μΩ-cm reported in Jing Liu's thesis.

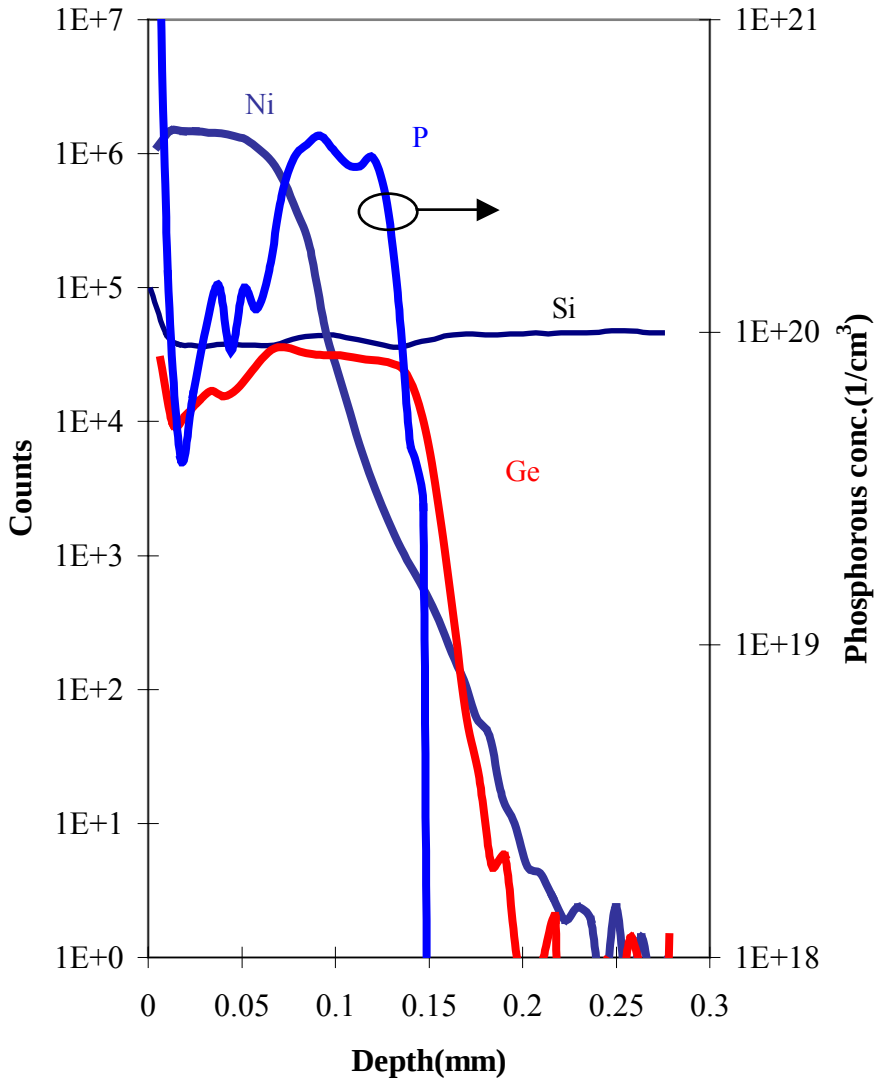

Figure III-6 Distribution of Ni, Si, Ge and P after RTA at 500°C for 30s in N_2.

Atomic force microscopy (AFM) was used to study the surface morphology of $NiSi_{1-x}Ge_x$ layers formed at different temperatures. Figure III-7 shows AFM surface micrographs of the $NiSi_{1-x}Ge_x$ layers formed at different temperatures. It can be seen that the surface roughness gradually increases with temperature from 400°C to 800°C suggestive of agglomeration.

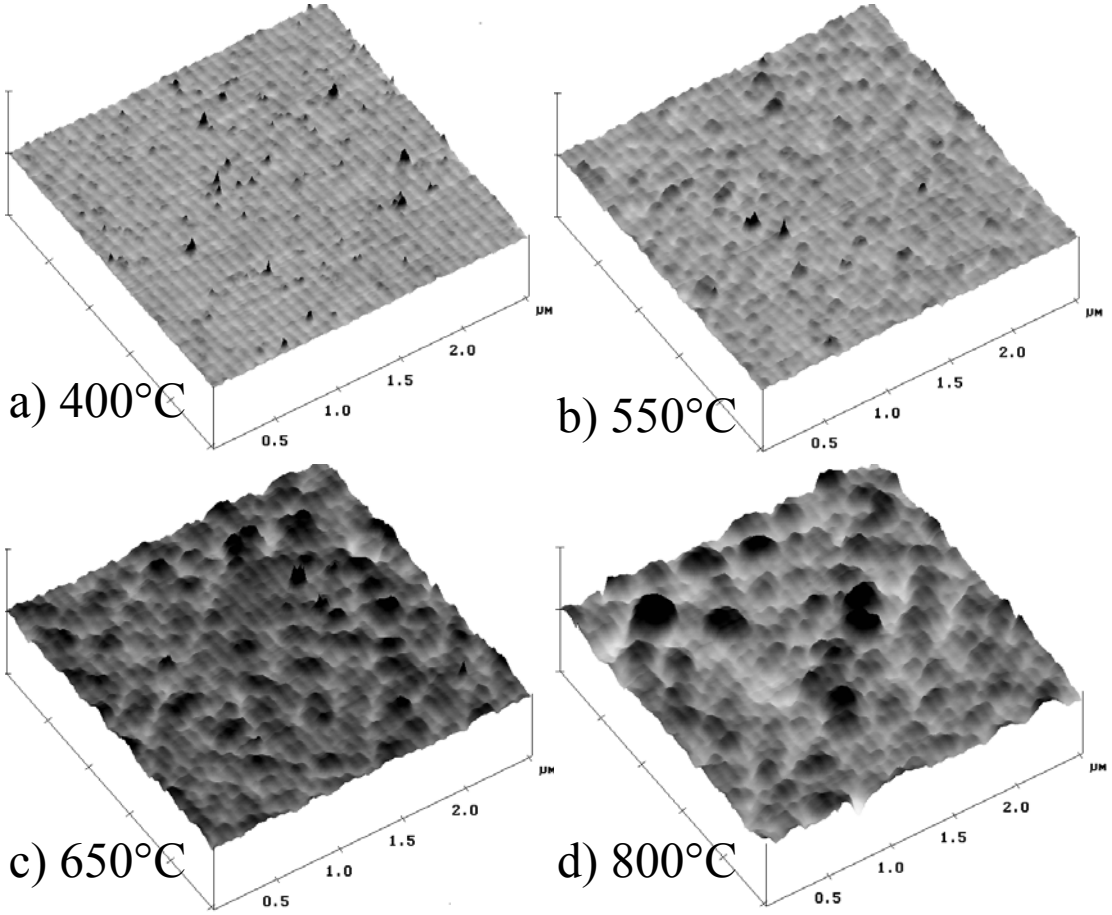

Figure III-7 AFM micrographs of germanosilicide surfaces obtained at 400, 550, 650, and 800°C. The starting Ni thickness is 10 nm.

There are three potential phenomena that can account for the agglomeration of a germanosilicide film:

1) Discontinuities in ultra-thin layers

2) Ge segregation

3) $NiSi_2$ formation

and they are illustrated in Figure III-8. We note that two or more of these effects may co-exist in a layer.

Discontinuities occur on thinner films and can be eliminated by emphasizing a clean surface and uniform Ni deposition. The $Ni(Si_{1-x}Ge_x)_2$ phase has never been observed for $Ni/Si_{1-x}Ge_x$ solid phase reactions. However, since Ge out-diffusion leads to NiSi grains surrounded by Ge rich $Si_{1-x}Ge_x$ regions, conversion from NiSi to $NiSi_2$ may occur.

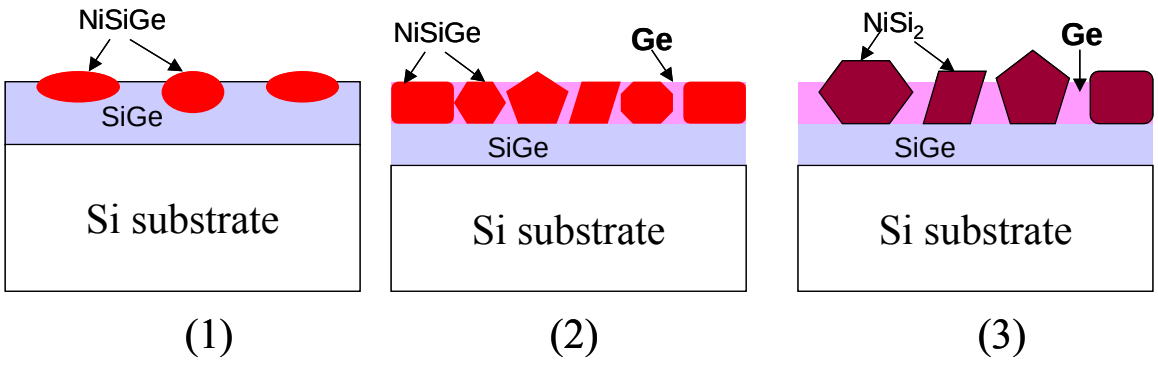

Figure III-8 3 potential causes of agglomeration: 1) discontinuous film, 2) Ge segregation from $NiSi_{1-x}Ge_x$ formation, and 3) $NiSi_2$ formation.

Figure III-9 shows the sheet resistance and surface roughness of $NiSi_{1-x}Ge_x$ layers formed using 10 and 30 nm thick Ni layers. When the Ni thickness is 10nm, the surface roughness gradually increases with the annealing temperature with a small step that appears to exist at ~ 400°C. At ~ 650°C, an abrupt increase is observed accompanied by an increase in the sheet resistance, which is suggestive of agglomeration or severe Ge accumulation at the grain boundaries. After this abrupt increase, the surface roughness reaches a plateau until 800°C, where the surface roughness exhibits a second sharp increase, which may be attributed to $NiSi_2$ formation. This may further promote Ge out-diffusion and segregation at the grain boundaries.

With a Ni thickness of 30 nm, a similar behavior is observed. The roughness begins to increase sharply at ~ 450°C and a plateau is reached at ~ 575°C. The sheet resistance begins to increase again starting at ~ 675°C. The fact that this final increase in roughness accompanied by an increase in sheet resistance occur at a lower temperature with 30 nm Ni suggests that $NiSi_2$ formation may be responsible for the observed changes. Lavoie et. al. showed that for thin Ni layers disilicide formation temperature is higher [6]. They proposed that thinner NiSi layers provide fewer nucleation sites for $NiSi_2$ formation and require higher temperatures to increase the likelihood of $NiSi_2$ formation. An argument that can be raised against the above hypothesis is that the sheet resistance of $NiSi_2$ is about four times the sheet resistance of NiSi. As shown in Figure III-9, with 30 nm Ni, the sheet resistance increases only slightly.

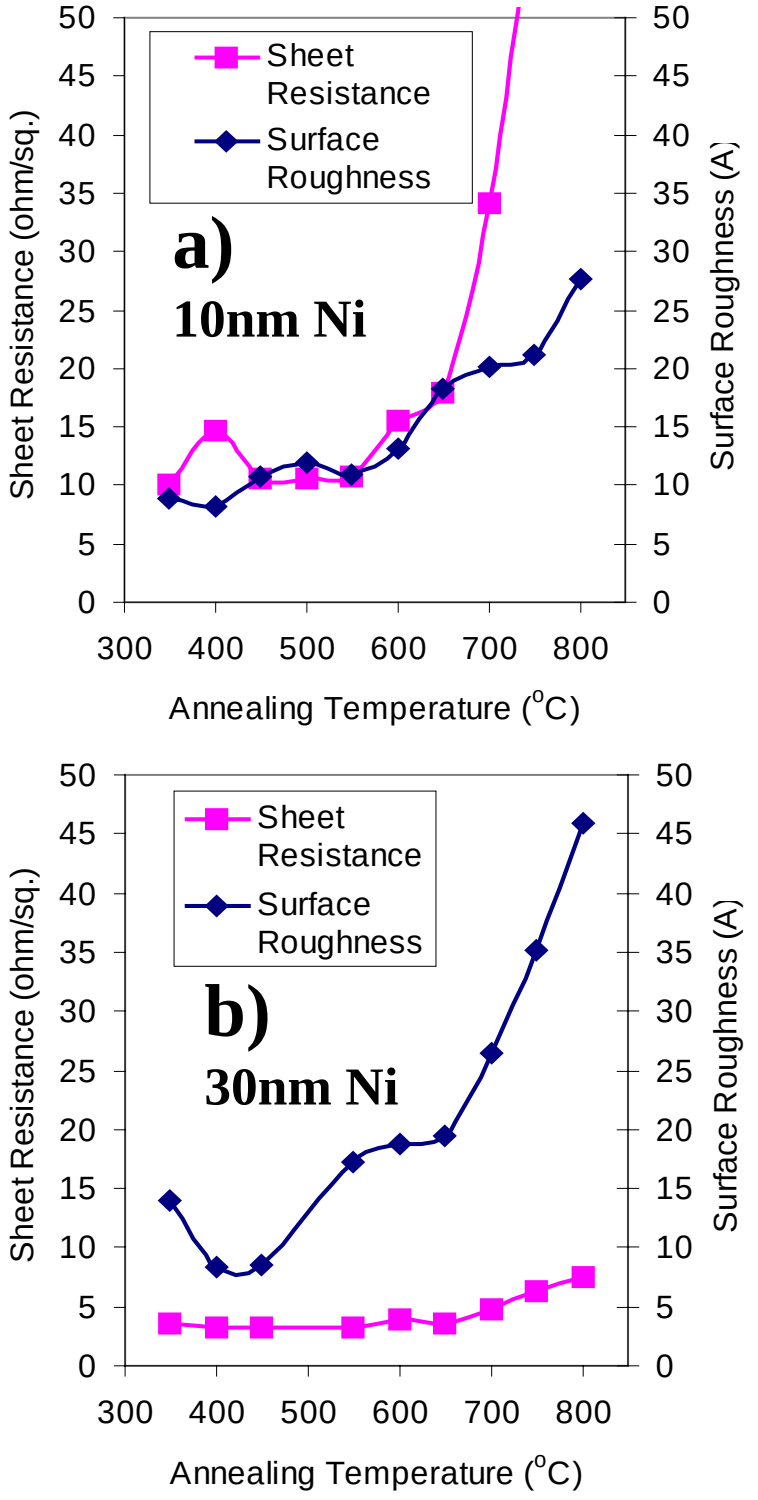

Figure III-9 Sheet resistance and surface roughness as a function of annealing temperature. a) 10nm Ni and b) 30nm Ni on N^+ $Si_{0.8}Ge_{0.2}$.

In summary, our results indicate that $NiSi_{1-x}Ge_x$ is a promising contact candidate for $Si_{1-x}Ge_x$. $NiSi_{1-x}Ge_x$ can form at annealing temperatures as low as 350°C. The thermal stability and sheet resistance of $NiSi_{1-x}Ge_x$ are not affected by phosphorous doping. The resistivity of $NiSi_{1-x}Ge_x$ is about 18 μΩ-cm, which is close to that of NiSi. This value is close to 16.7 μΩ-cm reported for $Si_{0.6}Ge_{0.4}$ M. Qing et al [9], but lower than values reported for $Si_{0.5}Ge_{0.5}$ by M. Qing and J. Liu [1, 9]. This suggests that Ge content can affect the resistivity of $NiSi_{1-x}Ge_x$. The thermal stability of $NiSi_{1-x}Ge_x$ is found to depend on the film thickness and the Ge content. Either reducing Ni thickness or increasing the Ge content can degrade the $NiSi_{1-x}Ge_x$ stability. This is consistent with results obtained by J. Liu for boron doped $Si_{1-x}Ge_x$ [1].

III.3 Platinum Germanosilicide

Pt is another promising germanosilicide candidate because it is known to form a monosilicide with very little consumption of the substrate. The variation of sheet resistance as a function of the formation temperature for both PtSi and $PtSi_{1-x}Ge_x$ is shown in Figure III-10. We note for both cases that the sheet resistance is independent of the formation temperature within 500 - 800°C. At 800ºC, the sheet resistance begins to increase abruptly indicative of a key change in the microstructure. The sheet resistance of the germanosilicide formed on undoped $Si_{1-x}Ge_x$ is higher than that of the germanosilicide formed on phosphorus-doped $Si_{1-x}Ge_x$ when the annealing temperature is lower than 700°C. This is due to the fact that the lower sheet resistance of the doped $Si_{1-x}Ge_x$ layer is in parallel with the germanosilicide sheet resistance.

The sheet resistance of $PtSi_{1-x}Ge_x$ is shown in Figure III-10 as a function of the formation temperature. The samples were prepared using 20nm Pt layers sputtered onto undoped and heavily phosphorous-doped $Si_{0.8}Ge_{0.2}$ layers. We note that the sheet resistance of both Pt/Si and Pt/N^+ SiGe is similar and roughly independent of temperature between 500-800°C.

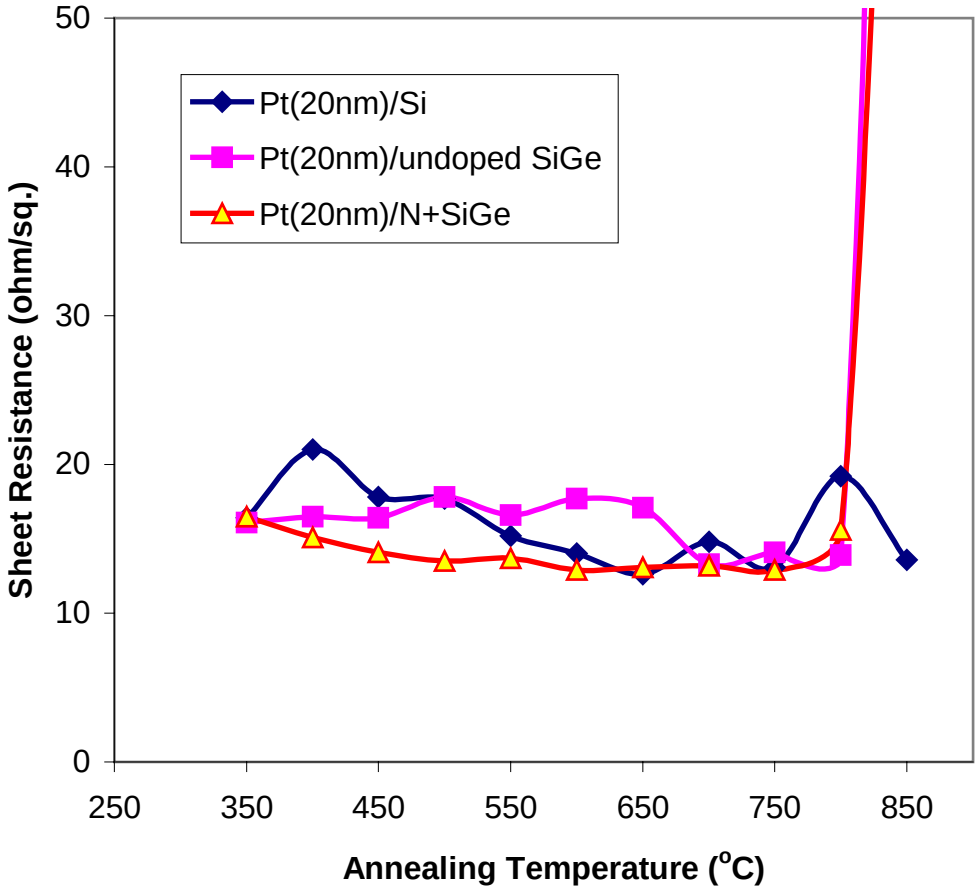

Figure III-10 Sheet resistance of PtSi and $PtSi_{1-x}Ge_x$ formed on both doped and undoped $Si_{1-x}Ge_x$ alloys.

The XRD spectra of $PtSi_{1-x}Ge_x$ samples formed on phosphorus-doped $Si_{0.8}Ge_{0.2}$ layers are shown in Figure III-11. The samples were annealed at temperatures ranging from 350 to 750°C. The 2θ angle of the $Pt(Si_{1-x}Ge_x)$ <121> peak stays at 43.85 degree for different temperatures ranging from 350 to 750°C, which indicates that the lattice constant remains the same. This also suggests that significant Ge out-diffusion does not occur in this temperature range. The XRD spectrum of PtSi is also shown in Figure III-11. The PtSi<121> peak is located at 44.05°, which indicates a smaller lattice constant than that of Pt(SiGe). On the other hand, when the Ge concentration is raised to 50%, the shift in the location of the <220> peak can be observed although it is more pronounced for $NiSi_{1-x}Ge_x$ [3]. The shifting occurs because with Ge out-diffusion at high temperatures the films gradually convert to PtSi.

Even though the XRD spectra show $Pt(Si_{1-x}Ge_x)$ peaks at temperatures as low as 350°C, the sheet resistance of the films in Figure III-10 shows that the lowest sheet resistance is reached at ~ 600°C. If the germanosilicide formation rate is limited by the diffusion of species, the reactions may require more than 30 s to complete at lower temperatures.

Figure III-12 shows Pt germanosilicide formation on $Si_{1-x}Ge_x$ films with Ge concentrations of 50% and 20%. The sheet resistances of both layers begin to increase abruptly at about 800°C. If the resulting Pt germanosilicide thickness per nanometer of Pt is the same as PtSi, i.e. ~2.0, both samples shown in Figure III-12 have the same resistivity of about 52 ohm-cm.

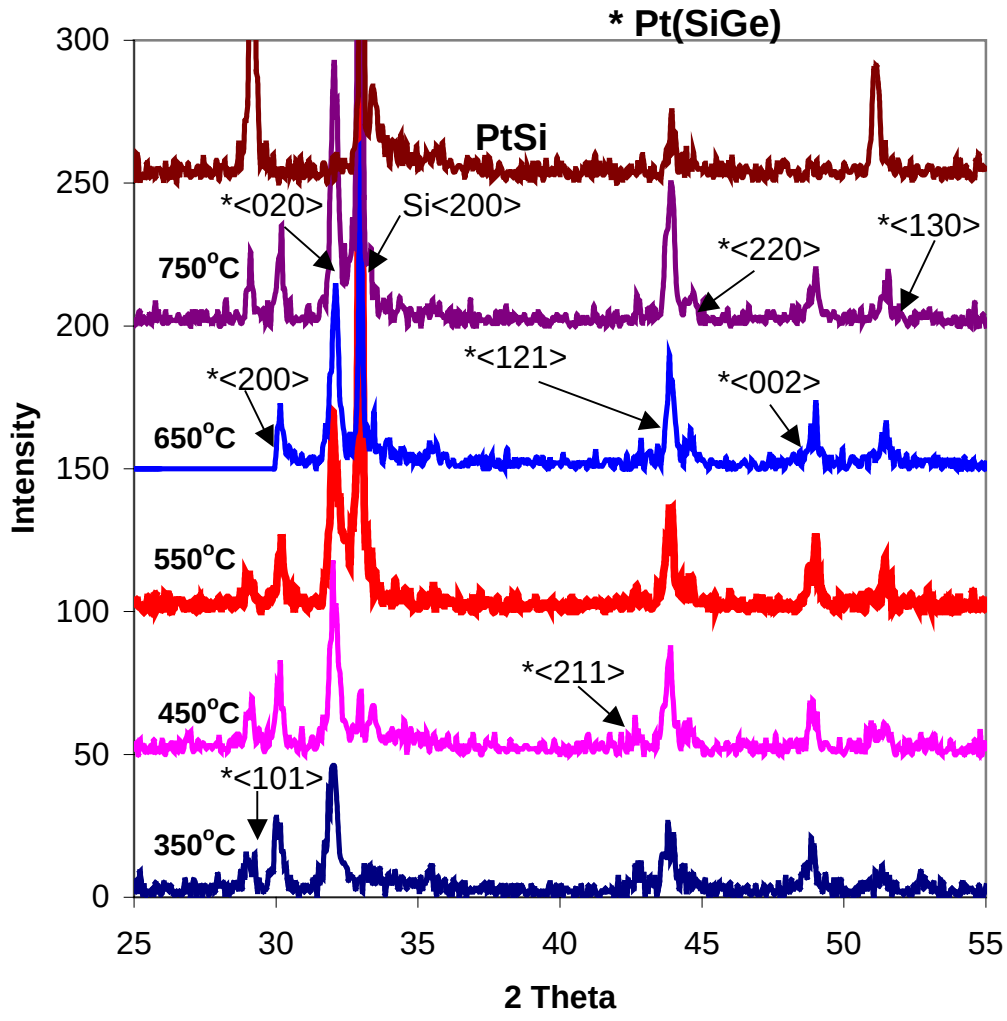

Figure III-11 XRD profiles of $PtSi_{1-x}Ge_x$ formed at different temperatures. The original Pt thickness is ~ 20nm.

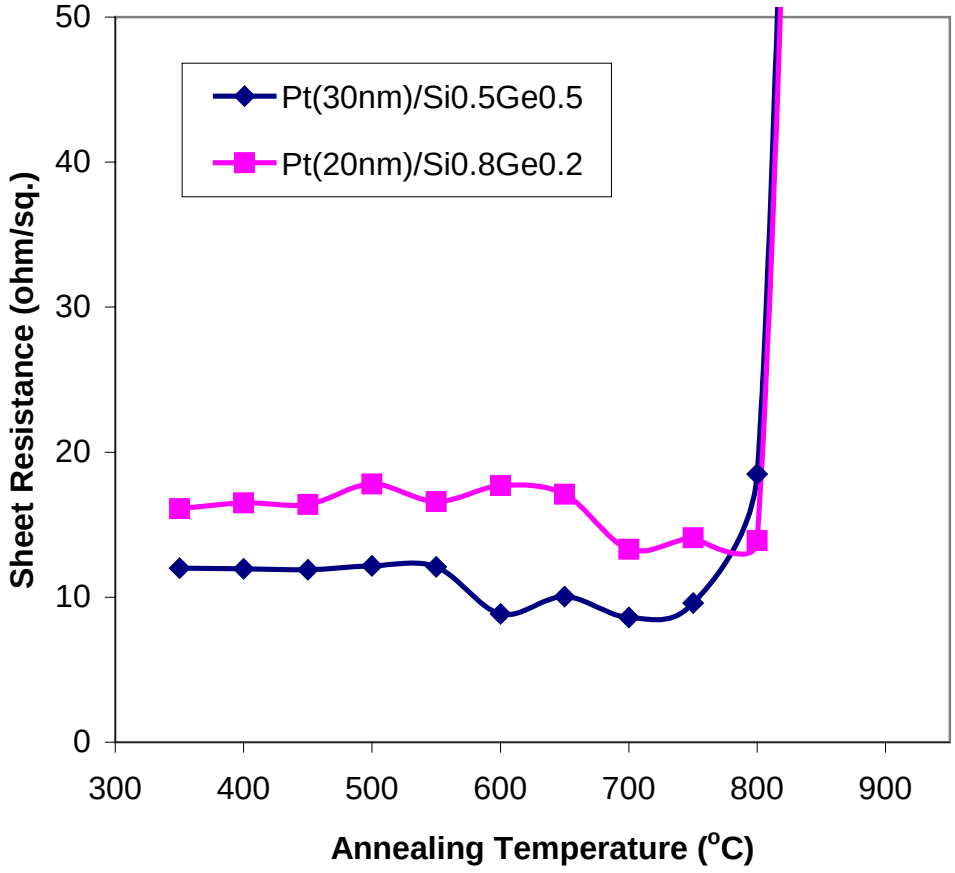

Figure III-12 Comparison of sheet resistance vs. annealing temperature profiles of Pt germanosilicide formation on undoped $Si_{0.5}Ge_{0.5}$ and $Si_{0.8}Ge_{0.2}$.

In Figure III-13, the sheet resistance data show that the thermal stability of germanosilicides formed using 10nm and 20 nm Pt layers are very similar. This is again different than $NiSi_{1-x}Ge_x$, which demonstrates a strong dependence of thermal stability on Ni thickness.

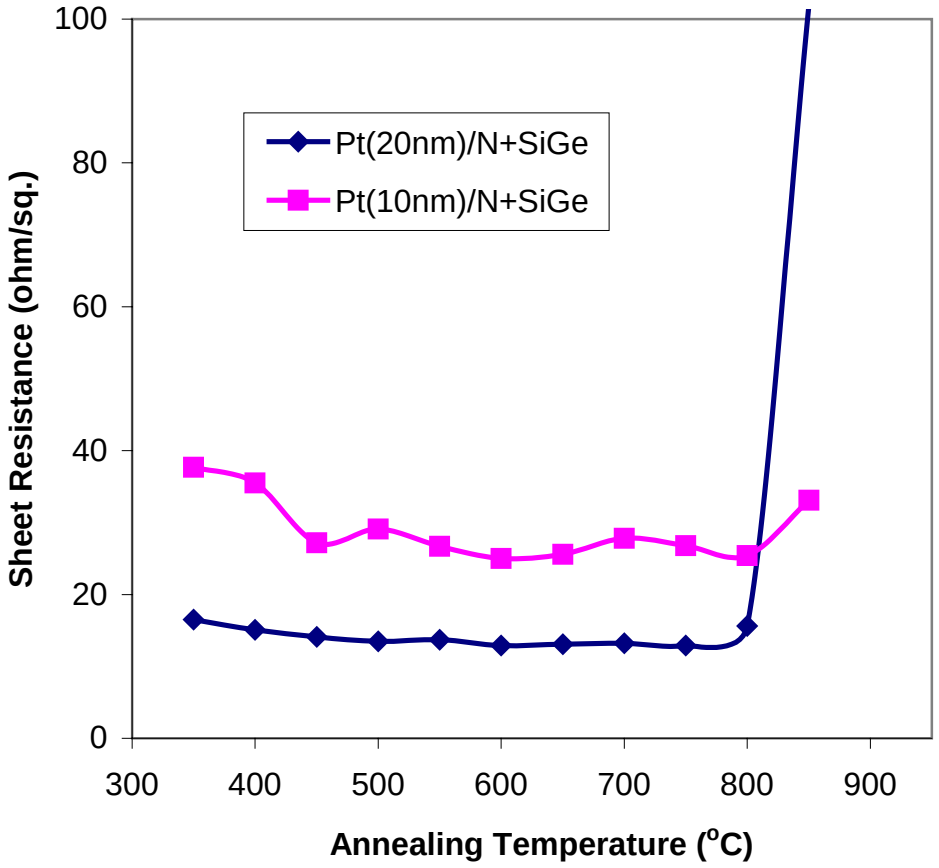

Figure III-13 Comparison of sheet resistance vs. annealing temperature profiles of Pt germanosilicide formation with 20nm and 10nm Pt on N^+SiGe films.

The stability of $PtSi_{1-x}Ge_x$ is clearly better than that of $NiSi_{1-x}Ge_x$ and the Heat of formation can be accounted for the difference. The heat of formation of NiSi, NiGe, PtSi and PtGe are –45, -32, -59, and –46 kJ/mol respectively [10]. There are two factors that determine the thermal stability of a metal-Si-Ge system: the driving force for Ge segregation and the average heat of formation [11]. The driving force for Ge segregation is the difference in the heat of formation between the silicide and the germanide. On the other hand, their average can be viewed as a measure of the strength of the atomic

bonding. A higher average implies a more stable system. The driving force for Ge segregation is 13 kJ/mol for Ni and Pt. On the other hand, the average heat of formation is 52.5 kJ/mol for Pt, which is much higher than that of Ni, which is 38.5 kJ/mol.

The results of Pt(SiGe) formed on P+SiGe with 50% Ge also show that Pt(SiGe) can withstand higher temperature than Ni(SiGe). Pt(SiGe) formed with 10nm of Pt can remain stable to 800°C. The increasing sheet resistance at higher temperatures is probably due to severe Ge segreation, which is also found in H.K. Liou's study[12].

III.4 Zirconium Germanosilicide

As stated in Chapter I, Zr results in a germanosilicide, which is more stable than the germanosilicides of Ni and Pt. To study the properties of $Zr(Si_{1-x}Ge_x)_2$ layers formed on heavily phosphorus doped layers, 30 nm thick Zr films were sputtered onto three different substrates: lightly doped Si, undoped $Si_{1-x}Ge_x$, and heavily phosphorus doped $Si_{1-x}Ge_x$. The temperature dependence of the sheet resistance is shown in Figure III-14. It can be observed that, the sheet resistance goes down with the annealing temperature until 700°C where the minimum sheet resistance is reached for the three substrates used. The effect of the parallel low resistance path is again evident for the heavily doped $Si_{1-x}Ge_x$.

The XRD spectra of the samples annealed at different temperatures are shown in Figure III-15. At 500°C, Zr(SiGe) is the dominant phase with a single <102> peak at a 2Θ value of 36.55. At 600°C, a second peak begins to appear at 39.10 corresponding to the <131> digermanosilicide phase and the intensity of this peak appears to increase with

temperature. However, it is interesting to note that the <102> monogermanosilicide peak still exists even after annealing at 900°C, which suggests that the conversion to digermanosilicide is still not complete.

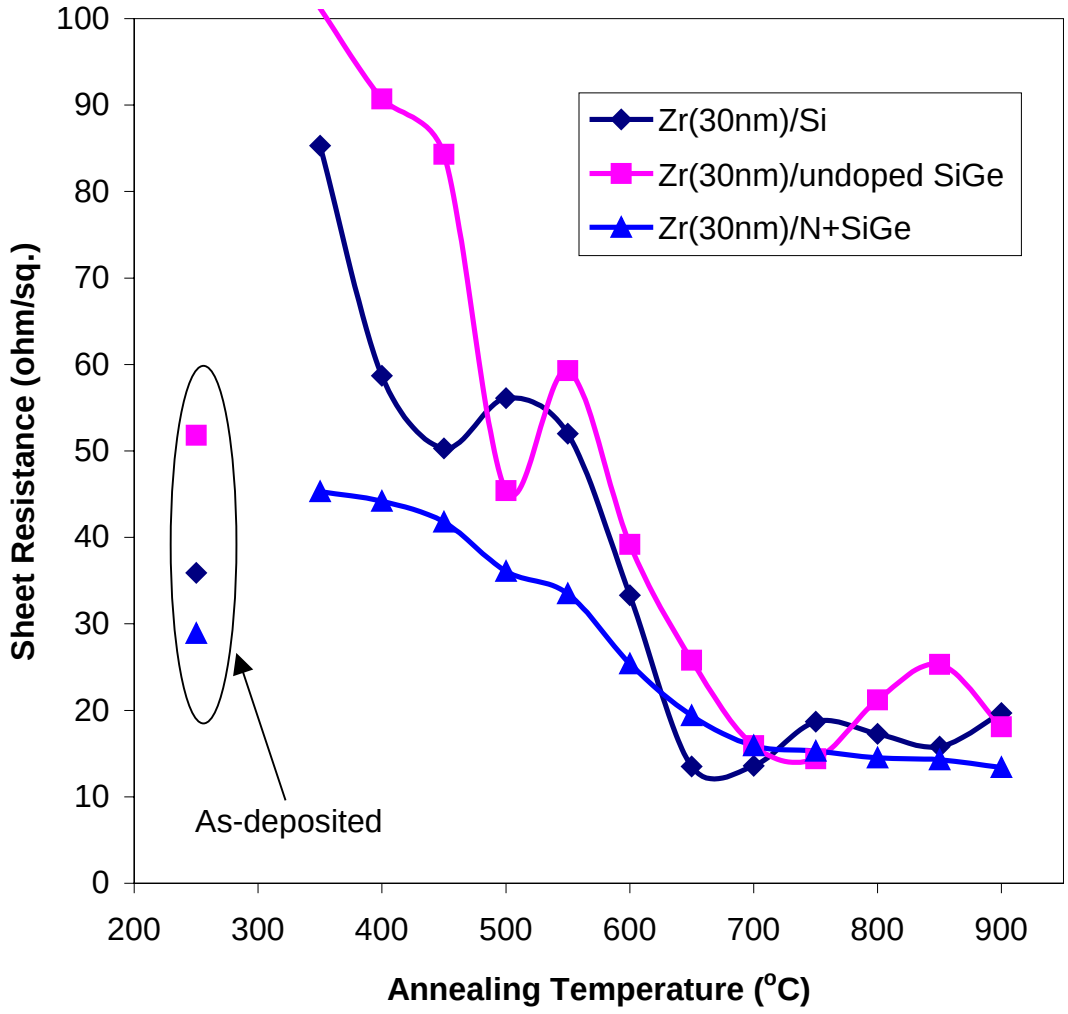

Figure III-14 Sheet resistance as a function of annealing temperature for 30 nm Zr on undoped $Si_{0.8}Ge_{0.2}$, phosphorus doped $Si_{0.8}Ge_{0.2}$ and Si substrates.

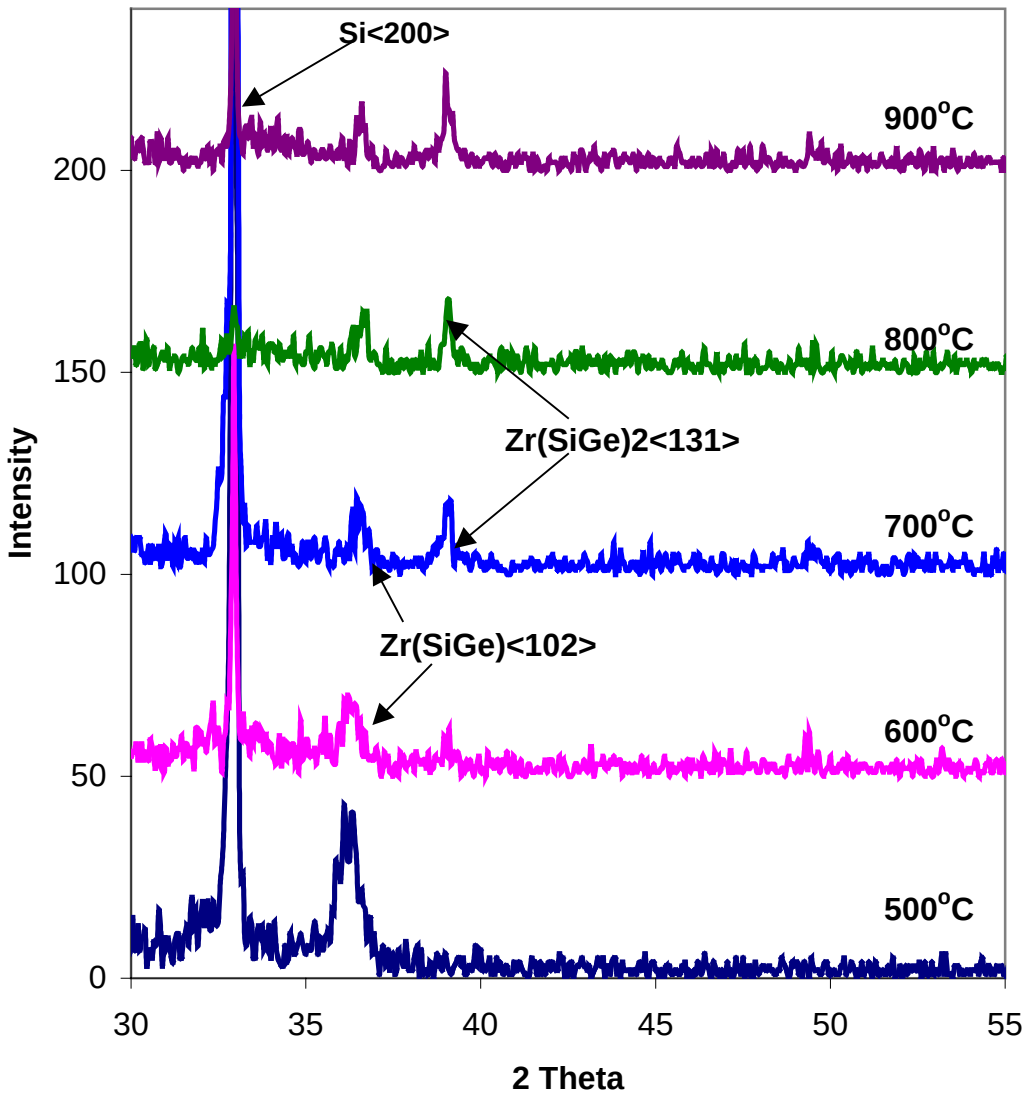

Figure III-15 XRD spectra of 30nm Zr on phosphorus doped SiGe after annealing at 500 to 900°C

At temperature above 700°C, the sheet resistance values obtained from the three samples are very close to one another. Since 1 nm Zr can form ~ 2.17 nm of $ZrSi_2$ we expect the thickness of the silicide to be ~ 65nm corresponding to a resistivity of 104μΩ-cm.

The clear advantage of Zr over Ni and Pt is its thermal stability. However, the fact that it is a digermanosilicide implies that it will result in a larger substrate consumption than the silicides of Ni and Pt. The material also has a higher resistivity than $NiSi_{1-x}Ge_x$, which may be an issue for certain applications.

From the sheet resistance results, phosphorous doping does not affect the resistivity and thermal stability of $Zr(Si_{1-x}Ge_x)_2$. In J. Liu's work, a large amount of boron was found in the $Zr(Si_{1-x}Ge_x)_2$ layer, which may due to the formation of a Zr-B compound [13]. The doping level at the germanosilicide/$Si_{1-x}Ge_x$ interface can thus be reduced, which should then increase the contact resistivity. In this study, phosphorous distribution after $Zr(Si_{1-x}Ge_x)_2$ formation has also been investigated, which will be shown in chapter 5.

III.5 Summary

As a summary of this chapter, the properties of Ni, Pt and Zr germanosilicides are compared in Table III-1.

The results in this chapter show that both $Ni(Si_{1-x}Ge_x)$ and $Pt(Si_{1-x}Ge_x)$ are promising candidates. The thermal stability of $Ni(Si_{1-x}Ge_x)$ on $Si_{0.5}Ge_{0.5}$ is rather poor. While $Zr(Si_{1-x}Ge_x)_2$ is the most stable germanosilicide, it is also the least desirable due to its high resistivity and higher substrate consumption.

Table III-1 Comparison of Best Candidates on Boron and Phosphorus Doped $Si_{1-x}Ge_x$

	$NiSi_{1-x}Ge_x$	$PtSi_{1-x}Ge_x$	$Zr(Si_{1-x}Ge_x)_2$
Resistivity (μΩ-cm)	18	52	>100
Formation temperature (°C)	~350	~350	>700
Maximum Temperature (°C)	~600 for 20%Ge ~450 for 50%Ge	~750 for 20%Ge ~700 for 50%Ge	>900
Substrate consumption	2.1	2.0	2.15

III.6 References

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IV. Nickel Germanosilicide Formation with a metal interlayer

The p^+-n junctions studied by Jing Liu during his doctoral work used $Si_{1-x}Ge_x$ alloys with Ge concentrations as high as 50 %. This was necessary to increase the doping activation and to reduce the $Si_{1-x}Ge_x$ band gap for lower contact resistivity. Jing Liu studied $NiSi_{1-x}Ge_x$ formation on boron doped $Si_{1-x}Ge_x$ layers and concluded that the material was stable only up to ~ 450°C[1-2]. To improve the thermal stability of the germanosilicide he inserted a thin Pt layer under Ni. This approach was previously used by L.W. Cheng et al to improve the thermal stability of NiSi[3-5]. Jing Liu showed that a significant improvement in stability was possible by using a Pt layer, which was as thin as 10% of the Ni layer. Jing Liu demonstrated that on undoped $Si_{1-x}Ge_x$ the stability improvement was about 200°C but on heavily boron doped $Si_{1-x}Ge_x$, the germanosilicide appeared to be stable up to 800°C.

The work presented in previous chapters of this thesis also showed that germanosilicide stability was a concern for phosphorus doped $Si_{1-x}Ge_x$ layers. However, because the Ge concentration in phosphorus doped layers was limited to ~ 20%, the phosphorus doped films were in general more stable than the germanosilicides formed by Jing Liu on boron doped $Si_{1-x}Ge_x$ layers.

The goal of the research project that provided funding for the experimental work presented in this thesis was to develop a self-aligned contact process that worked on both

p^+-n and n^+-p junctions. Therefore, the dual-layer approach proposed by Jing Liu had to be tested on phosphorus doped $Si_{1-x}Ge_x$ layers as well, which is the focus of this chapter.

IV.1 Germanosilicide Formation Using a Metal Interlayer

In the dual-metal approach, a thin interlayer is inserted between the $Si_{1-x}Ge_x$ and the primary metal, as shown in Figure IV-1. In the sputtering system constructed at NCSU, these two metal layers can be sputtered sequentially without breaking the vacuum thus reducing the possibility of any interface contamination. What happens to the thinner metal during the germanosilicide formation anneal is of interest. During this anneal, the interposed metal can stay at the interface, distribute uniformly across the germanosilicide or segregate at the surface.

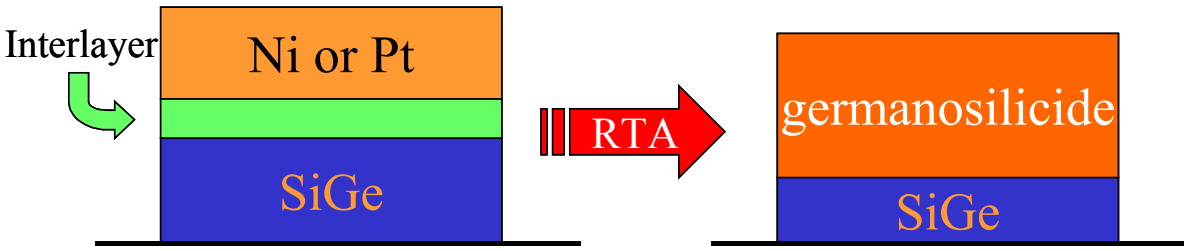

Figure IV-1 Germanosilicide formation using a metal interlayer.

Consideration of Pt as an interlayer is a straightforward choice since PtSi, PtGe, NiSi, and NiGe share the same orthorhombic lattice structure and all four compounds have very similar lattice constants as shown in Table IV-1 [6]. Furthermore, Pt was successfully used on boron doped $Si_{1-x}Ge_x$ layers by Jing Liu [1].

Table IV-1 Lattice constants of Pt and Ni silicide and germanide

	A	B	C
NiSi	5.66	5.23	3.26
NiGe	5.81	5.38	3.43
PtSi	5.94	5.60	3.60
PtGe	6.09	5.73	3.70

In addition to Pt, Zr was also considered as an interlayer. The work on Zr was in progress when it was determined in the project that Pt could successfully serve as the interlayer. After that discovery, the focus of this work shifted to Pt as prime interlayer candidate. The results on Zr are nevertheless included in this thesis, with the hope that the results will be helpful for other future applications.

IV.2 Nickel Germanosilicide Formation with an Interlayer

IV.2.1 Zirconium Interlayer

Shown in Figure IV-2 is the sheet resistance of $NiSi_{1-x}Ge_x$ layers formed with and without Zr interlayers. Without the interlayer, the Ni thickness was 30 nm and was reduced to 25 nm with the interlayer. Two different Zr thicknesses of 2 and 5 nm were considered. It can be seen in Figure IV-2 that there is not an obvious improvement in the germanosilicide thermal stability compared to the pure Ni case. With the Zr interlayer, the sheet resistance is higher, which is not surprising. At very low temperatures, Zr seems to act as a diffusion barrier for Ni since it requires higher temperatures to reach the

lowest sheet resistance value. This effect is more predominant with a thicker Zr interlayer. As shown, increasing the Zr thickness from 2 nm to 5 nm pushes the temperature needed to reach the low sheet resistance point by ~50°C.

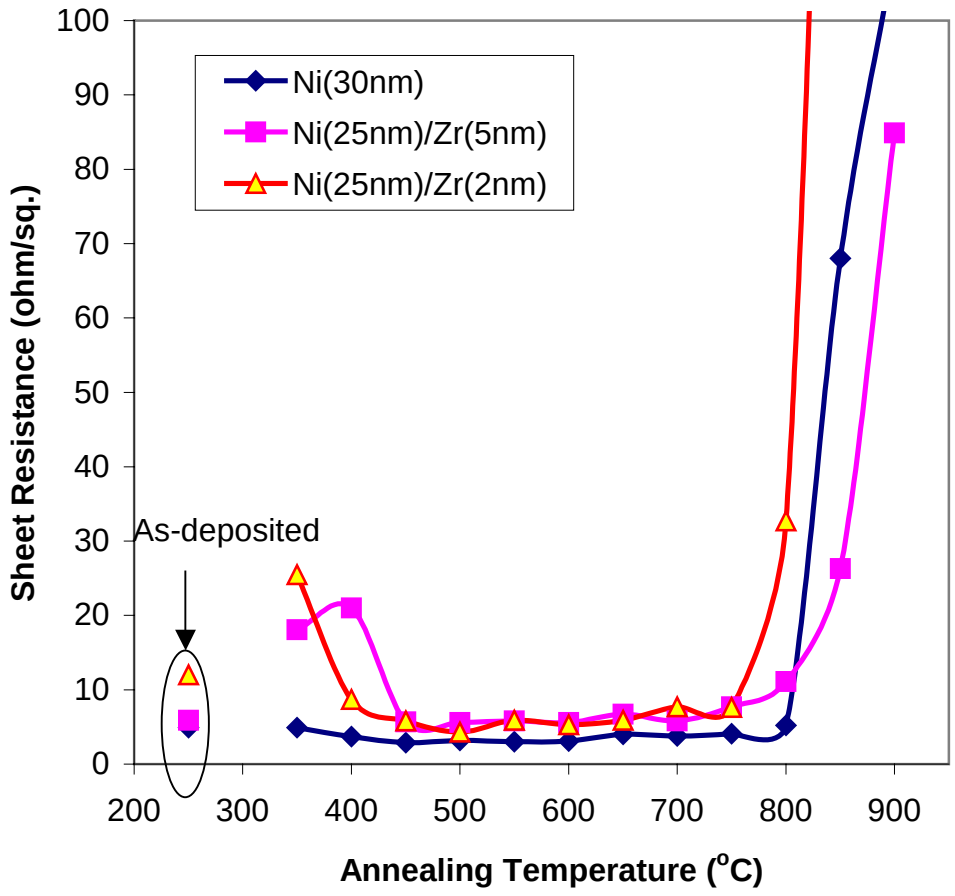

Figure IV-2 Sheet resistance of nickel germanosilicide plotted as a function of the formation temperature. A thin zirconium interlayer was used between Ni and phosphorus doped $Si_{1-x}Ge_x$.

Since the thermal stability is worse for thinner films, the effect of the Zr interlayer was investigated for thinner Ni layers. Shown in Figure IV-3 is the sheet resistance as a function of the formation temperature for a Ni thickness of 10 nm. The thickness of the Zr interlayer is 2 nm corresponding to 20% of the primary metal. It can be seen that similar to the behavior observed in Figure IV-2, the sheet resistance of both samples begin to go up right around the same temperature of ~ 700°C. Once again, the low sheet resistance point is pushed to higher temperatures by the inclusion of the Zr interlayer.

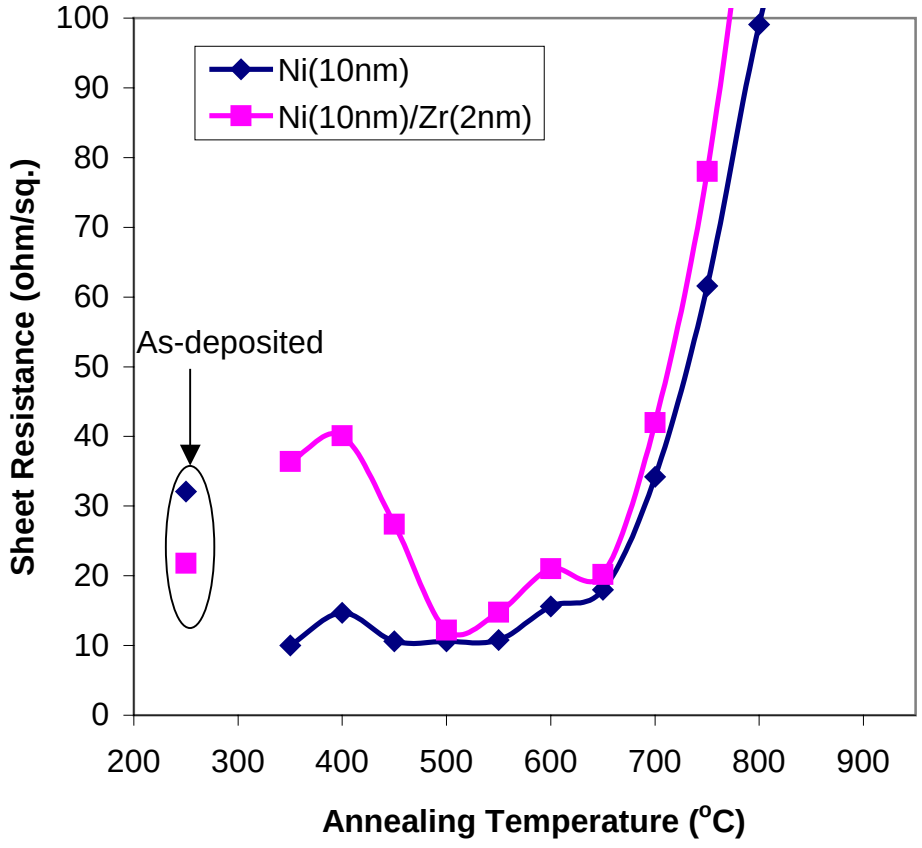

Figure IV-3 Sheet resistance as a function of annealing temperature for 10nm Ni germanosilicide formed with a Zr interlayer. The starting Ni and Zr thicknesses are 10nm and 2nm respectively.

XRD spectra obtained after annealing the Ni(25nm)/Zr(5nm)/$N^+Si_{1-x}Ge_x$ structure at different temperatures is shown in Figure IV-4. Above 450ºC, Zr monosilicide is the dominant phase. The digermanosilicide phase is clearly visible at 800ºC, which evidently requires temperatures above 600ºC.

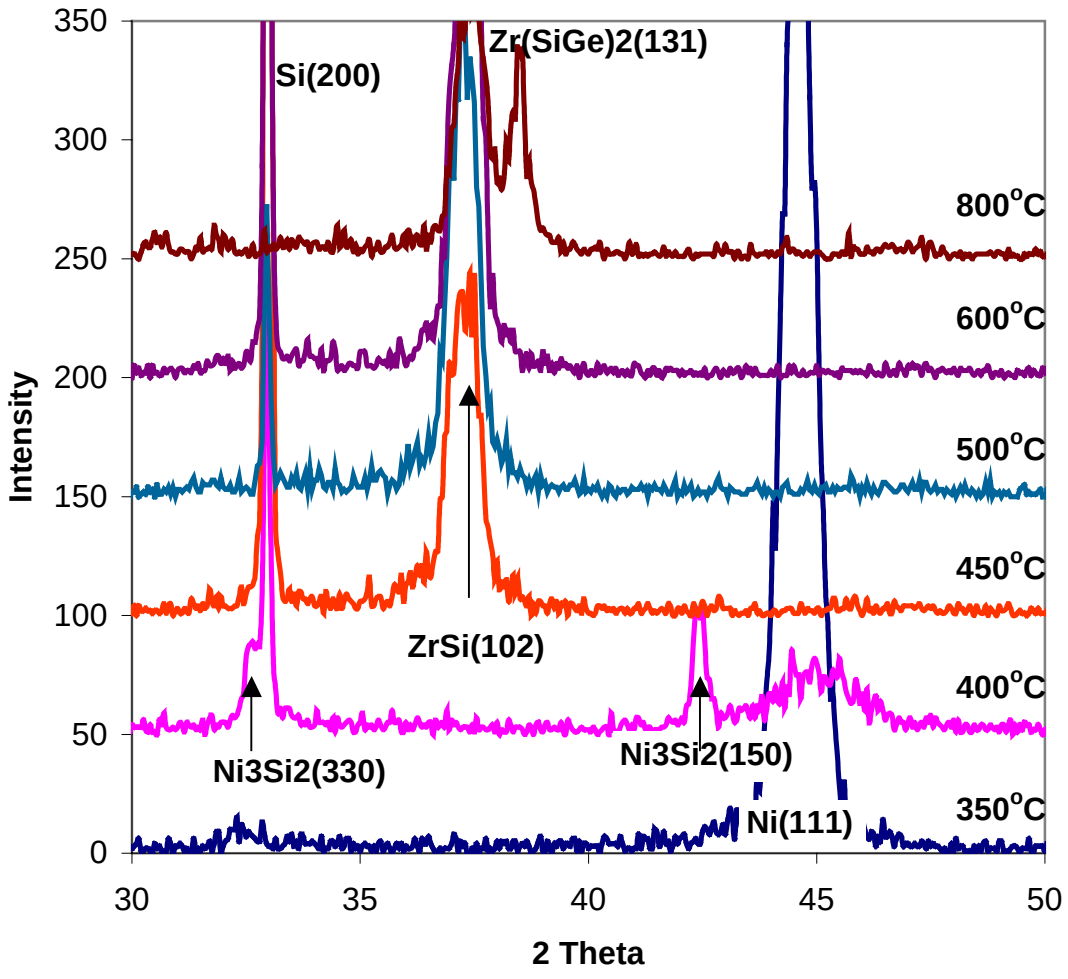

Figure IV-4 XRD spectra of Ni germanosilicide formations after annealing Ni(25nm)/Zr(5nm)/N^+ $Si_{1-x}Ge_x$ at different temperatures.

It is interesting to note that there exists a large Ni peak in the sample annealed at 350°C, which is not the case without the Zr interlayer as shown in Chapter III. This is suggestive of the role of Zr as a diffusion barrier at lower temperatures. In Figure IV-4, there also exists a metal-rich Ni silicide phase (Ni_3Si_2) for the annealing temperatures of 350 and 400°C, which is a high resistivity phase. Therefore, the high sheet resistance value obtained at 400°C in Figure IV-3 can be due to the formation of Ni_3Si_2,.

Previous studies have shown that the normal phase sequence for Ni and Si is: dimetal silicide, monosilicide, and disilicide. This is also the phase sequence for the Ni and $Si_{1-x}Ge_x$ system. In chapter III, XRD spectra show that the Ni_2Si phase formed at temperatures lower than that required for $Ni(Si_{1-x}Ge_x)$.

XRD spectra in Figure IV-4 indicates that with a Zr interlayer, Ni_3Si_2 is formed instead of Ni_2Si. In Ni silicide formation, Ni is the diffusion species. When Zr is used as an interlayer, Ni atoms need to diffuse through the Zr barrier layer to react with the $Si_{1-x}Ge_x$ layer, which may explain formation of the Ni_3Si_2 phase instead of Ni_2Si.

IV.2.2 Platinum Interlayer

Pt was successfully used by Jing Liu to improve the thermal stability of Ni germanosilicide on boron doped $Si_{1-x}Ge_x$. Shown in Figure IV-5 is the sheet resistance of Ni germanosilicide formed on phosphorous doped $Si_{1-x}Ge_x$ as a function of the annealing temperature. The thickness of the Pt interlayer is 5 nm. As shown, there appears to be a small improvement in thermal stability with the Pt interlayer. However, we also note that

the sheet resistance is already fairly stable without the Pt interlayer. As discussed previously, this is partly due the low Ge concentration of the alloy and partly due to the thickness of the starting metal.

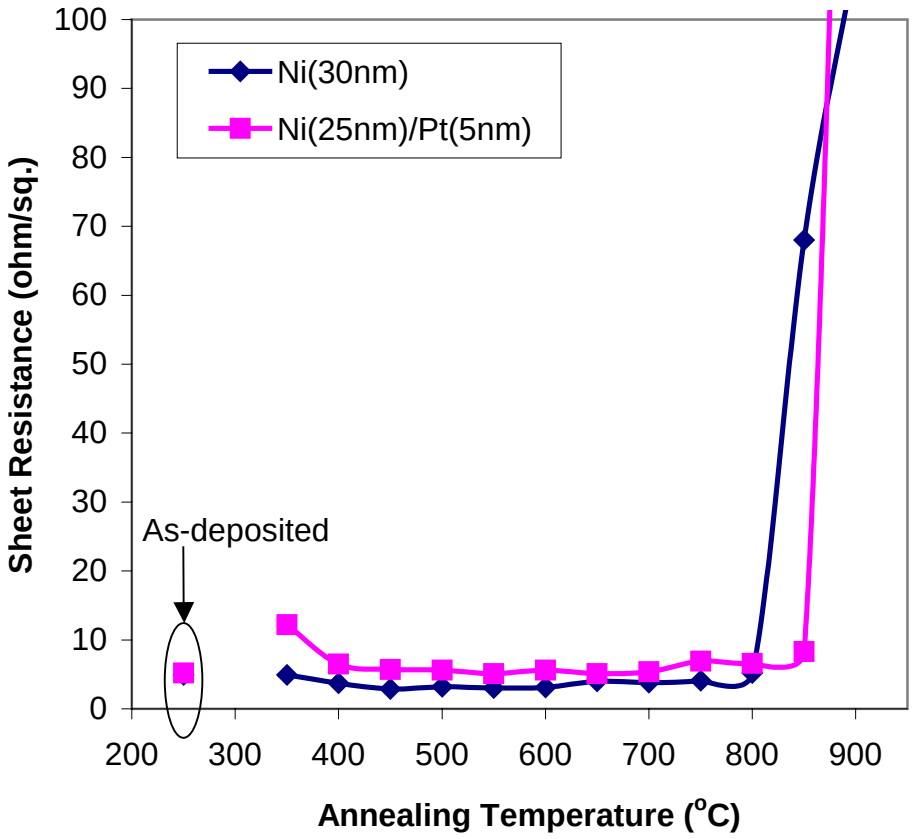

Figure IV-5 Sheet resistance of Ni(25nm)/Pt(5nm)/N^+ $Si_{1-x}Ge_x$ structure after annealing at different temperatures.

To study germanosilicide formation with thinner metal layers, the thickness of both Ni and Pt was varied from 1 to 10 nm and the measurement results are shown in Figure IV-6. The total metal thickness was kept constant at 10 nm. For all samples included in Figure IV-6, Pt was the first metal deposited even if the Pt thickness was larger than the Ni thickness. As shown, pure Pt has the best thermal stability while pure Ni has the worst. In between, the samples demonstrate varying degrees of improvement depending on the Pt percentage.

According to the classic theory of nucleation, the formation of a new phase is associated with a decrease in free energy and an increase in surface energy [7]. The change of free energy ΔG can be expressed as

$$\Delta G = br^2\sigma - ar^3\Delta G_1$$

where a and b are the geometrical terms, r is the dimension of the new phase, ΔG_1 is the change of energy per volume for formation, σ is the surface energy of the new phase. In our case for Ge atoms to segregate, the size of the Ge nucleus must be larger than r*, which can be expressed as:

$$r^* = \frac{2b\sigma}{3a\Delta G_1}$$

It shows that the surface energy can determine the size of the nucleus needed to form a stable phase. The presence of Pt in the film may change the surface energy, which suppresses the Ge segregation from the $NiSi_{1-x}Ge_x$ grains. Thus, the thermal stability is improved. However, Figure IV-6 also indicates that the germanosilicide layers that contain higher Pt percentages have a higher sheet resistance, which is in agreement with Jing Liu's results.

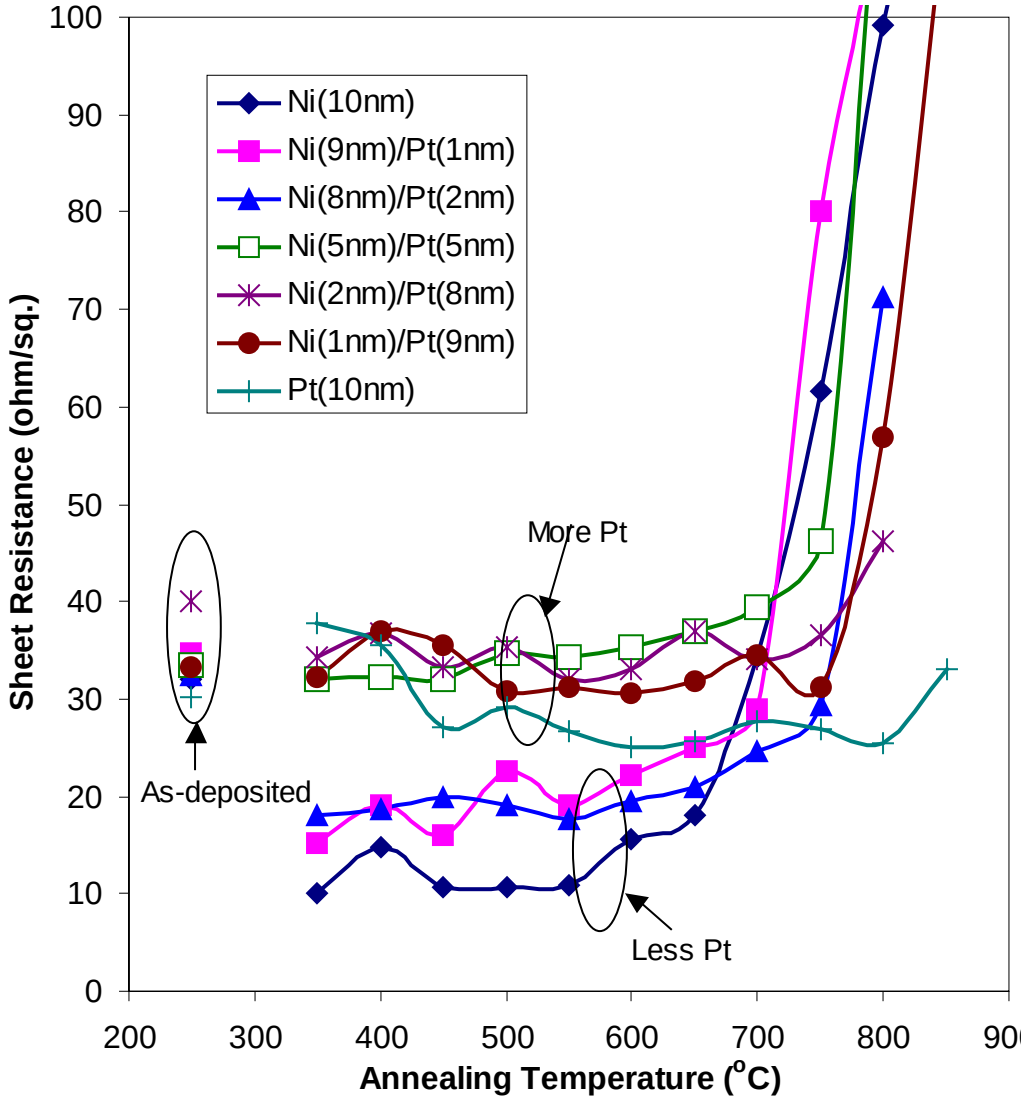

Figure IV-6 Ni germanosilicide formations with various Ni/Pt ratios. The total Ni and Pt thickness is 10nm.

To see the impact of depositing Ni before the Pt layer, samples were prepared following the same procedure except the order of the deposition of the two metal layers. The results are shown in Figure IV-7. As shown, again the best stability is obtained with pure Pt and the stability degrades as the percentage of the Ni layer is increased. This result indicates that the order of Ni and Pt does not matter, which may suggest that instead of two layers the two metals can be co-sputtered to obtain the stability improvement.

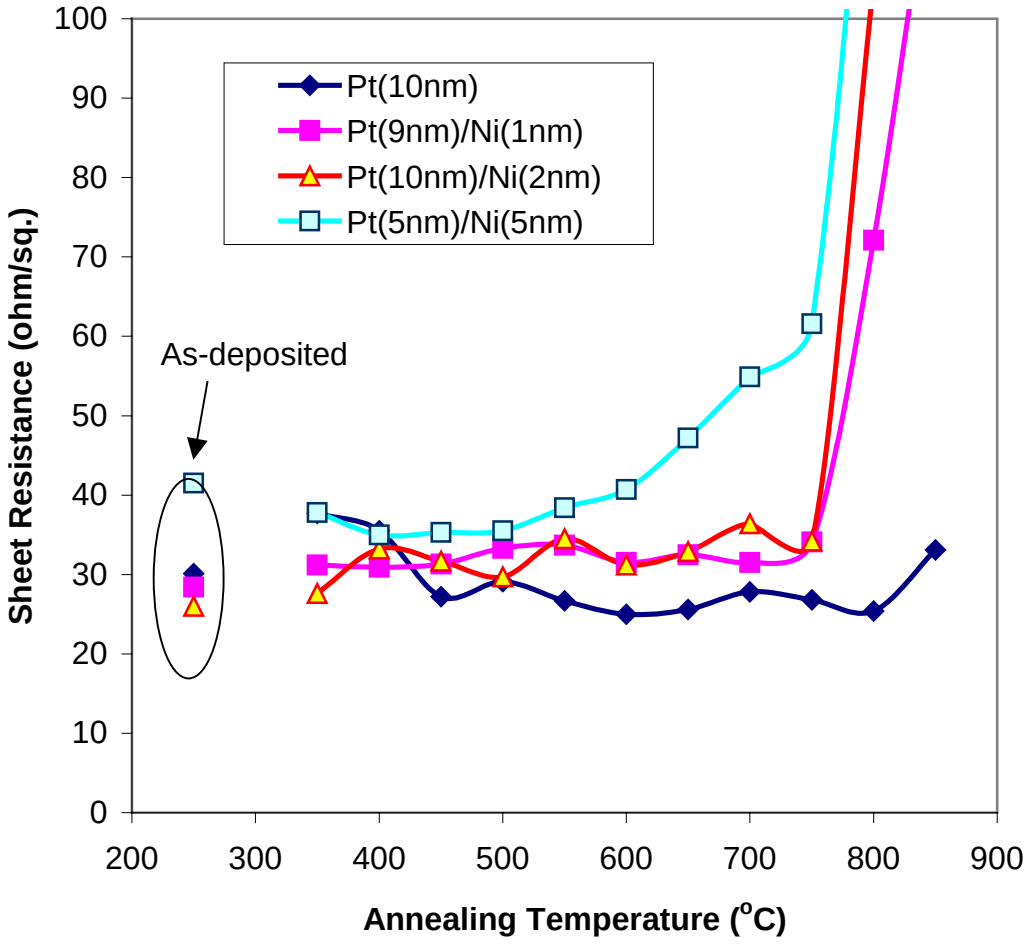

Figure IV-7 Thin Pt germanosilicide formation with Ni interlayer. Sheet resistance is plotted as a function of annealing temperature.

The sheet resistance of $NiSi_{1-x}Ge_x$ varies with the Pt percentage, as shown in Figure IV-8. The sheet resistance goes up to 32.1 Ω/sq. with 50% Pt, which is even higher than that obtained with pure Pt. The sheet resistance stays above 30 Ω/sq. for 50 – 90% Pt.

The germanosilicide thickness of Ni(15nm)/Pt(1.5nm)/$P^+Si_{0.5}Ge_{0.5}$ structure was measured by cross-sectional TEM analysis by J. Liu and was shown to be ~1.94 [1]. This ratio is very close to that of $NiSi_{1-x}Ge_x$ formed without a Pt interlayer. Also, PtSi and NiSi, both have a silicide/metal thickness ratio of about 2.0. All these factors suggest that the germanosilicide formed from Ni/Pt bilayers have the same thickness ratio as $NiSi_{1-x}Ge_x$, NiSi, and PtSi.

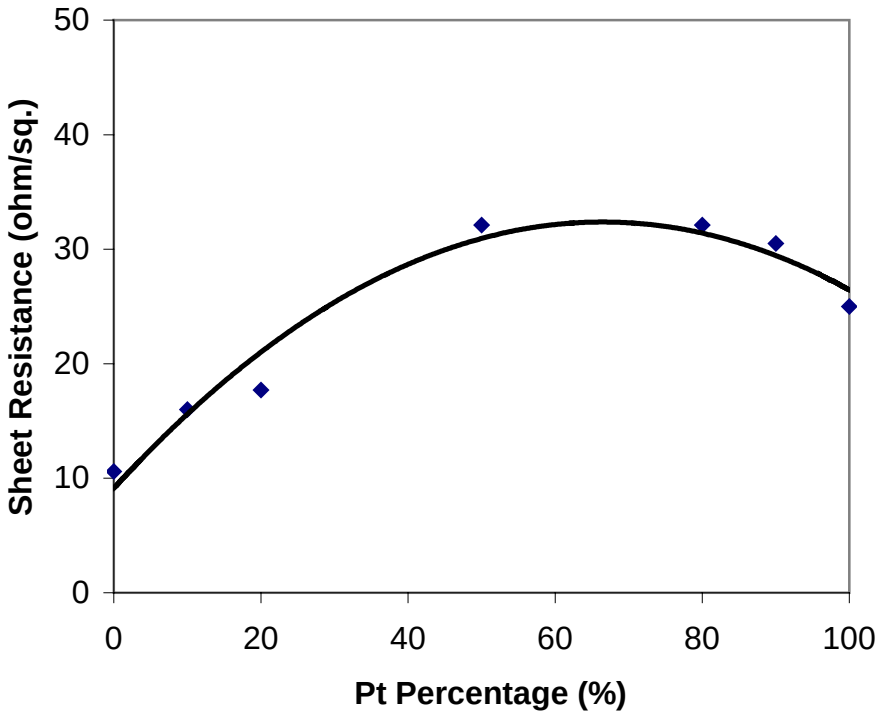

Figure IV-8 Sheet resistance of Ni/Pt germanosilicides plotted as a function of Pt percentage.

The results indicate that Pt behaves very different than Zr. In the Zr case, Ni is the diffusing species and Zr is the diffusion barrier at low temperatures. In the Pt case, Pt readily reacts with both Si and Ge at very low temperatures. Also, NiSi, NiGe, PtSi, and PtGe all have the same lattice structure and very similar lattice constants, which suggest that $NiSi_{1-x}Ge_x$ and $PtSi_{1-x}Ge_x$ can co-exist.

IV.3 Summary

In this chapter, formation of $NiSi_{1-x}Ge_x$ was studied using interlayers of Zr and Pt. The sheet resistance measurements showed that a Zr interlayer would delay $Ni(Si_{1-x}Ge_x)$ formation by 50 - 100°C possibly by acting as a diffusion barrier to Ni. It was also found that the thermal stability of $NiSi_{1-x}Ge_x$ was not affected by the Zr interlayer.

With a Pt interlayer, the thermal stability of $Ni(Si_{1-x}Ge_x)$ on phosphorus doped $Si_{0.8}Ge_{0.2}$ was improved by 50-100°C. The effect of Pt interlayer is not as pronounced as it is in Jing liu's work, where the $Si_{1-x}Ge_x$ film has a much higher (~50%) Ge content [1] A disadvantage of using the Pt interlayer is that the resistivity of the germanosilicide increases with the percentage of the Pt interlayer. It should be noted however that Jing Liu was able to improve the stability of the germanosilicide using Pt layers within 20% of the starting metal thickness, which does not have a significant impact on the resistivity. Furthermore, the resistivity of the germanosilicide may not be as important for future technology nodes, especially when the IC industry starts using metal gates [8].

In his work, Jing Liu always used Pt as an interlayer between Ni and $Si_{1-x}Ge_x$. In this work, we have also considered using Pt as the top layer. The results showed that

similar results could be obtained with Ni as the first layer suggesting that Ni and Pt could be co-sputtered simplifying the integration process.

IV.4 References

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V. Electrical Characterization of Ni and Pt Germanosilicide Contacts

In Chapters 3 and 4 formation of Ni, Pt and Zr germanosilicides was studied using sheet resistance measurements and X-Ray diffraction analysis. This chapter presents electrical characterization of n^+-p junctions with self-aligned germanosilicide contacts. Since the availability of a selective etch process is key to forming self-aligned contacts, this chapter begins with a discussion of the chemical processes used for this purpose. Gated diodes were fabricated to study the impact of the germanosilicide layer on the reverse bias leakage current of the junctions. The contact resistivity of the germanosilicide contacts was studied using four-terminal Kelvin structures. Schottky diodes were fabricated to study the barrier height. SIMS analysis was used to study distribution of Ni, Pt and P during germanosilicide formation.

V.1 Self-Aligned Germanosilicide Formation

In forming self-aligned silicide or germanosilicide contacts, selective etching of the unreacted metal on the insulator surface after metal sputtering and RTA is a critical step. The solution should not etch the germanosilicide or the commonly used materials in CMOS processing. While there are several commonly used selective etching solutions used in self-aligned silicide formation, very few reports exist for germanosilicides [1]. Whether we can use the same selective etching solution as silicide for germanosilicide or not is still unknown.

In this work, we have evaluated several different selective etching solutions for Ni, Pt and Zr germanosilicides. Our emphasis was again on phosphorus-doped layers. The impact of using an interlayer was also studied. The chemicals used in this study are shown in Table V-1.

Table V-1 Concentrations of chemicals used for germanosilicide selective etch

Chemical	Concentration (%)
HCl	33-40
HNO_3	70
H2SO4	66
H_2O_2	30

V.1.1 Self-Aligned $NiSi_{1-x}Ge_x$ Formation

Previous work on NiSi showed that both H_2SO_4+H_2O_2 and HCl +HNO_3 (also known as Aqua Regia) solutions could be used to achieve self-aligned silicide formation [2-5]. Both solutions effectively etch the unreacted Ni on insulator surfaces while not attacking the silicide. In this work, both solutions were tested to form self-aligned $NiSi_{1-x}Ge_x$ layers. In these experiments, the starting Ni thickness was 30 nm and the Ge concentration was 50%. The sheet resistance of the germanosilicide before and after the etch in H_2SO_4+H_2O_2 (1:1) is plotted in Figure V-1. The etching was carried out for 5 min at 110ºC. It can be seen that the sheet resistance does not change with etching indicating that the solution does not attack the germanosilicide. On the other hand, five minutes was sufficient to completely etch the unreacted Ni on the surrounding SiO_2 layer. This result shows suggests that the H_2SO_4+H_2O_2 (1:1) solution can be used to form self-aligned $NiSi_{1-x}Ge_x$ layers.

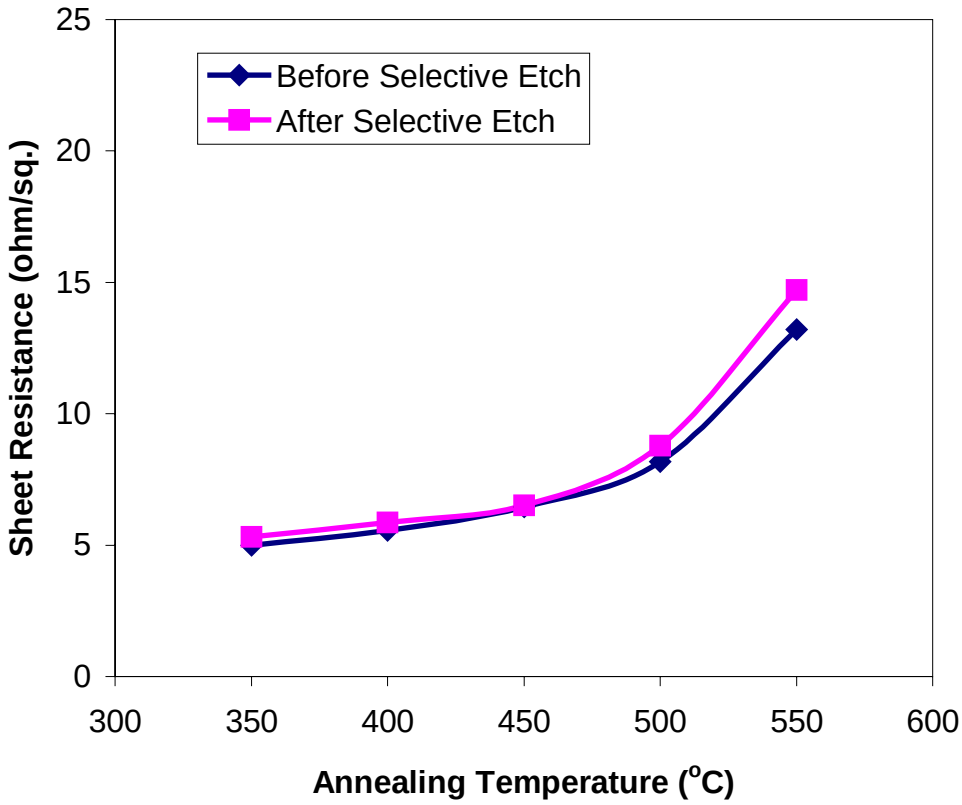


Figure V-1 $NiSi_{1-x}Ge_x$ was formed on $Si_{0.5}Ge_{0.5}$ layers at different temperatures and then selectively etched in $H_2SO_4+H_2O_2$ (1:1) at 110°C for 5 minutes. The plot shows the sheet resistance measured before and after the selective etch.

The experiments showed that Aqua Regia ($HCl+HNO_3+H_2O$) solution could also be used to form self-aligned $NiSi_{1-x}Ge_x$ layers. As shown in Figure V-2, the sheet resistance of the $NiSi_{1-x}Ge_x$ layers formed at different temperatures did not increase after etching them in the Aqua Regia solution. In the mean time, the unreacted Ni left on SiO_2 could be completely removed. However, it was also shown that the selectivity was not comparable to that obtained using the $H_2SO_4+H_2O_2$ (1:1) solution. Higher temperatures or longer processing times can result in significant germanosilicide etching. The selectivity was even worse with higher Ge concentrations as shown in J. Liu's dissertation [6].

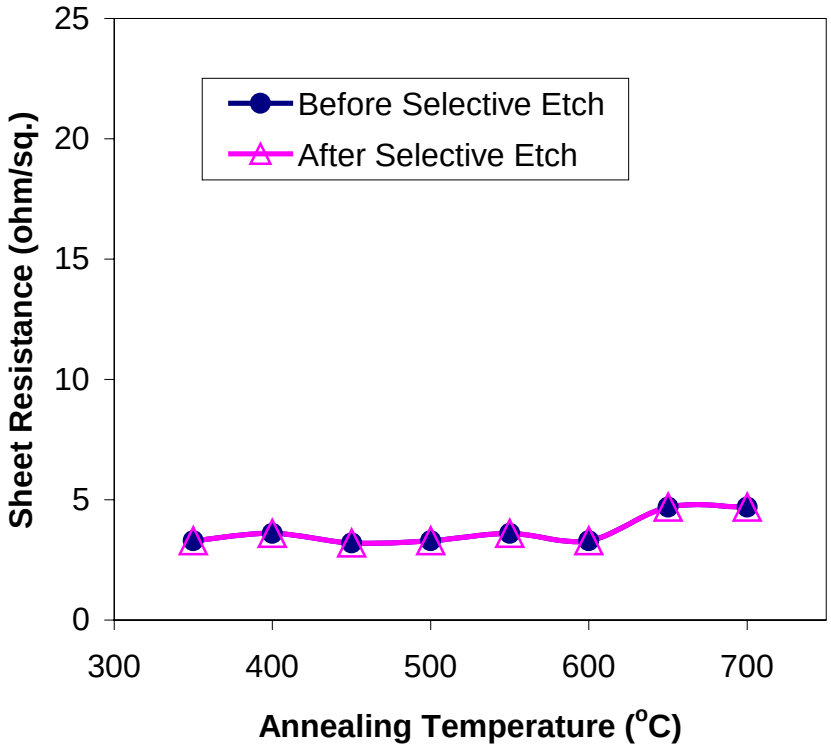


Figure V-2 Sheet resistance of Ni(30nm)/$N^{+}Si_{1-x}Ge_x$ as a function of annealing temperature before and after selective etch in $HCl+HNO_3+H_2O$ (3:1:4), at 70°C for 2 min. The un-reacted Ni on oxide can be completely removed with this condition.

V.1.2 Self-Aligned $PtSi_{1-x}Ge_x$ Formation

It is known that self-aligned PtSi can be formed using the Aqua Regia solution. Thus, we have tried $HCl+HNO_3+H_2O$ (3:1:4) to remove Pt from the insulator after forming the germanosilicide. Similar to the results reported by J. Liu for P^{+} $Si_{1-x}Ge_x$, we showed that this diluted Aqua Regia could be used to form self-aligned $PtSi_{1-x}Ge_x$ layers on N^{+} $Si_{1-x}Ge_x$.

V.1.3 Self-Aligned Germanosilicide Formation with Bi-Layers of Nickel and Platinum

Figure V-3 shows the sheet resistance of $NiSi_{1-x}Ge_x$ as a function of the etching time in $HCl+HNO_3+H_2O$ (3:1:4). This solution was our first choice because it can etch both Ni and Pt. The $NiSi_{1-x}Ge_x$ layers were formed at 600°C and 650°C. As shown, the sheet resistance of both samples remains the same with etching. We note however that without the Pt interlayer, the same solution can etch the germanosilicide at 70ºC. The same observation was also made by Jing Liu for boron doped $Si_{0.5}Ge_{0.5}$ layers [6]. In his work, Jing Liu showed that $NiSi_{1-x}Ge_x$ with x = 0.5 was readily etched in Aqua Regia. However, he also showed that this was not true with the Pt interlayer. The unreacted Ni and Pt layers on SiO_2 can be completely removed in $HCl+HNO_3+H_2O$ (3:1:4) at 70°C within 3 minutes.

We have shown that the above solution is also applicable to $PtSi_{1-x}Ge_x$ formation with a Ni interlayer. In our experiments, the thicknesses of the Pt and Ni layers were 25 and 2 nm respectively.

V.1.4 Self-Aligned $NiSi_{1-x}Ge_x$ Formation with a Zr Interlayer.

To etch the unreacted Ni and the underlying Zr interlayer on the insulator $H_2SO_4+H_2O_2$ (1:1) solution was tried at 90°C. The experiments showed that 25 nm Ni and 2 nm Zr could be etched within 2 minutes. The sheet resistance of $NiSi_{1-x}Ge_x$ before and after etching is shown in Figure V-4, which indicates that the germanosilicide layer is not etched in $H_2SO_4+H_2O_2$ making the solution suitable for self-aligned germanosilicide formation.

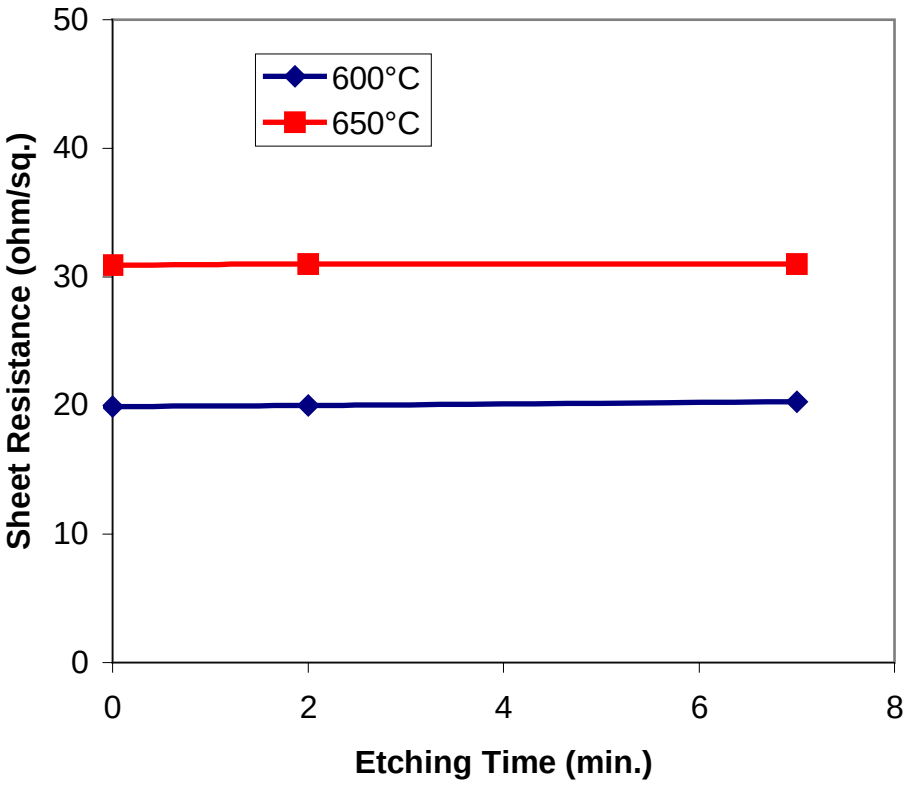


Figure V-3 Ni(10nm)/Pt(2nm)/$N^{+}Si_{1-x}Ge_x$ samples etched in $HCl+HNO_3+H_2O$ (3:1:4) at 70°C. The samples were annealed at 600°C and 650°C respectively.

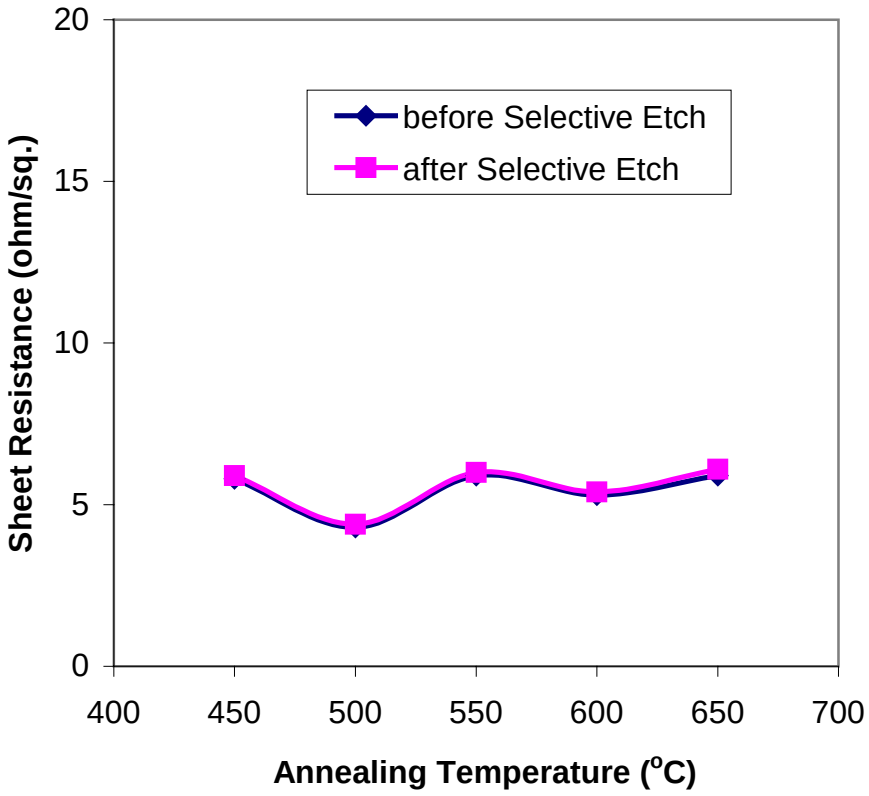


Figure V-4 Comparison of sheet resistance of Ni(25nm)/Zr(2nm)/ N^+ $Si_{1-x}Ge_x$ samples before and after selective etch in H_2SO_4+H_2O_2 (1:1) at 90°C for 2 min.

V.1.5 Self-Aligned $PtSi_{1-x}Ge_x$ Formation with a Zr Interlayer

For $PtSi_{1-x}Ge_x$ formation with a Zr interlayer, it is difficult to find a suitable selective etching solution. H_2SO_4+H_2O_2 can etch Zr but not Pt. Similarly, the Aqua Regia solution can etch Pt but not Zr. Since Aqua Regia can also etch the $PtSi_{1-x}Ge_x$, the etch time can not be too long. At 70°C, the etch times needed to remove the unreacted Pt(25nm)/Zr(2nm) and Pt(10nm)/Zr(2nm) layers were 5 minutes and 2 minutes respectively. The sheet resistance of the germanosilicide formed with 10 nm of Pt

increased about 10% after 2minutes of etching in Aqua Regia. After etching the top Pt layer Zr can be removed in H_2SO_4+H_2O_2 (1:1) at 90°C. A 30nm Zr layer can be etched in by this solution at 90°C within 5 min.

V.2 Diode Leakage

The reverse bias diode leakage is a good indicator of the electrical quality of a $Si_{1-x}Ge_x$ /Si junction. As shown in Figure V-5 depending on the germanosilicide, the starting metal thickness and RTA conditions, the interface between the germanosilicide can be far from the desired smooth interface shown in Figure V-5(a). Agglomeration can roughen the interface with grains approaching the depletion region of the junction resulting in excessive junction leakage due to generation of carriers at the germanosilicide/$Si_{1-x}Ge_x$ interface. With severe agglomeration, the germanosilicide grains can even penetrate through the metallurgical junction as shown in Figure V-5(c).

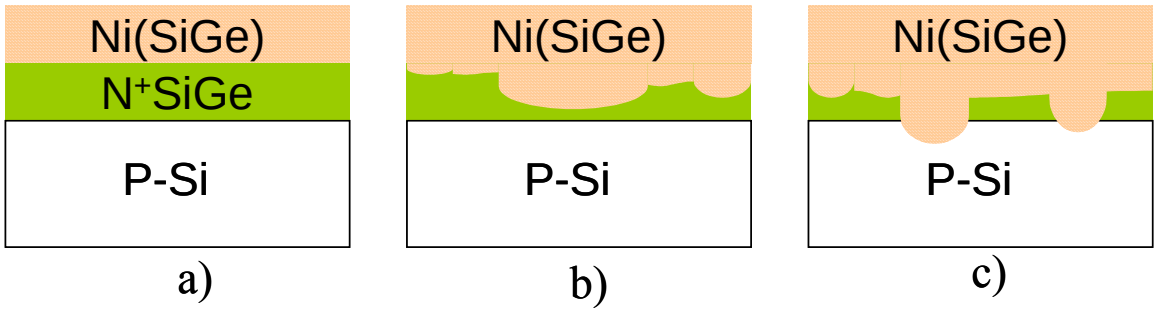


Figure V-5 A) Smooth Ni germanosilicide/$Si_{1-x}Ge_x$ interface. B) Germanosilicide/$Si_{1-x}Ge_x$ interface with interface roughening. C) Germanosilicide penetration through the junction.

V.2.1 Fabrication of the Test Structures

In this work, a gated diode structure was used to measure the leakage current of the junctions. A cross-sectional view of the gated diode structure is shown in Figure V-6.

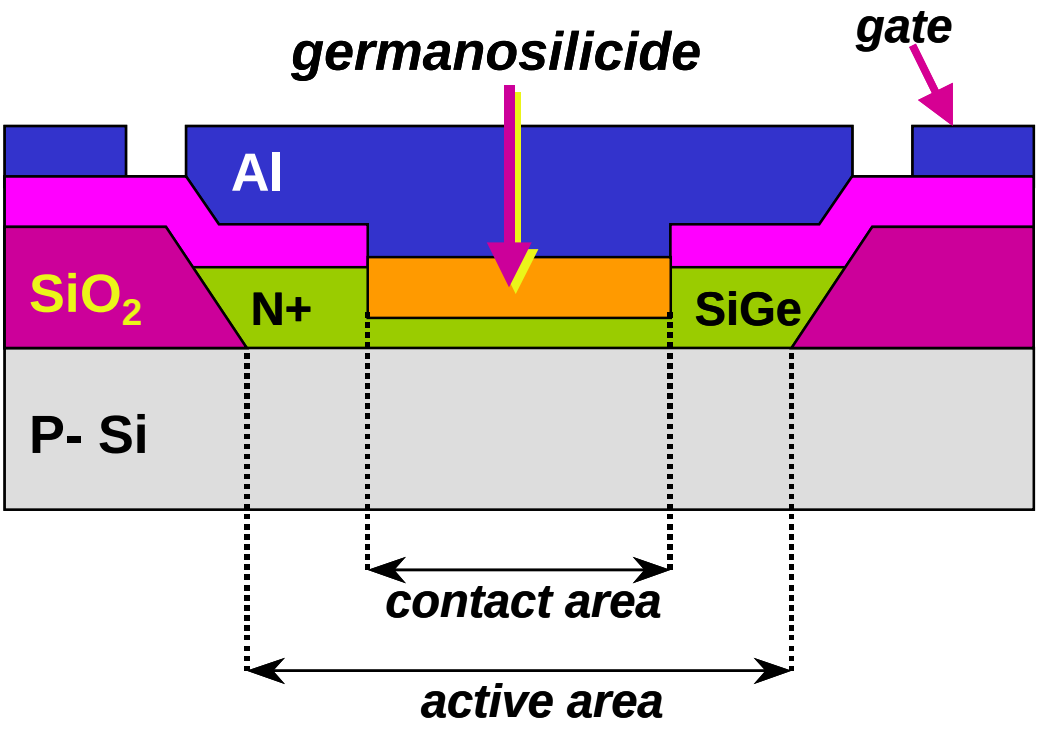
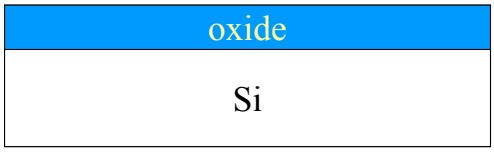
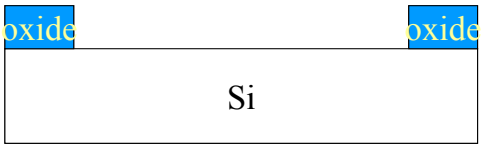
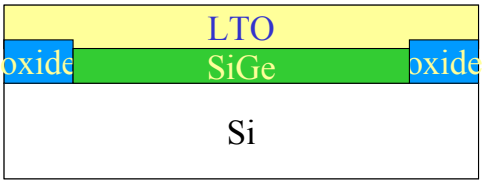


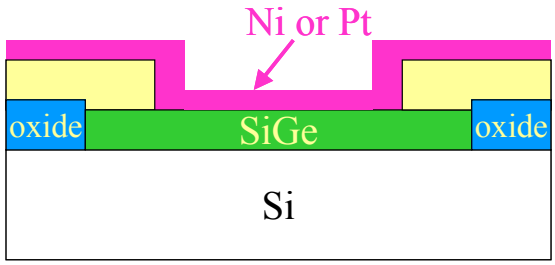
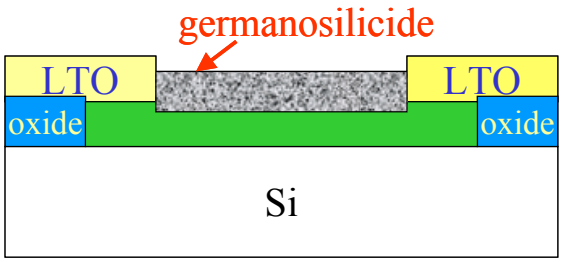
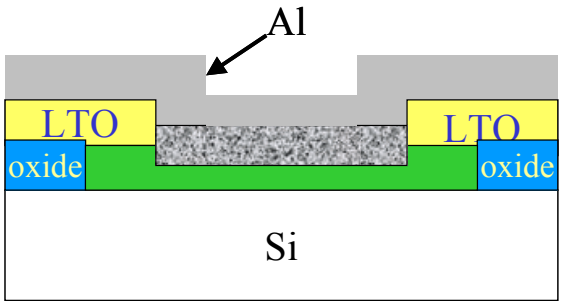
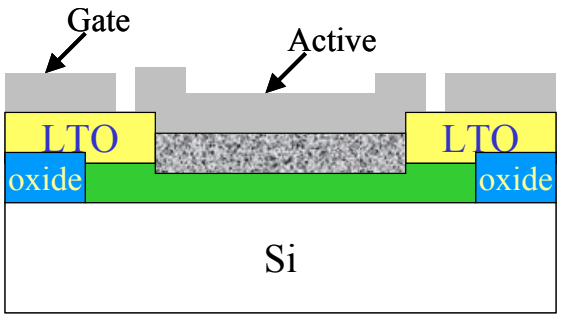
Figure V-6 A cross section view of a gated diode used in this study.

The main fabrication steps are illustrated in Table V-2. The substrates were 6-inch, p-type Si wafers with <100> orientation. The background doping density was $10^{15}/cm^3$. Wet oxidation was carried out in a conventional furnace. The low temperature oxide (LTO) was deposited at ~ 400°C in a conventional low pressure chemical vapor deposition (LPCVD) system using diethylsilane and oxygen. Al and Ti layers were deposited by evaporation. Three masks were used to define the diffusion, contact and metal layers. Patterns were defined by a GCA 800 DSW Wafer Stepper. The Shipley

510A positive photoresist was used and descum was carried out in a March PM-600 Plasma Etcher.

Table V-2 Process steps used in fabrication of the $Si_{1-x}Ge_x$ junctions with self-aligned germanosilicide contacts.

Wet Oxidation 1000 °C /8 min. Thickness: 120nm	
Photoresist spin and soft bake	
Expose photoresist (mask: active)	
Post bake, develop, hard bake and discum	
Etch oxide in BOE and strip photoresist	
RCA clean	
Selective $Si_{1-x}Ge_x$ deposition	
LTO deposition	
Photoresist spin and soft bake	
Expose photoresist (mask: contact)	
Post bake, develop, hard bake and discum	
Etch LTO in 1%HF and strip photoresist	

Metal (Ni and Pt) sputtering	
Rapid Thermal Annealing, Selective etch to remove the un-reacted metal	
Al(250nm)/Ti(50nm) deposition	
Photoresist spin and soft bake	
Exposure in stepper aligner with metal level mask	
Post bake, develop, and hard bake	
Al etch and Ti etch	
Photoresist removal with Accustrip 1165 remover	
Forming Gas annealing in H_2/N_2 (1:10) at 400°C for 30 min. to ensure good contact	

To study germanosilicide induced leakage, a set of diodes with the same active area of 600 x 600 μm^2 but three different germanosilicide areas of 200 x 200, 100 x 100, and 50 x 50 μm^2 were used. The top views of the diode structures are shown in Figure V-7.

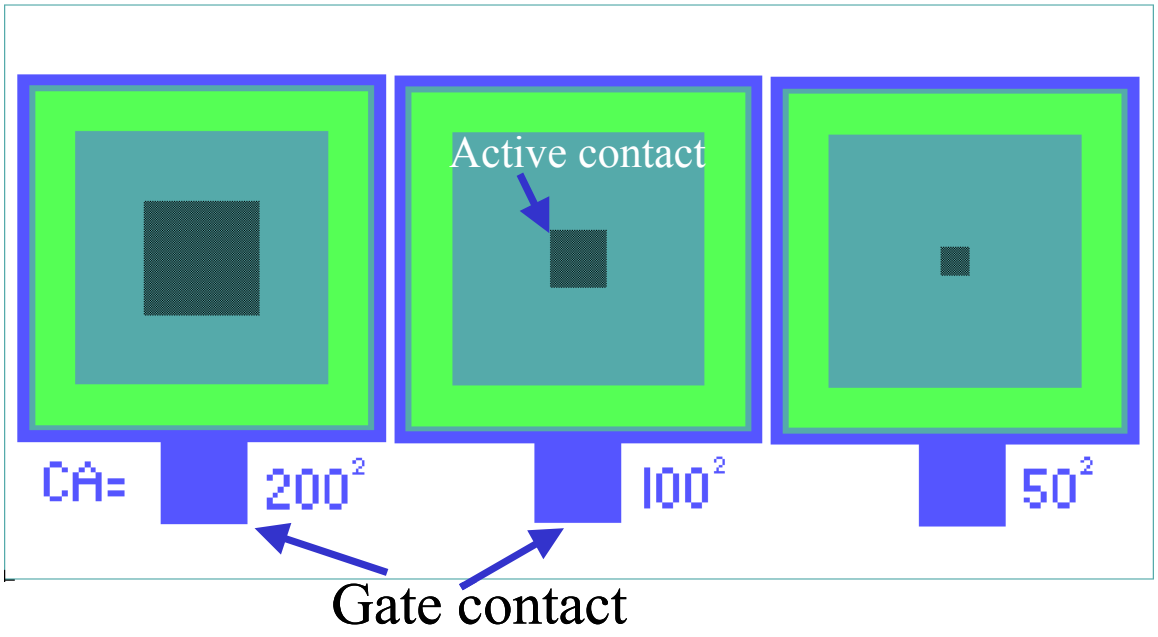


Figure V-7 A top view of the diodes used in this study. The active area is 600 x 600 μm^2. The contact areas are 200 x 200, 100 x 100, and 50 x 50 μm^2.

V.2.2 Junction Leakage without a Germanosilicide Contact

The leakage current of a pn junction diode can be expressed as

$$I = I_A + I_P = J_A \cdot A + J_P \cdot P \qquad (1)$$

where, J_A and J_P are the areal and peripheral leakage current densities, A is the junction area and P is the junction perimeter. J_A and J_P can be extracted if the junction leakage is measured from junctions with different size active areas.

From equation (1),

$$\frac{I}{P} = J_A \cdot \frac{A}{P} + J_P \qquad (2)$$

$$\frac{I}{A} = J_A + J_P \cdot \frac{P}{A} \qquad (3)$$

If I/P is plotted as a function of A/P, J_A can be extracted by finding the slope of the curve. Using the same method, J_P can be extracted by plotting I/A as a function of P/A.

Gated diodes with three different active areas were fabricated with Al/Ti layers. The measurements were carried out at a reverse bias voltage of 1.0 volt. The measurement results are shown in Figure V-8.

Using the average junction leakage currents shown in Figure V-8, J_A and J_P can be extracted using equations (2) and (3). The results of these calculations are shown in Figure V-9 and Figure V-10. From these measurements, the areal leakage component J_A and J_P were determined to be 0.7 nA/cm^2 and 30 pA/cm. Both current densities indicate these are excellent junctions with extremely low reverse leakage current densities.

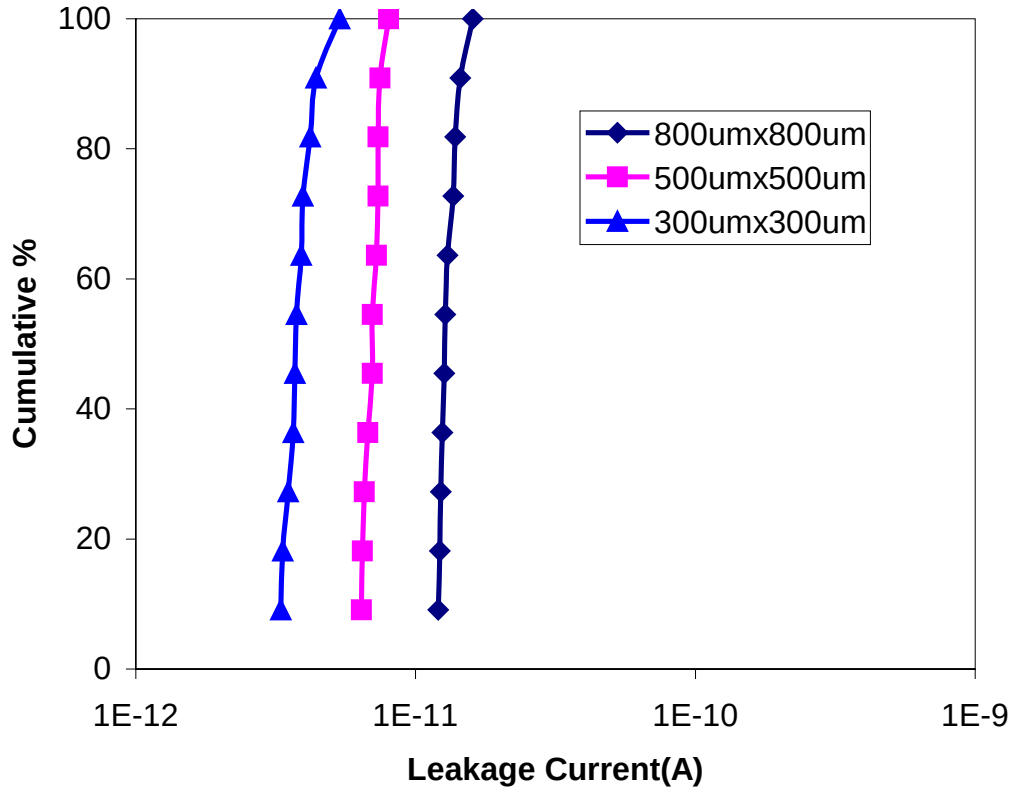


Figure V-8 Leakage currents of a typical N^+ $Si_{0.8}Ge_{0.2}$/P-Si junction with 3 different junction areas: 800 x 800, 500 x 500, and 300 x 300 μm^2. The junctions were reversed-biased with 1.0 volt and an optimal gate bias was applied.

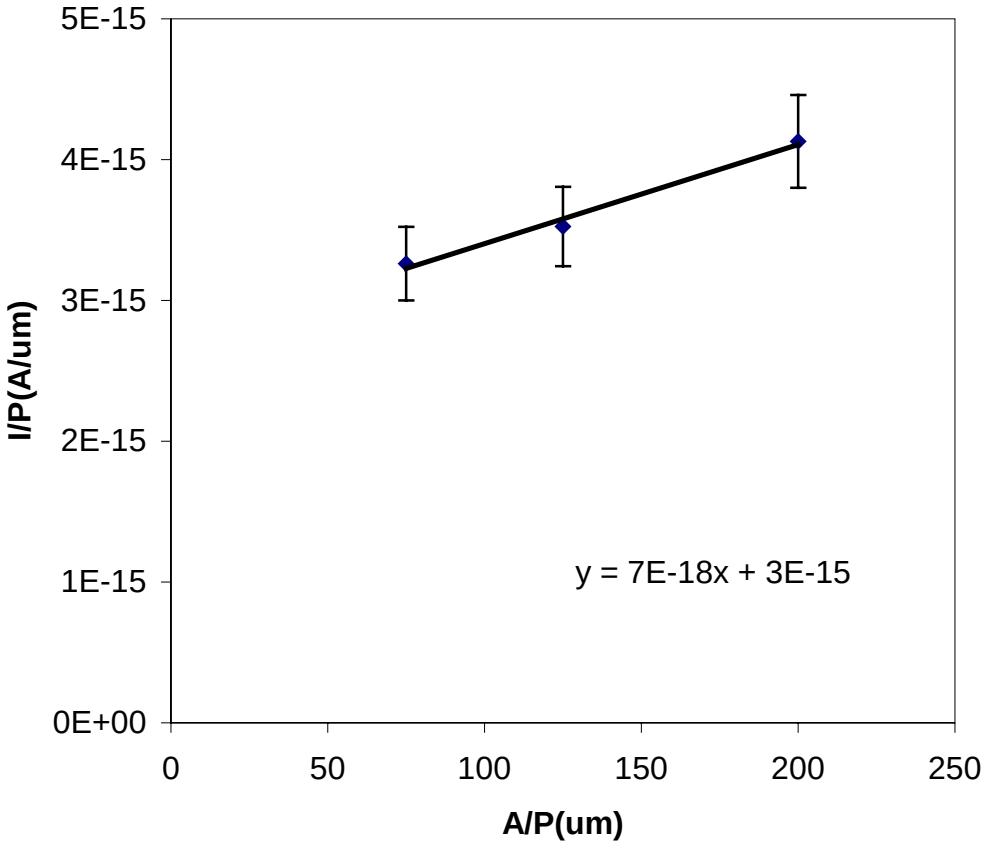


Figure V-9 Areal leakage component (J_A) extraction of N^+ $Si_{0.8}Ge_{0.2}$/P-Si junction.

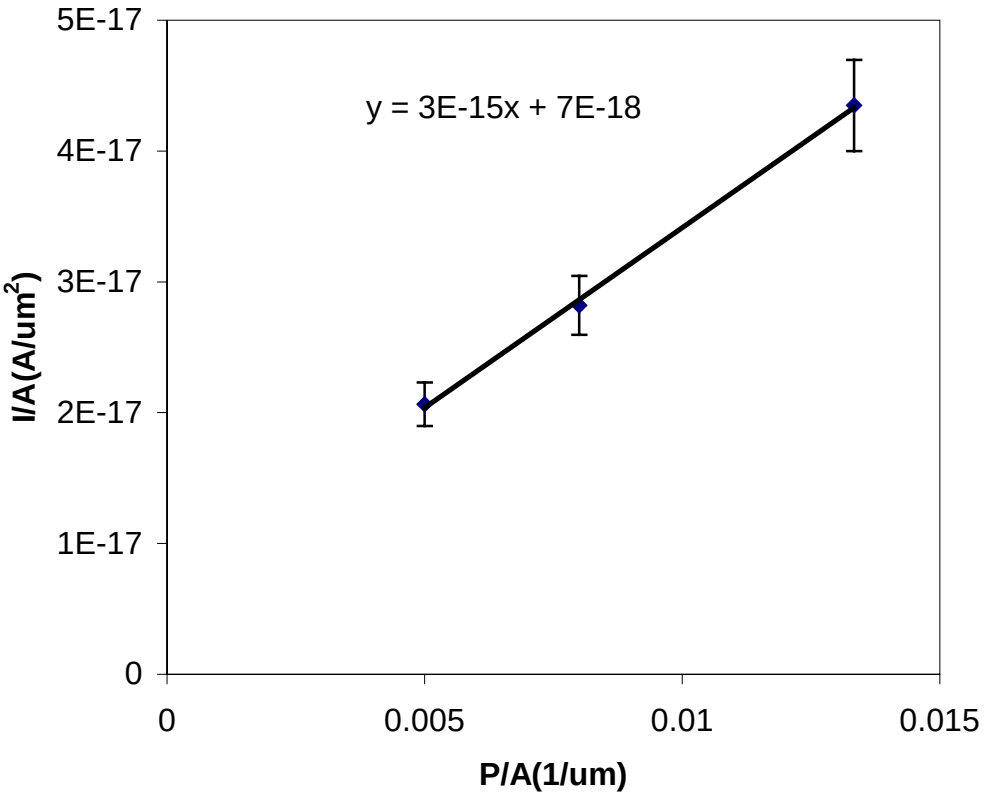


Figure V-10 Peripheral leakage component (J_P) extraction of N^+ $Si_{0.8}Ge_{0.2}$/P-Si junction.

V.2.3 Junction Leakage with Nickel Germanosilicide Contacts

Gated diodes with different contact areas were fabricated using 15nm Ni using the test structures shown in Figure V-7. The thickness of the phosphorus doped $Si_{1-x}Ge_x$ layers was 100 nm. After Ni deposition, the wafers were annealed at 600°C for 30s to form $Ni(Si_{1-x}Ge_x)$. The unreacted Ni on the insulator SiO_2 surface was etched in H_2SO_4+H_2O_2 (1:1).

Shown in Figure V-11 is the junction leakage as a function of the germanosilicide area. About 20 diodes were measured for each contact size. All three diodes had the same active area of 600 μm x 600 μm. Comparison of the leakage current data in Figure V-11

and Figure V-8 reveals that formation of the germanosilicide contact caused the leakage current to increase by several orders of magnitude. It can also be seen that the leakage current increases with the contact area verifying that the leakage current is indeed caused by the germanosilicide contact.

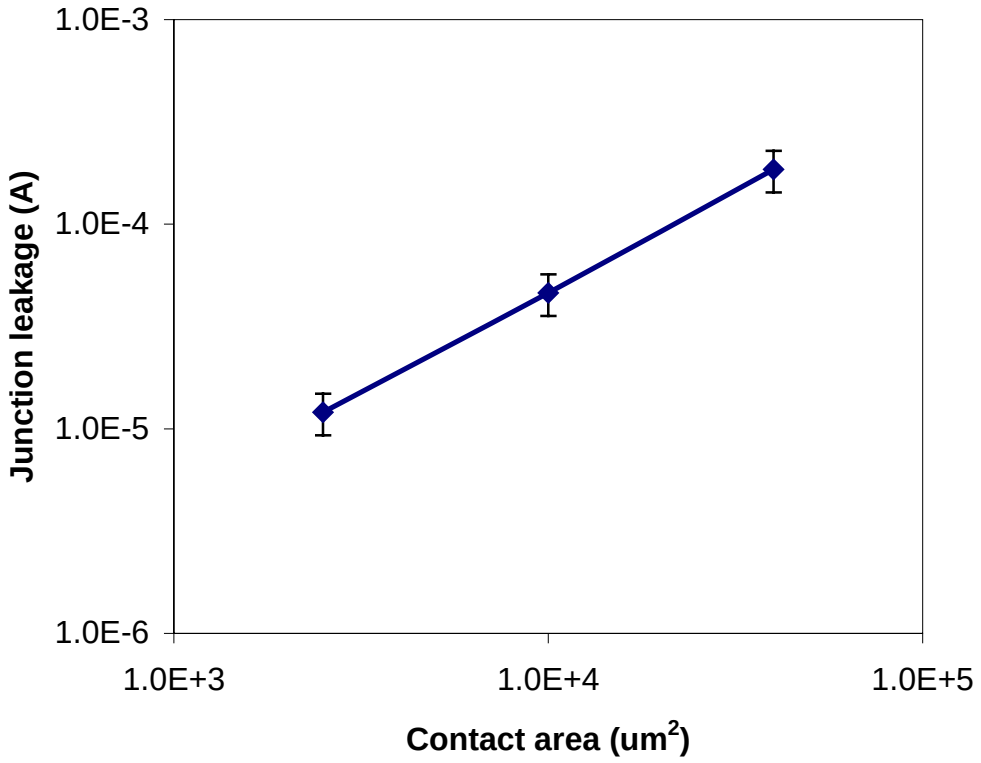


Figure V-11 Gated diodes with $Ni(Si_{1-x}Ge_x)$ contacts formed at 600°C. The junction leakage current is plotted as a function of the contact area. The dependence of leakage current on contact area indicates a rough $Ni(Si_{1-x}Ge_x)/Si_{1-x}Ge_x$ interface.

To understand this behavior, we have employed atomic force microscopy (AFM) to study the morphology of the $Ni(Si_{1-x}Ge_x)/Si_{1-x}Ge_x$ interface. The analysis was carried out after complete removal of the $Ni(Si_{1-x}Ge_x)$ layer in 10% HF at room temperature, which does not etch the underlying $Si_{1-x}Ge_x$ layer. The resulting micrographs are shown in Figure V-12. As shown in Figure V-12, the roughness of the interface increases with the annealing temperature. The interface becomes excessively rough when the annealing temperature is 600°C or higher. With such a rough interface, the possibility of $Ni(Si_{1-x}Ge_x)$ spikes penetrating through the $Si_{1-x}Ge_x$ layer into the Si substrate is very high.

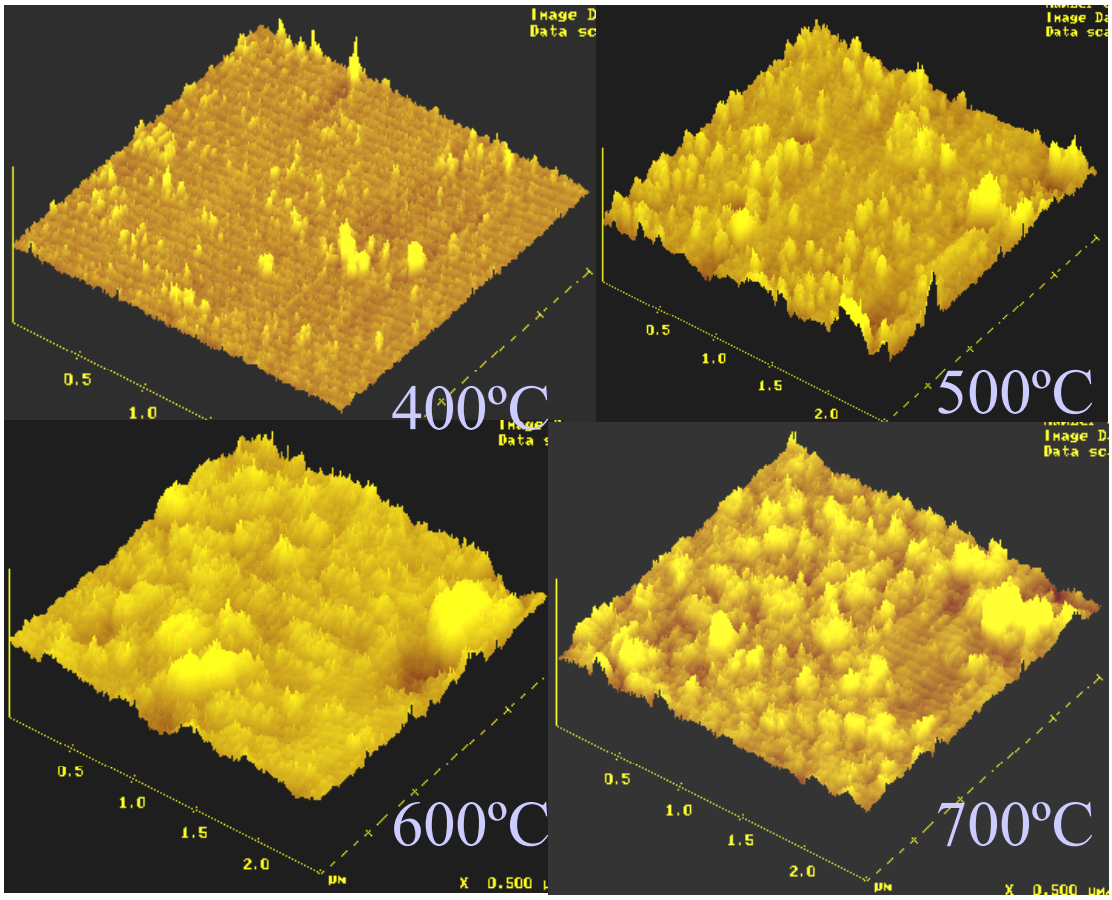


Figure V-12 The interface of $Ni(Si_{1-x}Ge_x)/Si_{1-x}Ge_x$ was exposed by removing the $Ni(Si_{1-x}Ge_x)$ films with HF. The images of $Ni(Si_{1-x}Ge_x)/Si_{1-x}Ge_x$ interface formed at 400°C, 500°C, 600°C and 700°C were obtained by AFM. The roughness of the interface increases with the annealing temperature.

Shown in Figure V-13 is the RMS roughness of the interface plotted as a function of the germanosilicide formation temperature. The measurements were obtained from the AFM micrographs shown in Figure V-12, It can be seen that the roughness is increasing linearly with the formation temperature, which was also observed for germanosilicides formed on boron doped $Si_{1-x}Ge_x$ [6]. With the Ge segregation, the Si atoms from the substrate will move up to react with Ni. Also, Ni is the diffusion species during the solid phase reactions. Therefore, Ni can diffuse via the vacancies left by Si atoms and the diffusion of Ni through the $Si_{1-x}Ge_x$ layer is enhanced, which leads to the formation of Ni germanosilicide spikes.

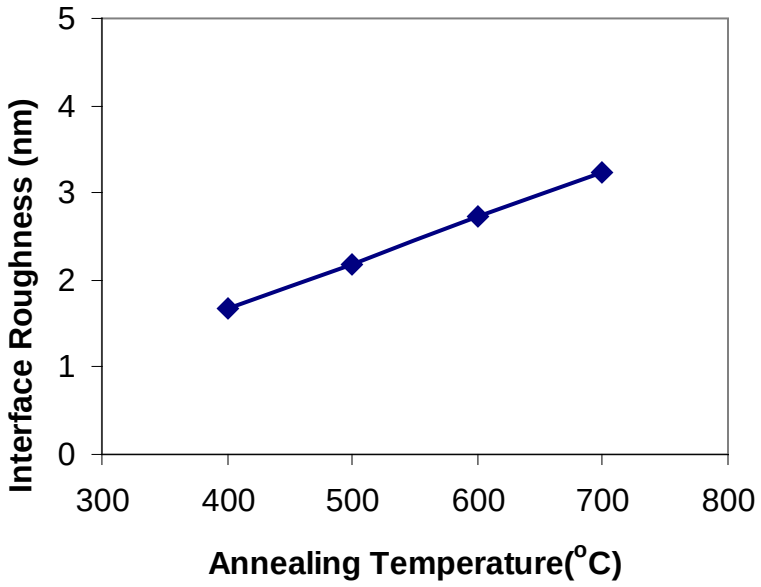


Figure V-13 Ni germanosilicide/$Si_{1-x}Ge_x$ interface roughness as a function of annealing temperature. The Ni($Si_{1-x}Ge_x$) film on the surface was removed by diluted HF solution.

The interface roughening was also studied using secondary ion mass spectroscopy (SIMS). Shown in Figure V-14 are Ni profiles obtained from samples with germanosilicides formed at different temperatures. The analysis was carried out using an O_2^+ ion beam since O_2^+ is more sensitive to Ni atoms than Cs^+. The lighter weight of O_2^+ can also improve the depth resolution. A Ge profile is also included in the figure to show the approximate location of the $Si_{1-x}Ge_x$/Si interface. We note that the Ni profiles for 400°C and 500°C are very similar and fairly abrupt. On the other hand at 600°C and 700°C the Ni profiles are much broader suggestive of a rougher interface. In fact the Ni profiles extend beyond the $Si_{1-x}Ge_x$/Si interface indicative of potential shorts. In conclusion, the SIMS profiles suggest that the germanosilicide formation temperature should not exceed 500ºC. Jing Liu showed that this temperature was already too high for his junctions, which contained 50% Ge in the $Si_{1-x}Ge_x$ layers [6].

V.2.4 Junction Leakage with Nickel Germanosilicide Contacts Formed with a Pt Interlayer

The junction leakage was studied for germanosilicide formed using different Ni and Pt percentages on 100nm $Si_{1-x}Ge_x$ film. The Pt percentages were 10%, 25%, 50%, 75% and 100%. The diode active and contact areas were 600 x 600 μm^2 and 100 x 100 μm^2 respectively. Twenty diodes were measured on each wafer. The junction leakage was measured at a reverse bias voltage of 1.0 V. The gate bias was –2.0 V. Shown in Figure V-15 is the leakage data obtained for germanosilicides formed at 450ºC. As shown, except the pure Pt case, all Ni/Pt contacts exhibit excellent reverse leakage behavior with a nominal leakage current of ~ 10^{-11} A.

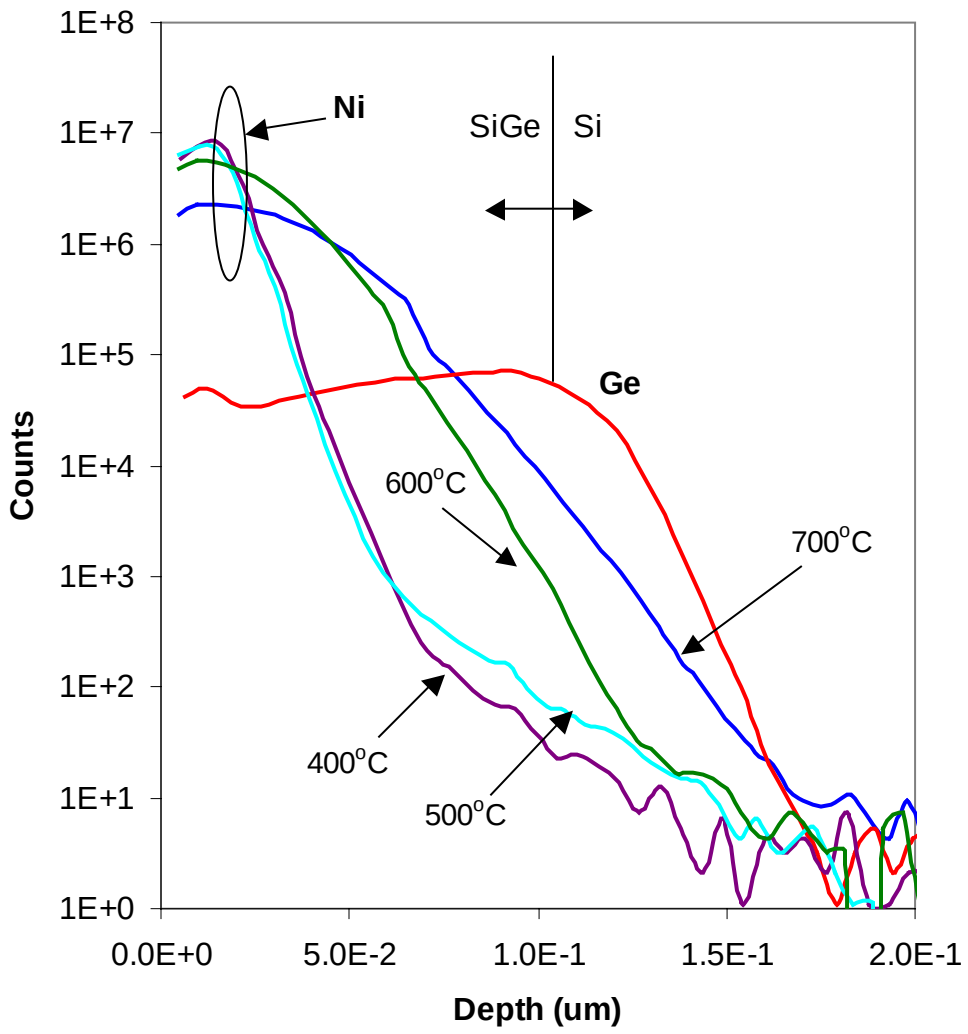


Figure V-14 Ni depth profiles after $Ni(Si_{1-x}Ge_x)$ is formed at different annealing temperatures. The samples were analyzed with SIMS.

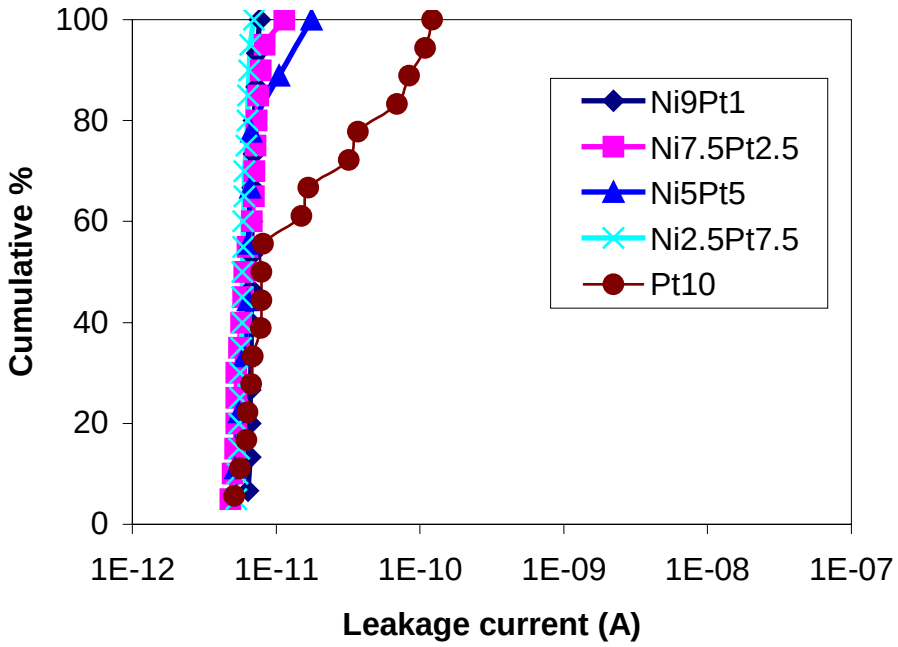


Figure V-15 Junction leakage obtained using germanosilicide contacts with various Ni/Pt ratios. The samples were annealed at 450°C for 30s. The gated diodes were measured at a reverse bias of 1.0 V. The contact area was 100 x 100 μm^2.

Shown in Figure V-16 is the leakage current data obtained with germanosilicide contacts formed at 550ºC. As shown, with the exception of the 9 nm Ni and 1 nm Pt case the junctions exhibit large failure percentages indicative of a poor interface. This result appears to contradict the sheet resistance data, which suggests that the thermal stability is improved with a Pt interlayer.

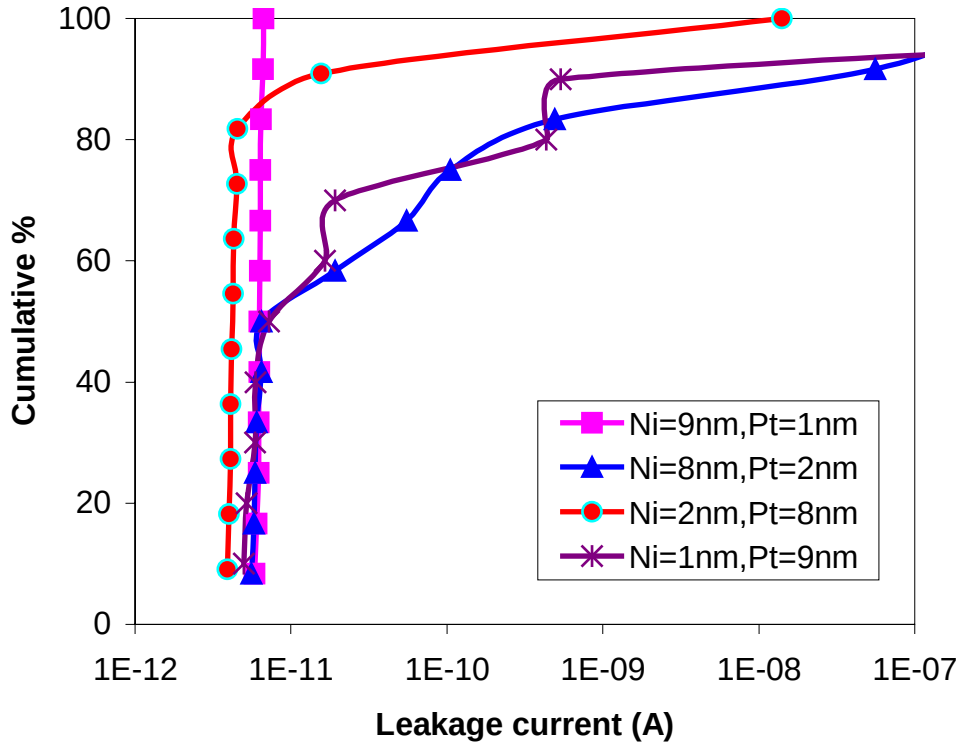


Figure V-16 Junction leakage current of Ni/Pt contacts with various Ni/Pt ratios on $Si_{1-x}Ge_x$ junction. The samples were annealed at 550°C for 30s. The gated diodes were measured with reversed bias of 1.0 v. The contact area was 100 x 100 μm^2.

Using the best Ni/Pt ratio of 9 to 1, germanosilicide contacts were formed at four different temperatures of 450°C, 500°C, 550°C and 600°C. The RTA time was fixed at 30s. The measurement results are shown in Figure V-17. It can be seen that for the temperatures of 450, 500°C and 550°C, the junction leakage is around 10 pA independent of the contact area. On the other hand, when the germanosilicide formation temperature is raised to 600°C, the leakage current increases by approximately fours orders of magnitude suggestive of excessive germanosilicide induced leakage. It is interesting to note however that this leakage is still much less than the leakage obtained at this

temperature without the Pt interlayer (Figure V-11). These results suggest that the Pt layer does improve the interface between the germanosilicide and the underlying $Si_{1-x}Ge_x$ layer. However, the leakage current increases with the Pt percentage, which seems to contradict the sheet resistance data.

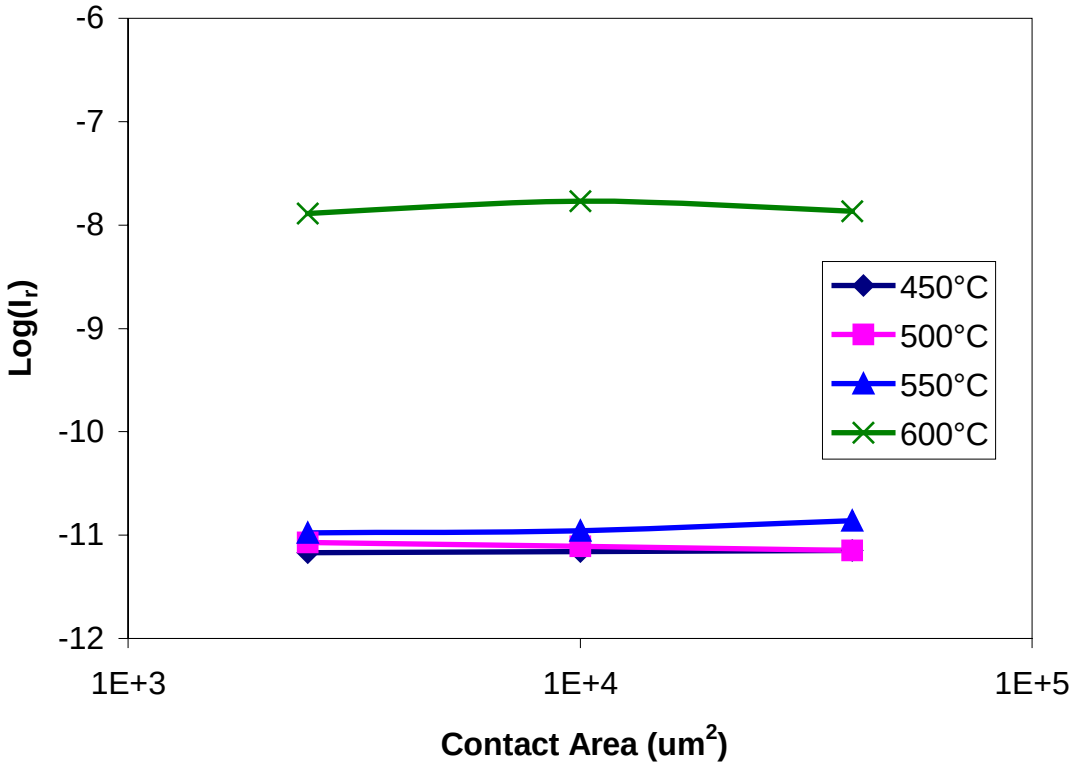


Figure V-17 Junction leakage current Ir of gated diodes with germanosilicide contacts formed using Ni(9nm)/Pt(1nm) at 450, 500, 550 and 600°C. The leakage currents were measured from junctions with the same active area but different contact areas.

V.3 Contact resistance of germanosilicides

The contact resistivity of germanosilicide contacts formed on heavily phosphorus doped $Si_{1-x}Ge_x$ was measured using the four-terminal Kelvin structure shown in Figure V-18. The contact resistance obtained from this structure can be expressed as [7]

$$R_k = R_c + R_{geom} = \frac{\rho_c}{L^2} + \frac{4R_s\delta^2}{3W_xW_y}\left[1 + \frac{\delta}{2(W_x - \delta)}\right] \quad (4)$$

where R_c is the 'real' contact resistance and R_{geom} is the geometrical resistance. The contact resistance is determined by the contact resistivity, ρ_c, the sheet resistance of the $Si_{1-x}Ge_x$ layer, R_s and the geometrical parameters, L, δ, W_x and W_y illustrated in Figure V-18.

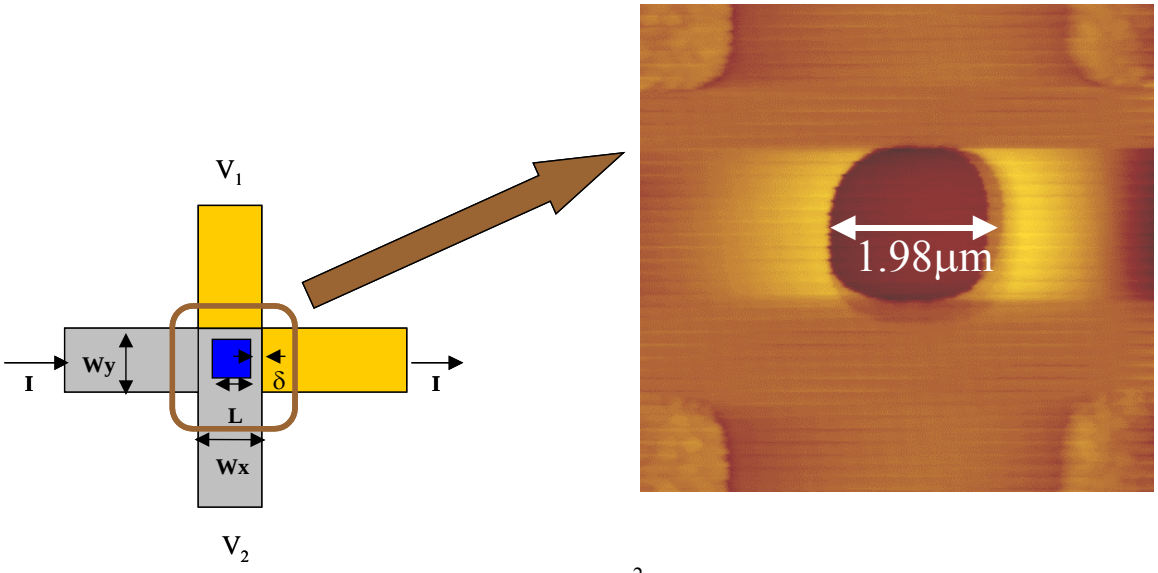


Figure V-18 The actual size of 1.5 x 1.5 μm^2 contact hole of Kelvin structure. The image was scanned with AFM. The actual contact size is larger than the printed size.

If the lateral dimensions of the Kelvin structure and the sheet resistance of the $Si_{1-x}Ge_x$ film are known, the contact resistivity ρc can be calculated from equation (4). However, resulting ρc is a strong function of L, which must be measured for accuracy. In this study, Kelvin structures with four different contact widths of 0.5, 0.7, 1 and 1.5 μm were used. The data points were plotted against the contact area and compared to equation (4) plotted for known contact resistivities.

Four-terminal Kelvin structures were fabricated with a total starting metal thickness of 10 nm. Both Pt and Ni were considered as the first deposited metal on $Si_{1-x}Ge_x$. Figure V-19 shows the contact resistance obtained with Ni/Pt germanosilicide contacts. Solid lines represent calculations based on the two-dimensional model given in equation (4) using three different contact resistivities ranging from 10^{-8} to 10^{-7} ohm-cm^2. The individual data points show the average contact resistance of approximately twenty structures. The thickness of the Pt layer is 10%, 25% and 50% of the total starting metal thickness. In all three cases Pt was the first metal deposited. As shown, all three samples exhibit low contact resistivity values between $1 – 5 \times 10^{-8}$ ohm-cm^2.

The contact resistance obtained with higher Pt percentages is shown in Figure V-20. The contact resistivity is still under 5×10^{-8} ohm-cm^2 with 25 % Ni in the starting metal stack. However, the contact resistivity jumps to 1×10^{-7} ohm-cm^2 when Pt is 80% or more.

The results of the contact resistance measurements on Ni/Pt germanosilicide contacts are summarized in Figure V-21. As shown, when the Pt thickness is more than 80% of the total thickness the contact resistivity jumps to 10^{-7} ohm-cm^2, which is too high for future CMOS technologies.

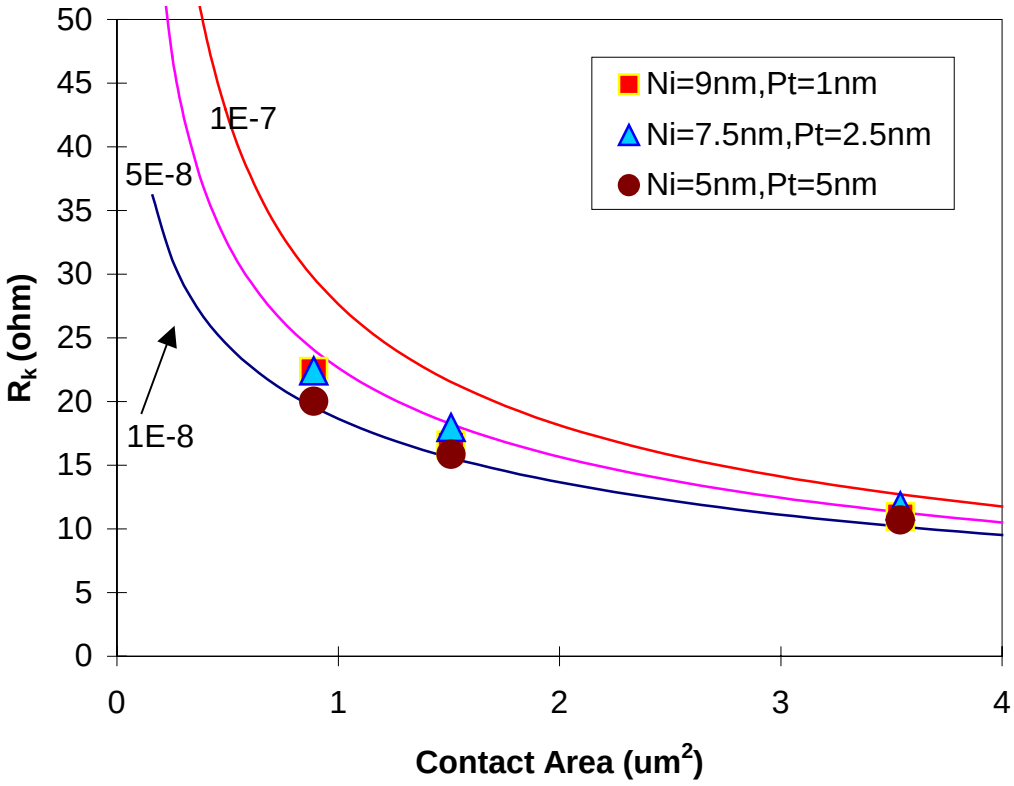


Figure V-19 Contact resistivity estimation using 2-D model for Ni germanosilicides. Ni and Pt interlayers were deposited on 100nm N^+ $Si_{0.8}Ge_{0.2}$. The samples were annealed at 450°C for 30s.

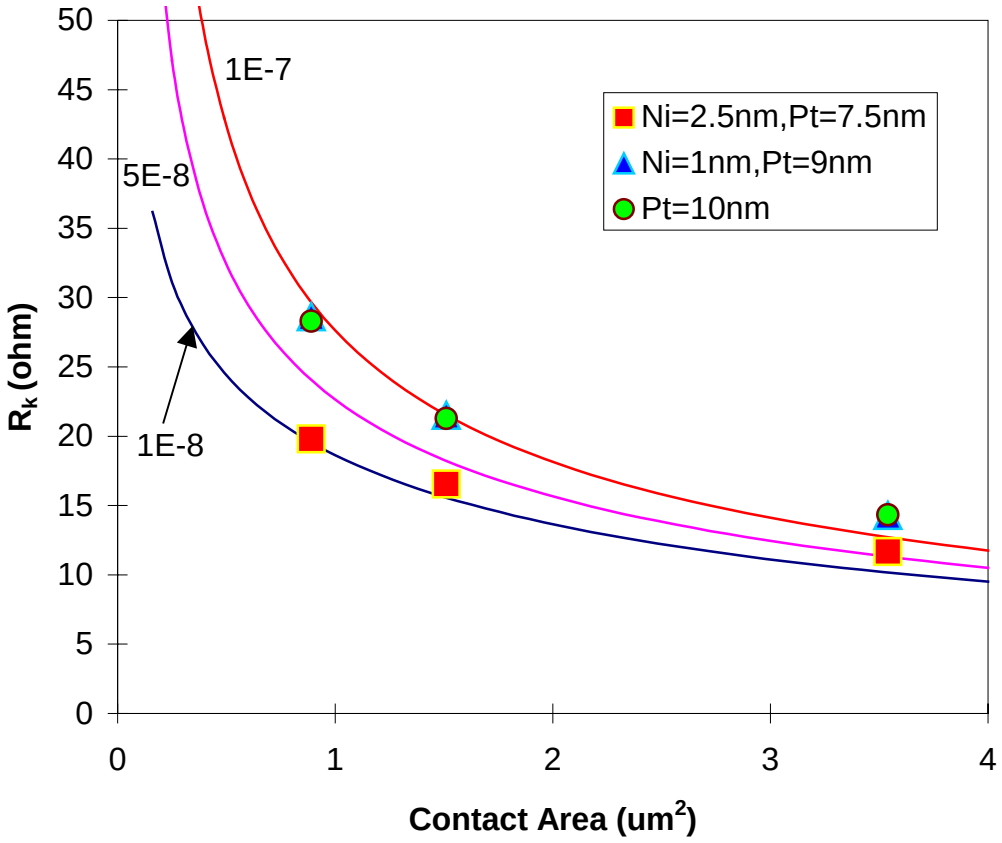


Figure V-20 Contact resistivity estimation using 2-D model for Ni germanosilicides. Ni and Pt interlayers were deposited on 100nm N^+ $Si_{0.8}Ge_{0.2}$. The samples were annealed at 450°C for 30s.

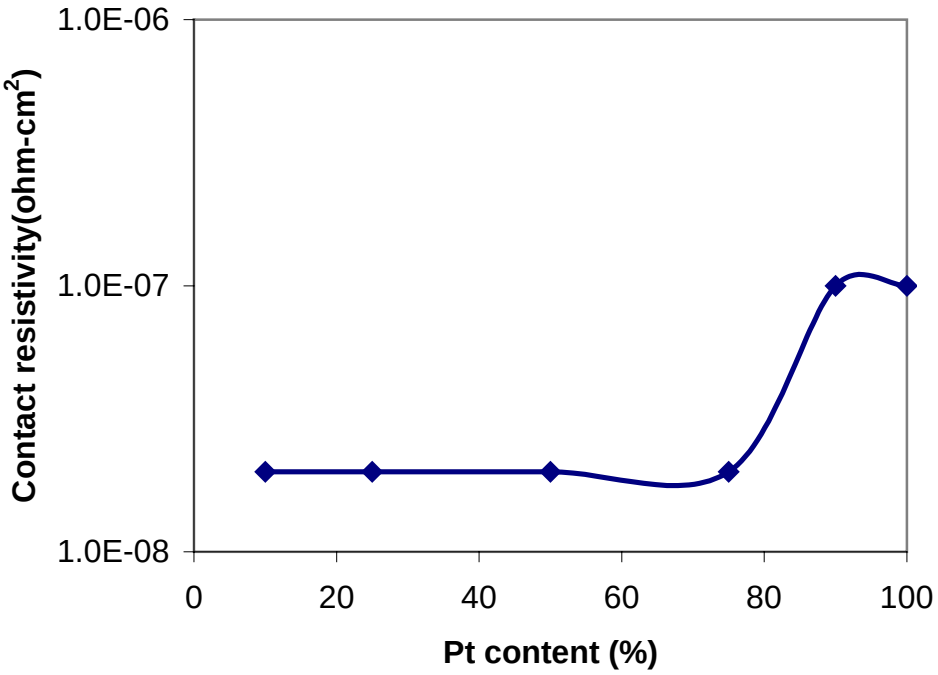


Figure V-21 Contact resistivity of Ni/Pt structures as a function of Pt content. The contact resistivity of Ni/Pt/ N^+ $Si_{0.8}Ge_{0.2}$ structure was measured with Kelvin structure.

The effect of a Zr interlayer on the contact resistance is shown in Figure V-22. The Ni and Zr layer thicknesses are given in the figure insert. The best contact resistivity possible with the structure appears to be around $5x10^{-8}$ ohm-cm^2, which is higher than that obtained using a Pt interlayer.

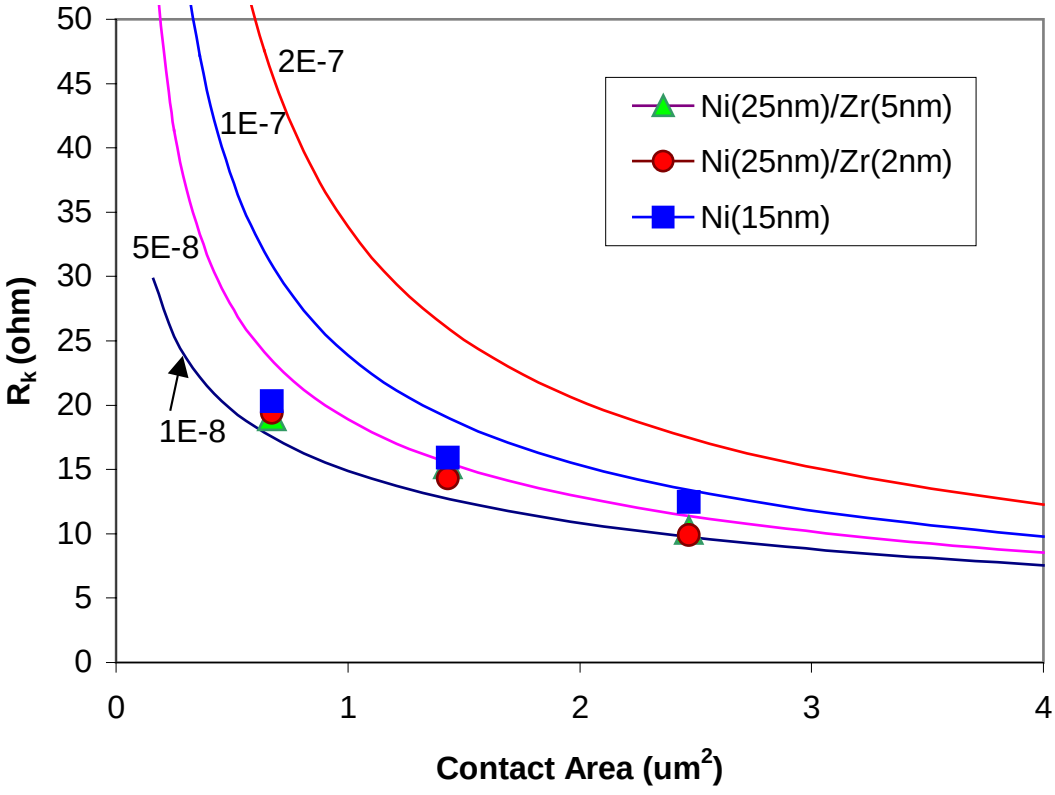


Figure V-22 Contact resistivity estimation using 2-D model for Ni germanosilicides. Ni with or without Zr interlayers was deposited on 100nm N^+ $Si_{0.8}Ge_{0.2}$. The samples were annealed at 600°C for 30s.

Figure V-23 shows the contact resistance obtained with pure Zr germanosilicide contacts. Also shown for comparison is the contact resistance obtained with just Al contacts (with Ti used as a diffusion barrier). The Al and Ti layers were 200 nm and 50 nm thick respectively. The $Zr(Si_{1-x}Ge_x)_2$ was formed at 800°C. The contact resistivity for Al/Ti contacts is about 5 x 10^{-8} ohm-cm^2, which is lower than what the conventional silicide process can deliver.

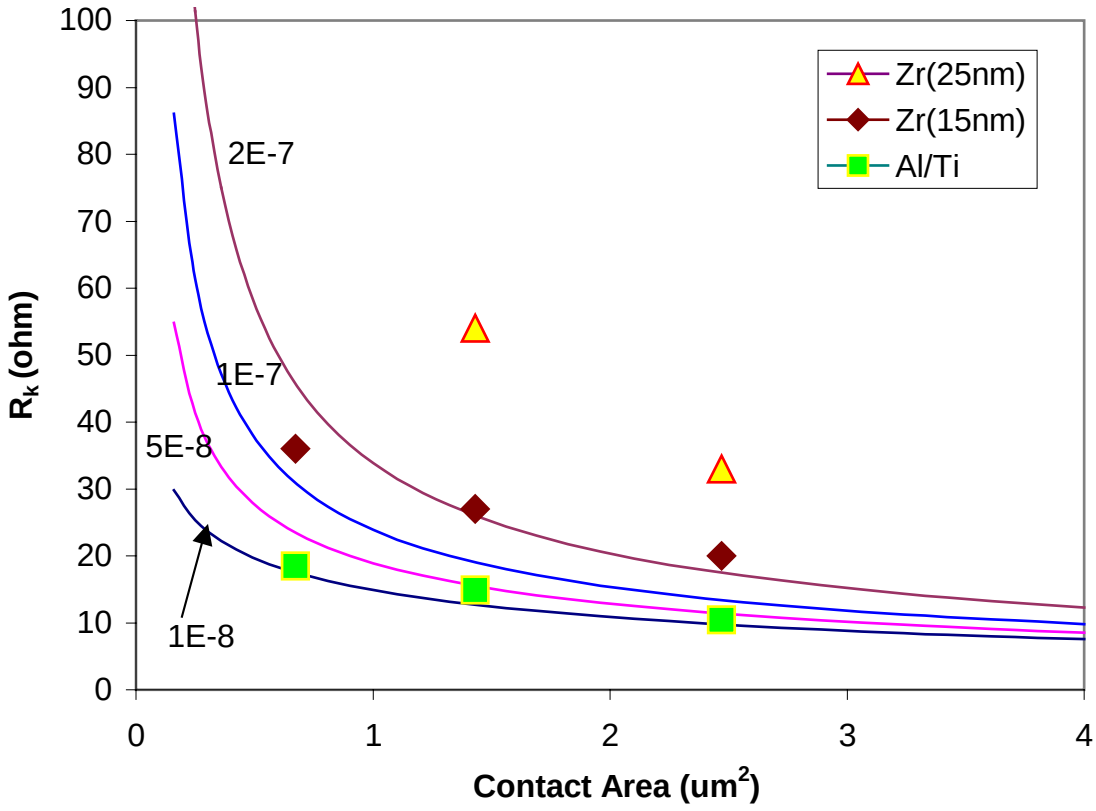


Figure V-23 Contact resistivity estimation using 2-D model for Zr germanosilicides and Al/Ti contacts. Zr films were deposited on 100nm N^+ $Si_{0.8}Ge_{0.2}$. The Zr samples were annealed at 800°C for 30s.

On the other hand, as shown in Figure V-23, the contact resistivity obtained with Zr germanosilicide contacts is considerably higher than the contact resistivity obtained with $NiSi_{1-x}Ge_x$. The reported values for the Schottky barrier heights of $ZrSi_2$ and NiSi contacts to Si are very similar to each other [8]. If we make the assumption that the germanosilicide counterparts will behave similarly, the reason for the high contact resistivity with Zr must come from a different direction. To study the distribution of phosphorus during $Zr(Si_{1-x}Ge_x)_2$ formation, we have analyzed the samples using SIMS. Figure V-24 shows the depth profiles of Zr, Si, Ge and P after forming the germanosilicide at 800 ºC. Uniform distributions of Zr, Si and Ge throughout the germanosilicide can be observed. The rapid drop in Si and Ge concentrations near the surface is suggestive of the presence of an unreacted Zr layer. It appears that there is a distinct P segregation peak at the metal/germanosilicide interface, which may be substantial. It is also possible that Zr may form stable compounds with P similar to Ti [8]. We also note that a thicker Zr layer results in higher contact resistivity, which may be due a higher phosphorus loss.

V.4 Factors Determining the Contact Resistance

In this section we consider key factors, which are expected to influence the contact resistance data presented in the previous section.

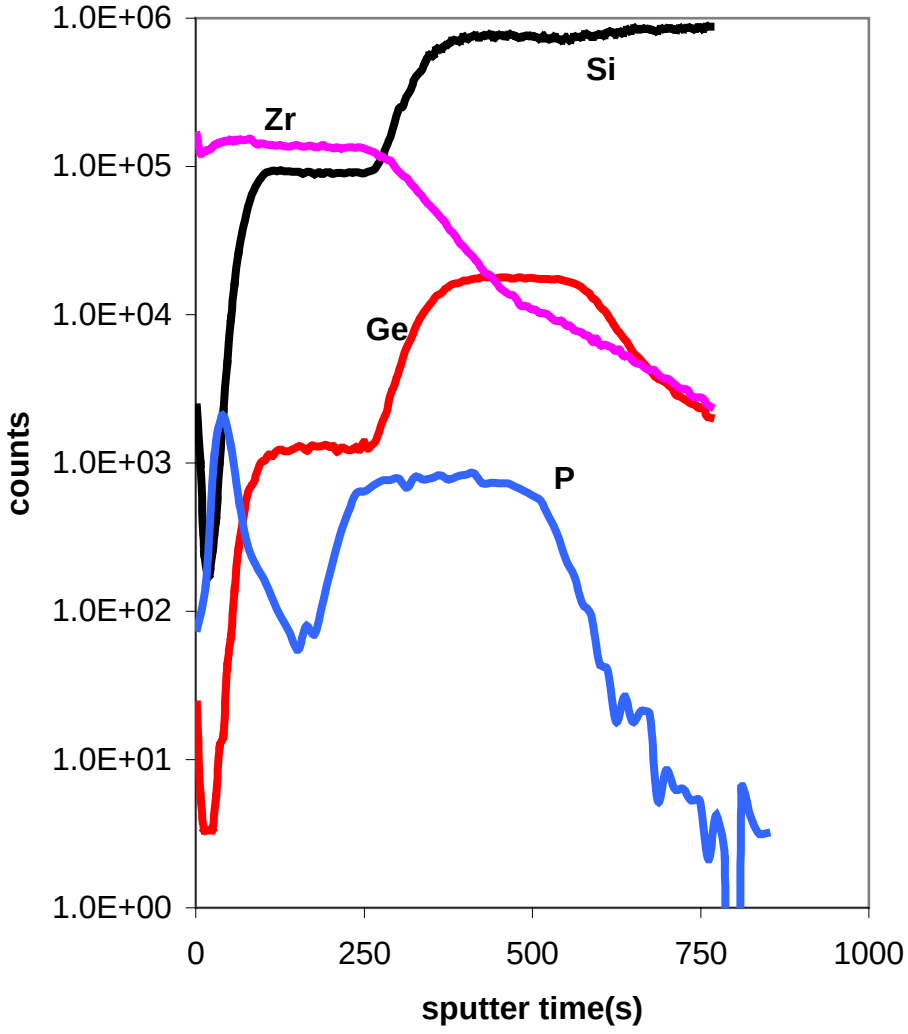


Figure V-24 SIMS profile of Zr(30nm)/ N^+ $Si_{0.8}Ge_{0.2}$ sample after annealing at 800°C for 30s.

V.4.1 Schottky Barrier Height

If the Fermi level in the metal layer is pinned at the semiconductor midgap, then the barrier height is equal to half the semiconductor bandgap. Then, the semiconductor bandgap becomes the key parameter one would hope to minimize to minimize the contact resistance.

One of the concerns with phosphorus doped $Si_{1-x}Ge_x$ layers used in this work was the relatively low Ge concentration of the films. In his work on boron doped $Si_{1-x}Ge_x$ alloys, Jing Liu was able to work with $Si_{1-x}Ge_x$ alloys with a Ge concentration near 50%. Unfortunately, as shown by Inkuk Kang in his Ph.D. dissertation, it is not possible to grow films with Ge concentrations above 30% when the films are heavily doped with phosphorus. The contact resistance measurements presented in the previous section were obtained from $Si_{1-x}Ge_x$ layers with a Ge concentration of ~ 20%.

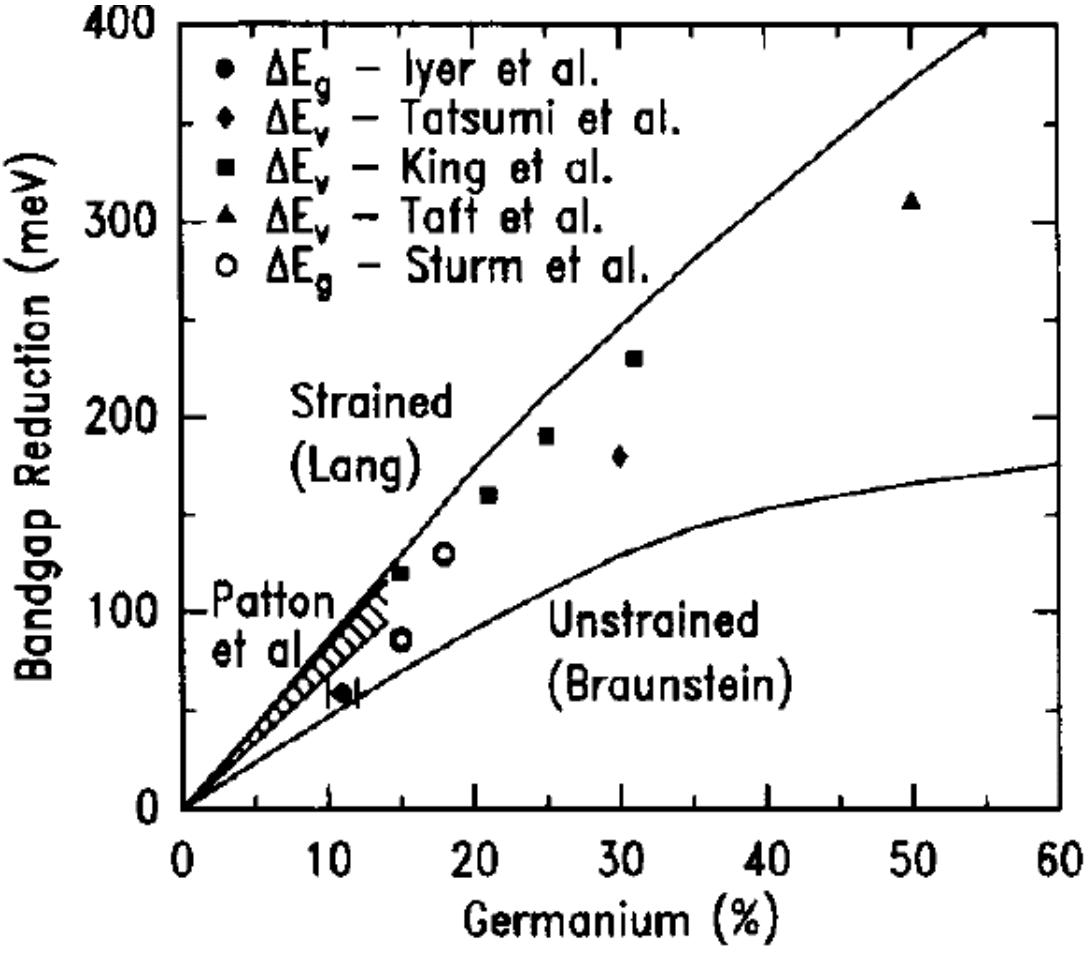


Figure V-25 Band offsets versus Ge composition for $Si_{1-x}Ge_x$ films [9-16].

The $Si_{1-x}Ge_x$ bandgap is determined by the Ge concentration and the amount of strain in the $Si_{1-x}Ge_x$ layer. The strain in turn is determined by the film thickness for a given Ge concentration. Shown in Figure V-25 is the bandgap reduction as a function of the Ge percentage for both strained and unstrained $Si_{1-x}Ge_x$ alloys. As shown, bandgap reduction with ~20% Ge can range from 0.09 to 0.18 eV depending on the amount of strain in the alloy [9], which is determined by the thickness of the alloy relative to the critical thickness for that Ge concentration.

The critical thickness of $Si_{1-x}Ge_x$ layers grown on Si (100) substrates is shown in Figure V-26 [9]. As shown, $Si_{1-x}Ge_x$ layers grown by chemical vapor deposition are expected to have a critical thickness of ~ 100 nm for a Ge concentration of 20%, which is the $Si_{1-x}Ge_x$ thickness used in this study. Furthermore, formation of the germanosilicide consumes a portion of the $Si_{1-x}Ge_x$ layer decreasing the thickness to ~ 80 nm. It has also been shown that the relaxation occurs only partially unless the film thickness is considerably larger than the critical thickness [17]. Therefore, it is likely that the films used in this study are strained. This means that a bandgap reduction of almost 0.2 eV can be expected, which is significant since the contact resistivity exhibits an exponential dependence on barrier height.

We have also attempted to measure the barrier height from Schottky barrier height diodes fabricated on lightly doped $Si_{1-x}Ge_x$ films grown on n-type Si substrates. A cross-sectional view of the Schottky diodes fabricated in this study is shown in Figure V-27. The germanosilicides were formed using 30 nm thick Pt or Ni layers and 25 nm Ni with a 2 nm Pt interlayer.

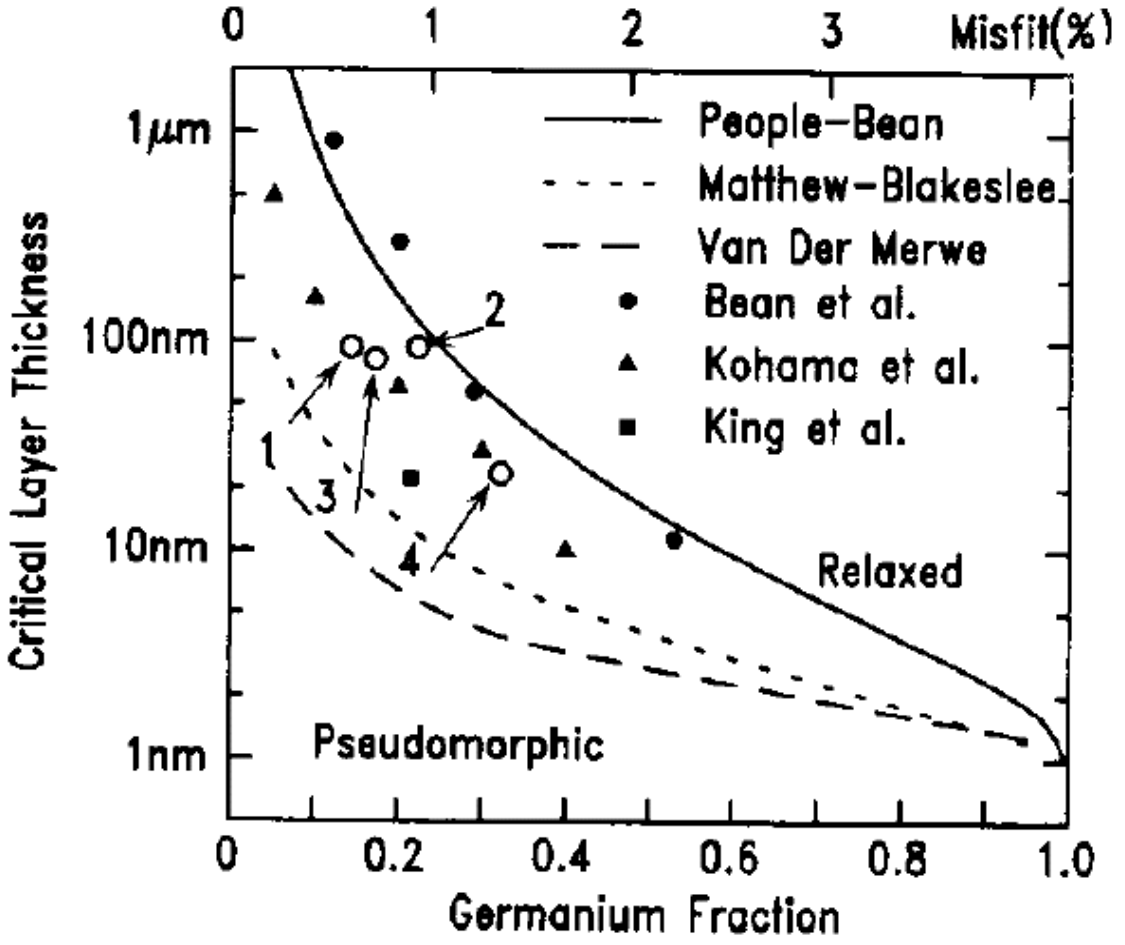


Figure V-26 Critical thickness plotted as a function of Ge content [9, 18-22]. 1 and 2 were grown with MBE. 3 was grown with CVD. 4 was grown with limited reaction processing (LRP)

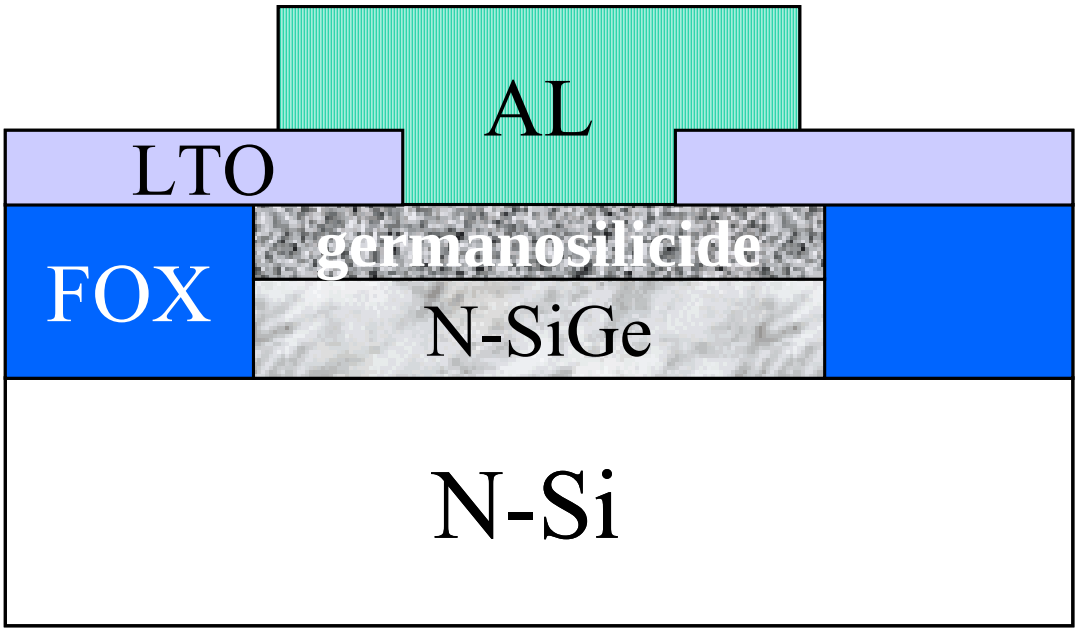


Figure V-27 Cross-sectional view of a germanosilicide/$Si_{1-x}Ge_x$ Schottky barrier diode

The Schottky barrier height was obtained from the I-V characteristic of a forward-biased Schottky diode, which can be expressed as [23]

$$I = I_0\left(e^{q\frac{(V-IRs)}{nkT}} - 1\right) \qquad (5)$$

where n is the ideality factor and R_s is the series resistance. A typical I-V characteristic is shown in Figure V-28, which was obtained from a $PtSi_{1-x}Ge_x/Si_{1-x}Ge_x$ Schottky diode.

From equation (5), we can find:

$$\frac{dI}{dV} = g_D = I\frac{1 - R_s \cdot g_D}{\frac{nkT}{q}} \qquad (6)$$

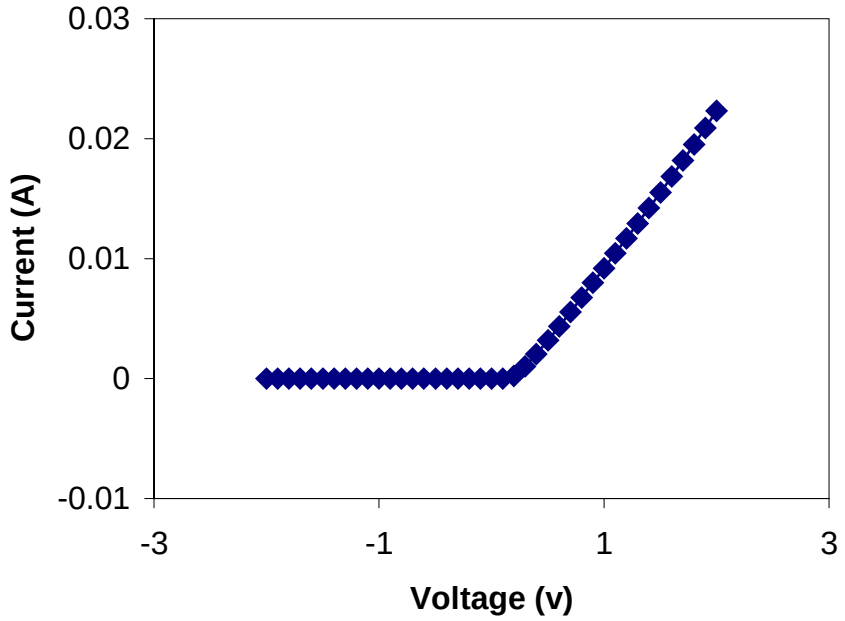


Figure V-28 A typical I-V curve of Pt germanosilicide/$Si_{1-x}Ge_x$ Schottky diode. The junction area is 500 x 500 μm^2.

Equation (6) can be rearranged as:

$$\frac{I}{g_D} = \frac{nkT}{q} + IR_s \qquad (7)$$

A plot of I/g_D versus I gives nkT/q as the intercept and R_s as the slope, as shown in Figure V-29.

Taking the logarithm of both sides of equation (5), we obtain:

$$\ln I + IR_s \frac{q}{nkT} = \ln I_0 + \frac{q}{nkT}V \qquad (8)$$

Plotting the left side of equation (8) as a function of V, $\ln I_0$ can be obtained as the intercept. This plot is shown in Figure V-30 for a $PtSi_{1-x}Ge_x/Si_{1-x}Ge_x$ diode.

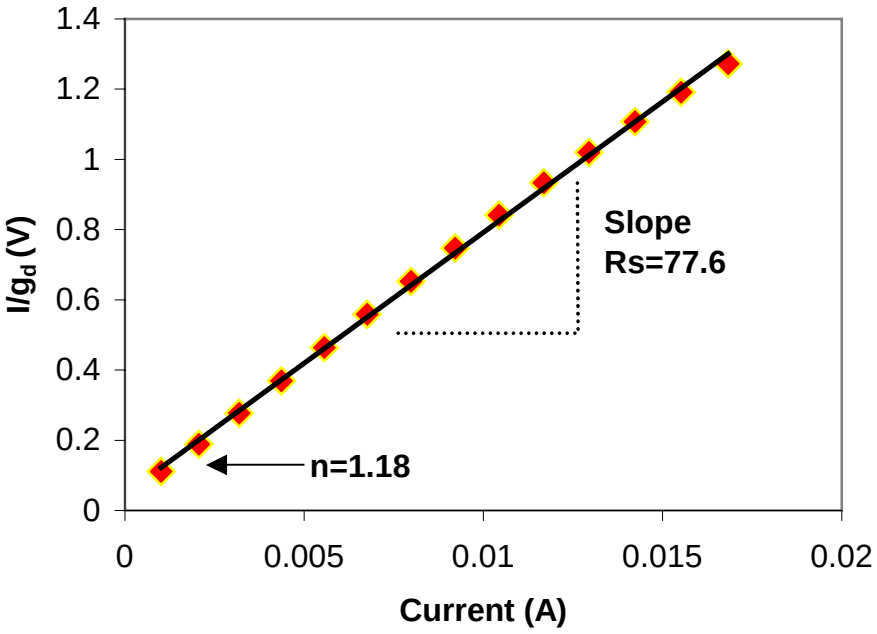


Figure V-29 I/g_D versus I for Pt germanosilicide/$Si_{1-x}Ge_x$ Schottky diode.

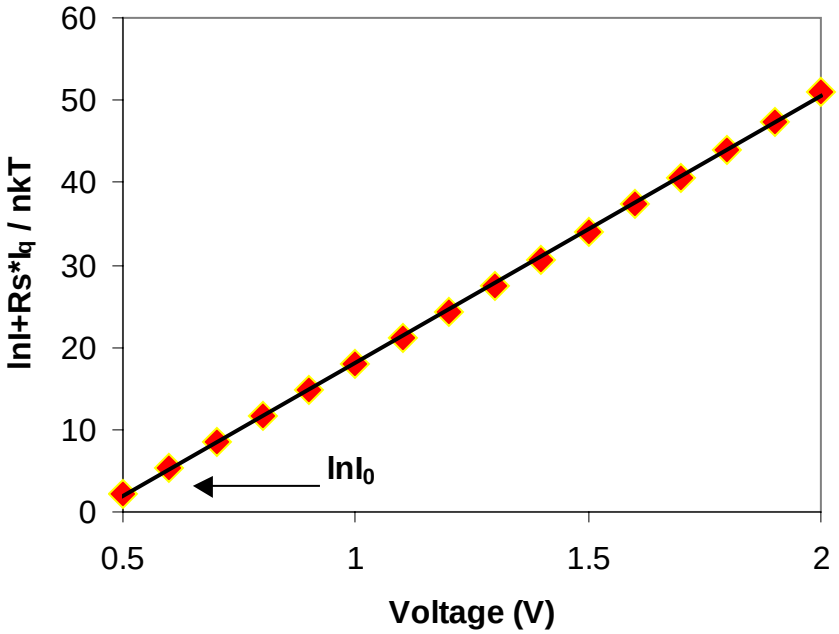


Figure V-30 lnI+ R_s *Iq/nkT versus V for Pt germanosilicide/$Si_{1-x}Ge_x$ Schottky diode.

I_0 is the saturation current given by

$$I_0 = A \cdot A^{**} \cdot T^2 \cdot e^{-\frac{q \cdot \Phi_B}{KT}} \qquad (9)$$

where A** is the effective Richardson constant, which can be obtained from (9) by varying the temperature. The Richardson constant for n type Si and Ge were reported as 112 and 50A/cm^{2}K^2 respectively [24]. Using Vegard's law, we estimate the Richardson constant for $Si_{0.8}Ge_{0.2}$ as 99.6 A/ cm^{2}K^2.

The effective Schottky barrier height Φ_B can be expressed as

$$\Phi_B = \frac{kT}{q}(\ln(A \cdot A^{**}T^2) - \ln I_0) \qquad (10)$$

Φ_B given above is lower than the ideal Schottky barrier height Φ_{B0} due to image force barrier lowering. Using the measured value of I_0 obtained in Figure V-30, Φ_B can be calculated using equation (10).

Using this method, Schottky barrier heights of germanosilicides were obtained. For Pt germanosilicide, Φ_B is determined to be ~ 0.60 eV. For germanosilicides formed with the Ni(25nm)/Pt(2nm) structure, Φ_B is 0.52 eV. The Schottky diode of pure Ni showed no rectification, which could be due to excessive leakage caused by the rough interface. The Schottky barrier height of $Ni(Si_{1-x}Ge_x)$ was found to be 0.48 eV by J. Liu using contacts formed on p-type $Si_{0.5}Ge_{0.5}$ layers and it indicates that the Fermi level locating at the middle of the bandgap [1]. Both of these germanosilicides have lower Schottky barrier height than their silicides. For PtSi, Φ_B is 0.87 eV on n type Si. For NiSi,

it is about 0.7 eV [25]. The Schottky barrier heights of Ni and Pt silicides and germanosilicides are listed in Table V-3.

Table V-3 Schottky barrier height of Ni and Pt silicides and germanosilicides

	NiSi	Ni(SiGe)	PtSi	Pt(SiGe)	Ni/Pt/SiGe (600°C)
Φ_B(eV)	0.7	0.48	0.87	0.6	0.52

The measurement results discussed above indicate that there is a difference of ~ 0.1 eV between the barrier heights obtained with $NiSi_{1-x}Ge_x$ and $PtSi_{1-x}Ge_x$ contacts which may explain the higher contact resistivity obtained with the latter. The fact that the Schottky diodes with $NiSi_{1-x}Ge_x$ contacts were too leaky may suggest an even smaller barrier height than that measured by J. Liu . These results are in agreement with results obtained on boron doped $Si_{1-x}Ge_x$ layers, which showed that the contact resistivity was lowest with $PtSi_{1-x}Ge_x$ contacts. In fact, the work on $PtSi_{1-x}Ge_x$ was terminated only after it was shown in this work that the contact resistivity on phosphorus doped $Si_{1-x}Ge_x$ was too high.

In the $N^+Si_{0.8}Ge_{0.2}$ film, the phosphorous doping level is about 2 x $10^{20}/cm^3$. The band gap narrowing due to heavily doping is about 120 meV for the $N^+Si_{1-x}Ge_x$ film used in this study, as shown in Figure V-31 [26]. If band gap narrowing due to heavily doping is considered, the total value of band gap narrowing should be larger and the actually Schottky barrier height for the germanosilicide/$N^+Si_{1-x}Ge_x$ contact should be even lower.

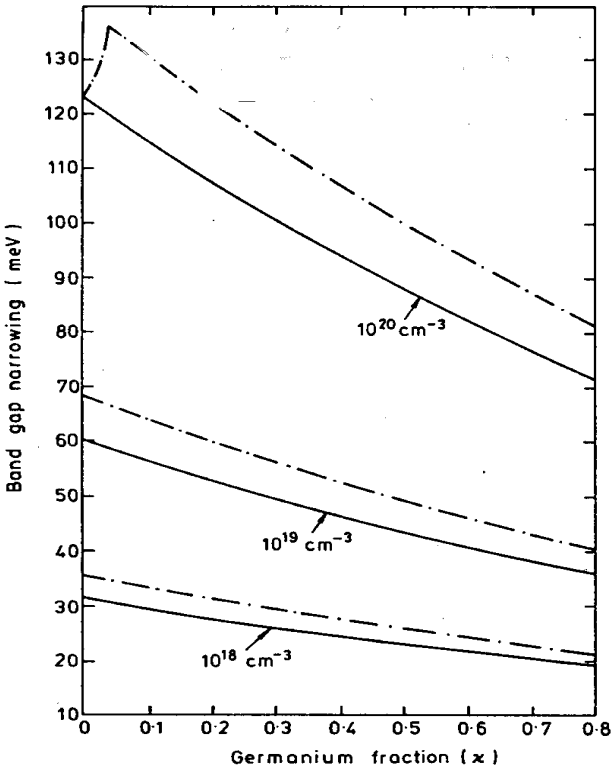


Figure V-31 Band gap narrowing effect (not including the band gap narrowing due to strain splitting) in n type $Si_{1-x}Ge_x$ as a function of Ge content for 3 different doping concentrations. The solid lines show the band gap narrowing on unstrained alloys. The dot-dashed lines show the band gap narrowing on strained layers on Si substrate.

V.4.2 Doping Density Under the Contact

Hall effect measurements indicated an active carrier density of 2 x $10^{20}/cm^3$ in the $Si_{1-x}Ge_x$ layer. However, as shown in Figure II-8, the phosphorous concentration is increasing toward the surface due to phosphorus segregation during growth. Therefore, prior to the solid phase reactions, doping density under the metal is higher than the value predicted by Hall effect measurements.

Figure V-32 shows the depth profiles for Ni, P, Si and Ge obtained by SIMS after forming the $NiSi_{1-x}Ge_x$ contact at 400°C. Cs^+ and O^{2+} are the two ions available for SIMS analysis. Cs^+ is sensitive to phosphorous but not to Ni. O^{2+}, however, is less sensitive to phosphorous than Cs^+. The SIMS profile shown in Figure V-32 was obtained with O^{2+}. The thickness of the Ni layer and the $Si_{1-x}Ge_x$ layer were 10 nm and 100 nm respectively. The profiles have interesting features. First, phosphorus appears to be uniformly distributed in the $Si_{1-x}Ge_x$ layer, which is not the case after depositing the $Si_{1-x}Ge_x$ layer. This may suggest a mechanism that enhances phosphorus diffusion in $Si_{1-x}Ge_x$ during germanosilicide formation. Another interesting feature is that the phosphorus concentration drops sharply in the germanosilicide layer. We also observe phosphorus and germanium peaks at what appears to be the $NiSi_{1-x}Ge_x/Si_{1-x}Ge_x$ interface, which is suggestive of a 'snow plow' effect. This implies that the phosphorus atoms prefer to stay in the $Si_{1-x}Ge_x$ layer instead of diffusing into the germanosilicide, which should then result in a higher phosphorus concentration under the metal contact. It is also interesting to note that Ge pile-up at the interface may further reduce the bandgap.

Shown in Figure V-33 are the depth profiles of from a sample with a $NiSi_{1-x}Ge_x$ layer formed at 600°C for 30s. Similar to Figure V-32, the phosphorus concentration decreases toward the surface where the germanosilicide layer exists. The phosphorus and germanium peaks are no longer observable, however, the spread in the Ni profile is suggestive of interface roughening, which would make delineation of such features rather difficult.

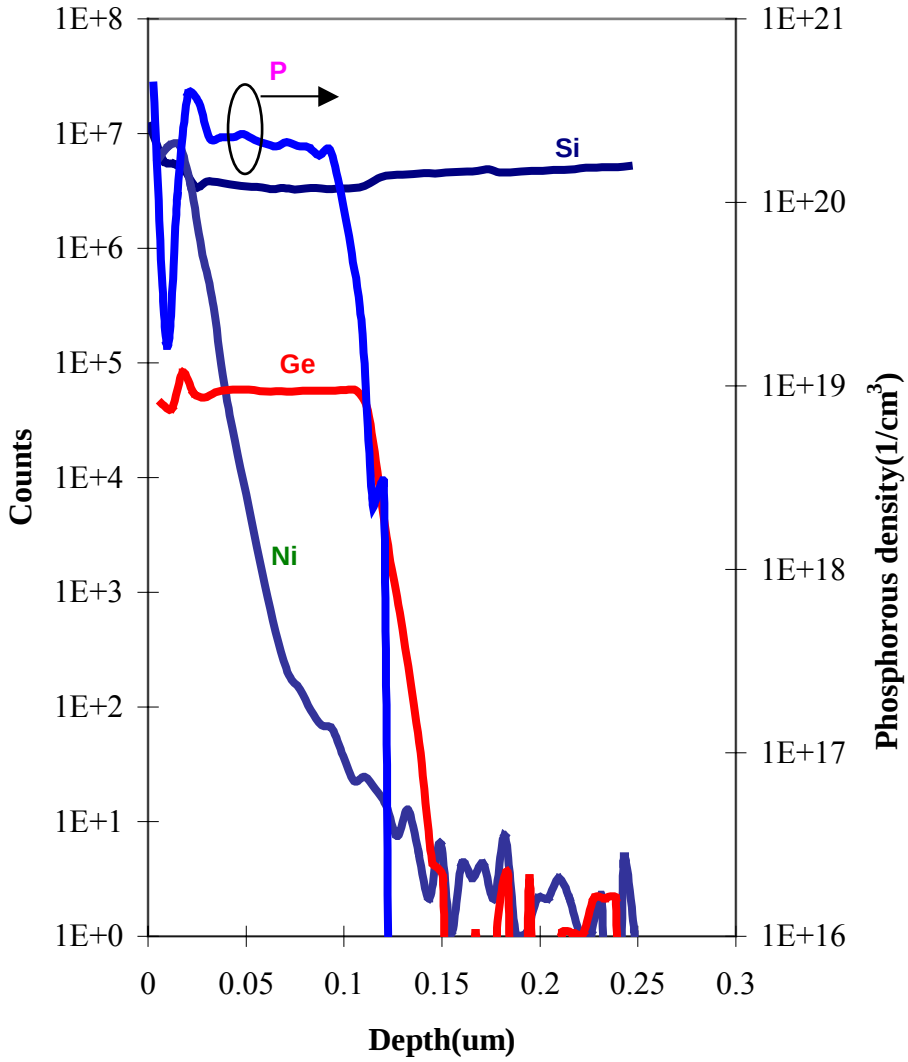


Figure V-32 SIMS depth profile of Ni(10nm)/ $N^{+}Si_{1-x}Ge_{x}$ annealed at 400°C for 30s.

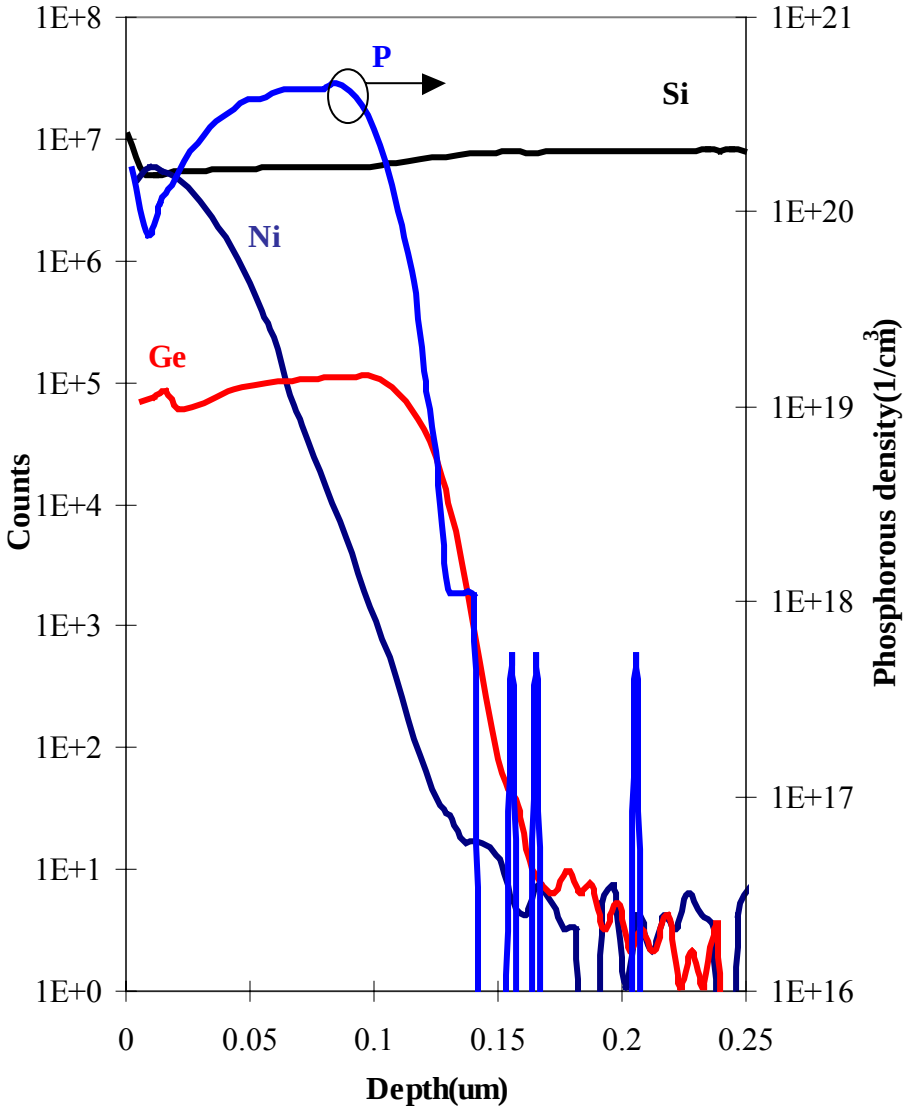


Figure V-33 SIMS depth profile of Ni(10nm) on N^+ $Si_{1-x}Ge_x$ annealed at 600°C, for 30s.

In order to analyze distribution of species more accurately, the analysis was performed on a sample with a thicker germanosilicide layer. Figure V-34 shows the depth profiles obtained from a sample with a germanosilicide layer formed using 25 nm of Ni and 5 nm of Pt. The germanosilicide was formed at 600ºC. The profiles shown in Figure V-34 confirm that the phosphorus atoms are rejected by the germanosilicide, which should effectively increase the phosphorus concentration in the underlying $Si_{1-x}Ge_x$ and result in a lower contact resistivity. It is also clear that the Ge concentration is decreasing toward the surface while the Si concentration is remaining the same. When Ge atoms are rejected from the germanosilicide grains it is possible that some of the Ge atoms are left behind instead of segregating at the grain boundaries. These results suggest that the germanosilicide formation is actually helpful in improving the properties of the underlying $Si_{1-x}Ge_x$ layer.

In Figure V-35, the contact resistivity is plotted as a function of the Schottky barrier height and doping density at the contact interface [14,15]. For conventional silicides, the Schottky barrier heights are between 0.55 – 0.65 eV and the dopant level can be as high as $2 \times 10^{20}/cm^3$, which yields a contact resistivity around 1×10^{-7} ohm-cm^2. In this work, bandgap reduction for ~20% Ge can range from 0.09 to 0.18 eV depending on the amount of strain in the alloy and the bandgap will be between 0.94 to 1.03 eV. If band gap narrowing due to heavily doping is considered, the band gap reduction can be 0.12 eV more. Our result also show that $Ni(Si_{1-x}Ge_x)$ is a middle bandgap material. So Schottky barrier height of Ni germanosilicide can be between 0.41 to 0.52 eV on N^+ $Si_{0.8}Ge_{0.2}$ and the dopant concentration is between $2 – 4 \times 10^{20}/cm^3$. The corresponding contact resistivity ranges are shown for conventional silicide and germanosilicide

contacts. As shown in Figure V-35, it is indeed possible to obtain a contact resistivity near ~ 10^{-8} ohm-cm^2 using germanosilicide contacts on phosphorus doped $Si_{1-x}Ge_x$ layers.

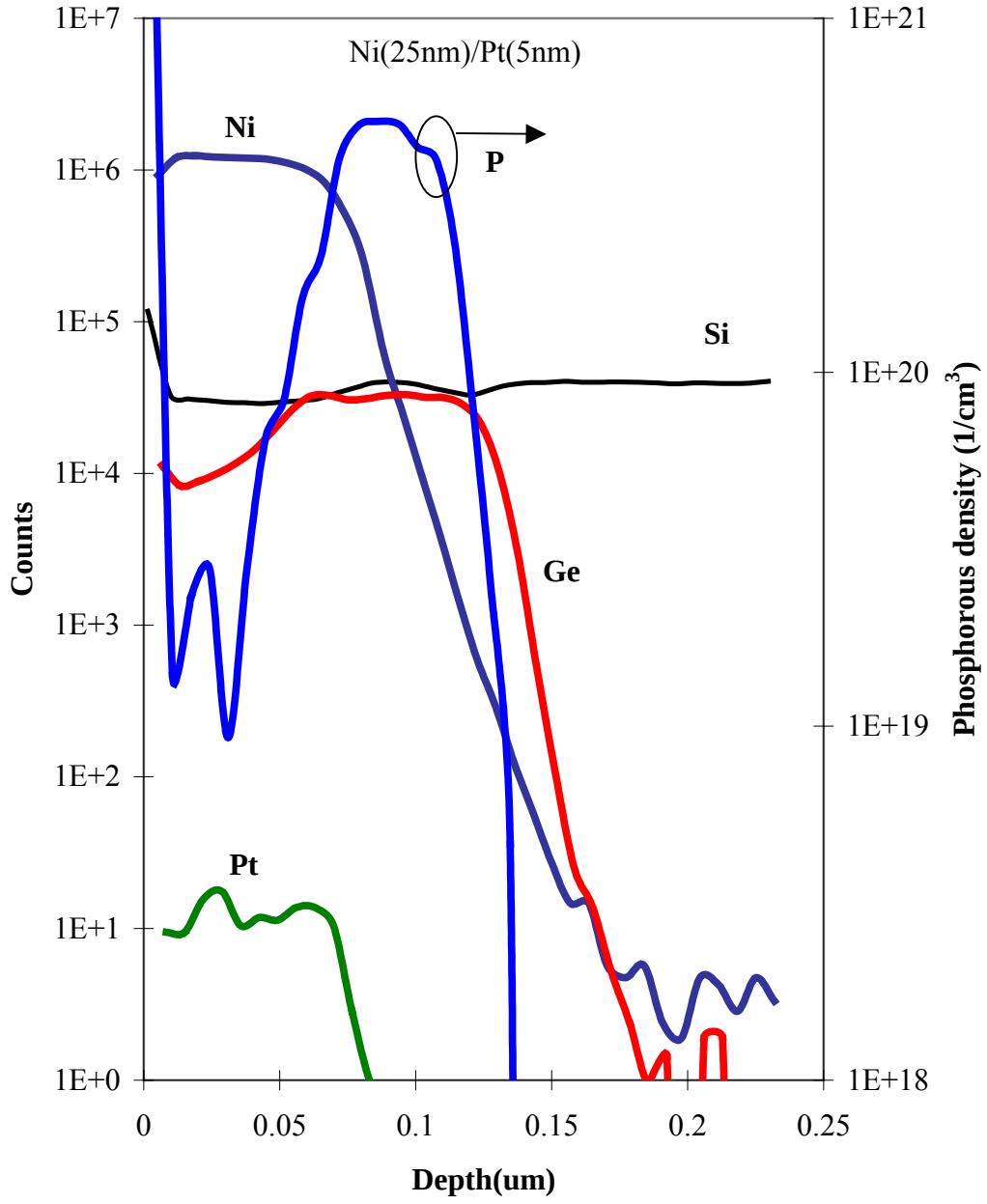


Figure V-34 Depth profiles of P, Ni, Si and Ge after forming a germanosilicide using 25 nm of Ni and 5 nm of Pt at 600ºC.

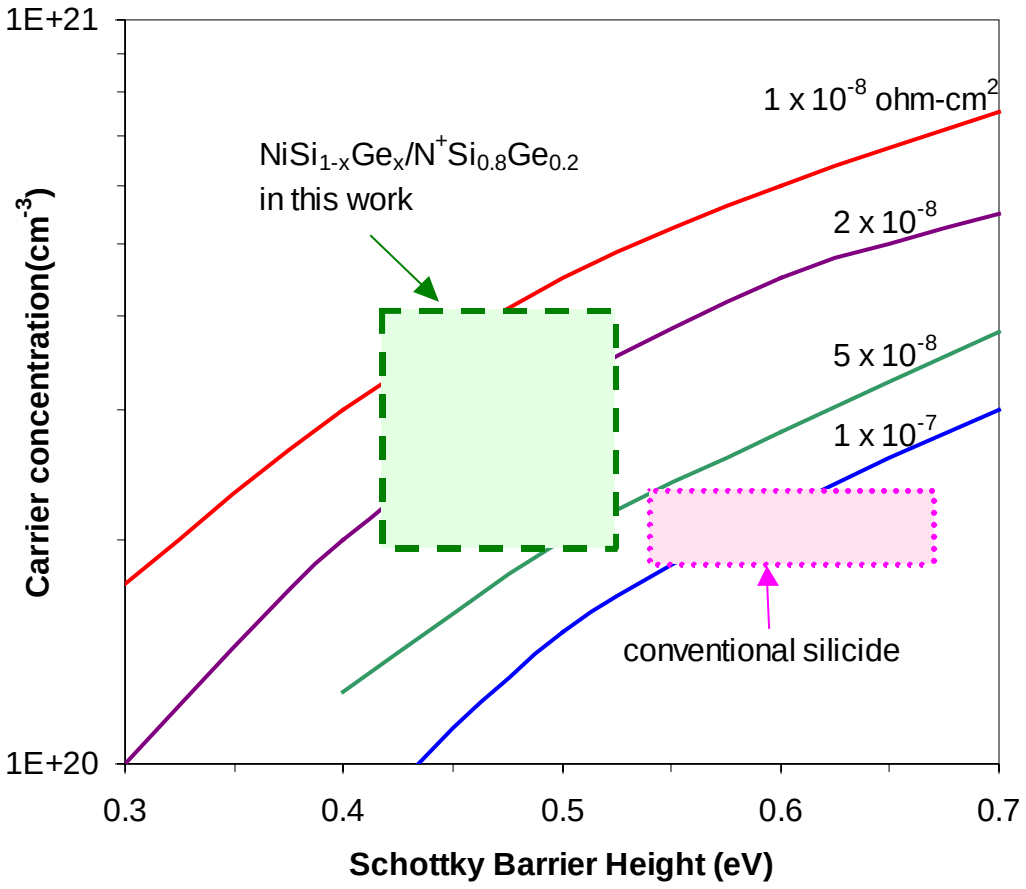


Figure V-35 Dependence of contact resistivity on Schottky barrier and carrier concentration at the interface. The rectangle areas indicate the contact resistivity of $NiSi_{1-x}Ge_x$ contact in this work and conventional silicide process respectively.

V.5 Summary

In this study, selective etch solutions for Ni, Pt and Zr germanosilicides were investigated. It was shown that Aqua Regia ($3HCl+HNO_3+4H_2O$) is an effective solution to form self-aligned Ni, Pt and Ni/Pt germanosilicides. $H_2SO_4+H_2O_2$ is suitable for the formation of Ni and Zr germanosilicides.

Gated diodes were used to measure the junction leakage of n^+-p junctions formed by depositing phosphorus doped $Si_{1-x}Ge_x$ layers on p-type Si substrates. Self-aligned germanosilicide contacts were formed on the junctions using Ni, Pt and Zr. It was shown that $NiSi_{1-x}Ge_x$ contacts resulted in excessive leakage when the formation temperature was 600ºC or higher. This was attributed to interface roughening during the solid phase reactions. It was shown that the germanosilicide induced leakage could be reduced by using a thin Pt interlayer.

Four-terminal Kelvin structures were fabricated to measure the contact resistivity of the germanosilicide/$Si_{1-x}Ge_x$ contacts. It was shown that the contact resistivity obtained with Pt and Zr germanosilicide contacts was 1×10^{-7} or higher. A contact resistivity of near 10^{-8} ohm-cm^2 was obtained using $NiSi_{1-x}Ge_x$ contacts formed with a thin Pt interlayer. For $PtSi_{1-x}Ge_x$ contacts, the high contact resistivity was attributed to the large Schottky barrier height. For $Zr(Si_{1-x}Ge_x)_2$, it was suspected that dopant loss into the germanosilicide was the main culprit.

In Chapter 4, the resistivity of the germanosilicide was also shown to increase with increasing Pt content. Therefore, the Pt content should be limited to the minimum percentage necessary to increase the stability of the germanosilicide contacts. This is a

more critical issue on boron doped $Si_{1-x}Ge_x$ since the Ge percentage is near 50%. Nevertheless, we show in this thesis that even though the Pt interlayer may not be crucial on phosphorus doped $Si_{1-x}Ge_x$ it can be used without increasing the contact resistivity provided the Pt percentage is kept below a threshold of 80%. It was shown in J. Liu's thesis that 20% is sufficient for improved stability of the germanosilicide.

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VI. Conclusions and Future Work

$Si_{1-x}Ge_x$ source/drain technology was proposed earlier to meet the requirements of the CMOS technology notes beyond 70nm. The technology offers abrupt junctions, high boron activation and narrow bandgap to address spreading, contact and extension resistance challenges of future MOS transistors. Furthermore, the technology can be used to form the source/drain junction and their contacts at much lower temperatures than conventional processes.

In this work, self-aligned germanosilicide contacts to heavily phosphorous-doped $Si_{1-x}Ge_x$ films were investigated. The work in this thesis was performed in parallel with research on germanosilicide contacts to boron doped $Si_{1-x}Ge_x$ layers by Jing Liu, who completed his dissertation in May 2003.

After considering a variety of metal candidates, Ni, Pt and Zr were selected as the most promising germanosilicide candidates. Experiments were carried out to study the sheet resistance, thermal stability, dopant distribution and surface and interface morphology of the germanosilicides. Electrical characterization of the contacts was achieved via reverse bias leakage, contact resistivity and Schottky barrier height measurements.

The experimental results showed that nickel germanosilicide ($NiSi_{1-x}Ge_x$) contacts provided the best properties. A contact resistivity of ~ 1 x 10^{-8} ohm-cm^2 was obtained for $NiSi_{1-x}Ge_x$ contacts on phosphorus doped $Si_{1-x}Ge_x$ layers. The contact resistivity obtained with $PtSi_{1-x}Ge_x$ and $Zr(Si_{1-x}Ge_x)_2$ was much higher. For $PtSi_{1-x}Ge_x$ Schottky barrier height

measurements indicated that the barrier height is larger than that of the $NiSi_{1-x}Ge_x$. For $Zr(Si_{1-x}Ge_x)_2$, substantial dopant loss from the $Si_{1-x}Ge_x$ layer was observed. On boron doped $Si_{1-x}Ge_x$ layers, Jing Liu was able to achieve low contact resistivity with both $NiSi_{1-x}Ge_x$ and $PtSi_{1-x}Ge_x$ but not with $Zr(Si_{1-x}Ge_x)_2$. This created a processing challenge since both Pt and Zr germanosilicides appeared to be more stable than $NiSi_{1-x}Ge_x$.

The stability of $Ni(Si_{1-x}Ge_x)$ layers considered in this thesis was significantly better than those considered by Jing Liu due to the fact that the $Si_{1-x}Ge_x$ layers used in this work had a maximum Ge concentration of 30% as opposed to 50% in Jing Liu's work. The experimental results showed that $NiSi_{1-x}Ge_x$ could be formed at temperatures as low as 350°C. While the sheet resistance of the $NiSi_{1-x}Ge_x$ appeared to be stable at least up to 800°C, leakage current measurements and AFM analysis of the $NiSi_{1-x}Ge_x/Si_{1-x}Ge_x$ interface showed that interface roughening begins to occur under 600ºC. On boron doped $Si_{1-x}Ge_x$, the maximum allowable temperature was shown to be less than 450ºC. It was also shown that the thermal stability could be improved by inserting a Pt interlayer between Ni and $Si_{1-x}Ge_x$. This method was also applied to phosphorus doped junctions primarily because it is desirable to form the germanosilicide contacts on boron and phosphorus doped junctions simultaneously. It was shown in this work that the Pt interlayer did not result in undesirable results. With 10% Pt junctions exhibited excellent reverse leakage behavior at 550°C and still a low contact resistivity of 1×10^{-8} ohm-cm^2. A drawback of the Pt interlayer is the resistivity of the germanosilicide, which is probably not as important. The physical mechanism which improves the thermal stability of $NiSi_{1-x}Ge_x$ with a Pt interlayer is not fully understood and requires further studies.

The low contact resistivity of $NiSi_{1-x}Ge_x$ was investigated. The Schottky diodes formed using $NiSi_{1-x}Ge_x$ contacts were quite leaky and could not be used to measure the barrier height. It was speculated that the leaky diode behavior may be the result of a very small barrier height. On the other hand, Schottky diodes fabricated with $PtSi_{1-x}Ge_x$ contacts showed rectifying characteristics with a barrier height of 0.52 eV. Analysis of the phosphorus distribution by secondary ion mass spectroscopy (SIMS) indicated that phosphorus atoms preferred to reside in the $Si_{1-x}Ge_x$ layer instead of the germanosilicide. Since the germanosilicide is formed by consuming the $Si_{1-x}Ge_x$ layer, this behavior results in a higher phosphorus concentration under the contacts. It is also interesting to note that during $Si_{1-x}Ge_x$ growth, phosphorus atoms segregate at the surface resulting in a higher concentration at the surface. Therefore, the non-uniform phosphorus distribution obtained during $Si_{1-x}Ge_x$ growth combined with the push effect of the germanosilicide is expected to result in a higher phosphorus concentration than the average values predicted by Hall Effect measurements.

One of the exciting advantages of $Si_{1-x}Ge_x$ junctions of future MOSFETs is their potential to introduce strain in the channel, leading to enhanced channel mobility. This was recently proposed by INTEL for boron doped $Si_{1-x}Ge_x$ junctions. There are many aspects of this process, which are unknown to the research community. Factors such as channel length, junction depth, Ge concentration determine the channel strain collectively. Dopant density will also have a significant influence when strain compensation is effective [1]. Another variable in this process is the impact of the germanosilicide on the channel strain, which may be profound considering the proximity of the contacts to the transistor channel.

VI.1 References

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