# ABSTRACT

LEE, JAEHOON. **Optimization of Gate Electrode Stack for Work Function Tuning**. (Under the direction of Veena Misra.)

This dissertation has focused on fabrication and characterization of gate electrode stacks containing high-k dielectrics and metal gates. This dissertation has focused on the research on the interactions between metal and high-k dielectrics and also explores a plausible scheme of integration for work function tuning of dual-metal-gate CMOS devices. Here are some important conclusions achieved in the past years.

In chapter 2, compatibility of dual metal gate electrodes such as Ru, Ru-Ta alloy, TaN and TaSiN on low EOT single layer $HfO_2$ and stacked $HfO_2/SiO_2$ gate dielectrics for CMOS were investigated and found that the work function of metal gates on $HfO_2$ and $SiO_2$ are similar. In addition, TaSiN resulted in the lowest EOT owing to its excellent oxygen diffusion properties out of all the gates. Although Fermi level pinning was not observed, the charges in the $HfO_2$ layer must be reduced to obtain the desired threshold voltages. Front and backside SIMS suggests that Ru does not suffer from diffusion problems through $HfO_2$ dielectrics at 1000$^{o}$C.

In chapter 3, the effect of the capping layer on the top of the gate electrodes was explored. Different thickness of Ru with the capping layer of the tungsten was used. The observed lower $V_{FB}$ for the capped Ru stack can be attributed to diffusion of oxygen between capped and uncapped films. The uncapped Ru and thick W capping samples suffered from peeling after 1000$^{o}$C anneal. AES depth profiling shows that significant amount of the oxygen or tungsten can diffuse into Ru films.

In chapter 4, integration of bi-layered metals with good modulation of the work function for the gate electrodes for P-MOSFET and N-MOSFET devices on the $SiO_2$ dielectrics was developed. Vertical stacks of Ru and Ta layers were subjected to high temperature anneals to promote intermixing which resulted in work function tuning. The Ru gates with the over-layer of Ta have excellent EOT stability at high temperatures. However, Ta underlayers are unstable on dielectrics, and Ru underlayers resulted in limited work function tuning. To increase work function change, stacks of $Ru_{50}Ta_{50}$/Ru were also evaluated and higher amount of change in work function was observed between $Ru_{50}Ta_{50}$/Ru and $Ru_{50}Ta_{50}$ electrodes. For $Ru_{50}Ta_{50}$ underlayers with Ru overlayers, nearly ~0.8eV shift in work function is observed as compared to the single $Ru_{50}Ta_{50}$ layer making this an attractive approach for bulk CMOS.

In chapter 5, Ru and $Ru_{50}Ta_{50}$ alloy vertically layered gate electrodes on the high-k dielectrics were investigated for work function tuning and ease in integration. It was found that $Ru_{50}Ta_{50}$/Ru stacks provided more than 1.0eV increase in work function compared to $Ru_{50}Ta_{50}$. The work function range of these alloys also provides ease in integration. Hence this approach will be advantageous for gate electrode formation on high-k dielectrics. Even though a larger shift was obtained with $HfO_2/SiO_2$, this cannot be attributed to a larger degree of intermixing than on the $SiO_2$ since other issues such as charges, reactions may have additional effects.

# Optimization of Gate Electrode Stack for Work Function Tuning

By

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## *Biography*

JaeHoon Lee received the B. S. and M. S. degree in Materials Engineering from Hanyang University, Seoul, Korea in 1990 and 1994 respectively. Form 1994 to 2001, he was with Memory R & D division of Samsung Electronic Co. as a research staff and senior research staff. He worked on the process integration for 0.13 um SRAM/LOGIC and SRAM/NVM technology. Other research projects included the characterization, parameter extraction, and cell layout for SRAM devices. Since 2001, he has been pursuing Ph. D. degree in the Department of Electrical and Computer Engineering at North Carolina State University. Under the guidance of Dr. Veena Misra, he has developed a greater understanding of microelectronics devices and advanced technology. He have developed and optimized metal gate electrode stack for work function tuning for CMOS application. His current research interests are process integration and device realization of high K gate dielectrics and metal gate electrodes for advanced CMOS process.

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# *Chapter 1 Introduction*

## 1.1 The scaling of MOSFET devices

Throughout the integrated circuit technology development over the past forty years, complementary metal-oxide-semiconductor field-effect transistor (CMOSFET) device technology has been the dominant very-large-scale-integrated (VLSI) technology. The scaling rules for CMOS device were originally predicted by Gordon Moore in 1965, and since then it has been the driving force for the improvement of speed and shrinkage of chip area of integrated circuits [1]. MOSFET device dimensions continue to be aggressively scaled to satisfy the high demand for improving circuit performance with decreased power and increased integration density [2].

Continuation of scaling rules will eventually reach fundamental limits of both materials and devices currently being used in CMOS devices. To keep up with these International Technology Roadmap for Semiconductors projections, (ITRS), innovative materials, device concepts and alternate process techniques will become increasingly important to overcome a number of issues associated with continued MOSFET scaling [3,4]. The reduction of gate oxide thickness is necessary to maintain device scaling, including threshold voltage and capacitance. An equivalent gate oxide thickness (EOT) of less than 1 nm is needed for high performance devices in 2006 ITRS [3]. However, it appears that the fundamental limit of the CMOS process will be reached in the near future and quantum mechanical effects need to be considered. As device size decreases, gate leakage current increases rapidly due to direct tunneling. In addition, gate control reduces and poly-silicon boron penetration effect into the channel becomes significant for PMOSFETs [5]. Since

$SiO_2$ and poly-silicon materials face fundamental issues for scaled devices, alternative materials are necessary to continue scaling. To achieve low EOT, and stable gate electrode characteristics, both high dielectric constant (k) oxides and metal gate electrodes have considered necessary for advanced devices. The issues of high-κ dielectrics and metal gates will be discussed in detail in the following sections [6-8].

## 1.2 Alternative High Dielectric Constant Gate Insulator

Silicon oxide ($SiO_2$) grown by high temperature oxidation has been used as a gate dielectric because of its several advantages which include having an electrically stable Si-$SiO_2$ interface, attaining good thickness controllability, having a high dielectric breakdown strength , good reliability and thermal stability (remaining in amorphous state after the integration processes) [9].

The gate capacitance *Cox* is expressed as,

$$C_{ox} = \frac{\varepsilon_0 k}{T_{phys}} \qquad (1)$$

where, $\varepsilon_o$ is the vacuum permittivity (= $8.85\times10^{-12}$ F/m), $k$ is dielectric constant (=3.9, dielectric constant of $SiO_2$), and $T_{phys}$ is the physical thickness of the oxide. A larger *Cox* can be achieved by reducing $T_{phys}$ and/or by increasing the $k$ of the dielectric.

As transistor channel length shortens, gate area and gate oxide thickness are scaled to maintain gate threshold voltages and capacitance, which is proportional to the gate area and dielectric constant while inversely proportional to the gate oxide thickness. Most of the short channel effects can be made less severe by having an electrically thinner gate oxide,

thereby increasing the gate oxide capacitance and increasing the gate control of the channel. Aggressively scaled oxides are necessary to achieve higher gate capacitance to attain better gate control of the channel and thereby suppress short-channel effects [2]. However, as gate oxide has scaled down to 1.5nm regime, $SiO_2$ has reached its limitations due to high gate currents. The significant increase in leakage current for these thin oxides is due to direct tunneling and severely degrades the circuit performance e.g., standby power and reliability [10]. In addition, quantum mechanical effects and the polysilicon depletion effect, which are amplified as the $SiO_2$ thickness is reduced, can result in an increase in the equivalent oxide thickness (EOT) [11, 12]. To decrease the leakage current while maintaining an appropriate capacitance, $SiO_2$ can be replaced with dielectrics with higher dielectric constant (high-k dielectric). Since high k dielectrics are physically thicker they reduce the probability of carrier tunneling and hence reduce the leakage current. If high k dielectrics are to replace $SiO_2$ as gate dielectrics, the permittivity must be balanced with the band offset, which directly impacts the barrier height for tunneling. High barrier heights greater than 1V are necessary for both electrons and holes relative to Si greater. According to a report [4], band offset less than 1.0 eV may lead to an unacceptably large leakage current. This problem is a major concern since barrier heights tend to decrease with increasing dielectric constant [13].

As discussed above, alternative high-k dielectrics must have reasonable energy gaps (>4eV) and low leakage currents (no trap-assisted tunneling or other defects degrading dielectric reliability). However, high-k oxide systems researched so far have unstable interfaces with Si thus resulting in an interfacial layer that is formed between the Si and the high-k dielectric which greatly impacts device properties. Most high-k materials have shown fixed charge density exceeding $10^{12}$ charges/$cm^{-2}$ at the interface, which is higher than

the desired values [13 - 16]. Low interface state densities (Dit) and low fixed charges, low bulk dielectric charges, minimal capacitance-voltage hysteresis effects, high process immunity to hot carrier effects and non-crystalline film morphology are all characteristics that need to be obtained from any high-K dielectric layer under consideration. Furthermore, these alternate dielectrics should also be compatible with top gate electrodes and existing CMOS processing sequences for cost and throughput considerations [17, 18]. High-k materials can be classified as four groups on the basis of dielectric constant.

Ultra high-*k* dielectric materials such as $BaSrTiO_3$ and $SrTiO_3$ can produce very high gate capacitances however they suffer from very small band gaps [19]. It is worth mentioning in addition that ultra- high-k dielectrics do not seem to be appropriate for use in MOSFETs since the high dielectric constant can cause field induced barrier lowering (FIBL) which can further degrade short channel effects [20]. Other higher-k materials, such as $Ta_2O_5$ and $TiO_2$, not only have low barrier heights but their interaction with poly-silicon or metal gate electrodes at high temperature is of large concern [21, 22].

Most of these high-K materials are also more efficient diffusers of oxygen than $SiO_2$, and therefore post-deposition annealing in an oxidizing ambient can easily cause the formation of interfacial layers which degrade the total gate capacitance [29]. Dielectrics such as $Al_2O_3$, $CeO_2$, and $Y_2O_3$ do not provide significant advantages over $SiO_2$ or $Si_3N_4$ because they have relatively low dielectric constants [30-33].

A variety of mid-range high-*k* materials have been reported as possible candidates for MOS gate dielectrics. These include dielectrics such as $La_2O_3$, $HfO_2$ and $ZrO_2$, which have all been proven to be thermodynamically stable on silicon. However, as discussed above, these materials are good diffusers of oxygen resulting in the formation of interfacial layers

upon high temperature annealing [34]. Another group of dielectrics that have been considered as strong potential candidates involve silicates namely, $HfSi_xO_y$, $SrTaO_6$, $ZrSiO_4$ and $ZrSi_xO_y$. These multi-elemental oxides are compatible with silicon substrate and are thus stable on it.

$ZrO_2$ and $HfO_2$ emerged as promising high-*k* dielectrics for ultra-thin gate dielectric application almost at the same time and it was reported that both films have promising characteristics such as low leakage current, good interface properties (Dit ~$10^{11}$/eV-$cm^2$), and excellent reliability properties [35-39]. However, during the past several years, hafnium based metal oxides and silicates have received significant attention as the most promising candidates for alternative high-k dielectric applications due to high dielectric constant, large barrier offsets, and thermal, chemical stability with polysilicon gates. In addition, an ultra thin $HfO_2$ gate dielectric with an effective oxide thickness of 0.9 nm was obtained. ***Lee et al***. reported that their $HfO_2$ film maintained its high quality after a high temperature boron dopant activation (950ºC for 30seconds) and also showed very good leakage current behavior (0.23 mA/$cm^2$ at Vg = 1 V) [40-43]. Hafnium silicates, with a dielectric constant around 11, are also being pursued as gate dielectric candidates for the 45 nm gate length CMOS technology [42].

Even though many research efforts have aggressively studied and solved several issues associated with the high-K dielectric, there are still many challenges for the process and integration of high k dielectrics. High temperature properties and interfacial layers between high k material and Si are currently the main issues for developing a high k based MOSFET. High k dielectrics have a fundamental limit for scaling EOT, since an interfacial layer can form even during the deposition of the high k resulting in a $SiO_2$ interfacial layer

attributed to the well-known fast diffusion of oxygen through high k dielectrics. Once oxygen from the ambient, and even from oxygen vacancies introduced in the dielectric itself, diffuses through metal oxides, it reacts with the Si substrate at the interface to form an uncontrolled interfacial layer. It was reported that the electrical contribution from the interfacial layer is around 5Å EOT, although a significant level of interface states are observed in the C-V curves at low frequencies [38]. It has been reported that nitrogen based materials and nitrogen annealing have shown the decrease of the interfacial layer [44-47]. An Additional issue to consider is that $HfO_2$ tends to crystallize even at low temperatures resulting in polycrystalline films which can contain high leakage paths along grain boundaries. The correlation between gate dielectric morphology and device performance requires further investigation prior to the use of high k dielectrics with polycrystalline films. Since junction activation is performed at a high temperature in conventional CMOS processing and there are many advantages to follow conventional CMOS flow, thermal stability is the one of the main requirements for high-κ dielectrics. The structure of high-κ dielectrics can be modified during high temperature processes, thereby resulting in a crystalline material and worse leakage behavior.

Mobility degradation is also a significant issue surrounding high k devices, especially in NMOS devices. It has been reported that the high permittivity of materials can result in the presence of large soft optical phonons which provide long-range scattering of electrons in the Si inversion layer and thus reduce the electron mobility can by as much as a factor of 3. Remote charge scattering can be another limiting factor of the carrier mobility in high k devices [48, 49].

There have been many ongoing research efforts to improve the quality of the interface between the high-k dielectric and silicon, or the region just below the interface. Interface states can act as minority carrier traps that are crucial to the MOS device operation. None of high-k dielectrics has been set as the most likely candidate to meet all of the requirements associated with processing, device performance and reliability. Major breakthroughs are very much needed to meet ITRS predictions.

## 1.3 Alternative Gate Electrode

Polycrystalline silicon has been used as a gate electrode in MOSFET devices for the last several decades. However, there are problems facing the present polysilicon gate technology for submicron CMOS technology due to aggressive scaling [50]. When the gate stack is biased in inversion, a polysilicon depletion layer is formed at the polysilicon/gate oxide interface and this depletion region is added to the total oxide thickness which can decrease the gate capacitance and consequently both the drive current and the transconductance [51]. Furthermore, as the gate dielectric is made thinner, the capacitance associated with the depleted layer at the poly-Si/gate dielectric interface becomes significant.

The increased sheet resistance of the polysilicon gate is another issue then limits the MOSFET circuit speed. Increasing the doping level of polysilicon may reduce the depletion capacitance and sheet resistance but the limit of polysilicon doping is $10^{21}$ $cm^{-3}$ which may not be enough to recover the capacitance. As scaling of MOS devices continues further, boron penetration into the gate dielectric can also occur, and may lead to adverse effects on the device's threshold voltage. Furthermore, it has been reported that Fermi level pinning problems occur when polysilicon gate electrodes are deposited on high k dielectrics.

Replacing polysilicon gate electrodes with metal gates is required to eliminate these problems [52, 53].

Candidates for new metallic gates have many requirements which include appropriate work functions, good thermal/chemical interface stability with underlying dielectric and high carrier concentration and process compatibility with current and future CMOS. A desirable metal gate should have an appropriate work function for NMOS or PMOS devices. This implies a work function of ~4eV for NMOS devices and ~5eV for PMOS devices. Dual metal gates or midgap metal gate electrodes can be used in CMOS processing however with a more complex process integration scenario. Midgap work function metal gates, which are being considered due to their ease of integration, will most likely not be suitable for scaled bulk CMOS devices due to a high resulting threshold voltage which cannot be reduced simply by lowering the substrate doping since the channel doping will then become too low to control short-channel effects. For this reason, two different gate metals are required with work functions near the conduction and valence band edges of Si [54]. It should also have good thermal stability with the underlying dielectric, signifying that the choice of high k dielectric is vital from a metal processing standpoint. In addition, a low diffusivity to oxygen and other dopants of the metal gate is necessary. Furthermore, candidate metals should have high carrier concentration so that gate depletion effects are negligible.

Much investigation is ongoing concerning alternative metal gate electrodes including elemental, nitrides, silicides, and alloys [55-58]. Metal gate electrodes have been successfully incorporated into the CMOS process and owing to their high carrier concentration they have not show any signs of gate depletion. It has been reported that

metal films have carrier concentration above $10^{22}cm^{-3}$ [59], which is significantly higher than the heaviest doped poly-Si films.

There are several NMOS candidate metals with work functions near 4eV such as Al, Ta, Mo, Zr, Hf, V and Ti and several PMOS candidate metals with work functions near 5eV such as Co, Pd, Ni, Re, Ir, Ru and Pt. There are also several conducting metal oxides such as $RuO_2$, $IrO_2$, ZnO, $MoO_2$, $ReO_2$, $In_2O_3$, $SnO_2$, $OsO_2$, and conducting metal nitrides such as TiNx, MoNx, WNx, TaNx, TaSixNy. Usually, work function of the conducting metal oxide is greater than that of the corresponding metal because of the Fermi level change.

Recently, it was reported that reactions between polysilicon gated and a metal gated electrode with the underlying dielectric may result in Fermi level pinning and further the threshold voltage shift in MOSFET devices. Fermi level pinning occurs when states at the interface are charged and cause a dipole which drives the band alignment to change so that a zero dipole will exist. This tends to shift the Fermi level towards the charge neutrality level and hence pinning of the Fermi level occurs at the interface. For Hf-based dielectrics, the interfacial Si-Hf bonds are believed to be the main mechanism creating dipoles. This dipole pins the Fermi level just below the poly-Si conduction band and thus increases the threshold voltage for both NMOS and PMOS devices [60].

## 1.4 High and Low Work Function Metal Gate Electrodes on Gate Dielectrics

For the next generation devices, dual metals are expected to replace poly-silicon in order to achieve low threshold voltages and thus high performance, i.e., high work function (Fermi level near the silicon valence band edge) for PMOS and low work function (Fermi

level near the silicon conduction band edge) for NMOS to achieve appropriate threshold voltage without compromising off-state leakage current [54].

Most metal gate electrodes suffer from high temperature instability resulting in a degraded interface with the underlying dielectric. Many elemental metals form silicides on $SiO_2$ containing dielectrics at high temperature. Due to the modification of work function and equivalent oxide thickness, any reaction at electrode/dielectric interface can be of major concern. Elemental metals with lower work functions have problems in stability due to electro-negativity, which is related to high free energy of formation, and is proportional to the work function. On the other hand elemental metals with higher work functions provide better stability due to their low free energy of formation but may suffer from adhesion issues since they don't react with gate oxide and may result in discontinuous films.

Finally, prediction of work function and the extraction of the actual value on dielectrics is another area that needs investigation. Work function of a metal at a dielectric interface is different from its value in vacuum. It was reported using experimental data as well as interface dipole theory [61-62] that the work function of the metal depends on the permittivity of the gate dielectric. It is necessary to take into account charge transfer across dielectric interfaces to predict metal work functions at dielectric interfaces. There are intrinsic interface states at metal-dielectric interfaces which can be acceptor or donor type. When the metal/dielectric interface is formed, these interface states can be charged resulting in a dipole that make the bands align to minimize the charge transfer. In case where the metal Fermi level is above the dielectric charge neutrality level, the dipole layer created at the interface will be charged negatively on the dielectric side. These dipoles tend to drive the metal Fermi level to charge neutrality level and therefore the effective metal work

function will be different from the vacuum metal work function. It can be the reason that high work function metals will most likely be very inert, while low work function metals will be very reactive with other atom. High work function metals are difficult to etch while low work function metals are likely to react with the underlying gate dielectric.

In addition, it has also been reported that minimal reactions are found to take place between conducting oxides and other dielectric materials at temperatures as high as 900$^{o}$C due to the diffusion barrier property of conducting oxides that can prevent interdiffusion at interfaces [63]. However, the major challenge with conducting oxides is that the oxygen necessary to form them can easily diffuse to the Si interface creating an unwanted interfacial $SiO_2$ layer.

## 1.5. Materials Selection for this research

Ru has high melting point (2334$^{o}$C), high work function (5.1eV), and very low resistivity (6.7Ωμcm). Its atomic mass and radius is 101.1 and 1.30Å, thermal expansion coefficient is 6.4x10-6/$^{o}$C, and has hcp structure with lattice parameter of a=2.71Å/c=4.18Å. It has been extensively studied for DRAM research, forms metallic oxide, can be easily alloyed, and is easily etched compared to Pt. However, it has adhesion problem on $SiO_2$/$HfO_2$ at low and high temperatures. Also, toxic $RuO_4$ forms depending on oxidation state. When Ru is exposed to air/ $H_2O$ at room temperature to 200$^{o}$C, a thin oxide (4~8Å) can form on the surface. $RuO_2$ can be reduced under a reductive condition even by 1% $H_2$. $RuO_2$ forms 600$^{o}$C and $p_{O2}$>100mTorr and dissociates to Ru metal $p_{O2}$ <$10^{-6}$Torr at 700$^{o}$C. $RuO_2$ decomposes to the Ru when heated in a vacuum or in an inert atmosphere. It is reported that $RuO_2$ is the only stable condensed oxide at 800-1500$^{o}$C and $p_{O2}$=0.01-1atm. However, when

$Ru/RuO_2$ is heated in oxygen stream/atmosphere at very high temperature and reactive ion etching of $RuO_2$ films, RuO4 can form. Corrosion product during oxygen evolution on ruthenium in acid media also can form $RuO_4$ which is very toxic and highly volatile at 7°C [64-66].

Ta is bcc structured material with atomic mass of 180.9, atomic radius of 1.45Å, thermal expansion coefficient of 6.3x10-6/$^o$C, and lattice parameter of 3.30Å. It has many advantages for metal gates such as high melting point (3017$^o$C), low work function (4.2eV), and very low resistivity (6.7Ωμcm), and low resistivity (20Ωμcm). It can be easily alloyed and easily etched. However, bad contact and high reactivity with underlying dielectrics are possible issues.

W is bcc structured material with atomic mass of 184.8, atomic radius: 1.35Å, work function of 4.6eV, thermal expansion coefficient of 4.5x10-6/$^o$C, and lattice parameter of 3.17Å. It has many advantages for the capping layer such as high melting point (3422$^o$C), resistivity (52.8Ωμcm) and ease of deposition. W has good contact and peeling can be controlled without straining metal underneath. However, oxide formation at the surface can be problem.

## 1.6. Overview of the dissertation

This research focuses on the interactions between metal and high-K dielectrics and also explores a plausible scheme of integration for dual-metal-gate CMOS devices. Following this introduction, Chapter 2 presents study of compatibility of dual metal gate electrodes with high-k dielectrics for CMOS. Ru, Ru-Ta alloy, TaN and TaSiN on low EOT single layer $HfO_2$ and stacked $HfO_2/SiO_2$ gate dielectrics are studied. In addition,

properties at thermal anneal of selected metals on the above dielectrics are introduced and the change in EOT and $V_{FB}$ values are discussed. Effects of capping layer of metal gates are explored in Chapter 3 and Chapter 4 provides information regarding a tunable work function dual metal gate technology for bulk and non-bulk CMOS on $SiO_2$ metal gate processes which provides both tunable work function values and ease of integration for dual metal gate process flow. Vertical stacks of Ru, Ta, and Ru-Ta alloy metal gate layers subjected to high temperature anneals to promote intermixing which resulted in work function tuning are presented.

Chapter 5 provides information regarding a tunable work function dual metal gate technology on high-k gate dielectric metal gate processes which provides both tunable work function values and ease of integration for dual metal gate process flow. Vertical stacks of Ru and Ru-Ta alloy metal gate layers subjected to high temperature anneals to promote intermixing which resulted in work function tuning are presented.

Finally Chapter 6 summarizes the research and provides directions for future work in this area.

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# *Chapter 2 Compatibility of Ru and Ta Based Metal Alloys with High-K Dielectrics for CMOS Applications*

In this chapter, candidate dual metal electrodes such as Ru, Ru-Ta alloy, TaN and TaSiN on low EOT single layer $HfO_2$ and stacked $HfO_2/SiO_2$ gate dielectrics will be presented. It was found that the work function values of various metal gates on $HfO_2$, $HfO_2/SiO_2$ and on $SiO_2$ are similar. Thermal anneal studies of selected metals on the above dielectrics were also performed to evaluate the change in EOT and $V_{FB}$ values.

## 2.1. Introduction

As has been discussed already, metal gate electrodes are necessary to eliminate gate depletion problems that are associated with conventional polysilicon gates. In addition to gate depletion, polysilicon gates have also been shown to suffer from Fermi level pinning on high-K dielectrics [1]. These issues warrant the investigation of metallic gate electrodes on high-k dielectrics. For bulk CMOS devices, metals must have work functions that are near the conduction and valence band edges of Silicon, i.e., ~4.1eV for NMOS and ~5.2eV for PMOS devices [2].

Although based on their work functions, several metal gate electrodes have been investigated for $SiO_2$, their thermal stability, carrier concentration, and their compatibility with high-K dielectrics is not yet fully understood. The questions that need to be addressed include thermal stability of metals on high-K, work function values, and Fermi level pinning and device performance. In this work, we have studied the characteristics of metal gate electrodes on $HfO_2$-based dielectrics with respect to equivalent oxide thickness (EOT),

flatband voltage ($V_{FB}$), leakage, work function and thermal stability. We also investigate the impact of high-K charges on extracting work function values.

Dual metal electrodes such as Ru, Ru-Ta alloy, TaN and TaSiN were investigated on low EOT single layer $HfO_2$ and stacked $HfO_2/SiO_2$ gate dielectrics. It was found that the work function values of metal gates on $HfO_2$ and $SiO_2$ are similar. Thermal stability studies of selected metals on the above dielectrics were also performed to evaluate the change in EOT and $V_{FB}$ values. All these metals have been shown to give good electrical properties on $SiO_2$ gate dielectrics. For the purpose of review, a brief description is given on the properties of the above metals on $SiO_2$. These properties provided the justification of analyzing them on high-k dielectrics.

*Ru-Ta Alloys*: We have previously shown that Ru films were studied as PMOS gate electrodes because of their low resistivity, proper work function, excellent thermal stability and high carrier concentration. The extracted work function values for Ru on $SiO_2$ from the literatures were ~5.0-5.3 eV [3-6]. We have also reported that binary alloys of Ru and Ta are good candidates for CMOS gate electrodes [3, 6]. Ru–Ta alloys are good NMOS gate electrode candidates since they exhibit low work functions and demonstrate superior thermal stability compared to Ta. Furthermore, by increasing the Ru concentration of this alloy, excellent PMOS gate characteristics could be also successfully achieved. The extracted work function values of metal alloys of Ru and Ta on $SiO_2$is strongly dependent on the alloy composition and varies from 4.2 eV to 5.1 eV as shown in Figure 2.1. The work function of this alloy can be varied by controlling the composition thereby enabling its use in both NMOS and PMOS devices. This suggests that $Ru_xTa_y$ films have work functions appropriate for both NMOS and PMOS devices. Although all films with Ta content

exceeding ~35% resulted in a low work function, only the films with Ta content between 40 and 54% exhibited a single Ru-Ta phase. Other films have either Ta phases or mixed phases. The change in EOT is plotted as a function of anneal temperature in Figure 2.2. For Ta > ~65%, a negative change in EOT is observed and is attributed to consumption of the $SiO_2$ from top interface reaction (formation of Ta2O5). On the other hand, films with Ta <54% display excellent thermal stability. Ru–Ta alloys with Ta < 20% exhibited excellent thermal stability equivalent to that of pure Ru films properties suitable for PMOS devices. As shown in Figure 2.3, films with Ta > ~60%, also exhibited a work function change under high temperature anneals. This change was attributed to the formation of $TaSi_2$ at the top interface. No such change was observed for Ta less than 60% and films with at. %Ta <54% on $SiO_2$ displayed excellent thermal stability. Alloys of $Ru_xTa_y$ with 40% < Ta < 54% on $SiO_2$ exhibited excellent properties as NMOS gate electrodes while alloys with Ta < 20% exhibited excellent properties as PMOS gate electrodes. It was believed that the $Ru_1Ta_1$ phase of the film and formation of Ru-Ta bonds improved the thermal stability of the gate-dielectric interface while maintaining appropriate work functions. Excellent thermal stability up to 1000ºC was observed in alloy compositions suitable for both NMOS and PMOS devices [3, 6].

***TaN***: We previously have seen that tantalum nitride appeared to have the correct combination of properties required of a gate electrode of the metal nitrides [7]. $Ta_{1-x}N_x$ with x=0.25 to 0.6 were found to have a work function of 4.5-4.6eV on $SiO_2$, about 0.25eV larger than that of Ta. Incorporation of nitrogen improved the thermal stability on $SiO_2$ from 400-500°C for pure Ta to above 800ºC for TaN films. It was discovered that Ta reduced the dielectric thickness and reacted with Si resulting in $TaSi_2$ formation. Incorporation of

nitrogen improved the thermal stability on $SiO_2$ from 400-500°C for pure Ta to above 800ºC for TaN films. The increase in the effective thickness contributed by this layer was independent of the thickness of the dielectric and stoichiometry of the gate. The amount of nitrogen within the dielectric was proportional to the partial pressure of $N_2$ during the deposition of the gate. In addition, nitrogen introduced into the dielectric during sputtering tends to diffuse to the $SiO_2$/Si interface under rapid thermal anneals causing a negative shift in the flatband voltage Nitrogen from $Ta_{1-x}N_x$ film can diffuse through the oxide when oxide layer is thin enough (less than 35 Å) since the Ta-N bond could also be reduced by the Si substrate, especially with the condition of thin gate oxide thickness, causing oxygen to move down to the Si substrate. This was found to manifest itself as a rollover in the VFB vs. EOT plots. However, thicker dielectrics and lower N content $Ta_{1-x}N_x$ films did not suffer from this mechanism. Although $Ta_{1-x}N_x$ films provide thermal stability their biggest drawback is the near midgap work function which is not suitable for bulk devices. However, these materials could still be useful for i) SOI gate electrodes, ii) and capping layers for CMOS bulk devices. We still investigated this electrode on high-K dielectrics to understand the impact of Fermi level pinning and thermal stability of TaN gates.

***$TaSi_xN_y$***: It has been reported that the work function of $TaSi_xN_y$ is compatible with NMOS devices, provided the right composition is achieved [8]. It was found that $TaSi_xN_y$ films on $SiO_2$ provide work function (4.2~4.4eV) compatible with NMOS devices and good thermal stability up to 1000ºC resulting in minimal change of EOT, while demonstrating low leakage current. The improved stability of $TaSi_xN_y$ gates is attributed to the presence of Si and N in the gate electrode, which can improve the film microstructure and the diffusion barrier properties at the gate-dielectric interface. As shown in Figure 2.4, the $TaSi_xN_y$ gates

display good stability on $SiO_2$ even up to 1000ºC with no degradation of the CV curves. As shown in Figure 2.5, negligible change in EOT of the TaSixNy/$SiO_2$ stack after high temperature anneals demonstrates the excellent thermal stability of these gates. The current-voltage (I-V) characteristics of $TaSi_xN_y$ gates on $SiO_2$ displayed lower gate leakage compared to the $TaSi_x$ gates for both 400ºC and 1000ºC anneals. It is believed that the microstructure of the film and the presence of nitrogen retards reaction rates and improves the chemical stability of the gate-dielectric interface. We found that the work function of $TaSi_xN_y$ (Si>Ta) with varying N contents ranges from 4.2 ~ 4.3 eV. However, the work function of $TaSi_xN_y$ (Ta>>Si) were higher and closer to those observed with $TaN_x$. It was found that the presence of excess Si resulted in an increase of the workfunction under high temperature anneals and was attributed to $TaSi_2$ formation at the gate-dielectric interface. This effect was prevented by reducing the Si content and adding N to the film. Also, the lack of Si (i.e. $TaN_x$) resulted in undesirably high work function values. Therefore, the improved stability of $TaSi_xN_y$ gates is attributed to the presence of both Si and N in the gate electrode, which can improve the film microstructure and the diffusion barrier properties at the gate-dielectric interface. This stability of $TaSi_xN_y$ films may enable high-k dielectrics and metallic electrode to be implemented in advanced CMOS devices [9].

## 2.2. Experimental

Details of the MOS capacitor fabrication process are summarized in Table 1. Thermally grown $SiO_2$ and PVD $HfO_2$ were used as gate dielectrics. $HfO_2$ films were prepared by sputtering 15-20Å of Hf followed by oxidation at 600°C in $N_2$ for 30seconds (expected EOT 10Å to 20Å). The gate electrodes studied include TaN, TaSiN, Ru and two

Ru-Ta alloy compositions: $Ru_{50}Ta_{50}$ (low work function) and $Ru_{90}Ta_{10}$ (high work function) [3, 8]. These two compositions of Ru-Ta are expected to give a low and a high work-function, respectively. Compositions of TaN and TaSiN are expected as $Ta_{56}N_{44}$ ($N_2$ flow rate= 10%) $Ta_{39}Si_{12}N_{49}$ ($N_2$ flow rate= 10%) [7, 9] All the $HfO_2$ samples were made by PVD process.

All gates were formed via sputtering (Ru), co-sputtering ($Ru_xTa_{1-x}$) and/or reactive sputtering (TaN, TaSiN) in a system with a base pressure of ~$3x10^{-9}$ Torr. All samples were annealed in 10% $H_2/N_2$ at 400°C for 30 min. The samples were then subjected to a rapid thermal anneal (RTA) in argon at 700°C, 800°C and 900°C for 30sec. Capacitance-voltage (C-V) and current-voltage (I-V) characteristics were obtained using HP4284 and HP4155B, respectively. The $V_{FB}$ and EOT were obtained using the NCSU C-V software [10].

## 2.3. Compatibility of Dual Metal Gate Electrodes with High-K Dielectrics for CMOS

Figure 2.7 shows the C-V curves for the Ru based electrodes, i.e. Ru, $Ru_{90}Ta_{10}$ and $Ru_{50}Ta_{50}$, on $HfO_2$ on p-type substrates. The inset of Figure 2.7 shows the data for the same electrodes on $SiO_2$. Although the flatband values are different for $SiO_2$ and $HfO_2$, similar $V_{FB}$ shifts are observed between the various gates on both $SiO_2$ and $HfO_2$ suggesting that the work function shifts are preserved between $SiO_2$ and $HfO_2$ with Ru based electrodes.

Figure 2.8 shows the C-V curves for Ta based electrodes, i.e. TaN, TaSiN and Ta, on $HfO_2$ and the inset of Figure 2.8 shows the C-V curves for Ta based electrodes on $SiO_2$.

Again, similar $V_{FB}$ shifts are observed for the gates on $HfO_2$ and $SiO_2$ suggesting that the work function differences between Ta, TaN and TaSiN observed on $SiO_2$ are also preserved for $HfO_2$.

Figure 2.9 demonstrates that very low EOT values are attainable with these metal electrodes on both n and p substrates after 400$^{o}$C forming gas anneal on $HfO_2$ gate dielectrics. Out of all the gates, TaSiN resulted in the lowest EOT owing to its excellent oxygen diffusion properties. Interface state densities obtained via conductance measurements are shown in Figure 2.10 for various metal gates on $HfO_2$ as a function of band gap energy. Conductance measurement is based on the measurement of the equivalent parallel conductance of the capacitor as a function of bias voltage at various frequencies. Since the conductance Gm represents the loss mechanism due to interface trap capture and emission of carriers and does not include any information other than on interface states unlike the capacitance, the detection level is better than that of C-V method and considered the most sensitive method to determine $D_{it}$ [11]. As shown, the Ru-rich gates display high interface state density values which can be attributed to a more damage compared to other gates. Sputter damage has many components of which ion bombardment is a major culprit. For heavier target atoms, such as Ru, the energy transferred to Ar will be much higher and hence more damage will be created in the substrate. Also, co-sputtering two metals at half the power each will reduce the voltage and hence the damage to the substrate. Therefore, for co-sputtered Ru-Ta alloys, even though the power density is the same, the voltage is lower and hence the damage is lower. For reactively sputtered samples, the target surface is coated with the reactive gas which also reduces the energy imparted to the Ar atoms [12-15]. Finally, the work function of the gate electrode involved also has an impact on the sputter damage. A lower work function metal will be able to generate more secondary electrons in

the plasma hence reducing the need for a high voltage to create the plasma. However, a high work function metal will require a higher voltage since the secondary electron emission is reduced. The combination of these effects is what is believed to cause the higher sputter damage for Ru films. In order to reduce the interface state density and improve the bulk quality of the film, it has been proposed that a heavier sputtering gas, such as Xe, will be more effective in reducing the imparting energy. This can be understood by Equation. 1 which represents the physical damage model, Here $\eta$ is the energy transfer efficiency from impinging atom (Ar or Xe) to the static atom on the substrate (Si or O), is the mass ratio of the impinging atom to the static atom.

$$h = \frac{4m}{(m+1)^2} \qquad (1)$$

The contribution of the metal atoms been sputtered is relatively small and hence can be neglected. These atoms are typically neutral and hence cannot accelerate in the plasma sheath and also their mean free path is typically much smaller than the substrate-target length. Having a heavier plasma gas will reduce the efficiency of energy transfer and hence minimize the damage imparted to the underlying substrate due to the increased values. As shown in Fig 2.11, indeed using Xe as the sputtering gas reduces the interface state density and the leakage current for Ru gates on ultra thin oxides. However, since Xe was not available during the high-K work, we resorted to using Ar. It's valid for my samples since both Ru and $Ru_{90}Ta_{10}$ have maximum 100W of sputtering power while $Ru_{50}Ta_{50}$ has only 50W of sputtering power resulting in less voltage than that of Ru gate.

The higher interface state density is also supported by the C-V curve shown in Figure 2.7.

$$V_{FB} = \Phi_{ms} - \frac{Q_f}{C_{ox}} - \frac{Q_{it}}{C_{ox}} \qquad (2)$$

where, $\Phi_{ms}$ = work function difference between metal and semiconductor, $Q_f$ is oxide fixed charge and $Q_{it}$ interface trap charge [16]. As shown above (Eq.2), the flatband voltage can vary with fixed charge as well as interface state charge in case that $Q_{it}$ is not negligible as $SiO_2$. When interface states cannot be neglected, $V_{fb}$ will be changed according to how they are charged. In this case, it may be better to use the midgap voltage, which corresponds to surface potential $\Phi s = 0$, instead of $V_{fb}$. $Q_{it}$ will not simply shift the C-V curves in parallel but stretch them out, because the interface state occupancy varies with Vg. Since acceptor and donor like interface states are only in the upper and lower halves of the bandgap, respectively, interface states are considered not to be charged when the surface potential $\phi s = 0$ , i.e., the intrinsic condition. Therefore, no shift $Q_{it}$ is observed in a high frequency C-V curve when C is equal to the midgap capacitance Cmg defined for $\Psi s = \phi_f$ [11, 17].

Figure 2.12 shows the comparison of midgap vs. EOT and flatband voltage vs. EOT with Ru gates. As shown, the midgap voltage leads to a different value of work function than the flatband voltage. This work function from midgap voltage doesn't include the effect of interface state charge. This confirms that the interface state densities do influence the work function extraction. It should be noted that on $SiO_2$ based dielectrics, the impact of $D_{it}$ is generally small. However, on high-K dielectrics where the $HfO_2$ layer is close the Si interface, large values of interface state densities can be observed. Furthermore, the assumption that the top half of the band gap contains acceptor type traps whereas the bottom half contains donor type traps may also not be completely valid for alternative dielectrics.

This issue will be addressed further in chapter 5. Finally, low hysteresis and low leakage currents are also observed in these samples as shown in Figures 2.13 and 2.14, respectively.

A key issue for metal gates on $HfO_2$ is their work function. Although Figures 2.7 and 2.8 indicate that the separation of $V_{FB}$ among various gates on $HfO_2$ is retained, it still does not reveal the true work function value. To obtain an accurate work function value, either a capacitance or a current based approach is typically used. Current methods require an accurate knowledge of the conduction mechanism mode whereas capacitance methods require varying the thickness of the $HfO_2$ layer to obtain an accurate bulk charge model.

Varying the thickness of the $HfO_2$ layer obtained by PVD, i.e. via depositing a thin layer of Hf metal and oxidizing it to form $HfO_2$, is quite difficult due to the variability in composition when oxidizing metals of different thicknesses. This issue can be overcome by depositing the $HfO_2$ by ALD or CVD however at the time of this work, these techniques were not available. Therefore, an alternate approach was used which consisted of forming $HfO_2/SiO_2$ stacks wherein the total EOT was varied by varying only the interfacial $SiO_2$ layer. The equation for $V_{FB}$ for this scenario is given by [18]:

$$V_{FB} = \Phi_{ms} - \frac{1}{e_{ox}}\left[\int_0^{EOT_1} x\,r(x)dx\right] - \frac{1}{e_{ox}}\left[Q_{f\,2\inf}\,EOT\right] - \frac{1}{e_{ox}}\left[\frac{1}{2}\,r_{f\,2bulk}EOT^2\right] + \frac{1}{e_{ox}}\left[\frac{1}{2}\,r_{f\,2bulk}EOT_1^2\right] \quad (3)$$

where ($\varepsilon_{ox}$ is the permittivity of $SiO_2$ and $\Phi_{ms}$ is the work-function difference between gate and substrate. The top high-k dielectric EOT is defined as $EOT_1$ and bottom $SiO_2$ dielectric EOT is defined as $EOT_2$. The gate dielectric charge distribution per unit volume is defined

as ρ, and the charges at the $SiO_2$/Si interface are defined as $Q_{f2int}$ (per unit area) and $SiO_2$ bulk charges are defined as $r_{f2bulk}$ (per unit volume).

The VFB vs. EOT curves for Ru and $Ru_{50}Ta_{50}$ gates with varying single layer $SiO_2$ and bilayers $SiO_2$/$HfO_2$ stacks consisting of varying $SiO_2$ interface layer and a constant $HfO_2$ are shown in Figure 2.15. As shown in equation 3 above, the charge analysis calculations reveal that the slope of the $V_{FB}$ vs. EOT curves of the $HfO_2$/$SiO_2$ stacks is proportional to the $SiO_2$ charge, however, the intercept is now a combination of $\phi_{ms}$ and the charge in the high-K layer. The slope with $HfO_2$/$SiO_2$ stacks is slightly larger, indicating that more charge is incorporated in the interfacial layer. This charge can be attributed to (i) process damage associated with Hf deposition and oxidation and/or (ii) Hf incorporation within the $SiO_2$ layer. The latter makes the assumption of $SiO_2$/$HfO_2$ bilayers not accurate and requires a three layer model. In fact, the EOT of the $SiO_2$/$HfO_2$ stacks is not as thick as expected from the $HfO_2$ deposition condition. The expected physical thickness from sputtering rate of $HfO_2$ was 50Å and thickness of $SiO_2$ measured by ellipsometer was 24~104Å but actual EOT of $SiO_2$/$HfO_2$ stacks for $Ru_{90}Ta_{10}$ was 30~104Å at 400°C. This indicates some degree of intermixing of the two layers during deposition of subsequent annealing leading to an internal interfacial reaction layer. Due to the various uncertainties in the stacks composition, accurate analysis of the work function is difficult. However, since the dielectrics of varying EOTs have the same $HfO_2$ layer and hence also the same interfacial layer, a comparison of the intercepts to assess the differences in work function of various electrodes on $SiO_2$ and on $HfO_2$/$SiO_2$ was made. In addition, as has been showed by Jha [18], if the top layer thickness is kept thin, then the addition of charges on the intercept can be kept to a minimum. Using this structure, we investigate the work function differences of Ru based and Ta based electrodes on $HfO_2$/$SiO_2$

and compared them to $SiO_2$. As shown in Figure 2.15, for both Ru and $Ru_{90}Ta_{10}$ electrodes, there is a positive shift in the intercept value with $HfO_2/SiO_2$ as compared to $SiO_2$ only. Table 2.2 lists the effective work functions (extracted from the intercepts) of Ru and $Ru_{50}Ta_{50}$ on $SiO_2$ and $HfO_2/SiO_2$ stacks. Although there is a shift between the $\phi_{ms}$ for $SiO_2$ compared to $HfO_2/SiO_2$, the shift between the two gates for a given dielectric is the same, suggesting that the work function difference is preserved even on $HfO_2$. This also suggests that Fermi Level pinning with these metals on $HfO_2$ is either not occurring or is minimal. This is a key advantage of metal gates over polysilicon gates, which have recently shown to suffer from Fermi Level pinning [1]. An accurate determination of the charge value of $HfO_2$ requires an alternate deposition technique, such as atomic layer deposition or chemical vapor deposition or comparison to an ideal curve. Also, although the above results indicate minimal pinning on $HfO_2$ surfaces, it should be noted that technologically relevant stacks do not have a thick $SiO_2$ interfacial layer and as such their work functions may be quite different than the ones being encountered here. In fact, as has been published recently the behavior of single layer $HfO_2$ vs. stacks $HfO_2/SiO_2$ is different [19].

Figure 2.16 shows that similar positive shifts are also observed with TaN and TaSiN on $HfO_2/SiO_2$ gates compared to $SiO_2$. It should also be noted that N diffusion observed in $SiO_2$ with TaN (Fig. 2.17) is suppressed in $HfO_2/SiO_2$ gates. It was reported that the $V_{FB}$ deviates from its linearity in $V_{FB}$ vs. EOT curves of Ta1-xNx gates only in the thin oxide regime (less than 35Å). The Ta-N bond could also be reduced by the Si substrate, especially with the condition of thin gate oxide thickness, causing oxygen to move down to the Si substrate. The reduction of Ta-N by Si-N is thermodynamically favored due to the low Gibbs free energy of Ru-O bond (-349~428kJ/mol) as compared to the Si-O bond (-

1000kJ/mol). Thus, nitrogen from $Ta_{1-x}N_x$ film can diffuse through the oxide when oxide layer is thin enough (less than 35 Å) It was also observed that this deviation was a strong function of the $N_2$ flow rate during sputtering [7]. It is well known that nitrogen tends to contribute a positive charge to the dielectric, which shifts the $V_{FB}$ to more negative values. It was suspected that charged species of nitrogen from the glow region of the plasma with significant kinetic energies are incident on the gate dielectric during the deposition of the electrode. If the dielectric thickness is very thin then N may reach the Si-$SiO_2$ interface where it may impact the flatband voltage. As can be seen in Figure 2.16, this is more severe on the thinnest sample on $SiO_2$. However, for the $HfO_2$ the physical thickness is thicker that of $SiO_2$. So there is less charge effect due to positive charge caused by nitrogen

This can be attributed to the $HfO_2/SiO_2$ layers being physically thicker at a given EOT. This also implies that the work function of TaN is closer to midgap but cannot be accurately determined on $SiO_2$ due to N diffusion, which causes rollover of $V_{FB}$ as seen in Figure 2.17.

The high temperature stability of various metals on $HfO_2$ is shown in Figure 2.18. Almost all gates suffer from 3-5Å EOT increase after 900°C, which can be attributed to the oxidation of the underlying silicon surface. TaSiN resulted in the smallest amount of change which is attributed to its excellent diffusion properties.

The C-V curves for Ru/$HfO_2$ and $Ru_{50}Ta_{50}/HfO_2$ (Figure 2.19) indicate negligible change in $V_{FB}$. Both these electrodes had a 500 Å W capping layer. However, a closer look at the thicker $HfO_2/SiO_2$ stacks reveals a positive change in the intercept value (~0.05V) for both TaSiN/$HfO_2/SiO_2$ and $Ru_{50}Ta_{50}/HfO_2/SiO_2$ stacks (Figure 2.20) indicating the evolution of negative charge. This can be either from interfacial reaction layer due to some degree of

intermixing of the layers or charge redistribution for the thermal energy after high temperature anneal.

In addition, the change in slope of $HfO_2/SiO_2$ layers in Figure 2.20 indicates that the fixed charge in the interfacial layer may also be changing since this slope change was not observed for $SiO_2$ as shown in Figure 2.21. As was mentioned earlier, some degree of intermixing in the $HfO_2/SiO_2$ stacks is expected at higher temperatures and this may be responsible for the increase in interface charge.

Figure 2.22 shows the $V_{FB}$ vs. EOT curves for Ta-based gates. The non-linearity that was observed with TaN on $SiO_2$ at 400°C (Figure 2.16) was also observed with $HfO_2/SiO_2$ stacks, indicating that N diffusion through $HfO_2$ can occur at higher temperatures.

The $D_{it}$ values obtained via conductance for annealed samples are provided in Figure 2.23 and indicate a slight increase in $D_{it}$ with increasing anneal temperature. However, the level of $D_{it}$ after anneal at 700°C was almost similar for $Ru_{50}Ta_{50}$ on $SiO_2$. There was no forming gas anneal after the high temperature anneal.

Another important point of concern is whether the metal is diffusing through the ultra thin $HfO_2$ films. To this end, we investigated Ru gates on 40Å of $HfO_2$ films and performed both front side and back side SIMS on them. As shown in Fig 2.24, the front side SIMS at both low and high temperature does not show any obvious change of the Ru profile suggesting that the diffusion is prevented. However, the W profile does change considerably. The role of the W on top of Ru and capping layers in general will be addressed in the next chapter. In order to investigate the electrodes where Ru is bonded and how that impacts the diffusion, we also studied Ru-Mo. As shown in the XRD plot in Figure 2.25, Ru-Mo bonds are clearly observed at low and high temperature. The SIMS

analysis results as shown in Fig 2.24a and b do not indicate any changes from the case of pure Ru. This suggests that Ru does not suffer from diffusion problems through $HfO_2$ dielectrics. From that point of view, it has advantages of Pt and Ni which are known to diffuse into $HfO_2$ after high temperature annealing [20, 21].

To further understand the diffusion issue, we also obtained backside SIMS profiles as shown in Fig. 2.27. An $O_2^+$ beam was used for SIMS analysis. It was observed that Ru appears to be relatively stable with respect to interdiffusion at high temperature anneal at $1000^oC$. Ru inter-diffusion with $HfO_2$/Si was not observed. However, it was observed some W inter-diffusion in the metal portion of the stack after annealing. From a structural point-of-view, crystallization and therefore grain boundary diffusion is a major factor with the $1000^oC$ anneals. Both Ru and of course $HfO_2$ will crystallize under these conditions. For the interfacial region with Si, we would probably need to do an even more surface sensitive approach (like TOFSIMs) to conclusively establish if there is any Hf, Ru or W penetration into the Si. The W also appears to go very near the Si substrate in these profiles, suggesting that there is some interpenetration with the $HfO_2$.

In the next chapter, we will investigate the impact of the capping layer on the final gate stack properties. As the SIMS in this section indicated, W was found to diffuse through Ru-Mo after high temperature anneal. Many of the gate electrode properties may be influenced by the ambient conditions and diffusion through the metal gate at high temperature. A Capping layer might suppress the unwanted properties of the gate stack or influence properties on the final gate stack. The Role of capping layer on Ru metal gates with another metal will be investigated in detail in terms of merit and issues that may be involved in the integration of such gates stacks in next section.

Figure 2.28 shows that the TEM pictures of our HfO2 films with RuTa gate. It was expected that physical thickness from sputtering rate of $HfO_2$ was 50Å and thickness of $SiO_2$ measured by ellipsometer was 24~104Å but actual EOT of $SiO_2/HfO_2$ stacks for $Ru_{90}Ta_{10}$ was 30~104 Å at 400$^oC$.

Microstructure and interface properties were investigated using cross-sectional transmission electron microscopy (TEM). Figure 2.28 demonstrates the TEM pictures of our $HfO_2$ films with Ru-Ta gate at 400$^oC$ annealing. It was expected that physical thickness from sputtering rate of Hf and subsequent anneal was 50Å.

A rough interface and the presence of an approximately 2.1nm interfacial layer between the $HfO_2$ and Si substrate were observed. It is believed that some native $SiO_2$ layer was formed before Hf deposition and the interfacial layer was formed when the Hf was sputtered and subsequently annealed in $N_2$ prior to the gate electrode deposition to make HfO2 dielectric. When annealed, oxygen is driven to the interface between $ZrO_2$ and Si-substrate thus Si gets oxidized which results in interfacial layer growth.

Since $V_{FB}$ is critically dependent on the state of the dielectric, this implies the $V_{FB}$ may be affected by interfacial layer. Therefore, the high-k dielectric needs to be optimized so that it contains low levels of excess oxygen prior to gate electrode deposition.

## 2.4. Summary

Dual metal electrodes such as Ru, Ru-Ta alloy, TaN and TaSiN on low EOT single layer $HfO_2$ and stacked $HfO_2/SiO_2$ gate dielectrics were investigated. Out of all the gates, TaSiN resulted in the lowest EOT owing to its excellent oxygen diffusion properties. It was found that the work function of metal gates on $HfO_2$ and $SiO_2$ are similar. Thermal

annealing studies of selected metals on the above dielectrics were also performed to study the change in EOT and $V_{FB}$ values. The properties of metal gates on $HfO_2$ were found to be similar to those on $SiO_2$. In extracting the work function values, the charges in the high-K dielectric must be included. Although Fermi level pinning was not observed, the charges in the $HfO_2$ layer must be reduced to obtain the desired threshold voltages. Front and backside SIMS suggests that Ru does not suffer from diffusion problems through $HfO_2$ dielectrics at high temperature.

## 2.5. References


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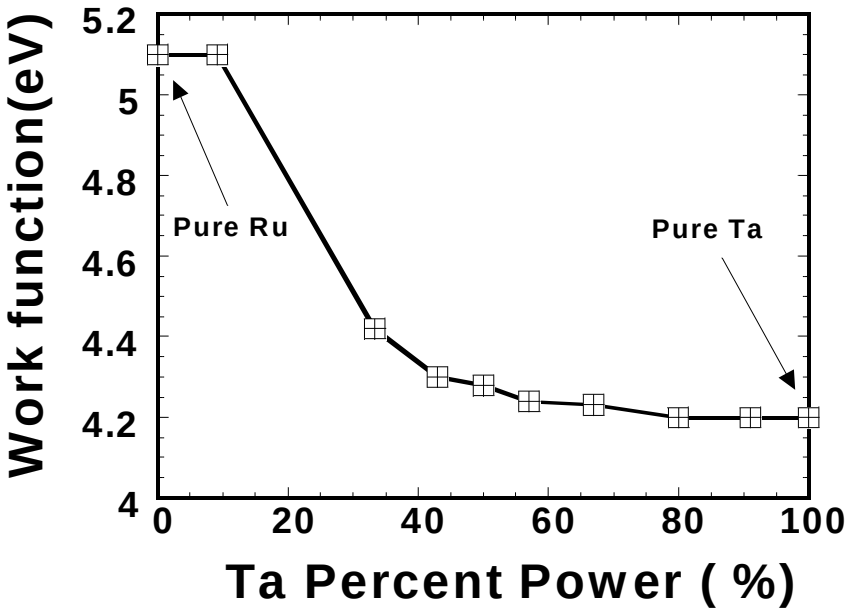



**Figure 2. 1 Work function extracted from C-V curves for various compositions of Ru-Ta alloys. Non-linear behavior as a function of content is observed [3]**

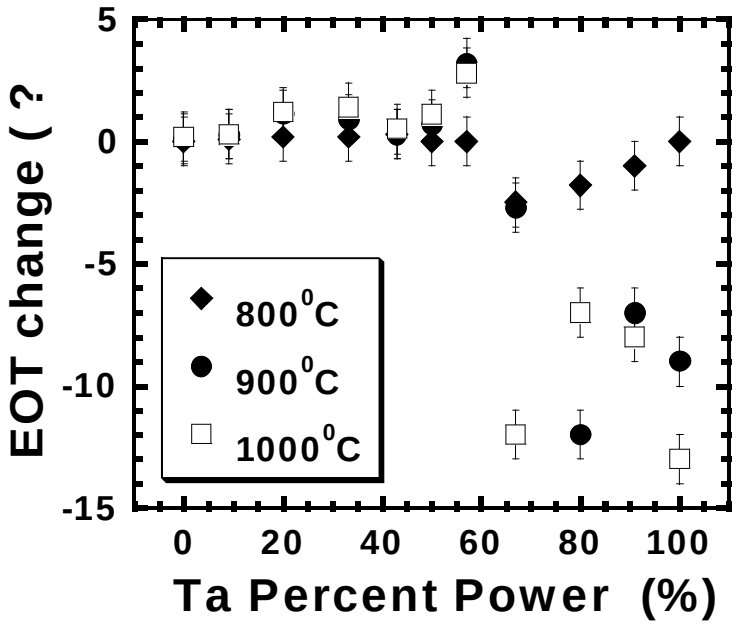



**Figure 2. 2 EOT change under high temperature annealing for Ru-Ta alloys with various Ta percent power conditions on 25Å $SiO_2$ gate dielectrics [3]**

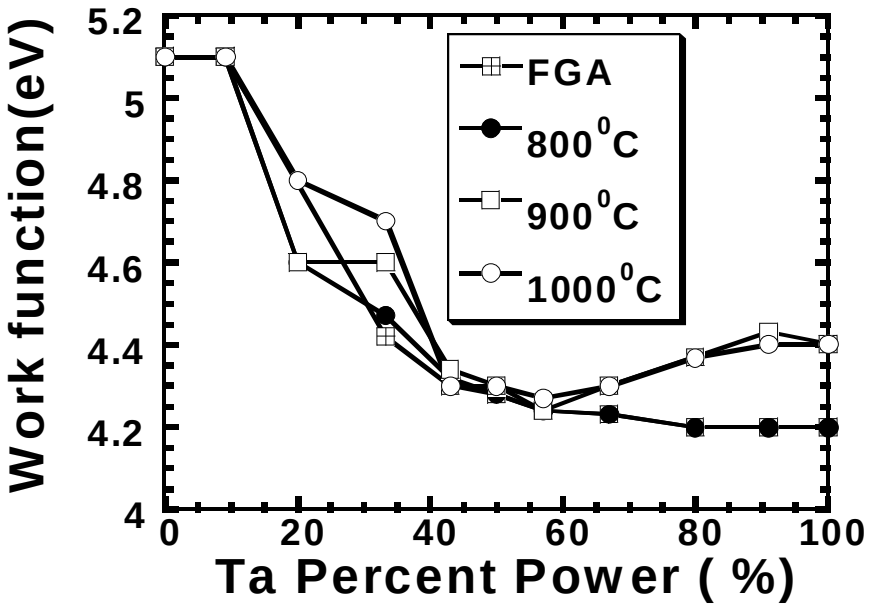



**Figure 2. 3 Work function extracted from CV curves vs. Ta percent power annealed at 800ºC, 900ºC and 1000ºC. The alloys with Ta percent power less than 60% remain stable under high temperature anneals [3]**

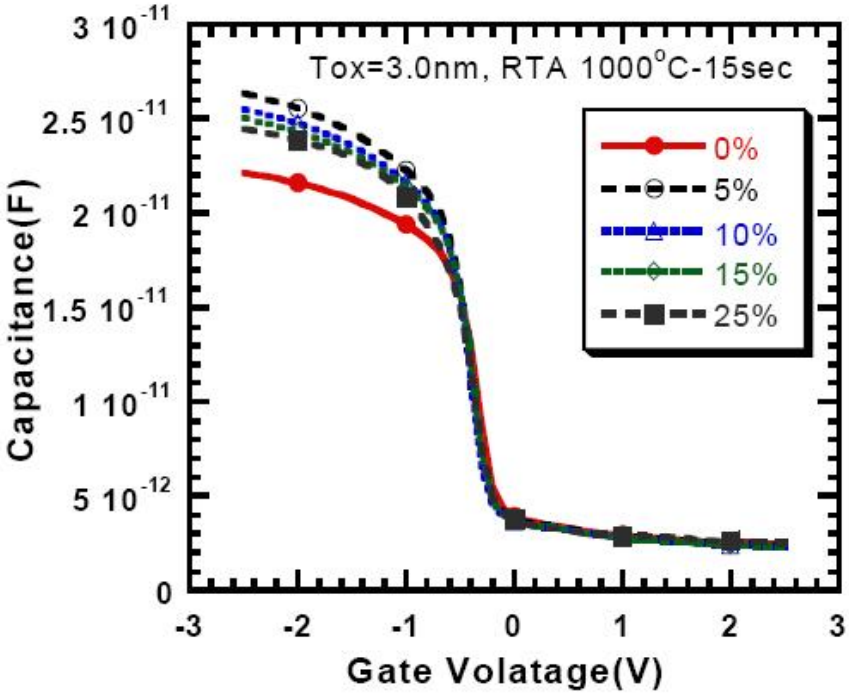



**Figure 2. 4 Typical C-V curves of TaSixNy electrode capacitor with the N2 flow rate, after annealing at 1000ºC for 30min. Capacitor area =2.5E-5cm2 [8]**

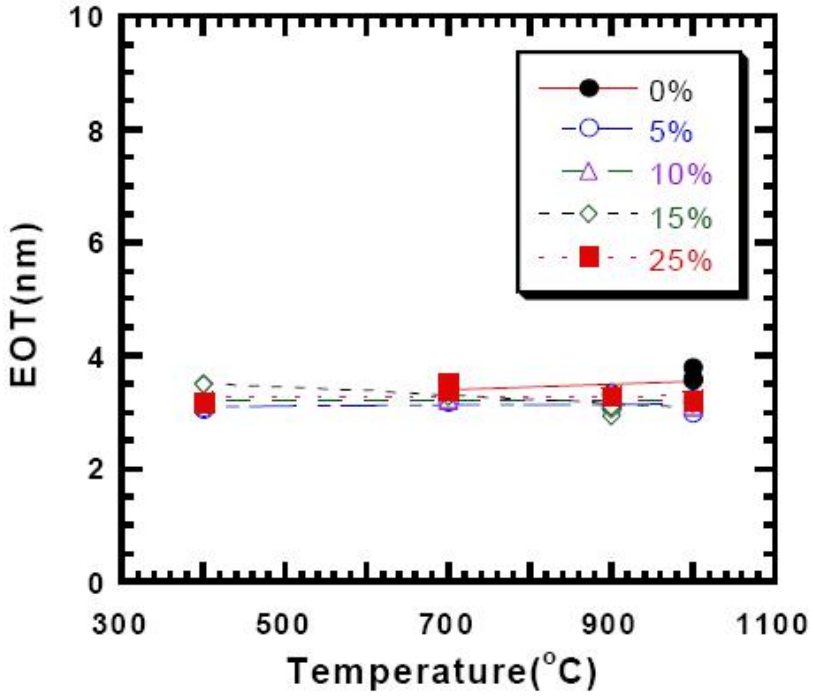



**Figure 2. 5 EOT vs. annealing conditions at the various TaSixNy electrodes [8].**

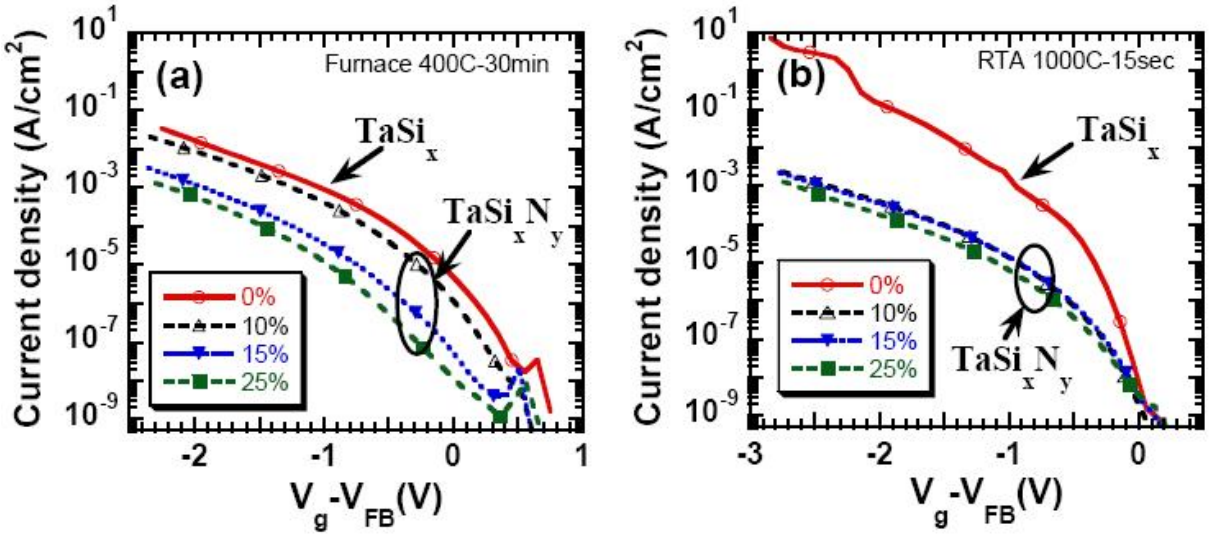



**Figure 2. 6 Typical I-V curves of TaSixNy electrode capacitor with the N2 flow rate. (a) Furnace annealing at 400ºC for 30min and (b) RTA at 1000 ºC for 30sec.[9]**

**Table 2. 1 MOS capacitor Fabrication Process**

- Isolation (Fox=3500Å)
- $SiO_2$ (2-10nm) and $HfO_2$ via Hf PVD (20sec) and oxidation at 600°C for 30sec
- TaN, TaSiN, Ru, Ru-Ta Alloys
  RF Magnetron sputtering
- Electrode patterning by Lift-off
- Annealing at 400°C for 30min in 10% $H_2$ in $N_2$
- RTA: 700ºC, 800ºC, 900ºC for 30sec

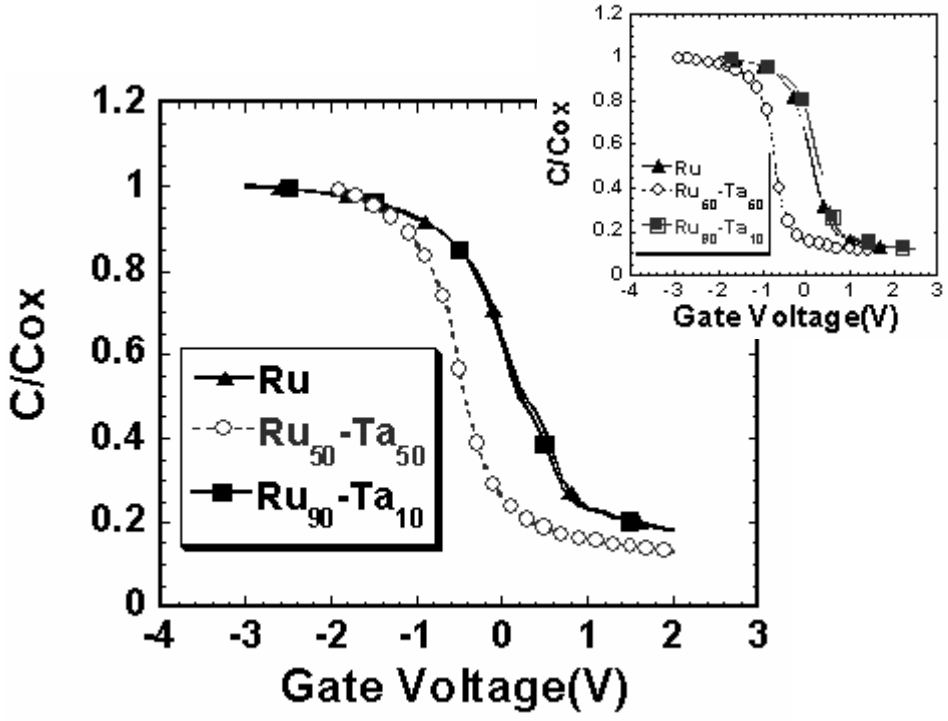



**Figure 2. 7 1 MHz C-V curves of Ru based metal electrodes on $HfO_2$ gate Dielectrics. EOT down to 11Å have been obtained. Inset shows the same electrodes on $SiO_2$.**

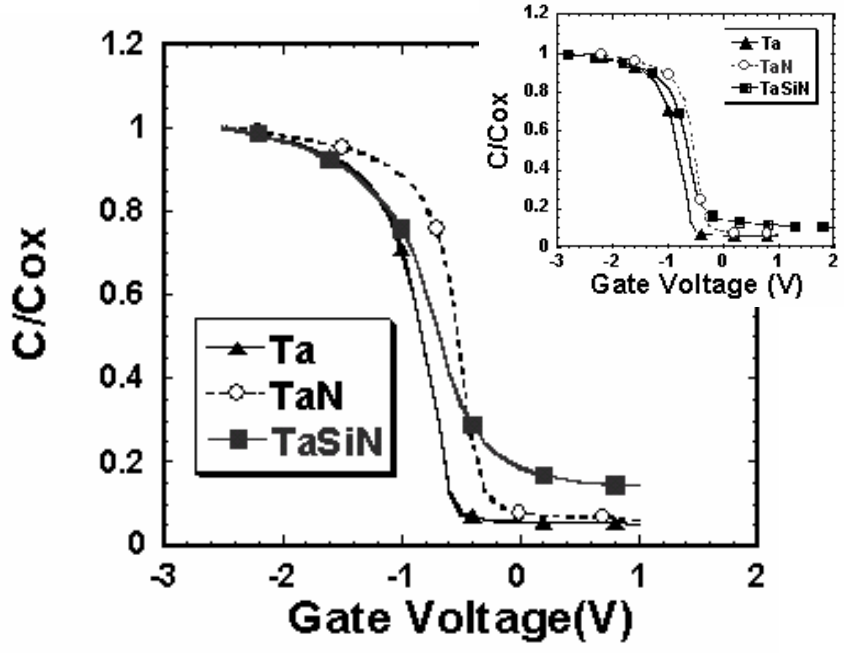



**Figure 2. 8 1 MHz C-V curves of Ta based metal electrodes on $HfO_2$ gate Dielectrics. EOT down to 11Å have been obtained. Inset shows the same electrodes on $SiO_2$. Similar shifts between the gates are observed on $HfO_2$ and $SiO_2$.**

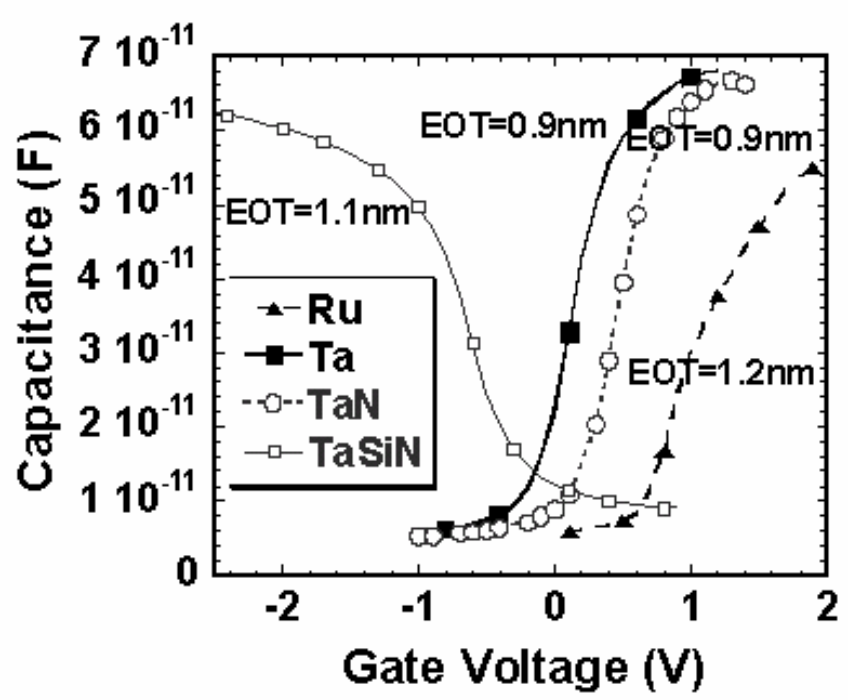



**Figure 2. 9 1MHz C-V curves of Ru, Ta, TaN and TaSiN on $HfO_2$ indicating low EOT values on both n and p substrates.**

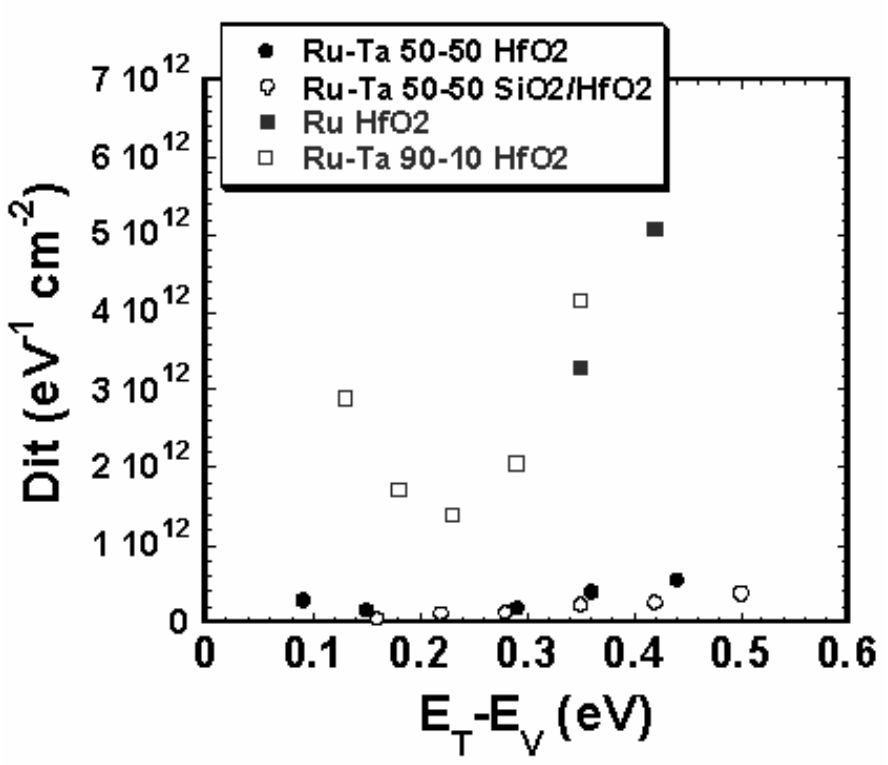



**Figure 2. 10 Interface State Densities of $HfO_2$ via conductance method for selected gate electrodes.**

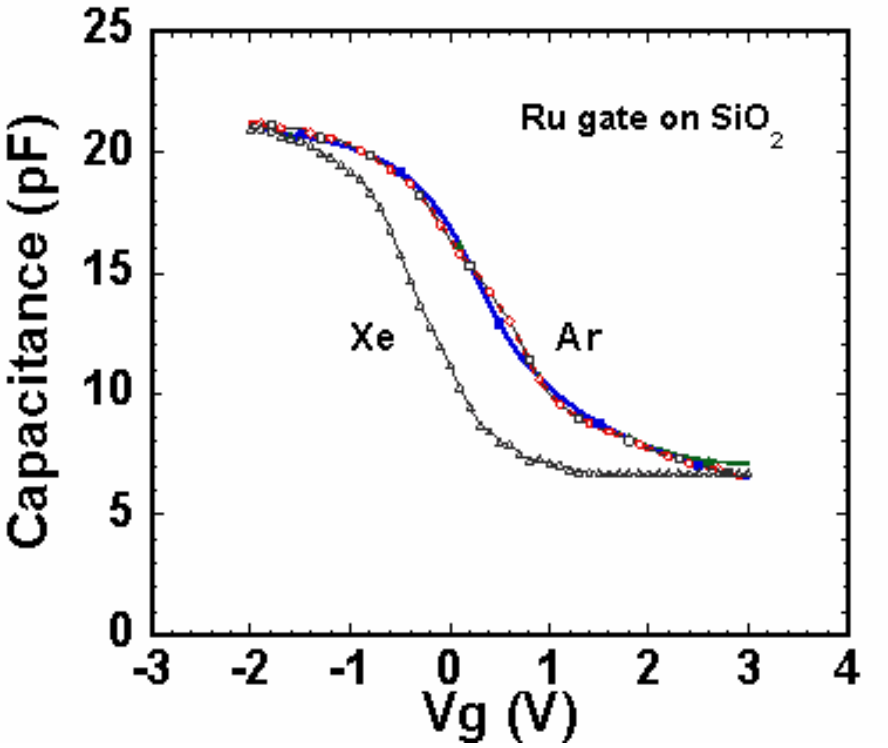



**Figure 2. 11 C-V curves Ru gates sputtered in Ar v. Xe on $SiO_2$**

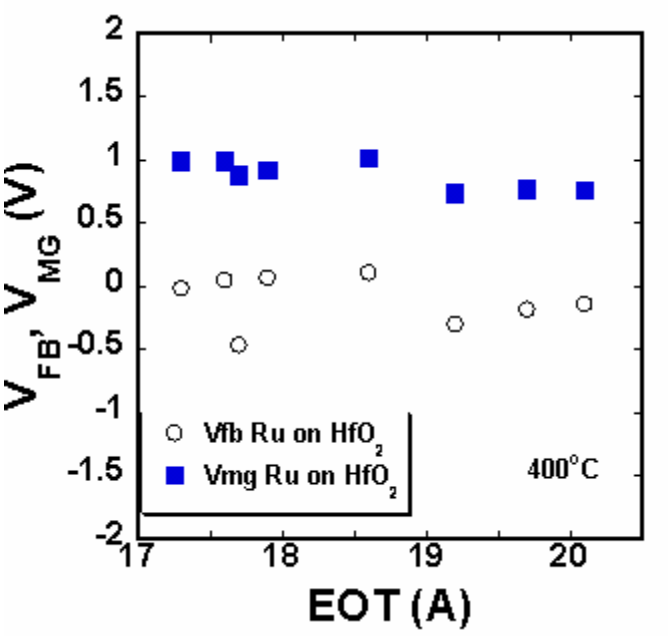



**Figure 2. 12 $V_{FB}$ vs. EOT and $V_{MG}$ EOT curves of Ru based metal electrodes on $HfO_2$ gate Dielectrics. $V_{FB}$ data is more scattered due to high $D_{it}$**

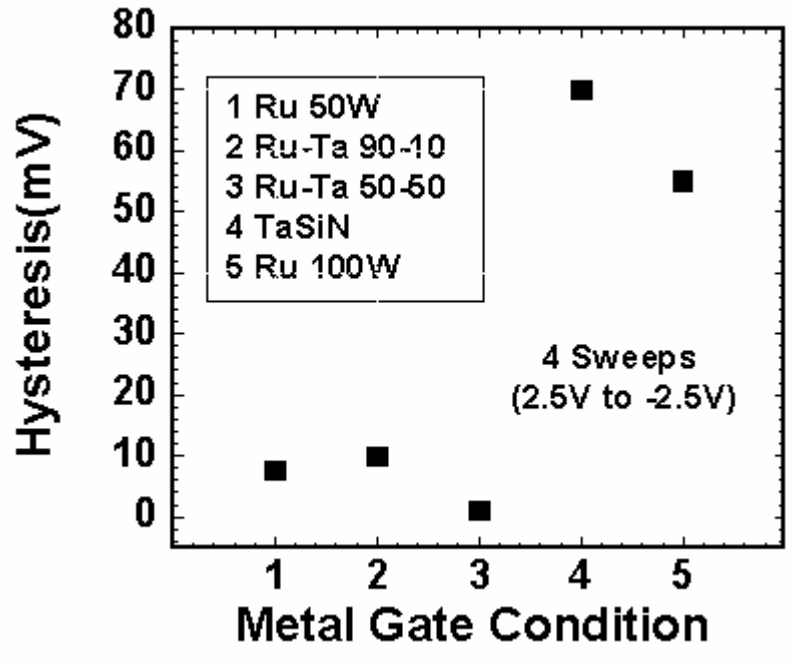



**Figure 2. 13 Hysteresis of $HfO_2$ gate dielectrics with all gate electrodes**

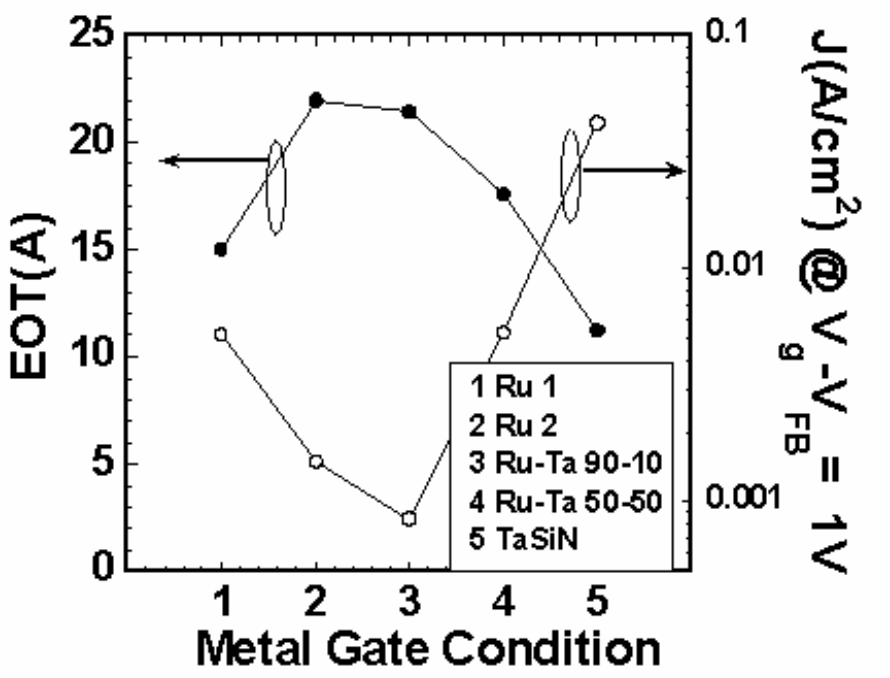



**Figure 2. 14 Leakage current plot for various metal gates on $HfO_2$ gate dielectrics taken at 1V beyond $V_{FB}$.**

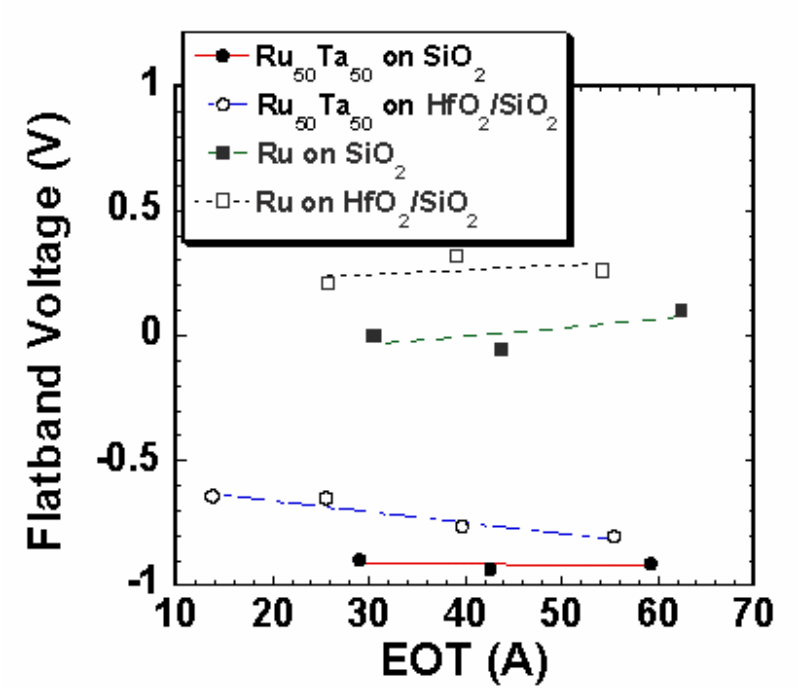



**Figure 2. 15 $V_{FB}$ vs. EOT for Ru and Ru-Ta alloy on $SiO_2$ and $HfO_2/SiO_2$. The stacks have varying $SiO_2$ with fixed $HfO_2$ thickness. Since similar separation is observed this indicates that Fermi Level pinning is not occurring.**

**Table 2. 2 $f_{ms}$ values for Ru and Ru-Ta alloy on $SiO_2$ and $HfO_2/SiO_2$. Since the $f_{ms}$ in the stacked case is dependent on both the workfunction and the charge in the $HfO_2$ layer, the separation between the two suggests that Fermi Level pinning is not occurring.**

| Dielectric | Ru-Ta $f_{ms}$ (V) | Ru $f_{ms}$ (V) | $Df_{ms}$ (V) |
|---|---|---|---|
| $SiO_2$ | -0.89 | -0.14 | +0.75 |
| $HfO_2/SiO_2$ | -0.57 | +0.20 | +0.77 |

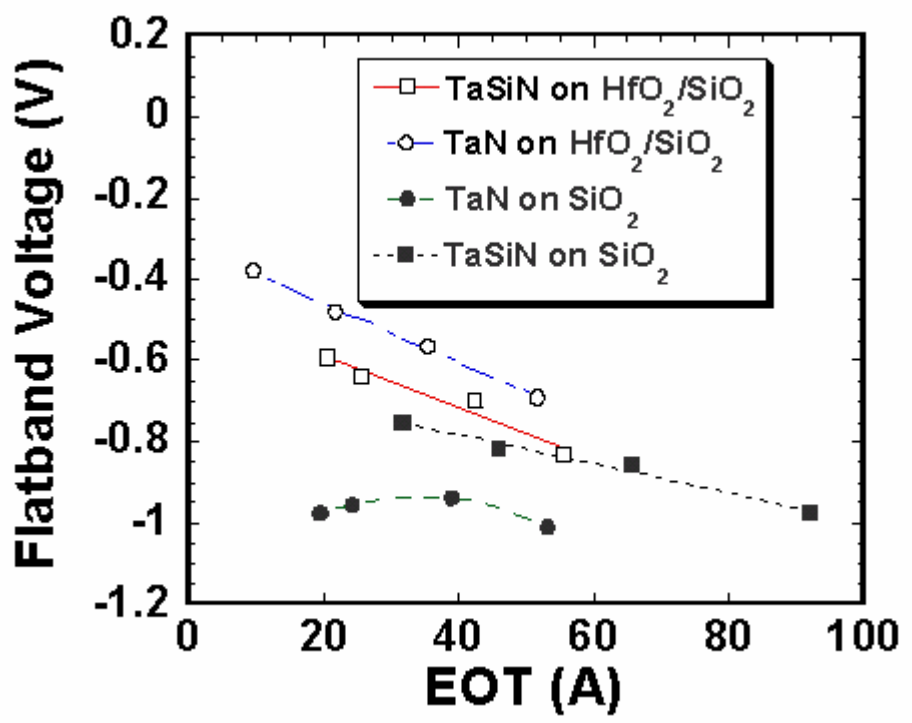



**Figure 2. 16 $V_{FB}$ vs. EOT for TaN and TaSiN on $SiO_2$ and $SiO_2/HfO_2$ stack. The N diffusion is suppressed through $HfO_2/SiO_2$ stack. The work function of TaN is midgap.**

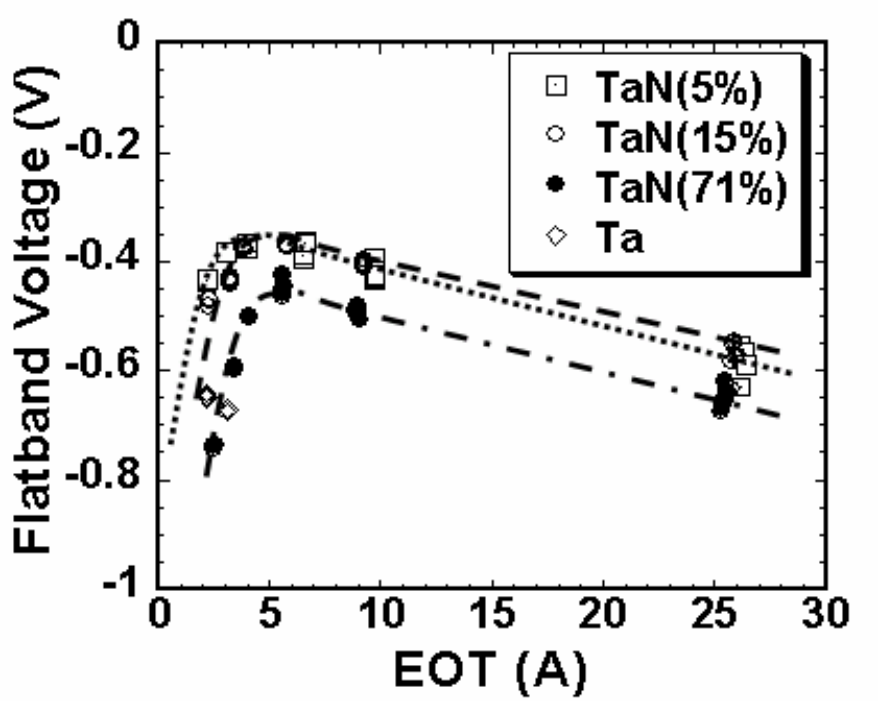



**Figure 2. 17 $V_{FB}$ vs. EOT for TaN on varying thicknesses of $SiO_2$ . The rollover of $V_{FB}$ is attributed to N diffusion into the $SiO_2$.**

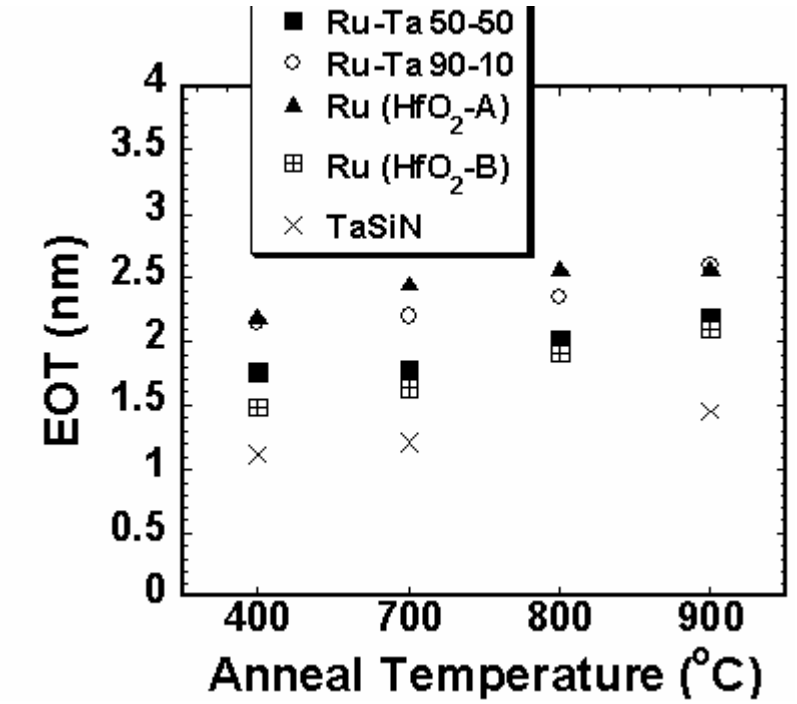



**Figure 2. 18 EOT vs. anneal temperature for all gates as a function of anneal temperature. Ru was investigated on two thicknesses of $HfO_2$.**

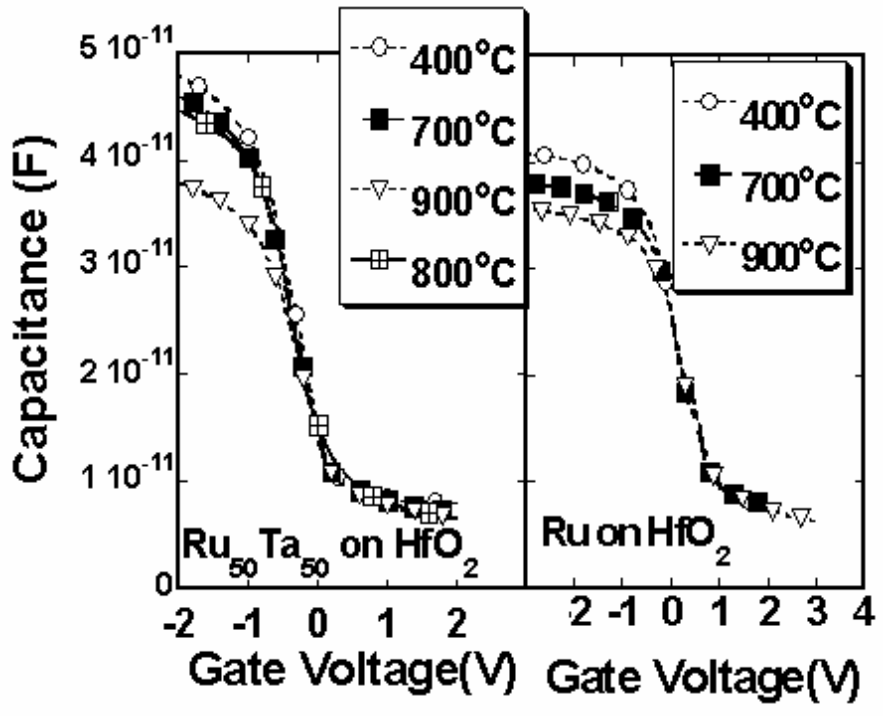



**Figure 2. 19 1MHZ C - V curves for metals on $HfO_2$ as a function of anneal temperature.**

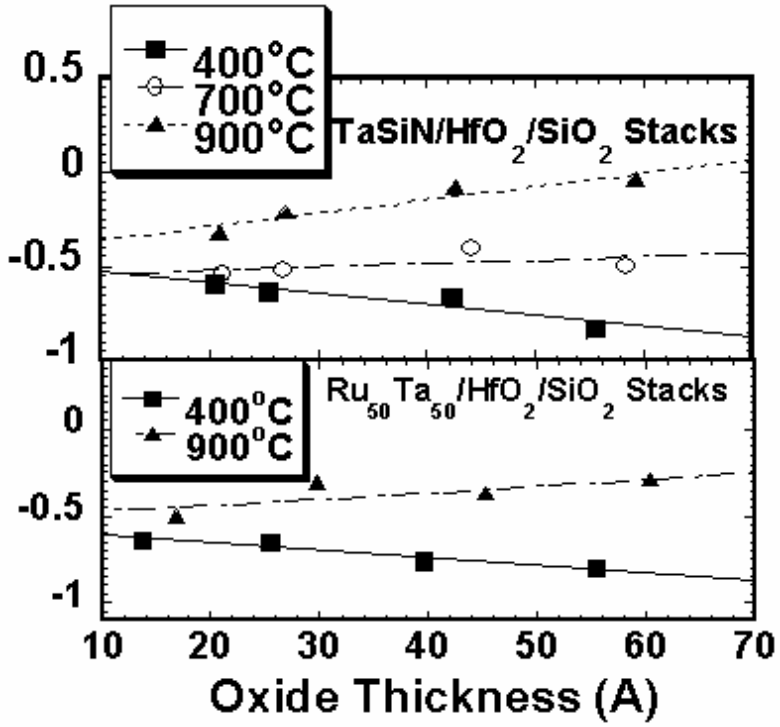



**Figure 2. 20 $V_{FB}$ vs. EOT for $Ru_{50}Ta_{50}$ and TaSiN on $HfO_2/SiO_2$ as a function of anneal temperature showing the improvement and charge.**

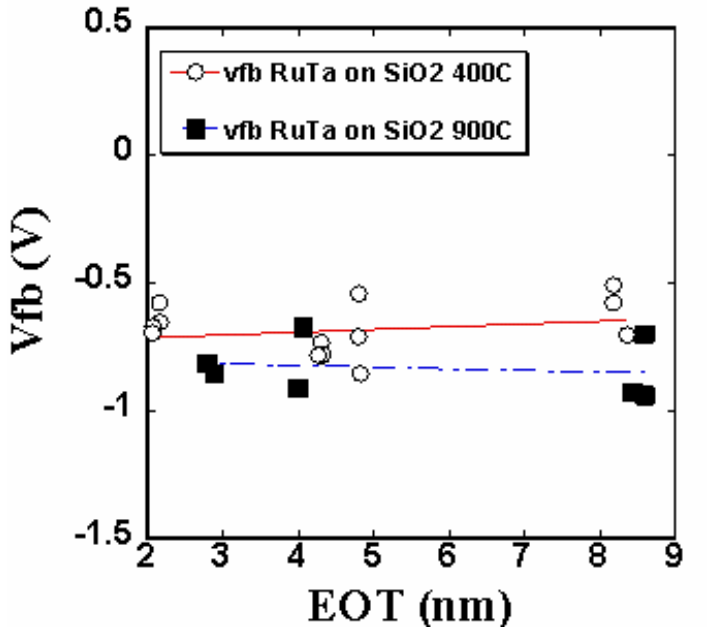



**Figure 2. 21 $V_{FB}$ vs. EOT for $Ru_{50}Ta_{50}$ on $SiO_2$ as a function of anneal temperature showing the improvement and charge. The difference in intercepts at 400°C and 900°C for both gates is ~0.05V**

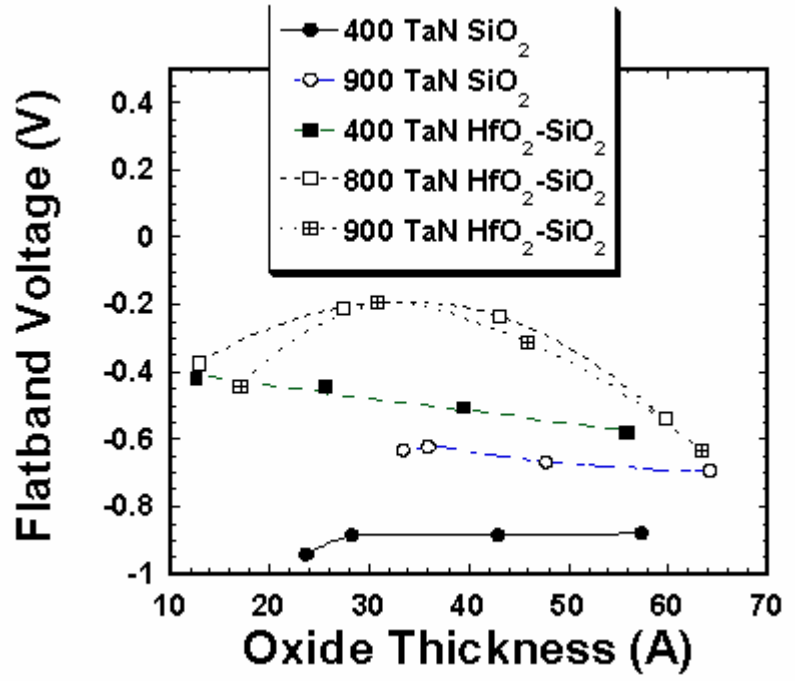



**Figure 2. 22 $V_{FB}$ vs. EOT for TaN on $HfO_2/SiO_2$ and $SiO_2$ as a function of anneal temperature showing the improvement and charge.**

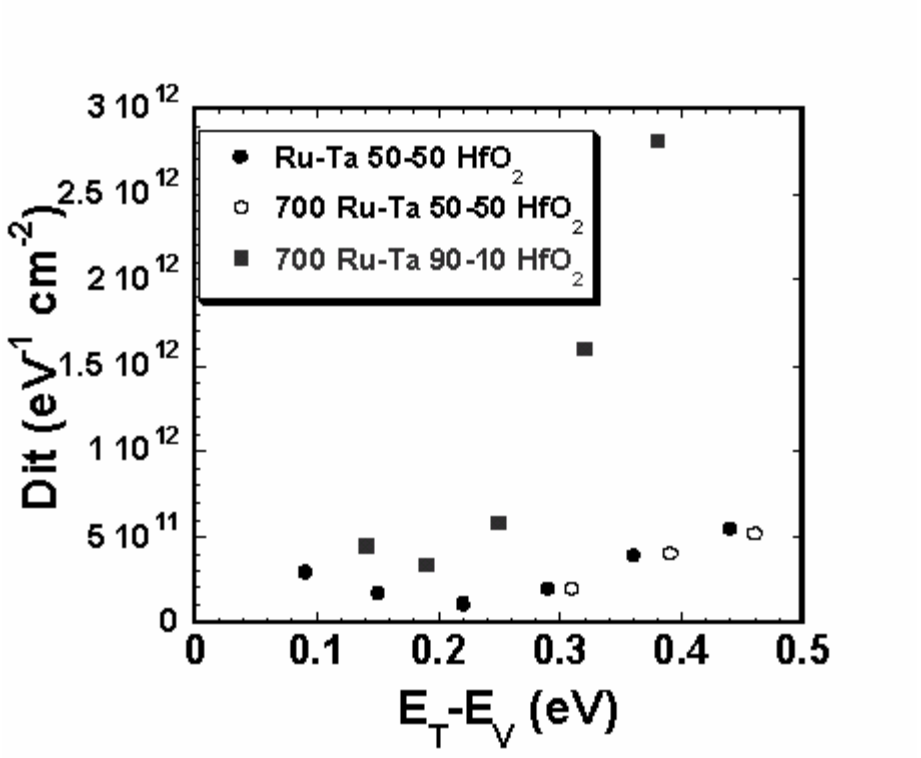
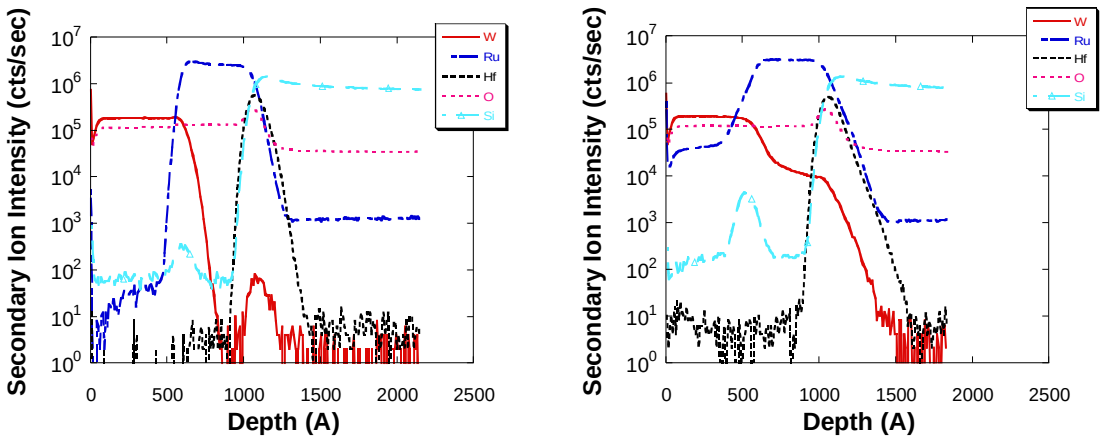



**Figure 2. 23 Interface state density via conductance method as a function of anneal temperature for metal gates on $HfO_2$**




(a) (b)

**Figure 2. 24 SIMS profile analysis (a) as-deposited (b) 900$^{O}$C anneal of W/Ru/$SiO_2$**

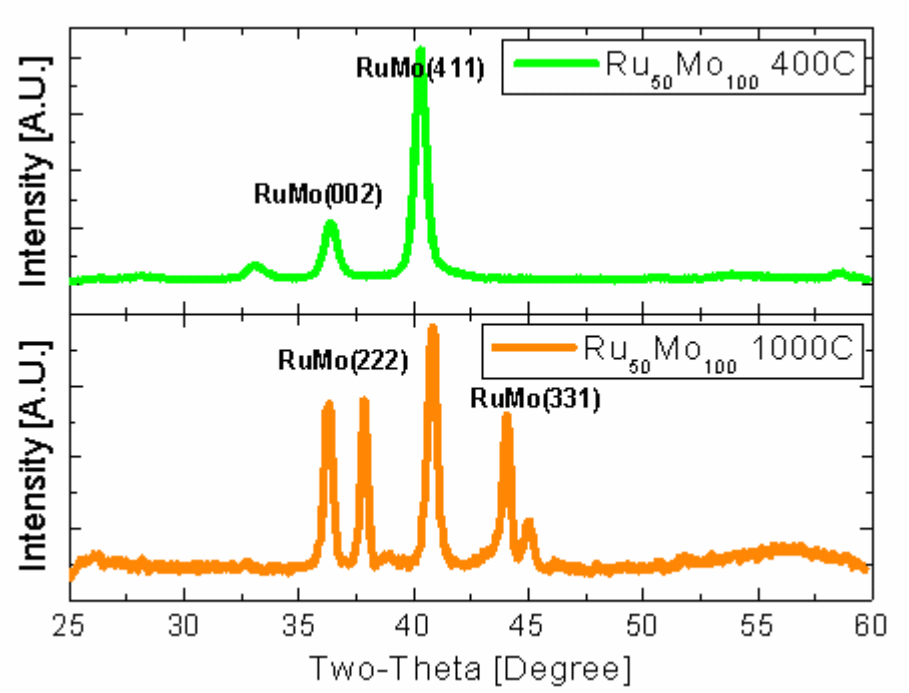
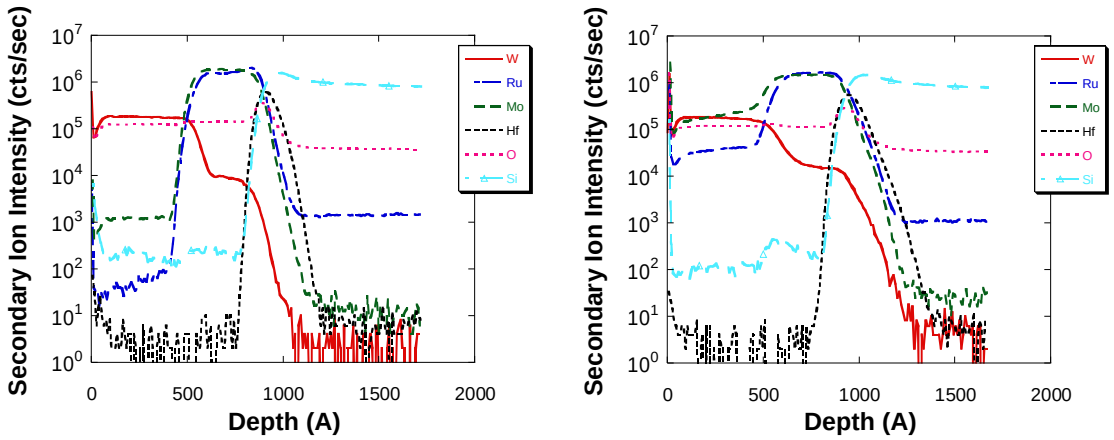



**Figure 2. 25 XRD analysis (a) 400°C (b) 1000°C of RuMo/$SiO_2$**




**(a)** **(b)**

**Figure 2. 26 SIMS profile analysis (a) as-deposited (b) 900°C anneal of W/RuMo/$SiO_2$**

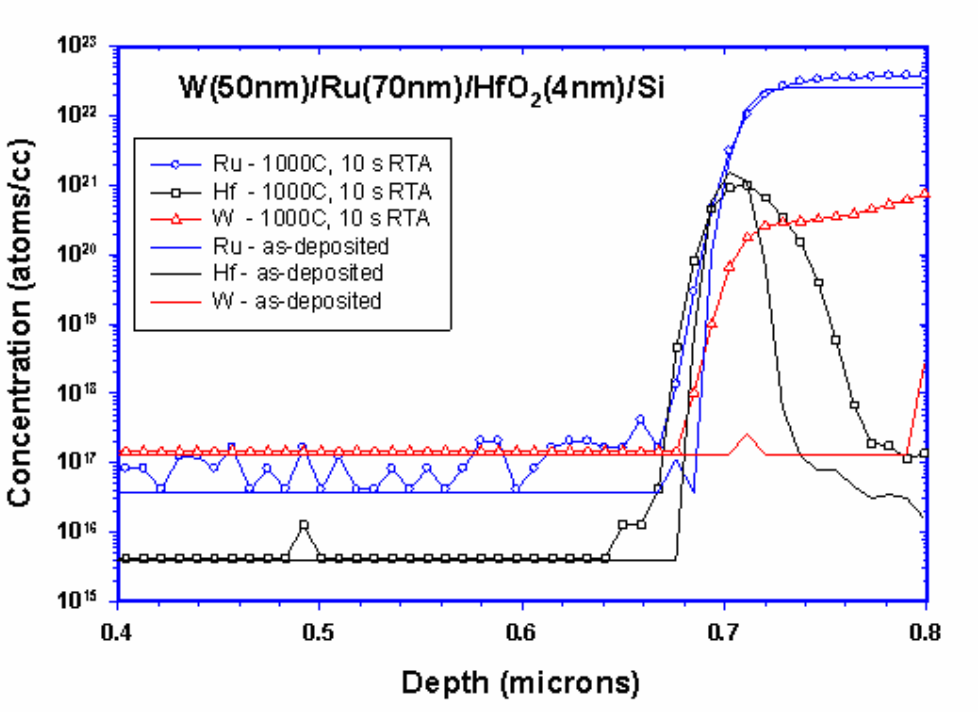



**Figure 2. 27 Back side SIMS profile analysis (a) as-deposited (b) 1000°C anneal of W/Ru/HfiO$_2$**

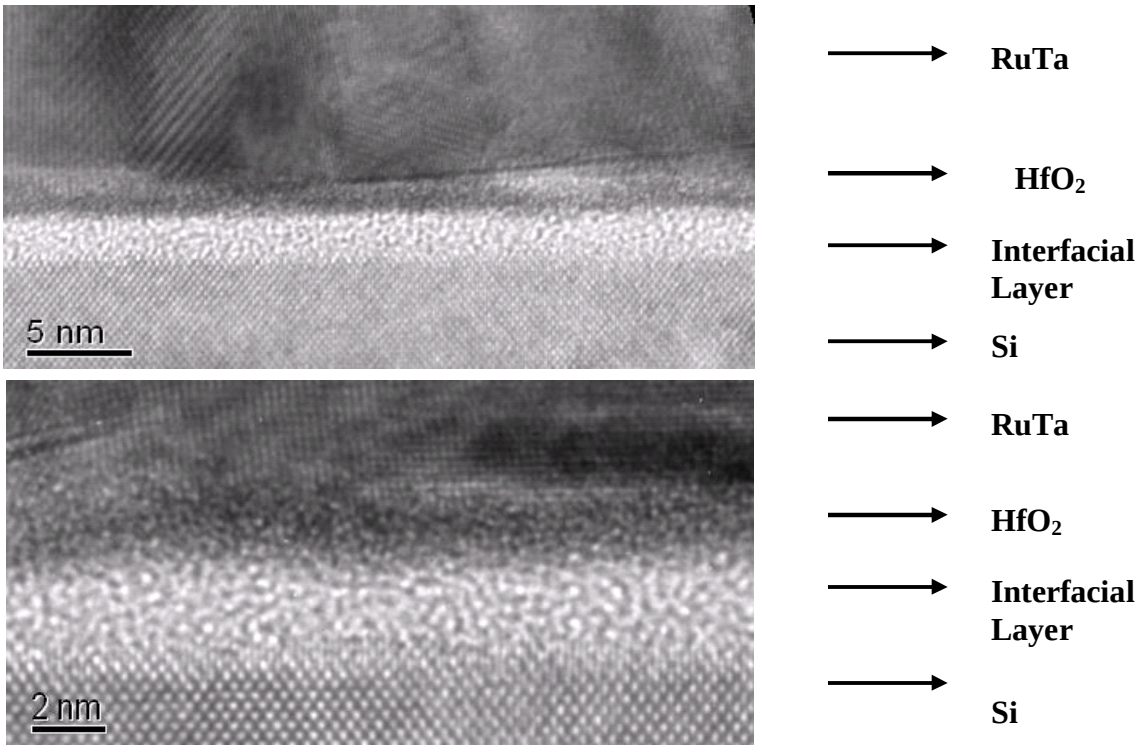



**Figure 2. 28 TEM picture at 400°C of RuTa on HfO$_2$**

# *Chapter 3* Role of the capping layer of Metal Electrodes

## 3.1 Introduction

Many of the gate electrode properties may be influenced by the ambient conditions like the presence of oxygen and its diffusion through the metal gate. The latter in turn will depend on the transparency of the metal gate for oxygen diffusion. The extent of oxygen diffusion through the metal gate may be responsible for the observed physical and electrical properties of the gate stack. It is therefore important to investigate the role of oxygen on the properties of gate stack in terms of change in equivalent oxide thickness (EOT) and flatband voltage ($V_{FB}$). Besides oxygen diffusion, high work function metals, such as Ru, high-k dielectrics can suffer from adhesion problem at high temperatures when placed on dielectrics such as $SiO_2$ or $HfO_2$. This is attributed to the weak bonding of the metal with the oxygen in the dielectrics. Furthermore, differences in thermal expansion coefficient can also lead to adhesion issues at higher temperatures. Capping layer is a potential route in suppressing this adhesion problem if the direction of the stress from the capping can compensate the stress from the underlayer. For the aforesaid reasons, the role of capping the Ru metal gate with another metal was investigated in detail. The effect of such a capping layer on gate electrodes is discussed in terms of the merit and issues that may be involved in the integration of such gates stacks. There are several criteria that guide the selection of the capping layer. The resistivity of the capping layer is a critical parameter. Proper choice of low resistivity material for the capping layer or sustaining low level of resistivity for the top layer of metal gate is important for integration of the entire metal gate electrode stack device. Many metals, under any kind of temperature treatment, undergo surface oxidation presenting severe contact resistivity for the top contact. The resistivity of most metal films is in the

range of 3Ω.cm to 100Ω.cm. For tungsten, the resistivity is $5.60 \times 10^{-8}$ Ω m, ruthenium $7.1\times 10^{-8}$ Ω m, and tantalum $15.52\times 10^{-8}$ Ω m each in case of the bulk resistivity. However, the resistivity of metal nitrides is usually two or three orders of magnitude higher than that of elemental metals, as resistivity of TaN is $252\times 10^{-8}$ Ω m. The resistivity of intrinsic conducting metal oxides is in the range of the metal counterpart.

As was mentioned earlier in this chapter, the role of the capping layer as an oxygen barrier is also important. If some amount of oxygen diffuses to the gate dielectric through the metal gate electrode, then the interface can be oxidized making the EOT higher and changing the effective work function and thus the threshold voltage. The increase of oxygen content of the films also tends to increase the bulk resistivity of the films resulting from more grain boundary scattering. It has also been shown that oxygen at the metal gate and dielectric interface can modify the metal gate work function due to the formation of interface dipoles and/or reactions layers [2, 3]. Therefore, control of oxygen diffusion through capping layers is a critical concern. Even if the capping layer is effective in blocking oxygen diffusion, it may get oxidized on the surface especially after a high temperature anneal. Furthermore, the metal comprising the capping layer can itself diffuse through underlying electrode layers under high thermal budget. Finally, the level of stress can increase total amount of stress and result in more exaggerated adhesion issues. High temperature stability of the capping layer is also critical to attain.

As mentioned above, the capping layer is a critical part of the gate stack, however, its impact on final device properties is not well understood. This chapter will present results on the effect of the capping layer on Ru and/or RuTa alloyed gate stack electrodes device.

## 3.2 Experimental

Thermally grown $SiO_2$ at 900°C with thicknesses ranging from 30–120 Å were used as gate dielectrics. Ru gate electrodes were deposited at 100 W in a RF magnetron sputtering system. An *in-situ* 600~1200Å W capping layer was deposited by sputtering W on single layered Ru gates. W was chosen as capping layer since it is refractory metal with high melting point, easily deposited and easily contacted even after high temperature anneals. Thick Ru layers (~900Å) without any W capping suffered from significant adhesion issues and most of these films peeled off. Due to this problem, no comparison of such gates with their capped counterparts (stack Ru/W) could be made at high temperatures.

All samples were subjected to a forming gas anneal (FGA) at 400°C for 30 minutes prior to characterization. To evaluate the thermal stability, the samples were subsequently subjected to a rapid thermal anneal (RTA) in Ar at 900°C for 30 seconds and 1000°C for 30 seconds. Auger Depth Profiling was performed to understand the diffusion behavior under as deposited and high temperature anneals conditions of the gate stack. Capacitance-voltage (C-V) characteristic were obtained using HP4284 LCR meter and HP4155, respectively. The flatband voltage ($V_{FB}$) and the EOT for the capacitors were obtained by using the NCSU CV program [4].

## 3.3 The effect of the capping layer: Ru vs. Ru/W stack

Figure.3.1 shows the C-V curves of the capacitors for the Ru gates 900Å and the Ru gate 200Å with 600Å capping layer of the tungsten (Ru 200Å / W600Å) after a forming gas anneal at 400ºC for $SiO_2$ thickness of 3, 6, 9 and 12nm.. Flat band voltages of Ru 200Å /W 600Å gate stack showed more negative values than those of Ru 900Å gates. The observed

lower $V_{FB}$ for the capped Ru stack can be attributed to either a different effective work function at the interface of Ru and $SiO_2$ for the capped films or a difference in work function associated with stress profile changes. It should be noted that oxygen profile is expected to be quite different between the two samples since the forming gas anneal furnace does contain a significant amount of oxygen which can easily diffuse through the large grain boundaries of Ru films for the uncapped Ru samples but get trapped within the W films for the capped samples. We have previously shown that W films can easily get oxidized at the surface in the forming gas anneal as shown in Figure 3.2. This point will be discussed further in this chapter.

Thickness of Ru was changed from 200Å to 900Å to see if there was any effect of Ru thickness on the work function. In order to decouple the effect of fixed charge from the work function, C-V measurements on several oxide thicknesses were used to generate a flat band voltage vs. EOT curve. The work function is extracted from the y-intercept of this curve [6]. Figure 3.3 shows the flat band voltage vs. EOT extracted from the CV curves for uncapped Ru films after a forming gas anneal at 400ºC and capped Ru gates (Ru/W:200-700Å/600Å) on $SiO_2$ after a forming gas anneal at 400ºC. Capped Ru gates (Ru/W:200Å/600Å) show a lower work function than uncapped Ru films even at 400$^{o}$C. Work function of capped Ru after FGA is 4.90eV, whereas that of uncapped Ru was 5.11eV As will be discussed in further detail, it is proposed that the reduction in work function of the capped samples is directly related to the oxygen content at the Ru-$SiO_2$ interface. When uncapped Ru samples are taken out from forming gas anneal furnace, they are still very hot and easily absorb oxygen from exposed air. Oxygen from the FGA process can diffuse through the large grains of Ru films and accumulate at the Ru-$SiO_2$ interface creating an

abundance of Ru-O bonds which gives high work function associated with Ru-O. However, for capped samples, the W layer on top blocks/absorbs the oxygen from the annealing ambient hence not allowing oxygen accumulation at the Ru-$SiO_2$ interface. This results in a lowering of the work function. Some oxygen that is present on the surface of indicating uncapped Ru has enough amount of oxygen to make Ru-O bonding to make higher work function. Negligible change in EOT was also observed after FGA for uncapped Ru films compared to their capped.

Figure.3.4 shows the C-V curves of the capacitors for Ru capped and uncapped samples after an annealing at 1000ºC in Ar ambient. As was mentioned earlier, the uncapped Ru samples suffered from peeling and hence data at 1000$^{o}$C could not be obtained. For reference, the data after FGA is displayed instead. The data for the capped samples consists of Ru gates of 200 Å with 600 Å capping layer of the tungsten which were subjected to a forming gas annealed at 400$^{o}$C followed by an annealing at 1000ºC in Ar ambient. The Ru 200 Å gates with 600 Å capping layer of the tungsten after anneal at 1000ºC show more negative values than Ru 900 Å gates at 400$^{o}$C. Thickness of Ru and W was changed 200Å-900Å and 600Å-1200Å, respectively, to see if there was any effect of Ru/W thickness on the work function. After 1000$^{o}$C anneal, 1200Å W capped sample and Ru 900Å suffered from peeling and hence data at 1000$^{o}$C were not be acceptable. It will be discussed further in detail.

Figure 3.5 shows the flat band voltage vs. EOT extracted from the CV curves for uncapped Ru films after a forming gas anneal at 400ºC and capped Ru gates (Ru/W:200-700Å/600Å) on $SiO_2$ after a forming gas anneal at 400ºC and a subsequent anneal at 1000ºC in Ar. Capped Ru gates (Ru/W:200Å/600Å) show a lower work function than uncapped Ru

films even at 400°C as shown in Figure 3.5(a). Work function of capped Ru after FGA is 4.90eV, whereas that of uncapped Ru was 5.11eV. Negligible increase in EOT was also observed after FGA for uncapped Ru films compared to their capped counterparts. The capped films suffered from 1~3Å EOT growth after 1000°C. This is attributed to the diffusion of oxygen from the W film (which was incorporated there during the FGA) down to the Si substrate when annealed at 1000°C. Figure 3.6 shows the AES depth profile of Ru (700Å)/W(600Å) gate stack with the capping layer of the tungsten on $SiO_2$ after 900°C anneal and a subsequent 1000°C anneal with the pre-forming gas anneal at 400°C indirectly indicating that some amount of oxygen was detected even in the Ru film.

The source of oxygen does not have to be only the W layer. Other sources of oxygen at high temperature include the outside ambient and even oxygen located within the gatestack. For e.g., the Ru-O bond could also be reduced by the Si substrate, especially at high temperatures, causing oxygen to move down to the Si substrate. The reduction of Ru-O by Si is thermodynamically favored due to the low Gibbs free energy of Si-O bond (-1000kJ/mol at 900°C) as compared to the Ru-O bond(-427kJ/mol at 900°C) in Ru-Si-O system. Also W-O bond is also thermodynamically favored due to the low Gibbs free energy of W-O bond as compared to the Ru-O bond. As discussed previously, it is proposed that the reduction in work function of the capped samples is directly related to the reduction in the oxygen content at the Ru-$SiO_2$ interface. $RuO_2$, the most stable form of Ru oxide, becomes less stable and Ru-O bonding is easy to be broken at elevated temperature. At high temperatures, the capped films suffer from further reduction of the Ru-O interface causing a bigger reduction in the work function and the W layer on top blocks/absorbs the oxygen from the anneal ambient hence not allowing oxygen accumulation at the Ru-$SiO_2$

interface. In addition to this, W as a capping layer and W that has diffused through Ru as shown in AES results can also be attractive source for oxygen as shown in Figure 3.7. This results in a further lowering of the work function. Some Ru-O bonding that is present on the surface of the $SiO_2$ at lower temperature is decomposed at elevated temperature. However, at 1000$^oC$, another cause for reduction in work function could be intermixing of Ru and W films as shown in Figure 3.5

Figure 3.8 shows the I-V curves of the Ru gate 200 Å with 600 Å capping layer of the tungsten on $SiO_2$ (EOT : 82Å ) after anneal at 400°C and 1000°C. The gate current decreased after 1000$^oC$ anneal and curves showed clearly different shapes. Values of barrier height for samples at 400$^oC$ are 3.1eV and 3.5eV at 1000$^oC$. The reduction in current could be attributed to increase in EOT or increase of Barrier height.

However, as shown in Figure 3.9, the Ru gate 700 Å with 600 Å capping layer of the tungsten on $SiO_2$ (EOT : 83Å ) shows similar gate current at both temperatures with a barrier height of 4.1eV after anneal at 400°C and 4.2eV after anneal at 1000°C. The gate current decreased after 1000$^oC$ anneal and curves showed clearly different shapes. Combination of thickness of Ru and the capping layer of the tungsten is important since thick enough Ru film for protecting from the tungsten diffusion at high temperature and low enough thickness of the capping layer could suppress adhesion problem of Ru gate on $SiO_2$.

Auger Electron Spectroscopy (AES) depth profiling analysis was performed to investigate the profile of the composition of Ru (700Å)/W(600Å) gate stack. AES depth profiling in combination with 3keV Ar+ ion sputtering was performed on part of the samples in order to detect the interfacial region between the alloy film and $SiO_2$. The AES depth profiling of the Ru gate with capping layer of tungsten film as deposited state is illustrated in

Figure 3.10. It clearly shows the abrupt interface composition change between W and Ru film.

In contrast to as deposited films, the AES depth profile of Ru (700Å)/W(600Å) gate stack with tungsten capping layer SiO2 after 400$^{o}$C forming gas annealed films is shown in Figure 3.11. A high intensity oxygen peak was easily detected, which indicates the considerable amount of oxygen content in the surface of the tungsten. As shown, approximately 200Å of the surface of capping layer tungsten has been oxidized after forming gas anneal even at 400$^{o}$C with about 60 percent of atomic concentration in oxygen. This is the reason that thickness of bottom layer need to have enough thick to be protected by significant diffusion and oxidation.

However, from the AES depth analysis, there is no obvious oxygen diffusion into the Ru film since there is not enough high thermal energy for oxygen to diffuse through Ru film. It indicates that if the tungsten film is used as a capping layer and then it is exposed at 400$^{o}$C forming gas anneal, some amount of surface can be easily oxidized. However, the amount of the oxidation is dependent on the temperature and time of the exposure to the post deposit annealing process because diffusion process is the function of the time and temperature.

The AES depth profile of Ru (700Å)/W(600Å) gate stack with the capping layer of the tungsten on $SiO_2$ after 900$^{o}$C anneal and a subsequent 1000$^{o}$C anneal with the pre-forming gas anneal at 400$^{o}$C in Figure 3.12 indicate that some amount of oxygen was detected even in the Ru film. Some amount of intermixing between the tungsten capping layer and the Ru gate is observed. Significant amount oxygen is detected in the Ru gate electrode after high temperature anneal. Also, the some tungsten diffuses through Ru gate electrode. However, it is not clear that there is a significant amount of the tungsten and the oxygen on the SiO2

interface from the diffusion at high temperature since Ru and SiO2 interface remains abrupt indicating negligible amount and the profiles of the tungsten and oxygen can be considered as tails from the AES depth profiling analysis.

Figure 3.13 shows the AES depth profiling analysis of Ru gate with W capping layer after 1000°C anneal without pre-forming gas anneal. Compared with the pre-forming gas annealed Ru with the capping layer of the tungsten, negligible oxidation of the W capping layer occurs even after 1000°C anneal. We attributed this observation as the primary reason that there was significantly different amount of incorporation of the oxygen into the tungsten between with and without pre-forming gas anneal followed by high temperature anneal. Some amount of inter-diffusion between the tungsten and Ru film was observed after 1000°C anneal without pre-forming gas anneal. However, the amounts of diffusion into Ru film rapidly decrease approximately at the point of 200 Å top of the Ru film.

It is well known that thin film may show features that are different from the bulk materials. For example, the elastic strength obtained in the thin films can be up to two hundred times as large as those found in corresponding bulk material. Thin films usually have s strong internal stress of $10^9$-$10^{10}$ dyne/cm$^2$ and this stress arises from the mismatch in the lattice parameter and the thermal expansion coefficient between the films and the substrates.

For use in an electrode application, good adhesion between the alloy film and the underlying substrate is critical for reliability. Even though it is of critical importance, adhesion is one of the least understood properties.

The adhesion of a film to the substrate is strongly dependent on the chemical nature, cleanliness, and the microscopic topography of the surface. The adhesion is better for

higher values of adsorption energy of the deposit and kinetic energy of the incident species. However, higher values of kinetic energy of the incident species may create more damage on gate oxide. Adhesion of the film can be improved by pre-coating with suitable materials but they can also affect the work function. Poor vacuum are less adherent than compact deposits.

From the gate integration and productivity point of view, it is good to have thinner metal gate to sustain lower step coverage for the metal gate electrode stack. When the thickness of the capping layer W increases to 1200Å, peeling has been observed in some samples. Also when the thickness of the Ru increases to 900Å, peeling phenomena has also been observed. This indicates that too thick of a capping layer could not effectively suppress the adhesion problem of Ru gate on $SiO_2$.

High stress values in the thin films can cause a film to migrate, crack and even peel off [19]. It is well known that the deposited films include internal stress during film growth. The elastic energy is stored in the films primarily due to the stress. The elastic energy density, $u_v$, is expressed by

$$u_v = \sigma^2/2Y \text{ (in J/m}^3\text{)} \tag{1}$$

where Y denotes Young's modulus of thin films.

Thus, the stored energy at the unit area of the films, $u_s$, becomes

$$u_s = u_v d = \sigma^2 d/2Y \text{ (in J/m}^3\text{)} \tag{2}$$

where d shows the thickness of the deposited films. When $u_s$ is larger than the adhesive energy, the deposited films will peel off. Under a given adhesive condition, there

is a critical film thickness. Beyond the critical thickness, the deposited films will peel off. The internal stress originates mainly from adhesion to the substrates. Stress can be introduced in the films and/or lattice misfit with substrates. All films are found to be stressed internally even without the application of external forces. The mechanical behavior of films cannot be considered apart from the substrate to which they are attached. Thus, sources of internal film stress include both the mismatch in thermal coefficient and mismatch in lattice parameter between film and substrate. For these reason, properties of capping material W and $SiO_2$ as well as Ru are needed to be studied. Lattice parameter of W (bcc structure) is ~3.17Å and that of Ru (hcp structure) is ~2.71Å and ~4.28Å for a- and c-axis, respectively. Lattice parameter of RuTa is expected between that of Ta, ~3.30Å and that of Ru. Thermal expansion coefficients of W and Ru are $4.5x10^{-6}/^{o}K$ and $6.4x10^{-6}/^{o}K$, respectively. Since that of Ta is $6.3x10^{-6}/^{o}K$, the value of thermal expansion coefficients of $Ru_xTa_y$ alloy is expected 6.3~6.4 $x10^{-6}/^{o}K$. However, the value of thermal expansion coefficients of $SiO_2$ is $\sim 5.5x10^{-7}/^{o}K$. Those factors mentioned above influence overall internal stress. Furthermore, residual stress might be expected to be increased as the melting point of the film increases. Thermal stress, by Hooke's law, can be expressed by $\sigma = Y\alpha(T-T_0)$ where $Y$ is Young's modulus and $\alpha = \Delta l/l_0$ ($K^{-1}$). This expression can be extended to volume change. When a film attached to a substrate strains differentially relative to it, similar thermal stresses arise due both to differences in thermal expansion coefficient ($\alpha_1$-$\alpha_2$) and temperature. The film stress changes in response to the thermal strain applied by the difference in coefficients of thermal expansion between Si and the Ru.

It is known that the stress in sputtered metal films appears to be 2-3 times higher than for evaporated metals. It is known that the generalization with respect to stress for sputtered

films is very difficult because of the complexity of the plasma environment and deposition process. However, for Ru and Pt, intrinsic tensile stress is mainly observed and this type of stress is associated with island impingement and coalescence [20, 21]. It is reported that as the Ru film grew, tensile stress increased. The reason is that tensile stress is built up in Ru film without the release of stress due to low atomic mobility. This means that stress buildup occurred rather than stress release. In contrast, compressive stresses are reported in sputtered W with low Ar pressure [20]. Since the signs of the stress from Ru and W are different, W can reduce overall strain from compensated stress.

When the thickness of the capping layer W increases to 1200 Å, some peeling was observed indicating too much compressive stress was involved. This indicates that too thick capping a layer could not effectively suppress the adhesion problem of Ru gate on $SiO_2$. Also when the thickness of the Ru increases to 900 Å with W capping layer 600A, peeling was also observed. This indicates when Ru thickness thicker than some critical thickness that can be suppressed by compressive stress W 600A, the tensile stress of Ru is believed to make peeling in this gate stack system.

Surface morphology was imaged using a Digital Instruments Dimension 3000 in an intermittent-contact mode. The atomic force micrography (AFM) was performed in a vibration-shielded hood to improve image quality. The cantilever probes were *c*-Si with a nominal tip radius of 5–10 nm. The AFM analysis was performed to study surface morphology and analyze surface roughness comparison of the capping layer and its oxide to compare before and after the effect of the high temperature anneal. The areas examined were 5 x 5 $\mu m^2$, and the images were post-processed using a flattening algorithm. Figure.3.14 (a) shows the AFM image of before high temperature anneal with post-forming

gas annealed Ru with W capping layer and the surface has a uniform microstructure and a smooth surface. Figure.3.14 (b) shows after annealed film at 800$^{o}$C for 10min with post-forming gas annealed Ru with W capping layer. After high temperature anneal, the surface of W becomes more non-uniform with a rougher. It is apparent that the surface of the capping layer of W film is strongly affected by the annealing condition, which leads to significant grain size growth. The extracted Root Mean Square (RMS) surface roughness before high temperature anneal was 0.441 nm. The RMS roughness of after high temperature anneal was 6.626 nm. Therefore, the high temperature annealed capping layer films exhibit roughness one order higher value than that of non-annealed one. It attributed to more oxidation and some amount of Ta out-diffusion and oxidation. This is also consistent with the AES analysis.

## 3.4 Summary

In this chapter, the effect of the capping layer on the top of the gate electrodes was discussed. Different thickness of Ru with the capping layer of the tungsten was used. The observed lower $V_{FB}$ for the capped Ru stack can be attributed to either a different effective work function at the interface of Ru and $SiO_2$ for the capped films or a difference in work function associated with stress profile changes. The uncapped Ru and thick W capping samples suffered from peeling after 1000$^{o}$C anneal. It was shown that gate electrode with capping layer needs to be thick enough or protected from the diffusion for high temperature stability. AES depth profiling shows that significant amount of the oxygen or tungsten can diffuse into film. However, the amount of diffusion depends on underlayer, overlayer and the history of heat treatment.

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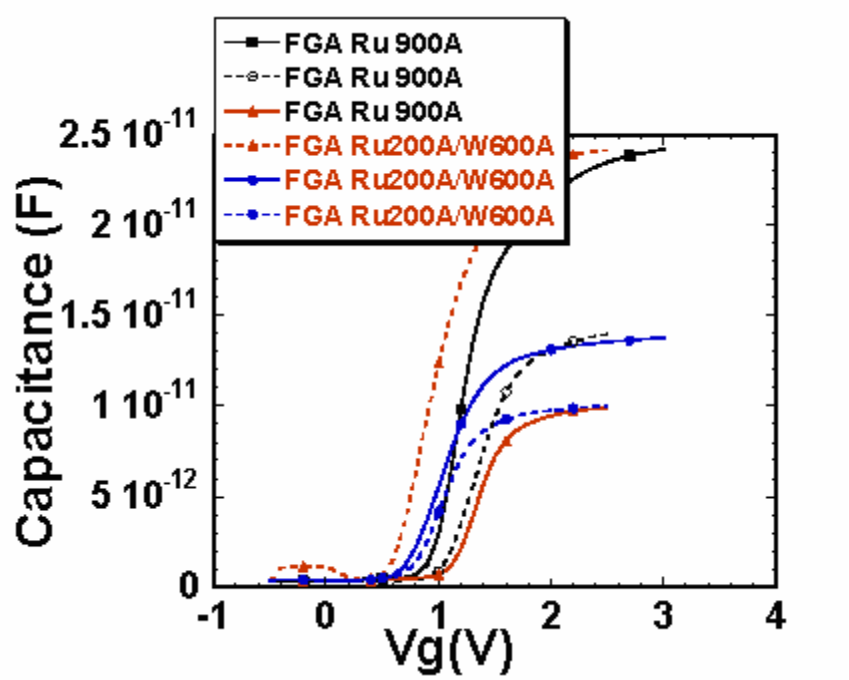



**Figure 3. 1 C-V curves of Ru 200A with W 600A films and Ru 900A film on $SiO_2$ forming gas annealed at 400°C**

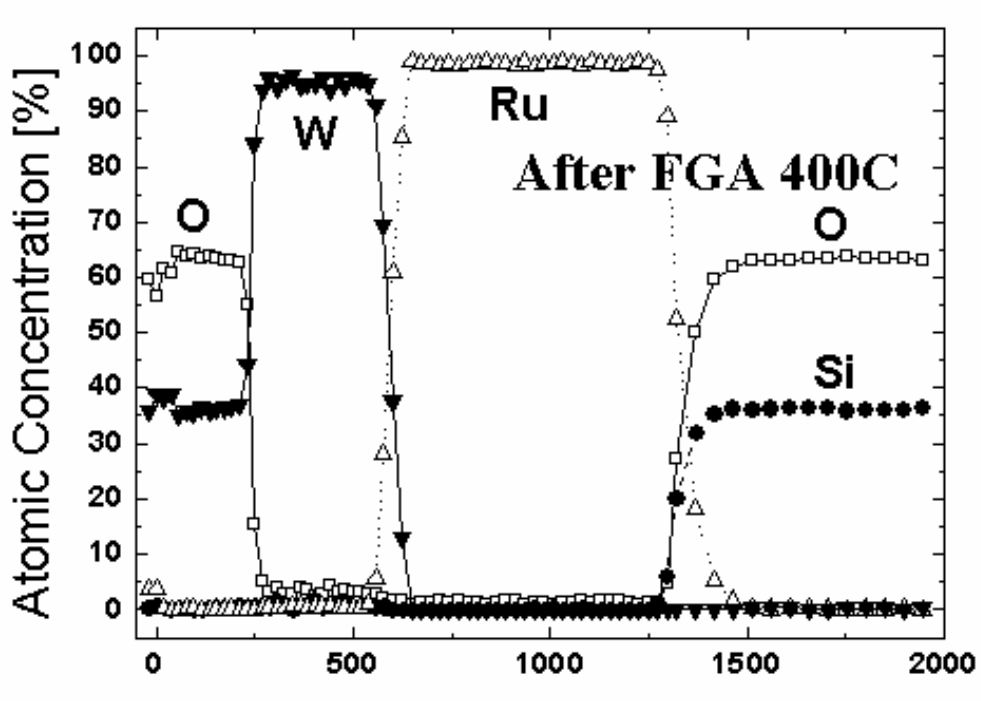



**Figure 3. 2 AES depth profile of Ru 700A with W 600A films on $SiO_2$ after forming gas anneal at 400°C**

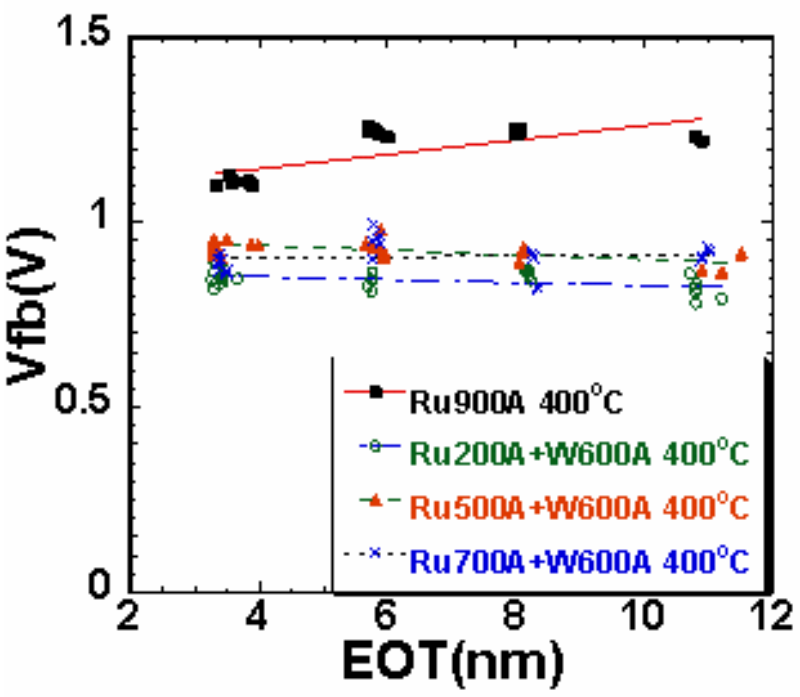



**Figure 3. 3 VFB vs. EOT for various metal stack conditions FGA at 400°C**

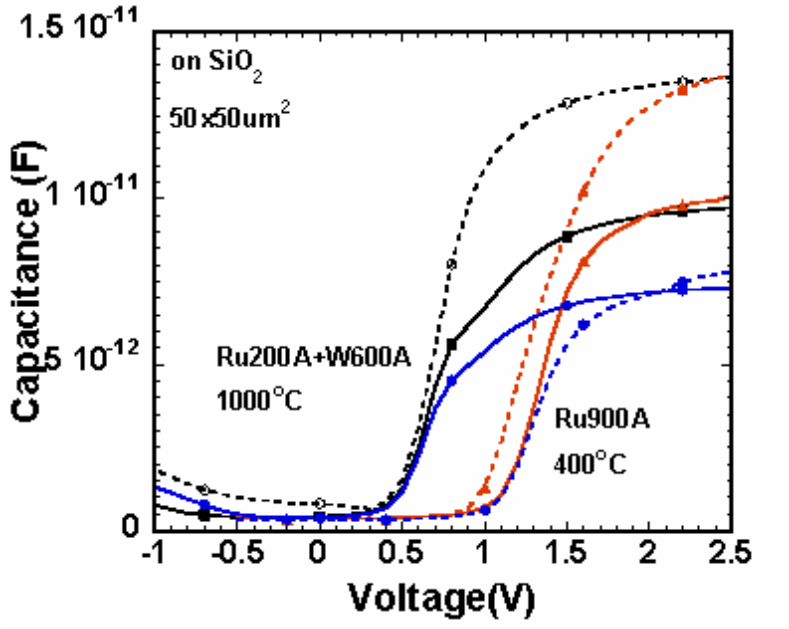



**Figure 3. 4 C-V curves of Ru 200A with W 600A films on $SiO_2$ annealed at 1000°C with pre-FGA at 400°C and Ru 900A film forming gas annealed at 400°C**

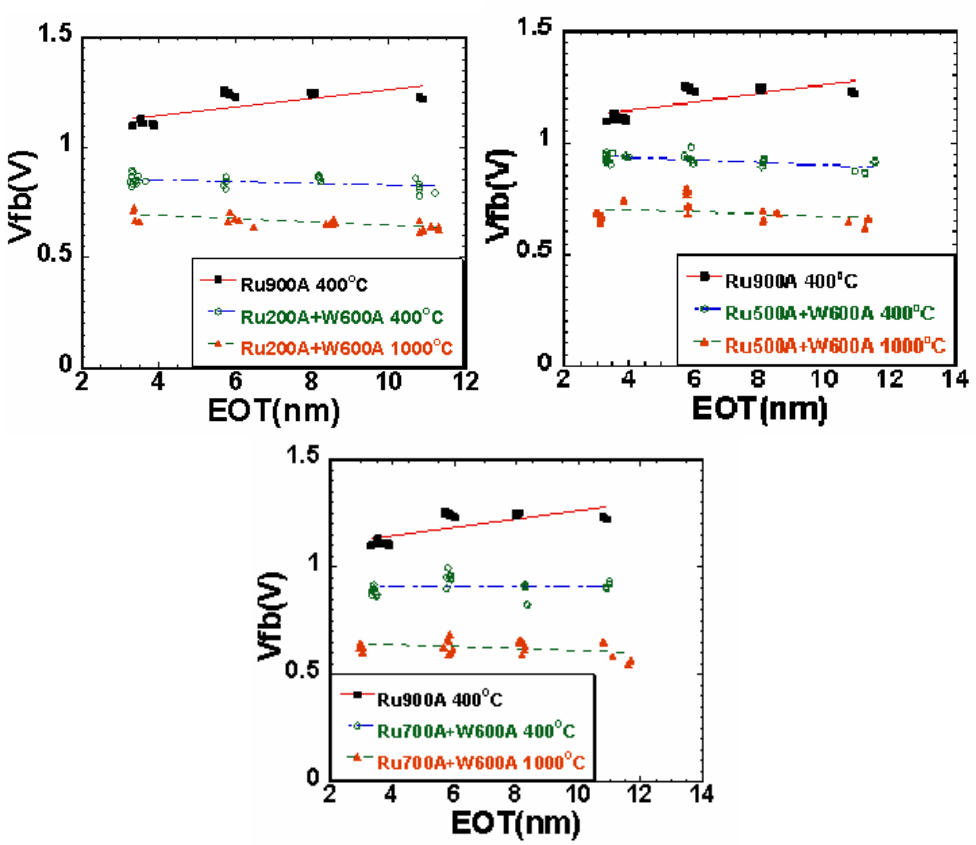



**Figure 3. 5 Vfb vs. EOT for various metal stack conditions FGA at 400°C and subsequent 1000°C anneal in Ar.**

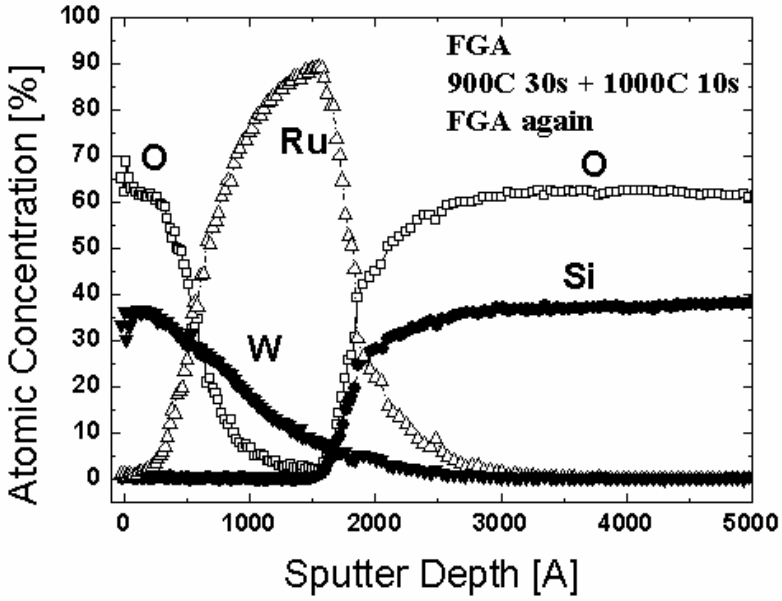
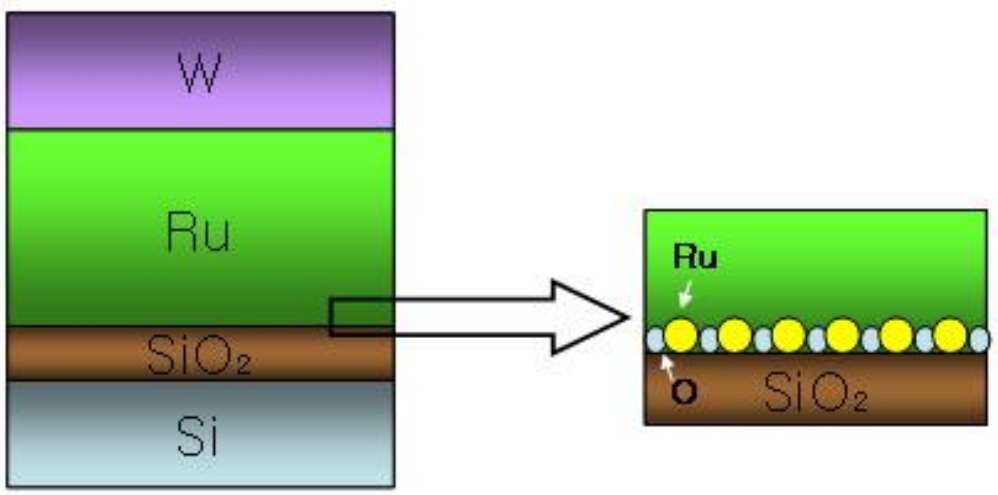
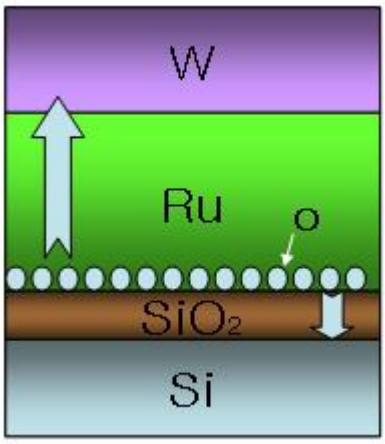



**Figure 3. 6 AES Depth profile of Ru 700A with W 600A films on $SiO_2$ with pre-FGA at 400°C and subsequent 900°C and 1000°C anneal in Ar followed by FGA at 400°C. Shows how much oxygen diffuse Ru film at high temperature**




**(a) at low temperature**




**(b) at high temperature**

**Figure 3. 7 Schematic of proposed work function change at low and high temperature**

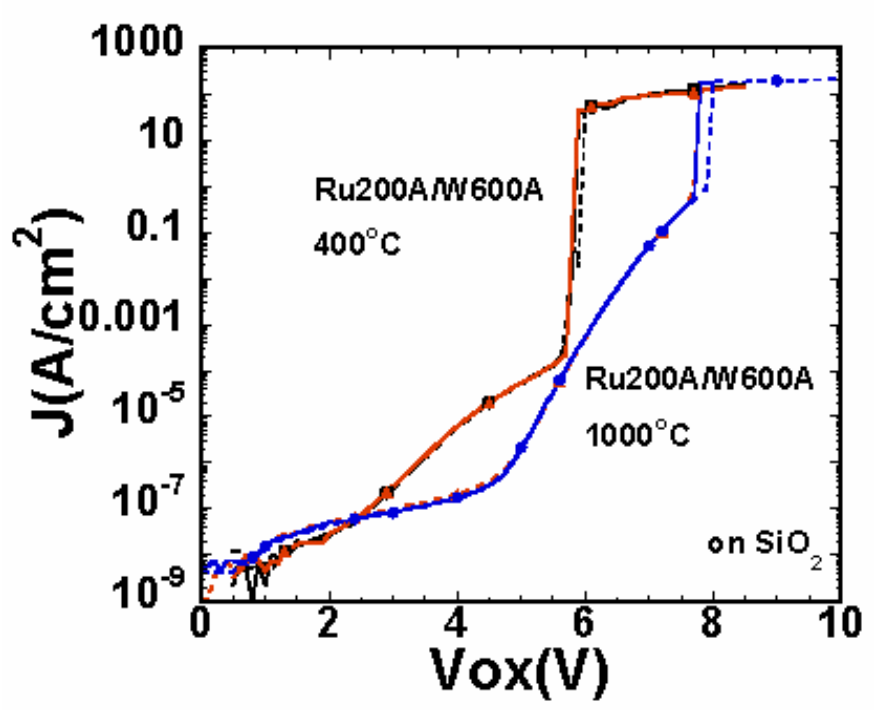



**Figure 3. 8 I-V curves of Ru 200A with W 600A films on $SiO_2$ annealed at 400°C and at 1000°C**

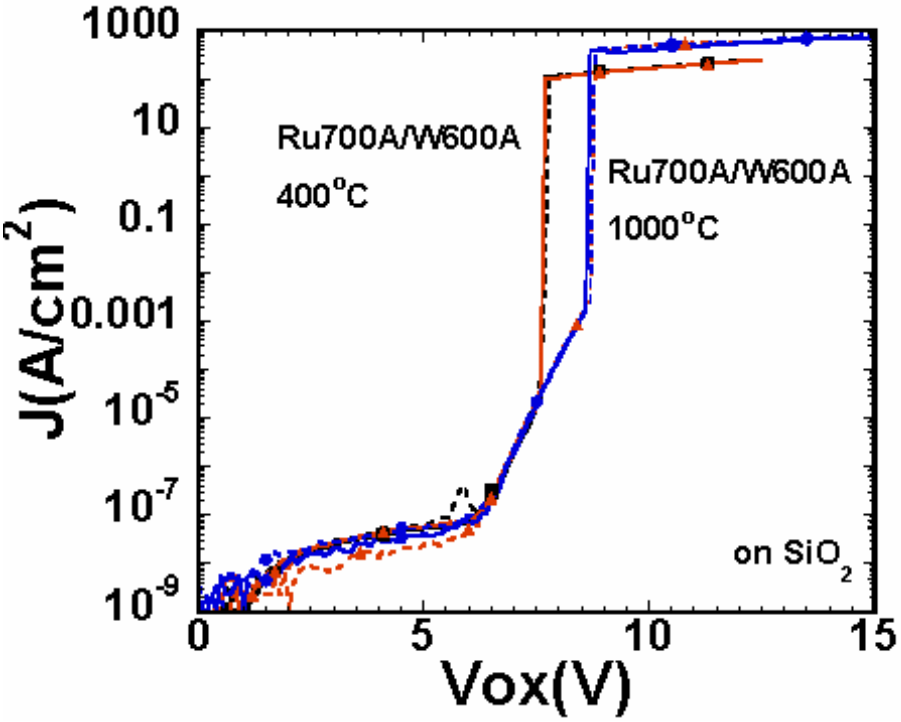



**Figure 3. 9 I-V curves for Ru 700A with W 600A films on $SiO_2$ with FGA at 400°C and 1000°C anneal in Ar.**

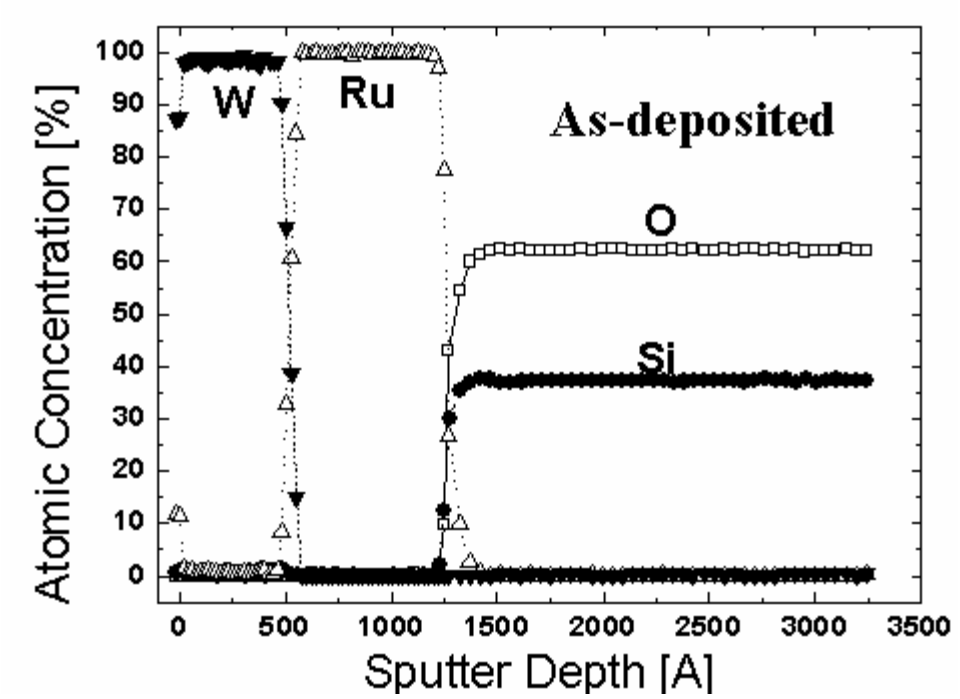



**Figure 3. 10 AES Depth profile of as-deposited Ru 700A with W 600A films on $SiO_2$**

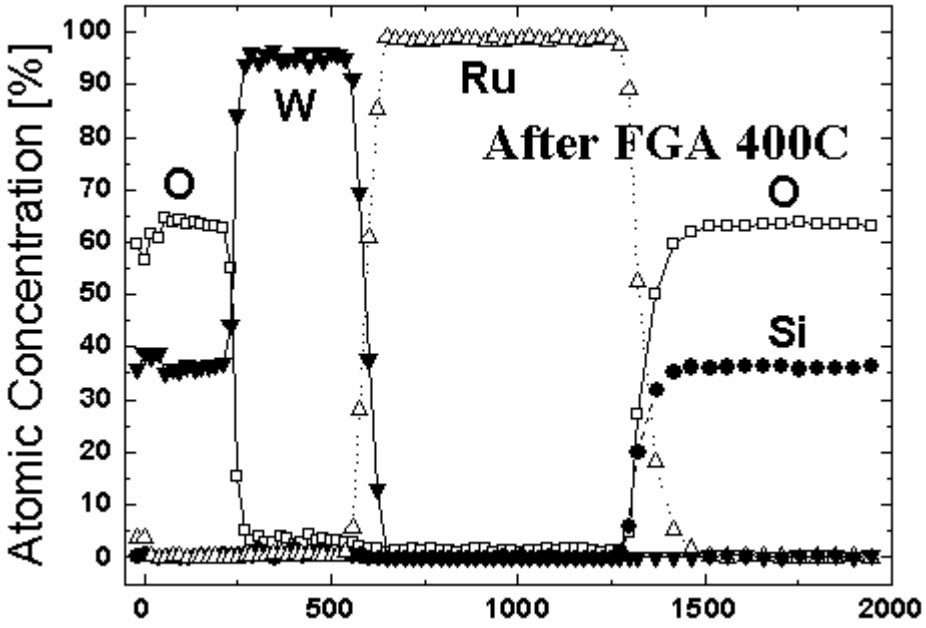



**Figure 3. 11 AES Depth profile of Ru 700A with W 600A films on $SiO_2$ forming gas annealed at 400$^{o}$C**

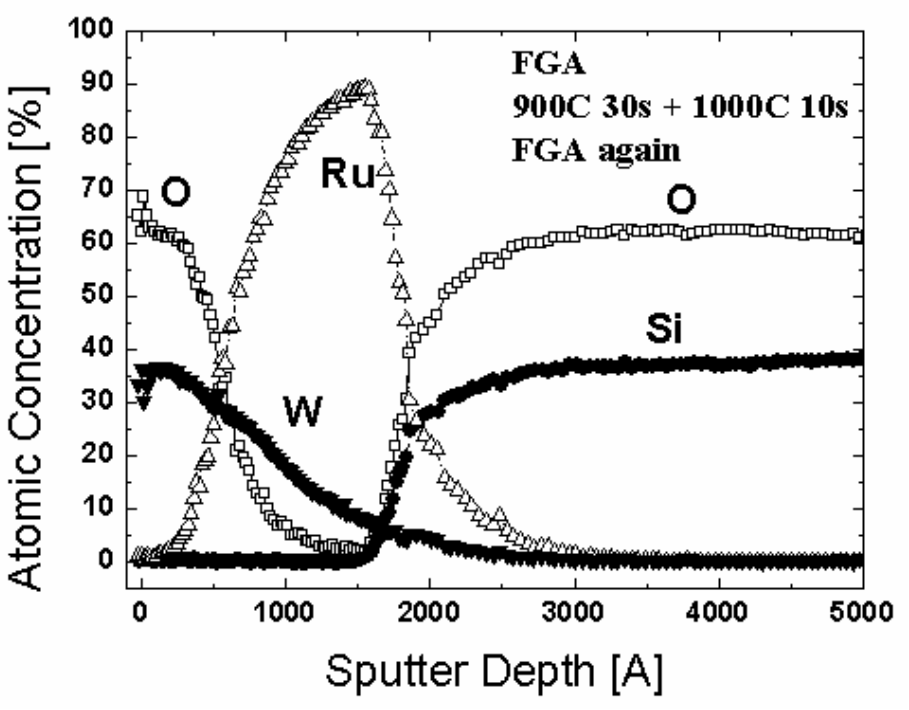



**Figure 3. 12 AES Depth profile of Ru 700A with W 600A films on $SiO_2$ with pre-FGA at 400°C and subsequent 900°C and 1000°C anneal in Ar followed by FGA at 400°C**

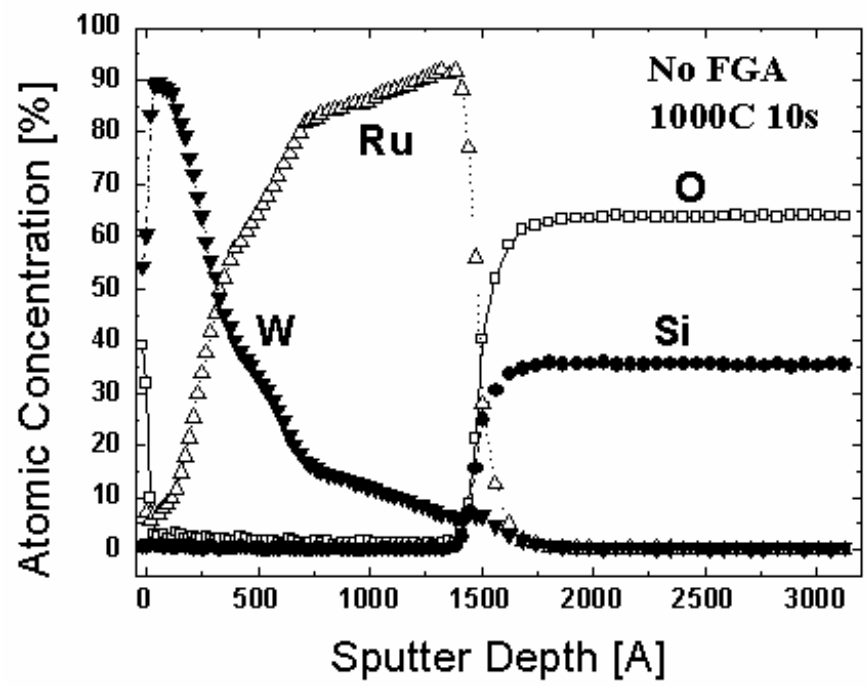
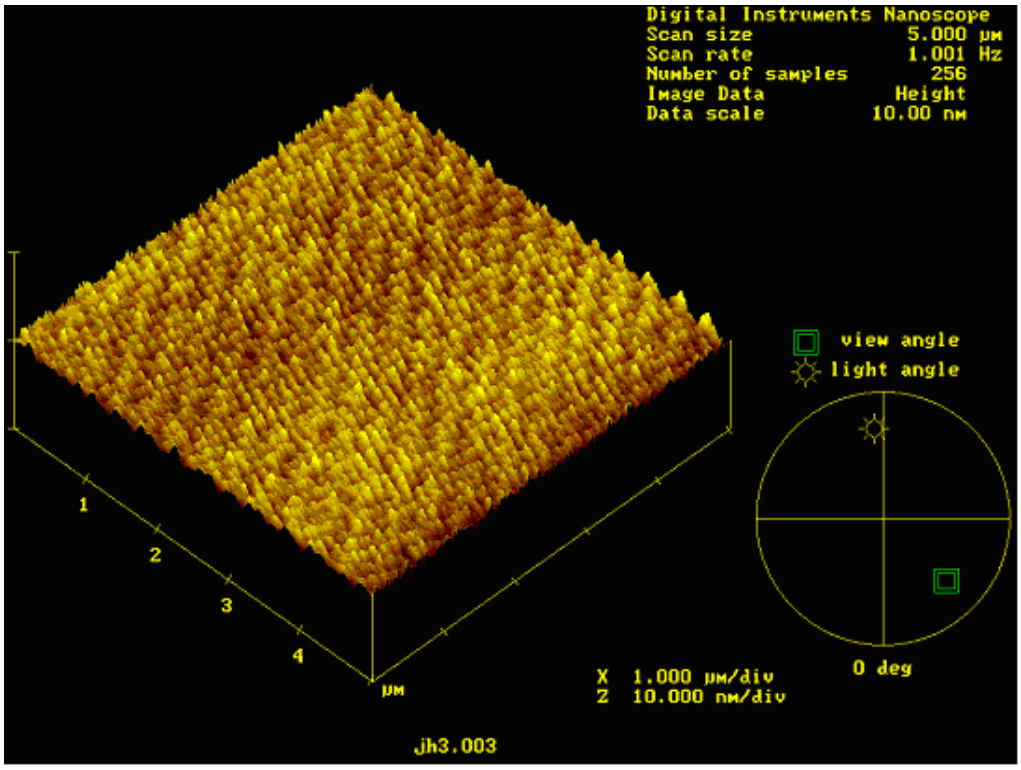
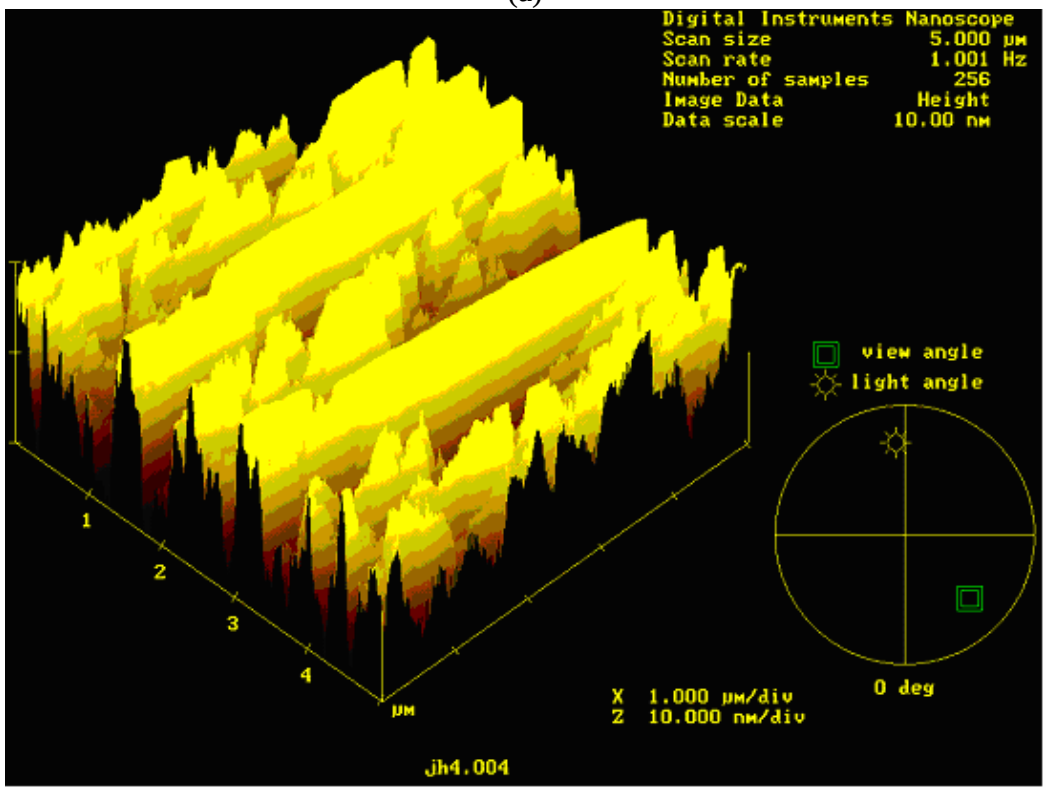



**Figure 3. 13 AES Depth profile of Ru 700A with W 600A films on $SiO_2$ without pre-FGA and subsequent 900°C and 1000°C anneal in Ar.**




(a)




(b)

**Figure 3. 14 AFM surface scans Ru 700A with W 600A films with pre-forming gas anneal at 400°C: (a) before anneal at 800°C for 10min. in Ar: RMS ~ 0.441 nm**

# *Chapter 4 Tunable Work Function Approach Via Bi-layer Metallic Gate Electrodes*

*In this chapter, a tunable work function dual metal gate technology approach will be discussed as potential gate electrode candidates for P-MOSFET and N-MOSFET devices.*

## 4.1 Introduction

As mentioned in Chapter 1, CMOS technology beyond the 45 nm technology node will require need new materials and process integration. Furthermore, many of these materials being considered for the MOSFET gate stack will need novel process integration techniques. This chapter introduces a new process integration route for deep sub-micron CMOS transistors as well as in searching for alternative gate electrodes.

The use of metal gate electrodes instead of the conventional polycrystalline silicon electrodes is one of the main gate stack challenges. One of the major challenge facing metal gate electrodes is a method that allows the metal gate work function to be tuned over the required range to get gate work functions for N-MOSFET and P-MOSFET devices on a single silicon substrate.

One of the most important properties of the gate electrode is the effective work function at the dielectric interface. The most direct impact of the gate electrode on the operation of a MOSFET is through its control of the device threshold voltage ($V_T$). The voltage required for the onset of inversion in the MOSFET channel is determined by the work function in the gate electrode. The threshold voltage of a MOSFET is typically given by the following expression:

$$V_T = V_{FB} + 2f_B + \frac{\sqrt{2qN_A e_S 2f_B}}{C_{OX}} \quad (1)$$

where $\varepsilon_s$is the permittivity of Si, $q$ is the electronic charge, $N_A$ is the dopant concentration in the channel, $\phi_B$ is the band bending in the Si substrate and $COX$ is the oxide capacitance.

The threshold voltage of the transistor of a MOSFET is dependent on the work function of the gate electrode. The flat band voltage is across the MOS stack and is applied on the gate electrode that eliminates any band bending across the stack. In the absence of interfacial and bulk charges, the flat band voltage is given by the following expression:

$$V_{FB} = f_{ms} - \frac{Q_O}{C_{OX}} \quad (2)$$

where $\phi ms$ indicates the work function difference between the metal gate and the Si substrate and $Qo$ denotes the magnitude of fixed charge in the oxide film.

The threshold voltage of the MOSFET is thus directly controlled by the gate electrode through the work function difference between the gate and the channel. The work function of the gate controls the threshold voltage of the device for inversion of transistor substrate to control how much applied voltage. It is desirable to have low and symmetric threshold voltages on the N-MOSFET and P-MOSFET for the CMOS [1-4].

It is crucial that the two gate electrodes have two different work functions to obtain low and symmetric threshold voltages on both P-MOSFET and N-MOSFET with reasonable short channel performance. The ideal gate work function of N-MOSFET and P-MOSFET for bulk-Si is ± 0.2 eV of the $E_C$ ($E_V$) of Si respectively. However, the ideal gate work function for ultra-thin body MOSFET is ± 0.2 eV of $E_i$, the intrinsic level for the Si. The

integration of tunable work function schemed metals on a single substrate will be important in future CMOS gate stacks [5-8].

In this chapter, the tunable work function dual metal gate technology will be discussed as gate electrodes for P-MOSFET and N-MOSFET devices. Capacitance-voltage (C-V) and current-voltage (I-V) results were obtained on metal-oxide-semiconductor capacitor structures. The flatband voltage and electrical dielectric thickness value extracted from C-V measurement after the thermal budget was monitored to evaluate the compatibility of the tunable work function dual metal gate technology gates.

In the first section, the electrical and material properties of the bi-layered metal gate process on $SiO_2$ dielectric are discussed in detail. The range of tunable work function values and ease of integration for dual metal gate process flow are investigated. Both Ru/Ta and $Ru_{50}Ta_{50}$/Ru stacks were investigated to maximize the increase in work function tunability. The stability of the dielectric under the bilayer intermixing was also investigated.

In the second section, the process of the Ru gates with the underlayer of very thin metal layer was investigated on the $SiO_2$ dielectrics for the PMOSFET. In this work, we discuss a metal gate process technology system that provides not only the approach to solve the adhesion issues but also obtain high work function on $SiO_2$ dielectrics.

## 4.2. Tunable work function dual metal gate technology on $SiO_2$ dielectric device

### 4.2.1. Introduction

Tunability of the work function is a very desired property since it allows for many devices to benefit from the same electrode system. Work function tuning has been

proposed in the past by work function alloy (RuTa), N implantation in Mo and Ni diffusion in Ti. There are some disadvantages of each approach.

*RuTa*: Since it's based on dual metal gate process, from the point of device integration, the incorporation of dual work function metals greatly increases the integration complexity because dual metal gates will most likely require extra photo step with two metal deposition steps. To avoid damaging the underlying dielectric of the region in which the 1st metal is removed, the deposition of the dielectric will accompany the second metal deposition. Another non-critical photo step will be needed to remove the 2nd metal and dielectric from the 1st metal region and planarization process like CMP may be needed to remove the dielectric. This results in a net two additional non-critical photo steps.

*N implantation in Mo*: It is expected that increased high temperature anneal leads to an enhanced segregation of N at the Mo interface, resulting in a lowering of the interstitial work function. Once the interface is saturated with N, further increase in the annealing temperature does not affect the work function.

*Ni diffusion in Ti*: Even though Ni and Ti interdiffuse very well, Ni is known as a very notorious diffusing metal at elevated temperature, and it is reported that Ni diffuses through even high-k dielectric at high temperature.

The proposed integration route in this chapter involves the deposition of a metal stack consisting of metals for NMOS and PMOS followed by the removal of the top metal from one of the well regions as shown in Figure 4.1. A reaction, either diffusion or intermixing, between the two metals can be controlled to produce a different work function compared to the region in which only the other metal exists.

Density of states differences between the two layers can also play a role however in the metals being considered here, the density of states is high for both metals. Various growth modes can be observed when the two metals are immiscible in each other. Even more complex modes observed when the two metals are miscible in each other. For e.g., substrate atoms can migrate into 2nd layer, surface energies can dominate alloy formation and metal-metal bond can results in large modulation of electrical properties.

In general, bilayer metals have depicted the following characteristics: a) Highest core-level shift observed for most stable bonds. The larger the electronic perturbations in the atoms, the stronger the bimetallic bond, b) Magnitude of core-level shift for an admetal increases when the fraction of empty states in the valence band rises (Ru<Ti<Al) and c) Core-level shift increases as the admetal d band occupancy increases (Ni: $4s^2$ $3d^8$ < Pt: $6s^1$ $5d^9$ < Pd: $4d^{10}$) The largest electronic perturbations are observed for systems that combine an admetal with an electron-rich d band and a substrate with an electron-poor valence band.

The factors that control the final work function depend on the thicknesses of each of the metals, the diffusivity of one metal into another, the order of the metals stacks and the dielectric stability underneath. It is reported that top surface metal layer with low work function has the effect of lowering the electrostatic potential for the image forces and thus is more feasible to form surface alloy. If this approach is now applied towards the gate electrode, then it is reasonable to expect that the $2^{nd}$ metal may impact the work function obtained observed by the dielectric.

Even though the integration of bi-layered metals as a gate is possible, several critical factors need to be considered to get the exact work function depending on the choice of the metals. Firstly, the degree of intermixing will depend on the solubility and diffusivity of

one metal into another. In our case, solubility of Ta in Ru is 20% and that of Ru in Ta is 35% at 900C, No diffusivity data of Ru in Ta and Ta in Ru are available. The resulting work function will depend on the degree of intermixing between the two metals. The thickness of each of the metals is also critical.

The value depends on the inter-diffusion coefficients, the thicknesses and composition of the two metal layers, and the intermixing ratio of each other. When A and B metal can inter-diffuse, the interface and its location depends on the diffusivity in each other metal. It's very difficult to predict the composition of interface, however, in general, the interface can be averaged composition of A+B.

If A metal can diffuse to B metal easier, A-B interface will be located at more B side. In case A-B interface will be located at more B side A) If thickness of B metal is enough thin, B side can be all interface, which can have averaged composition of A+B. B) If thickness of B metal is enough thick, B side can be interface + B metal. While the interface forms, A metal also can diffuse to more B side than interface. The amount of A metal diffusion depends on the thermal energy, diffusivity and solubility. In this case, final work function will depend primarily on thickness of B metals, total thermal budget, diffusivity of A metal in B metal. AES result shows that Ta and Ru intermix in each other easily since only after $900^{o}$C for 30sec, which will be discussed further.

Secondly, the top layer metal could also diffuse through the under-lying metal and segregate on the dielectric interface. This segregation is based on the enthalpy of mixing and the atomic size mismatch of A and B. Segregation behavior was reported in Nb/Ti/Cu system. After certain period of time, Cu segregates along with Ti on Nb. In this case, work function value relies on the segregated metal layer.

Net diffusion coefficient between over-layered metal and under-layered metal are the important key for this process. This segregation is based on the heat of solution of alloys and the atomic radii of A and B. When A-A and B-B bonding are more favorable than A-B and one of them has driving force to diffuse to the other, the segregation will be occurred. In other words, how many over-layered metal atoms can be efficient number of atoms through under-layered metal, segregation coefficient in over-layered metal in under-layered metal, the properties of the over-layered metal on the given dielectrics need to be considered.

Thirdly, the alloying of the two metals to form a binary alloy with a work function determined by the exact composition of the alloy. Another advantage of the bi-layer gate approach over the dual-metal gate approach is the protection of the gate dielectric at all times since the under-layered metal is always present to protect the dielectric, resulting less reliability problems. In order to choose which metal needs to be on the bottom, one needs to consider reactivity with underlying dielectrics, location of diffusion interface, diffusion behavior of each metal, adhesion of the underlying metal on dielectrics.

Finally, all the possibilities for obtaining the desired work function rely on the thermal budget. The temperature range of being annealed for the bi-layer gate and annealing time are also key factors of this integration process since all the coefficients depend on the thermodynamics.

The next section will describe the metal gate process, which provides tunable work function values and ease of integration for the dual metal gate process flow. Vertical stacks of Ru and Ta layers were subjected to high temperature anneals to promote intermixing which resulted in work function tuning.

In this work, we discuss a metal gate process technology that provides not only tunable work function but also simplifies the integration. We have previously shown that binary alloys of Ru and Ta provide a range of work function values (4.2eV to 5.2eV) that are thermally stable up to 1000ºC [12].

In this work, we propose an alternate means to achieve the work functions range of these alloys that also provides ease of integration.

The proposed scheme as shown in Figure 4.1(a) starts with deposition of Ru/Ta stacks. Next, the top Ta layer is removed from the PMOS regions via a non-critical photo step. High temperature anneals are performed to produce a Ru-Ta alloy on regions with vertical stacks. An alternate scheme is shown in Figure 4.1(b) starts with deposition of $Ru_{50}Ta_{50}$ alloy and then Ru as an overlayer. The top Ru layer is removed from the NMOS regions via a non-critical photo step. High temperature anneals are performed to produce a Ru-Ta alloy on regions with vertical stacks.

The resulting work function is expected to be strong function of the thickness and composition of the two layers. Although other metal gate integration schemes have been proposed [13,14], our approach offers the following advantages: a) a range of work function from 4.2eV to 5.2eV, b) avoids the use of N implantation and c) use of thermally stable metals that do not react with the underlying dielectric.

## 4.2.2. Experimental

The MOS capacitor fabrication process is summarized in Table 4.1. Ru and Ta stacks were sputtered on the thermally grown $SiO_2$ from Ru (purity of 99.95%) and Ta (purity of 99.95%) targets in a system with a base pressure of ~$3x10^{-9}$ Torr. Samples with

Ta on top were covered with W to enable ease of contact since exposed Ta easily oxidizes. W capping layer was chosen due to prior evidence of its stability with Ta [12]. The key sample conditions are listed in Table 4.2 and 2.3. C-V and I-V characteristics were obtained using HP4284 and HP4155B, respectively. The $V_{FB}$ and equivalent oxide thickness (EOT) for the capacitors were obtained using the NCSU C-V program [9].

### 4.2.3. Results and Discussion

Figure 4.2 shows the C-V curves of the capacitors for samples listed in Table 4.2 after a forming gas anneal at 400ºC. Only the Ru gate without a Ta overlayer displayed the expected Ru $V_{FB}$ value. The stacked Ru/Ta samples displayed $V_{FB}$ values that were more negative than pure Ru gates.

In order to decouple the effect of fixed charges and work function on $V_{FB}$, C-V measurements on MOS capacitors with varying oxide thicknesses were used to generate a $V_{FB}$ vs. EOT curve. The work function of the stacked Ru/Ta gates were determined using the flatband voltage vs. EOT relation as shown in Equation 3 assuming there are negligibly few interface states in the Si-$SiO_2$ system.

$$V_{FB} = f_{MS} - \frac{Q_f * eot}{e_{ox}} \qquad (3)$$

As shown in Figure 4.3, the work function can be extracted from the y-intercept of this curve. All stacked conditions exhibited linear behavior from which work function could be extracted. The work functions of the metal gate can also be extracted from the barrier heights of gate\SiO2 by using Fowler–Nordheim tunneling analysis. The Fowler–Nordheim current is given by

$$J_{FN} = A^* Eox^2 * \exp\left[-\frac{B}{Eox}\right] \quad (4)$$

The parameter A and B depend on the barrier height and the effective mass of the tunneling electron in the oxide. Eox is the electric field across the dielectric.

The effective barrier heights of Ru/Ta stacks at the metal-oxide interface via Fowler-Nordheim current analysis were obtained. The trend of barrier height shows similar trend as the change in work function of Ru/Ta stacks which was extracted from the C-V analysis. The extracted work function values from a $V_{FB}$ vs. EOT curve, which are correlated to barrier heights from Fowler-Nordheim tunneling analysis, (Figure 4.4) indicate some degree of intermixing/alloying of Ru and Ta at 400ºC.

Moreover, since the values of extracted effective barrier height of the stacks with Ru on the bottom as well as those of extracted work function from C-V exhibit larger change, the stacks with Ru on the bottom display a larger degree of intermixing compared to the stacks with Ta on the bottom.

It is attributed to the non-linear behavior of work function of varying Ru and Ta composition. As shown in Figure 4.5, change in the value of work function as a function of Ru composition when Ru is dominant, is lager than Ta is dominant. Even though there was some degree of intermixing/diffusion, majority atoms near dielectric which is more important to determine work function is from the bottom layer. In other words, Ru on the bottom has more Ru representing high Ru composition which shows lager work function change as a function of Ru composition than high Ta high composition which is from Ta on the bottom at this temperature.

High temperature anneals in Ar at 500ºC, 700ºC and 900ºC for 30sec and 1000ºC for 10sec were performed to further promote intermixing/alloying. For 700ºC anneal, the $V_{FB}$

values shift to the positive direction for the stacks with Ru on the bottom from 400ºC as shown in Figure 4.6. It also shows for the stacks with Ta on the bottom, the shift of the $V_{FB}$ values from 400ºC is negative and smaller than for the stacks with Ru on the bottom.

Fig.4.7 shows EOT stability of Ru 100A with Ta over-layer and Ta 100A with Ru over-layer under various high temperatures. The Ru gates with the over-layer of Ta have excellent EOT stability at high temperatures. However, it is shown that the EOT of the Ru gates with the under-layer of Ta increases as a function of temperature. Figure.4.8 shows I-V curves of Ta 100A with Ru overlayer on $SiO_2$ 50A after 900$^o$C anneal in Ar, indicating large leakage at high temperature attributed to $TaSi_2$ formation [11].

The $V_{FB}$ vs. EOT plots for sample #4 as shown in Figure 4.9 indicate parallel shifts as a function of temperature indicating a work function change. The work function values of all conditions as a function of anneal temperature are shown in Figure 4 10. As shown, the final work function of various gate stacks depends strongly on the thickness of the bottom and top layers and the anneal condition. Single layer Ru gates maintain their work function around 5eV after anneal. However, as the Ru layer on the bottom is made thinner with a Ta overlayer, the work function starts decreasing and saturates to ~4.6eV at ~900ºC, regardless of the Ru thickness.

This is either attributed to fast intermixing/alloying or decreasing the oxygen content at the Ru-$SiO_2$ interface at high temperatures. Intermixing is a key indicator of alloy formation as reported for alloys of Ru-Sm and Ru-Ag bi-layers [14]. In addition to this, an abundance of Ru-O bonds which gives high work function associated with Ru-O at low temperature.

However, the Ru-O bond could also be reduced by the Si substrate, especially at high temperatures, causing oxygen to move down to the Si substrate. as discussed previously. $RuO_2$, the most stable form of Ru oxide, becomes less stable and Ru-O bonds are easily broken at elevated temperature. At high temperatures, the films will suffer from further reduction of the Ru-O interface causing a reduction in the work function

Auger depth analysis, as shown in Figures.4.11 and 4.12, revealed significant levels of intermixing and inter-diffusion between the two layers after anneal although negligible inter-diffusion between the metal layers is observed in the as-deposited state. The Ru/Ta approach results in a work function decrease of ~0.4eV between Ru and Ru/Ta stacks.

For the case of Ta/Ru stacks, the work function starts increasing with temperature and with decreasing Ta thickness. However, even the work function for thick Ta layers increases owing to $TaSi_2$ formation and $SiO_2$ reduction [11]. This instability of Ta prevents the use of Ta/Ru stacks in this integration approach with Si containing dielectrics.

To further understand the degree of intermixing and alloy formation, in-situ XRD under heat treatments was performed in collaboration with Cyril Cabral of IBM. Figures 4.13 and 4.14 shows in-situ XRD analysis for the stacked layer of Ru 500A/Ta 100A on $SiO_2$, which is annealed at a constant temperature ramp rate of $3^oC/s$ from 100°C to 1100°C in forming gas anneal. During the anneal x-ray diffraction, sheet resistance and optical scattering were monitored. The intensity vs. 2θ plots are shown for (a) the as-deposited samples and after (b) the 1100°C anneal.

In addition, the contour plot of two theta vs. temperature with XRD intensity color coded (dark red highest intensity and dark blue lowest) and a plot showing normalized sheet resistance and optical scattering as a function of temperature are also included. Sheet

resistance as a function of temperature for a metal film should increase linearly and any deviation indicates a change in microstructure or phase.

In the as deposited samples, only a Ru (002) peak is present in the 2θ range from 20 to 60 deg., indicating strong texturing with minimal alloy formation. Examining the XRD and sheet resistance plots as a function of temperature at about 375$^{o}$C the intensity of the Ru(002) peak increases and the sheet resistance levels off. Both are an indication of possible grain growth in the Ru film. The next change observed is at about 820$^{o}$C, indicated by a increase in sheet resistance and a shoulder peak developing at lower 2θ off the Ru(002). This is attributed to the formation of the RuTa (101) phase. The possible RuTa (101) shoulder peak is also evident. The data suggests that the bilayer must be annealed above 820$^{o}$C before a reaction between the Ru and Ta takes place that can be detected.

Figure 4.15 and 4.16 shows in-situ XRD analysis for the stack of W 500A/Ta 200A /Ru 100A on $SiO_2$. The XRD shows the reflection from the W (110) peak. The W does not seem to react with the underlayers during the annealing and with its very high melting point there is just a small amount of grain growth.

Figure 4.13 shows a Ru (100) peak and a Ta (212) peak. During the annealing there appears to be two phases that form over the temperature range. The first occurs at 710$^{o}$C (one peak) and the last at 880$^{o}$C (two peaks). Both XRD and sheet resistance give indications to the phase formation sequence.

Figure 4.17 and 4.18 show XRD results for the stacked layer of W 500A/Ta 200A /Ru 70A on $SiO_2$. Again with this sample the probable alpha W (110) peak does not interact with the other layers during the anneal and undergoes a small amount of grain growth. As received are also the Ru(100) and beta Ta(212) peaks. The phase labeled 2 appears at about

770°C and phase 3 at 880°C (about the same temperature as the first sample) indicating phase formation depends on thickness.

Although the Ru/Ta stacks indicate a work function shift from pure Ru, the amount of shift is insufficient to meet the bulk CMOS requirements. It should be noted however that this shift may be sufficient for non-bulk devices. The main mechanism preventing a large work function decrease for the Ru/Ta stacks is believed to be the low Ta content of the resulting alloy and reduction of the Ru-O bond.

To overcome the limited range of work function tuning, an alternate approach utilizing $Ru_{50}Ta_{50}$/Ru stacks was investigated. Since $Ru_{50}Ta_{50}$ alloys have low work function values similar to the work function value of Ta but are also thermally stable [11] they can be utilized in the integration scheme of Figure 4.1(b) where the low workfunction layer is placed on the bottom. Table 4.3 lists the sample conditions evaluated.

Figure 4.19 shows the C-V curves of the capacitors for the $Ru_{50}Ta_{50}$ alloys with Ru overlayers annealed at 400ºC for 30min. A slight shift in $V_{FB}$ is observed between $Ru_{50}Ta_{50}$/Ru and $Ru_{50}Ta_{50}$ layers suggesting a small degree of interdiffusion between $Ru_{50}Ta_{50}$ and Ru at 400ºC.

Figure 4.20 shows the C-V curves for all conditions annealed at 800ºC for 10min. A significant positive shift in $V_{FB}$ is observed compared to the single layer $Ru_{50}Ta_{50}$ gate electrodes.

Figure 4.21 indicates the $V_{FB}$ vs. EOT curve for sample #2 in Table 4.3. The work function of the stacked layer after anneal is close to the Ru control as shown. A significant increase in work function of ~0.6V for sample #2 is observed for the $Ru_{50}Ta_{50}$/Ru stacked sample after 800ºC anneal. Moreover, nearly ~0.8eV shift in work function is observed as

compared to the single $Ru_{50}Ta_{50}$ layer making this an attractive approach for bulk CMOS as shown in Figure 4.22. The resulting work function value can be further tuned in by controlling the composition of the two layers.

Figures 4.23 and 4.24 shows in-situ XRD analysis for the stacked layer of Ru 500A/RuTa 100A on $SiO_2$, which is annealed at a constant temperature ramp rate of $3^oC/s$ from 100°C to 1100°C in forming gas anneal. For as received sample, the Ru (002) peak is strongly shown. Upon annealing there is no strong evidence of grain growth since there is no intensity increase or deviation in the sheet resistance. At approximately $750^oC$ there is a decrease in both optical scattering signals, a slight kink in the sheet resistance and a shoulder peak which forms just to the lower two theta side of the Ru (002) peak. This shoulder peak may be the crystallization of the RuTa (101).

Figures 4.25 and 4.26 shows XRD results for the stacked layer of Ru 500A/RuTa 30A on $SiO_2$ During the anneal the indication of grain growth starts at about $390^oC$ with both an increase in x-ray intensity and a leveling off of the sheet resistance. A slight shoulder peak of the Ru(002) peak is evident at about $820^oC$ although it is very weak. The weak shoulder peak may be crystallization.

$Ru_{50}Ta_{50}$ on the bottom with the overlayer of Ru can be more efficient way than Ru on the bottom with the overlayer of $Ru_{50}Ta_{50}$. When $Ru_{50}Ta_{50}$ on the top, it sometimes suffers from surface oxidation at high temperature, and thus for good contact a proper capping layer is needed on it. In addition to this, adhesion issue of Ru film on dielectric at high temperature can be another disadvantage of Ru on the bottom with the overlayer of $Ru_{50}Ta_{50.}$

### 4.2.4. Conclusion

Ru and Ta vertically layered gate electrodes were investigated for work function tuning and ease of integration. It was found that Ru/Ta stacks provided up to 0.4eV reduction in work function compared to Ru. To increase this change, stacks of $Ru_{50}Ta_{50}$/Ru were also evaluated and nearly a 0.8eV change in work function was observed between $Ru_{50}Ta_{50}$/Ru and $Ru_{50}Ta_{50}$ electrodes. The work function range of these alloys that also provides ease of integration will be advantageous approach for gate electrode in bulk CMOS.

## 4.3. Ru gate with monolayer electrode Process on $SiO_2$ dielectric device

The bilayer integration route presented in the previous section was taken a step further wherein only monolayers of Ta were placed underneath the Ru films. These ultrathin bilayers were investigated to a) minimize the reaction of the Ta layers with $SiO_2$, b) improve adhesion of Ru on $SiO_2$ and c) explore Ru bonding on Ta rich surfaces as compared to $SiO_2$. For the last point, the motivation was to explore whether Ta-O bonding would help stabilize the dielectric surface and Ru bonding via creating a ultrathin charged (dipole) layer that can assist in increasing or decreasing the work function.

The proposed scheme is the deposition of only a few monolayers of very thin Ta layer to change the work function of the Ru as well to provide a better interface for the adhesion issues prior to the deposition of Ru. The resulting work function is expected to be strong function of the thickness Ta layer. Vertical stacks of Ru with Ta monolayer were subjected to high temperature anneals to investigate the stability and further work function tuning at the high temperature.

The key sample conditions are listed in Table 4.4. The thickness of Ta is based on the calculation from sputtering rate and the deposition time. Some samples were covered with W to prevent the possible adhesion issues at high temperature anneal. W capping layer was chosen due to prior evidence of its stability with Ta [12].

Figure 4.27 shows the C-V curves of the capacitors for the Ru 900 Å gates with underlayers of ~0-15 Å of thickness of Ta after a forming gas anneal at 400ºC. The Ru gate without a Ta underlayer and the Ru gate with a monolayer of Ta underlayer displayed the expected value of Ru flat band voltage indicating the monolayer of Ta under the Ru gates did not affect the flat band voltages of the Ru gates. However, The Ru gate with 15 Å of Ta underlayer samples displayed flat band voltage values that were more negative than pure Ru gates as shown in Figure 4.28.

Figure 4.29 shows a $V_{FB}$ vs. EOT curve from C-V measurements on MOS capacitors with varying oxide thicknesses for the Ru 900A gates with a monolayer of thickness of Ta after anneals at various temperatures. All samples were exposed to a forming gas anneal at 400$^{o}$C prior to and after high temperature anneal. Most of the conditions didn't exhibit linear behavior and thus it was difficult to obtain the work function which can be extracted from the y-intercept of this curve. The values of the flat band voltage at 600$^{o}$C were more negative values than those at 400$^{o}$C. However, the values of the flat band voltages at 800$^{o}$C and 900$^{o}$C, both for 30sec. in Ar, were very scattered and attributed to peeling of Ru gates on the $SiO_2$ at higher temperatures. The amounts of increase in EOT were ~1-2 Å after 800$^{o}$C and 900$^{o}$C.

Figure 4.30 shows that a $V_{FB}$ vs. EOT curve from C-V measurements on MOS capacitors with varying oxide thicknesses for the Ru 900A gates with several momolayers of

thickness of Ta after anneals at various temperatures. All samples were given to forming gas anneal at 400°C prior to and after high temperature anneal. Most of the conditions exhibit linear behavior and the values of the flat band voltage at 600°C show more positive values than those of 400°C. Furthermore, the values of the flat band voltages at 800°C are more positive values than those at 600°C. It could be attributed to the effect of $TaSi_2$ formation [11] or Ru diffusion to the interface between dielectrics and the gate electrode. This instability of Ta prevents the use of Ru with several monolayered Ta stacks in this integration approach with Si containing dielectrics. However, the values of the flat band voltages at 900°C show scattered data which can be attributed to the peeling of Ru gates on the $SiO_2$ at 900°C. It was shown that the changes in EOT at different temperature were negligible.

Since Ru gates and Ru gates with a Ta underlayer show scattered flat band voltages that are attributed to the peeling of Ru gates on $SiO_2$, samples were covered with the tungsten films to suppress the peeling of Ru gates on $SiO_2$. W capping layer was chosen due to prior evidence of its stability with Ta [12]. Figure 4.31 shows the C-V curves of the capacitors for the Ru 500 Å gates with underlayer of 0~15 Å of thickness of Ta with 500 Å of W capping layer after a forming gas anneal at 400ºC.

The Ru gate without a Ta underlayer and the Ru gate with a monolayer of Ta underlayer with 500 Å of W capping displayed the expected value of the Ru flat band voltage, but the Ru gate with a 15 Å Ta underlayer displayed more negative flat band voltage values than those of pure Ru gates. These C-V data show similar result to those for the Ru 900 Å gates with the underlayer of ~0-15 Å underlayer of Ta without tungsten capping layer after a forming gas anneal at 400ºC.

Figure 4.32 shows that a $V_{FB}$ vs. EOT curve from C-V measurements on MOS capacitors with varying oxide thicknesses for the Ru 500 Å gates with a underlayer of 0~15 Å Ta and 500 Å of W capping layer after anneals at various temperatures. All samples were given a forming gas anneal at 400$^{o}$C before and after high temperature anneal. Samples exhibit linear behavior at different annealing conditions indicating there was no peeling problem with these gates on the $SiO_2$ after high temperature anneal.

The values of the flat band voltages at 600$^{o}$C were more negative values than those of 400$^{o}$C. Furthermore, the values of the flat band voltages at 800$^{o}$C are slightly more negative than those at 600$^{o}$C, which could be attributed to either the effect of Ru diffusion to the interface between dielectrics and the gate electrode or Ta out-diffusion from the dielectric interface. It will be further discussed in chapter 4. Changes in EOT were negligible after anneals at various temperature indicating there were not significant amount of oxidation near the interface between gate metal and $SiO_2$ dielectrics at high temperatures.

Figure 4.33 shows that a $V_{FB}$ vs. EOT curve from C-V measurements on MOS capacitors with varying oxide thicknesses for the Ru 900 Å gates with several momolayers of thickness of Ta after anneals at various temperatures. All the conditions exhibit linear behavior indicating there was no peeling problem with these gates on the $SiO_2$ after high temperature anneal. Flat band voltages were more positive after 900$^{o}$C annealing than after 400$^{o}$C.

This could be attributed to the effect of $TaSi_2$ formation [11] or Ru diffusion to the interface between dielectrics and the gate electrode. This instability of Ta prevents the use of Ru with several monolayered Ta stacks in this integration approach with Si containing dielectrics. However, the values of the flat band voltages at 900$^{o}$C were scattered because

of peeling of Ru gates on the $SiO_2$ at 900$^oC$. It was shown that the changes in EOT at different temperature were negligible.

## 4.4. Summary

Integration of bi-layered metals with good modulation of the work function for the gate electrodes for P-MOSFET and N-MOSFET devices on the $SiO_2$ dielectrics was developed and discussed. A reaction, either diffusion or intermixing, between the two metals can be controlled to produce a different work function compared to the region in which only the other metal exists.

Vertical stacks of Ru and Ta layers were subjected to high temperature anneals to promote intermixing which resulted in work function tuning. The flatband voltage and electrical dielectric thickness value extracted from C-V measurement after the thermal budget was monitored to evaluate the compatibility of the tunable work function dual metal gate technology gates. The Ru gates with the over-layer of Ta have excellent EOT stability at high temperatures. However, Ta underlayers are unstable on dielectrics, and Ru underlayers resulted in limited work function tuning.

To increase work function change, stacks of $Ru_{50}Ta_{50}$/Ru were also evaluated and higher amount of change in work function was observed between $Ru_{50}Ta_{50}$/Ru and $Ru_{50}Ta_{50}$ electrodes. For $Ru_{50}Ta_{50}$ underlayers with Ru overlayers, nearly ~0.8eV shift in work function is observed as compared to the single $Ru_{50}Ta_{50}$ layer making this an attractive approach for bulk CMOS.

In the second section, only monolayers of Ta were placed underneath the Ru films. These ultrathin bilayers were investigated to minimize the reaction of the Ta layers with $SiO_2$,

improve adhesion of Ru on $SiO_2$ and explore Ru bonding on Ta rich surfaces as compared to $SiO_2$.

## 4.5. References


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**Table 4. 1MOS Capacitor**

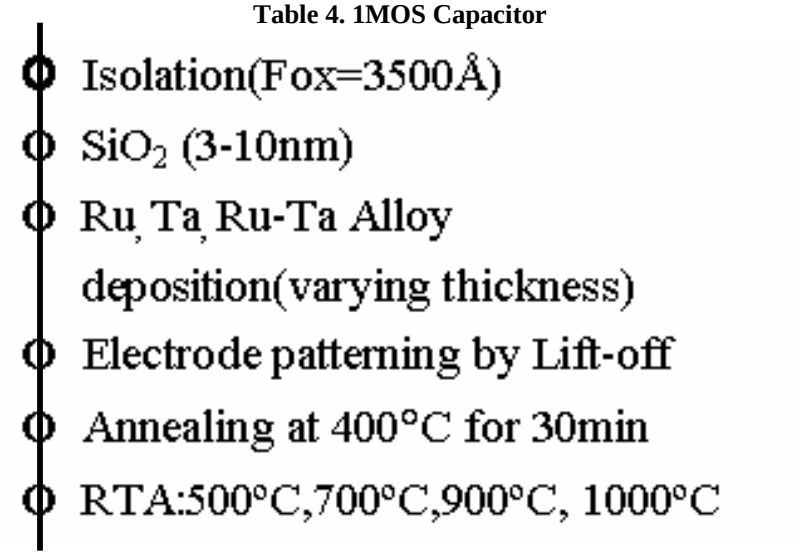


**Table 4. 2 Sample Conditions for Stack**

| Sample | Bottom Metal | Top Metal | Capping Layer |
|---|---|---|---|
| 1 | Ru 700Å | --- | --- |
| 2 | Ru 100Å | Ta 200Å | W 500Å |
| 3 | Ru 30Å | Ta 200Å | W 500Å |
| 4 | Ta 30 Å | Ru500Å | --- |
| 5 | Ta 100Å | Ru500Å | --- |
| 6 | Ta 500Å | --- | W 500Å |

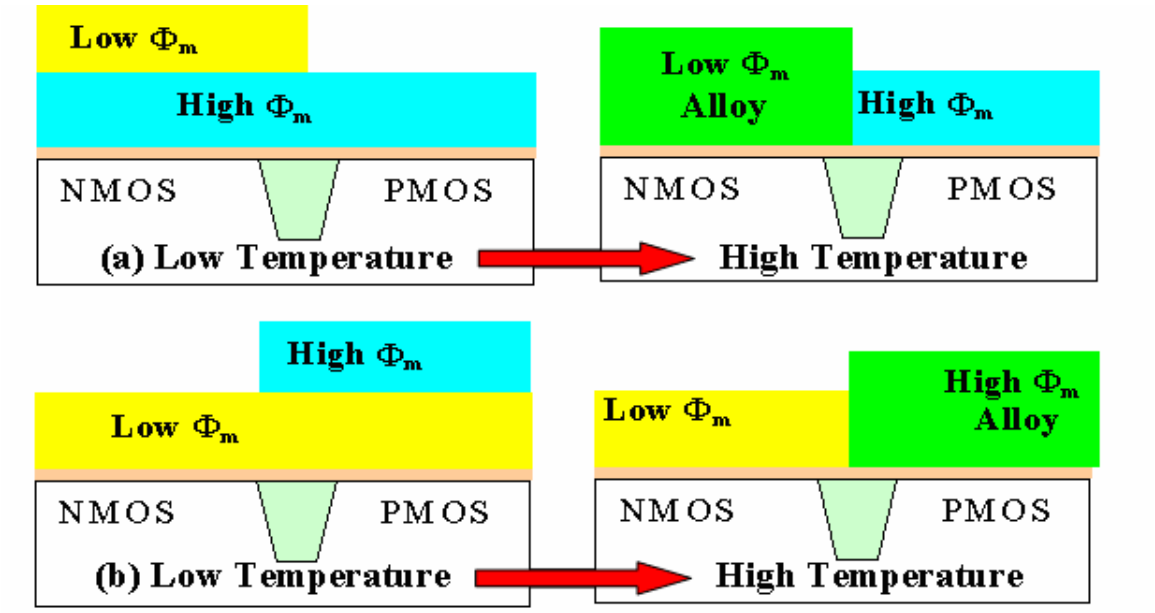


**Figure 4. 1 Integration approach for dual metal gate CMOS**

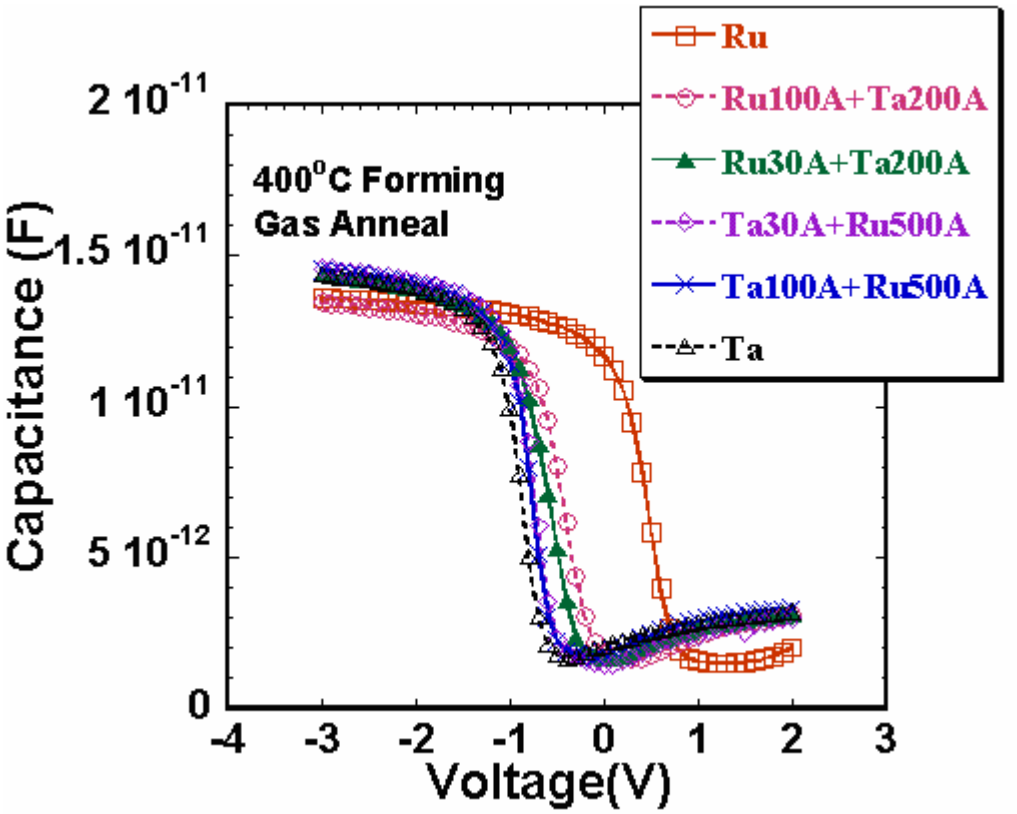


**Figure 4. 2 C-V curves of stacked metal on $SiO_2$**

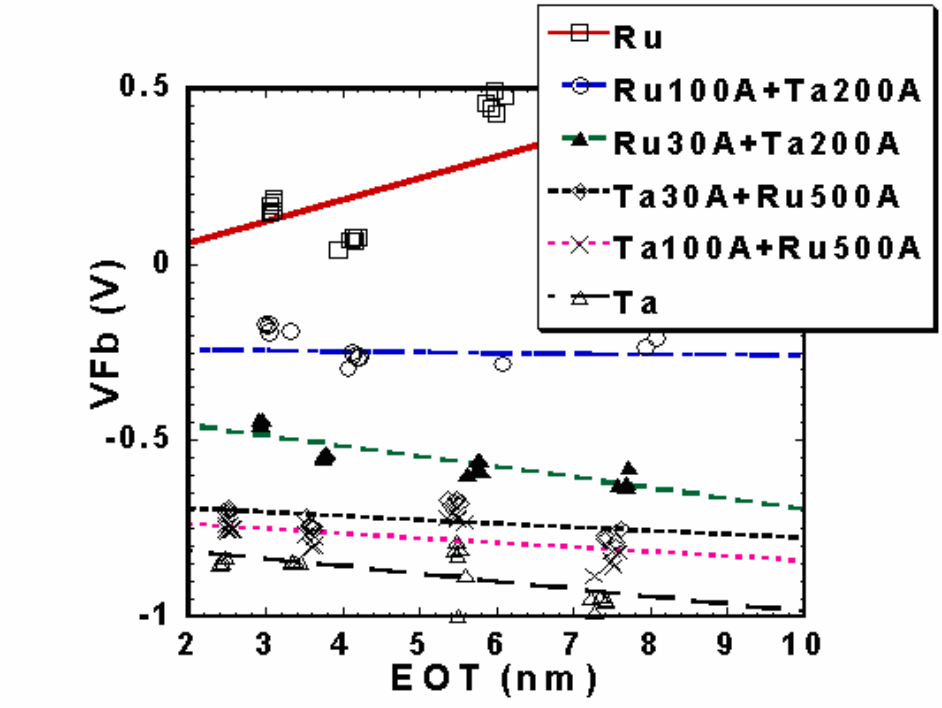


**Figure 4. 3 VFB vs. EOT for various metal gate stack conditions**

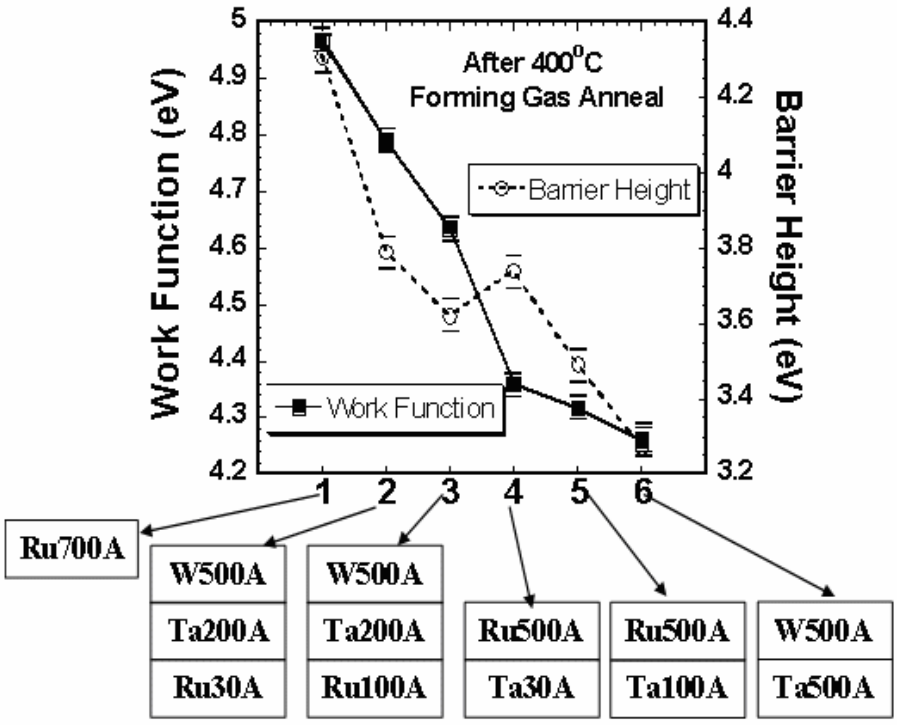


**Figure 4. 4 Work function extracted from C- V curves for various conditions of Ru and Ta stacks.**

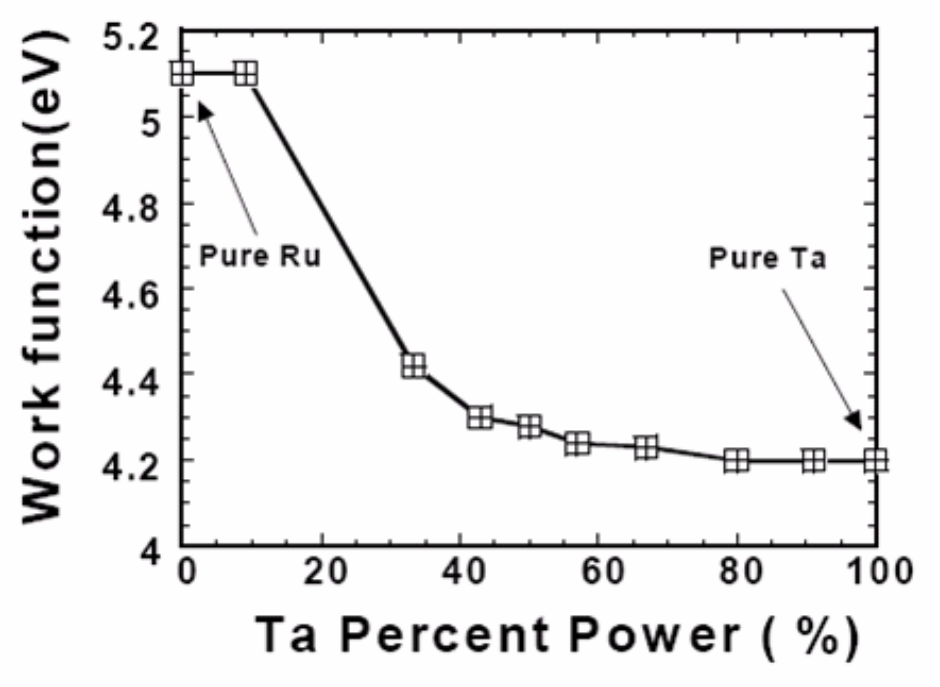


**Figure 4. 5 Work function extracted from C-V curves for various compositions of Ru-Ta alloys. Non-linear behavior as a function of content is observed**

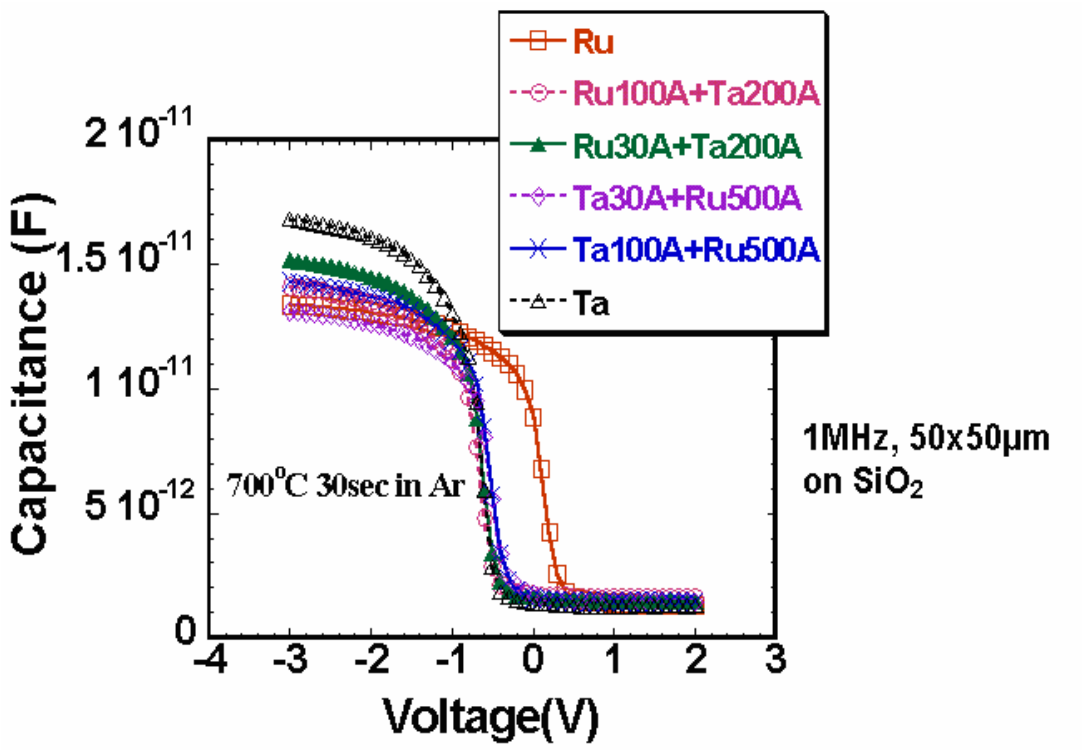


**Figure 4. 6 C-V curves for stacked metal gates on $SiO_2$ after annealing 700°C 30s**

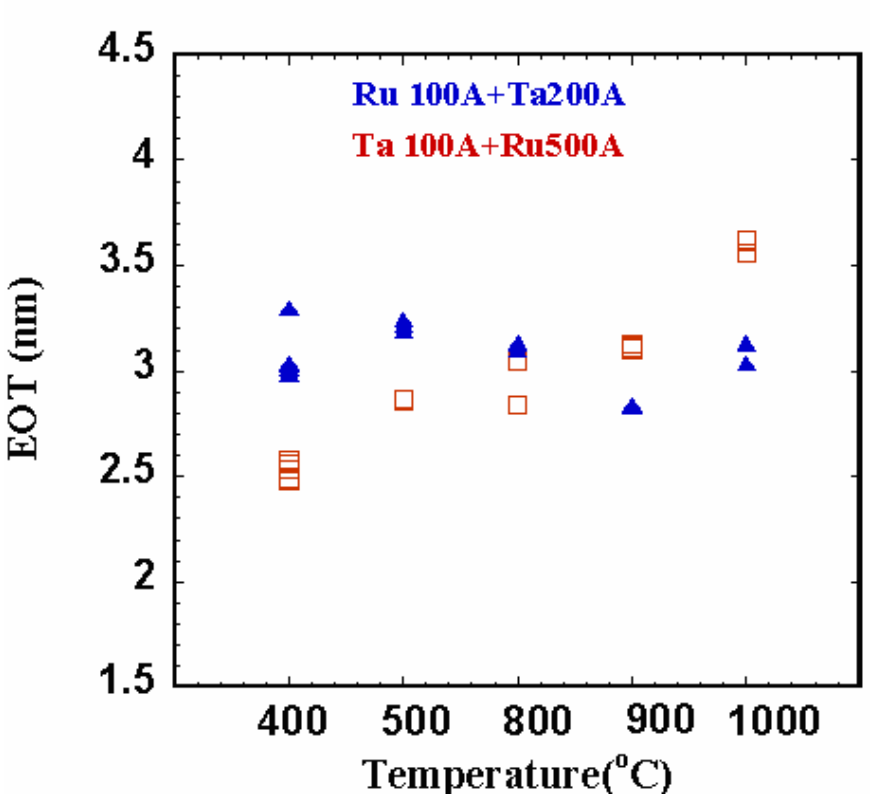


**Figure 4. 7 EOT Stability Under High Temperature**

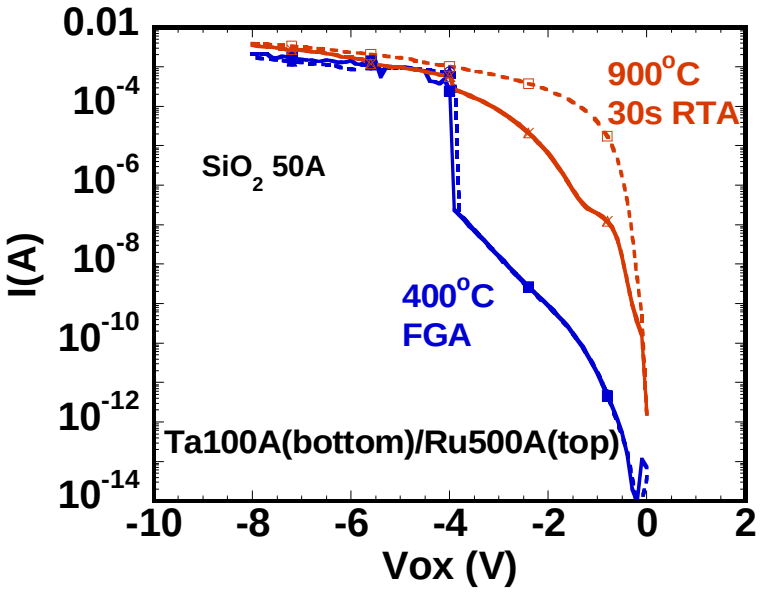


**Figure 4. 8 I-V curves of Ta30A/Ru500A on SiO2 50A Under High Temperature**

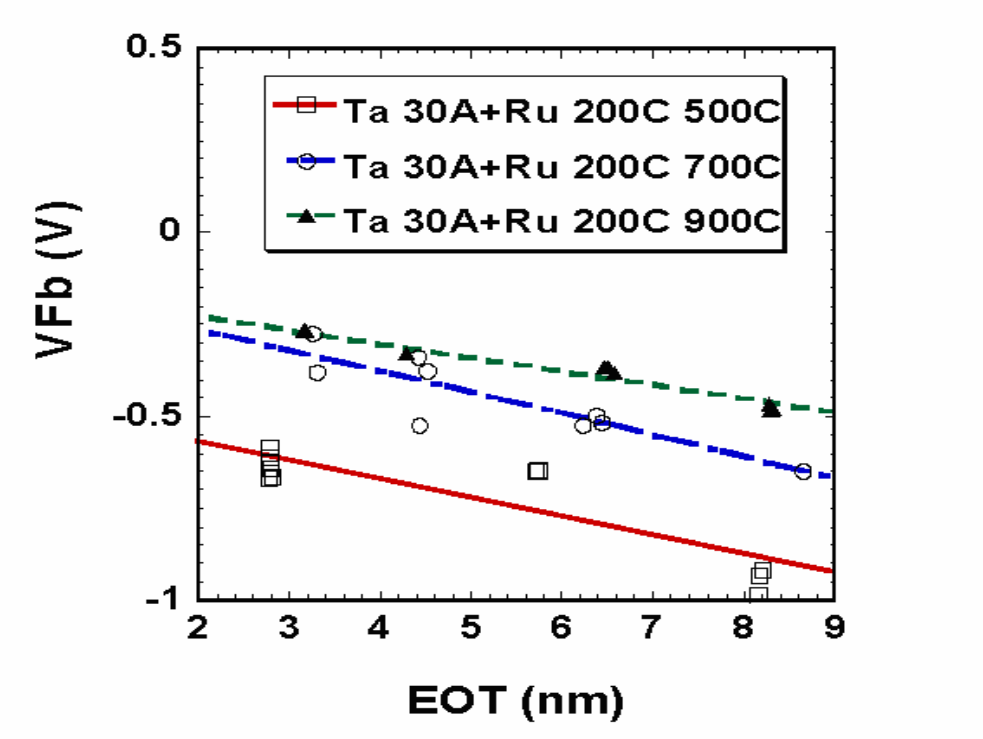


**Figure 4. 9 VFB vs. EOT of Ta/Ru stack for various temperature**

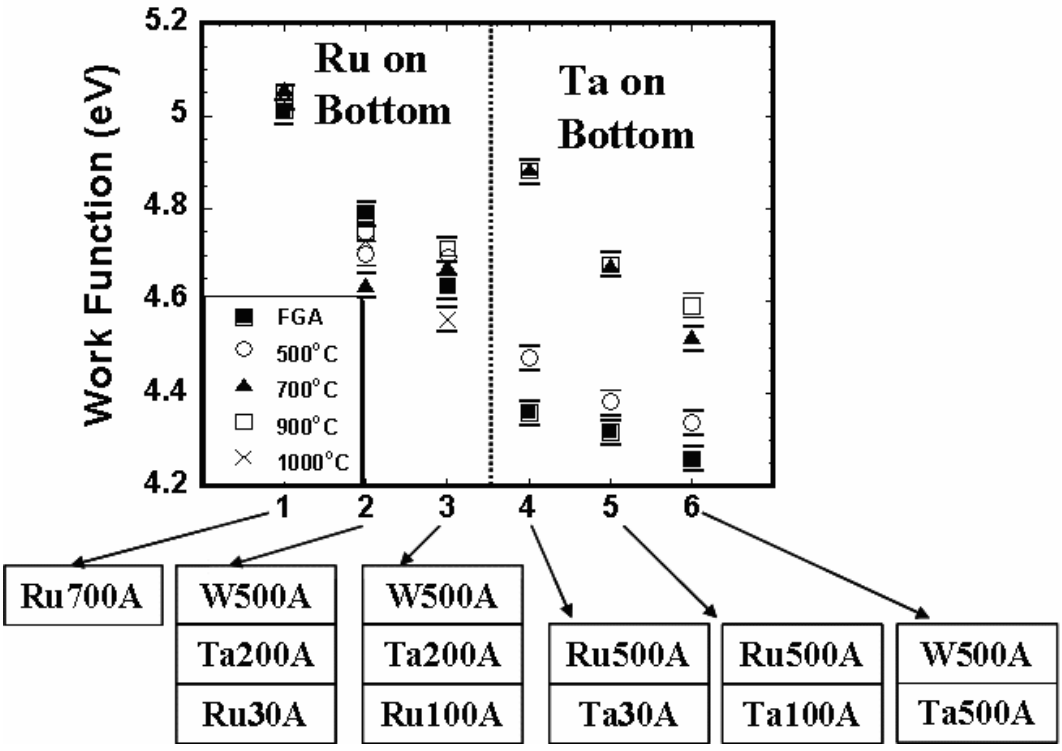


**Figure 4. 10 Work function extracted from CV curves vs. Ta percent power annealed at 500°C, 700°C, 900°C and 1000°C.**

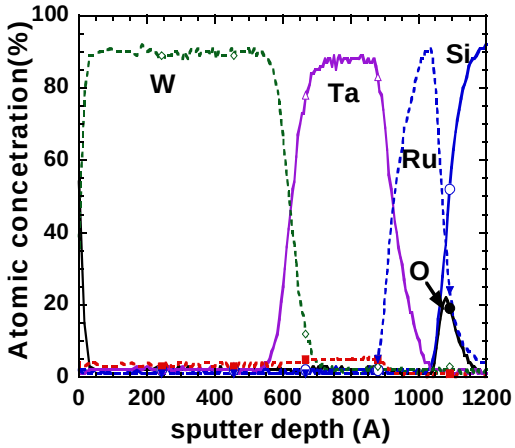


**Figure 4. 11 (a) Auger Depth Profile of as deposited Si/$SiO_2$/Ru 100Å/Ta 200Å/W 500Å**

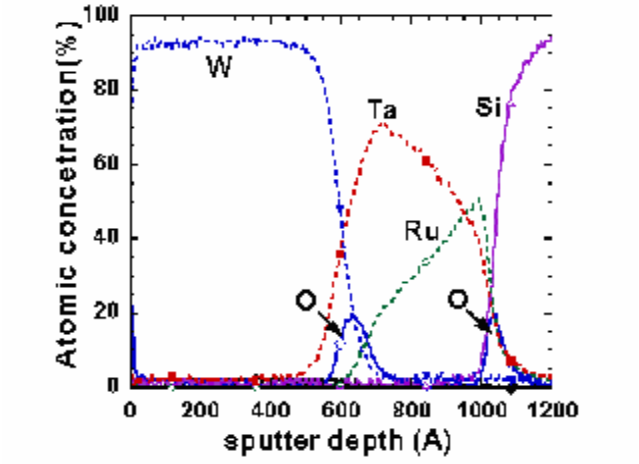


**Figure 4. 12 (a) Auger Depth Profile after annealing of Si/$SiO_2$/Ru 100Å/Ta 200Å/W 500Å**

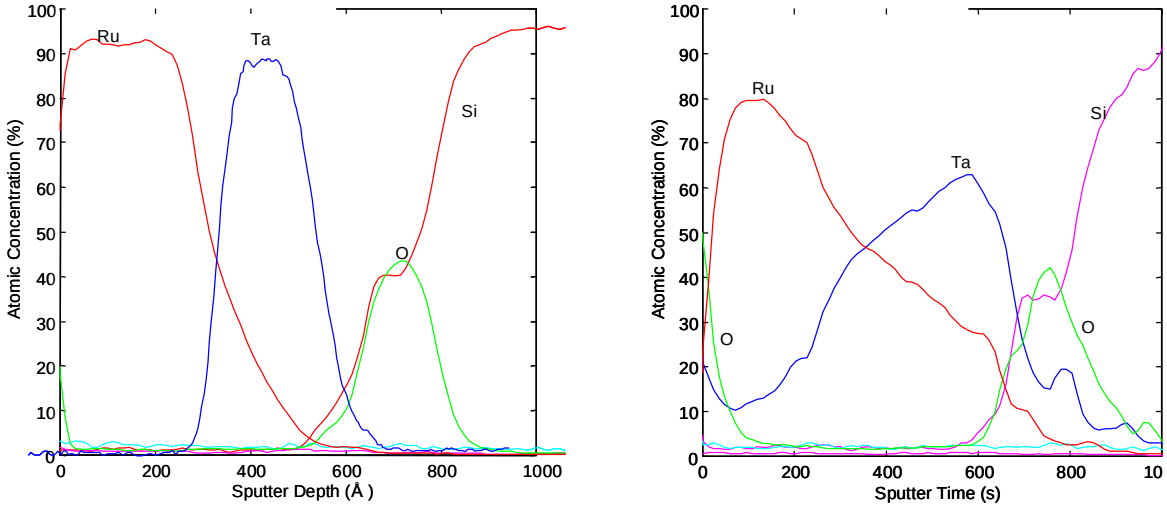


**Figure 4. 13 Auger Depth Profile after annealing of Si/$SiO_2$/Ru 100Å/Ta 200Å/W 500Å**

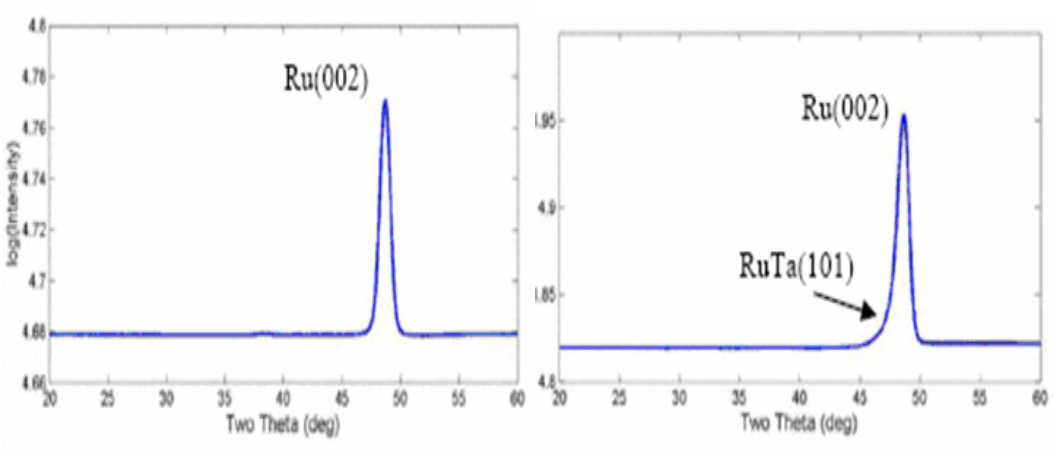


**Figure 4. 14 The in-situ XRD data of 500A Ru / 100A Ta / SiO2 (a) As-deposited (b) after 1100°C anneal**

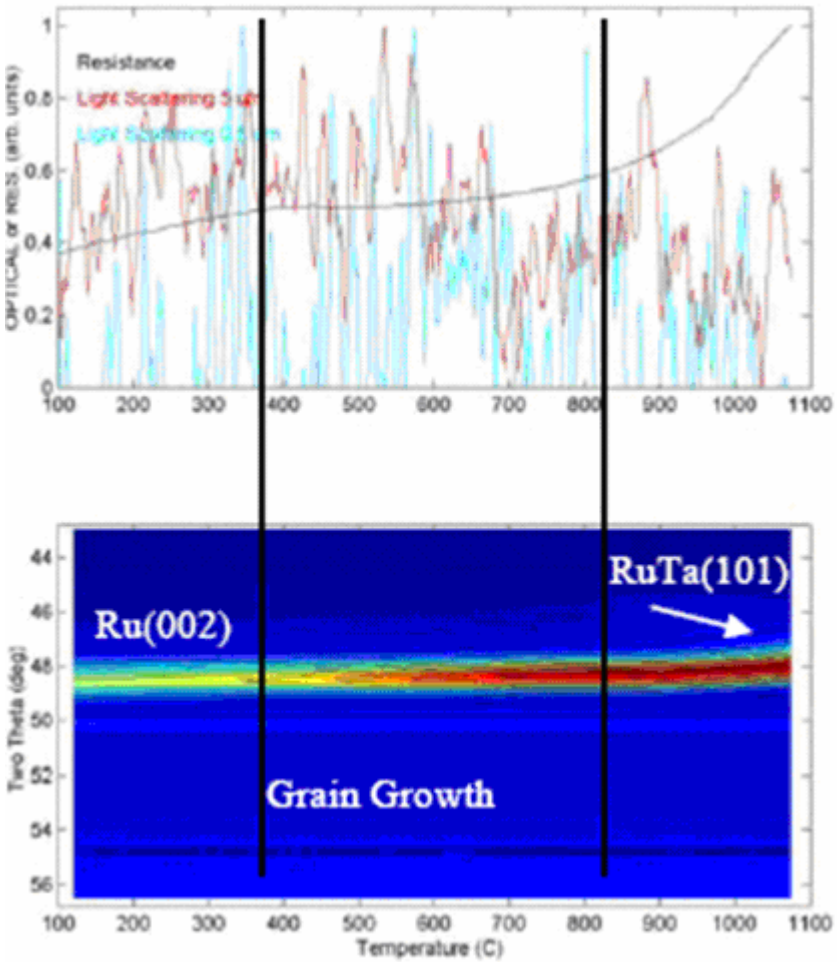


**Figure 4. 15 In-situ XRD data of 500A Ru/ 100A Ta on $SiO_2$ annealed from 100°C to 1100°C**

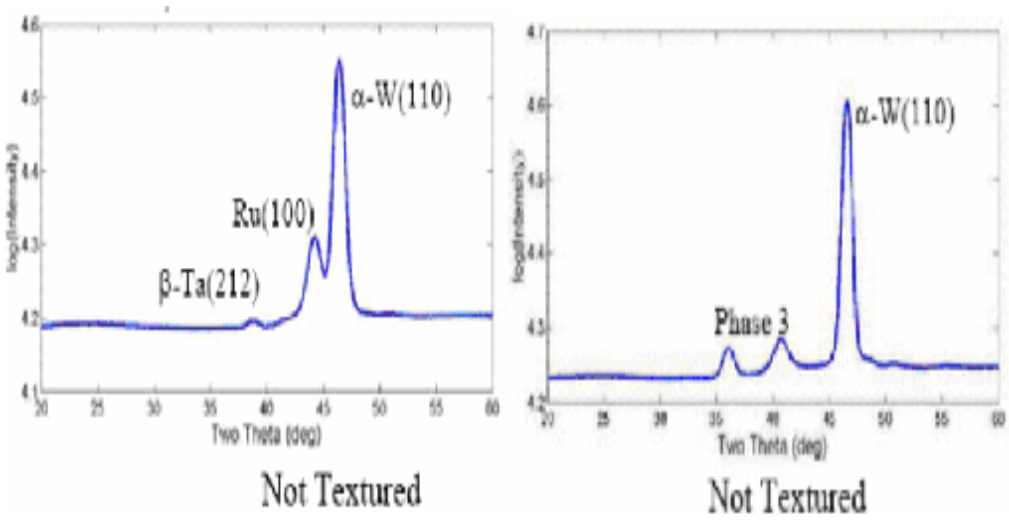


**Figure 4. 16 The in-situ XRD data of 500A W / 200A Ta / Ru 100A /SiO2 (a) As-deposited (b) after 1100°C anneal**

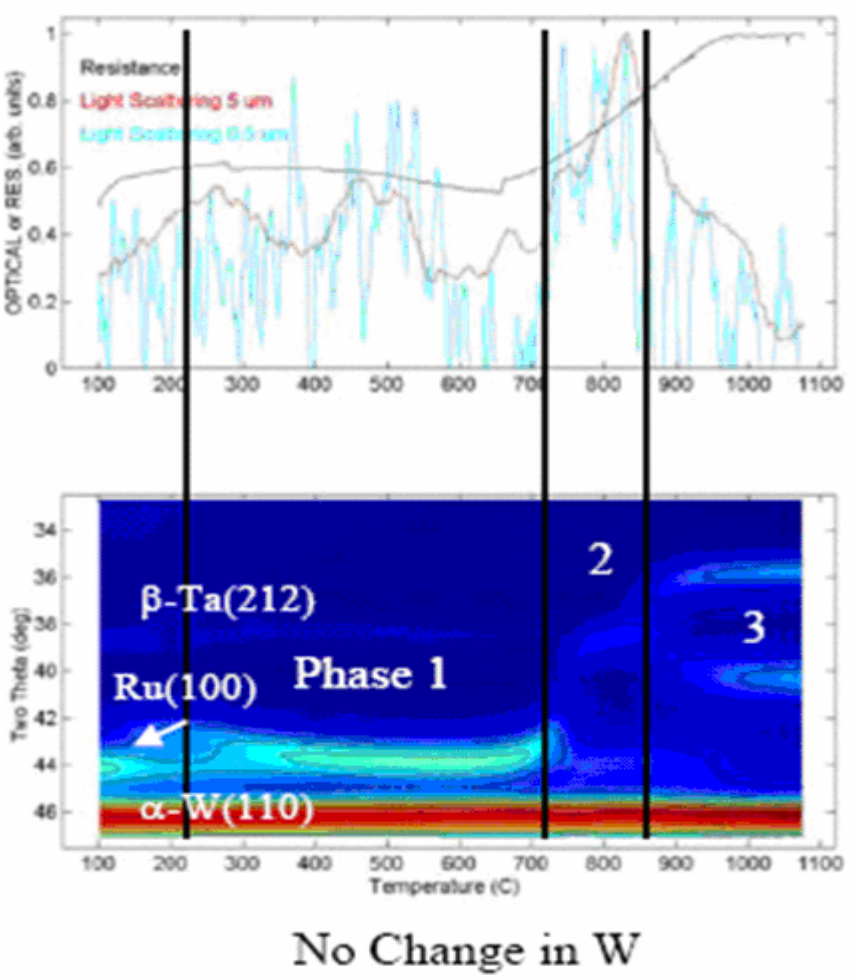


**Figure 4. 17 In-situ XRD data of 500A W / 200A Ta / 100A Ru on $SiO_2$ annealed from 100°C to 1100°C**

**Table 4. 3 Sample conditions for stacked alloys with Ru overlayers on SiO2 in MOS capacitor**

| Sample Set B | Bottom Metal | Top Metal | Capping Layer |
|---|---|---|---|
| 1 | $Ru_{50}Ta_{50}$ 500Å | --- | --- |
| 2 | $Ru_{50}Ta_{50}$ 100Å | Ru 500Å | --- |
| 3 | $Ru_{50}Ta_{50}$ 70Å | Ru 500Å | --- |
| 4 | $Ru_{50}Ta_{50}$ 30Å | Ru 500Å | --- |

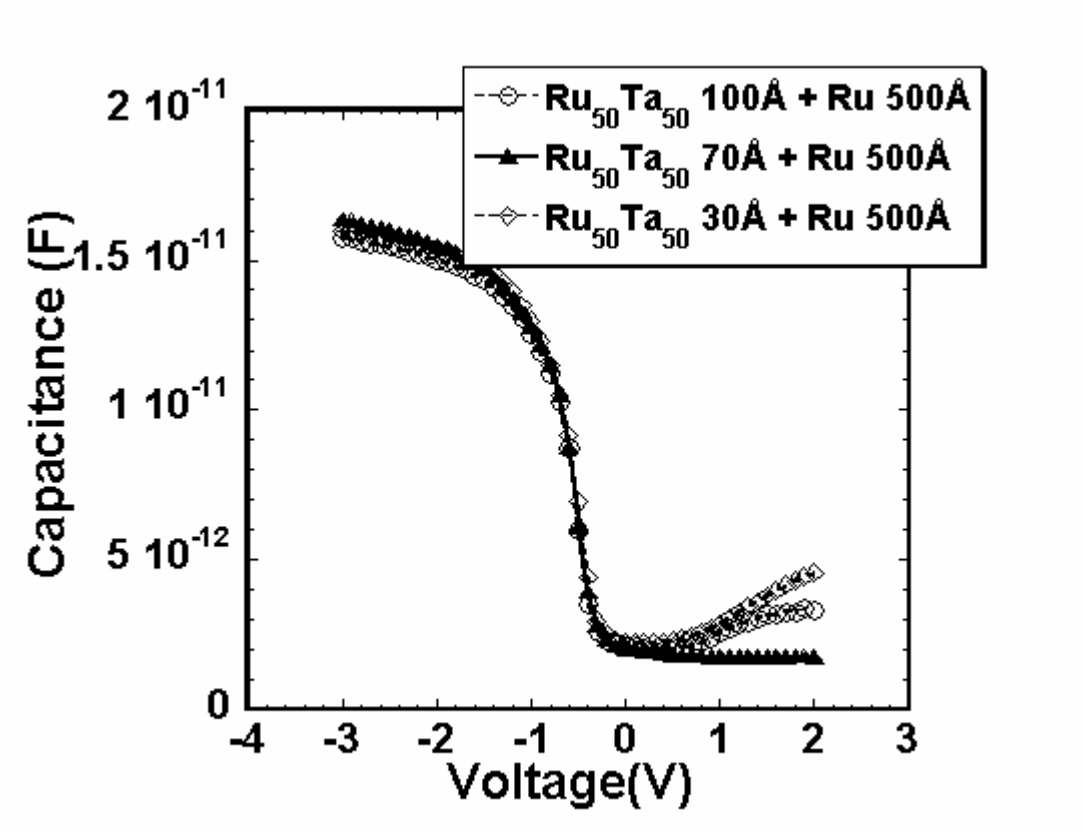


**Figure 4. 18 C- V curves of $Ru_{50}Ta_{50}$/Ru stacks annealed at 400ºC for 30min.**

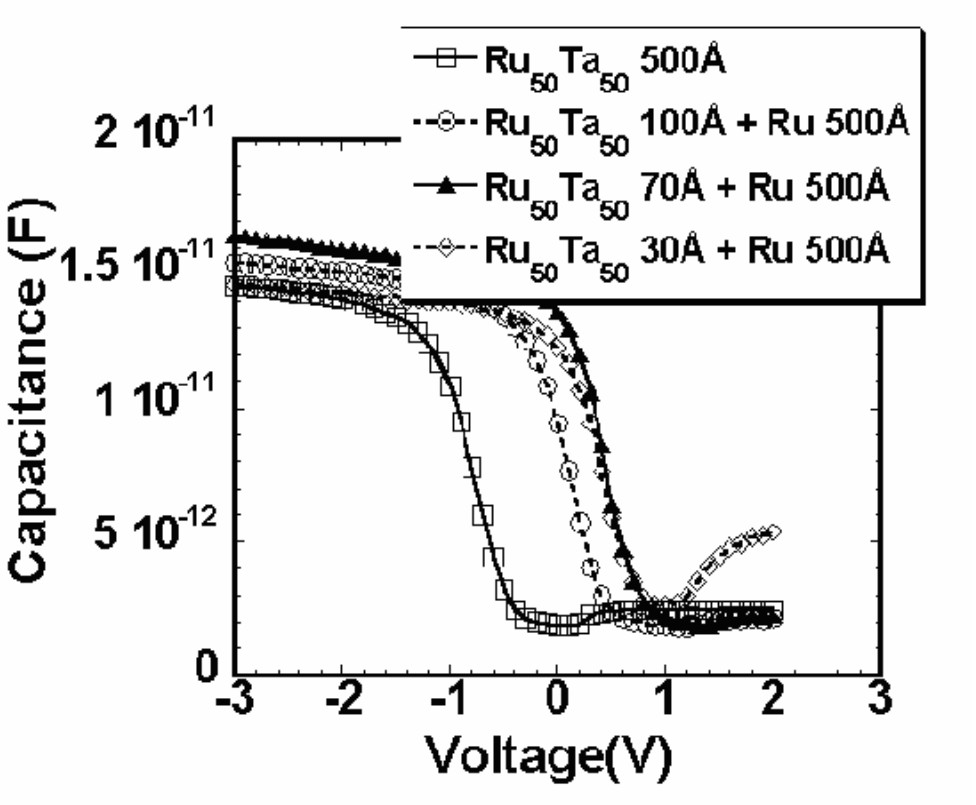


**Figure 4. 19 C- V curves of $Ru_{50}Ta_{50}$/Ru stacks annealed at 800°C for 10min.**

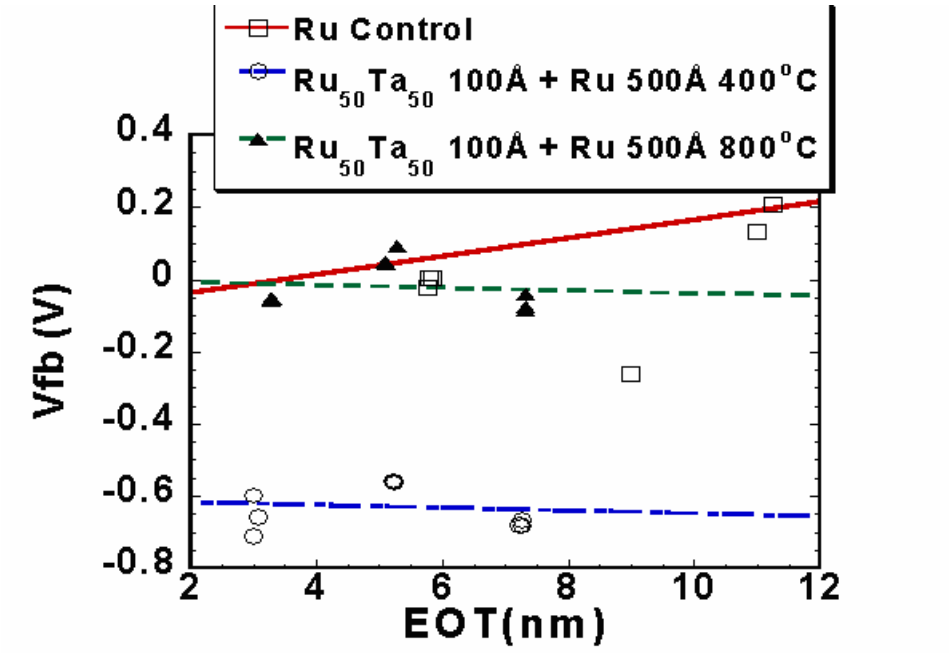


**Figure 4. 20 Vfb vs. EOT for $Ru_{50}Ta_{50}$/Ru stacks annealed at 800°C for 10min.**

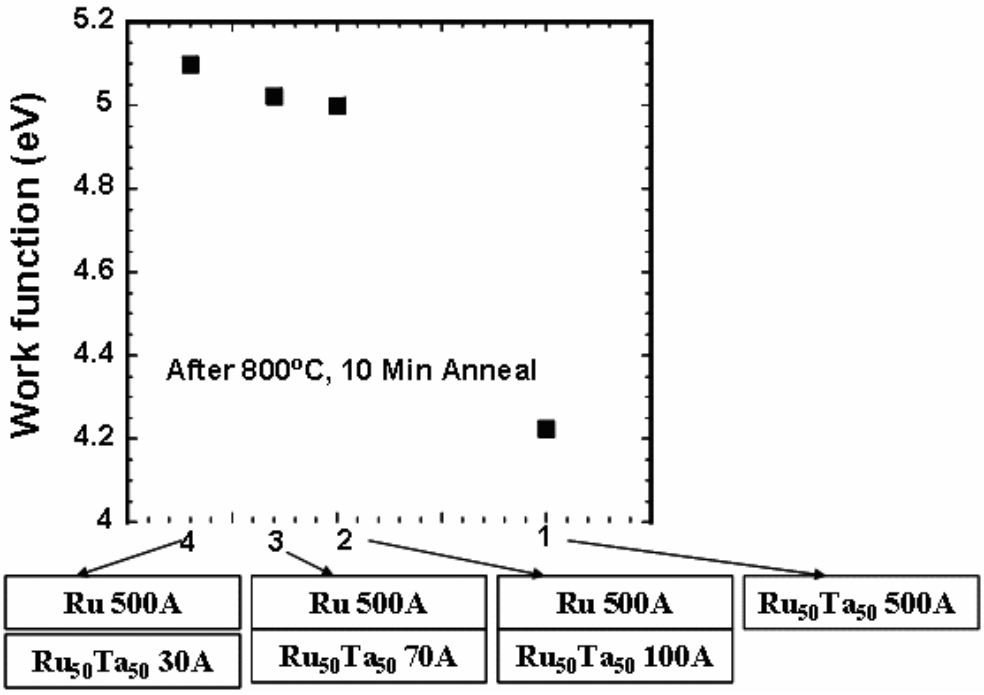


**Figure 4. 21 Work function vs. sample condition: $Ru_{50}Ta_{50}$/Ru stacks annealed at 800°C for 10min.**

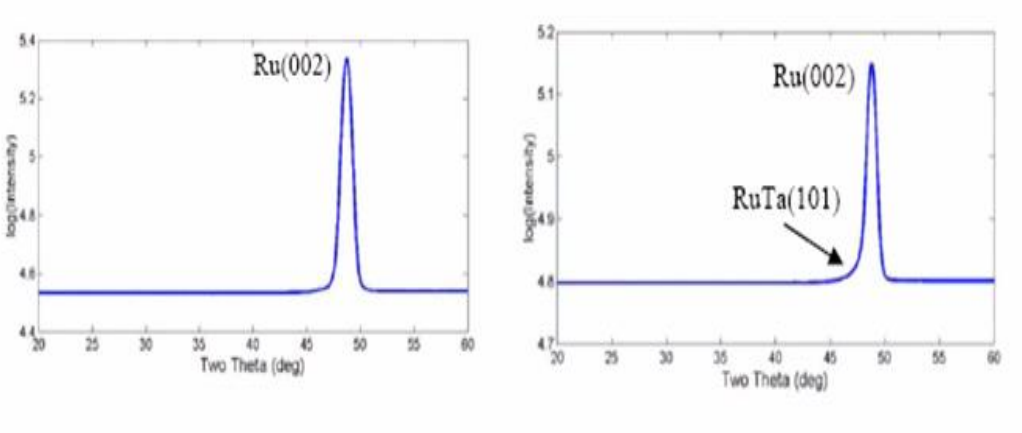


**Figure 4. 22 The in-situ XRD data of 500A Ru / 100A RuTa / $SiO_2$ (a) As-deposited (b) after 1100°C anneal**

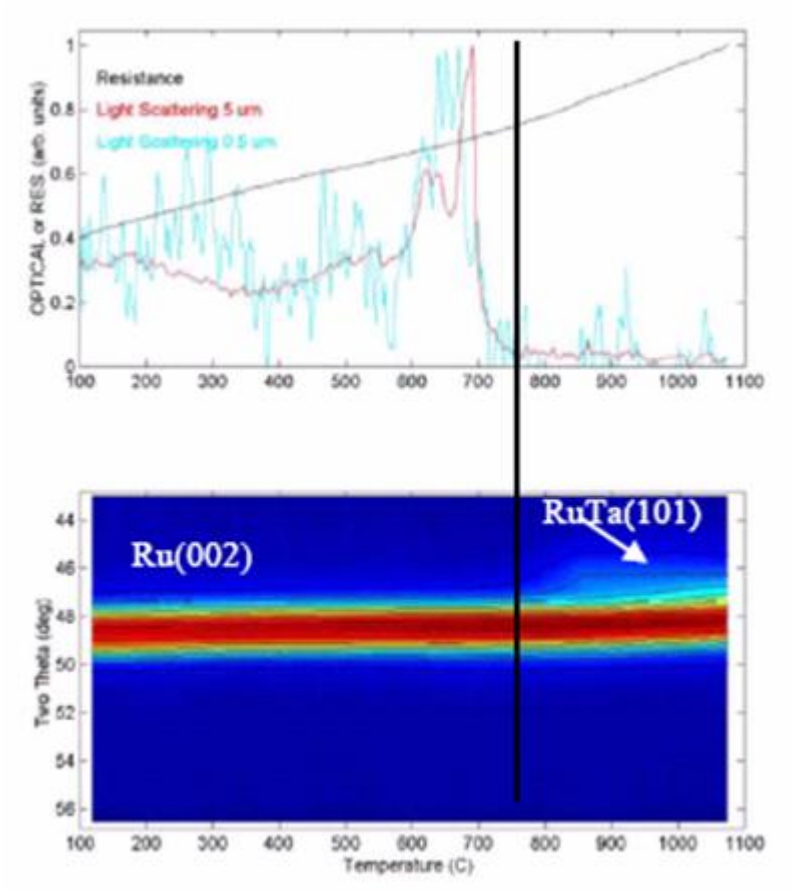


**Figure 4. 23 The in-situ XRD data of 500A Ru / 100A RuTa / $SiO_2$ annealed from 100°C to 1100°C**

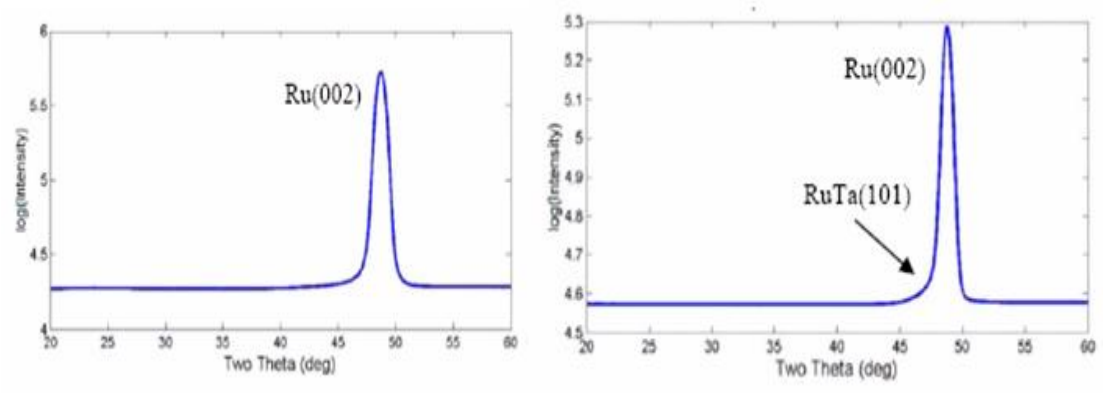


**Figure 4. 24 The in-situ XRD data of 500A Ru / 30A RuTa / SiO2 (a) As-deposited (b) after 1100°C anneal**

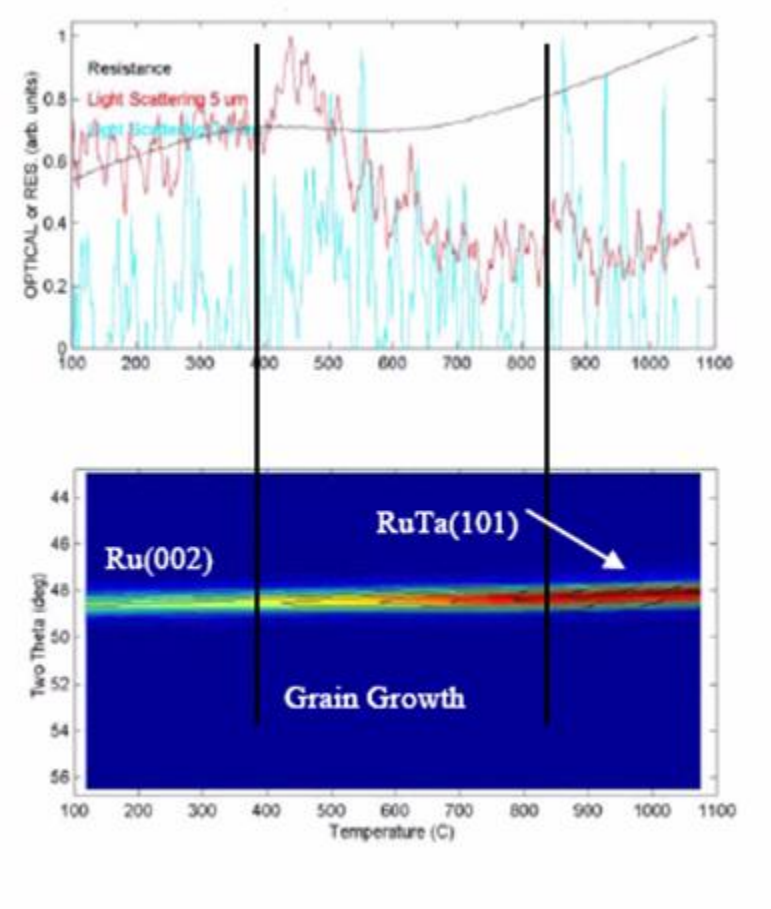


**Figure 4. 25 The in-situ XRD data of 500A Ru / 30A RuTa / SiO2 annealed from 100°C to 1100°C**

**Table 4. 4 Sample conditions for Ta with Ru overlayer gate stacks on $SiO_2$ in MOS capacitor**

| Sample | Bottom Metal | Top Metal | Capping Layer |
|---|---|---|---|
| 1 | Ta 0Å | Ru 500Å | W 500Å |
| 2 | Ta 2.5Å | Ru 500Å | W 500Å |
| 3 | Ta 15Å | Ru 500Å | W 500Å |
| 4 | Ta 0Å | Ru 900Å | --- |
| 5 | Ta 2.5Å | Ru 900Å | --- |
| 6 | Ta 15Å | Ru 900Å | --- |

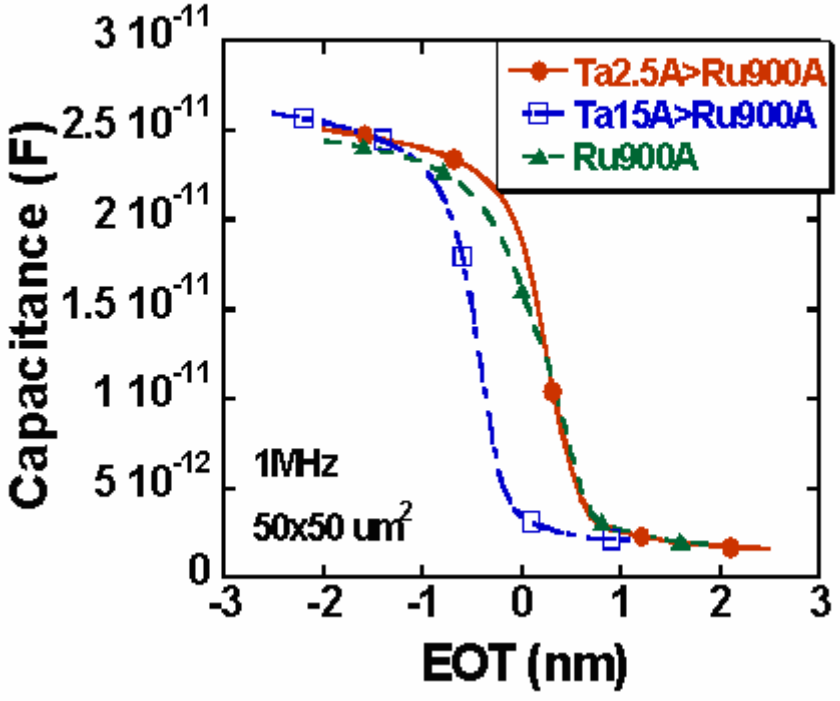


**Figure 4. 26 C-V curves for Ta with Ru overlayer gate stacks forming gas annealed at 400°C**

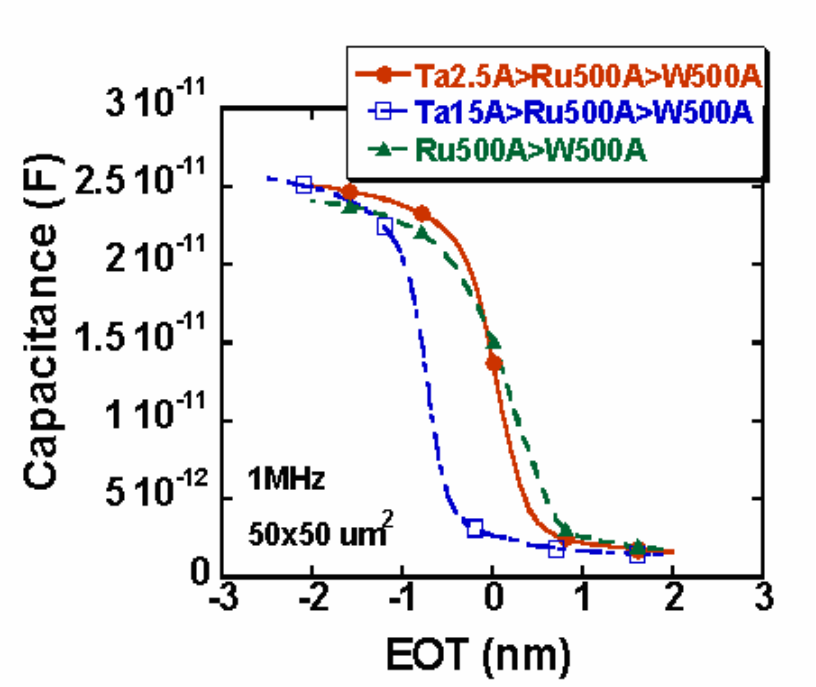


**Figure 4. 27 C-V curves for Ta with Ru overlayer with W capping layer gate stacks forming gas annealed at 400°C**

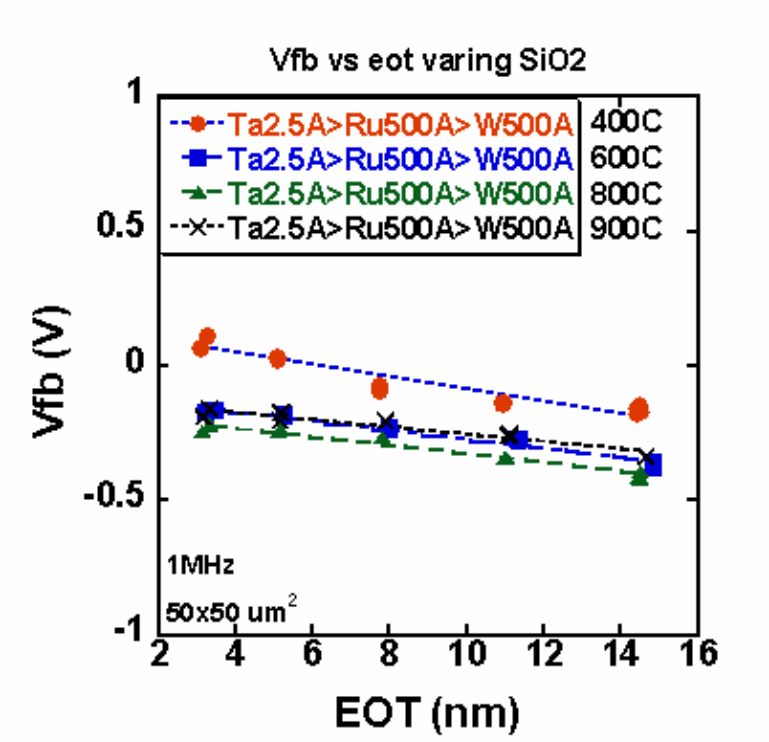


**Figure 4. 28 Vfb vs. EOT curves for Ta monolayer with Ru overlayer with W capping layer gate stacks forming gas annealed at various temperatures.**

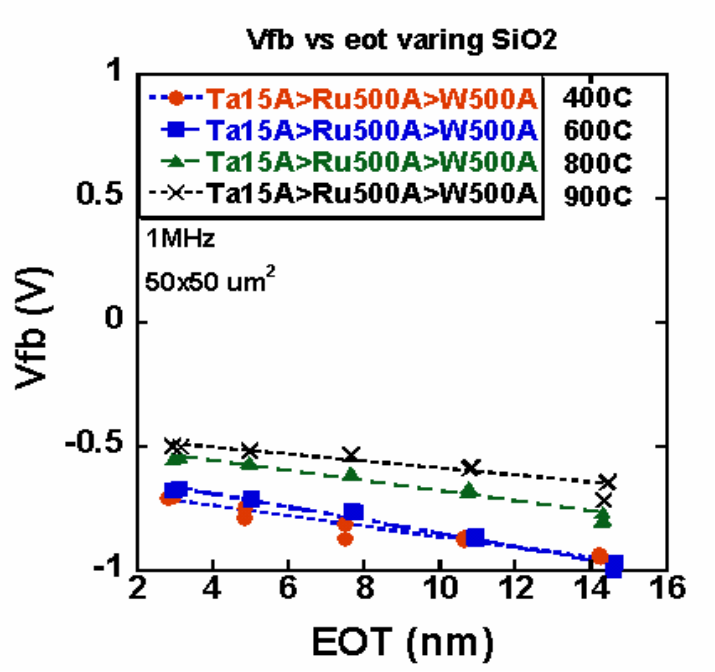


**Figure 4. 29 Vfb vs. EOT curves for Ta monolayers with Ru overlayer with W capping layer gate stacks forming gas annealed at various temperatures.**

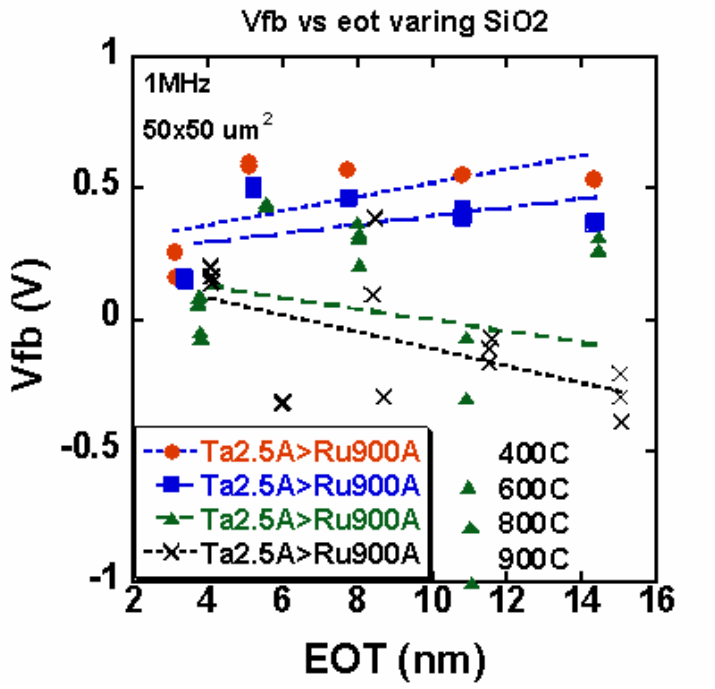


**Figure 4. 30 Vfb vs. EOT curves for Ta monolayer with Ru overlayer gate stacks forming gas annealed at various temperatures.**

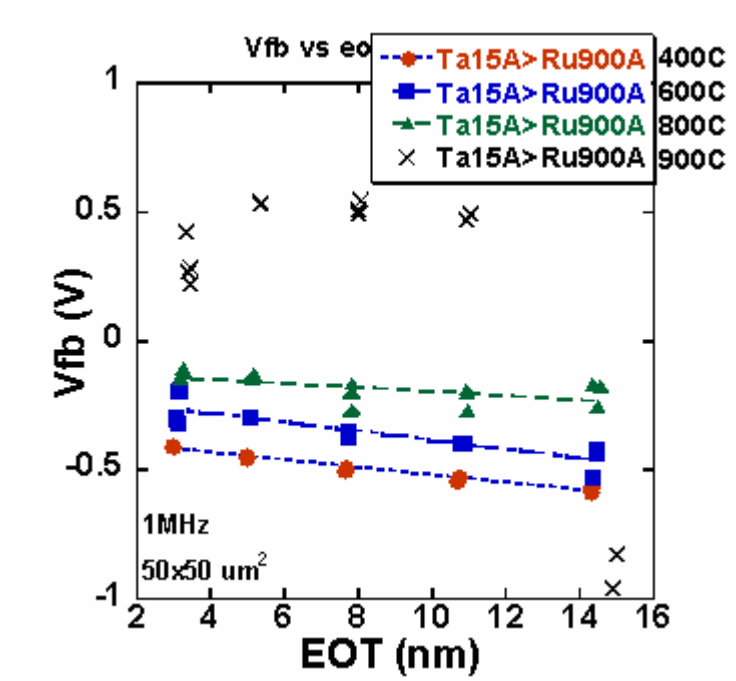


**Figure 4. 31 Vfb vs. EOT curves for Ta monolayers with Ru overlayer gate stacks forming gas annealed at various temperatures.**

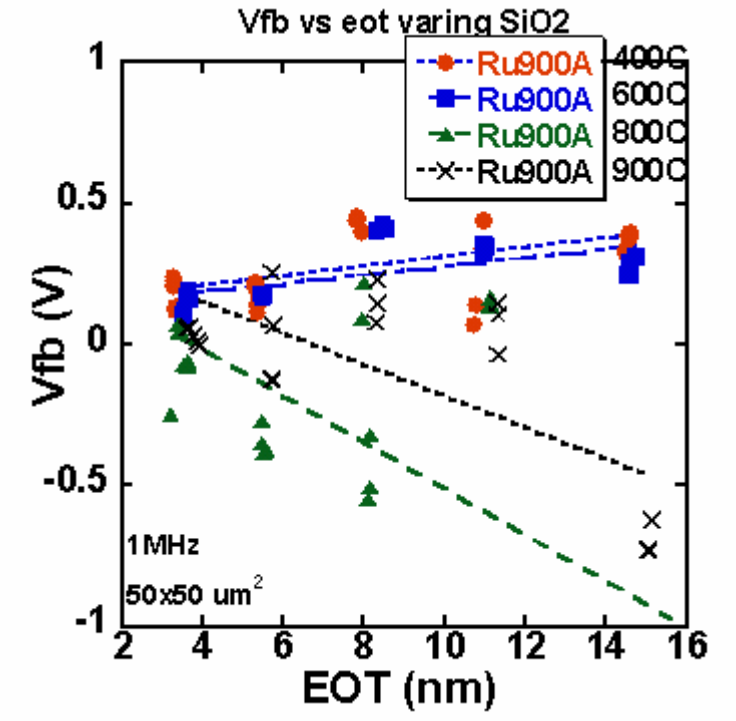


**Figure 4. 32 Vfb vs. EOT curves for Ru single gate stacks forming gas annealed at various temperatures.**

# *Chapter 5* Dual Metal Gate Electrodes Integration on High-K Dielectrics

In chapter 4, the bilayer metal gate electrode system was investigated on $SiO_2$ dielectric. The range of work function tuning, the stability of the gate dielectric and feasibility of integration was investigated. Although the results indicated that both tunable work function values and ease of integration could be achievable, the extension of the same approach on high-K dielectrics is not guaranteed to give the same result due to many issues such as Fermi level pinning, defects on the high-K interface and other instability issues. Hence it is important to investigate the work function behavior of the bilayer system on high-k dielectrics. In this chapter, a bilayer metal gates were investigated on $HfO_2$ and $HfO_2/SiO_2$ stacks.

## 5. 1. Introduction

In the previous sections, we have studied bi-layered metal gates on $SiO_2$, which provide tunable work function values and ease of integration for dual metal gate process flows. An important consideration in the selection of metal gate electrodes is the work function dependence when in contact with high-k dielectrics. In general, the work function of a metal at a dielectric interface is different from its value in vacuum. It has also been reported that work function on high-k dielectrics is different than that on $SiO_2$. This needs to be taken into account when designing transistor gate stacks with alternative gate dielectrics. It has been reported that according to interface dipole theory, the metal work function depends on the permittivity of the gate dielectric. In order to accurately predict metal work function at dielectric interfaces, one needs to take into account charge transfer across such

interfaces. However, it is difficult to predict the amount of charge transfer, since intrinsic interface states are always present and act as donors or acceptors at metal-dielectric interfaces [6-8]. In this section, a bi-layer metal gate which provides tunable work function values and ease of integration for dual metal gate process flow on high-K dielectrics is presented as shown in Figure 5.1.

## 5.2. Experimental

The MOS capacitor fabrication process is summarized in Table 5.1. Atomic layer deposited (ALD) $HfO_2$ of varying thicknesses (20Å, 40Å, 60Å and 80Å) with 20Å $SiO_2$ as an intentional interfacial layer (IL) was used as a gate dielectric. $HfO_2$ was prepared using the precursor of hafnium dimethylamide, $Hf(N(CH_3)_2)_4$. Ozone was used as a reactant gas. Since Ta underlayers are unstable on dielectrics, and Ru underlayers resulted in limited work function tuning, only $Ru_{50}Ta_{50}$ underlayers with Ru overlayers were selected for this study. $Ru_{50}Ta_{50}$ stacks were co-sputtered on the ALD $HfO_2/SiO_2$ from Ru (purity of 99.95 %) and Ta (purity of 99.95%) targets in a system with a base pressure of ~$7x10^{-9}$ Torr. A standard FGA (400$^oC$, 30min, 10% $H_2$) was performed after the lift-off photo process. $Ru_{50}Ta_{50}$ 30-100 Å was prepared by co-sputtering with the power of 50W from Ru and Ta, respectively and then 500 Å Ru was in-situ deposited with the power of 100W.

The thickest $Ru_{50}Ta_{50}$ control sample (500 Å) was covered with a capping layer of the tungsten to enable ease of contact since exposed Ta in $Ru_{50}Ta_{50}$ oxidizes easily. W capping layer was chosen due to prior evidence of its stability with Ta [3]. $Ru_{50}Ta_{50}$ 500 Å was prepared by co-sputtering with the power of 50W from Ru and Ta, respectively and then 500 Å W was in-situ deposited with the power of 100W. C-V characteristics were obtained

using HP4284. The $V_{FB}$ and equivalent oxide thickness (EOT) for the capacitors were obtained using the NCSU C-V software [5]. All samples were annealed in 10% $H_2/N_2$ at 400$^o$C for 30min.

In order to measure the amounts of interdiffusion of elements through films, Auger electron spectroscopy (AES) analysis was performed. X-ray photoelectron spectroscopy (XPS) analysis was performed to measure the diffusion of metals to the top surface. Scanning transmission electron microscopy (STEM) and energy dispersive x-ray (EDX) microanalysis was performed to investigate the diffusion in the films and interfacial reaction between $Ru_{50}Ta_{50}$, Ru and $HfO_2$.

## 5.3. Results and Discussion

Figure 5.2 shows the C-V curves of the capacitors on $HfO_2/SiO_2$ dielectrics after a forming gas anneal at 400ºC. Similar EOTs are obtained for all gates. Only the $Ru_{50}Ta_{50}$ gate without a Ru overlayer displayed the expected $Ru_{50}Ta_{50}$ flat band voltage value. The stacked $Ru_{50}Ta_{50}$/Ru samples displayed flat band voltage values that were more positive than pure $Ru_{50}Ta_{50}$ gate. Figure 5.3 and Figure 5.4 show that the C-V frequency dispersion property of the capacitors with $Ru_{50}Ta_{50}$ 70-100A /Ru 500A bi-layered gates and $Ru_{50}Ta_{50}$ 500A /W 500A stacked gates on $HfO_2/SiO_2$ dielectrics. There was negligible C-V frequency dispersion of this gate from 1MHz to 1 kHz.

C-V measurements on MOS capacitors with varying oxide thicknesses were used to generate a $V_{FB}$ vs. EOT curve in order to decouple the effect of fixed charges and work function on flat band voltage. As shown in Figure 5.5, the work function can be extracted from the y-intercept of this curve. Gate stacks annealed at 400$^o$C showed 3.97~4.29eV of

effective work function. High temperature anneals in Ar at 800ºC for 10min. were performed to further promote intermixing/alloying and compare with the data on $SiO_2$ as discussed in the previous chapter. After the 800ºC anneal, the flat band voltage values shift in the positive direction for the stacks with $Ru_{50}Ta_{50}$ on the bottom compared to 400ºC as shown in Figure 5.6. Significant changes were observed in the EOT and the slope of $V_{FB}$ vs. EOT. Since the thick $Ru_{50}Ta_{50}$ gate on $HfO_2/SiO_2$ with W capping layer has no change in sign of charge as well as in EOT after 800ºC anneal, which is different behavior than seen in other $Ru_{50}Ta_{50}$/Ru stacked gates annealed at high temperature, the change of the sign in charge could originate from the effect of thickness of $Ru_{50}Ta_{50}$ layer, the intermixing between Ru and $Ru_{50}Ta_{50}$, or the impact of different overlayer layers on the top. Since the values of the flat band voltage shift between 400ºC and 800ºC is bigger than for the results obtained with similar stacks on $SiO_2$, this cannot be attributed to only intermixing between Ru and $Ru_{50}Ta_{50}$.

Figure 5.7 summarizes the EOT change in capacitors with $Ru_{50}Ta_{50}$/Ru binary layered gates on varying $HfO_2/SiO_2$ dielectrics between 400ºC and 800ºC in Ar ambient for 10min. The equivalent theoretical values of silicon oxide thickness (EOT) for the capacitors were obtained by using the NCSU CV program. For the case of thin $Ru_{50}Ta_{50}$ bottom layers on $HfO_2/SiO_2$ dielectric, there was a significant EOT increase from 21.4Å after 400ºC forming gas annealing to 28.6Å after 800ºC annealing in Ar, while negligible change was observed for the single gate of $Ru_{50}Ta_{50}$ capped with W on $HfO_2/SiO_2$ between 400ºC and 800ºC annealing. This can be attributed to reactions occurring at high temperatures, either on the top of high-k dielectrics or within the metal gates. Since there was significant

amount of EOT change after high temperature anneal, the reaction $HfO_2$ itself at high temperature is strongly suspected.

Effective work function and charge profiles for $Ru_{50}Ta_{50}$/Ru stack gates on $HfO_2/SiO_2$ also changed drastically after high temperature anneals compared to anneals at 400ºC. While no major change was observed for the single gate of $Ru_{50}Ta_{50}$ capped with W on $HfO_2/SiO_2$ under the same condition, the effective work function of the stacks with $Ru_{50}Ta_{50}$ on the bottom on $HfO_2/SiO_2$ was separated by more than 1eV after 400ºC anneal. Since the single gate of $Ru_{50}Ta_{50}$ on $HfO_2/SiO_2$ with W capping layer has no significant change in the work function after 800ºC anneal, the increase could also be attributed to the interaction between Ru and $Ru_{50}Ta_{50}$, different capping layers on top, impact of the charged layers, the role of diffused Ru within the layer of the thin $Ru_{50}Ta_{50}$, and dipoles near the interface between $Ru_{50}Ta_{50}$ and the dielectrics. It also shows that the shift of the flat band voltage values from 400ºC to 800ºC is more positive and the value of the shift is bigger than for the results obtained with similar stacks on $SiO_2$. However, even though a larger shift was obtained with $HfO_2/SiO_2$, this cannot be attributed to a larger degree of intermixing than on the $SiO_2$ since other issues such as charges, reactions may have additional effects. Since there was a significant amount of EOT change after high temperature anneal, the reaction $HfO_2$ itself at high temperature is strongly suspected. Since the thick $Ru_{50}Ta_{50}$ gate on $HfO_2/SiO_2$ with W capping layer has no change in sign of charge as well as in EOT after 800ºC anneal, which is different behavior than other $Ru_{50}Ta_{50}$/Ru stacked gates at high temperature, the change of the sign in charge could be originated from the effect of thickness of $Ru_{50}Ta_{50}$ layer, the intermixing between Ru and $Ru_{50}Ta_{50}$, or impact of different overlayer layers on the top. Since the values of the flat band voltage shift from 400ºC to 800ºC is is

bigger than for the results obtained with similar stacks on $SiO_2$, this cannot be attributed to only intermixing between Ru and $Ru_{50}Ta_{50}$.

Figure 5.8 shows the TEM image of $Ru_{50}Ta_{50}$ 100 Å with the overlayer of Ru 500 Å on $HfO_2/SiO_2$ (20 Å /20 Å) dielectric after a forming gas anneal at 400$^o$C. As shown, $Ru_{50}Ta_{50}$ film shows amorphous structure and very smooth interface on the top of $HfO_2$ attributed to some reaction. The layer thicknesses were 100 Å which matched the deposition conditions. Pt layer was deposited on the top of Ru film during TEM sample preparation.

In order to investigate whether intermixing between the Ru and $Ru_{50}Ta_{50}$ was the main mechanism of the work function tuning, TEM image of $Ru_{50}Ta_{50}$ 100A with the overlayer of Ru 500 Å on $HfO_2/SiO_2$ (20 Å /20 Å) dielectric annealed at 800$^o$C for 10min. in Ar was shown in Figure 5.9. The sample was forming gas annealed at 400$^o$C before and after anneal at 800$^o$C. As shown, the interface between $Ru_{50}Ta_{50}$ and $HfO_2$ was smooth even after high temperature anneal. There was some amount of intermixing between $Ru_{50}Ta_{50}$ film and Ru. Ru grains became bigger after high temperature anneals indicating no obvious reaction between $Ru_{50}Ta_{50}$ with $HfO_2$ at this temperature. However, on top of the Ru layer, ~10-20nm thickness of a new layer was formed. XPS analysis was done on the surface of sample $Ru_{50}Ta_{50}$ with Ru overlayer after high temperature annealing at 800$^o$C in order to investigate the composition of the new layer formed after high temperature anneal. As shown in Figure 5.10, the Ta peak can be clearly seen on the surface of the film indicating out diffusion to bind with oxygen. From electrical data, it was observed that EOT increase significantly. It suggested that Ta out-diffuse through Ru grain boundary from $Ru_{50}Ta_{50}$ to

surface to from $Ta_xO_y$ layer on the surface. It is believed that TaxOy contributes EOT increase. It will be further studied using AES depth profiling and EDX analysis.

Figure 5.11 shows a TEM image of $Ru_{50}Ta_{50}$ 500A with the capping layer of W 500 Å on $HfO_2/SiO_2$ (20 Å /20 Å) dielectric after a forming gas anneal at 400$^o$C. As shown, $Ru_{50}Ta_{50}$ film amorphous structure and $Ru_{50}Ta_{50}$ layer thicknesses were ~500 Å which matched the deposition conditions. However, W capping layer has been oxidized ~300A leaving ~200A W layer which is from the deposition condition of 500 Å W layer even after a forming gas anneal at 400$^o$C. As discussed earlier, W is very easily oxidized after FGA at 400$^o$C and thus forms ~200-300 Å WOx.

In order to investigate whether Ta out-diffuses from $Ru_{50}Ta_{50}$ 500 Å with the capping layer W 500 Å after high temperature anneal, TEM image of $Ru_{50}Ta_{50}$ 500 Å with the capping layer W 500 Å on $HfO_2/SiO_2$ (20 Å /20 Å) dielectric annealed at 800$^o$C for 10min. in Ar was shown in Figure 5.12. The sample was forming gas annealed at 400$^o$C before and after anneal at 800$^o$C. The thickness of the oxidized W capping layer has not been significantly changed as thick as ~300A from after FGA at 400$^o$C. It will be studied more using AES depth profiling. XPS analysis was done on the surface of thick $Ru_{50}Ta_{50}$ (500 Å) with W capping (500 Å) after high temperature annealing at 800$^o$C in order to investigate the composition of the oxide layer formed. As shown in Figure 5.13, the W peak can be clearly seen on the surface of the film indicating Ta couldn't out-diffuse to bind with oxygen at the surface. No significant EOT increase was observed with thick $Ru_{50}Ta_{50}$ (500 Å) with W capping (500 Å) after high temperature annealing at 800$^o$C. It suggested that Ta has no driving force to out-diffuse to surface through W capping and oxidized WOx layer. It is

believed that TaxOy contributes to the EOT increase. It will be further studied using AES depth profiling and EDX analysis.

The AFM analysis was performed to study surface roughness to compare before and after the effect of the high temperature anneal. The areas examined were 5 x 5 $\mu m^2$, and the images were post-processed using a flattening algorithm. After high temperature anneals, the surface became rough and the extracted Root Mean Square (RMS) surface roughness before high temperature anneal was 0.393 nm. The RMS roughness of after high temperature anneal was 23.092 nm. Therefore, the high temperature annealed films exhibit roughness two order higher value than that of non-annealed one.

In order to confirm Ta peak on the surface and measure intermixing of diffusion of this gate at high temperature, the Auger Electron Spectroscopy depth profiling of $Ru_{50}Ta_{50}$(100 Å)/Ru(500 Å) film after 800$^oC$ anneal in Ar ambient for 10 min. is illustrated in Figure 5.15. The highest intensity of the oxygen peak was detected at the surface and it decreases with depth, which indicates that a considerable amount of oxidation exists on the surface. This oxygen probably comes during the forming gas anneal and then the high temperature anneal can provide the oxygen with enough thermal budget to diffuse. Significant amount of tantalum was found on the surface, which indicates tantalum diffusion through the Ru film from the bottom layer of $Ru_{50}Ta_{50}$ to bind the oxygen at higher temperature. From electrical data, it was observed that TaxOy contributes to the EOT increase. It is attributed to Ta out-diffusion to the surface to from $Ta_xO_y$ layer on the surface.

In order to compare the AES result of $Ru_{50}Ta_{50}$ (100Å)/Ru(500Å) film after 800$^oC$ anneal, the Auger Electron Spectroscopy depth profiling of thick $Ru_{50}Ta_{50}$(500Å) with

capping layer of W(500 Å) film after 800°C anneal in Ar ambient for 10 min. is illustrated in Figure 5.16. The high of the oxygen peak was detected at the surface and it decreases rapidly 200 Å from the surface, which indicates that a considerable amount of oxidation exists on the surface. This oxygen comes after the FGA and then the high temperature anneal can provide the oxygen with enough thermal budget to diffuse. No tantalum was observed on the surface, which is attributed that tantalum couldn't diffuse through the W film from the bottom layer of $Ru_{50}Ta_{50}$ to bind the oxygen at higher temperature. No formation of TaxOy contributes EOT increase supports no significant EOT increase.

As shown, the final work function of various gate stacks depends strongly on the thickness of the bottom and top layers and the gate dielectrics. Work function of single layer $Ru_{50}Ta_{50}$ gates with W capping didn't change much after annealing. However, as the $Ru_{50}Ta_{50}$ layer at the bottom is made thinner with a Ru overlayer, the work function increases at 800ºC, regardless of the $Ru_{50}Ta_{50}$ layer thickness. The main mechanism responsible for a large work function increase for the $Ru_{50}Ta_{50}$/Ru stacks is believed to be the high Ru content of the resulting alloy. However, since the shift of the flat band voltage values of the stacks with $Ru_{50}Ta_{50}$ after 800ºC anneal is larger than that on $SiO_2$, it can not be attributed solely to the intermixing but the charge or reaction over the layers can also be responsible for it. The resulting work function value can be further tuned by controlling the composition of the two layers and that of the interface and also by charge engineering.

Scanning tunneling electronic microscopy (STEM) analysis and energy dispersive x-ray (EDX) microanalysis was performed on $Ru_{50}Ta_{50}$ with the overlayer of Ru on $HfO_2/SiO_2$ dielectric structure before and after the 800°C anneal. Figure 5.17 (a) shows the STEM image of the cross section of Ru with the $Ru_{50}Ta_{50}$ underlayer on $HfO_2$/ $SiO_2$ after the

forming gas anneal at 400°C and subsequent anneal at 800°C for 10minutes in Ar. Figure 5.17 (b) shows that the composition of the bottom layer of $Ru_{50}Ta_{50}$ using EDX analysis. It was found that Ru peak was higher than Ta and this was also expected from the original composition obtained from the sputtered film. Even though its resolution is approximately ~5-10 nm depending on the structure, it indicates that either Ru diffuses to the interface or Ta out diffuses to the surface, since the thickness of $Ru_{50}Ta_{50}$ is ~10nm.

At the interface of Ru and $Ru_{50}Ta_{50}$, the intensity of Ru and Ta was almost the same as shown in Figure 5.17 (b). Figure 5.17 (c) shows that there were only Ru peaks, indicating the absence of Ta in this region. Both these regions are consistent with their original composition from sputtering conditions. Some amount of intermixing was observed after high temperature annealing. Figure 5.17 (d) shows that there is more Ta than Ru near the surface of the stack. Even though it was expected that only Ru peaks would be observed, higher intensity Ta peaks were detected. This indicates that Ta diffuses out towards the surface to be oxidized. From electrical data, it was observed that EOT goes up. It is attributed that Ta out-diffuses to the surface to from $Ta_xO_y$ layer on the surface. This result is also consistent with the XPS, TEM and AES depth analysis.

Figure 5.18 shows that the composition of the top layer of $W/Ru_{50}Ta_{50}$ using EDX analysis on $HfO_2$/ $SiO_2$ after the FGA at 400°C and subsequent anneal at 800°C for 10minutes in Ar. It was found that only W peak was observed and Ta peak wasn't observed indicating no Ta out-diffusion through W capping layer. This result is also consistent with the XPS, TEM and AES depth analysis. Even though a larger shift was obtained with $HfO_2/SiO_2$, this cannot be attributed to a larger degree of intermixing than on the $SiO_2$ since other issues such as charges, reactions may have additional effects. For $Ru_{50}Ta_{50}$/Ru

stacked gates, ~10-20nm thickness of a layer was formed on the surface. The layer was revealed mainly as tantalum and oxygen. The Ta peak can be clearly seen on the surface of the film indicating out-diffusion from RuTa at high temperature to bind with oxygen ambient. However, it was found that Ru peak was higher than Ta near $HfO_2$ and this was also changed from the original composition obtained from the sputtered film. Composition of the $Ru_{50}Ta_{50}$ film changed due to Ta out-diffusion. AES data also shows Ta out-diffuses through Ru grain boundaries to the surface to form oxide. It is attributed that Ta out-diffuse through Ru from $Ru_{50}Ta_{50}$ to surface to from $Ta_xO_y$ layer on the surface. It is believed that TaxOy contributes EOT increase and out-diffusion of Ta may change the composition of RuTa film and thus change work function. Even though a larger shift was obtained with $HfO_2/SiO_2$, this cannot be attributed to a larger degree of intermixing than on the $SiO_2$ since other issues such as charges, reactions may have additional effects.

However, for $Ru_{50}Ta_{50}$ 500 Å gate with the capping layer of W 500 Å on $HfO_2/SiO_2$, it was not observed Ta out-diffusion to the surface after high temperature. It is believed that no significant EOT and effective work function increase after high temperature anneal is related with no Ta out-diffusion and thus no TaxOy formation and no change of composition of RuTa film and thus change work function. To prevent EOT increase, capping or diffusion barrier is needed for this research. From the data (electrical) with W capping layer, EOT didn't increase as much as with Ru overlayer due to no TaxOy formation. No obvious data dielectric can be damaged with this approach, but since too big work function change was observed, there could be possible reaction. From TEM pictures, no evidence was observed that there is void from Ta leaving to form oxide. It is attributed to Ru substitutional diffusion with Ta sites.

In summary, the reason that work function of Ru is higher than Ru/W stack at 400$^{o}$C is attributed to more Ru-O bonding since Ru has no barrier for $O_2$ but W trap $O_2$. Then Ru/W became lower at high temperature than 400$^{o}$C since Ru-O more decompose at higher temperature. Since thinner layer Ru with overlayer Ta shows lower work function at 400C, some amount intermix at 400$^{o}$C is believed to be involved. When underlayer Ru thickness low, intermixing can affect more. Since thinner and thicker Ru underlayer should have same amount of Ru-O bonding and barrier height show similar change as work function change as a function of composition, dependence of work function on the underlayer Ru at 400$^{o}$C is more related with intermixing or stress than Ru-O bonding. If there is available oxygen Ta has stronger tendency to bind with oxygen from Ru-O. Work function of underlayer Ta with overlayer Ru stack is higher than pure Ta at 400$^{o}$C a nd it could be indirect reason since work function of Ta is not related with oxygen profile. For this reason, same intermixing theory can be applied to underlayer Ta with overlayer Ru stacks. Since thinner layer Ta with overlayer Ru shows lower work function than thicker underlayered Ta stack at 400$^{o}$C, some amount intermix at 400$^{o}$C is believed to be involved. W capping doesn't react with underlayer Ta since W peak doesn't change from XRD result.

Since thinner layer $Ru_{50}Ta_{50}$ with overlayer Ru shows higher work function at 400$^{o}$C, some amount intermixing at 400$^{o}$C is believed to be involved. Work function of $Ru_{50}Ta_{50}$ stacks with overlayer Ru at 1000$^{o}$C is higher than 400$^{o}$C since some Ta diffuse out to surface and thus Ta concentration decrease near metal/dielectric interface and thus leaves relatively high Ru composition. Work function of thinner $Ru_{50}Ta_{50}$ with overlayer Ru at 1000$^{o}$C is higher than that of thicker $Ru_{50}Ta_{50}$ with overlayer Ru. Thinner Ta gives relatively more Ta

concentration (higher Ru composition in $Ru_xTay$) decrease near metal/dielectric interface since Ta diffuse out to surface.

## 5.4. Conclusion

Ru and $Ru_{50}Ta_{50}$ alloy vertically layered gate electrodes on the high-k dielectrics were investigated for work function tuning and ease in integration. It was found that $Ru_{50}Ta_{50}$/Ru stacks provided more than 1.0eV increase in work function compared to $Ru_{50}Ta_{50}$. The work function range of these alloys also provides ease in integration. Hence this approach will be advantageous for gate electrode formation on high-k dielectrics. Even though a larger shift was obtained with $HfO_2/SiO_2$ than $SiO_2$, this cannot be attributed to a larger degree of intermixing than on the $SiO_2$ since other issues such as charges, reactions may have additional effects.

## 5.5 References


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**Table 5. 1MOS capacitor Fabrication Process**

- ALD $HfO_2$ /$SiO_2$
- Ru, Ru-Ta Alloys

RF Magnetron sputtering

- Electrode patterning by Lift-off
- Annealing at 400°C for 30min in 10% $H_2$ in $N_2$
- RTA: 800°C for 30sec in Ar

Annealing at 400°C for 30min in 10% $H_2$ in $N_2$

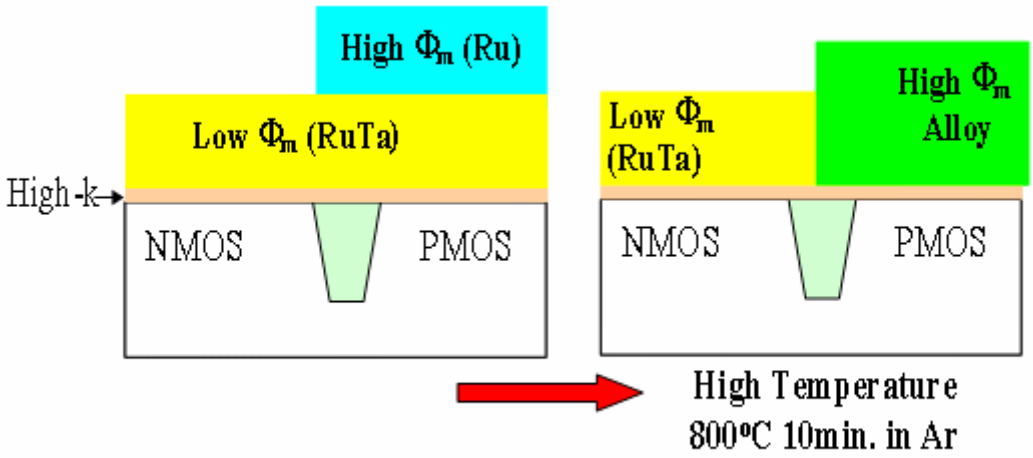



**Figure 5. 1 Integration approach for dual metal gate CMOS on high-k**

**Table 5. 2** Integration details for dual metal gate CMOS on high-k.

| | A | B | C | D |
|---|---|---|---|---|
| Top layer | Ru 500A | Ru 500A | Ru 500A | W 500A |
| Bottom layer | RuTa 30A | RuTa 70A | RuTa 100A | RuTa 500A |

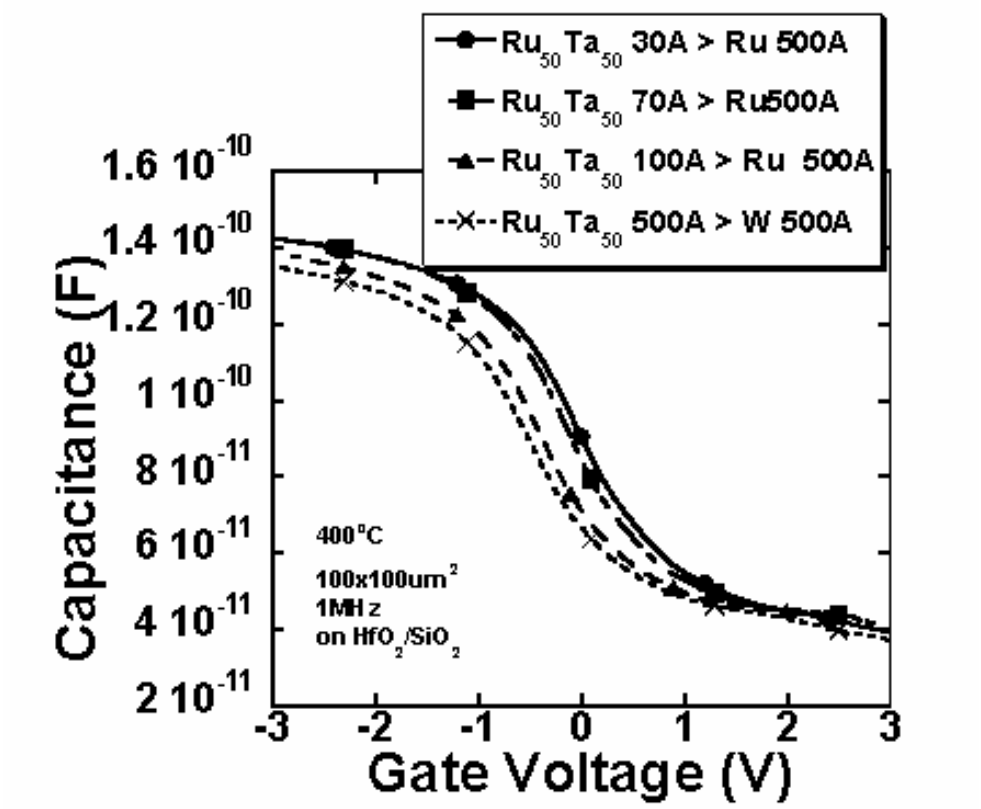
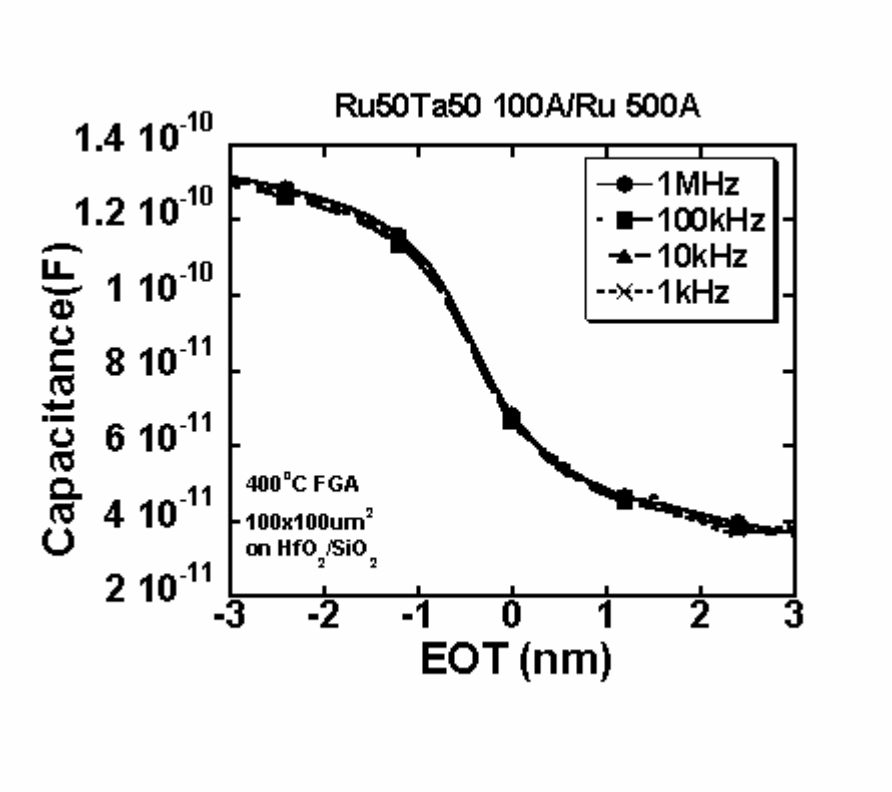
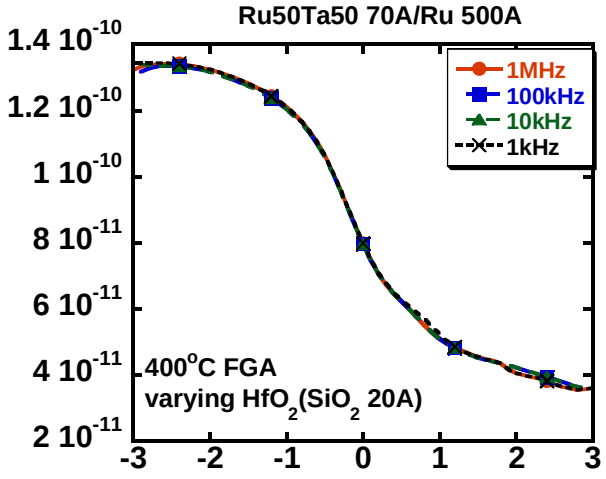



**Figure 5. 2 C - V curves of stacked metal gates on $HfO_2/SiO_2$ after annealing at 400°C**




**(a)**




**(b)**

**Figure 5. 3 C-V curve frequency dispersion of RuTa70/100A with overlayer Ru 500A stacked metal gate on $HfO_2/SiO_2$ after annealing at 400°C**

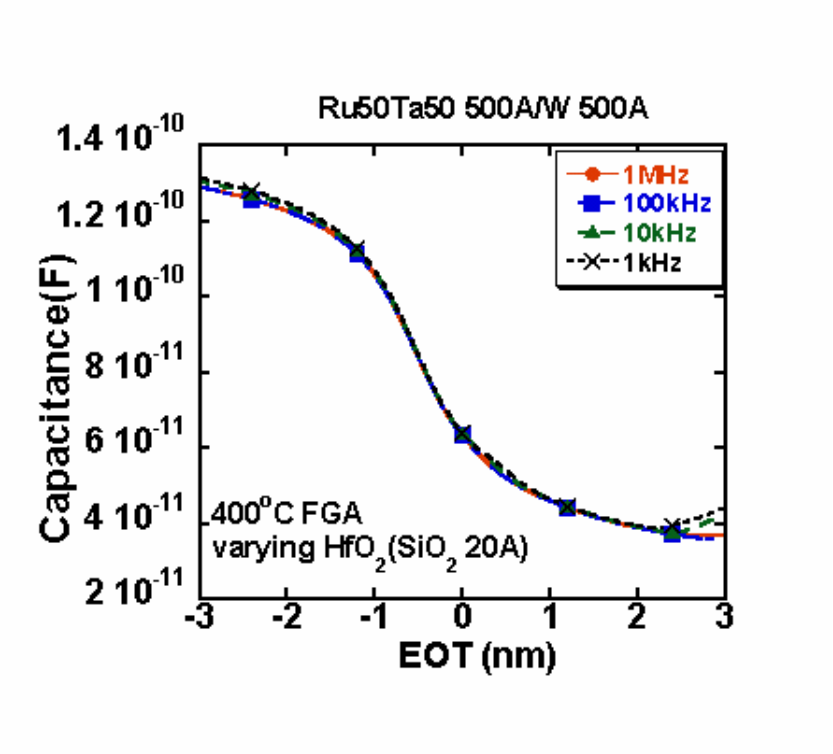



**Figure 5. 4 C-V curve frequency dispersion of RuTa500A/W500A with overlayer Ru 500A stacked metal gate on $HfO_2/SiO_2$ after annealing at 400°C**

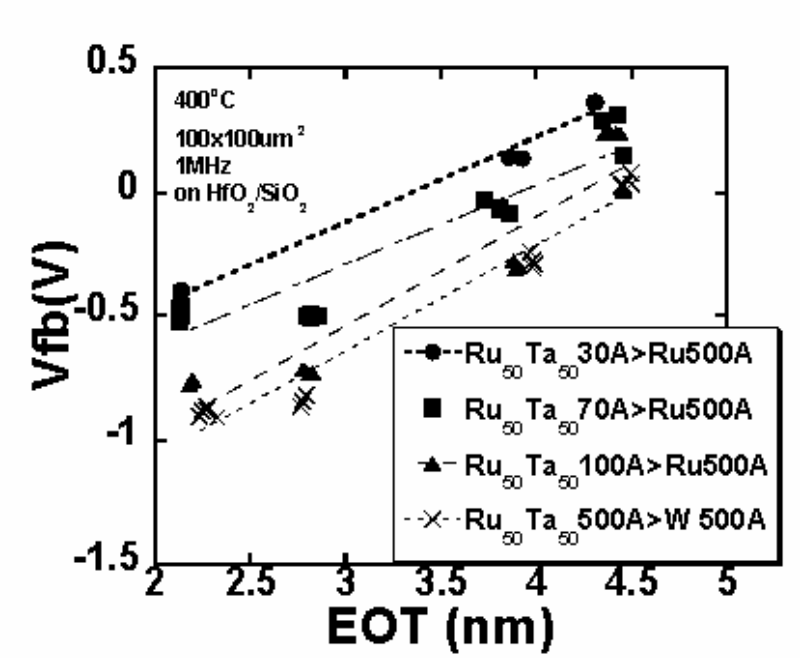



**Figure 5. 5 Vfb vs. EOT curves of stacked metal gates on $HfO_2/SiO_2$ after annealing at 400°C**

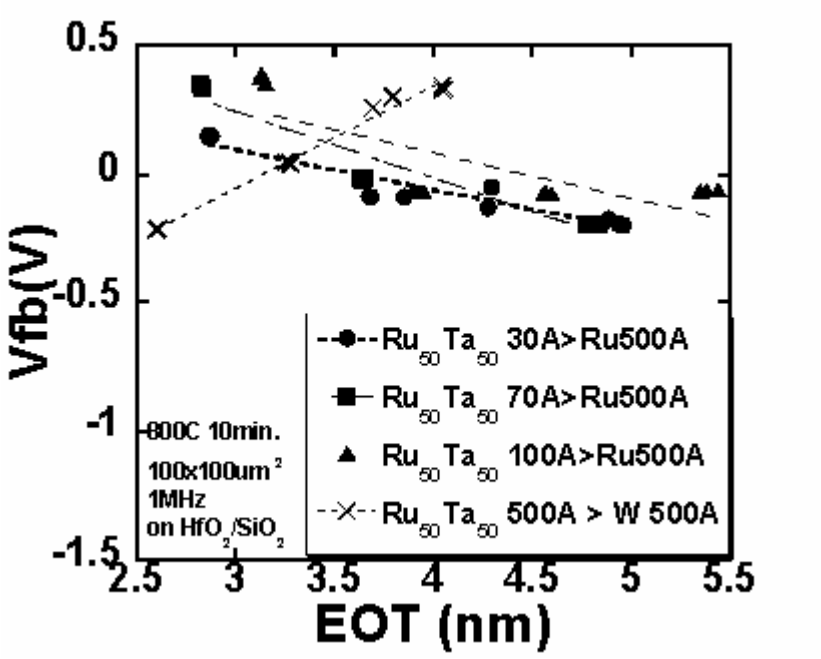



**Figure 5. 6 Vfb vs. EOT curves of stacked metal gates on $HfO_2/SiO_2$ after annealing at 800°C**

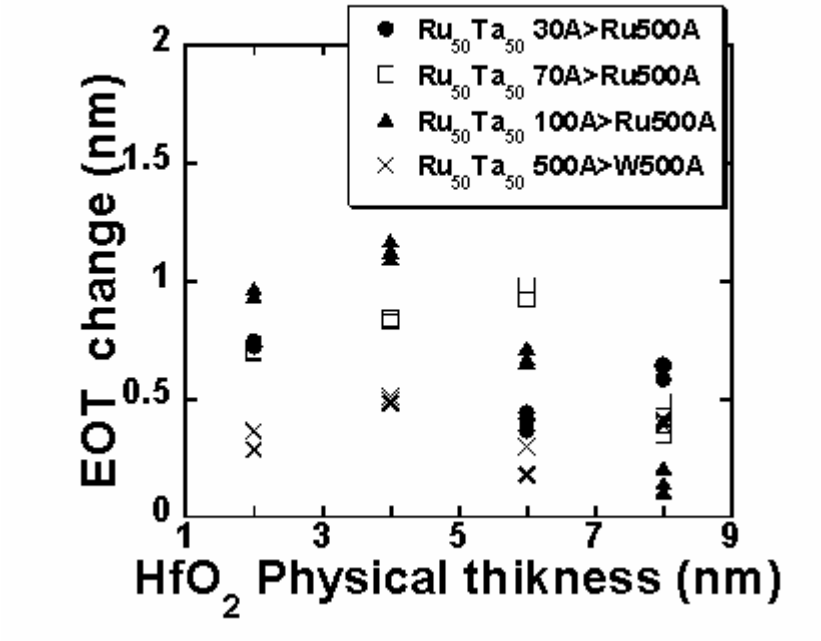



**Figure 5. 7 EOT change vs. $HfO_2$ physical thickness curve of stacked metal gates on $HfO_2/SiO_2$ after annealing at 400°C**

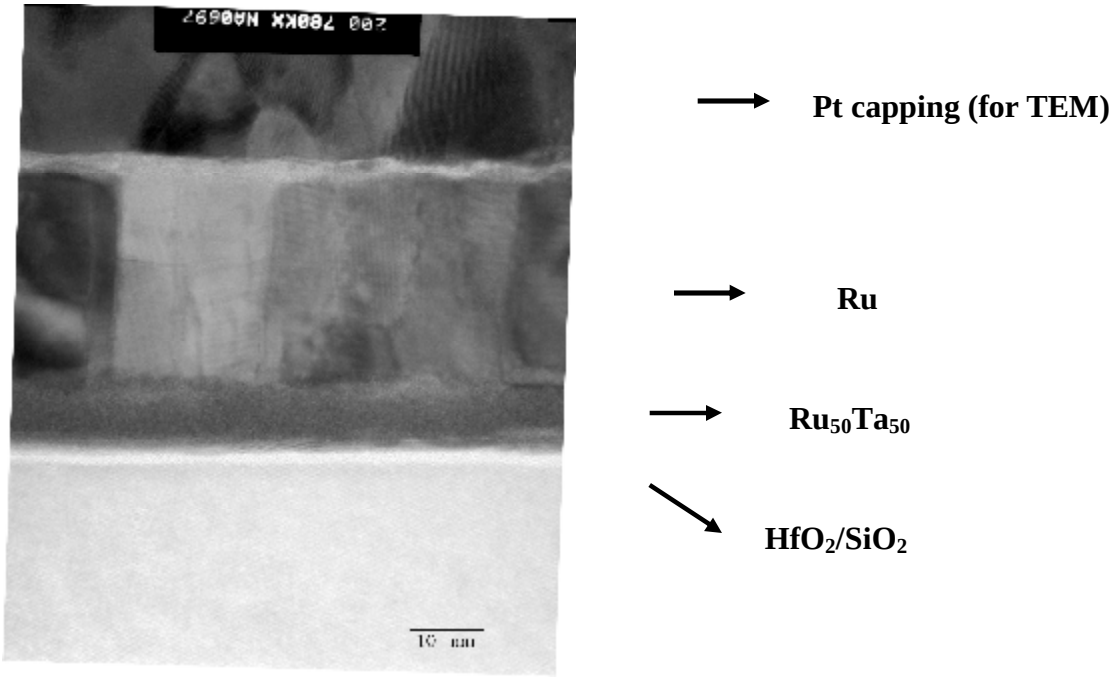



**Figure 5. 8 TEM image of Ru 500A gates with underlayer of $Ru_{50}Ta_{50}$ 100A on $HfO_2/SiO_2$ after annealing at 400°C**

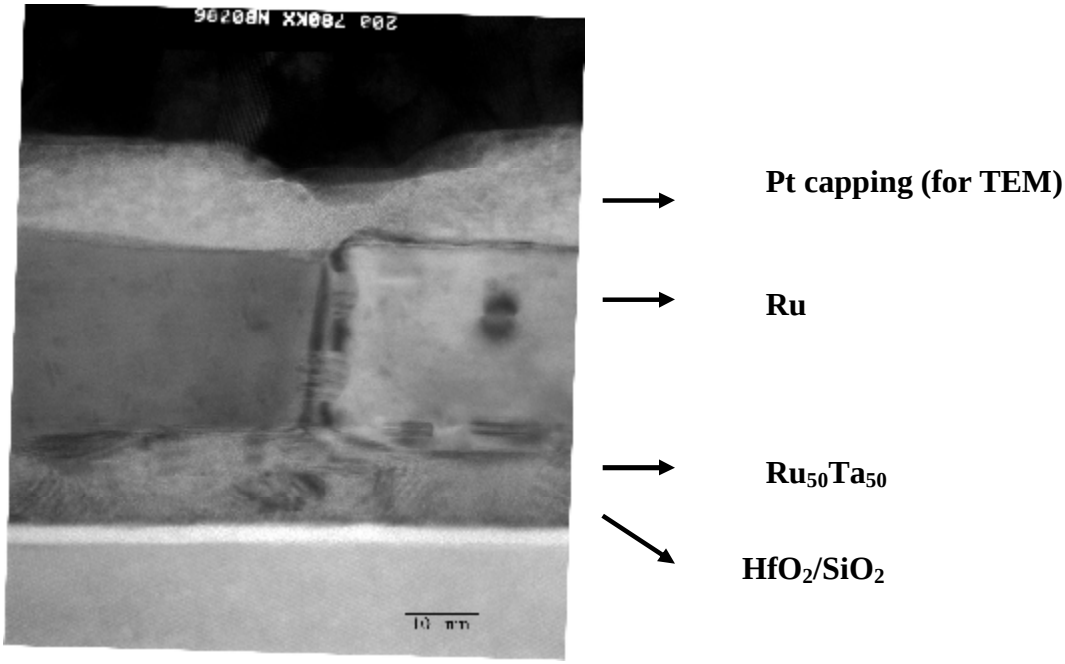



**Figure 5. 9 TEM image of Ru 500A gates with underlayer of $Ru_{50}Ta_{50}$ 100A on $HfO_2/SiO_2$ after annealing at 800°C in 10min.**

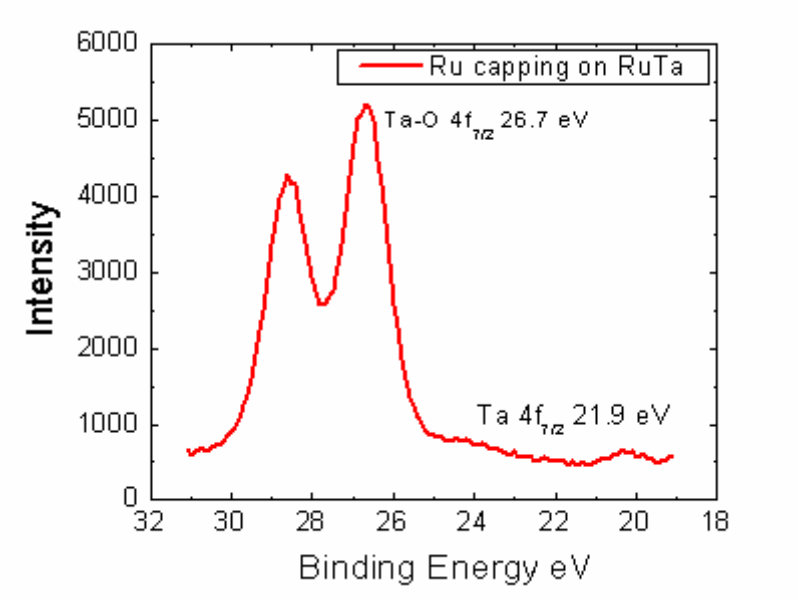



**Figure 5. 10 XPS results of Ru 500A/RuTa 100A stacked metal gates after annealing at 800°C**

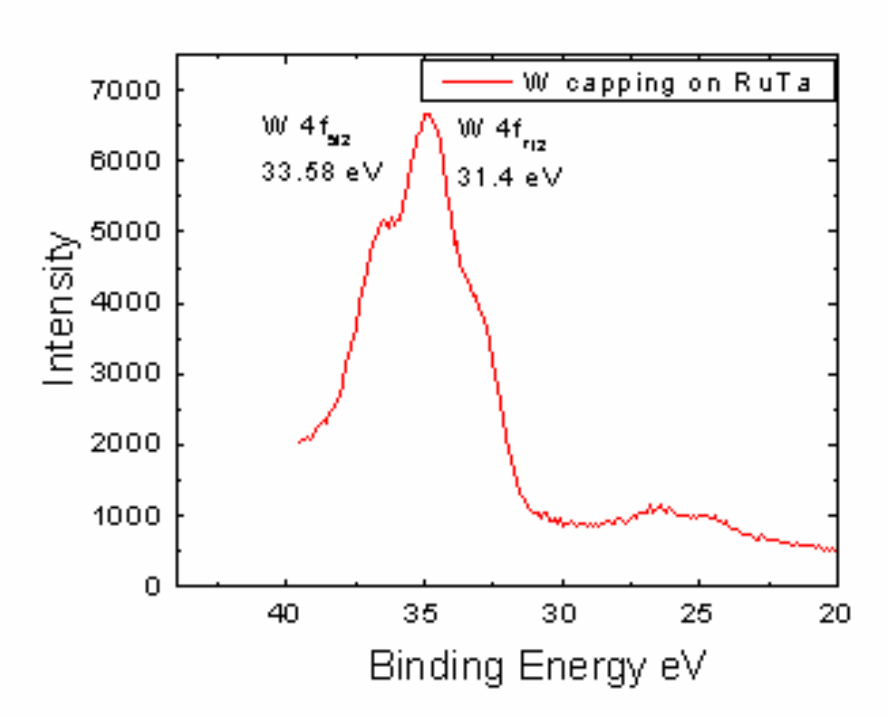
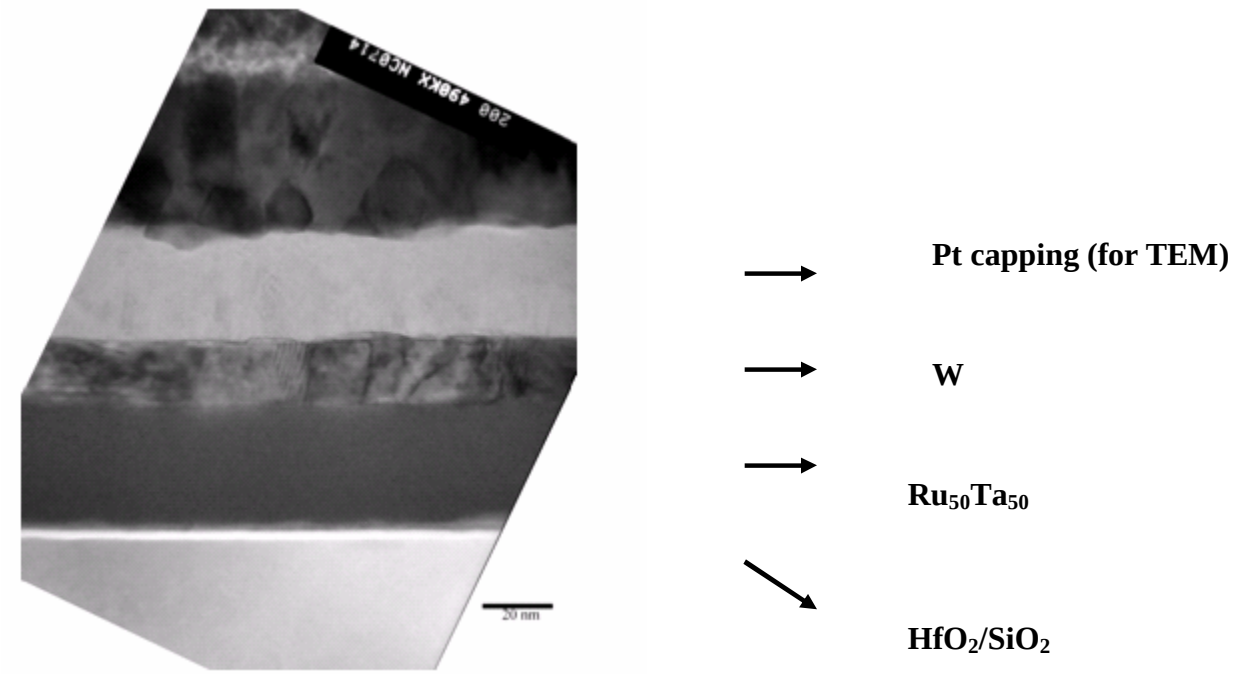



**Figure 5. 11 XPS results of W 500A/RuTa 500A stacked metal gates after annealing at 800°C**




**(a)**

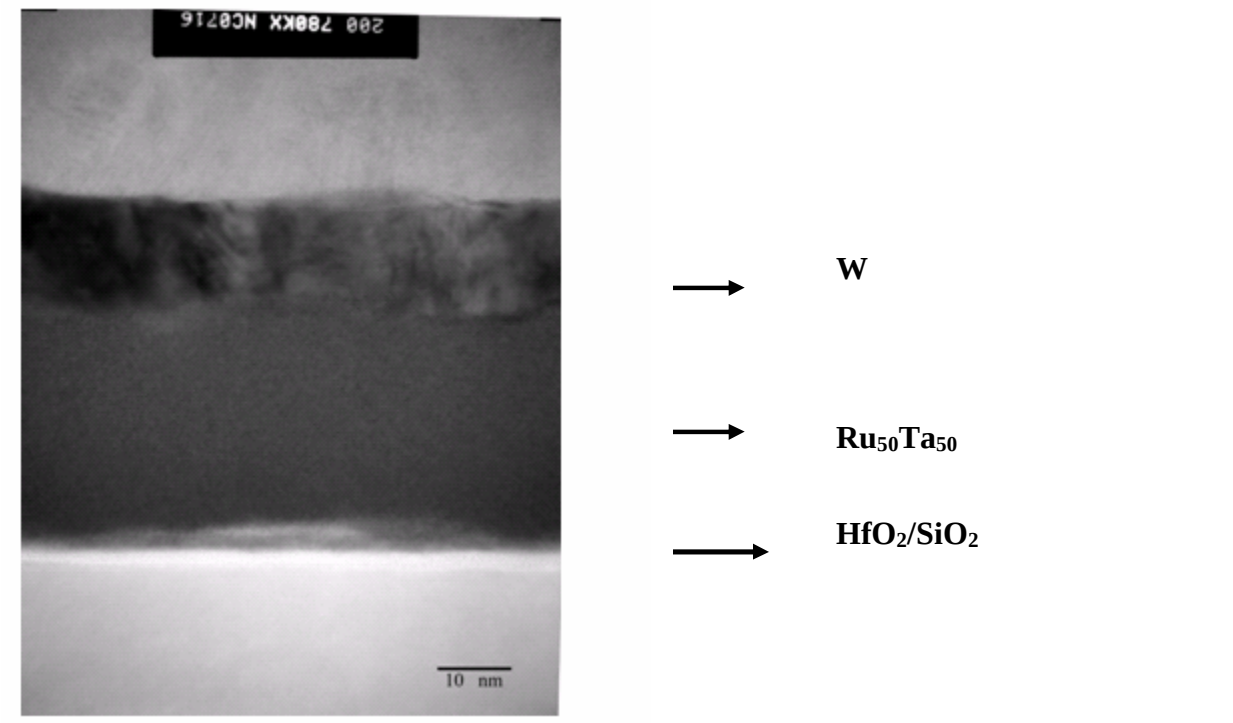
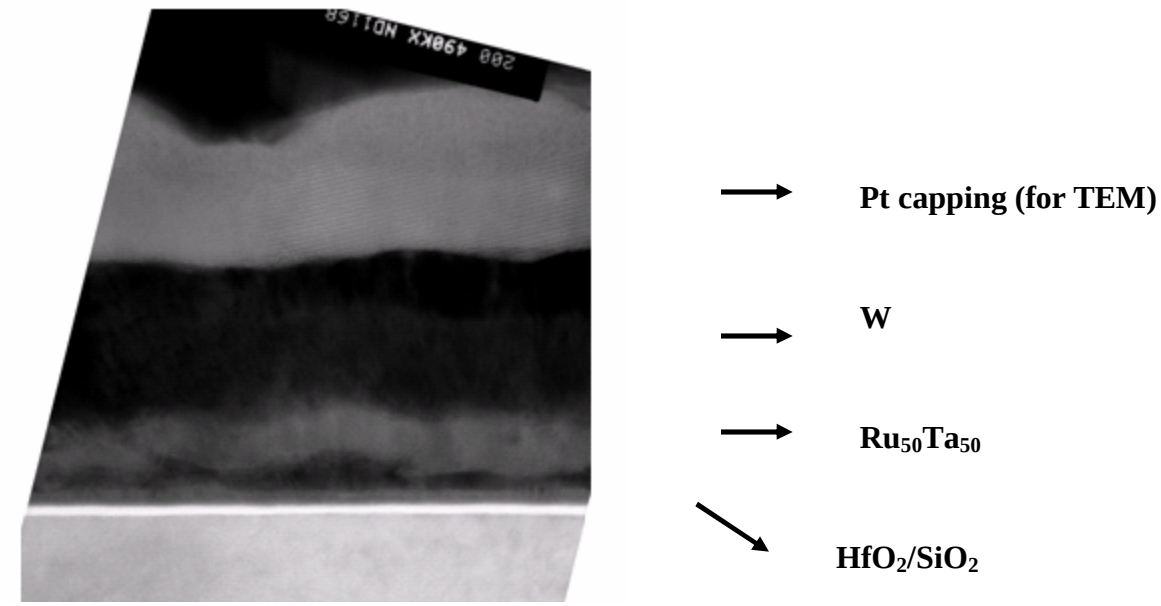



**Figure 5. 12 TEM image of $Ru_{50}Ta_{50}$ 100A with W capping layer on $HfO_2/SiO_2$ after annealing at 400°C**

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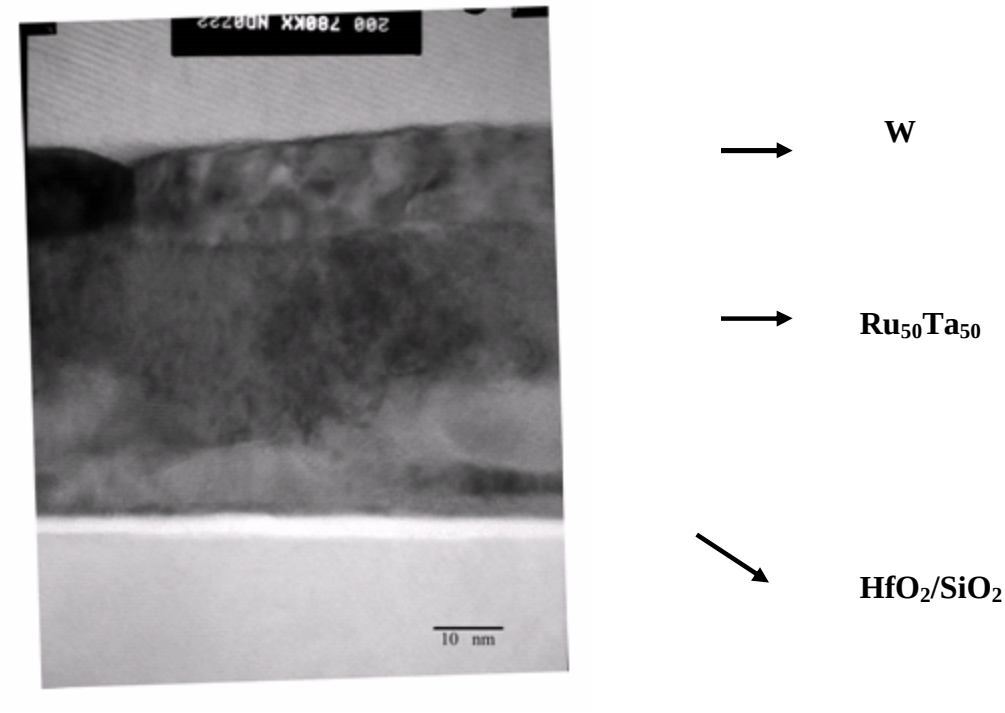



**(b)**

**Figure 5. 13 TEM image of $Ru_{50}Ta_{50}$ 100A with W capping layer on $HfO_2/SiO_2$ after annealing at 800°C**

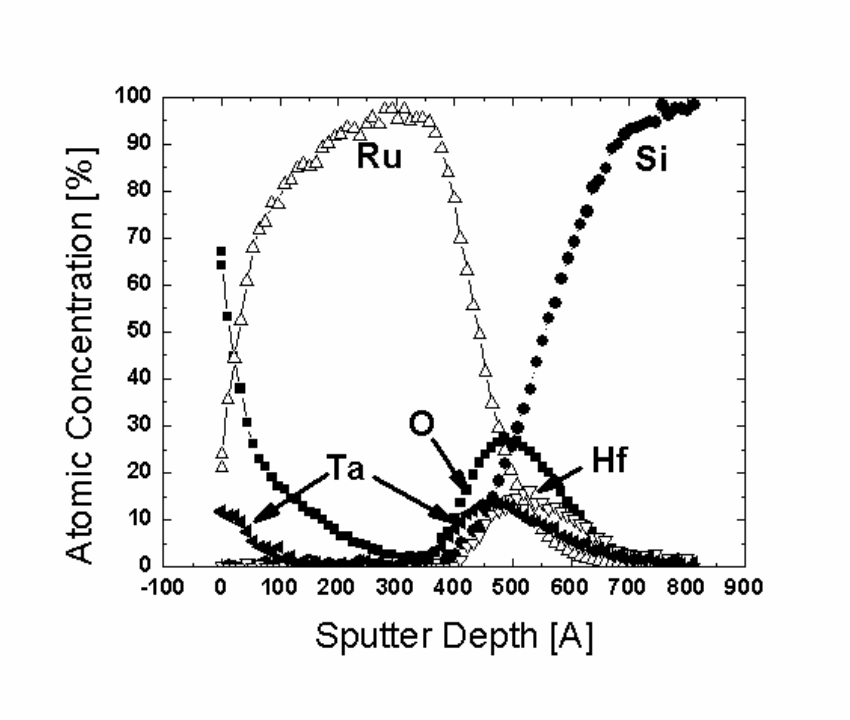



**Figure 5. 14 AES depth analysis of Ru 500A with the underlayer of $Ru_{50}Ta_{50}$ 100A on $HfO_2/SiO_2$ after annealing at 800°C for 10min.**

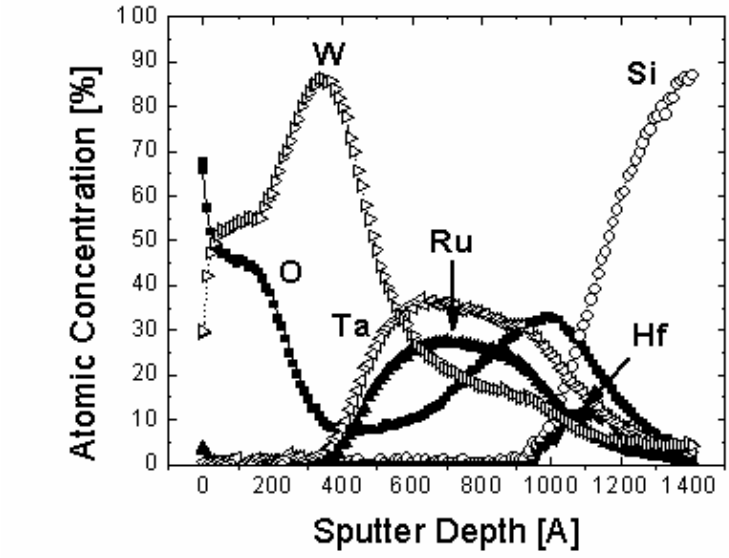
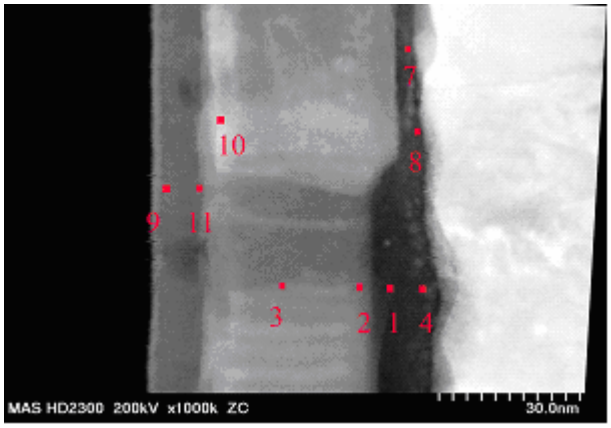



**Figure 5. 15 AES depth analysis of $Ru_{50}Ta_{50}$ 500A with capping layer 500A W on $HfO_2/SiO_2$ after annealing at 800°C for 10min.**



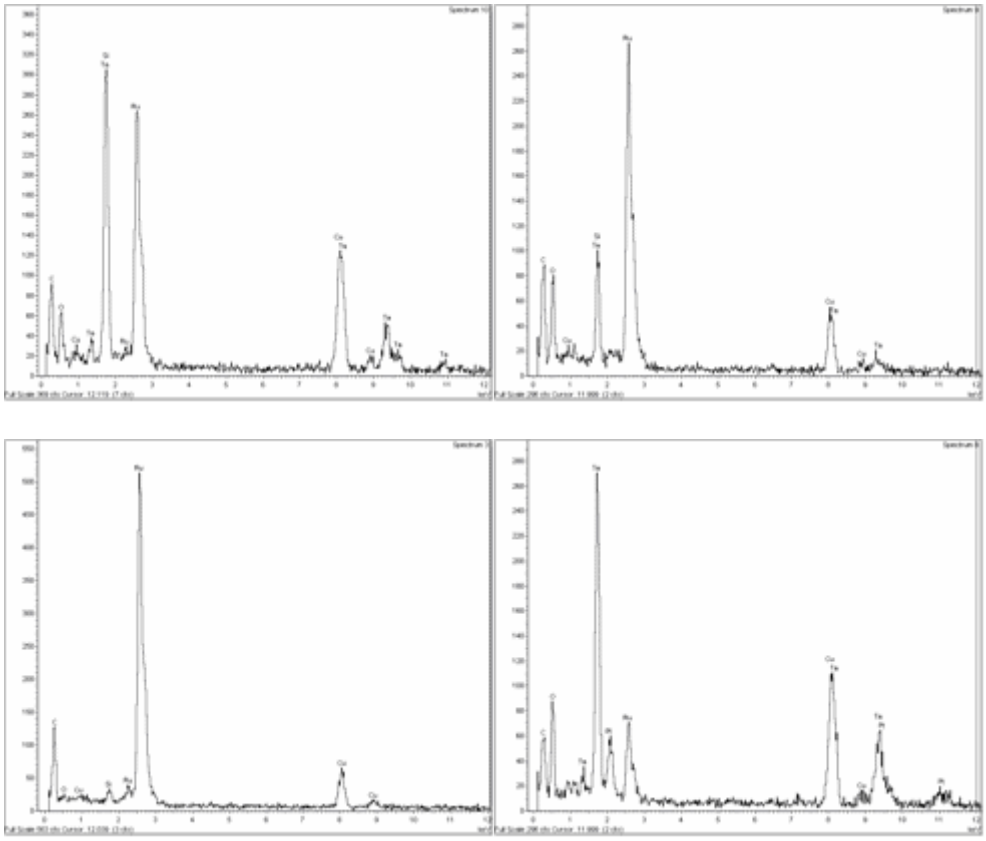



**Figure 5. 16 EDX/STEM analysis of Ru 500A with the underlayer of $Ru_{50}Ta_{50}$ 100A on $HfO_2/SiO_2$ after annealing at 800°C for 10min.**

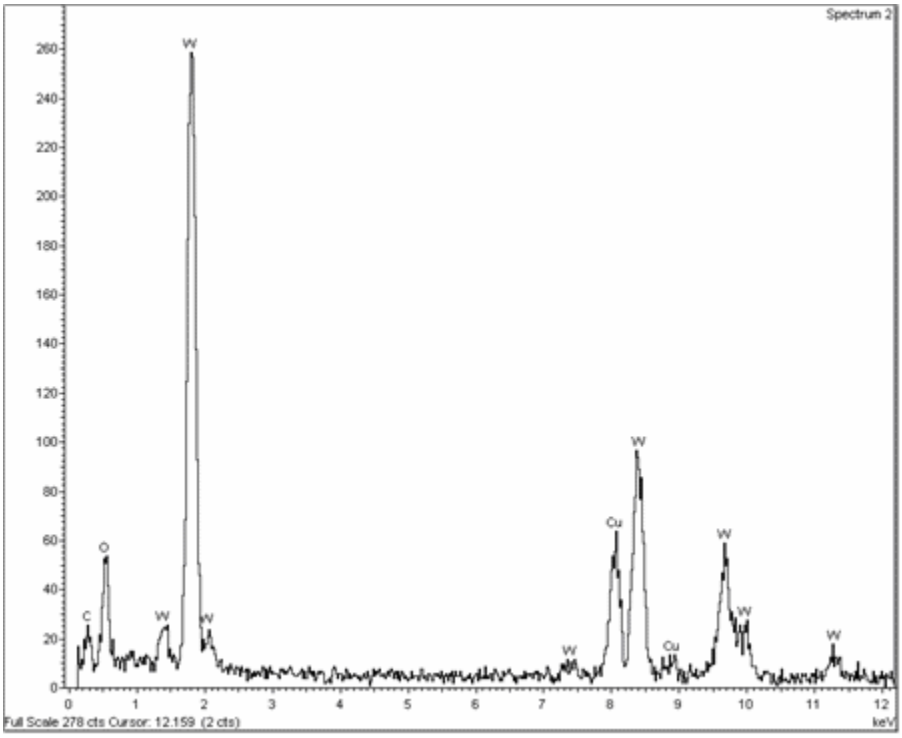



**Figure 5. 17 EDX analysis of surface of $Ru_{50}Ta_{50}$ 500A with capping layer W 500A on $HfO_2/SiO_2$ after annealing at 800°C for 10min.**

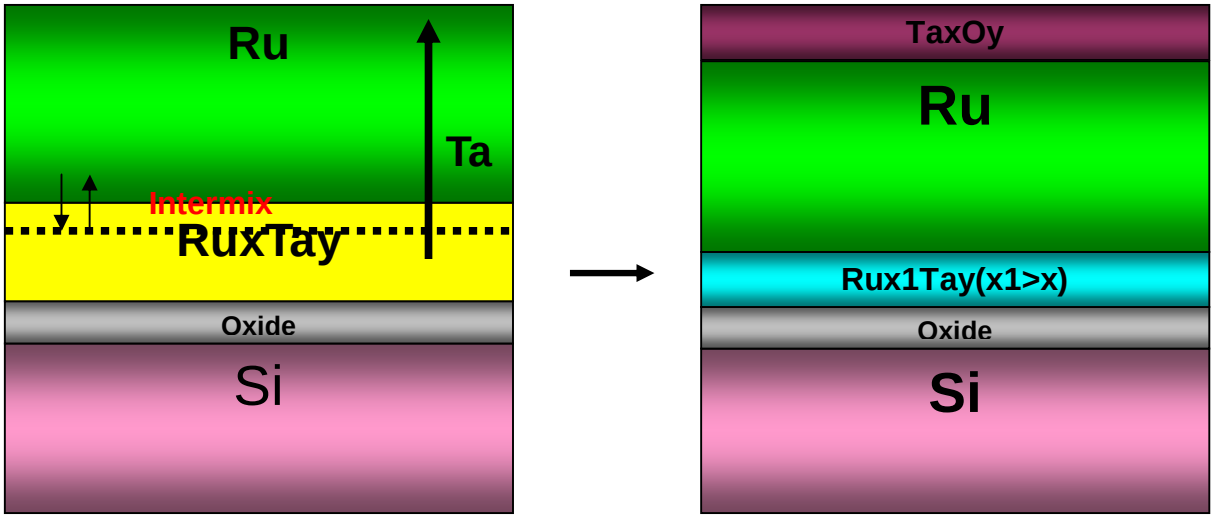



**Figure 5.18 Schematic of Ru 500A with the underlayer of $Ru_{50}Ta_{50}$ 100A on $HfO_2/SiO_2$ after annealing at 800°C for 10min**

# *Chapter 6* Summary and Future Work

## 6.1. Conclusion

This dissertation has focused on the research of the interactions between metal and high-k dielectrics and also explores a plausible scheme of integration for dual-metal-gate CMOS devices. Here are some important conclusions achieved in the past years.

First, we have investigated compatibility of dual metal gate electrodes such as Ru, Ru-Ta alloy, TaN and TaSiN on low EOT single layer $HfO_2$ and stacked $HfO_2/SiO_2$ gate dielectrics for CMOS and found that the work function of metal gates on $HfO_2$ and $SiO_2$ are similar. In addition, TaSiN resulted in the lowest EOT owing to its excellent oxygen diffusion properties out of all the gates. Thermal annealing studies of selected metals on the above dielectrics were also performed to study the change in EOT and $V_{FB}$ values. The properties of metal gates on $HfO_2$ were found to be similar to those on $SiO_2$. In extracting the work function values, the charges in the high-K dielectric must be included. Although Fermi level pinning was not observed, the charges in the $HfO_2$ layer must be reduced to obtain the desired threshold voltages. Front and backside SIMS suggests that Ru does not suffer from diffusion problems through $HfO_2$ dielectrics at high temperature.

Second, the effect of the capping layer on the top of the gate electrodes was explored. Different thickness of Ru with the capping layer of the tungsten was used. The observed lower $V_{FB}$ for the capped Ru stack can be attributed to either a different effective work function at the interface of Ru and $SiO_2$ for the capped films or a difference in work function associated with stress profile changes. The uncapped Ru and thick W capping samples suffered from peeling after $1000^oC$ anneal. It was shown that gate electrode with capping layer needs to be thick enough or protected from the diffusion for high temperature stability.

AES depth profiling shows that significant amount of the oxygen or tungsten can diffuse into film. However, the amount of diffusion depends on underlayer, overlayer and history of heat treatment.

Third, integration of bi-layered metals with good modulation of the work function for the gate electrodes for P-MOSFET and N-MOSFET devices on the $SiO_2$ dielectrics was developed. Vertical stacks of Ru and Ta layers were subjected to high temperature anneals to promote intermixing which resulted in work function tuning. The Ru gates with the over-layer of Ta have excellent EOT stability at high temperatures. However, Ta underlayers are unstable on dielectrics, and Ru underlayers resulted in limited work function tuning. To increase work function change, stacks of $Ru_{50}Ta_{50}$/Ru were also evaluated and higher amount of change in work function was observed between $Ru_{50}Ta_{50}$/Ru and $Ru_{50}Ta_{50}$ electrodes. For $Ru_{50}Ta_{50}$ underlayers with Ru overlayers, nearly ~0.8eV shift in work function is observed as compared to the single $Ru_{50}Ta_{50}$ layer making this an attractive approach for bulk CMOS.

Finally, Ru and $Ru_{50}Ta_{50}$ alloy vertically layered gate electrodes on the high-k dielectrics were investigated for work function tuning and ease in integration. It was found that $Ru_{50}Ta_{50}$/Ru stacks provided more than 1.0eV increase in work function compared to $Ru_{50}Ta_{50}$. The work function range of these alloys also provides ease in integration. Hence this approach will be advantageous for gate electrode formation on high-k dielectrics. Even though a larger shift was obtained with $HfO_2/SiO_2$, this cannot be attributed to a larger degree of intermixing than on the $SiO_2$ since other issues such as charges, reactions may have additional effects.

## 6.2. Future work

In the past years, metal gate and high-k dielectrics have been intensively investigated. In order to apply real devices more research will be needed. My work shows ease of integration to apply real process and some fundamental understanding is still needed such as interfacial dipole and oxygen impact on gate and dielectrics. All of these issues were studied in our research. The material selection of metal gates and high-k dielectrics is still going on. Since oxygen plays a critical role for gate stacks and can diffuse easily through gate stacks, material selection of metal gates to monitor and control oxygen profile strictly. Based on my work on capping layer, some oxygen diffusion barriers such as TaSiN is the possible choice for capping layer in the near future.

# Appendix

## *Properties of Ru-Mo Gate Electrodes and Future Work*

In this chapter, properties of Ru-Mo alloy films on high-k dielectrics were evaluated as gate electrodes for P- MOSFET devices in detail. Electrical properties of the reactive sputtering deposited Ru-Mo alloy films with various film compositions were evaluated as gate electrodes on MOS capacitors.

### 1. Introduction

As field effect transistors are scaled deep into the sub-micron region, advanced high-k gate dielectrics and metal gate electrodes will be required to obtain equivalent oxide thickness, $T_{ox-eq}$, < 1.0 nm. The search for metallic gates faces many challenges since they must have compatible work functions, process compatibility with dielectric deposition, and thermal/chemical interface stability with dielectrics.

Alternative metal gates for PMOS including elemental metals, metal nitrides, metal silicides or other metallic alloys have been intensively investigated [1, 2]. However, most high work function metal gate electrodes studied to date suffer from high temperature instability resulting in lower work function for PMOS gates. Metals such as Ru, Ir, and Pt have been reported as gate electrodes for P-MOSFET devices [3-6]. However, gate electrodes for PMOS (work function if metal gates near 5.2eV) have more challenges than NMOS gates (work function of metal gates near 4.0eV). Firstly, oxygen diffusion through high work function elemental metals will be higher than through alloys or nitrides due to lack of reactivity. Second, high work function elemental metals may also diffuse through

grain boundaries of crystalline dielectrics. Increased focus on alloys for PMOS metals may be necessary to obtain a high thermal budget compatible solution.

In searching for an alternative gate electrode, the electrode materials should satisfy several requirements, such as proper work function, low electrical resistivity, high thermal stability, good oxidation resistance and good adhesion to dielectrics. Ru film has been studied as a PMOS gate electrode because of its low resistivity, proper work function and high carrier concentration. However, there are some needs to get optimize PMOS gate electrode with proper properties since it is difficult to obtain elemental metals that satisfy all of the criteria mentioned above. Elemental metals with high work function such as Ru and Pt, are PMOS gate electrode candidates but they have adhesion issues on $SiO_2$ and high-k dielectrics under high temperature. Also diffusion of elemental metal at high temperature can be improved by making alloy elemental metal and alloy can minimize effect of capping layer. Given the above issues with elemental high work function metals, it is desirable to seek alternate routes in obtaining high work function PMOS gates. As well as obtaining the high work function material for PMOS gate applications, the alloys may also offer thermodynamic stability and better diffusion property.

The target of this chapter is to obtain a Ru-based alloy with high work function which also has good thermal stability.

Molybdenum is a transition metal and has one of the highest melting points (2623°C) of all pure elements. The structure of Mo is bcc. The work function of Mo is about 4.6~5.0 eV. Mo melting point is 2623 °C and the resistivity is bout 5.47 μΩ.cm at 25 °C.

The Ru-Mo alloy system has not been experimentally studied for semiconductor applications, although Ru-Mo has been studied for superconducting applications, catalysts. In

addition, Ru-Mo-Si multilayer has been studied for masks. The Ru-Mo phase diagram is plotted in Figure 1. The solid solubility of Mo in Ru is 35 atomic percent whereas the solubility of Ru in Mo is 10 atomic percent, which makes it difficult to get a single Ru phase alloy. Other regions consist primarily of mixtures of Ru and Mo phases. Since the work function of Ru and Mo are both close to the valence band of Si, a high work function proper for PMOSFET is expected to occur in the Ru-Mo alloy system and is anticipated to be linearly dependent on the alloy composition. The work function and heat of alloy phase formation are important to determine if the Ru-Mo alloy is a proper candidate for gate electrode. The Ru-Mo alloy therefore is expected to be an appropriate candidate as a PMOSFET gate electrode material in our research because it is expected high work function and better adhesion property on the $SiO_2$ and high-k gate dielectrics even at high temperature. In the following sections, we will discuss the properties of Ru-Mo alloy film as gate electrode material in detail.

## 2. Experimental of Ru-Mo Alloy on High-k dielectrics

In our research, Ru-Mo alloy thin films were deposited using an ultra-high-vacuum (UHV) DC magnetron sputtering system. The MOS capacitor fabrication process is summarized in Table.1. The gate oxides were a thickness of 20Å~80Å of single layer $HfO_2$ and varying thickness of 40Å~150Å of $HfO_2$ with varying thickness of 40Å~150Å of the under-layered $SiO_2$ to get work function of the gate electrode of Ru-Mo alloy on $HfO_2$. $HfO_2$ layers were deposited via and thermal $SiO_2$ were grown at 900$^{o}$C. Samples in Set I consisted of fixed top $HfO_2$ physical thickness of 60A over varying interface $SiO_2$ (40, 60, 80, 100 and 150A). Set II consisted of varying top $HfO_2$ $SiO_2$ (40, 60, 80, 100 and 150A) physical

thicknesses over fixed interface $SiO_2$ (40A). The Ru-Mo alloy films with 70nm thickness were deposited by co-sputtering from both 2-inch Ru (purity of 99.95%) and Mo (purity of 99.95%) targets, simultaneously in a system with a base pressure of ~$5x10^{-9}$ Torr. The sputtering rate is 3nm/min for both Ru and Mo targets at 100W sputtering power. Alloy films containing various Ru/Mo ratios were deposited by adjusting the RF power fed into the Mo and Ru targets to change the composition as shown in Table 1. No intentional heating was applied to the Si-substrate. The sputtering power of Mo was varied (25W-100W) and the sputtering power of Ru was also varied (50W-100W) simultaneously in order to obtain $Ru_xMo_y$ alloy films. Sputtering was carried out in Ar gas ambient at 5.4mTorr. Total 4 sputtering conditions were performed. W layers with thickness of ~60nm were used as capping layers to prevent possible adhesion issue of Ru based metal gate on the dielectric. The substrates used were p-Si wafers. The $Ru_xMo_y$ gate electrodes were patterned using lift-off lithography. All samples were annealed in 10% $H_2/N_2$ at 400°C for 30 min. High temperature rapid thermal annealing (RTA) in Ar ambient is employed in order to activate the source and drain ion implantation of CMOS devices. The alloy films were then annealed by RTA in argon to simulate the actual CMOS process and various RTA treatments (800°C 30sec, 900°C 30sec and 1000°C 10sec) of the alloy films were performed in Ar. C-V and I-V characteristics were obtained using HP4284 and HP4155B, respectively .The capacitance was measured on an area equal to $2.5x10^{-5}cm^2$ at 1MHz. The flat-band voltage ($V_{FB}$) and equivalent oxide thickness (EOT) for the capacitors were obtained by using the NCSU CV program [7].

The properties of the alloy films were studied both before and after rapid thermal anneal (RTA). Rutherford Backscattering Spectrometry (RBS) analysis was used to get

quantitative determination of absolute concentrations of thin film of co-sputtered Ru and Mo with W capping layer. Secondary Ion Mass Spectrometry (SIMS) analysis was utilized to examine the diffusion behavior among alloy films/$HfO_2$/interfaces/Si-substrate. The crystal structure of the films was determined by X-ray diffraction (XRD).

## 3. Electrical properties of Ru-Mo Alloys on High-k dielectrics

In this chapter, we report the electrical characteristics of devices using Ru-Mo alloy film gate electrodes on $HfO_2$ dielectric.

Figure 2 shows the C-V characteristics of P-MOSFET with co-sputtered Ru 100W and Mo 25W alloy gate electrode on $HfO_2$ 40A after a forming gas anneal at 400ºC. The capacitance was measured at a frequency of 1MHz on an area equal to $2.5x10^{-5}cm^2$. From RBS analysis, the Ru and Mo atomic contents for Mo (25W) and Ru (100W) were calculated to be 94%, 6%, respectively.

In order to decouple the effect of fixed charge from the work function, C-V measurements on several oxide thicknesses were used to generate a $V_{FB}$ vs. EOT curve as shown in Figure 3. The equation for $V_{FB}$ as proposed by Jha [8] was used to obtain the effective work function.

The extracted work function values for all $Ru_xMo_y$ alloys with varying Mo contents after a forming gas anneal at 400ºC range from 5.0-5.3 eV as shown in Figure 4. In order to get the exact amount of concentration of co-sputtered Ru and Mo layers, RBS analysis was performed. As table 1 shows, Mo concentrations range from 6% atomic percent at co-sputtered Ru100W and Mo25W alloy to 50% atomic percent at co-sputtered Ru50W and Mo100W alloy. Mo has been shown to give different work function values in particular

orientations. The work function of Mo is reported about from 4.6eV to 5.0 eV (110 on $SiO_2$) [9]. For an $A_xB_{1-x}$ alloy such as Ni-Cu alloy system [10], it is natural to consider that the work function $\phi(x)$ changes with x as $\phi_{average}(x)= x\phi_A+(1-x)\phi_B$, where $\phi_A$ and $\phi_B$ represent the work function of pure elements. Since work function of $Ru_xMo_y$ is from 5.0-5.3 eV, Mo in this alloy might be high work function. However, this is not necessarily the case for all binary alloys such as the work function of Ag-Au alloys and Pt-Rh alloys [11]. The relationship between charge transfer in alloys and electronegativity, work function resulting from the modified electron-electron Coulomb has been used to explain the non-linear relationship between the work function and alloy composition [12]. In our research, a non-linear relationship between work function and Ru-Mo alloy composition was observed especially in Ru 50W Mo 100W alloy.

The thermal stability of the films was evaluated by annealing the samples in Ar at 800°C for 30sec, 900°C for 30sec and 1000°C for 10sec. After 800ºC annealing, negligible change in work function values of co-sputtered Ru 100W and both Mo 50W and 100W was observed. The stability of the work function suggests that these films are stable on $HfO_2$ up to 800°C. About 0.2~0.3eV of decrease in work function was observed after 900ºC annealing indicating that the reduction in work function of the samples is directly related to the oxygen content at the $Ru_xMo_y$-$HfO_2$ interface. However, after 1000°C anneal, work function of all gates increased back to ~4.95eV-5.0eV except for Ru 50W and Mo 100W, which still shows ~4.8eV. These results show that high temperature property of $Ru_xMo_y$ alloy films with composition of less than Mo 50 atomic % is different than other $Ru_xMo_y$ alloy gates and exhibits similar high temperature property to Ru gates. This is attributed to a different structure of $Ru_xMo_y$ (y>38 at 1000°C: Ru +Mo mixture) than other gates with

different structure (Ru phase with Mo) from phase diagram. However, XRD shows RuMo phase which does not exist in the phase diagram.

Figure 5 shows the work function as a function of Mo composition and it decrease as Mo composition increases. This result is markedly different for Ru 50W Mo 100W alloy compared to the previous set indicating alloy composition of Ru 50W Mo 100W is different than previous set. This is attributed to differences in sputtering tool setup.

Figure 6 shows a $V_{FB}$ vs. EOT curve from C-V measurements of co-sputtered Ru 100W and Mo 25W alloy gate electrode ($2^{nd}$ set of $Ru_xMo_y$) after a forming gas anneal at 400ºC of the on varying $SiO_2/HfO_2$ in order to decouple the effect of fixed charge from the work function. Linear curves were observed and their slopes at 400$^o$C and 800$^o$C were similar. However, at 900$^o$C and 1000$^o$C show smaller values of slope indicating smaller charges after high temperature anneal. $V_{FB}$ decreases at 800$^o$C and increase back at 1000$^o$C. EOT shows negligible change of at high temperature.

Figure 7 show a $V_{FB}$ vs. EOT curve from C-V measurements of co-sputtered Ru 100W and Mo 25W alloy gate electrode ($2^{nd}$ set of $Ru_xMo_y$) after a forming gas anneal at 400ºC of the on varying $HfO_2$. The intercept and slopes of the linear curves were observed and the slopes at 400$^o$C and 800$^o$C were similar and after 800$^o$C anneal $V_{FB}$ decreased indicating that the reduction in work function of the samples is directly related to the oxygen content at the $Ru_xMo_y$-$HfO_2$ interface. After a 900$^o$C anneal, these values decrease more, and EOT further increased. However, those at 1000$^o$C show higher values showing similar trend on varying $HfO_2/SiO_2$ at high temperature. EOT shows significant change at high temperature indicating large amount of reaction with intentional $SiO_2$.

Figure 8 shows the EOT change of as Ru 100W Mo 25W on varying $HfO_2/SiO_2$ after different anneal. Negligible EOT change was observed at high temperature in $HfO_2/SiO_2$. However, as shown in Figure 9, EOT increased significantly at high temperature on thin $HfO_2$ indicating reaction at high temperatures.

The thermal stability of the films was evaluated by annealing the samples ($2^{nd}$ condition) in Ar at $800^oC$ for 30sec, $900^oC$ for 30sec and $1000^oC$ for 10sec. After 800ºC annealing, a decrease in work function values for all conditions was observed as shown in Figure 10. However, the values of decreased amount were different. However, after $1000^oC$ anneal, work function of all gates increased back to ~4.9eV-5.1eV. These results at $1000^oC$ show similar behavior as the $1^{st}$ condition. Figure 11 shows that the work functions of Ru-Mo gates on varying only $HfO_2$ after different temperature anneal. After an $800^oC$ anneal, work function values decrease and those at $900^oC$ decrease even more. However, work function value increased after $1000^oC$.

## 4. RBS analysis of Ru-Mo Alloy Films

Rutherford backscattering spectroscopy (RBS) analysis was utilized to analyze the composition of the alloy films. RBS analysis was performed on the samples in order to detect the compositions of the alloy films on thick $SiO_2$ using 2MeV He. RBS simulations were done using SIMNRA 4.0 program. RBS simulation compositions of an as-deposited alloy film with sputtering power Mo (25W-100W) and Ru (50W-100W) are shown in the Table 1. The Ru and Mo atomic contents for Mo (25W) and Ru (100W) were calculated to be 94%, 6%, respectively. As sputtering power of Mo was increased, the Ru and Mo atomic contents

for Mo (100W) and Ru (50W) were calculated to be 50%, 50%, respectively. Thickness obtained from the RBS simulation was smaller than expected from the sputtering condition.

It should be pointed out that Ru and Mo RBS signals overlap substantially and Ru/Mo ratios were very difficult to estimate. The RBS analysis demonstrates (not shown) that Ru or Mo diffuse into top W layer for all annealed samples at 900$^{o}$C for 30sec in Ar (it was simulated as uniform Ru concentration in W but, it could be as well Mo in W or mixture of Mo and Ru in W). RBS results indicate that concentration of Ru or Mo gradually changes with W layer depth indicating grain boundary diffusion. Similar W diffusion was observed into $Ru_xMo_y$ layer. Concentration of W gradually changes with $Ru_xMo_y$ layer depth indicating grain boundary diffusion. It was not observed any diffusion in unannealed samples.

Table 2 shows the summary of the RBS simulation compositions and thicknesses after 900$^{o}$C 30sec in Ar.

## 5. X-Ray diffraction analysis of Ru-Mo films

The crystal structure of the films was determined by X-ray diffraction (XRD) using Cu Kα radiation. X-ray analysis of the Ru-Mo alloy films annealed at 400$^{o}$C indicated that all of the films which were annealed at 400$^{o}$C were crystalline. Figure 2 shows the XRD analysis for the films annealed at 400$^{o}$C. As shown, Ru phase was found to be dominant in Ru-enriched films. The Ru (002) and (101) phases in Ru-enriched film diminished with increasing Mo content and RuMo (002) became dominant in alloys with Mo at. content of 50 %. A single phase region is not obtained as it was expected from binary phase diagram of Ru-Mo. Further increase of Mo content resulted in the formation of RuMo (002) phase, which is second dominant in the Ru-Mo alloy samples with 38 % < Mo atomic % < 50%.

After 1000ºC RTA, XRD patterns were also obtained and are shown in Figure 3. For the Ru-Mo alloy with Mo at. % content of 38, many Ru-Mo phases appeared. Narrow diffraction peaks, observed for annealed $Ru_xMo_y$ films, suggest that grain size growth occurred upon annealing. The driving force for grain growth is the surface energy of the grain boundaries. The larger the grain size, the smaller the amount of grain boundary, and so the lower its energy is expected to be.

As shown, Mo phase was found to be dominant in the alloy films with the atomic Mo% is 38% and 50% while the Ru peaks were found in alloys with Ru at. % content of 94%. When the atomic Mo% is < 26%, a dominant Ru phase is obtained and when it is > 62% a Mo phase is formed. Any single phase is obtained when the Mo concentration is between 0% and 50% in Ru-Mo alloy films. Mixed phases are observed under all the conditions.

## 6. SIMS analysis of Ru-Mo Alloys on High-k dielectrics

Secondary Ion Mass Spectrometry (SIMS) shows the difference Ru and RuxMoy diffusion behavior among alloy films/$HfO_2$/interfaces/Si-substrate as sputtered and after high temperature anneal. Figure 4 and Figure 5 show clear step thickness of each element as sputtered. After 900$^o$C anneal, there is no evidence that either Ru or RuxMoy diffuse through $HfO_2$ to Si substrate. However, W tails are observed indicating W diffusion into Ru and RuxMoy layers. These W tails indicate that concentration of W gradually change with RuxMoy layer depth indicating grain boundary diffusion.

## 7. Summary

In this work, various conditions of $Ru_xMo_y$ alloys films deposited via reactive co-sputtering were evaluated as candidate gate electrodes on high-k dielectrics. Electrical properties were evaluated and it show that some $Ru_xMo_y$ films having proper work function for P-MOSFET at 400$^oC$ on $HfO_2$. However, work function was not stable after high temperature annealing. There is no evidence both Ru and $Ru_xMo_y$ diffuse through $HfO_2$ to Si substrate indicating both metal element and metal alloy didn't affect work function on $HfO_2$.

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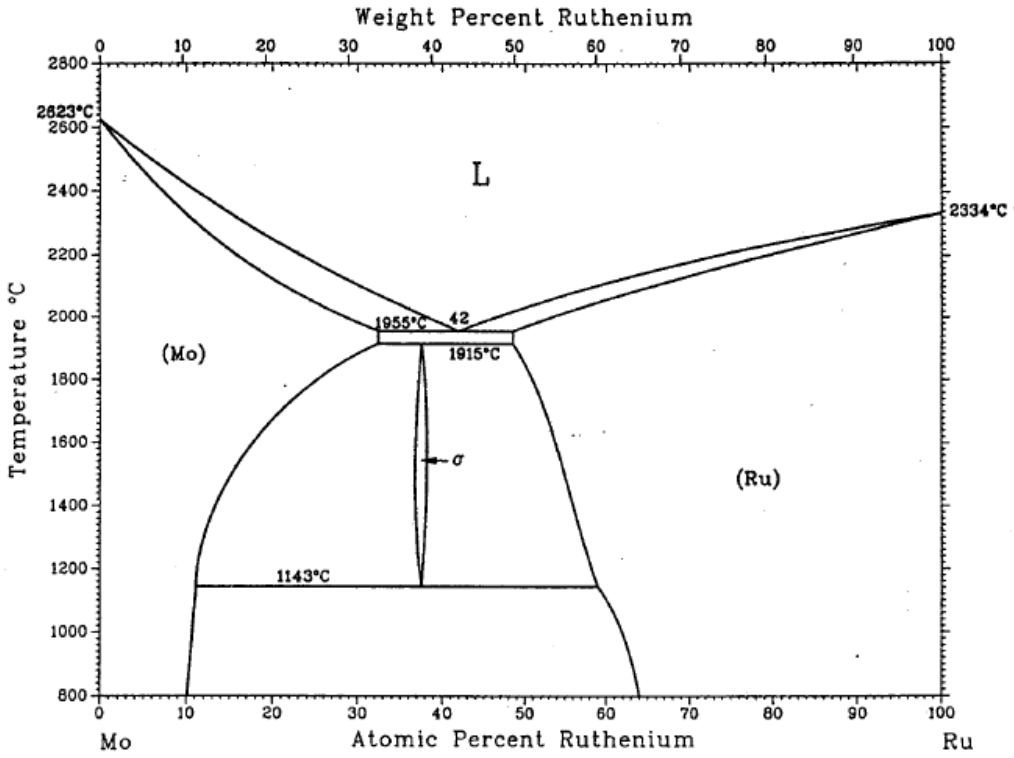



**Figure A. 1 Mo-Ru Phase Diagram**

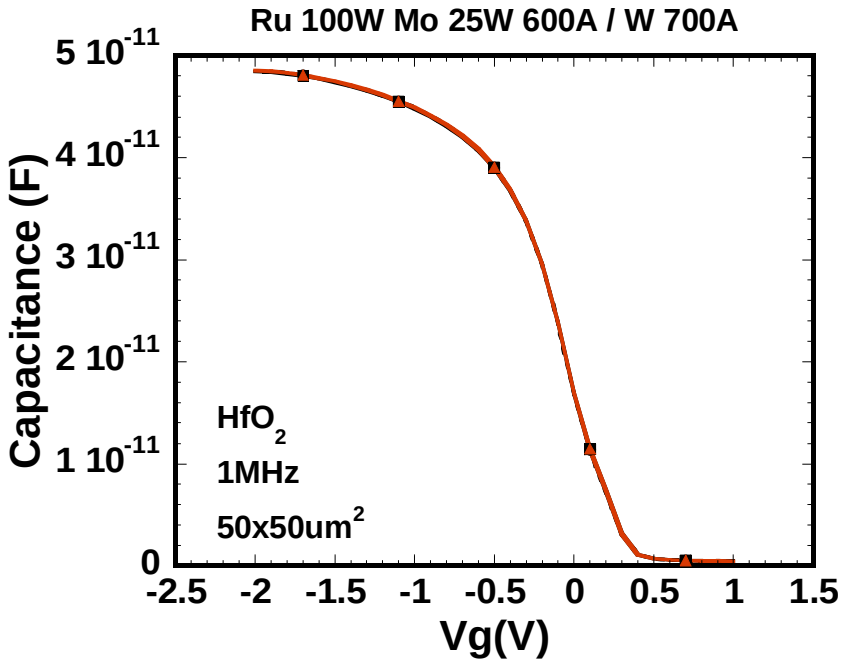



**Figure A. 2 C-V curev of as Ru100W-Mo25W on varying $HfO_2$ after 400°C FGA**

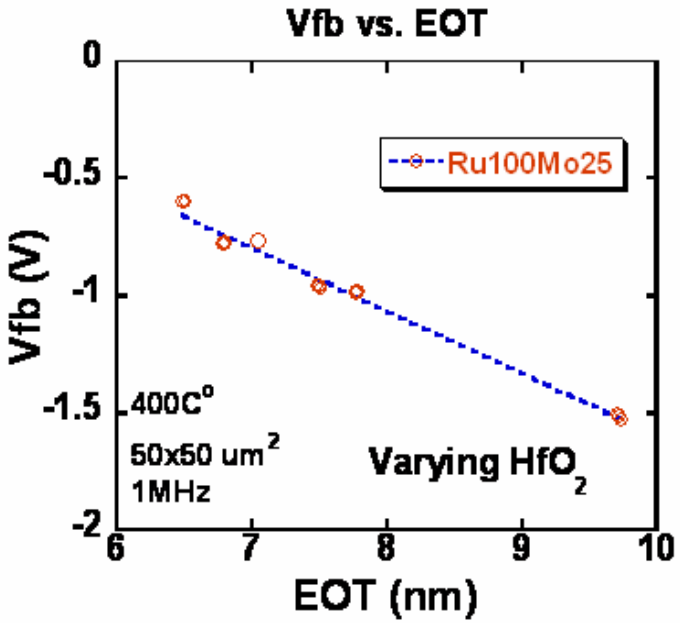



**Figure A. 3 $V_{FB}$ vs. EOT of as Ru100W-Mo25W on varying $SiO_2$ with 40A $HfO_2$ after 400°C FGA**

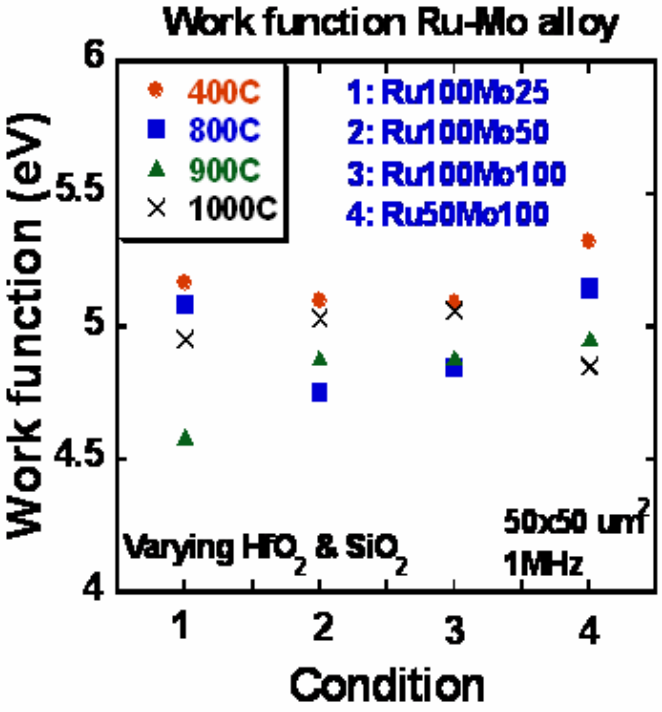



**Figure A. 4 1st exp. Work functions of as Ru-Mo on varying $SiO_2$ and $HfO_2$ after different temperature anneal**

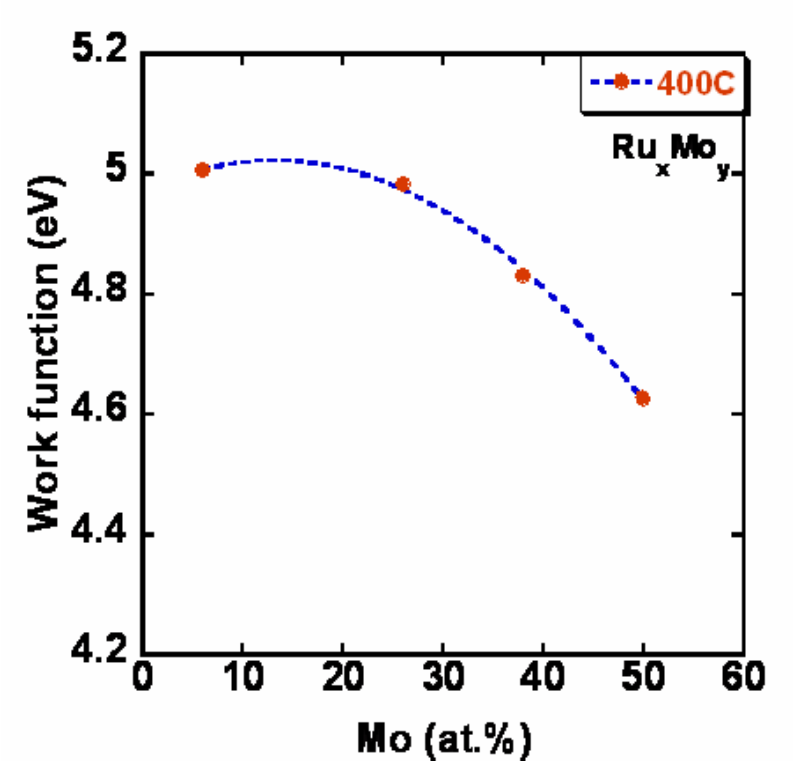



**Figure A. 5 2st exp. Work functions of as Ru-Mo on varying $SiO_2$ and $HfO_2$ after 400°C FGA**

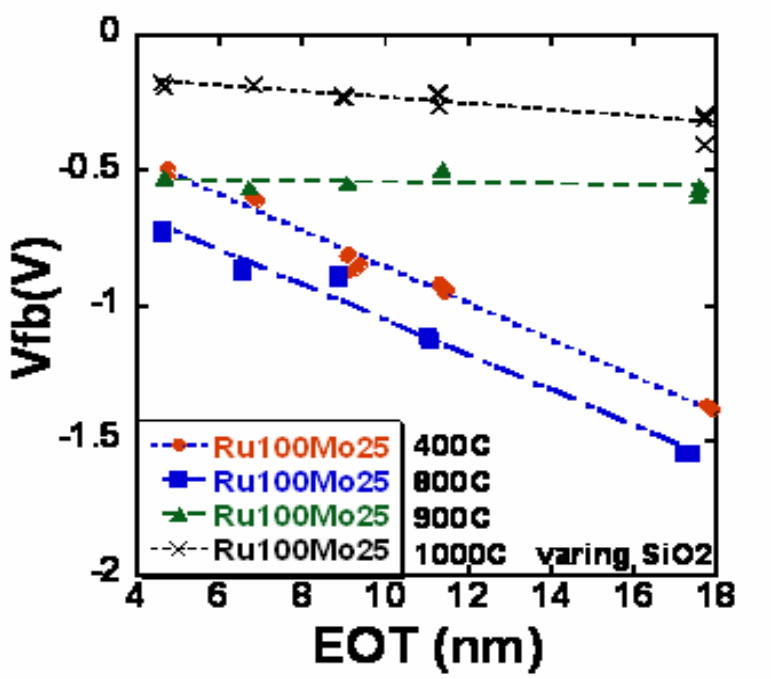



**Figure A. 6 $V_{FB}$ vs. EOT of as Ru-Mo on varying $SiO_2$ with fixed $HfO_2$ after different temperature anneal**

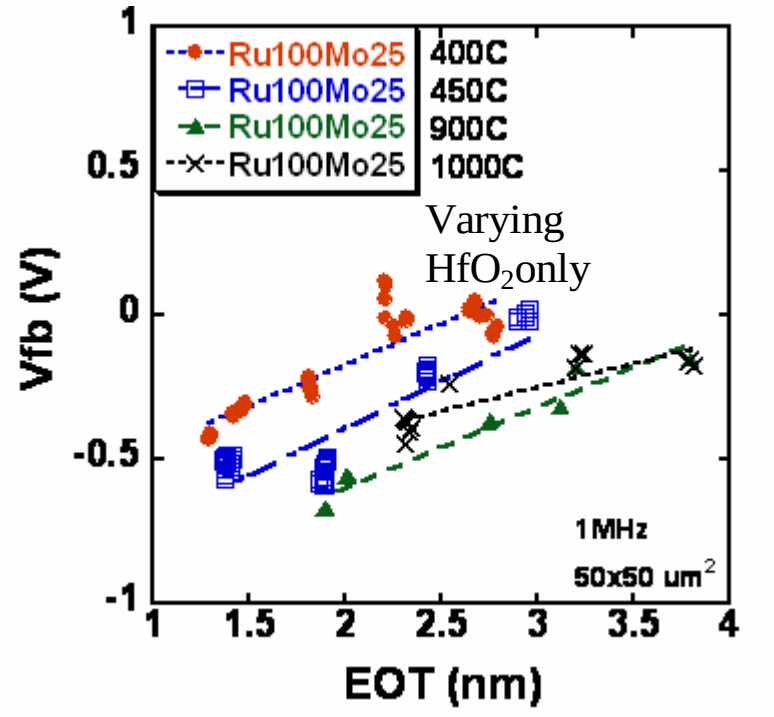



**Figure A. 7 $V_{FB}$ vs. EOT of as Ru-Mo on varying $HfO_2$ after different anneal**

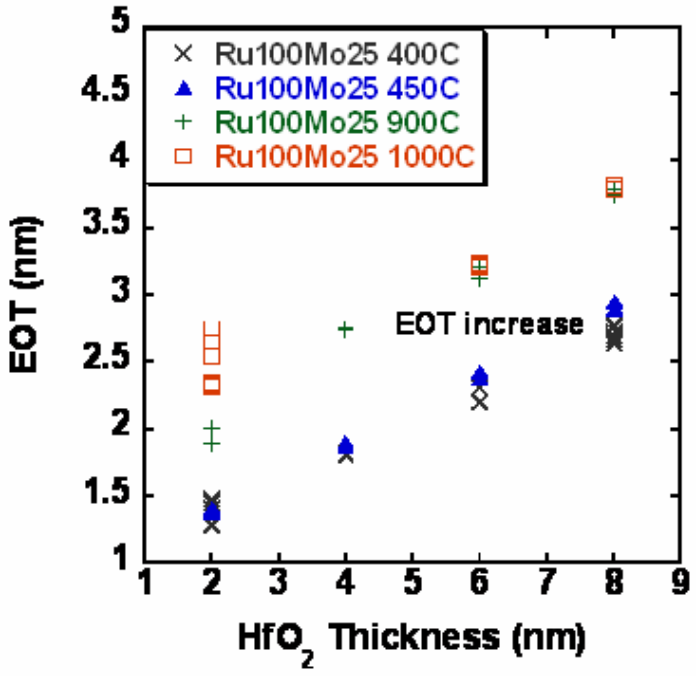



**Figure A. 8 EOT change of as Ru 100W Mo 25W on varying $HfO_2/SiO_2$ after different anneal**

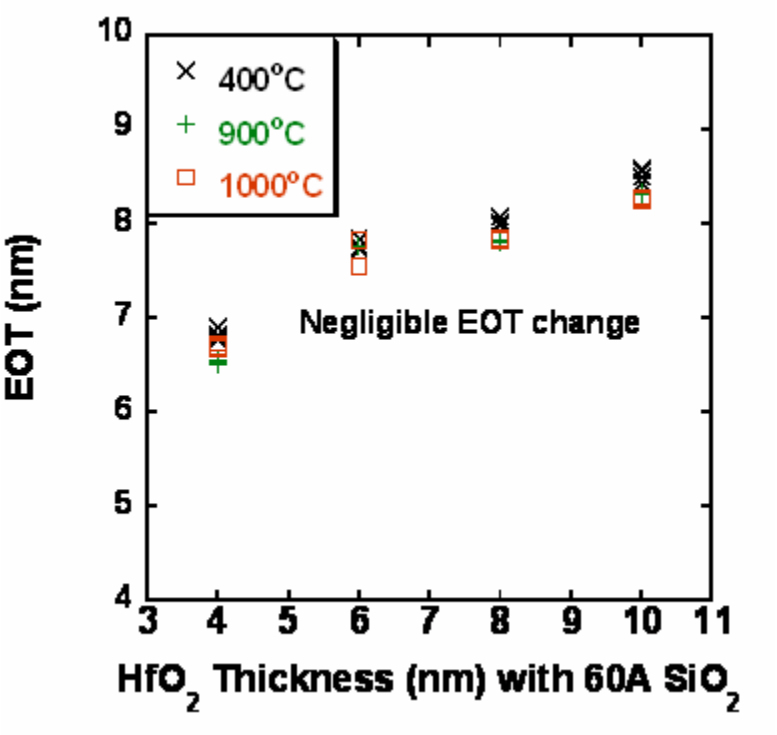



**Figure A. 9 change of as Ru 100W Mo 25W on varying $HfO_2$ after different anneal**

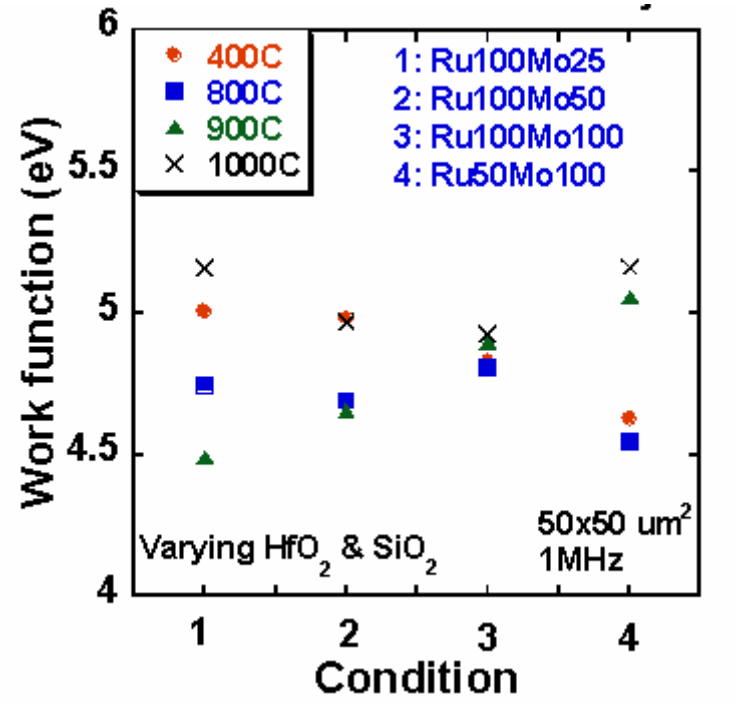



**Figure A. 10 1st exp. Work functions of as Ru-Mo on varying $HfO_2/SiO_2$ after different temperature anneal**

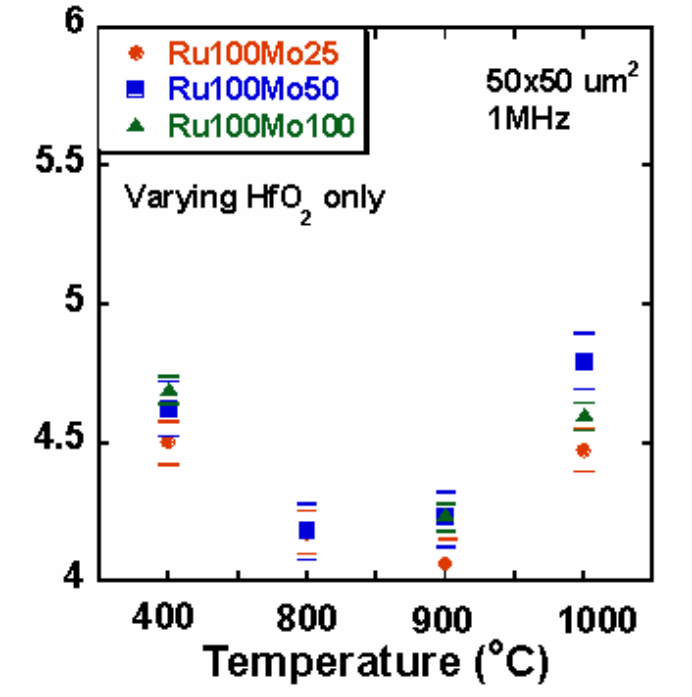



**Figure A. 11 Work functions of as Ru-Mo on varying $HfO_2$ after different temperature anneal**

**Table A. 1 Sputtering condition and composition of as-deposited films from RBS analysis**

| Sputtering Condition | Thickness (Å) from RBS | Composition Bottom layer(RBS) | Thickness (Å) from RBS | Composition Top layer (RBS) |
|---|---|---|---|---|
| Ru 100W Mo 25W 700Å W 600 Å | 325 | Ru 94% Mo 6% | 269 | W 100% |
| Ru 100W Mo 50 W 700Å W 600 Å | 300 | Ru 74% Mo 26% | 258 | W 100% |
| Ru 100W Mo 100W 700Å W 600 Å | 298 | Ru 62% Mo 38% | 254 | W 100% |
| Ru 50W Mo 100W 700Å W 600 Å | 226 | Ru 50% Mo 50% | 222 | W 100% |

**Table A. 2 Compositions of films after 900°C anneal from RBS analysis**

| Sputtering Condition | Thickness (Å) from RBS | Composition Bottom layer(RBS) | Thickness (Å) from RBS | Composition Top layer (RBS) |
|---|---|---|---|---|
| Ru 100W Mo 25W 700Å W 600 Å | 350 | Ru 79% Mo 8% W 13% | 226 | W 93 % Ru 7% |
| Ru 100W Mo 50 W 700Å W 600 Å | 335 | Ru 77% Mo 13% W 10% | 267 | W 93 % Ru 7% |
| Ru 100W Mo 100W 700Å W 600 Å | 290 | Ru 69% Mo 22% W 9% | 267 | W 91 % Ru 9% |
| Ru 50W Mo 100W 700Å W 600 Å | 265 | Ru 50% Mo 40% W 10% | 315 | W 91 % Ru 9% |

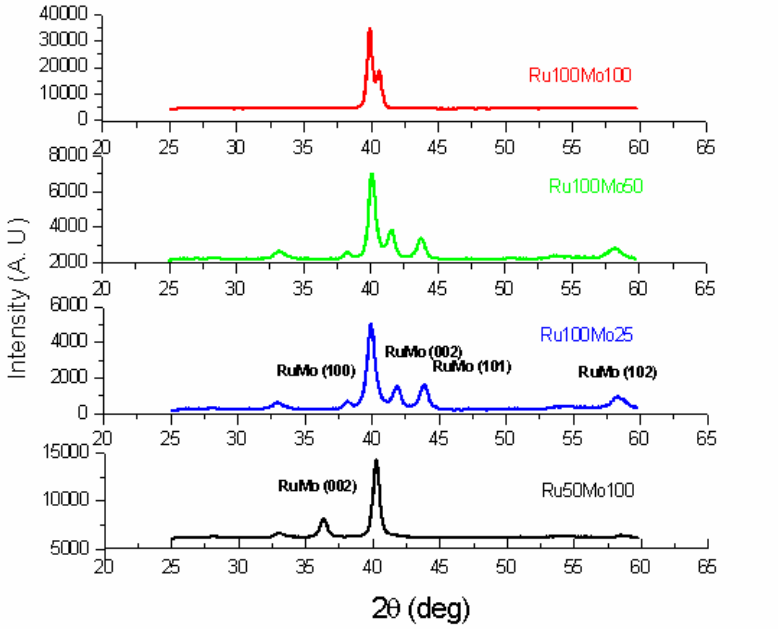



**Figure A. 12 XRD analysis of as Ru-Mo after 400°C FGA**

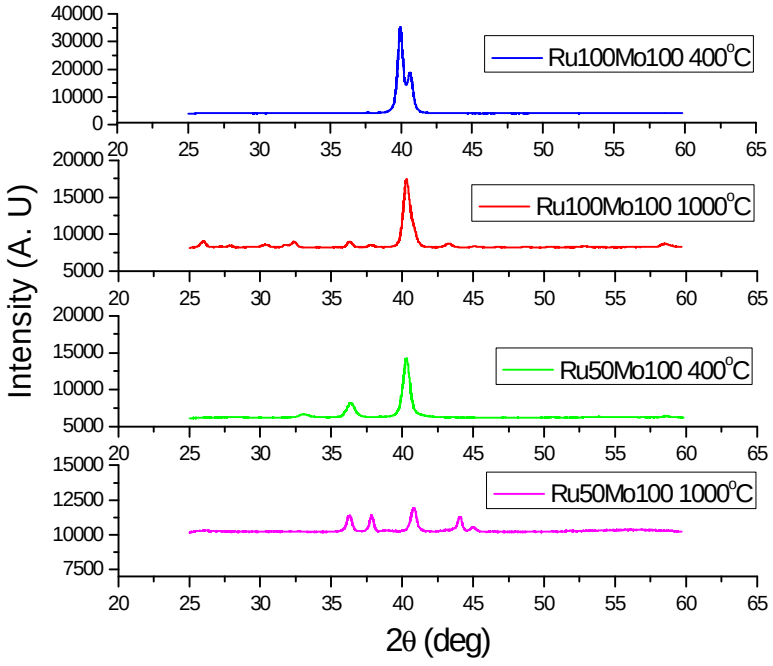
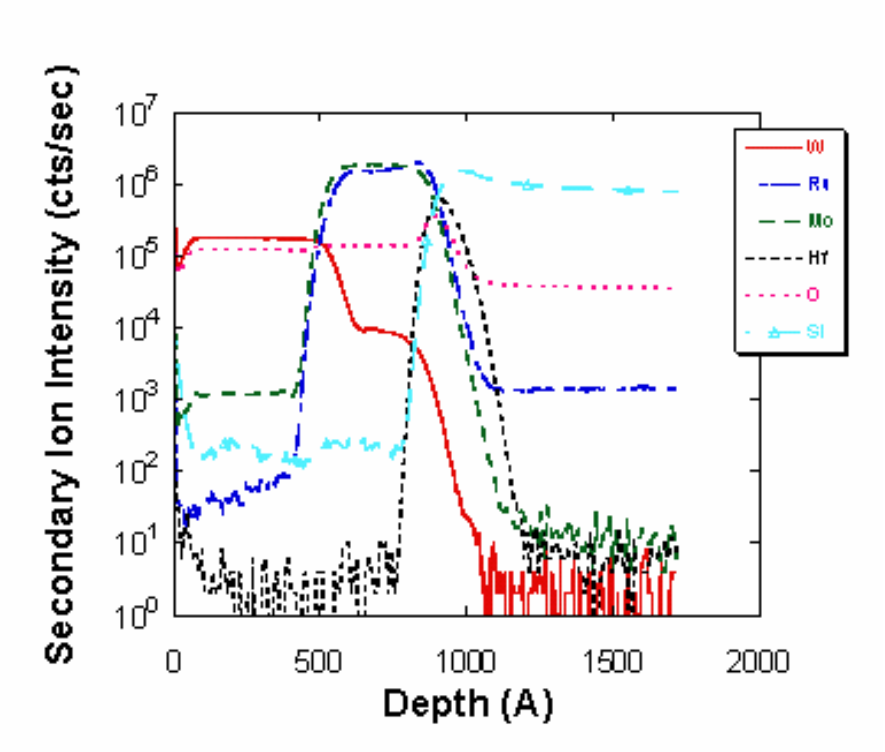
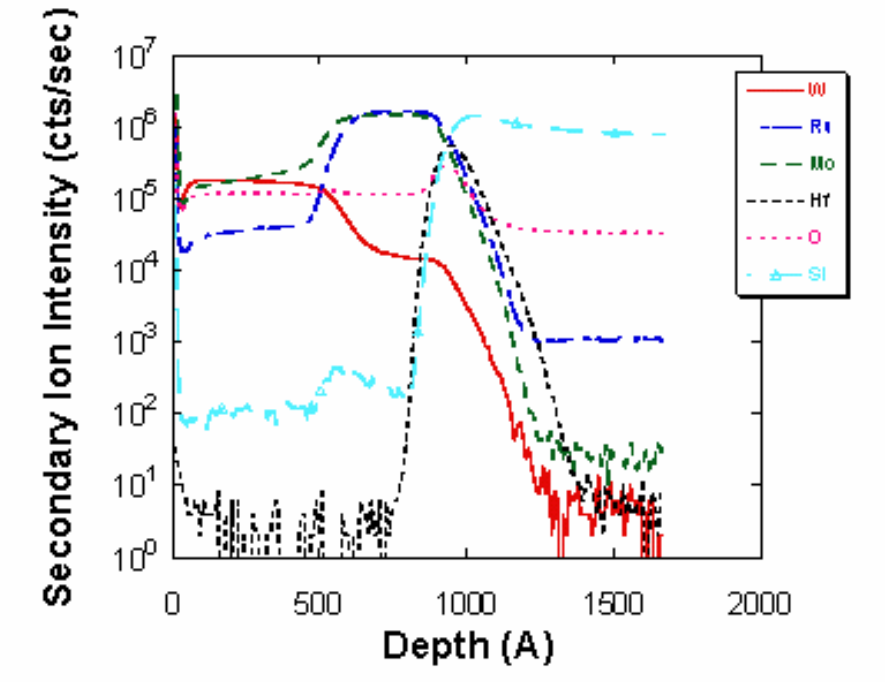



**Figure A. 13 XRD analysis of as Ru-Mo after 1000°C anneal**

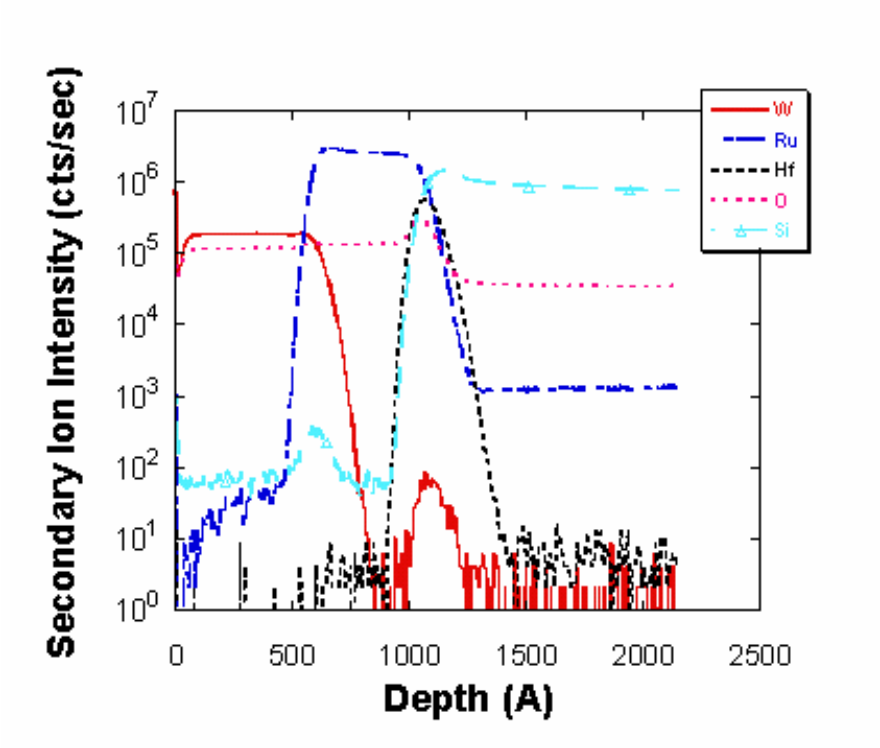



(a)

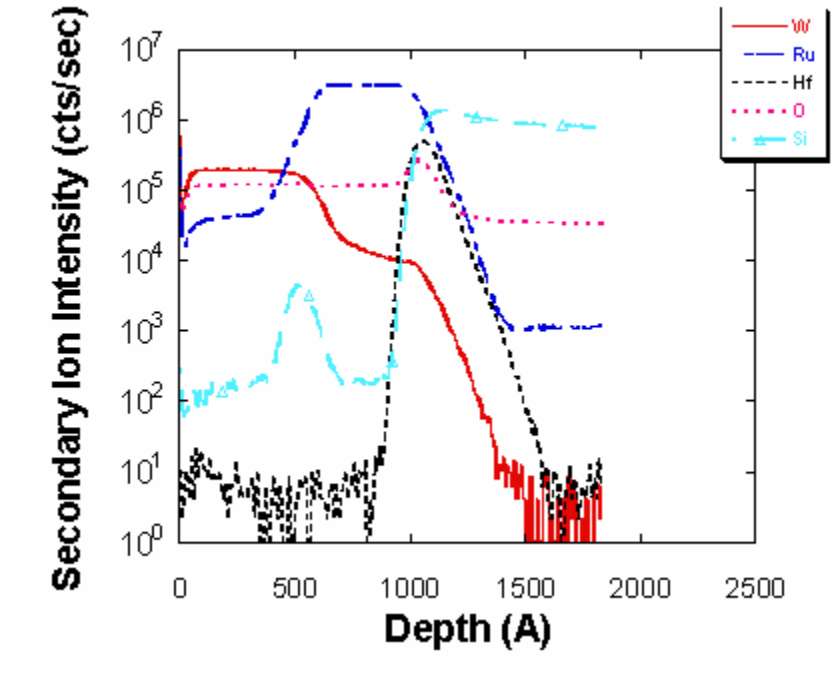



(b)

**Figure A. 14 SIMS analysis of as Ru 100W Mo 100W 700A W 600A (a) as-deposited (b) 1000°C anneal**




(a)




(b)

**Figure A. 15 SIMS analysis of as Ru 100W Mo 100W 700A W 600A (a) as-deposited (b) 1000°C anneal**