

ABSTRACT

YANG, MINGYU. Process Development of an Ultra High Density Chip-on-Chip Power Module. (Under the direction of Dr. Douglas C Hopkins).

This research developed a fabrication process for novel 3D chip-on-chip power modules for the NCSU-PREES laboratory. Past and present 3D power module packaging technologies have been reviewed, and flex-circuit-based chip-on-chip approach has been selected to demonstrate fabrication processes to produce very high power density modules. Based on this concept, the flex circuit and testing circuit topologies have been designed with the assist of electrical and thermal simulations. Because flex materials have low modulus, mechanical stress analysis was not pursued for this particular research. An extra need of the module is double-sided solderable power devices since the devices will be sandwiched between different flex circuit layers in the module to realize electrical and thermal connections. This required a surface metallization process to be developed at the NCSU-NNF facility to convert Al die pads to solderable Ag or Cu. A Ti/Ni/Cu metallization solution has been chosen to deposit on Al pads of the devices. Lastly, the flex circuits and test circuits have been assembled and tested to show fabrication process success.

Although the flex module has not been electrically tested due to the failure of the surface metallization process, the entire fabrication process for the NCSU-PREES Laboratory has been presented in this thesis and can be repeated once solderable devices are available. Some potential improvements are suggested at the end of the thesis.

© Copyright 2014 by Mingyu Yang

All Rights Reserved

Process Development for Ultra High Density Chip-on-Chip Power Modules

by
Mingyu Yang

A thesis submitted to the Graduate Faculty of
North Carolina State University
in partial fulfillment of the
requirements for the degree of
Master of Science

Electrical Engineering

Raleigh, North Carolina

2015

APPROVED BY:

Dr. Douglas C Hopkins
Committee Chair

Dr. Subhashish Bhattacharya

Dr. Wensong Yu

DEDICATION

This thesis is dedicated to my parents.

For their endless love, support and encouragement

BIOGRAPHY

Mingyu Yang was born in Harbin, Heilongjiang Province in People's Republic of China. He received his Bachelor of Science degree in Electrical Engineering from Huazhong University of Science and Technology, Wuhan, China. He is a graduate of North Carolina State University under the guidance of Dr. Douglas C Hopkins. His research interests are in power electronics and power module design and fabrication.

ACKNOWLEDGMENTS

First, I would like to gratefully and sincerely thank my advisor, Dr. Douglas C Hopkins, for his kindly instruction and help in this research. This work could not have been finished without his guidance, support and time.

I would also like to thank Dr. Subhashish Bhattacharya and Dr. Wensong Yu to be my committee member. Their suggestions and help in my study are greatly appreciated.

The colleagues at PREEs lab and FREEDM center also give me a lot of help during the entire research. I would like to thank Yang Xu, Haotao Ke, Adam Morgan, Sean Ketring, Liqi Zhang, Xin Zhao, Xiao Zhang, Yang Lei, Junning Jiang, Yifan Jiang, Juncheng Zhou, Xinyu Zhang, Youxi Shao, Qinmiao Li, Shangmin Lin, Hongyu Wu, Dr. Xijun Ni, Anjie Jiang, Qian Wu, Jingwen Xiong, Lisha Sun, Yue Shi for their help, discussions and friendships.

I would also like to acknowledge the laboratory support from Hesse Mechatronics and Sikama companies for donating equipment that made this research work more professional, much easier and quickly possible, and from CREE for bare die and Fairchild.

Finally, I would like to give my deepest thanks to my parents for giving me the opportunity as well as educating me how to live, to love, to learn and to grow. All the support they have

provided me over the years was the greatest gift anyone has ever given me. They are the source of my power and strength, as well as my future family.

TABLE OF CONTENTS

LIST OF TABLES.....	viii
LIST OF FIGURES	ix
CHAPTER 1 INTRODUCTION.....	1
1.1 Background	1
1.2 Overview of Stacked Chip Power Module.....	5
1.3 Problem Statement and Objective	9
1.4 Methodology	11
1.5 Thesis Outline	13
CHAPTER 2 TOPOLOGY AND DEVICE CHARACTERISTICS.....	14
2.1 Bare Chip Characteristics.....	14
2.2 Circuit Topology and Design.....	18
2.3 Flex Circuit Development	20
2.3.1 Layout Challenges	20
2.4 Test Circuit Development	26
2.5 Simulation Results.....	27
2.5.1 Electrical simulation	27
2.5.2 Thermal simulation	34
CHAPTER 3 MODULE MATERIALS AND FABRICATION PROCESS	41
3.1 MOSFET and Diode.....	41
3.1.1 Metallization Preparation.....	41
3.1.2 Metallization process	42
3.1.3 Pull test and results	49
3.2 Flex circuit.....	50
CHAPTER 4 ASSEMBLY, TESTING AND RESULTS.....	51
4.1 Power Module Assembly	51
4.2 Electrical Characterization	60
CHAPTER 5 SUMMARY AND FUTURE WORKS.....	63
REFERENCES	65
APPENDICES	68
Appendix A CPM2-1200-0025B SiC MOSFET Datasheet.....	69

Appendix B CPW5-1200-Z050B SiC Diode Datasheet 72
Appendix C FAN3122C Gate Driver Datasheet..... 81

LIST OF TABLES

Table 2-1 Power device electrical specifications	15
Table 2-2 FAN3122C specifications	17
Table 2-3 Circuit specifications	18
Table 2-4 Passive components.....	19
Table 2-5 Thermal characteristics.....	37
Table 3-1 Deposition process and thickness obtained	47
Table 4-1 Two types of solder with different melting temperature	51

LIST OF FIGURES

Figure 1-1 Typical power multi-chip module	2
Figure 1-2 Double-sided flexible PCB	4
Figure 1-3 IPEM using flex circuit	6
Figure 1-4 Flex-circuit based power module	7
Figure 1-5 Comparison of standard connection technology (solder/bonding) and SKiN technology	8
Figure 1-6 TI PowerStack technology	9
Figure 1-7 Cross sectional view of flex module	10
Figure 1-8 Fabrication flow chart	12
Figure 2-1 Power devices dimension	15
Figure 2-2 FAN3122C die attachment diagram	17
Figure 2-3 Reverse buck converter	18
Figure 2-4 Double layer double access part.....	21
Figure 2-5 Single layer double access part	21
Figure 2-6 Incorrect gate driver footprint for wire bonding and not flip-chip.....	22
Figure 2-7 Gerber files and fabricated circuits	23
Figure 2-8 PCB design file in Altium Designer.....	26
Figure 2-9 PCB circuit	27
Figure 2-10 Critical loop in buck power stage.....	28
Figure 2-11 Gate drive turn-on and turn-off current path	29
Figure 2-12 Reverse buck topology	31
Figure 2-13 Output voltage waveform.....	32
Figure 2-14 Steady state inductor current.....	33
Figure 2-15 Module top view	39
Figure 2-16 Module bottom view	40
Figure 3-1 Single-layer double-access flex	50
Figure 3-2 E-beam evaporator	43
Figure 3-3 Ti deposition sample	44
Figure 3-4 Raw data obtained from Nanometrics.....	45
Figure 3-5 Mechanical chips on metal plate	46
Figure 3-6 Samples after process	48
Figure 3-7 MOSFET samples under microscope.....	48
Figure 3-8 Pull test set up	49
Figure 4-1 Size comparison of flex circuit parts and one cent coin.....	52
Figure 4-2 Sikama conduction belt reflow oven.....	53
Figure 4-3 Reflow temperature profile	54
Figure 4-4 Semi-finished module after Step 1	54
Figure 4-5 Solder paste on pads.....	55
Figure 4-6 Part A with components	56
Figure 4-7 lower temperature reflow profile	55

Figure 4-8 Semi-finished module after Step 2.....	56
Figure 4-9 Bottom sides of Part A and B.....	57
Figure 4-10 Part B assembly status.....	57
Figure 4-11 Solder paste on pads.....	58
Figure 4-12 Flex module before reflow process.....	59
Figure 4-13 Finished flex module.....	59
Figure 4-14 Finished system assembly.....	60
Figure 4-15 Test bench set up.....	61
Figure 4-16 Vgs&Vds switching waveforms.....	62

CHAPTER 1 INTRODUCTION

This chapter gives a basic background of power electronic module design. A section of literature review is included to show state-of-the-art packaging technologies. The motivation and methodology of this research will also be addressed.

1.1 Background

Power electronic modules are widely used in power electronic systems, such as switching power supplies, motor drives and electric vehicles. The packaging of power electronics is a critical factor to performance and reliability of power electronics systems [1]. The current R&D focus on power electronic packaging is on cost reduction, increase of power density, increase of reliability and reduction of effects due to parasitic elements. These parasitics are undesirable capacitance between circuit parts and inductance in circuit traces. They both can have a negative effect, such as increases in electromagnetic radiation and switching loss. Therefore, designers and manufacturers try to minimize the parasitic elements of the modules. Another concern for power modules is thermal management since power modules are basically used for high current and high voltage applications. Massive heat will be generated during the switching process. The heat has to pass through different layers such as solder, baseplate, thermal interface material and heat sink [2]. Since modern silicon carbide power semiconductors become more and more popular in various applications, the power density of power modules becomes higher, which requires more efficient and effective heat transfer design.

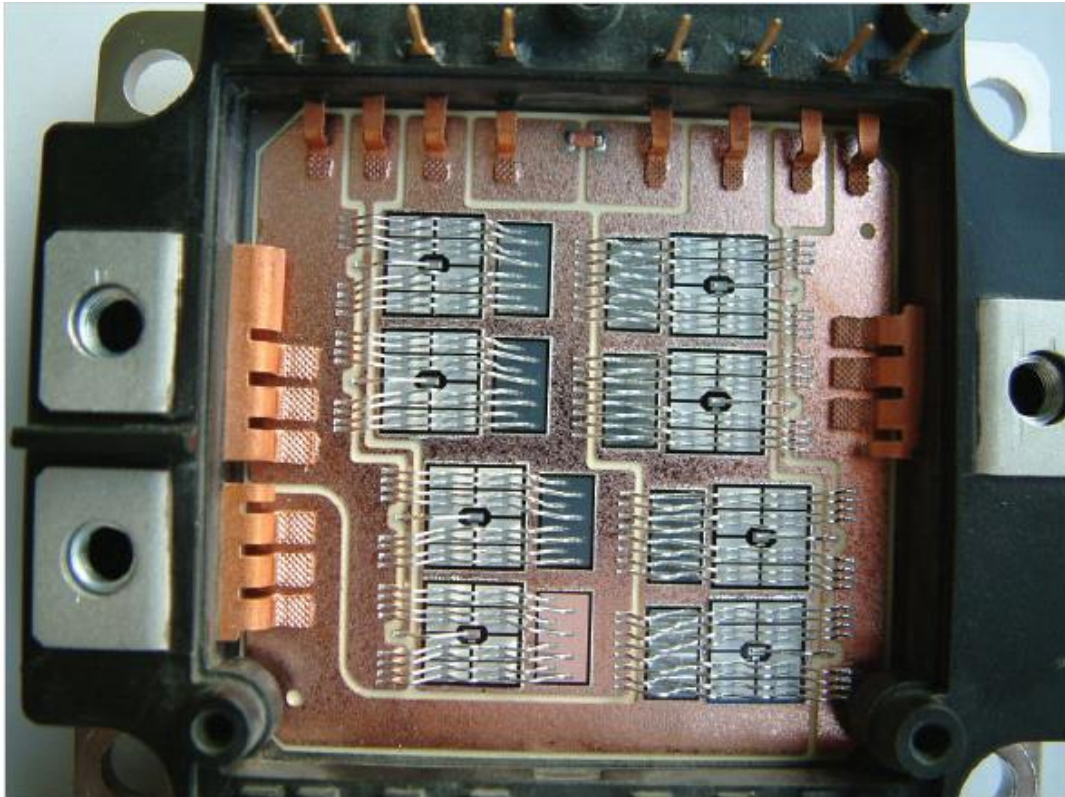


Figure 1-1 Typical power multi-chip module [3]

Figure 1-1 is a typical power multi-chip semiconductor module. It has six power devices paralleled with power diodes respectively, which constitute a 3-phase full bridge converter circuit. In this conventional power module, wire-bonding technology is adopted to provide electrical interconnection. Currently, wire bonding is generally considered the most cost effective and flexible interconnect technology, and is used to assemble the majority of semiconductor packages. However, wire-bonding has some inherent disadvantages. For example, wires used to connect devices can induce stray inductance, and power devices can be only planar. As the demand of power rating and switching speed of power electronics

devices increase, the di/dt is getting faster [4]. Therefore, the stray inductance inside the module plays an ever more important role in high current and high frequency operation.

The objective of this work is to develop a packaging fabrication method suitable for chip-stack technology and apply flexible PCB circuit technology for interconnection to reduce the stray inductance to realize high power density. The 3D chip-stack advantages are:

- Smaller Footprint: more functionality fits into a smaller space
- Shorter interconnect: the average interconnect length is reduced and thus stray inductance is reduced as a result
- Higher power: flexible circuit connection leads to higher power capability by choosing heavy Cu layer up to 5 ounce (175 μ m/6.9mil) thick

Flexible printed circuit, also known as flex circuit or flexible PCB, is a technology for assembling electronic circuits by mounting electronic devices on flexible polymer substrates, such as polyimide [5]. Flexible circuits can be manufactured using identical components of small size as used in rigid printed circuit boards, but allowing the circuit to flex during use.

This is the major reason why fabrication of flex circuitry was chosen for the thesis work.

Flex circuits also have other benefits compared to traditional rigid boards, e.g.

- Higher circuit density
- More robust operating temperature range
- Stronger signal quality

- Improved reliability and impedance control
- Size and weight reduction
- Elimination of mechanical connectors, such as lead frame in traditional modules

The objective of this thesis is to develop and demonstrate in the NCSU-PREES laboratory the fabrication processes to create stacked power electronic circuits, which can realize the above advantages.

There are a few approaches to flex circuit construction. The most common from simple to complex may include single-layer single-access flex circuits, single-layer double-access flex, double-sided flex, multilayer flex and rigid-flex circuits. Double-sided flex will be used in the thesis, and the design and fabrication details will be covered in Chapter 2. As an example, Figure 1-2 shows the cross sectional view of a double-sided flexible circuit.

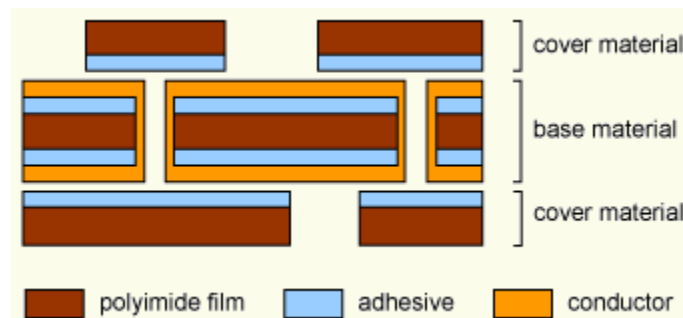


Figure 1-2 Double-sided flexible PCB [6]

1.2 Overview of Stacked Chip Power Module

Flip-Chip technology was firstly introduced in the IC industry as a low cost, high density and reliable chip attachment approach. [7] Bonding wires are eliminated in this method. Instead, solder joints are utilized for interconnection and provide more current capability with lower parasitic inductance and capacitance. In addition, the flip-chip package also becomes smaller since it does not need a lead frame. This section, we will go through some of the existing research and state-of-the-art technologies of flip-chip and flex circuit technology.

In the paper '*Power Electronics Modules for Inverter Applications using Flip-Chip on Flex-Circuit Technology*', researchers from Rensselaer Polytechnic Institute and University of Wisconsin developed an integrated power electronics module (IPEM) for motor drive application. Figure 1-3 is the cross sectional schematic of the power module which is based on half bridge circuitry. The direct bond copper (DBC) substrate that provides the power device drain interconnections. The underside of flex circuit provides the gate and source interconnections. Gate driver circuitry is placed at the top side of the flex substrate.

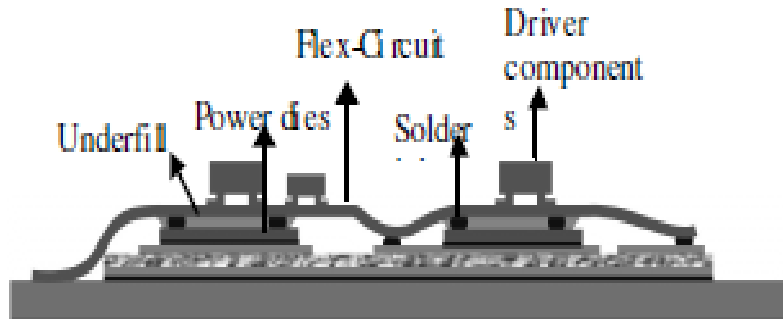


Figure 1-3 IPEM using flex circuit [8]

In the paper ‘*Flip-Chip on Flex Integrated Power Electronics Modules for High-Density Power Integration*’, researchers from Virginia Tech presented a high-density power module using flip-chip on flex (FCOF) technology as shown in Figure 1-4. The flex circuit is etched on both sides and one side of the flex provides interconnection to power devices while the other is used to construct a simple gate drive circuit. Via holes through the flex integrate the power stage and gate driver together. The MOSFET and Schottky diode used in this study were acquired from IXYS and have been processed by sputtering metallization.

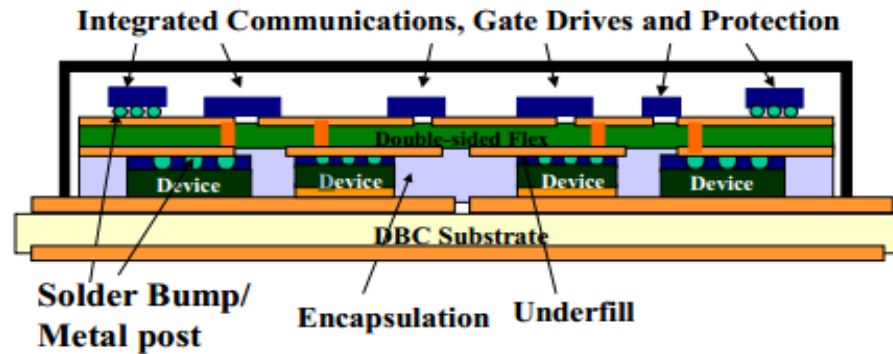
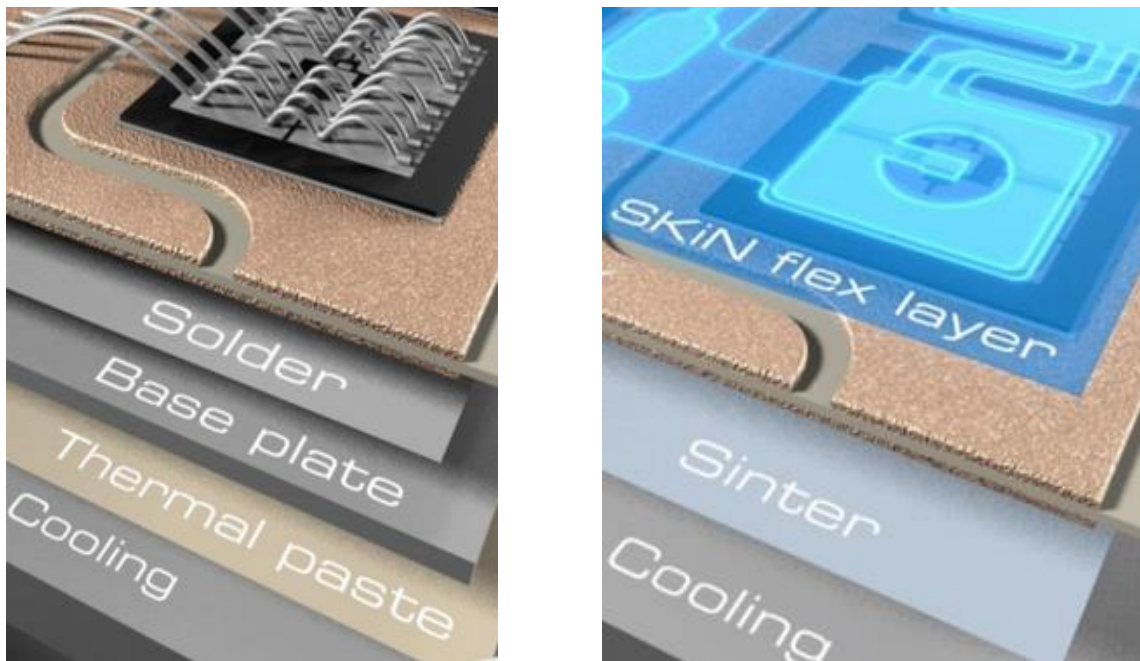


Figure 1-4 Flex-circuit based power module [9]

On the industrial side, Semikron has developed a technology which they named SKiN Technology, using multiple flex layers made up of flex foil. Figure 1-5 shows the difference between standard power module package and SKiN Technology. As can be seen, the traditional wire bonding is substituted by flex layers, and also all soldering and bond connections are replaced by sintered compositions. According to Semikron's experimental data, advantages lie in the aspects below:

- Thermal resistance between semiconductor and coolant is decreased by 30%
- Bond wires can only make contact to about 21% of the total metallized chip surface, while sintered flex foil exhibits a die contact area of up to 85%. This leads to a 60% reduction of inner commutation inductance.
- Without wire bonding and lead frame, power density is increased by 50% in this 3D packaging solution.



a) Standard Technology

b) SKiN Technology

Figure 1-5 Comparison of standard connection technology (solder/bonding) and SKiN technology [10]

Texas Instrument's PowerStack technology also provides another solution for 3D chip-on-chip packaging. With this packaging technology, high side and low side MOSFET dies are stacked in a single package as shown in Figure 1-6. Source of high side MOSFET faces down and is interconnected with low-side MOSFET drain through a low resistance copper clip. Another clip connects to the high side drain. Low side die sits on the lead frame, which has an exposed pad on the bottom of the package at ground potential.

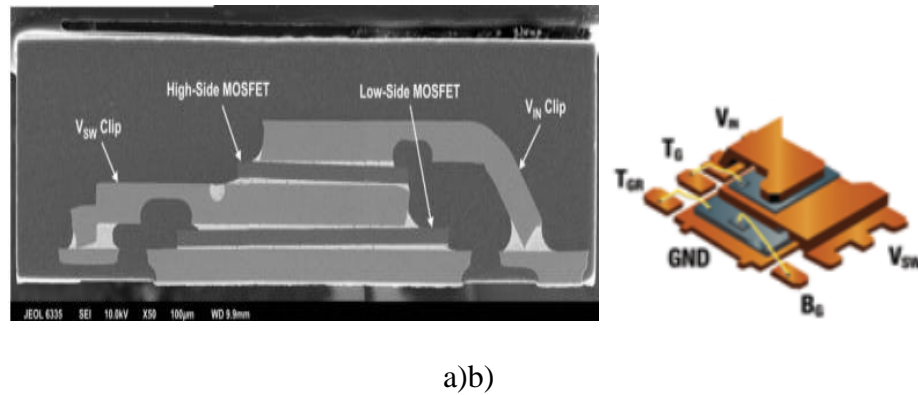


Figure 1-6 TI's PowerStack technology [11]

1.3 Problem Statement and Objective

This research develops a procedure in the NCSU Laboratory for Packaging Research in Electronic Energy Systems (PREES) for fabricating stacked components, such as a MOSFET, diode and gate driver, to create a single module. A demonstration module is constructed with flex-circuit technology with focus on process development and documenting the process. The module is constructed as a planar geometry with extended planar interconnection onto the next package level, e.g. a printed circuit board (PCB). The planar connections provide very high frequency performance. Silicon carbide devices are used to realize high voltage and high frequency characteristics, i.e. 1200V SiC MOSFET and Schottky diode bare dies are acquired from CREE. The cross section of the demonstration module sitting inside a well that is drilled into the PCB is shown in Figure 1-7. The diode sits on the very bottom of the module with anode face up, and cathode connected to a heat sink through thermal paste. Anode of the diode is then connected to the MOSFET drain by a

double-sided flex circuit, i.e. the MOSFET and diode are both soldered to same piece of flex circuit. Extensions to this flex circuit also plays the role of interconnect to realize the connection between power module and outer PCB circuitry. Similarly, the MOSFET source (top-side) is soldered to another flex circuit which hosts the gate drive control circuitry. Hence, the MOSFET and diode are sandwiched by two pieces of flex circuit as shown Figure 1-7. Finally, the module is tested in a buck topology. Electrical connection is covered in Chapter 2.

In order to solder bare die, i.e. MOSFET and diode, onto flex circuit, additional surface metallization processes are necessary for the devices. After the semiconductor device becomes solderable, the device is soldered by a reflow process. During the reflow processes, different melting temperature solders should be applied to the joints between devices and circuits so that multiple reflows become feasible.

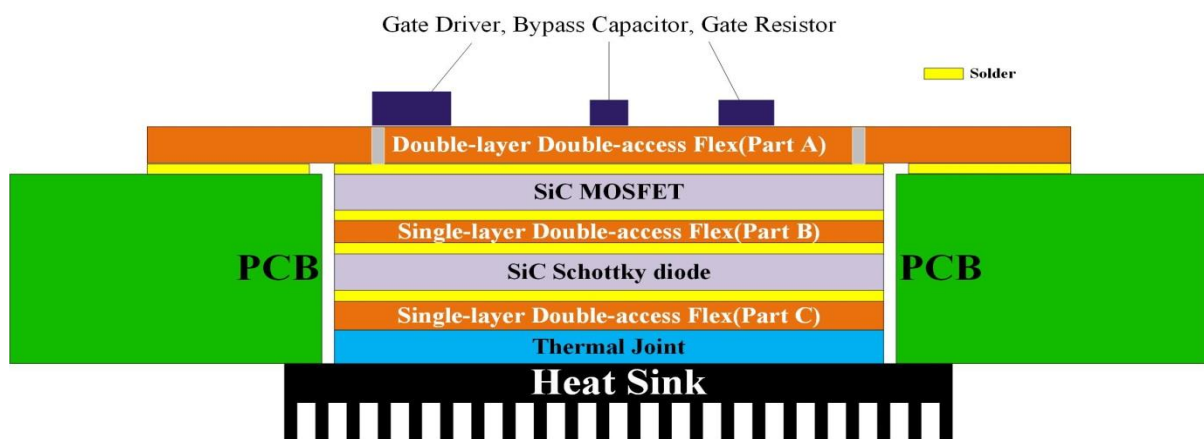


Figure 1-7 Cross sectional view of flex module

1.4 Methodology

From electrical design point of view, power modules are normally quite simple to be designed [12]. However, a lot of issues are associated with thermal management, material selection and reliability of the 3D structure because the power modules are always pursuing higher voltage, current, frequency as well as higher level integration capabilities. This thesis work is comprised of four major steps which are literature review and idea proposal, establishing design guidelines for chip-stack power module, electrical and thermal simulation, and power module physical testing.

Literature reviews have been done for several packaging technologies, such as flip-chip, 3D (stacked chip) packaging, direct work in stacked power chips, and reports on publications relevant to designing a chip-stack power module.

The designed chip-stack power module aims at 1600W with 400V input voltage and 4A input current. Thermal management is a crucial part of the design. Therefore, electrical and thermal simulation plays an important role in designing the system topology.

The topology uses a stacked silicon-carbide MOSFET, diode, and gate driver chip. Silicon carbide MOSFET and diode will be pre-processed to change the surface metallization for soldering onto a flexible printed circuit. It is followed by multiple reflow steps to assemble the power module and test circuit. The power module will be physically assembled and tested

in a typical buck converter circuit. Electrical characteristics, such as gate signal, conductive current, drain to source voltage and turn-on and turn-off transient waveforms can be monitored. For the construction of this 3D power module, a fabrication flow chart is shown in Figure 1-8.

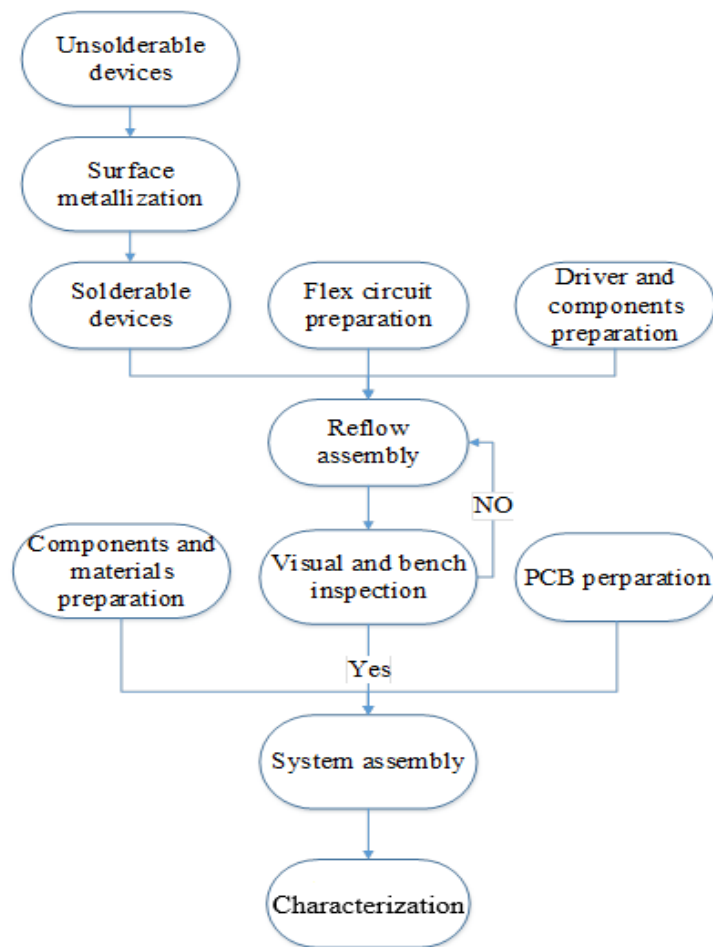


Figure 1-8 Fabrication flow chart

1.5 Thesis Outline

This thesis consists of the following chapters:

Chapter 1 introduces the stacked chip power module, states thesis topic and problem and reviews relevant literatures.

Chapter 2 proposes a chip-on-chip MOSFET power module topology for a stacked MOSFET, diode and gate driver chips. This chapter also introduces the characteristics of the bare die MOSFET, diode and Fairchild's gate drive chip. Simulation results are provided to show module's performance.

Chapter 3 introduces the material and gives detailed procedures for fabricating a module. Process procedures and results are also given for providing a solderable interface in place of aluminium pads on the chips.

Chapter 4 provides the test board assembly and test results.

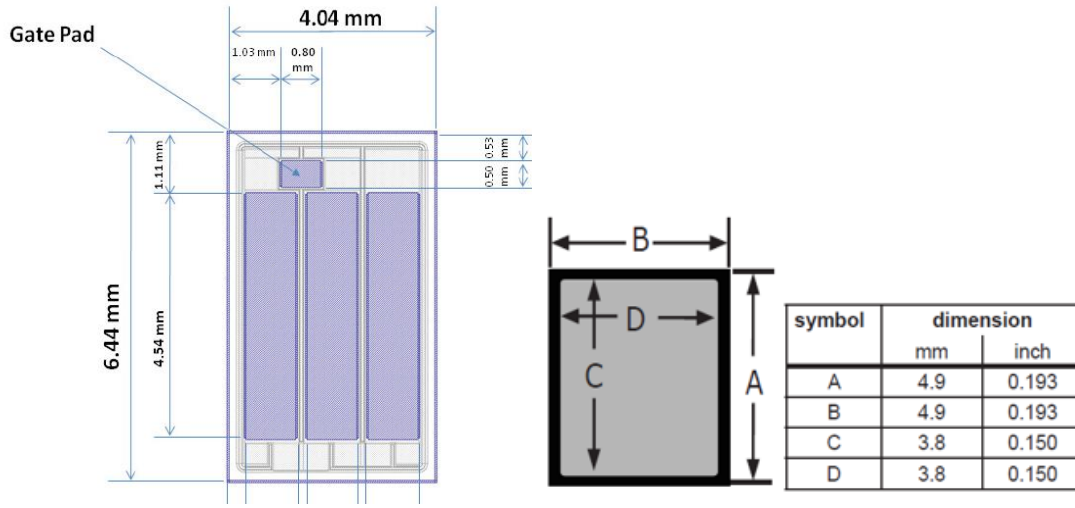
Chapter 5 is summary of the thesis and future work for completing this research topic.

CHAPTER 2 TOPOLOGY AND DEVICE CHARACTERISTICS

This chapter introduces the characteristics of the power devices and the gate drive chip. Electrical circuit design is shown as two parts, flex circuit module and PCB test circuit motherboard. Electrical and thermal simulation is developed in Simplis®SIMetrix and Comsol to assist the system design.

2.1 Bare Chip Characteristics

The power devices used in this research are acquired from CREE, with part number CPM2-1200-0025B and CPW5-1200-Z050B. The CPM2-1200-0025B is an N-channel enhancement mode silicon carbide power MOSFET. The CPW5-1200-Z050B is silicon carbide Schottky diode. Both are bare die devices. The MOSFET has aluminum pads on its source and gate. The diode has aluminum pad on anode. Drain of MOSFET and cathode of diode are metallized with Ni/Ag. Physical dimensions and layout of chips can be seen in Figure 2-1. Some of the major electrical parameters which are useful throughout the thesis are shown in the Table 2-1. Others can be found in the datasheets for the devices in Appendix A.



a) MOSFET chip dimensions

b) Diode chip dimensions

Figure 2-1 Power devices dimension [13] [14]

Table 2-1 Power device electrical specifications [13] [14]

Component	Specifications
MOSFET: CPM2-1200-0025B	Drain source breakdown voltage: 1200V Continuous drain current: 50A@120°C Gate threshold voltage: 2.3V Gate-source voltage: -10/+25V gfs: 22S Qg: 179nC Ciss: 2980pF

Table 2-1 (continued)

	Coss:220pF
Diode: CPW5-1200- Z050B	Breakdown voltage: 1200V Maximum DC current: 50A DC forward voltage: 1.6V@50A,25 ⁰ C

Bare gate drive chips are acquired from Fairchild Semiconductor with part number FAN3122C which is a single low-side gate driver. Figure 2-2 is die attachment diagram. Actual die size is 67.72x51.17 mils (1720.00x1310.00um). Table 2-2 gives some major electrical parameters of the gate driver. Other detailed specifications can be found in Appendix C.

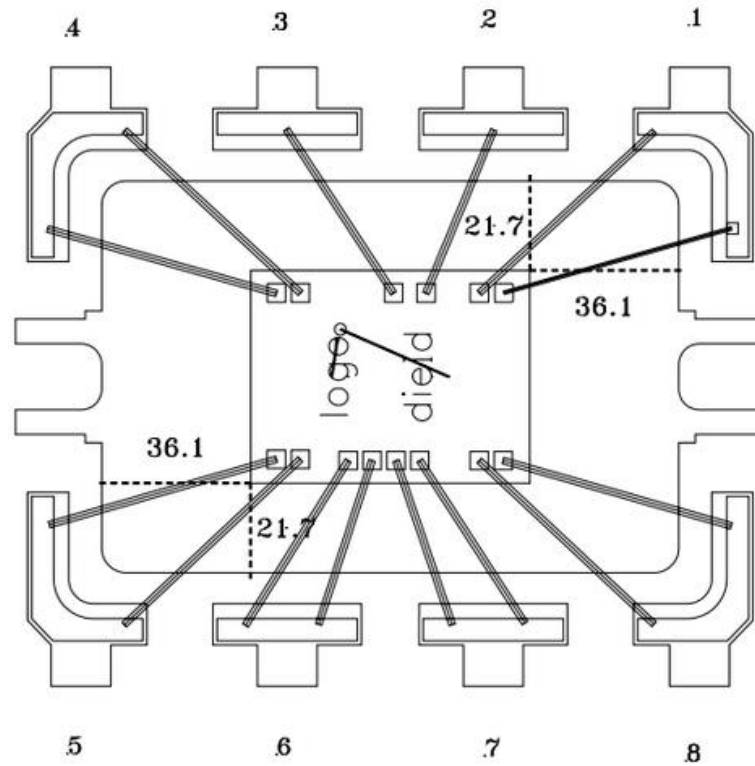


Figure 2-2 FAN3122C die attachment diagram [15]

Table 2-2 FAN3122C specifications [16]

Parameter	Value
Supply voltage range VDD	4.5-18V
Input logic high threshold	55% \times VDD
Peak sinking current	11.4A
Peak sourcing current	10.6A

2.2 Circuit Topology and Design

The power module is designed for placement into a buck converter topology. Figure 2-3 shows a traditional buck schematic with the power MOSFET and inductor on the low side.

Gate driver shares the same ground as the power circuit which makes control easier.

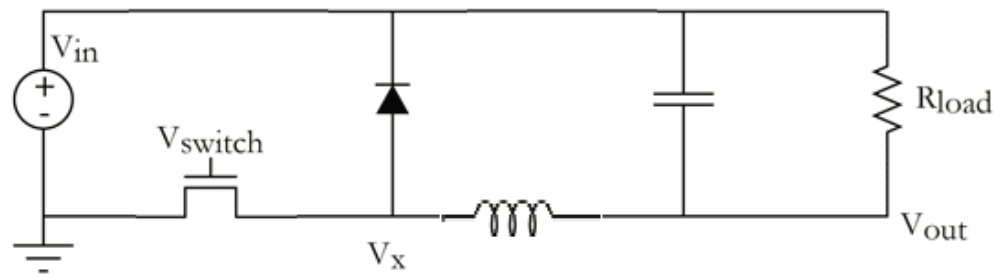


Figure 2-3 Reverse buck converter

The passive components are designed and selected based on buck converter design requirements, as shown in Table 2-3.

Table 2-3 Circuit specifications

V_{in}	400V
V_{out}	160V
I_{out}	10A
F_{sw}	500kHz
$\Delta I_L(\text{peak to peak})$	30%

Table 2-3 (continued)

$\Delta V_{out}(\text{peak to peak})$	1%
Pout	1600W

The following ideal passive component values are selected based on the specifications above.

Table 2-4 Passive components

Component	Value
Output capacitor	1 μ F
Inductor	64 μ H
Resistive load	16ohm

The bulk capacitor value also needs to be selected. The magnitude of the input current transient is calculated from formulas below [17]. Efficiency can be assumed at 70% as a lower value in order to leave design margin. Bulk capacitor calculated value from the formulas below is 88 μ F.

$$\Delta I_{IN} = \frac{V_{OUT}}{V_{IN} \times \eta} \times \Delta I_{OUT}$$

$$C = \frac{1.21 \times I_{tr}^2 \times L}{\Delta V^2}$$

In addition, 1 μ F ceramic capacitors should be applied to both input and output as bypass capacitors since the design aims at 500kHz switching frequency which is a relatively high operating frequency. These ceramic capacitors also reduce the equivalent series resistance and inductance (ESR and ESL) of the bulk capacitor and output capacitor since ceramic capacitors have extremely low parasitic elements. These will improve the efficiency and switching performance.

2.3 Flex Circuit Development

There are three flex parts needed for the flex power module. First is used as interconnection between gate driver and MOSFET, which has a double layer double access feature. Gate drive bare die is flipped and attached to the top side of this layer as well as a 0.1 μ F bypass capacitor and gate resistor in a 0805 standard package. The power MOSFET die is attached to the bottom side of the layer. Gate signal generated by a signal generator is amplified by gate driver and applied to the MOSFET gate through vias. Copper traces are extended and solderable pads are placed at both ends of the part in order to make electrical connection with the PCB mother board. Figure 2-4 is the actual circuit picture.

2.3.1 Layout Challenges

Notice that the bright silver areas are solderable pads which are covered with solder and hot-air leveled during production. All flex circuits were patterned and etched by an outside contractor to the specifications and layout created in this thesis. The light black area which is

circled in red is where a mistake occurred due to misinterpretation in the layout files. The pads should be solder filled. Unfortunately, the Cu trace was covered by insulated material. After communication with the manufacturer, we found a misunderstanding happened because the part was designed with “partial” double-layer double-access and “partial” single-layer double-access, which are not standard for manufacturing. The other two parts which are single-layer double-access parts have similar issues as shown in Figure 2-5. Designers should be careful when placing single layer and double layer parts on the same panel for fabrication.



Figure 2-4 Double layer double access part

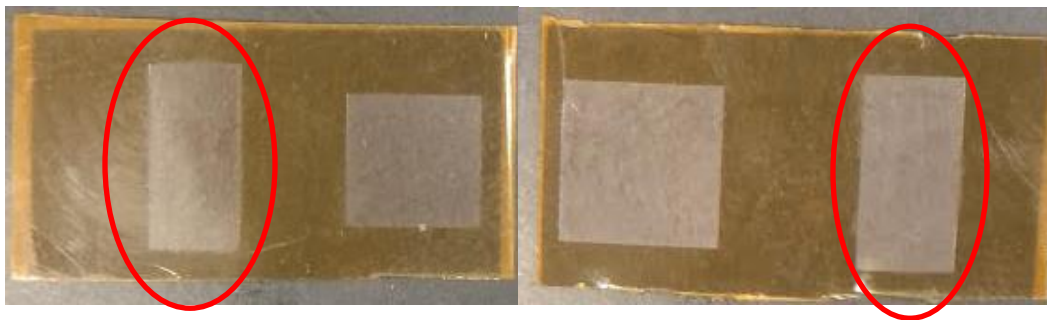


Figure 2-5 Single layer double access part

Another design flaw of the flex circuit is the gate driver landing pattern as Figure 2-6 shows. Comparing the pattern with die attachment diagram in Figure 2-2, they have identical top

views. However, since the die flips and is soldered onto the circuit, the landing pattern should be mirrored against the diagram. This is also a critical point that new designers should pay close attention to when creating flip-chip versus wire-bond footprints. Since flex circuits generally require longer turnaround time and higher expense (usually a few hundred dollars for a single-layer panel), a lot of details should be taken into consideration before ordering.

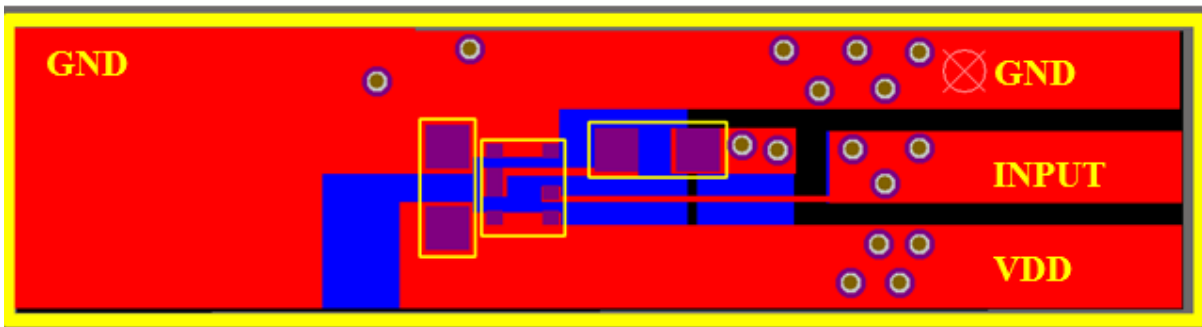
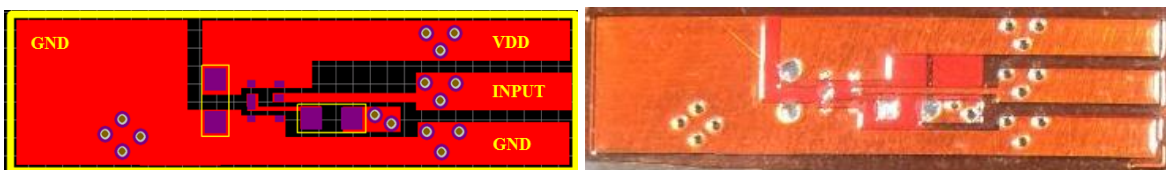


Figure 2-6 Incorrect gate driver footprint for wire bonding and not flip-chip

The final flex circuits were ordered from American Circuits, Inc. of Charlotte, NC. The three parts are modified to be double-layer double-access. By use of vias to create “single-layer double-access” parts, gerber-file layouts and actual circuits for Part A-C are shown side-by-side in Figure 2-7. The Part A is 825x220mil (21x5.5mm); Part B is 625x 410mil (16x10mm); and Part C is 625x425mil (16x10mm).

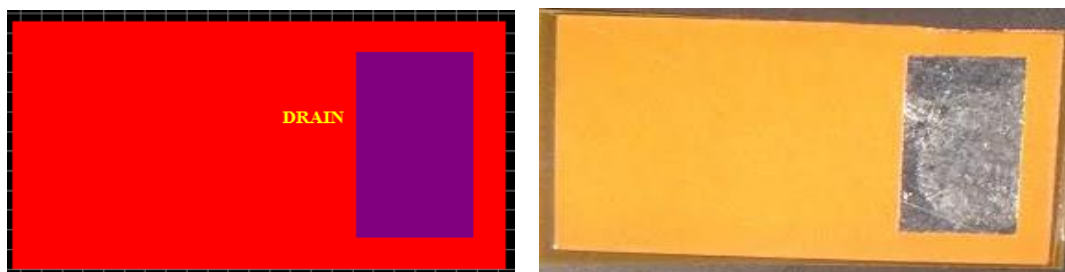
Figure 2-7 Gerber files and fabricated circuits



a) Part A top side (Gerber and circuit)



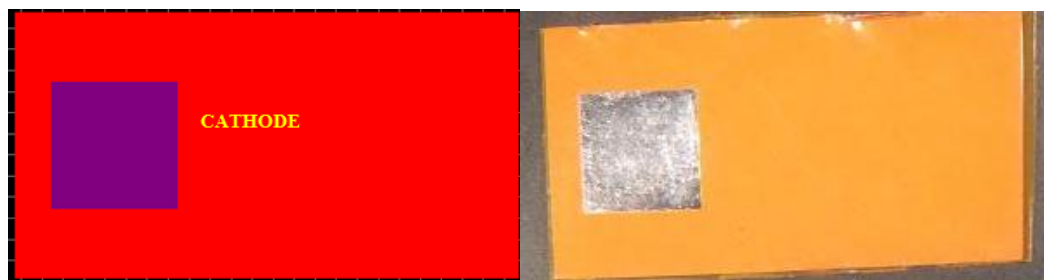
b) Part A bottom side



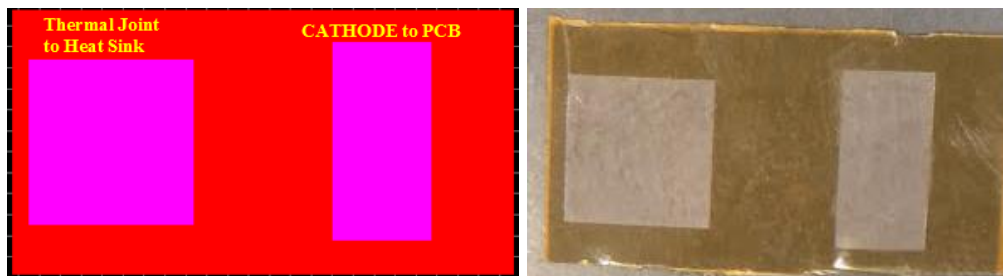
c) Part B top side



d) Part B bottom side



e) Part C top side



f) Part C bottom side

2.4 Test Circuit Development

Test circuit development is the circuit design of a FR4 PCB mother board. Altium designer is the circuit design software used in the thesis. The circuit design problems, though not very complicated to a seasoned designer, shows the difficulties in designing flex for a beginner. Figure 2-8 is the PCB circuit under Altium Designer environment. Six solderable pads are available in the blue-square area. However, as it shows in Figure 2-9, pads are covered by epoxy insulation material in the blue-square area. This is because mask relief was absent for these pads. In Altium Design, the Top Solder layer is the solder mask layer. One should always pay attention to make the mask relief for the pads. This issue was resolved in the later chapter by physically removing the insulation and exposing Cu trace.

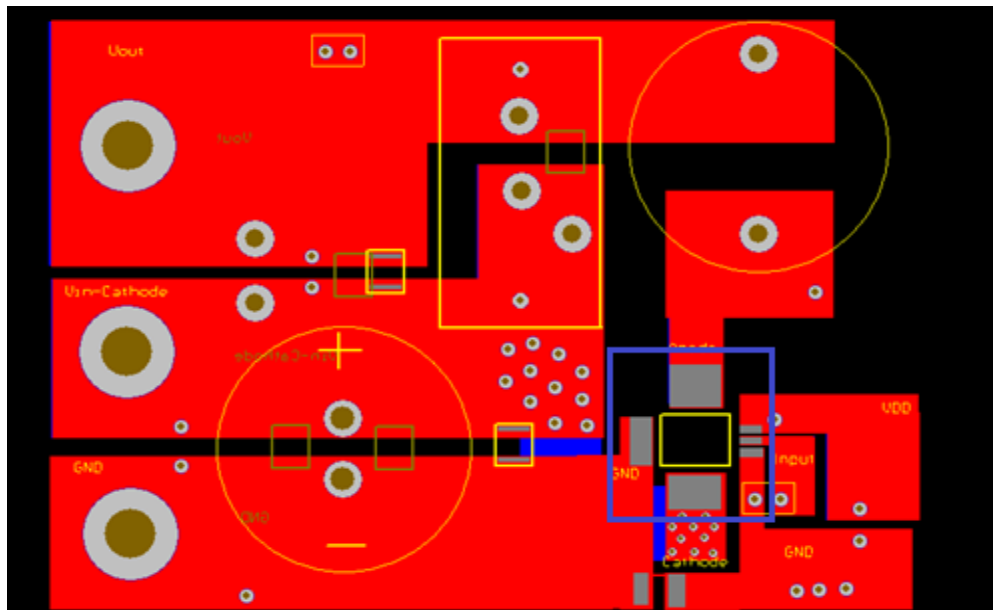


Figure 2-8 PCB design file in Altium Designer

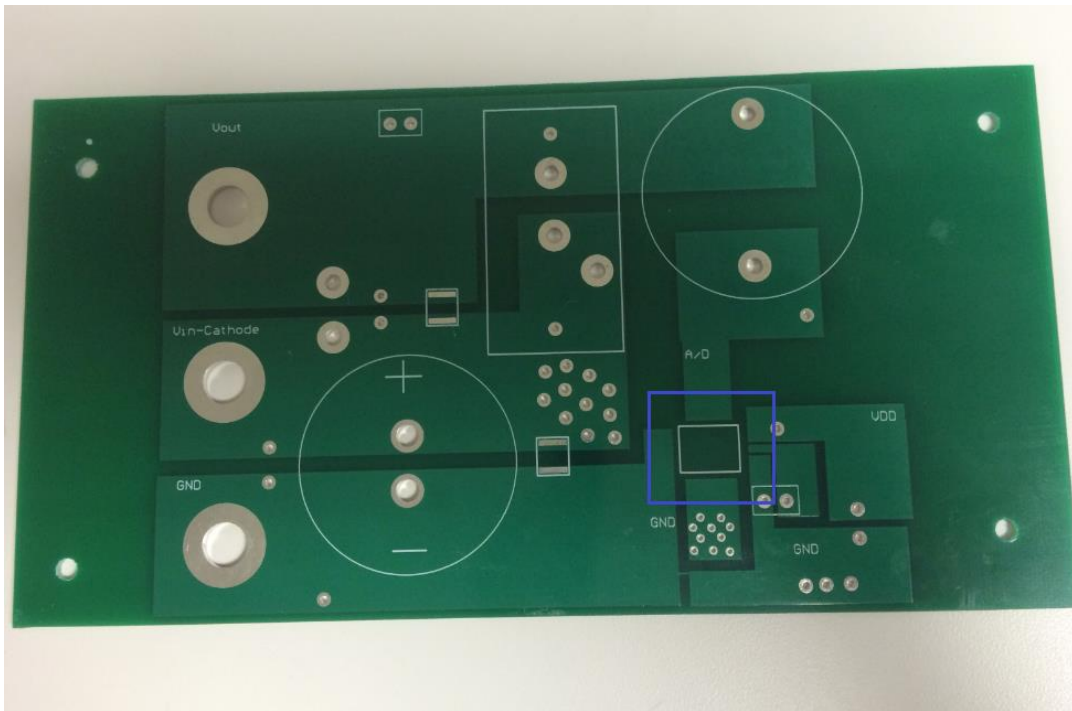


Figure 2-9 PCB circuit

2.5 Simulation Results

2.5.1 Electrical simulation

Both electrical and thermal simulations are presented in this section. Electrical simulation is based on LTspice® Linear Technology. Circuit functionality and device switching performance will be checked. In addition, simulation results are also helpful with component selection and thermal analysis.

Electric parasitic elements should be considered for high-current and high-frequency switching circuit operation. The parasitics particularly inductances in the critical loops of a

buck topology, are critical for the overall switching speed. There are two critical loops in the design. One is the AC current loop in the power stage as shown in Figure 2-10. Parasitic inductance between diode and MOSFET can be neglected since they are stacked vertically without any wire or via through the interconnection. The parasitic inductance in the loop is mostly induced by vias between input bypass capacitor and anode of the diode. The PCB via inductance value can be calculated using formula below:

$$\text{Inductance: } L=5.08h \times [\ln(4h/D)+1] \text{ [18]}$$

Where D is the diameter of the via, h is the thickness of the PCB, and H is the length of the via. There are two kinds of vias in the critical loop on the PCB which have the diameter of 94mil and 56mil. For a 1.6mm standard thickness FR4 PCB, one 94mil via will add $L=5.08 \times 0.063 \times [\ln(4 \times 0.063/0.094)+1]=0.64\text{nH}$. The other 56mil via will add $L=0.8\text{nH}$. On the PCB, there are eleven 47mil vias parallel and ten 28mil vias parallel in the loop. Hence the parasitic inductance of these vias is $0.63\text{nH}/11+0.8\text{nH}/10=0.14\text{nH}$

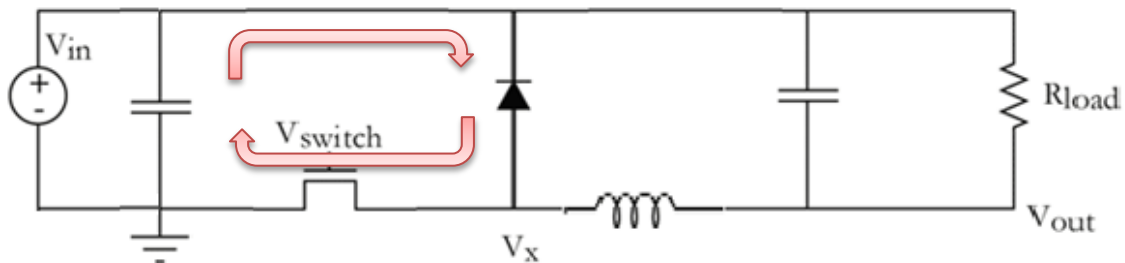


Figure 2-10 Critical loop in buck power stage

For gate drive control, the current paths for the MOSFET turn-on and turn-off are shown in Figure 2-11. Blue and yellow arrow lines represent the turn-on loops, whereas yellow and red lines represent the turn-off loop. These critical loops play crucial roles on determining the switching speed, and designers should make every effort to shorten the loops and minimize inductance and resistance in the paths.

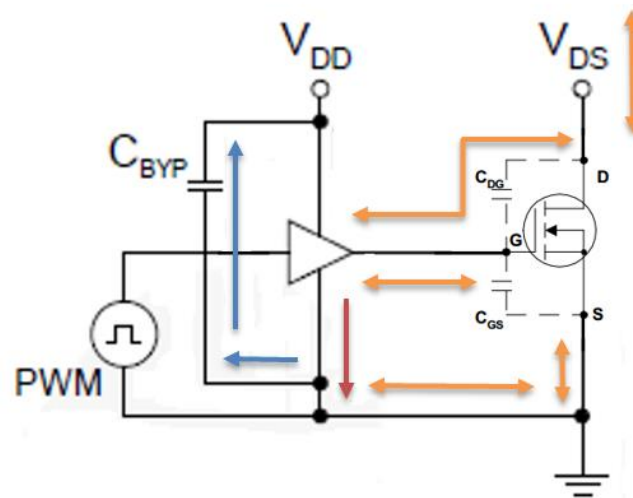


Figure 2-11 Gate drive turn-on and turn off current paths [16]

The buck topology constructed in LTspice®Linear Technology is shown in Figure 2-12. Parasitic inductance is included. Notice that the MOSFET and diode model number are different from what we mentioned in previous chapter. In fact, the MOSFET represents the same device, and however diode represents another similar CREE's device which has 1200V blocking voltage and 20A average current rating. The reason why we use this device model is

that CPW5-1200-Z050B is a new product of CREE and spice model is not available for the moment. This 20A model is good enough for the thesis since its material is same as CPW5-1200-Z050B and our load current is 10A at maximum. The MOSFET electro-thermal spice model is provided with five terminals which are drain, source, gate Tj and Tc. The terminals Tj and Tc were specifically included in the design to analyze the self-heating of the device as a function of time. The terminal Tc represents the case temperature and Tj represents the junction temperature. The temperature connections are working as voltage pins. Therefore a potential difference of 1V refers to a temperature difference of 1°C [19]. In this case, Tc is set to be 25°C as room temperature. The Tj is initially set to be worst case 150°C and a switching loss can be obtained under this junction temperature. This loss is then put into thermal simulation to get a new junction temperature. The Tj is then updated with the new value and a new switching loss is obtained again. As a result, a converged Tj is obtained by multiple iterations, which is 98°C as shown in Figure 2-12. Figure 2-13 is drain-source voltage (Vds) and drain current (Id) waveforms under 500kHz switching frequency and 40% duty cycle. Switching loss in one cycle can be obtained as 130μJ, which is the integral of the product of Vds and Id. Steady state inductor current is shown in Figure 2-14 and a 14A current rated inductor is selected accordingly. Schottky diode switching transient is also provided in Figure 2-15, where the switching loss of diode is obtained as 14μJ.

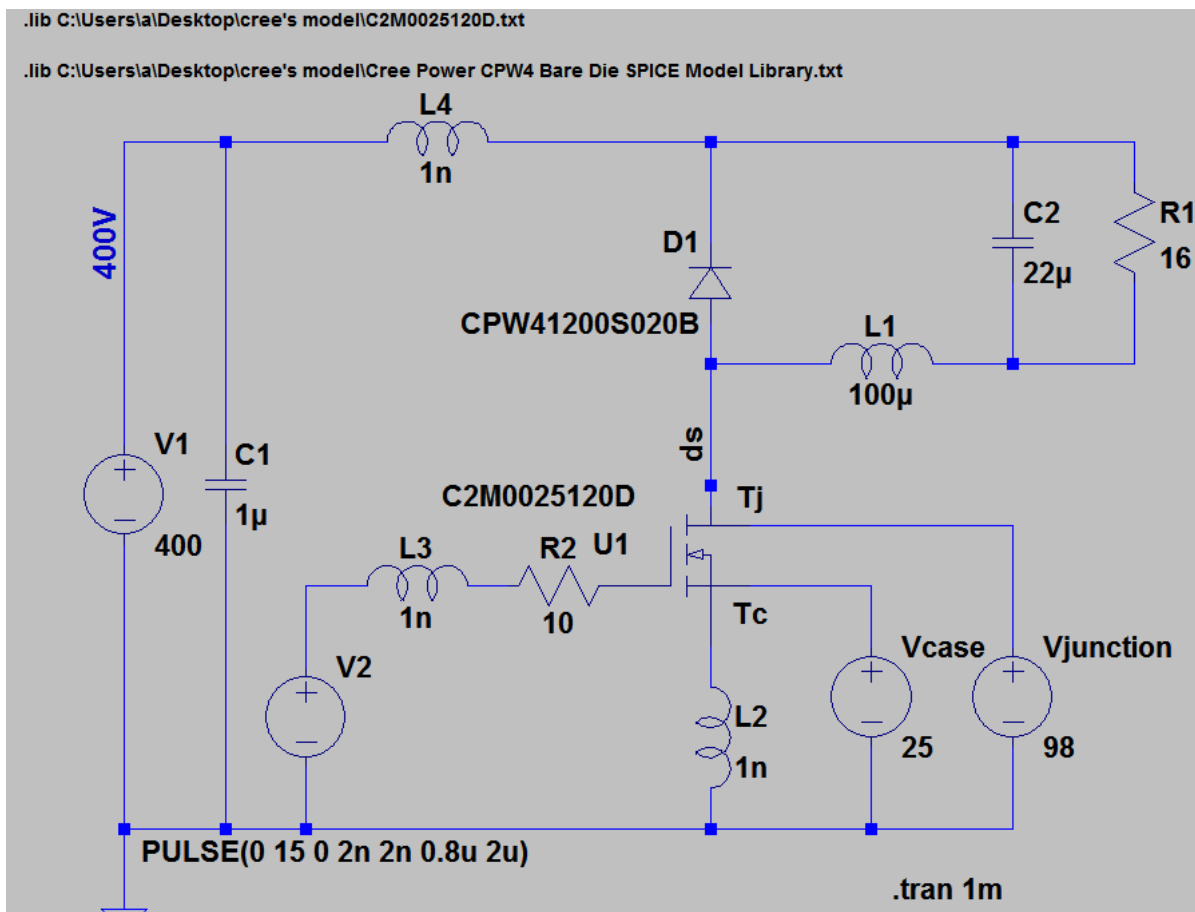


Figure 2-12 Reverse buck topology

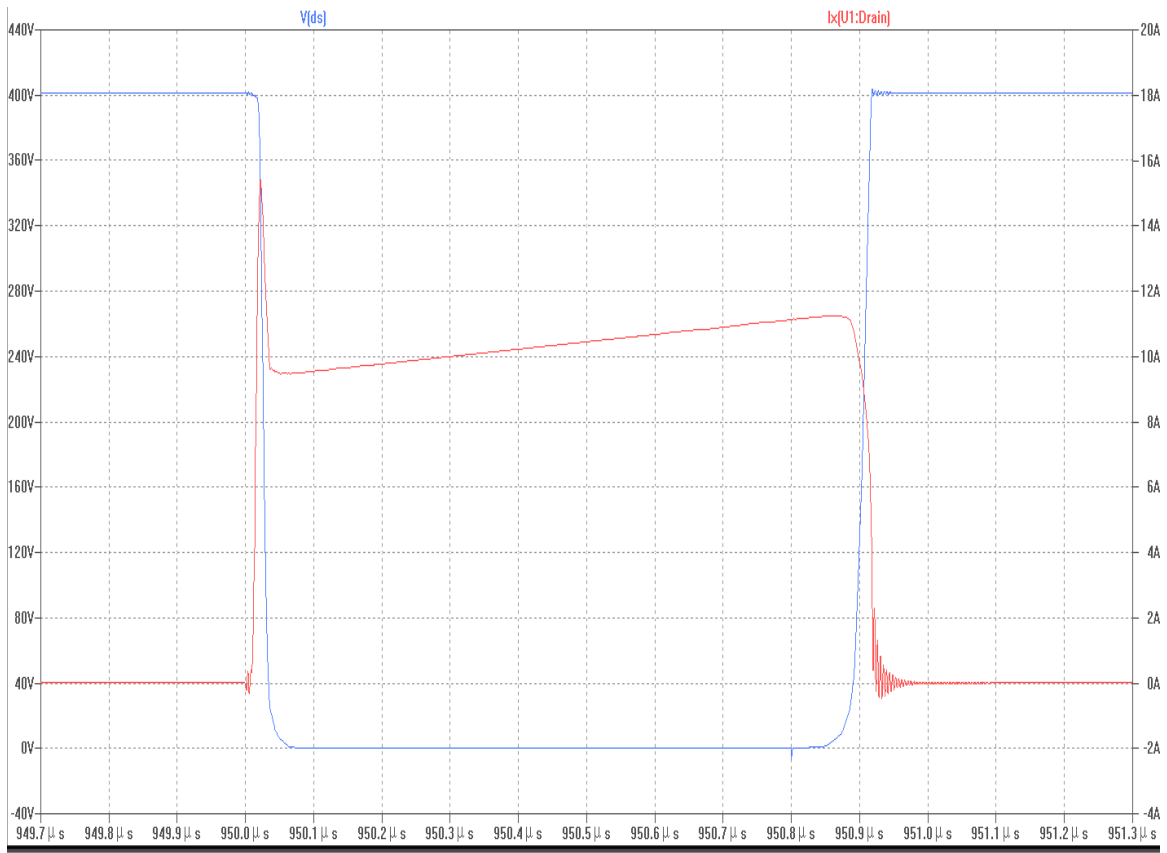


Figure 2-13 V_{ds} & I_d

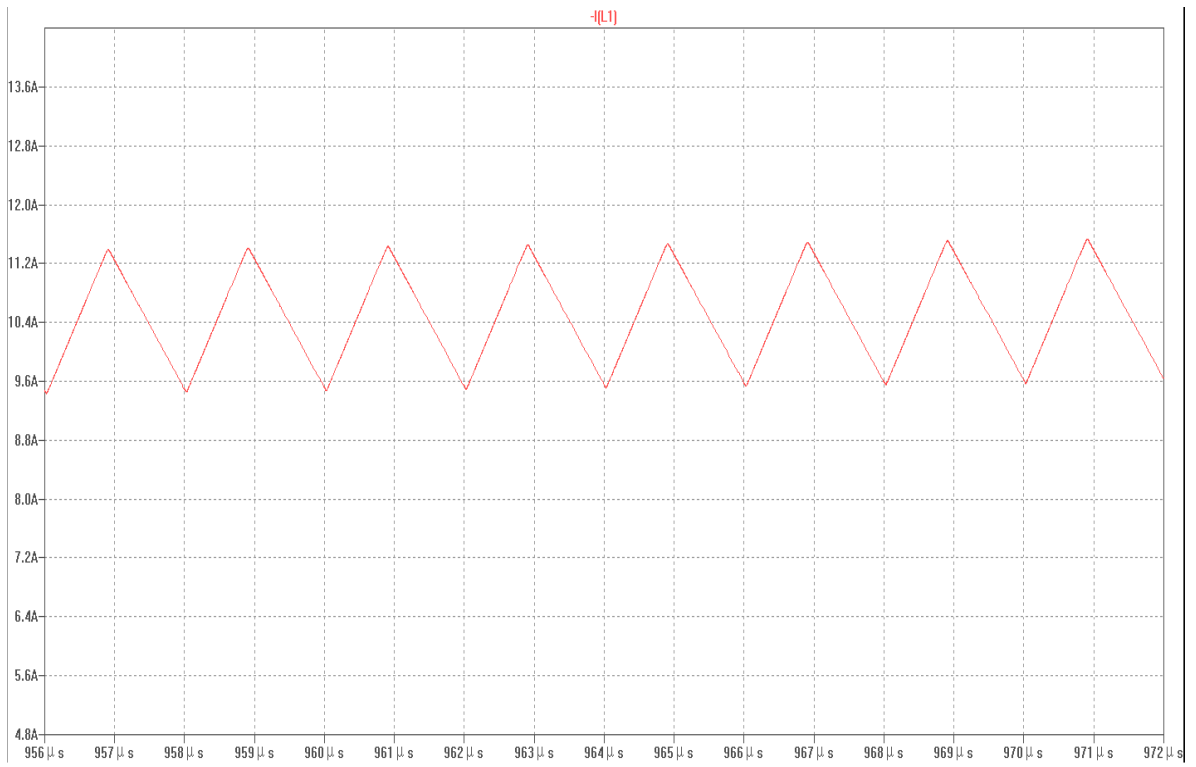


Figure 2-14 Steady state inductor current

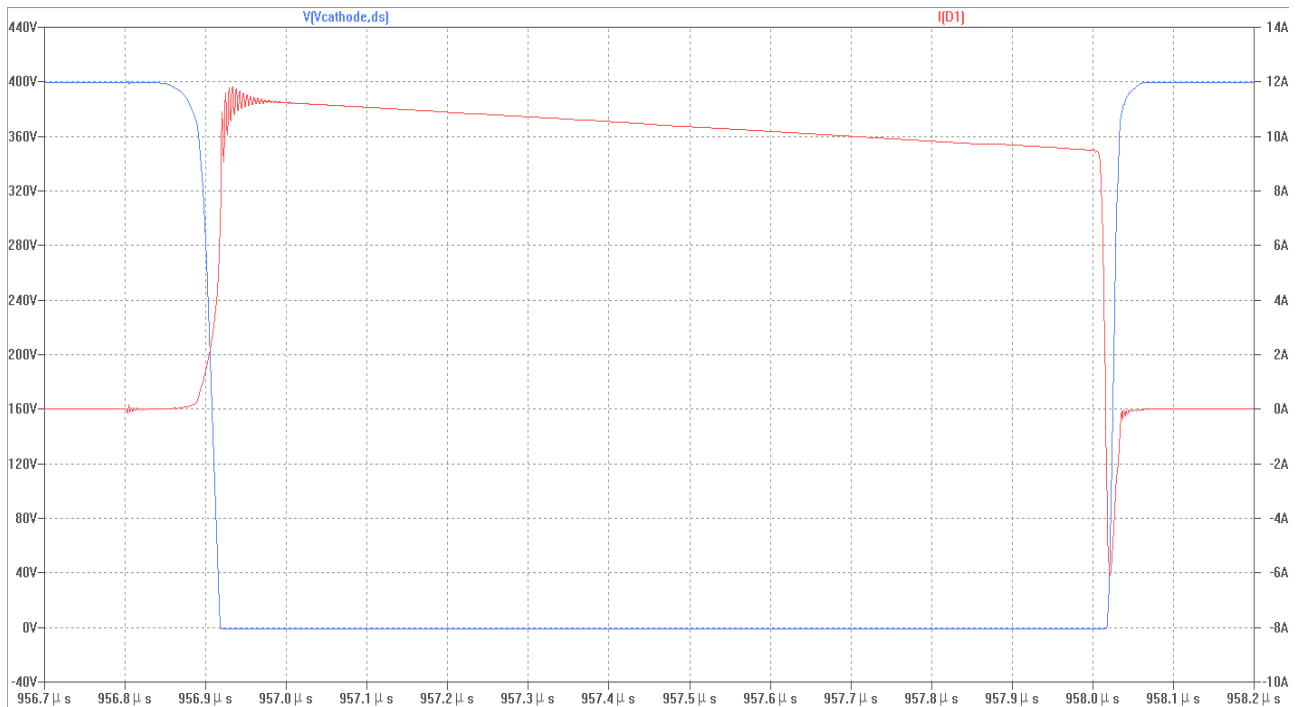


Figure 2-15 Vdiode & Idiode

2.5.2 Thermal simulation

Thermal analysis calculates the temperature and heat transfer within and between components in the design and its environment. The simulation analysis is conducted in COMSOL Multiphysics® Modeling Software. The flex module is modeled in the software and steady-state heat transfer condition is obtained.

To determine whether or not power devices are suitable for a particular application from a thermal standpoint, it is necessary to calculate their power dissipation. The power devices in the thesis, SiC MOSFET and diode, are major heat sources in the flex module. Heat dissipation of gate drive chip (FAN3122C) can be neglected compared with the power

devices. The MOSFET power dissipation is mainly made up of two parts, resistive losses and switching losses. The switching MOSFET's resistive losses are calculated using its duty factor and $R_{ds(on)}$:

$$P_{resistive} = [I_{on}^2 \times R_{ds(on)}] \times (V_{out}/V_{in})$$

According to the datasheet, $R_{ds(on)}=43m\Omega$ @50A, 150°C which can be used as worst case condition. In addition, duty cycle and I_{on} is set to be 40% and 10A respectively. Resistive loss is then obtained as 1.72W.

Calculating the switching MOSFET's switching loss is difficult because it depends on many difficult-to-quantify and typically unspecified factors that influence both turn-on and turn-off. As switching losses per cycle are obtained in the electrical simulation, the following formula is used as a rough approximation to be the first step in evaluating a MOSFET:

$$P_{switching}=f_{sw} \times \text{Switching loss per cycle}$$

Where f_{sw} is the targeted switching frequency 500kHz. Switching loss per cycle is 130μJ. Hence, power dissipation of switching losses is 65W. Switching losses should be calculated again once switching waveform is obtained on the lab bench.

For the Schottky diode, the following formula can be used for conduction loss calculation:

$$P_{con}=V_f \times I_f \times (1-V_{out}/V_{in})$$

Where V_f is DC forward voltage, I_f is forward current. According to the datasheet, $V_f=1.5V @ 25A, 125^\circ C$. Assume $I_f=10A$. Conduction loss is then obtained as 9W. Switching loss of the diode is calculated based on electrical simulation:

$$P_{\text{switching}} = f_{\text{sw}} \times \text{Switching loss per cycle}$$

Where f_{sw} is 500kHz and switching loss per cycle is 14 μ J. Hence, the power dissipation of switching loss is 7W.

Then the flex module is built and studied in COMSOL environment. Figure 2-16 shows how the module is built. The parts in the module are built as blocks. Table 2-5 shows the part dimensions from top to the bottom in the model.

Table 2-5 Part Dimensions

	Thickness(mm)	Planar dimension(mm)
Part A Cu trace	0.1	5.5 \times 12.3
Solder 2	0.1	3.05 \times 4.54
MOSFET	0.18	4.04 \times 6.44
Solder 1	0.1	4.04 \times 6.44
Part B Cu trace	0.1	16 \times 10
Solder 2	0.1	3.8 \times 3.8

Table 2-5 (continued)

Diode	0.38	5×5
Solder	0.1	5×5
Part C Cu trace	0.1	16×10
MX-4	0.2	6×6

The materials should be assigned to each block after the 3D model is constructed. Table 2-6 shows the thermal characteristics of the materials used in the analysis. Copper is assigned to the flex circuit trace. Silicon carbide is assigned to the power devices. The MX-4 is a non-conductive thermal paste that is used to thermally connect Part C to heat sink. The Sn63Pb37 is a solder that will be described in a later chapter.

Table 2-5 Thermal characteristics

Materials	Density (kg/m ³)	Thermal conductivity (W/(m*K))
Copper	8700	400
Silicon Carbide	3200	450
MX-4	2500	8.5
Sn63Pb37	9000	50

Figure 2-16 and Figure 2-17 show the steady-state temperature model of the flex module. Figure 2-15 is top view and Figure 2-16 is bottom view. The bottom of the module, which is the thermal paste layer, is set to be room temperature as it is directly connected to bulk heat sink. The extended ends of three flex part are also set to be room temperature since they are connected with the PCB traces directly. The hottest point is located in the MOSFET layer and reaches 99°C, which is below the maximum operating temperature of 150°C in the datasheet. The thermal paste layer is one of the main reasons that causes this high temperature rise since thermal conductivity of MX-4 is very low compared with other layers. In conclusion, the flex module design is in compliance with the thermal requirements of the power devices.

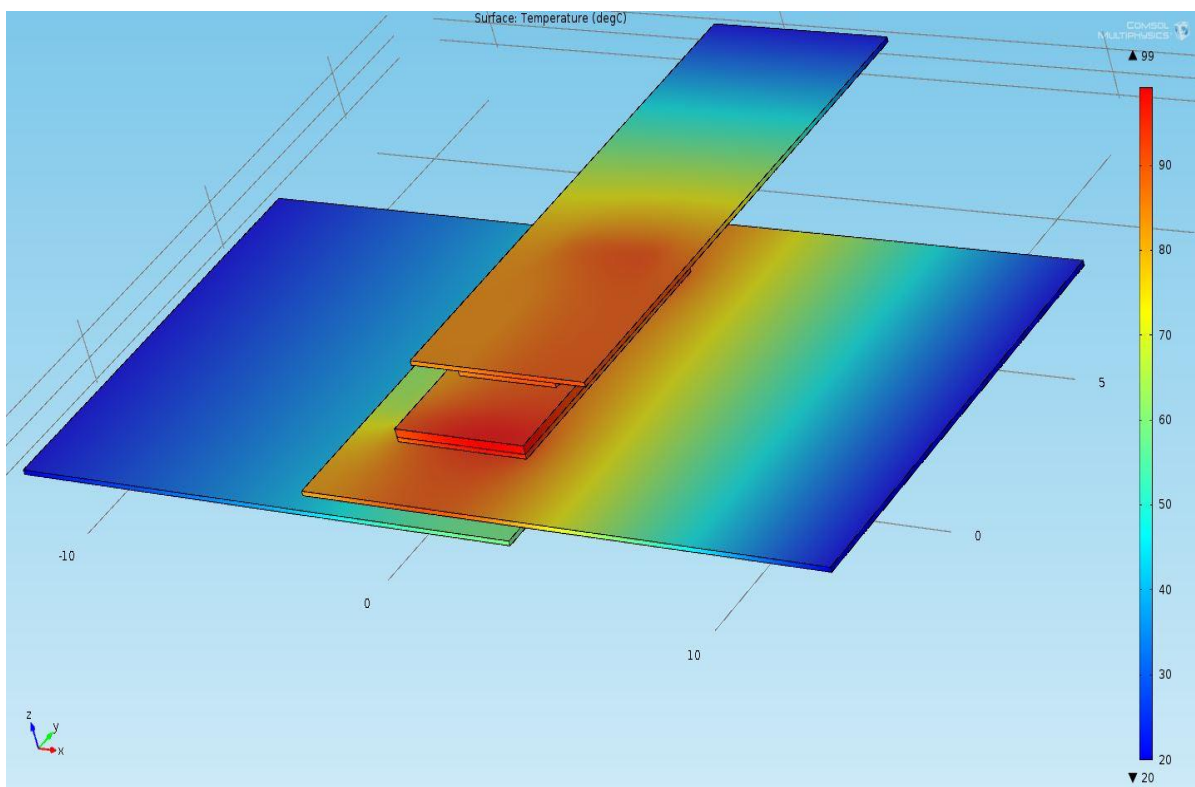


Figure 2-16 Module top view

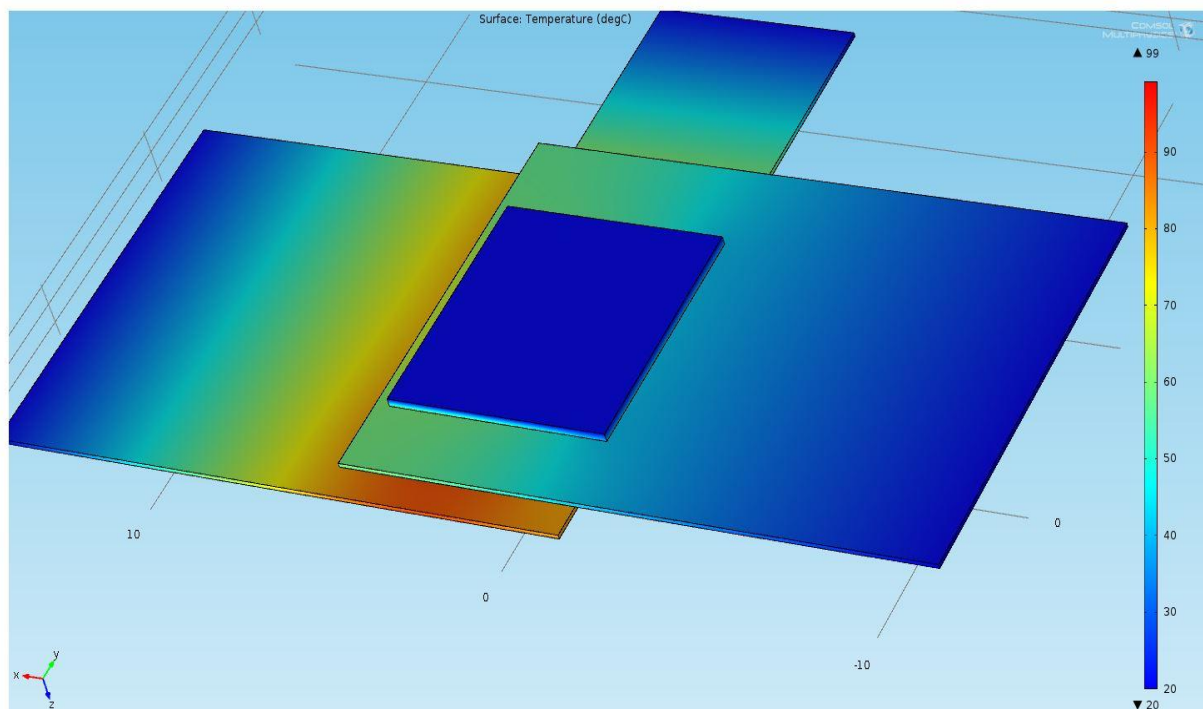


Figure 2-17 Module bottom view

CHAPTER 3 MODULE MATERIALS AND FABRICATION PROCESS

This chapter introduces the materials in the module and fabrication process in the lab. The SiC MOSFET and diode are from CREE, Inc and the flex circuit is chosen as the substrate. Surface metallization of the power devices is a major issue addressed in this chapter. However, the base process has been developed, but needs further improvement due to an undesirable metallization result.

3.1 MOSFET and Diode

Currently, most of the devices in commercial power modules are interconnected by bonding wires. Almost all power devices are designed for wire bonding instead of direct solder interconnect. The power MOSFET and diode used in this thesis were acquired from CREE, Inc. For the SiC power MOSFET, it has source and gate pads with approximately 4um thick Al. The backside of the die is the drain, which has a Ag solderable metallization (0.8/0.6um thick Ni/Ag). For the SiC Schottky diode, similarly, it has 4um Al anode metallization and a Ag (1.8um Ni/Ag) cathode metallization, according to the datasheet. Except for the bond pads, the rest of the die is covered with a polyimide passivation to form the insulation between pads and die edges. The absence of solderable metallization on the source and gate pads of the MOSFET, and anodes in the Schottky diodes, has to be addressed to achieve solder interconnection between die and the flexible printed circuit.

3.1.1 Metallization Preparation

Electron beam physical vapor deposition approach (EBPVD) is selected for the metallization process to make the Al pads solderable. For the thin film materials, Ti/Ni/Cu under bump metallization was selected. Target thickness is 200nm/1000nm/200nm respectively. The Ti layer adheres well to the Al surface on the device pads. The Cu layer on top helps with solder wetting as well as acting as an oxidization layer. The Ni layer has three functions: [9]

- It acts as a diffusion barrier between Al and Cu, otherwise intermetallic formation between them could lead to the depletion of the Cu layer, thereby preventing solder wetting.
- It is an excellent solder diffusion barrier
- It may also provide a solder wetting surface in case Cu on top of the metallization layers is consumed

3.1.2 Metallization process

The metallization process in this thesis has been developed in the Nanofabrication Facility (NNF) at the NCSU Monteith Research Center building. The major equipment that has been used in this project is an e-Beam Evaporator in Figure 3-1. It is equipped with 4 load locks for thin film metal depositions and can accommodate wafers of up to 6'' in diameter.

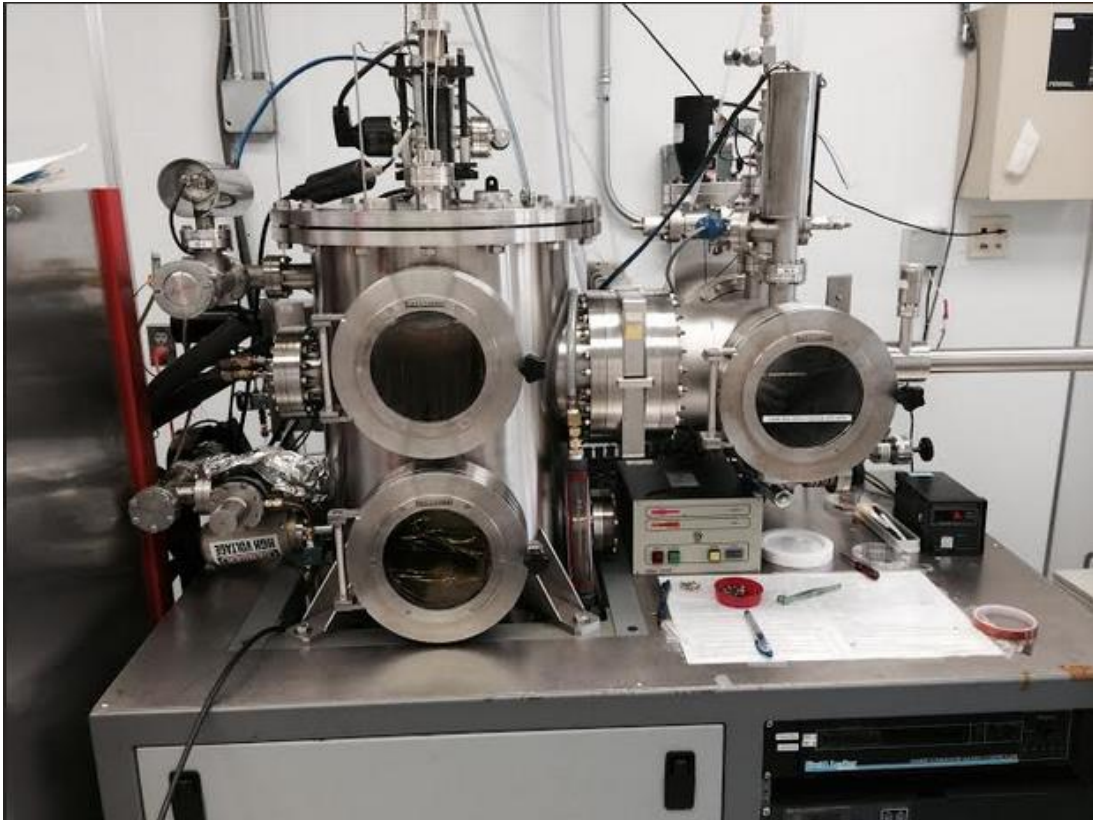


Figure 3-1 E-beam evaporator

First, the deposition rate of each metal should be obtained respectively in order to keep good track of the thickness during the deposition process. Therefore, glass slides are used to monitor each metal deposition rate. Figure 3-2 is an example of a Ti deposition on glass. The mirror areas on the glass are where Ti adheres to the glass. The transparent glass area was covered by kapton tape so that the thickness of metal layer can be obtained by measuring the height difference between these two areas. Precise measuring tool, Nanometrics in NNF, was used for thickness measurement. Figure 3-3 shows selected raw thickness data measured.

According to the data, the average thickness of the Ti glass slide is 2194\AA . The mean deposition rate then can be calculated by dividing thickness by deposition time.



Figure 3-2 Ti deposition sample

Scan Parameters					
Scan Type	Standard Scan				
ID	0				
Stylus	Radius: 12.5 μm				
Location	-16894.7 μm	23841.3 μm			
Length	1674.0 μm				
Duration	10 sec				
Resolution	0.558 $\mu\text{m}/\text{sample}$				
Force	10.00 mg				
Measurement Range	6.5 μm				
Profile	Hills&Valleys				
Display Range	Auto				
R. Cursor	Pos: 618.8 μm Width: 71.8 μm				
M. Cursor	Pos: 429.7 μm Width: 62.1 μm				
Analytical Results					
Function	R.Cur Pos	R.Cur Width	M.Cur Pos	M.Cur Width	Result
ASH	618.8 μm	71.8 μm	944.1 μm	62.1 μm	2194.1 A

Figure 3-3 Raw data obtained from Nanometrics

After deposition of each layer of metal, the deposition rate was obtained for each of the three kinds of metal. The rates are $2\text{\AA}/\text{sec}$ for Ti, $4.5\text{\AA}/\text{sec}$ for Ni and $0.3\text{\AA}/\text{sec}$ for Cu. Then three layers of metal were deposited at one time which means to load all metal materials into e-beam chamber and run the entire process without breaking vacuum. The reason of doing this is because metal layers should not be exposed to air during the deposition since the metal may oxidize and prevent the metal vapor from solidifying and sticking to the previous metal layer. Figure 3-4 are mechanical chips (dummy chips) that were stabilized onto metal plate using Kapton tape but left openings at source and gate on MOSFET, and anode on diode.



Figure 3-4 Mechanical chips on metal plate

During the deposition, another issue made the process much slower than estimated. The tool has its own cooling system using water. As the process went on, the water temperature was also rising. According to the equipment manual, temperature of the cooling system should not go beyond 40°C , otherwise users should turn off the power until the temperature falls back to laboratory room temperature 17°C . Because of this, the deposition of Ni and Cu layers was not able to be finished in a single heating cycle. Table 3-1 shows some deposition parameters obtained from the test.

Table 3-1 Deposition process and thickness obtained

Metal	Heating cycles	Deposition time (one cycle)	Cooling time (one cycle)	Total time	Total thickness obtained(A)	Average deposition rate(A/sec)
Ti	1	15	10	25	2015	1.34
Ni	5	30	10	200	9295	0.77
Cu	11	30	10	440	1834	0.07

*Time is in minute

Metallization results are not desirable. As shown in Figure 3-5 are the samples taken out of the e-beam after the process. The Cu layer is the outer layer, and therefore, the metal layer presents a reddish brown color. However, the stacked layer failed to stick on the aluminum pads (on the chip) or metal plate. It showed weak strength and was easy to peel off. Only three MOSFETs among the 6 samples can be taken for mechanical pull test after visual inspection under a microscope (Figure 3-6).



Figure 3-5 Samples after process

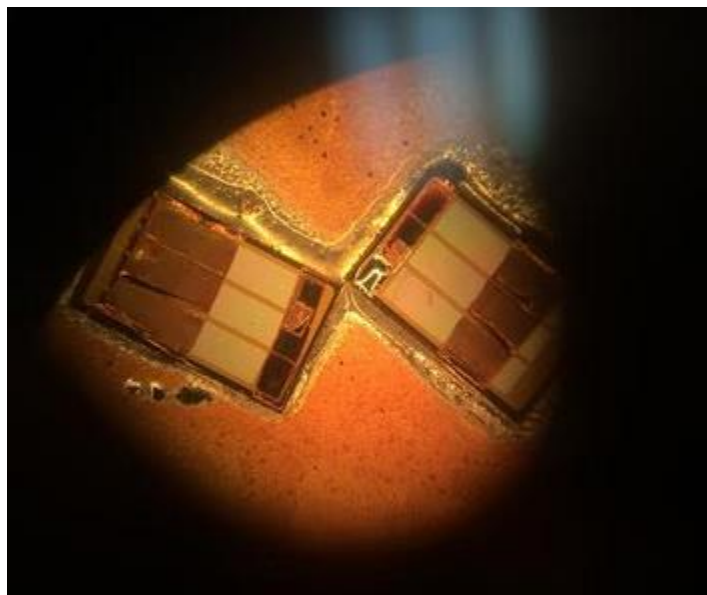


Figure 3-6 MOSFET samples under microscope

3.1.3 Pull test and results

Pull test is illustrated in Figure 3-7. Metallized MOSFET die was attached to a direct bonded copper (DBC) plate. A specifically sized pull stud with a rounded end used for this type of testing was soldered onto the metallized side of the MOSFET. The other end was bent for pull test. A force meter was then hooked up to measure the tension. As a result, the peak tension recorded in the pull test is 182g at $2.3 \times 4.0 \text{ mm}^2$ area which equals to 0.02 kg/mm^2 . According to [20], average strength of PVD Cu metallization is larger than 55 MPa which equals to 5.5 kg/mm^2 . In contrast, the strength of the metallized layers on MOSFET is not enough for the application. As a result, the metallization approach needs to be improved. The improvement should be made will be mentioned in future work in the last chapter.

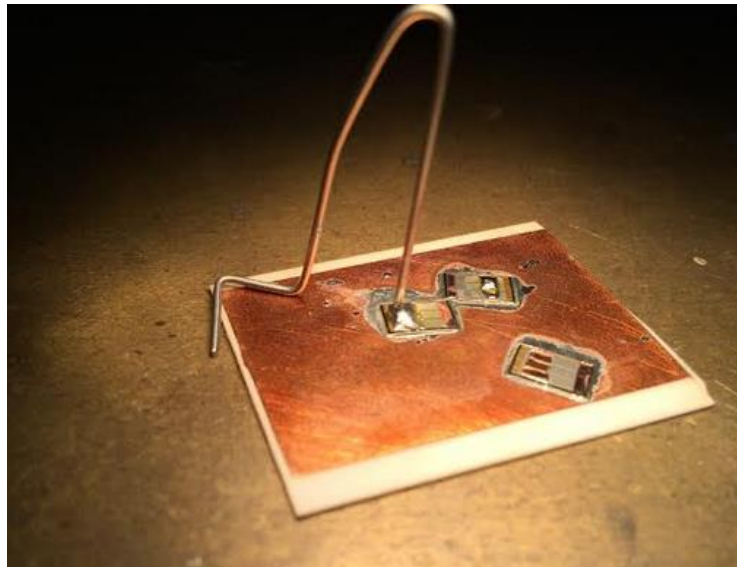


Figure 3-7 Pull test set up

3.2 Flex circuit

Flex circuits are ordered from American Circuit, Inc. Materials of Part A are depicted in Figure 1-2 where each polyimide layer is 1mil (25.4 μ m) thick and each Cu layer is 1oz (35 μ m). The Parts B and C are single-layer double-access, which use the same thickness materials as Part A. The reason of using single-layer for Parts B and C is because single-layer flex can provide better heat transfer capability than double layer. As it is shown in Figure 1-2, double-layer flex circuits always have an internal insulation material as well as adhesive layers in between the Cu layers which significantly increase the thermal resistance in the path. In contrast, single-layer double access flex is able to create a low thermal resistance path as shown in Figure 3-8. MOSFET and diode are vertically placed on both sides of Part B, since SiC has fairly good thermal conductivity. The thermal path made up of SiC and Cu materials is good for heat dissipation.

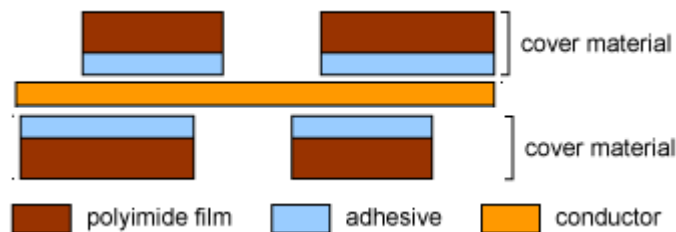


Figure 3-8 Single-layer double-access flex [6]

CHAPTER 4 ASSEMBLY, TESTING AND RESULTS

This chapter introduces the assembly and testing procedures of the chip-on-chip power module. However, due to failure of chip surface metallization, the actual MOSFET and diode were not used in the process. Since the thesis focuses on developing a fabrication process for the chip-on-chip power module, an identically sized Cu plate was used as substitution for the power devices. As a result, electrical characterization was developed with a wire-bonded power module. These procedures can be repeated once metallized power devices are obtained.

4.1 Power Module Assembly

Figure 4-1 shows the final flex circuit parts. The Part A has four component footprints on it, i.e. gate drive chip, MOSFET, gate drive bypass capacitor and gate resistor. Gate drive chip and MOSFET have the finest footprints that needs much effort to make sure they are connected well both mechanically and electrically. Since they are on opposite sides of Part A. Two kinds of solder (Table 4-1) with different melting temperatures are needed. The lower temperature solder (Sn63Pb37) is used for all the top side component attachment. The higher temperature solder (Sn10Pb88Ag2) is used for all the bottom side component attachment.

Table 4-1 Two types of solder with different melting temperature

Solder#	Alloy	Melting Temp

Table 4-1 (continued)

1	Sn63Pb37	183 ⁰ C
2	Sn10Pb88Ag2	268-290 ⁰ C

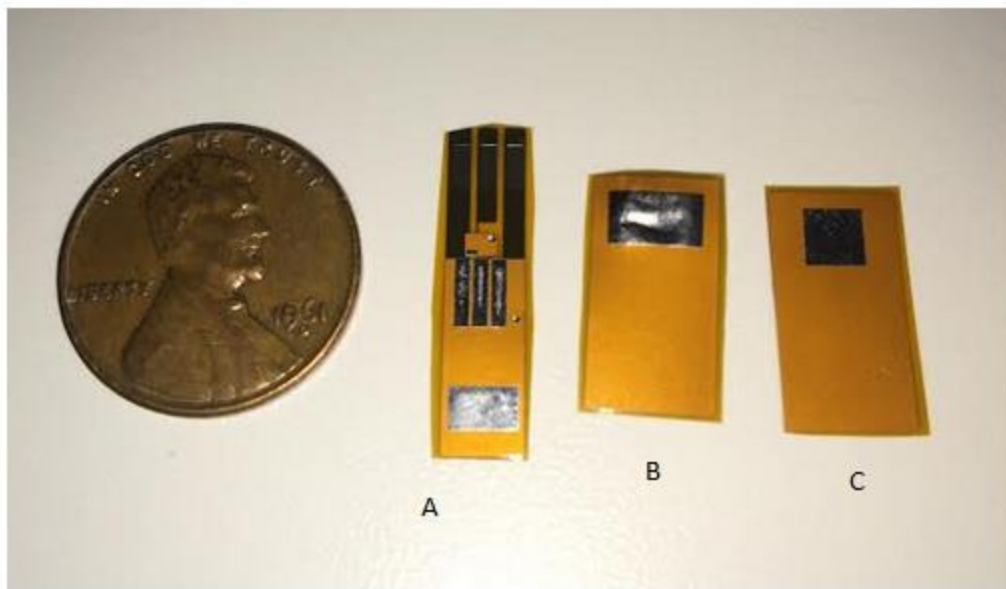


Figure 4-1 Size comparison of flex circuit parts and one cent coin

The assembly and electrical test process is developed step by step as below:

Step1. MOSFET source and gate attachment on Part A

MOSFET source and gate are attached to the bottom side of Part A. Therefore solder 2 should be used. In order to reach the high melting point of solder 2, a Sikama conduction belt reflow oven (Figure 4-2) was used in this step. The reflow process consists of four zones: pre-heat, pre-reflow, reflow and cool-down [21]. The reflow profile is shown in Figure 4-3

and belt speed was set as 6 inch/min. In addition, because of physical proximity of gate and source pads, short circuit may happen between gate and source and therefore need extra attention. A multimeter can be used to check the insulation between gate and source by probing plated vias. Figure 4-4 illustrates the module status after Step 1 in contrast with the finished module in Figure 1-7.



Figure 4-2 Sikama conduction belt reflow oven

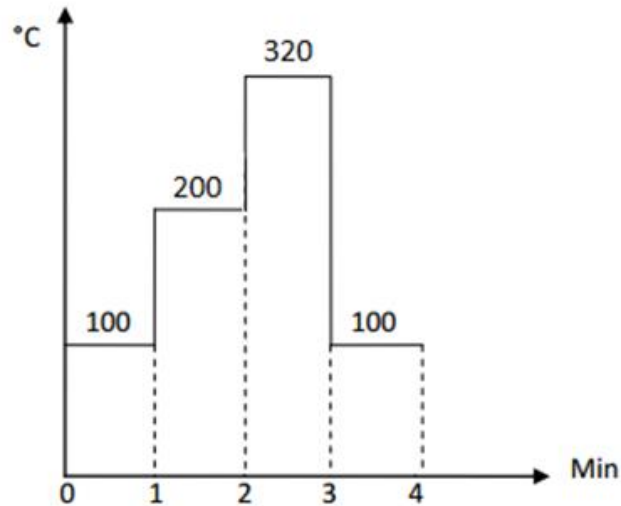


Figure 4-3 Reflow temperature profile



Figure 4-4 Semi-finished module after Step 1

Step2. Gate driver, capacitor and resistor attachment on Part A

Gate driver, capacitor and resistor were then attached on the top side of Part A with solder 1 applied on flex circuit pads. Figure 4-5 shows how solder paste is applied on pads. Since solder 1 is used for this step, the reflow temperature profile needs to be adjusted as Figure 4-6. After one cycle of lower temperature reflow process, Part A assembly was completed as Figure 4-7 shows (gate driver chip is absent). Figure 4-8 illustrate the module status after Step2.

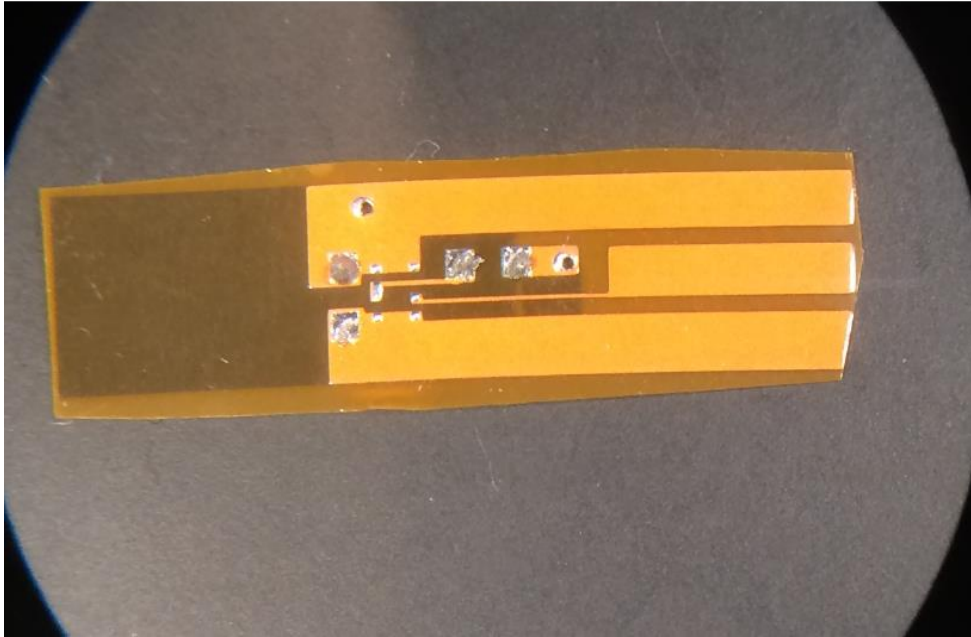


Figure 4-5 Solder paste on pads

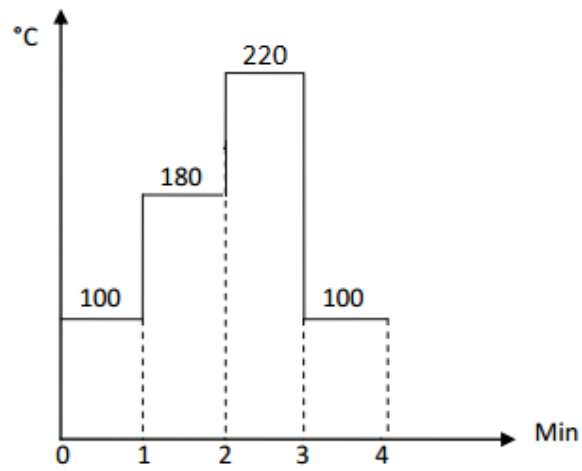


Figure 4-6 lower temperature reflow profile

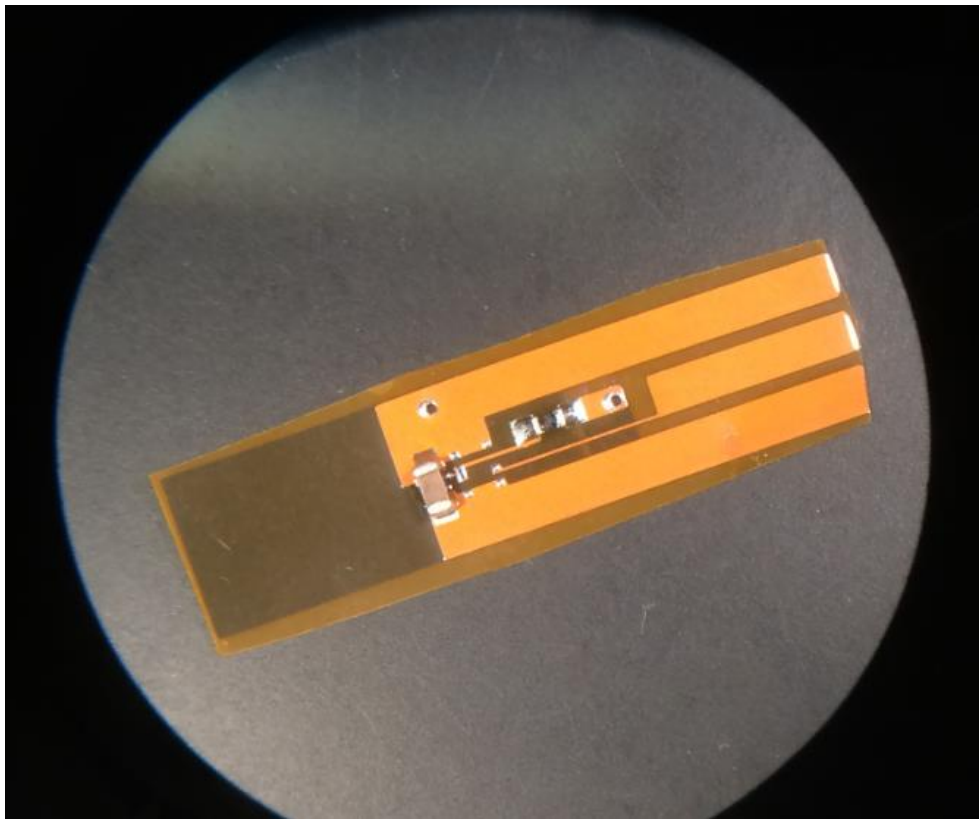


Figure 4-7 Part A with components

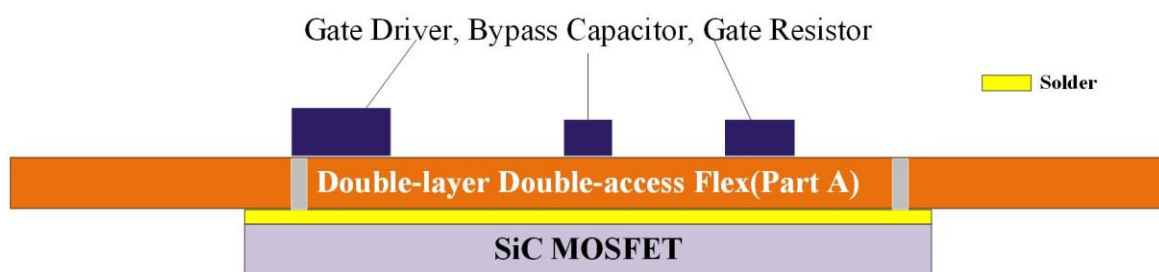


Figure 4-8 Semi-finished module after Step 2

Step3. Diode anode attachment to Part B

A similar process is done to Part B in this step. Diode anode should be soldered to the bottom side of Part B using 300⁰C Solder 2 as shown in Figure 4-9 with cathode . Likewise, Part B is probed at anode and cathode by a multimeter to check electrical conductivity. Figure 4-10 illustrates Part B assembly status. Thus far, pre-assembly of Parts A, B and C is finished.

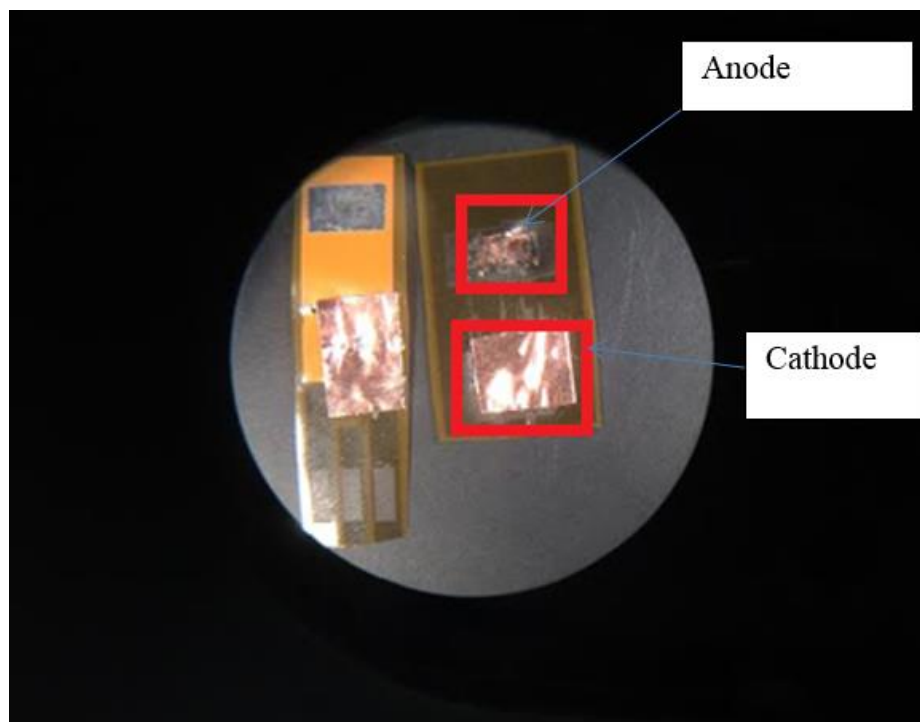


Figure 4-9 Bottom sides of Part A and B



Figure 4-10 Part B assembly status

Step4. Module final assembly

In this step, the top side of Part B should be attached to the MOSFET drain, and the top side of Part C should be attached to diode cathode. Solder 1 was applied on top sides of Part B and C (Figure 4-11), and then three parts were stacked together and placed into the reflow oven (Figure 4-12). Kapton tape is used to stabilize each part since the flowability of liquid solder paste during reflow may cause the parts to drift away from original place. Typically, a solder dam material is applied to confine solder spreading, but is skipped for this demonstration. The finished flex module is illustrated in Figure 4-13.

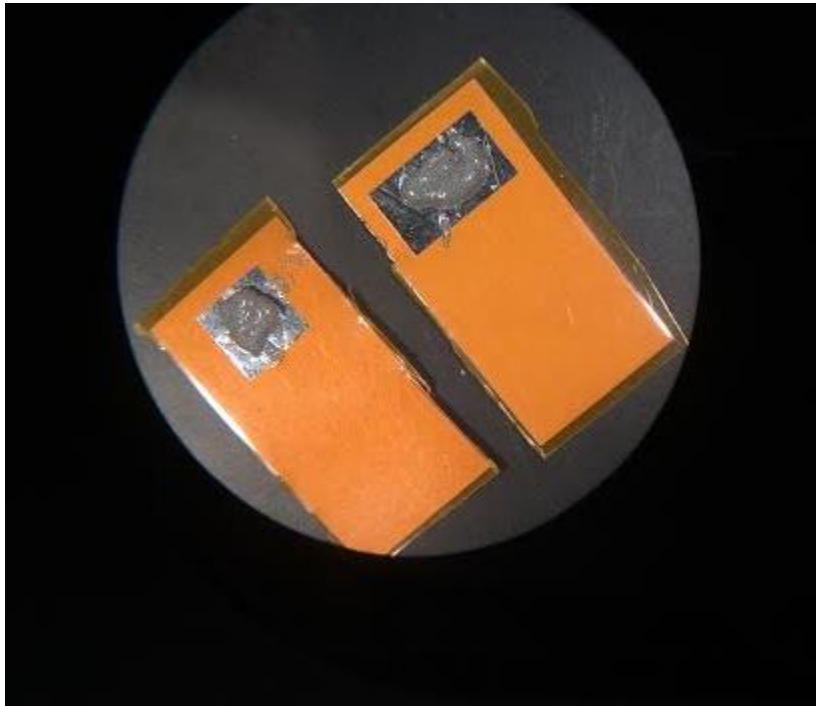


Figure 4-11 Solder paste on pads



Figure 4-12 Flex module before reflow process

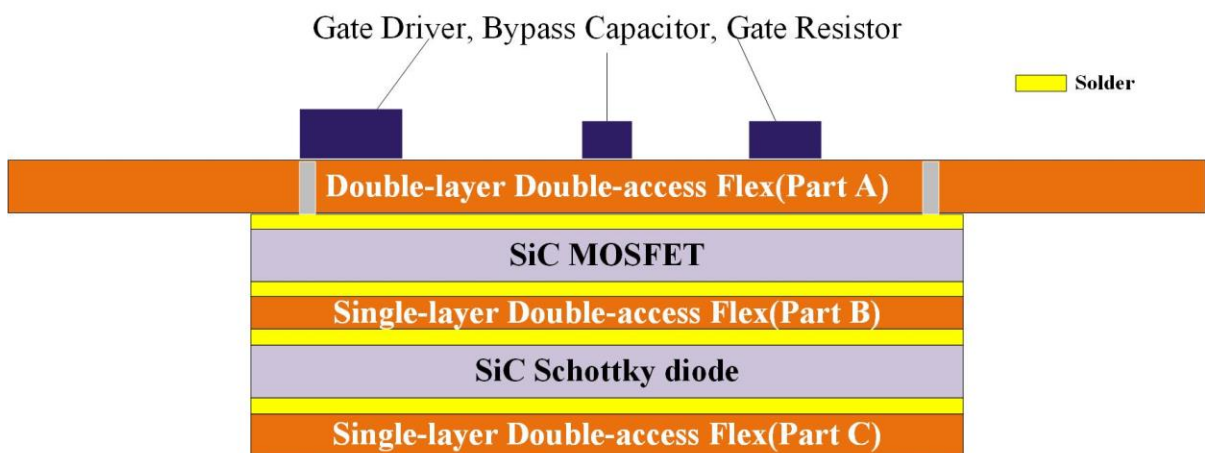


Figure 4-13 Finished flex module

Step5. Test circuit assembly

One more reflow process is needed in this step in order to solder the flex module onto the PCB mother board. Other loose components can be mounted manually. Figure 4-14 shows the finished system assembly.

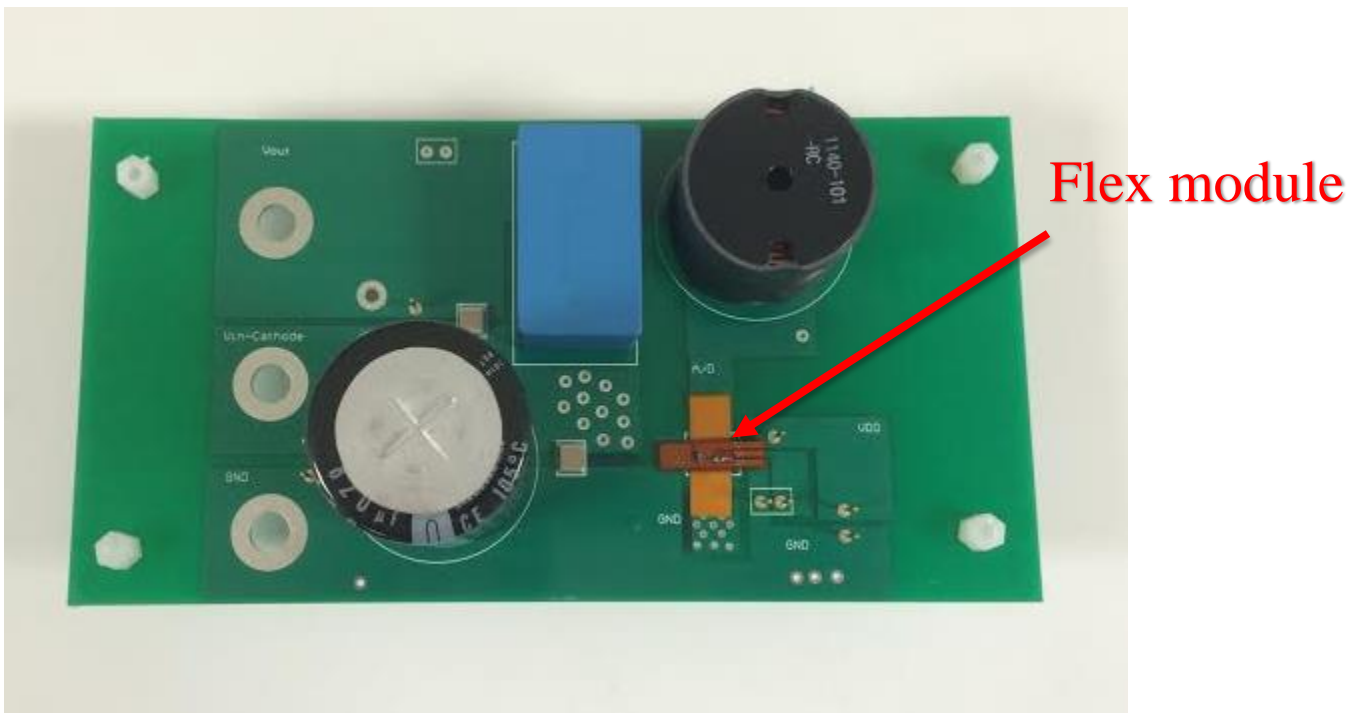


Figure 4-14 Finished system assembly

4.2 Electrical Characterization

Electrical characterization is conducted with a traditional wire-bonded power module due to unavailability solderable power devices. Figure 4-15 shows the testbench set up. Tektronix

AFG 3252 Dual Channel Arbitrary/Function Generator and DPO 2024B Digital Phosphor Oscilloscope were used to perform the test.

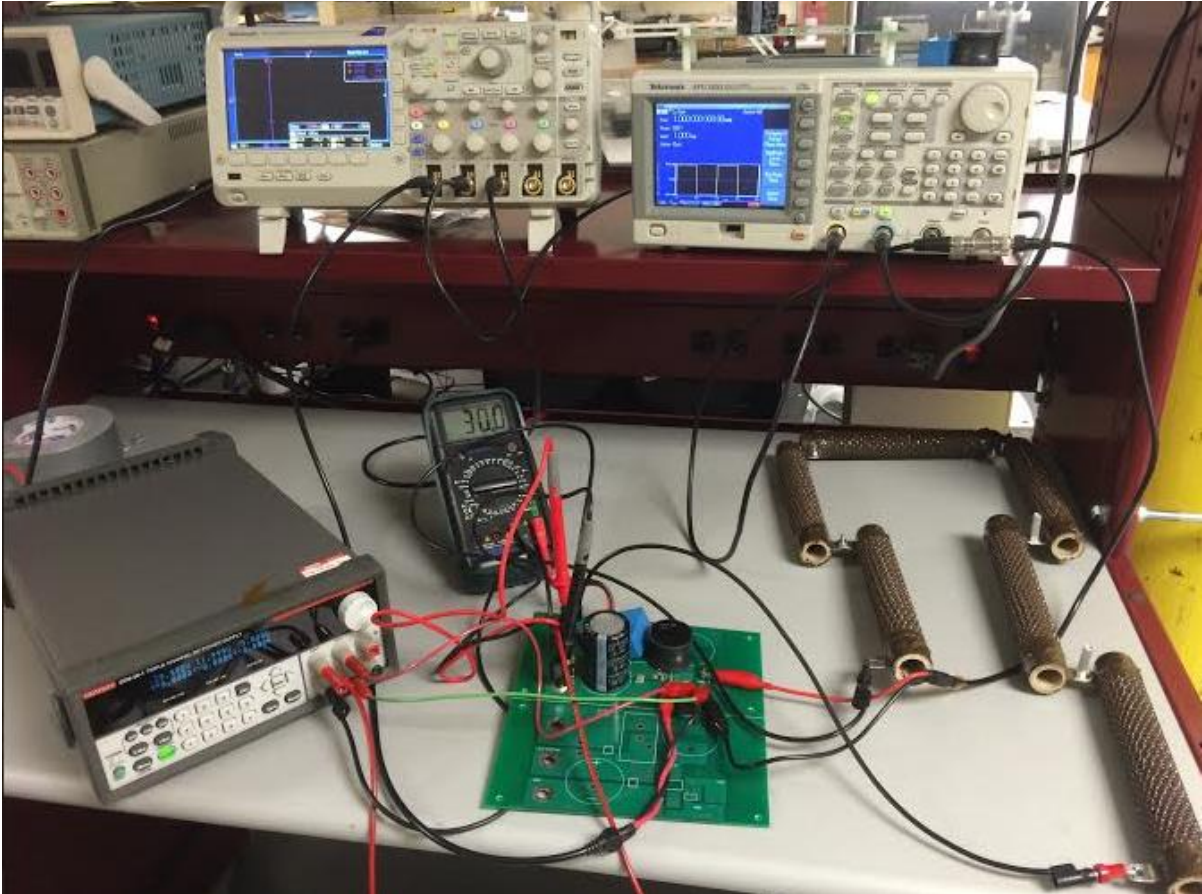


Figure 4-15 Test bench set up

DC power source is Keithley 2230-30-1 triple channel DC power source. Channel 1 and channel 2 are able to provide 0-30V and 0-15A DC power which are used to provide 30V DC input for the PCB board and 15V supply for gate drive chip respectively. A 400V test could not be performed since the high voltage power supply needed a substantial time to create a

safe set-up for the PCB board and module. It was decided to spend more time on pad metalization, since the thesis is to develop the design process.

Gate-source and drain-source voltages are probed and recorded as shown in Figure 4-16. This provides suitable verification that the testing approach could be followed in flex module design.

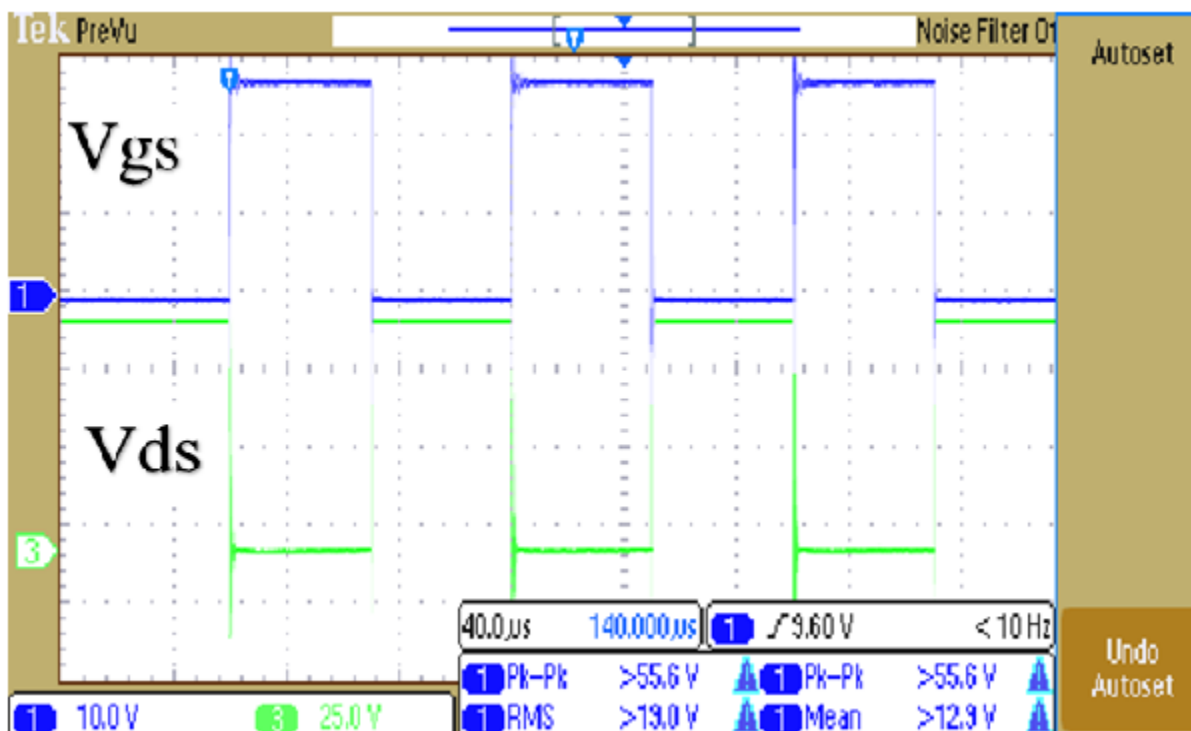


Figure 4-16 Vgs&Vds switching waveforms

CHAPTER 5 SUMMARY AND FUTURE WORKS

This research developed a fabrication process for novel 3D chip-on-chip power modules for the NCSU-PREES laboratory. First, the thesis introduces the background of power semiconductor modules, and reviews the past and current technologies of power packaging. Based on the past and current packaging technologies, the thesis proposes an idea of 3D chip-on-chip module using flex circuit substrate. The module have three potential advantages against other packaging approaches:

- Smaller footprint
- Shorter interconnect
- Higher power capacity

For future works, three other areas should be addressed when designing a chip-on-chip power module.

- Parasitic extraction: Ansoft®Q3D extractor would be a good choice to extract the parasitics of the circuit design. The parasitics can be quantified more accurately by software simulation than by theoretical calculation.
- PCB mother board layout: the PCB test board, though not the major work of the thesis, directly influences the module's performance electrically when testing it on the bench. The layout of the PCB still should be improved. For example, electrical vias which add inductance in the loop can be further reduced. These vias, add inductance at a few nano Henry, and can be harmful by slowing down the switching speed in high current and high frequency applications.

Other improvable issues include separating and shortening ground return of both power and signal loops, the approach to measure I_d and so on. These are very specific engineering efforts that require careful and patient considerations.

- Zincate treatment: Zincate treatment for aluminum pads on power devices should be investigated for surface metallization. The zincate process is the most widely used for plating onto aluminum. It basically adds a zinc layer on top of the aluminum and this zinc layer (or double zinc layers if needed) can improve the adhesion of the metal layers [22].

REFERENCES

- [1] Wang, Wei. "Power Module with Series-connected MOSFETs in Flip-chip Configuration." PhD diss., Virginia Polytechnic Institute and State University, 2010.
- [2] Sheng, William W., and Ronald P. Colino. Power electronic modules: design and manufacture. CRC press, 2004.
- [3] John H.Day. "Power Electronics Challenges for Hybrids", Auto Electronics, 2008.
- [4] Li, Shengnan. "Packaging Design of IGBT Power Module Using Novel Switching Cells." PhD diss., University of Tennessee, 2011.
- [5] Flexible electronics, Wikipedia, http://en.wikipedia.org/wiki/Flexible_electronics
- [6] Fjelstad, Joseph. An Engineer's Guide to Flexible Circuit Technology: Materials, Design, Applications, Manufacturing. Electrochemical Publications, 1997.
- [7] Lau, John H. Flip chip technologies. Vol. 1. New York: McGraw-Hill, 1996.
- [8] Shah, H. N., Y. Xiao, T. P. Chow, R. J. Gutmann, E. R. Olson, S-H. Park, W-K. Lee, J. J. Connors, T. M. Jahns, and R. D. Lorenz. "Power electronics modules for inverter applications using flip-chip on flex-circuit technology." 39th IAS Annual Meeting Conference Record, vol. 3, pp. 1526-1533. IEEE, 2004.
- [9] Bai, John G., Guo-Quan Lu, and Xingsheng Liu. "Flip-chip on flex integrated power electronics modules for high-density power integration." IEEE Transactions on Advanced Packaging, vol. 26, no. 1, pp54-59, 2003.
- [10] Thomas Graphoff. "SkiN technology for ultra compact power modules." Semikron, www.semikron.com, Sep.2012.

- [11] Matt Romig, Ozzie Lopez. "3D packaging advancements drive performance, power and density in power devices." Texas Instruments, www.ti.com, Jul.2011.
- [12] Haque, Shatil. "Processing and characterization of device solder interconnection and module attachment for power electronics modules." PhD diss., Virginia Polytechnic Institute and State University, 1999.
- [13] Cree, Inc. "Silicon Carbide Power MOSFET Z-FET MOSFET." CPM2-1200-0025B datasheet, 2013.
- [14] Cree, Inc. "Silicon Carbide Schottky Diode Chip." CPW5-1200-Z050B datasheet, 2013.
- [15] Fairchild Semiconductor international, Inc. "FAN3122C Die Attachment Diagram."
- [16] Fairchild Semiconductor international, Inc. "Single 9-A High-Speed, Low-Side Gate Driver." FAN3121/FAN3122 datasheet, 2013.
- [17] Jason Arrigo. "Input and Output Capacitor Selection." Texas Instruments, Application Report SLTA055, Feb.2006.
- [18] Quick-teck. "Tips for PCB Vias Design.", Internal Technical Note EN-00417.
- [19] Cree, Inc. "Cree C2M SiC MOSFET PSPICE MODEL.", Quick start guide, rev 1.8.
- [20] Braeckelmann, G., D. Manger, S. C. Seo, S. Beasor, S. Nijsten, and A. E. Kaloyeros. "Deposition of barrier layer and CVD copper under no exposed wafer conditions: adhesion performance and process integration." In Materials for Advanced Metallization, 1997. MAM'97 Abstracts Booklet., European Workshop, pp. 27-29. IEEE, 1997.
- [21] Bai, Guofeng. "Low-temperature sintering of nanoscale silver paste for semiconductor device interconnection." PhD diss., Virginia Polytechnic Institute and State University, 2005.

[22] Jiang, Li. "Thermo-mechanical reliability of sintered-silver joint versus lead-free solder for attaching large-area devices." PhD diss., Virginia Polytechnic Institute and State University, 2010.

APPENDICES

5.1 Appendix A CPM2-1200-0025B SiC MOSFET Datasheet



CPM2-1200-0025B

Silicon Carbide Power MOSFET
C2M™ MOSFET Technology
N-Channel Enhancement Mode

V_{DS}	1200 V
$I_D @ 25^\circ\text{C}$	90 A
$R_{DS(on)}$	25 m Ω

Features

- New C2M SiC MOSFET technology
- High Blocking Voltage with Low On-Resistance
- High Speed Switching with Low Capacitances
- Easy to Parallel and Simple to Drive
- Avalanche Ruggedness
- Resistant to Latch-Up
- Halogen Free, RoHS Compliant

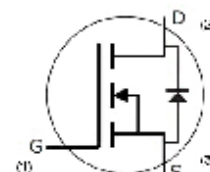
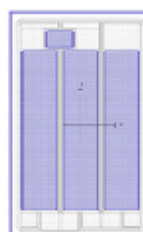
Benefits

- Higher System Efficiency
- Reduced Cooling Requirements
- Increased Power Density
- Increased System Switching Frequency

Applications

- Solar Inverters
- Switch Mode Power Supplies
- High Voltage DC/DC converters
- Battery Chargers
- Motor Drive
- Pulsed Power Applications

Chip Outline



Part Number	Die Size (mm)
CPM2-1200-0025B	4.04 x 6.44

Maximum Ratings ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{DSmax}	Drain - Source Voltage	1200	V	$V_{GS} = 0\text{ V}, I_D = 100\ \mu\text{A}$	
V_{GSmax}	Gate - Source Voltage	-10/+25	V	Absolute maximum values	
V_{GSop}	Gate - Source Voltage	-5/+20	V	Recommended operational values	
I_D	Continuous Drain Current	90	A	$V_{GS} = 20\text{ V}, T_C = 25^\circ\text{C}$	Note 1
		60		$V_{GS} = 20\text{ V}, T_C = 100^\circ\text{C}$	
$I_{D(pulse)}$	Pulsed Drain Current	250	A	Pulse width t_p limited by T_{Jmax}	
T_J, T_{stg}	Operating Junction and Storage Temperature	-55 to +150	$^\circ\text{C}$		
T_L	Solder Temperature	260	$^\circ\text{C}$	1.6mm (0.063") from case for 10s	
T_{Proc}	Maximum Processing Temperature	325	$^\circ\text{C}$	10 min. maximum	

Note (1): Assumes a $R_{\theta jc} < 0.27\text{ K/W}$


Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1200			V	$V_{GS} = 0\text{ V}, I_D = 100\ \mu\text{A}$	
$V_{GS(th)}$	Gate Threshold Voltage	2.4	3.0		V	$V_{DS} = 10\text{ V}, I_D = 12.5\text{mA}$	Fig. 11
		1.8	2.0		V	$V_{DS} = 10\text{ V}, I_D = 12.5\text{mA}, T_J = 150^\circ\text{C}$	
I_{DSS}	Zero Gate Voltage Drain Current		2	100	μA	$V_{DS} = 1200\text{ V}, V_{GS} = 0\text{ V}$	
I_{GSS}	Gate-Source Leakage Current			600	nA	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	
$R_{DS(on)}$	Drain-Source On-State Resistance		25	34	m Ω	$V_{GS} = 20\text{ V}, I_D = 50\text{ A}$	Fig. 4,5,6
			43			$V_{GS} = 20\text{ V}, I_D = 50\text{ A}, T_J = 150^\circ\text{C}$	
g_{fs}	Transconductance		23.6		S	$V_{DS} = 20\text{ V}, I_{DS} = 50\text{ A}$	Fig. 7
			21.7			$V_{DS} = 20\text{ V}, I_{DS} = 50\text{ A}, T_J = 150^\circ\text{C}$	
C_{iss}	Input Capacitance		2788		pF	$V_{GS} = 0\text{ V}$	Fig. 17,18
C_{oss}	Output Capacitance		220			$V_{DS} = 1000\text{ V}$	
C_{riss}	Reverse Transfer Capacitance		15			$f = 1\text{ MHz}$	
E_{oss}	C_{oss} Stored Energy		121			$V_{AC} = 25\text{ mV}$	
E_{AS}	Avalanche Energy, Single Pluse		3.5		J	$I_D = 50\text{ A}, V_{DS} = 50\text{ V}$	
E_{ON}	Turn-On Switching Energy		1.4		mJ	$V_{DS} = 800\text{ V}, V_{GS} = -5/20\text{ V},$ $I_D = 50\text{ A}, R_{Q(EXT)} = 2.5\ \Omega, L = 412\ \mu\text{H}$	
E_{OFF}	Turn Off Switching Energy		0.3				
$t_{d(on)}$	Turn-On Delay Time		14		ns	$V_{DS} = 800\text{ V}, V_{GS} = -5/20\text{ V}$ $I_D = 50\text{ A},$ $R_{Q(EXT)} = 2.5\ \Omega, R_L = 16\ \Omega$ Timing relative to V_{DS} Per IEC60747-8-4 pg 83	
t_r	Rise Time		32				
$t_{d(off)}$	Turn-Off Delay Time		29				
t_f	Fall Time		28				
$R_{Q(EXT)}$	Internal Gate Resistance		1.1				
Q_{gs}	Gate to Source Charge		46		nC	$V_{DS} = 800\text{ V}, V_{GS} = -5/20\text{ V}$ $I_D = 50\text{ A}$ Per IEC60747-8-4 pg 83	Fig. 12
Q_{gd}	Gate to Drain Charge		50				
Q_g	Total Gate Charge		161				

Reverse Diode Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	3.3		V	$V_{GS} = -5\text{ V}, I_{SD} = 25\text{ A}$	Fig. 8, 9, 10
		3.1		V	$V_{GS} = -5\text{ V}, I_{SD} = 25\text{ A}, T_J = 150^\circ\text{C}$	
I_S	Continuous Diode Forward Current		90		$T_C = 25^\circ\text{C}$	Note 2
t_{rr}	Reverse Recovery Time	45		ns	$V_{GS} = -5\text{ V}, I_{SD} = 50\text{ A}, T_J = 25^\circ\text{C}$ $VR = 800\text{ V}$ $di/dt = 1000\text{ A}/\mu\text{s}$	Note 2
Q_{rr}	Reverse Recovery Charge	406		nC		
I_{rrm}	Peak Reverse Recovery Current	13.5		A		

Note (2): When using SiC Body Diode the maximum recommended $V_{GS} = -5\text{V}$

Note (3): For inductive and resistive switching data and waveforms please refer to datasheet for packaged device.
Part number C2M0025120D.



Typical Performance

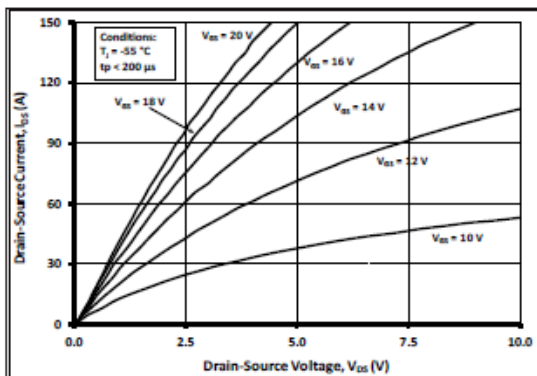


Figure 1. Output Characteristics $T_j = -55\text{ }^\circ\text{C}$

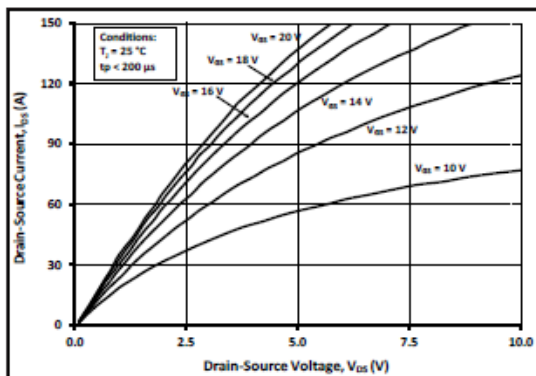


Figure 2. Output Characteristics $T_j = 25\text{ }^\circ\text{C}$

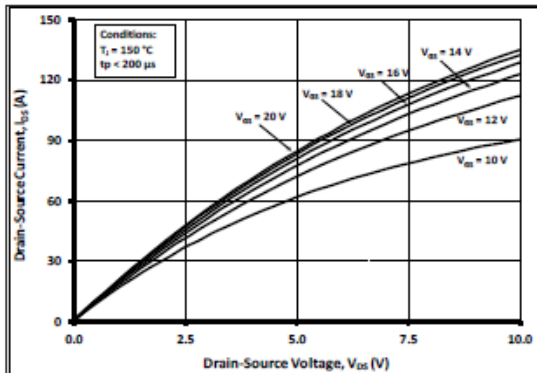


Figure 3. Output Characteristics $T_j = 150\text{ }^\circ\text{C}$

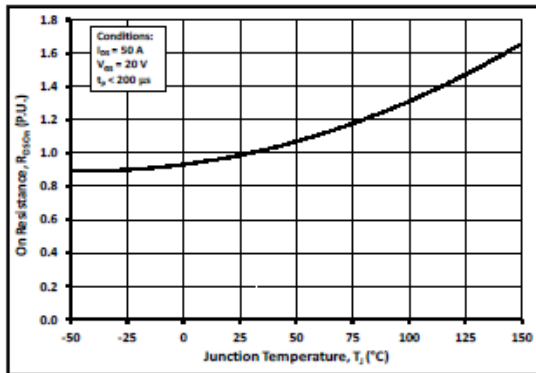


Figure 4. Normalized On-Resistance vs. Temperature

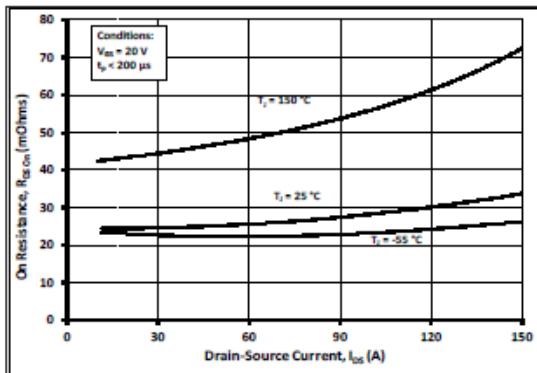


Figure 5. On-Resistance vs. Drain Current For Various Temperatures

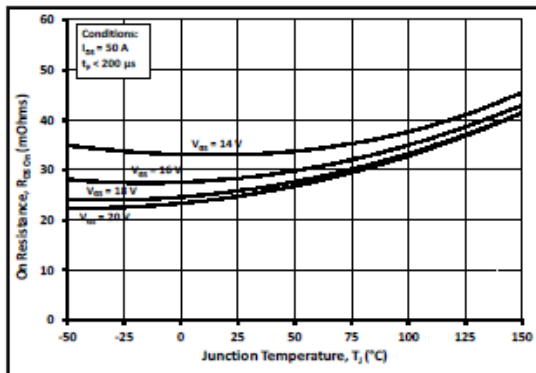


Figure 6. On-Resistance vs. Temperature For Various Gate Voltage



Typical Performance

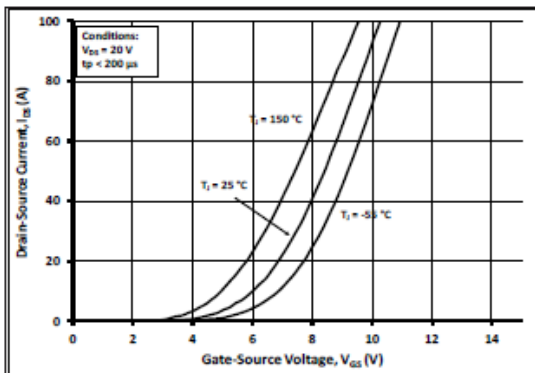


Figure 7. Transfer Characteristic For Various Junction Temperatures

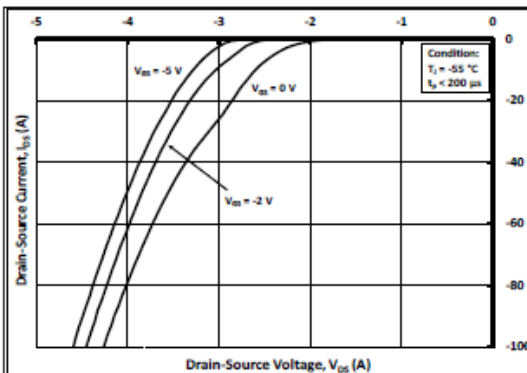


Figure 8. Body Diode Characteristic at -55 °C

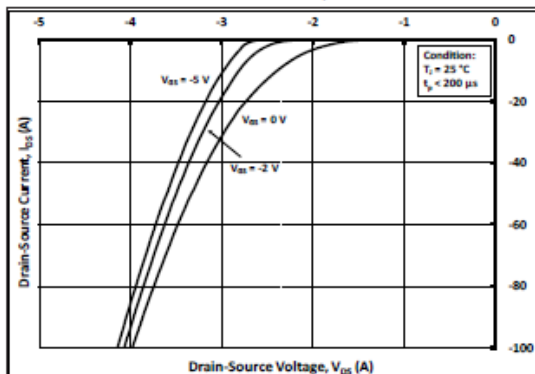


Figure 9. Body Diode Characteristic at 25 °C

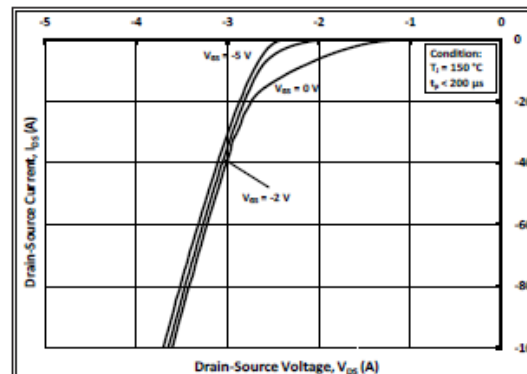


Figure 10. Body Diode Characteristic at 150 °C

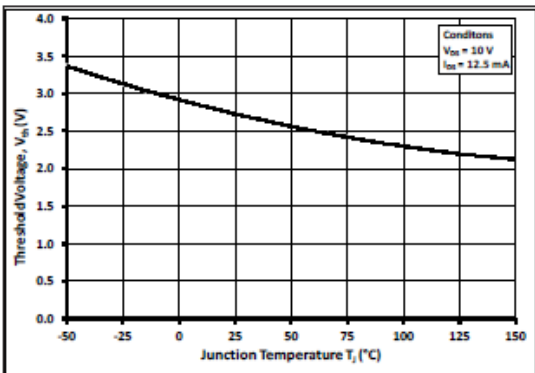


Figure 11. Threshold Voltage vs. Temperature

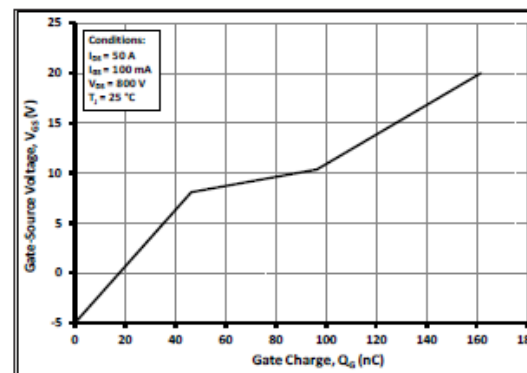


Figure 12. Gate Charge Characteristic



Typical Performance

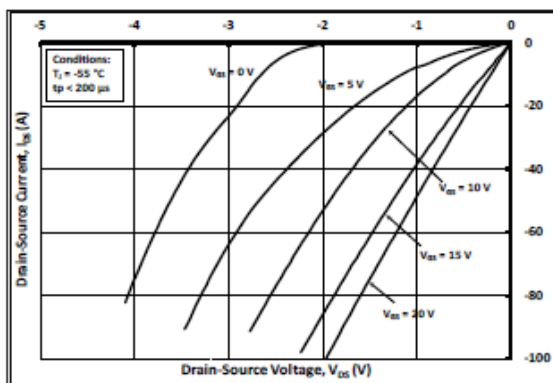


Figure 13. 3rd Quadrant Characteristic at -55 °C

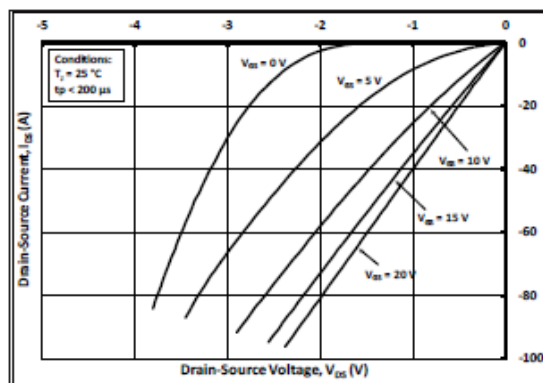


Figure 14. 3rd Quadrant Characteristic at 25 °C

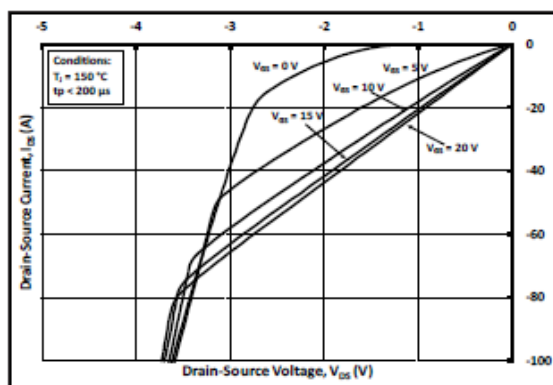


Figure 15. 3rd Quadrant Characteristic at 150 °C

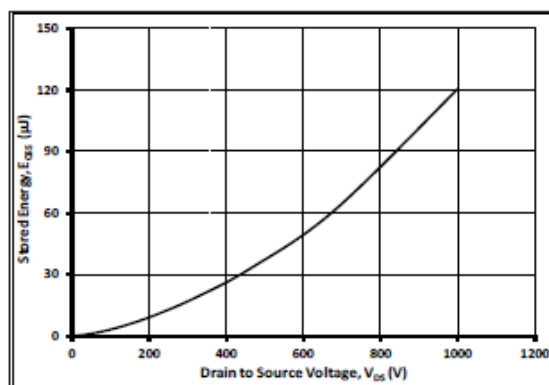


Figure 16. Output Capacitor Stored Energy

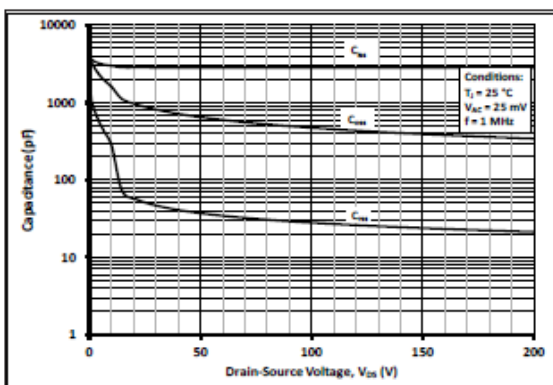


Figure 17. Capacitances vs. Drain-Source Voltage (0-200 V)

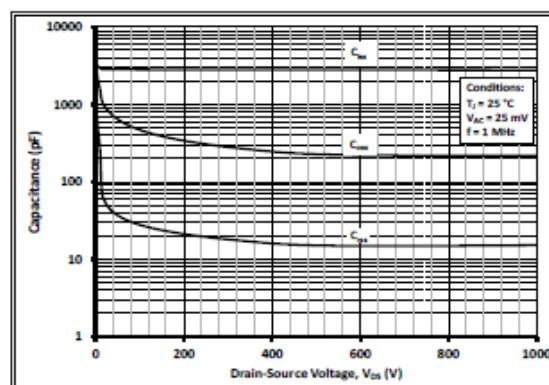


Figure 18. Capacitances vs. Drain-Source Voltage (0-1000 V)



Notes

- RoHS Compliance**
 The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS2), as implemented January 2, 2013. RoHS Declarations for this product can be obtained from your Cree representative or from the Product Documentation sections of www.cree.com.
- REACH Compliance**
 REACH substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, please contact a Cree representative to insure you get the most up-to-date REACH SVHC Declaration. REACH banned substance information (REACH Article 67) is also available upon request.
- This product has not been designed or tested for use in, and is not intended for use in, applications implanted into the human body nor in applications in which failure of the product could lead to death, personal injury or property damage, including but not limited to equipment used in the operation of nuclear facilities, life-support machines, cardiac defibrillators or similar emergency medical equipment, aircraft navigation or communication or control systems, air traffic control systems.

Related Links

- C2M PSpice Models:** www.cree.com/power
- SiC MOSFET Isolated Gate Driver reference design:** www.cree.com/power
- Application Considerations for Silicon-Carbide MOSFETs:** www.cree.com/power

Copyright © 2014 Cree, Inc. All rights reserved.
 The information in this document is subject to change without notice.
 Cree, the Cree logo, and Zero Recovery are registered trademarks of Cree, Inc.

Cree, Inc.
 4600 Silicon Drive
 Durham, NC 27703
 USA Tel: +1.919.313.5300
 Fax: +1.919.313.5451
www.cree.com/power

5.2 Appendix B CPW5-1200-Z050B SiC Diode Datasheet



CPW5-1200-Z050B
Silicon Carbide Schottky Diode Chip
Z-REC[®] RECTIFIER

V_{RRM}	= 1200 V
I_F	= 50 A
Q_c	= 246 nC

Features

- 1200-Volt Schottky Rectifier
- Zero Reverse Recovery
- Zero Forward Recovery
- High-Frequency Operation
- Temperature-Independent Switching Behavior
- Extremely Fast Switching
- Positive Temperature Coefficient on V_f

Chip Outline



Part Number	Die Size	Anode	Cathode
CPW5-1200-Z050B	4.9 x 4.9 mm ²	Al	Ni/Ag

Maximum Ratings

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{RRM}	Repetitive Peak Reverse Voltage	1200	V		
V_{RSM}	Surge Peak Reverse Voltage	1200	V		
V_R	DC Peak Blocking Voltage	1300	V		
I_F	Continuous Forward Current	50	A	$T_J=175^{\circ}\text{C}$	1
T_J, T_{stg}	Operating Junction and Storage Temperature	-55 to +175	$^{\circ}\text{C}$		
T_{PDC}	Maximum Processing Temperature	325	$^{\circ}\text{C}$	10 min Maximum	

Note:

1. Assumes $R_{\theta JC}$ Thermal Resistance < 0.25 $^{\circ}\text{C}/\text{W}$ and $T_C = 145^{\circ}\text{C}$



Electrical Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_f	DC Forward Voltage	1.6	1.8	V	$I_f = 50 \text{ A}$ $T_j = 25^\circ\text{C}$	Fig 1
		1.25			$I_f = 25 \text{ A}$ $T_j = 25^\circ\text{C}$	
		2.25	2.7		$I_f = 50 \text{ A}$ $T_j = 175^\circ\text{C}$	
		1.55			$I_f = 25 \text{ A}$ $T_j = 175^\circ\text{C}$	
I_r	Reverse Current	100	500	μA	$V_R = 1200 \text{ V}$ $T_j = 25^\circ\text{C}$	Fig 2
		6			$V_R = 800 \text{ V}$ $T_j = 25^\circ\text{C}$	
		300	1000		$V_R = 1200 \text{ V}$ $T_j = 175^\circ\text{C}$	
		40			$V_R = 800 \text{ V}$ $T_j = 175^\circ\text{C}$	
Q_C	Total Capacitive Charge	246		nC	$V_R = 800 \text{ V}$, $T_j = 25^\circ\text{C}$	Fig 4
C	Total Capacitance	3380		pF	$V_R = 0 \text{ V}$, $T_j = 25^\circ\text{C}$, $f = 1 \text{ MHz}$	Fig 3
		230			$V_R = 400 \text{ V}$, $T_j = 25^\circ\text{C}$, $f = 1 \text{ MHz}$	
		173			$V_R = 800 \text{ V}$, $T_j = 25^\circ\text{C}$, $f = 1 \text{ MHz}$	

Mechanical Parameters

Parameter	Typ.	Unit
Die Size	4.9 x 4.9	mm
Anode Pad opening	3.8 x 3.8	mm
Thickness	380 ± 10%	μm
Wafer Size	100	mm
Anode Metalization (Al)	4	μm
Cathode Metalization (Ni/Ag)	1.8	μm
Frontside Passivation	Polyimide	



Typical Performance

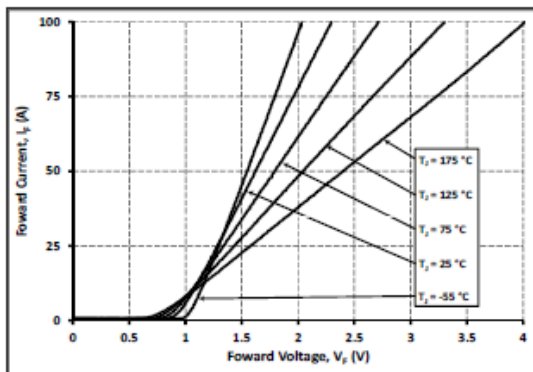


Figure 1. Typical Forward Characteristics

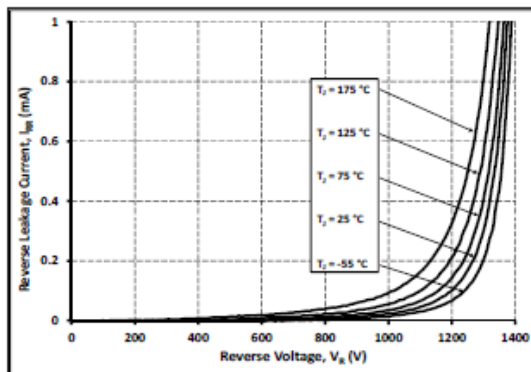


Figure 2. Typical Reverse Characteristics

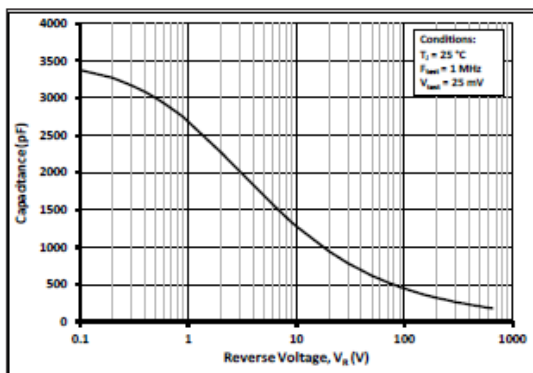


Figure 3. Typical Capacitance vs. Reverse Voltage

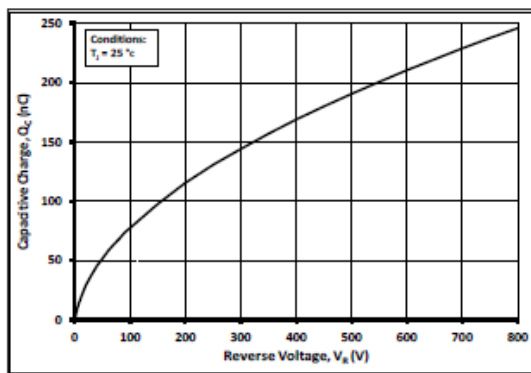
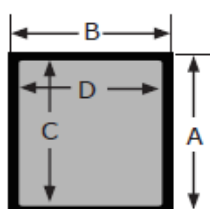


Figure 4. Typical Recovery Charge vs. Reverse Voltage



Chip Dimensions



symbol	dimension	
	mm	inch
A	4.9	0.193
B	4.9	0.193
C	3.8	0.150
D	3.8	0.150

Notes

- RoHS Compliance**
 The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS2), as implemented January 2, 2013. RoHS Declarations for this product can be obtained from your Cree representative or from the Product Documentation sections of www.cree.com.
- REACH Compliance**
 REACH substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, please contact a Cree representative to insure you get the most up-to-date REACH SVHC Declaration. REACH banned substance information (REACH Article 67) is also available upon request.
- This product has not been designed or tested for use in, and is not intended for use in, applications implanted into the human body nor in applications in which failure of the product could lead to death, personal injury or property damage, including but not limited to equipment used in the operation of nuclear facilities, life-support machines, cardiac defibrillators or similar emergency medical equipment, aircraft navigation or communication or control systems, or air traffic control systems.

Copyright © 2014 Cree, Inc. All rights reserved.
 The information in this document is subject to change without notice.
 Cree, the Cree logo, and Zero Recovery are registered trademarks of Cree, Inc.

Cree, Inc.
 4600 Silicon Drive
 Durham, NC 27703
 USA Tel: +1.919.313.5300
 Fax: +1.919.313.5451
www.cree.com/power

5.3 Appendix C FAN3122C Gate Driver Datasheet



FAN3121 / FAN3122

Single 9-A High-Speed, Low-Side Gate Driver

Features

- Industry-Standard Pin-out with Enable Input
- 4.5-V to 18-V Operating Range
- 11.4 A Peak Sink at $V_{DD} = 12\text{ V}$
- 9.7-A Sink / 7.1-A Source at $V_{OUT} = 6\text{ V}$
- Inverting Configuration (FAN3121) and Non-Inverting Configuration (FAN3122)
- Internal Resistors Turn Driver Off If No Inputs
- 23-ns / 19-ns Typical Rise/Fall Times (10 nF Load)
- 18 ns to 23 ns Typical Propagation Delay Time
- Choice of TTL or CMOS Input Thresholds
- MillerDrive™ Technology
- Available in Thermally Enhanced 3x3 mm 8-Lead MLP or 8-Lead SOIC Package (Pb-Free Finish)
- Rated from -40°C to $+125^{\circ}\text{C}$
- Automotive Qualified to AEC-Q100 (F085 Versions)

Applications

- Synchronous Rectifier Circuits
- High-Efficiency MOSFET Switching
- Switch-Mode Power Supplies
- DC-to-DC Converters
- Motor Control
- Automotive-Qualified Systems (F085 Versions)

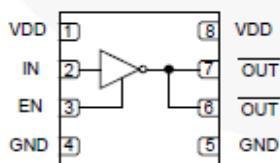


Figure 1. FAN3121 Pin Configuration

Description

The FAN3121 and FAN3122 MOSFET drivers are designed to drive N-channel enhancement MOSFETs in low-side switching applications by providing high peak current pulses. The drivers are available with either TTL input thresholds (FAN312xT) or V_{DD} -proportional CMOS input thresholds (FAN312xC). Internal circuitry provides an under-voltage lockout function by holding the output low until the supply voltage is within the operating range.

FAN312x drivers incorporate the MillerDrive™ architecture for the final output stage. This bipolar / MOSFET combination provides the highest peak current during the Miller plateau stage of the MOSFET turn-on / turn-off process.

The FAN3121 and FAN3122 drivers implement an enable function on pin 3 (EN), previously unused in the industry-standard pin-out. The pin is internally pulled up to V_{DD} for active HIGH logic and can be left open for standard operation.

The commercial FAN3121/22 is available in a 3x3 mm 8-lead thermally-enhanced MLP package or an 8-lead SOIC package. The AEC-Q100 automotive-qualified versions are available in the 8-lead SOIC package.

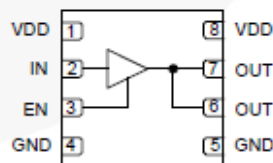


Figure 2. FAN3122 Pin Configuration

Ordering Information

Part Number	Logic	Input Threshold	Package	Packing Method	Quantity per Reel
FAN3121CMPX	Inverting Channels + Enable	CMOS	3x3 mm MLP-8	Tape & Reel	3,000
FAN3121CMX			SOIC-8	Tape & Reel	2,500
FAN3121CMX_F085 ⁽¹⁾			SOIC-8	Tape & Reel	2,500
FAN3121TMPX		TTL	3x3 mm MLP-8	Tape & Reel	3,000
FAN3121TMX			SOIC-8	Tape & Reel	2,500
FAN3121TMX_F085 ⁽¹⁾			SOIC-8	Tape & Reel	2,500
FAN3122CMPX	Non-Inverting Channels + Enable	CMOS	3x3 mm MLP-8	Tape & Reel	3,000
FAN3122CMX			SOIC-8	Tape & Reel	2,500
FAN3122CMX_F085 ⁽¹⁾			SOIC-8	Tape & Reel	2,500
FAN3122TMPX		TTL	3x3 mm MLP-8	Tape & Reel	3,000
FAN3122TMX			SOIC-8	Tape & Reel	2,500
FAN3122TMX_F085 ⁽¹⁾			SOIC-8	Tape & Reel	2,500

For additional information on Fairchild's Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html

Note:

1. Qualified to AEC-Q100.

Package Outlines

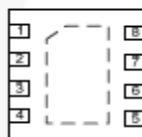


Figure 3. 3x3 mm MLP-8 (Top View)

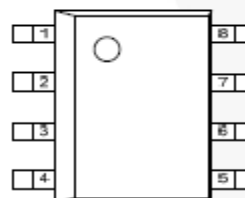


Figure 4. SOIC-8 (Top View)

Thermal Characteristics⁽²⁾

Package	θ_{JL} ⁽³⁾	θ_{JT} ⁽⁴⁾	θ_{JA} ⁽⁶⁾	Ψ_{JB} ⁽⁶⁾	Ψ_{JT} ⁽⁷⁾	Units
8-Lead 3x3 mm Molded Leadless Package (MLP)	1.2	64	42	2.8	0.7	°C/W
8-Pin Small Outline Integrated Circuit (SOIC)	38	29	87	41	2.3	°C/W

Notes:

2. Estimates derived from thermal simulation; actual values depend on the application.
3. θ_{JL} (θ_{JL}): Thermal resistance between the semiconductor junction and the bottom surface of all the leads (including any thermal pad) that are typically soldered to a PCB.
4. θ_{JT} (θ_{JT}): Thermal resistance between the semiconductor junction and the top surface of the package, assuming it is held at a uniform temperature by a top-side heatsink.
5. θ_{JA} (θ_{JA}): Thermal resistance between junction and ambient, dependent on the PCB design, heat sinking, and airflow. The value given is for natural convection with no heatsink, as specified in JEDEC standards JESD51-2, JESD51-5, and JESD51-7, as appropriate.
6. Ψ_{JB} (Ψ_{JB}): Thermal characterization parameter providing correlation between semiconductor junction temperature and an application circuit board reference point for the thermal environment defined in Note 5. For the MLP-8 package, the board reference is defined as the PCB copper connected to the thermal pad and protruding from either end of the package. For the SOIC-8 package, the board reference is defined as the PCB copper adjacent to pin 6.
7. Ψ_{JT} (Ψ_{JT}): Thermal characterization parameter providing correlation between the semiconductor junction temperature and the center of the top of the package for the thermal environment defined in Note 5.

Pin Definitions

FAN3121	FAN3122	Name	Description
3	3	EN	Enable Input. Pull pin LOW to inhibit driver. EN has logic thresholds for both TTL and CMOS IN thresholds.
4, 5	4, 5	GND	Ground. Common ground reference for input and output circuits.
2	2	IN	Input.
	6, 7	OUT	Gate Drive Output. Held LOW unless required input is present and V_{DD} is above the UVLO threshold.
6, 7		$\overline{\text{OUT}}$	Gate Drive Output (inverted from the input). Held LOW unless required input is present and V_{DD} is above the UVLO threshold.
1, 8	1, 8	V_{DD}	Supply Voltage. Provides power to the IC.
		P1	Thermal Pad (MLP only). Exposed metal on the bottom of the package; may be left floating or connected to GND; NOT suitable for carrying current.

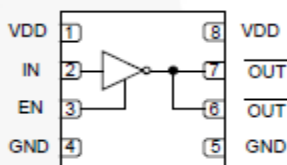


Figure 5. FAN3121 Pin Assignments (Repeated)

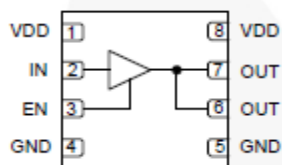


Figure 6. FAN3122 Pin Assignments (Repeated)

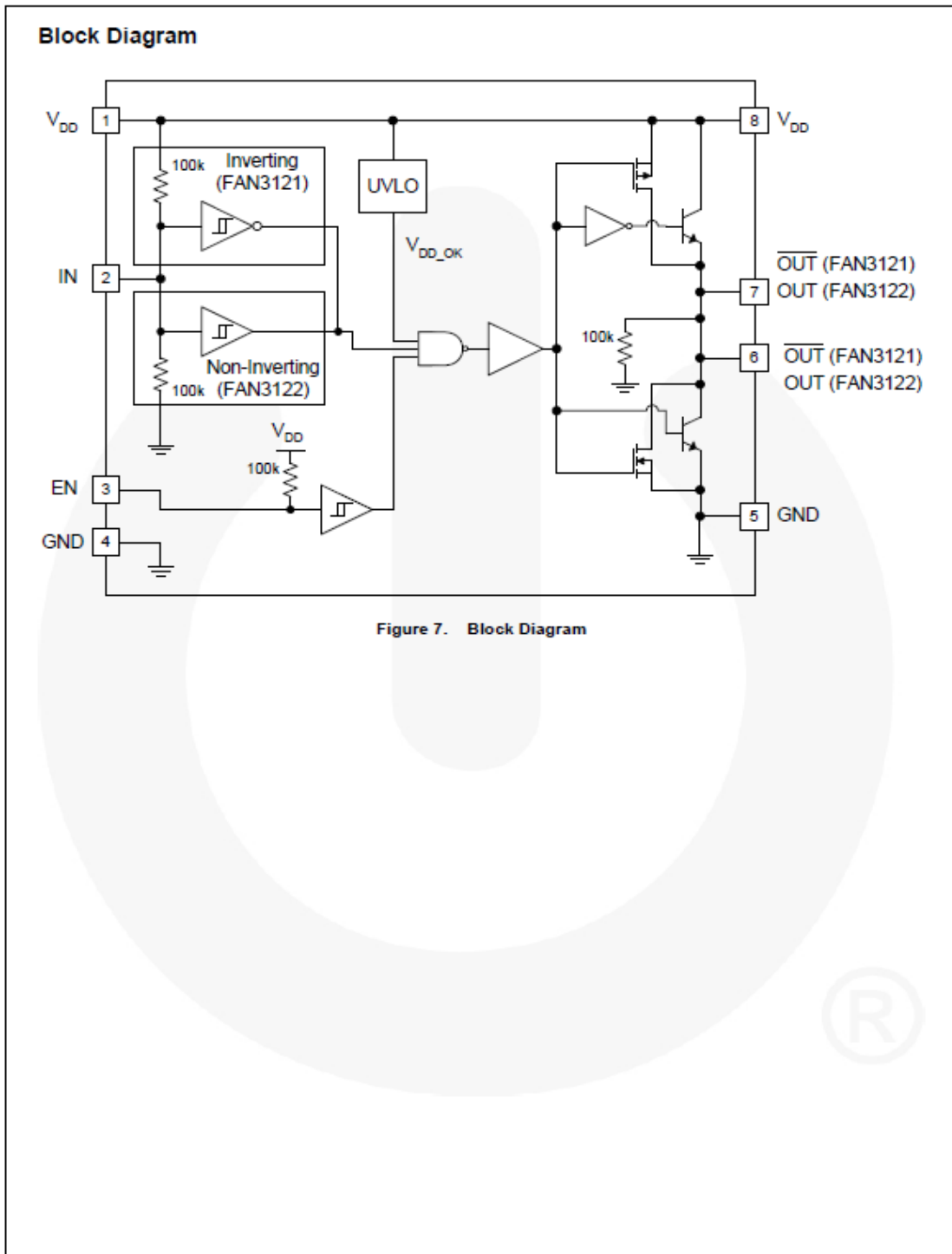
Output Logic

FAN3121		
EN	IN	$\overline{\text{OUT}}$
0	0	0
0	1 ⁽⁸⁾	0
1 ⁽⁸⁾	0	1
1 ⁽⁸⁾	1 ⁽⁸⁾	0

FAN3122		
EN	IN	OUT
0	0 ⁽⁸⁾	0
0	1	0
1 ⁽⁸⁾	0 ⁽⁸⁾	0
1 ⁽⁸⁾	1	1

Note:

8. Default input signal if no external connection is made.



Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	V_{DD} to GND	-0.3	20.0	V
V_{EN}	EN to GND	GND - 0.3	$V_{DD} + 0.3$	V
V_{IN}	IN to GND	GND - 0.3	$V_{DD} + 0.3$	V
V_{OUT}	OUT to GND	GND - 0.3	$V_{DD} + 0.3$	V
T_L	Lead Soldering Temperature (10 Seconds)		+260	°C
T_J	Junction Temperature	-55	+150	°C
T_{STG}	Storage Temperature	-85	+150	°C

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply Voltage Range	4.5	18.0	V
V_{EN}	Enable Voltage EN	0	V_{DD}	V
V_{IN}	Input Voltage IN	0	V_{DD}	V
T_A	Operating Ambient Temperature	-40	+125	°C

Electrical Characteristics

Unless otherwise noted, $V_{DD}=12\text{ V}$ and $T_J=-40^\circ\text{C}$ to $+125^\circ\text{C}$. Currents are defined as positive into the device and negative out of the device.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply						
V_{DD}	Operating Range		4.5		18.0	V
I_{DD}	Supply Current, Inputs / EN Not Connected	TTL		0.65	0.90	mA
		CMOS ⁽⁹⁾		0.58	0.85	
V_{ON}	Device Turn-On Voltage (UVLO)		3.5	4.0	4.3	V
V_{OFF}	Device Turn-Off Voltage (UVLO)		3.30	3.75	4.10	V
FAN3121_F085, FAN3122_F085 (Automotive-Qualified Versions)						
V_{DD}	Operating Range		4.5		18.0	V
I_{DD}	Supply Current, Inputs / EN Not Connected	TTL		0.65	1.00	mA
		CMOS ⁽⁹⁾		0.58	0.85	
V_{ON}	Device Turn-On Voltage (UVLO)		3.5	4.0	4.3	V
V_{OFF}	Device Turn-Off Voltage (UVLO) ⁽¹³⁾		3.25	3.75	4.15	V
Inputs (TTL, FAN312xT)⁽¹⁰⁾						
$V_{IL,T}$	INx Logic Low Threshold		0.8	1.0		V
$V_{IH,T}$	INx Logic High Threshold			1.7	2.0	V
$V_{HYS,T}$	TTL Logic Hysteresis Voltage		0.40	0.70	0.85	V
FAN3121TMX, FAN3122TMX						
I_{IN+}	Non-Inverting Input Current	IN from 0 to V_{DD}	-1		175	μA
I_{IN-}	Inverting Input Current	IN from 0 to V_{DD}	-175		1	μA
FAN3121TMX_F085, FAN3122TMX_F085 (Automotive-Qualified Versions)						
$I_{INL,T}$	Non-inverting Input Current ⁽¹³⁾	IN=0 V	-1.5		1.5	μA
$I_{INL,T}$	Non-inverting Input Current ⁽¹³⁾	IN= V_{DD}	90	120	175	μA
$I_{INL,T}$	Inverting Input Current ⁽¹³⁾	IN=0 V	-175	-120	-90	μA
$I_{INL,T}$	Inverting Input Current ⁽¹³⁾	IN= V_{DD}	-1.5		1.5	μA
Inputs (CMOS, FAN312xC)⁽¹⁰⁾						
$V_{IL,C}$	INx Logic Low Threshold		30	38		% V_{DD}
$V_{IH,C}$	INx Logic High Threshold			55	70	% V_{DD}
$V_{HYS,C}$	CMOS Logic Hysteresis Voltage		12	17	24	% V_{DD}
FAN3121CMX, FAN3122CMX						
I_{IN+}	Non-Inverting Input Current	IN from 0 to V_{DD}	-1		175	μA
I_{IN-}	Inverting Input Current	IN from 0 to V_{DD}	-175		1	μA
FAN3121CMX_F085, FAN3122CMX_F085 (Automotive-Qualified Versions)						
$I_{INL,C}$	Non-Inverting Input Current ⁽¹³⁾	IN=0 V	-1.5		1.5	μA
$I_{INL,C}$	Non-Inverting Input Current ⁽¹³⁾	IN= V_{DD}	90	120	175	μA
$I_{INL,C}$	Inverting Input Current ⁽¹³⁾	IN=0 V	-175	-120	-90	μA
$I_{INL,C}$	Inverting Input Current ⁽¹³⁾	IN= V_{DD}	-1.5		1.5	μA

Continued on the following page...

Electrical Characteristics (Continued)

Unless otherwise noted, $V_{DD}=12\text{ V}$ and $T_J=-40^\circ\text{C}$ to $+125^\circ\text{C}$. Currents are defined as positive into the device and negative out of the device.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
ENABLE (FAN3121, FAN3122)						
V_{ENL}	Enable Logic Low Threshold	EN from 5 V to 0 V	1.2	1.6	2.0	V
V_{ENH}	Enable Logic High Threshold	EN from 0 V to 5 V	1.8	2.2	2.6	V
V_{HYS_T}	TTL Logic Hysteresis Voltage		0.2	0.6	0.8	V
R_{PU}	Enable Pull-up Resistance		68	100	134	k Ω
t_{D1}, t_{D2}	Propagation Delay, CMOS EN ⁽¹¹⁾		8	17	27	ns
t_{D1}, t_{D2}	Propagation Delay, TTL EN ⁽¹¹⁾		14	21	33	ns
ENABLE (FAN3121_F085, FAN3122_F085) (Automotive-Qualified Versions)						
V_{ENL}	Enable Logic Low Threshold	EN from 5 V to 0 V	1.2	1.6	2.0	V
V_{ENH}	Enable Logic High Threshold	EN from 0 V to 5 V	1.8	2.2	2.6	V
V_{HYS_T}	TTL Logic Hysteresis Voltage		0.20	0.60	0.85	V
R_{PU}	Enable Pull-up Resistance		68	100	134	k Ω
t_{D1}, t_{D2}	Propagation Delay, CMOS EN ⁽¹¹⁾		6	17	35	ns
t_{D1}, t_{D2}	Propagation Delay, TTL EN ⁽¹¹⁾		8	22	34	ns
Outputs						
I_{SINK}	OUT Current, Mid-Voltage, Sinking ⁽¹²⁾	OUT at $V_{DD}/2$, $C_{LOAD}=1.0\ \mu\text{F}$, $f=1\ \text{kHz}$		9.7		A
I_{SOURCE}	OUT Current, Mid-Voltage, Sourcing ⁽¹²⁾	OUT at $V_{DD}/2$, $C_{LOAD}=1.0\ \mu\text{F}$, $f=1\ \text{kHz}$		7.1		A
I_{PK_SINK}	OUT Current, Peak, Sinking ⁽¹²⁾	$C_{LOAD}=1.0\ \mu\text{F}$, $f=1\ \text{kHz}$		11.4		A
I_{PK_SOURCE}	OUT Current, Peak, Sourcing ⁽¹²⁾	$C_{LOAD}=1.0\ \mu\text{F}$, $f=1\ \text{kHz}$		10.6		A
t_{RISE}	Output Rise Time ⁽¹¹⁾	$C_{LOAD}=10\ \text{nF}$	18	23	29	ns
t_{FALL}	Output Fall Time ⁽¹¹⁾	$C_{LOAD}=10\ \text{nF}$	11	19	27	ns
t_{D1}, t_{D2}	Output Propagation Delay, CMOS Inputs ⁽¹¹⁾	$0 - 12\ V_{IN}$, 1 V/ns Slew Rate	9	18	28	ns
t_{D1}, t_{D2}	Output Propagation Delay, TTL Inputs ⁽¹¹⁾	$0 - 5\ V_{IN}$, 1 V/ns Slew Rate	9	23	35	ns
I_{RVS}	Output Reverse Current Withstand ⁽¹²⁾		1500			mA
FAN3121_F085, FAN3122_F085 (Automotive-Qualified Versions)						
t_{RISE}	Output Rise Time ⁽¹¹⁾ CMOS Inputs	$C_{LOAD}=10\ \text{nF}$	12	23	31	ns
t_{FALL}	Output Fall Time ⁽¹¹⁾ CMOS Inputs	$C_{LOAD}=10\ \text{nF}$	12	19	27	ns
t_{RISE}	Output Rise Time ⁽¹¹⁾ TTL Inputs	$C_{LOAD}=10\ \text{nF}$	18	23	36	ns
t_{FALL}	Output Fall Time ⁽¹¹⁾ TTL Inputs	$C_{LOAD}=10\ \text{nF}$	10	19	28	ns
t_{D1}, t_{D2}	Output Propagation Delay, CMOS Inputs ⁽¹³⁾	$0 - 12\ V_{IN}$, 1 V/ns Slew Rate	6	18	35	ns
t_{D1}, t_{D2}	Output Propagation Delay, TTL Inputs ⁽¹¹⁾	$0 - 5\ V_{IN}$, 1 V/ns Slew Rate	9	23	36	ns
V_{OH}	High Level Output Voltage ⁽¹³⁾	$V_{OH}=V_{DD}-V_{OUT}$, $I_{OUT}=-1\ \text{mA}$		15	35	mV
V_{OL}	Low Level Output Voltage ⁽¹³⁾	$I_{OUT}=1\ \text{mA}$		10	25	mV

Notes:

9. Lower supply current due to inactive TTL circuitry.
10. EN inputs have modified TTL thresholds; refer to the ENABLE section.
11. See *Timing Diagrams of Figure 8 and Figure 9*.
12. Not tested in production.
13. Automotive-qualified F085 version specifications.

Timing Diagrams

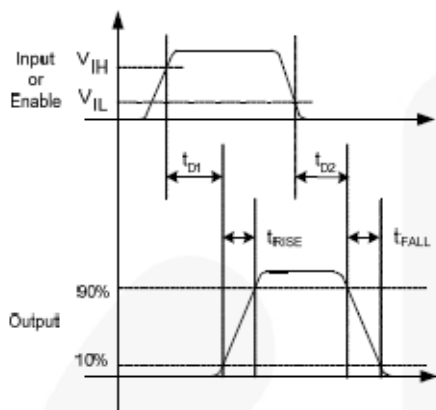


Figure 8. Non-Inverting

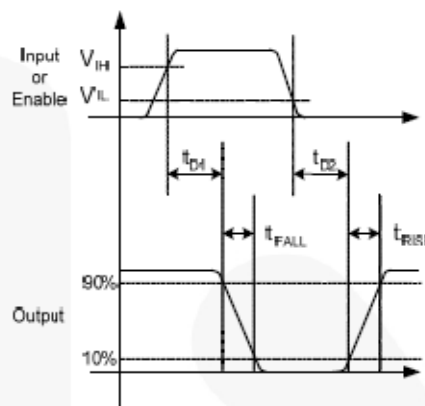


Figure 9. Inverting

FAN3121 / FAN3122 — Single 9-A High-Speed, Low-Side Gate Driver

Typical Performance Characteristics

Typical characteristics are provided at 25°C and $V_{DD}=12\text{ V}$ unless otherwise noted.

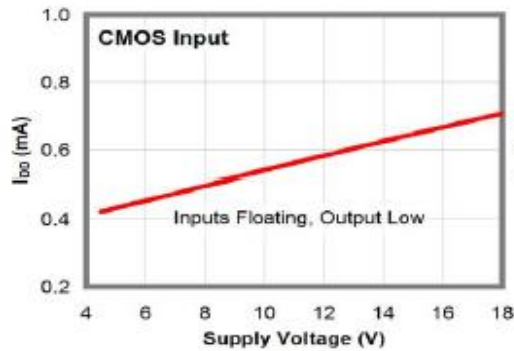


Figure 10. I_{DD} (Static) vs. Supply Voltage⁽¹⁴⁾

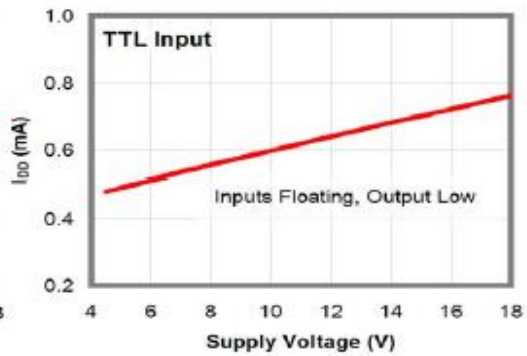


Figure 11. I_{DD} (Static) vs. Supply Voltage⁽¹⁴⁾

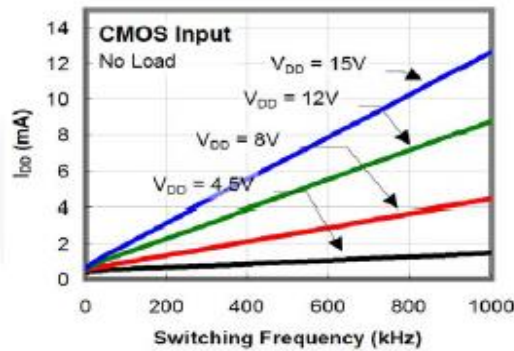


Figure 12. I_{DD} (No-Load) vs. Frequency

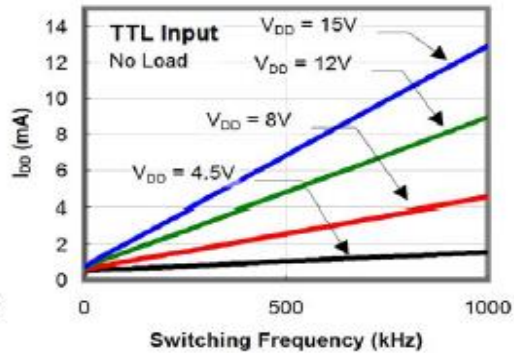


Figure 13. I_{DD} (No-Load) vs. Frequency

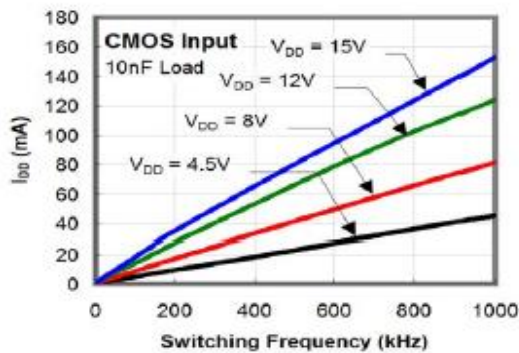


Figure 14. I_{DD} (10 nF Load) vs. Frequency

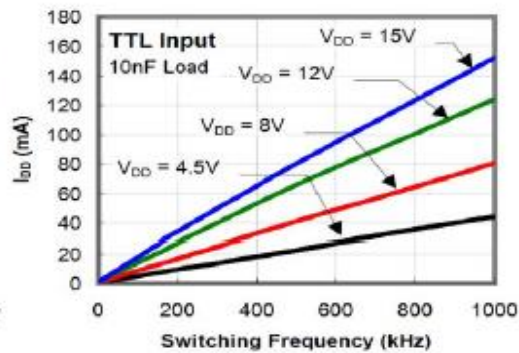


Figure 15. I_{DD} (10 nF Load) vs. Frequency

Typical Performance Characteristics

Typical characteristics are provided at 25°C and $V_{DD}=12\text{ V}$ unless otherwise noted.

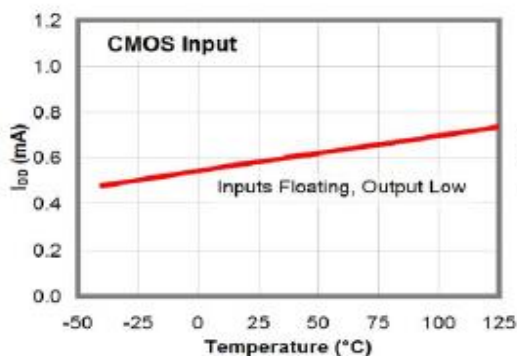


Figure 16. I_{DD} (Static) vs. Temperature⁽¹⁴⁾

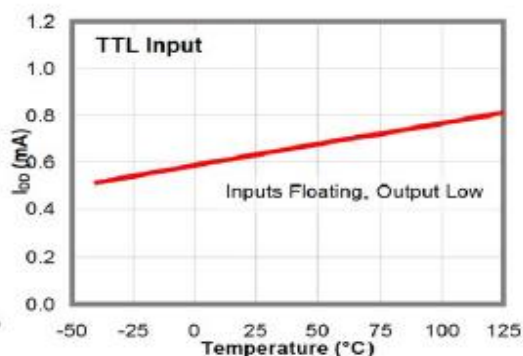


Figure 17. I_{DD} (Static) vs. Temperature⁽¹⁴⁾

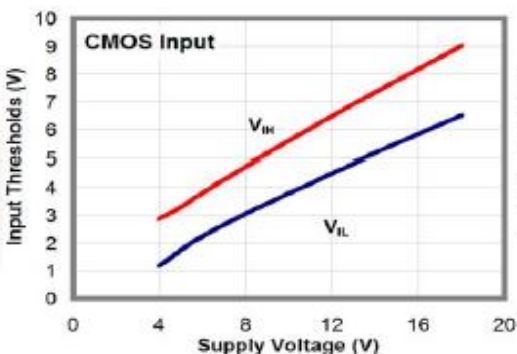


Figure 18. Input Thresholds vs. Supply Voltage

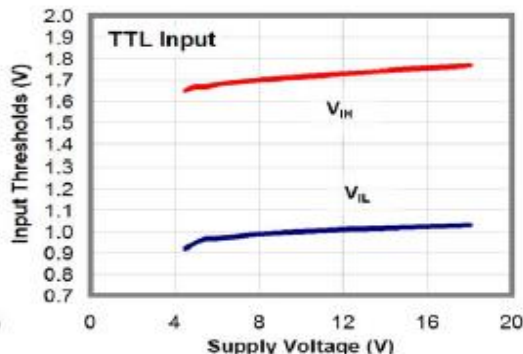


Figure 19. Input Thresholds vs. Supply Voltage

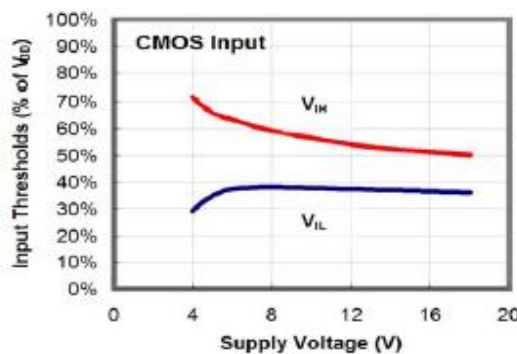


Figure 20. Input Thresholds % vs. Supply Voltage

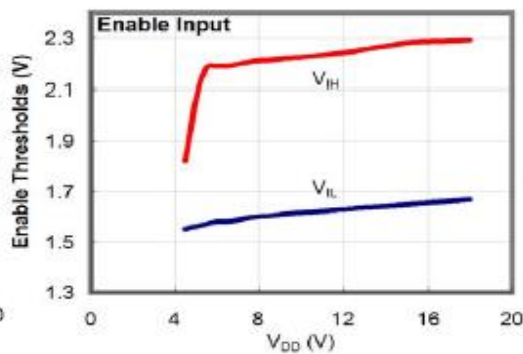


Figure 21. Enable Thresholds vs. Supply Voltage

Typical Performance Characteristics

Typical characteristics are provided at 25°C and $V_{DD}=12\text{ V}$ unless otherwise noted.

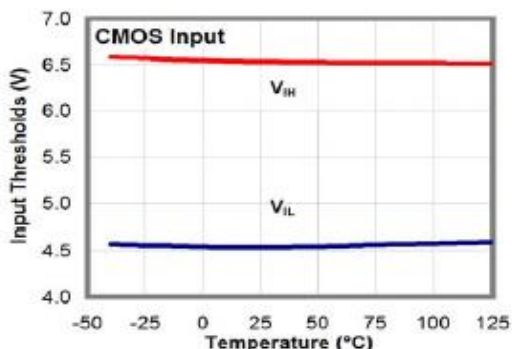


Figure 22. CMOS Input Thresholds vs. Temperature

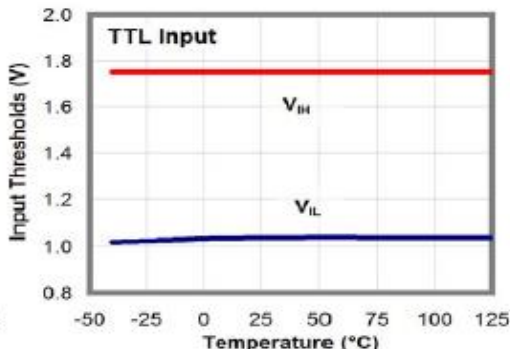


Figure 23. TTL Input Thresholds vs. Temperature

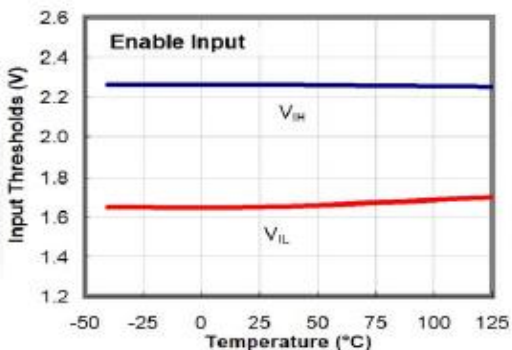


Figure 24. Enable Thresholds vs. Temperature

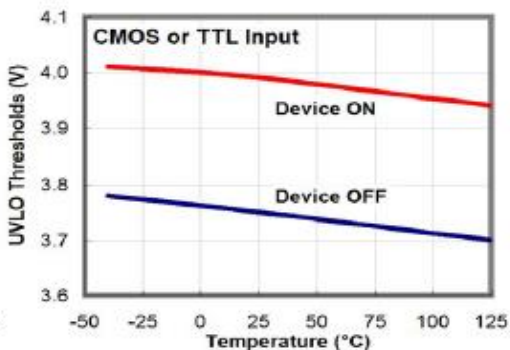


Figure 25. UVLO Thresholds vs. Temperature

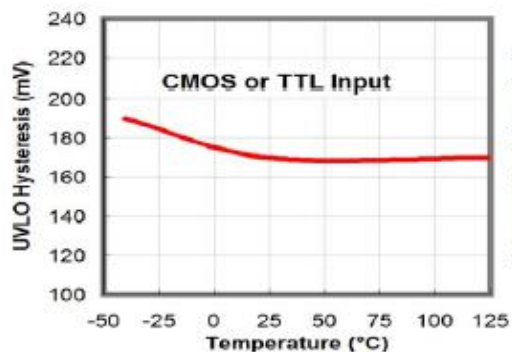


Figure 26. UVLO Hysteresis vs. Temperature

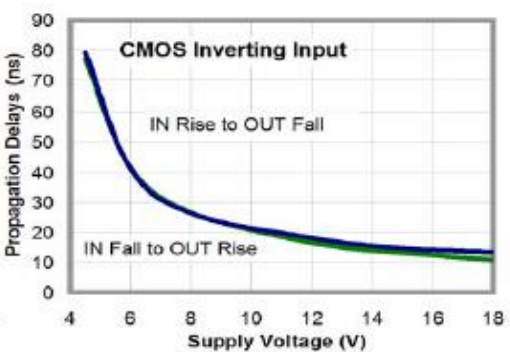


Figure 27. Propagation Delay vs. Supply Voltage

Typical Performance Characteristics

Typical characteristics are provided at 25°C and $V_{DD}=12\text{ V}$ unless otherwise noted.

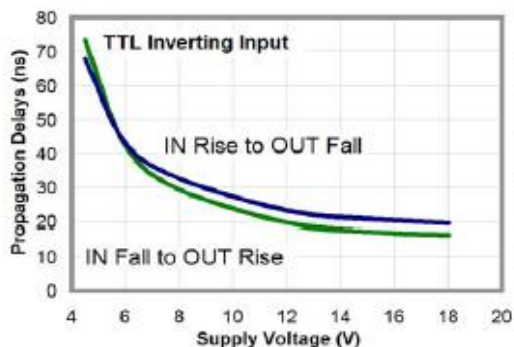


Figure 28. Propagation Delay vs. Supply Voltage

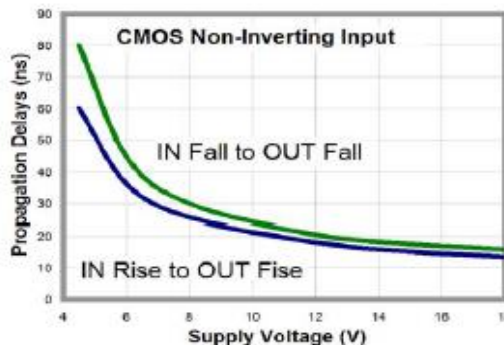


Figure 29. Propagation Delay vs. Supply Voltage

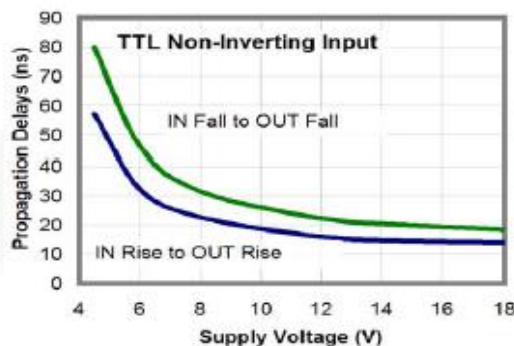


Figure 30. Propagation Delay vs. Supply Voltage

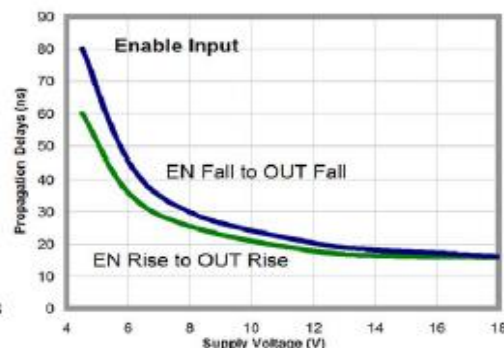


Figure 31. Propagation Delay vs. Supply Voltage

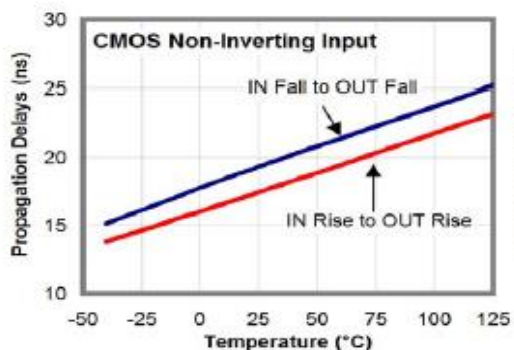


Figure 32. Propagation Delays vs. Temperature

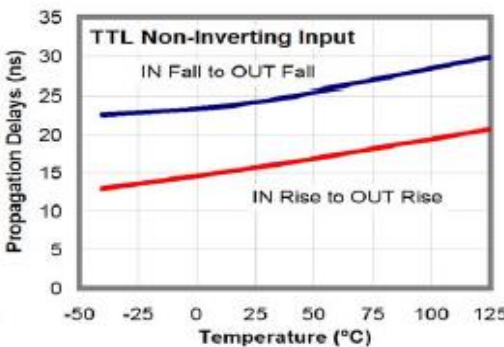


Figure 33. Propagation Delays vs. Temperature

Typical Performance Characteristics

Typical characteristics are provided at 25°C and $V_{DD}=12\text{ V}$ unless otherwise noted.

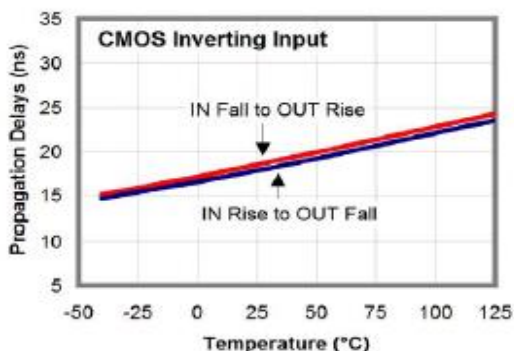


Figure 34. Propagation Delays vs. Temperature

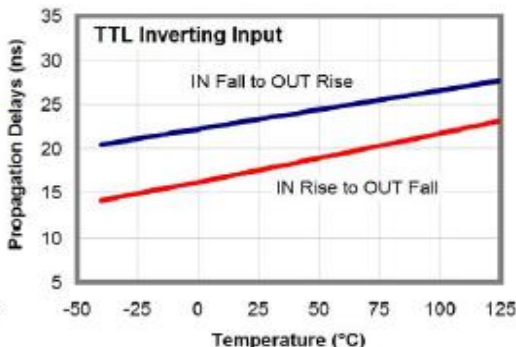


Figure 35. Propagation Delays vs. Temperature

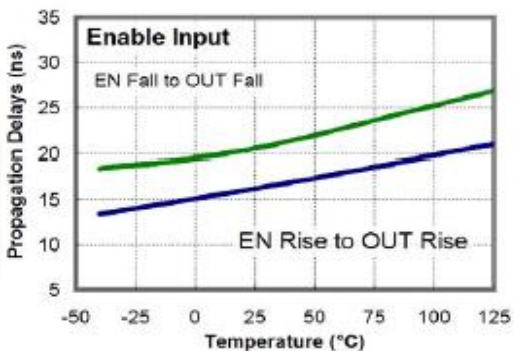


Figure 36. Propagation Delays vs. Temperature

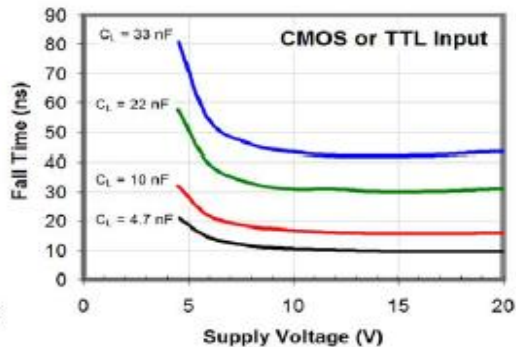


Figure 37. Fall Time vs. Supply Voltage

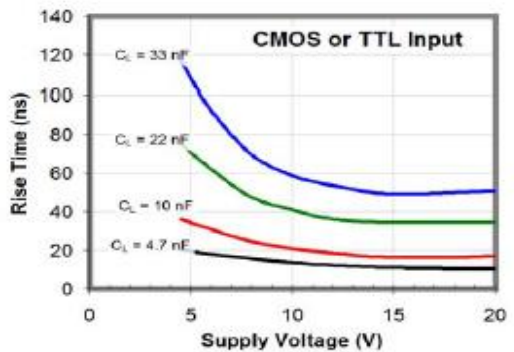


Figure 38. Rise Time vs. Supply Voltage

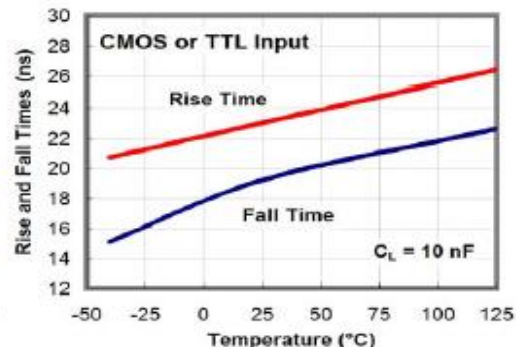


Figure 39. Rise and Fall Time vs. Temperature

Typical Performance Characteristics

Typical characteristics are provided at 25°C and $V_{DD}=12\text{ V}$ unless otherwise noted.

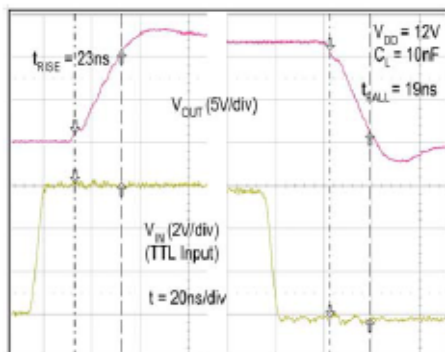


Figure 40. Rise / Fall Waveforms with 10 nF Load

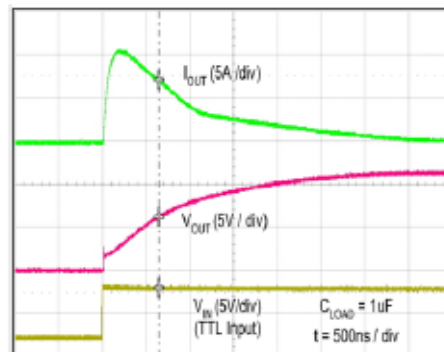


Figure 41. Quasi-Static Source Current with $V_{DD}=12\text{ V}$ ⁽¹⁵⁾

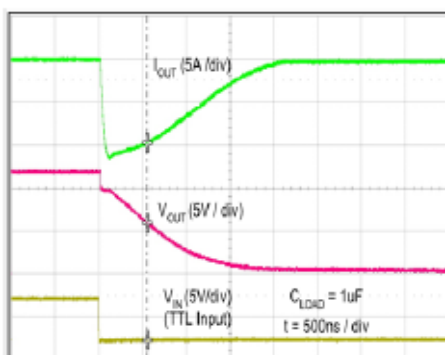


Figure 42. Quasi-Static Sink Current with $V_{DD}=12\text{ V}$ ⁽¹⁵⁾

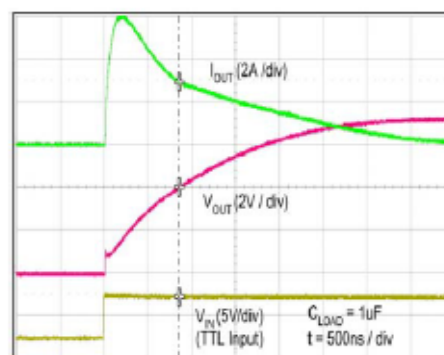


Figure 43. Quasi-Static Source Current with $V_{DD}=8\text{ V}$ ⁽¹⁵⁾

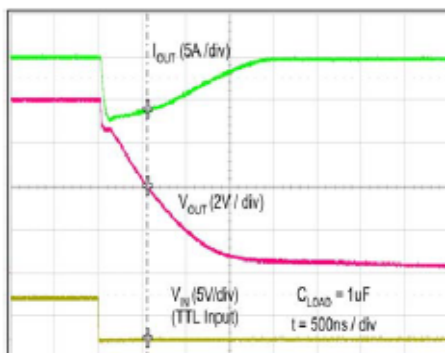


Figure 44. Quasi-Static Sink Current with $V_{DD}=8\text{ V}$ ⁽¹⁵⁾

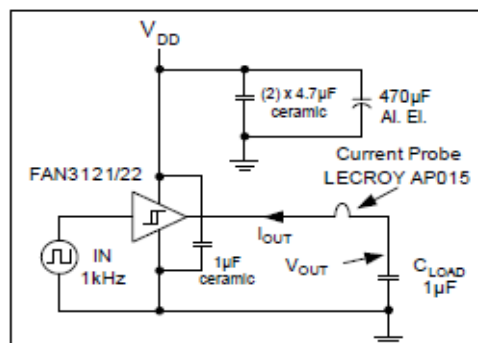


Figure 45. Quasi-Static I_{OUT} / V_{OUT} Test Circuit

Notes:

- 14. For any inverting inputs pulled LOW, non-inverting inputs pulled HIGH, or outputs driven HIGH; static I_{DD} increases by the current flowing through the corresponding pull-up/down resistor, shown in Figure 7.
- 15. The initial spike in each current waveform is a measurement artifact caused by the stray inductance of the current-measurement loop.

Applications Information

The FAN3121 and FAN3122 family offers versions in either TTL or CMOS input configuration. In the FAN3121T and FAN3122T, the input thresholds meet industry-standard TTL-logic thresholds independent of the V_{DD} voltage, and there is a hysteresis voltage of approximately 0.7 V. These levels permit the inputs to be driven from a range of input logic signal levels for which a voltage over 2 V is considered logic HIGH. The driving signal for the TTL inputs should have fast rising and falling edges with a slew rate of 6 V/ μ s or faster, so the rise time from 0 to 3.3 V should be 550 ns or less.

The FAN3121 and FAN3122 output can be enabled or disabled using the EN pin with a very rapid response time. If EN is not externally connected, an internal pull-up resistor enables the driver by default. The EN pin has logic thresholds for parts with either TTL or CMOS IN thresholds.

In the FAN3121C and FAN3122C, the logic input thresholds are dependent on the V_{DD} level and, with V_{DD} of 12 V, the logic rising edge threshold is approximately 55% of V_{DD} and the input falling edge threshold is approximately 38% of V_{DD} . The CMOS input configuration offers a hysteresis voltage of approximately 17% of V_{DD} . The CMOS inputs can be used with relatively slow edges (approaching DC) if good decoupling and bypass techniques are incorporated in the system design to prevent noise from violating the input voltage hysteresis window. This allows setting precise timing intervals by fitting an R-C circuit between the controlling signal and the IN pin of the driver. The slow rising edge at the IN pin of the driver introduces a delay between the controlling signal and the OUT pin of the driver.

Static Supply Current

In the I_{DD} (static) Typical Performance Characteristics, the curves are produced with all inputs / enables floating (OUT is LOW) and indicates the lowest static I_{DD} current for the tested configuration. For other states, additional current flows through the 100 k Ω resistors on the inputs and outputs, as shown in the block diagram (see Figure 7). In these cases, the actual static I_{DD} current is the value obtained from the curves, plus this additional current.

MillerDrive™ Gate-Drive Technology

FAN312x gate drivers incorporate the MillerDrive™ architecture shown in Figure 46. For the output stage, a combination of bipolar and MOS devices provide large currents over a wide range of supply voltage and temperature variations. The bipolar devices carry the bulk of the current as OUT swings between 1/3 to 2/3 V_{DD} and the MOS devices pull the output to the HIGH or LOW rail.

The purpose of the Miller Drive™ architecture is to speed up switching by providing high current during the Miller plateau region when the gate-drain capacitance of the MOSFET is being charged or discharged as part of the turn-on / turn-off process.

For applications with zero voltage switching during the MOSFET turn-on or turn-off interval, the driver supplies high peak current for fast switching, even though the Miller plateau is not present. This situation often occurs in synchronous rectifier applications because the body diode is generally conducting before the MOSFET is switched on.

The output pin slew rate is determined by V_{DD} voltage and the load on the output. It is not user adjustable, but a series resistor can be added if a slower rise or fall time at the MOSFET gate is needed.

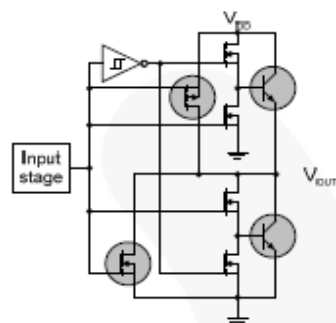


Figure 46. Miller Drive™ Output Architecture

Under-Voltage Lockout (UVLO)

The FAN312x startup logic is optimized to drive ground-referenced N-channel MOSFETs with an under-voltage lockout (UVLO) function to ensure that the IC starts in an orderly fashion. When V_{DD} is rising, yet below the 4.0 V operational level, this circuit holds the output low, regardless of the status of the input pins. After the part is active, the supply voltage must drop 0.25 V before the part shuts down. This hysteresis helps prevent chatter when low V_{DD} supply voltages have noise from the power switching. This configuration is not suitable for driving high-side P-channel MOSFETs because the low output voltage of the driver would turn the P-channel MOSFET on with V_{DD} below 4.0 V.

V_{DD} Bypassing and Layout Considerations

The FAN3121 and FAN3122 are available in either 8-lead SOIC or MLP packages. In either package, the V_{DD} pins 1 and 8 and the GND pins 4 and 5 should be connected together on the PCB.

In typical FAN312x gate-driver applications, high-current pulses are needed to charge and discharge the gate of a power MOSFET in time intervals of 50 ns or less. A bypass capacitor with low ESR and ESL should be connected directly between the V_{DD} and GND pins to provide these large current pulses without causing unacceptable ripple on the V_{DD} supply. To meet these requirements in a small size, a ceramic capacitor of 1 μ F or larger is typically used, with a dielectric material such as X7R, to limit the change in capacitance over the temperature and / or voltage application ranges.

Figure 47 shows the pulsed gate drive current path when the gate driver is supplying gate charge to turn the MOSFET on. The current is supplied from the local bypass capacitor C_{BYP} and flows through the driver to the MOSFET gate and to ground. To reach the high peak currents possible with the FAN312x family, the resistance and inductance in the path should be minimized. The localized C_{BYP} acts to contain the high peak current pulses within this driver-MOSFET circuit, preventing them from disturbing the sensitive analog circuitry in the PWM controller.

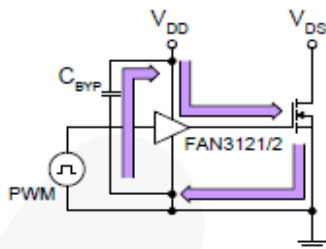


Figure 47. Current Path for MOSFET Turn-On

Figure 48 shows the path the current takes when the gate driver turns the MOSFET off. Ideally, the driver shunts the current directly to the source of the MOSFET in a small circuit loop. For fast turn-off times, the resistance and inductance in this path should be minimized.

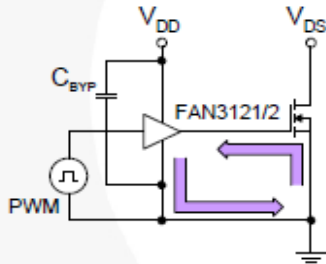


Figure 48. Current Path for MOSFET Turn-Off

Operational Waveforms

At power up, the FAN3121 inverting driver shown in Figure 49 holds the output LOW until the V_{DD} voltage reaches the UVLO turn-on threshold, as indicated in Figure 50. This facilitates proper startup control of low-side N-channel MOSFETs.

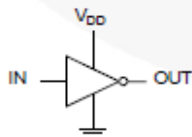


Figure 49. Inverting Configuration

The OUT pulses' magnitude follows V_{DD} magnitude with the output polarity inverted from the input until steady-state V_{DD} is reached.

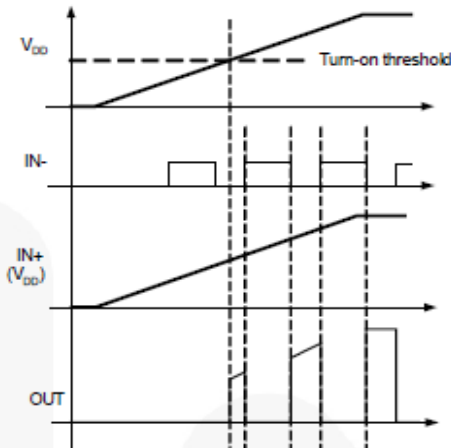


Figure 50. Inverting Startup Waveforms

At power up, the FAN3122 non-inverting driver, shown in Figure 51, holds the output LOW until the V_{DD} voltage reaches the UVLO turn-on threshold, as indicated in Figure 52. The OUT pulses magnitude follow V_{DD} magnitude until steady-state V_{DD} is reached.

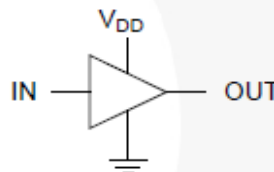


Figure 51. Non-Inverting Driver

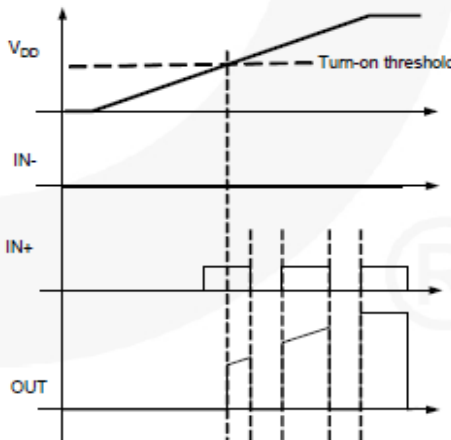


Figure 52. Non-Inverting Startup Waveforms

Thermal Guidelines

Gate drivers used to switch MOSFETs and IGBTs at high frequencies can dissipate significant amounts of power. It is important to determine the driver power dissipation and the resulting junction temperature in the application to ensure that the part is operating within acceptable temperature limits.

The total power dissipation in a gate driver is the sum of two components, P_{GATE} and $P_{DYNAMIC}$:

$$P_{TOTAL} = P_{GATE} + P_{DYNAMIC} \quad (1)$$

Gate Driving Loss: The most significant power loss results from supplying gate current (charge per unit time) to switch the load MOSFET on and off at the switching frequency. The power dissipation that results from driving a MOSFET at a specified gate-source voltage, V_{GS} , with gate charge, Q_G , at switching frequency, f_{SW} , is determined by:

$$P_{GATE} = Q_G \cdot V_{GS} \cdot f_{SW} \quad (2)$$

Dynamic Pre-drive / Shoot-through Current: A power loss resulting from internal current consumption under dynamic operating conditions, including pin pull-up / pull-down resistors, can be obtained using the "IDD (No-Load) vs. Frequency" graphs in Typical Performance Characteristics to determine the current $I_{DYNAMIC}$ drawn from V_{DD} under actual operating conditions:

$$P_{DYNAMIC} = I_{DYNAMIC} \cdot V_{DD} \quad (3)$$

Once the power dissipated in the driver is determined, the driver junction rise with respect to circuit board can be evaluated using the following thermal equation, assuming Ψ_{JB} was determined for a similar thermal design (heat sinking and air flow):

$$T_J = P_{TOTAL} \cdot \Psi_{JB} + T_B \quad (4)$$

where:

T_J = driver junction temperature;

Ψ_{JB} = (psi) thermal characterization parameter relating temperature rise to total power dissipation; and

T_B = board temperature in location as defined in the Thermal Characteristics table.

In a full-bridge synchronous rectifier application, shown in Figure 53, each FAN3122 drives a parallel combination of two high-current MOSFETs, (such as FDM8880S). The typical gate charge for each SR MOSFET is 70 nC with $V_{GS} = V_{DD} = 9$ V. At a switching frequency of 300 kHz, the total power dissipation is:

$$P_{GATE} = 2 \cdot 70 \text{ nC} \cdot 9\text{V} \cdot 300 \text{ kHz} = 0.378 \text{ W} \quad (5)$$

$$P_{DYNAMIC} = 2 \text{ mA} \cdot 9 \text{ V} = 18 \text{ mW} \quad (6)$$

$$P_{TOTAL} = 0.396 \text{ W} \quad (7)$$

The SOIC-8 has a junction-to-board thermal characterization parameter of $\Psi_{JB} = 42^\circ\text{C/W}$. In a system application, the localized temperature around the device is a function of the layout and construction of the PCB along with airflow across the surfaces. To ensure reliable operation, the maximum junction temperature of the device must be prevented from exceeding the maximum rating of 150°C ; with 80% derating, T_J would be limited to 120°C . Rearranging Equation 4 determines the board temperature required to maintain the junction temperature below 120°C :

$$T_{B,MAX} = T_J - P_{TOTAL} \cdot \Psi_{JB} \quad (8)$$

$$T_{B,MAX} = 120^\circ\text{C} - 0.396 \text{ W} \cdot 42^\circ\text{C/W} = 104^\circ\text{C} \quad (9)$$

For comparison, replace the SOIC-8 used in the previous example with the 3x3 mm MLP package with $\Psi_{JB} = 2.8^\circ\text{C/W}$. The 3x3 mm MLP package can operate at a PCB temperature of 118°C , while maintaining the junction temperature below 120°C . This illustrates that the physically smaller MLP package with thermal pad offers a more conductive path to remove the heat from the driver. Consider tradeoffs between reducing overall circuit size with junction temperature reduction for increased reliability.

Typical Application Diagrams

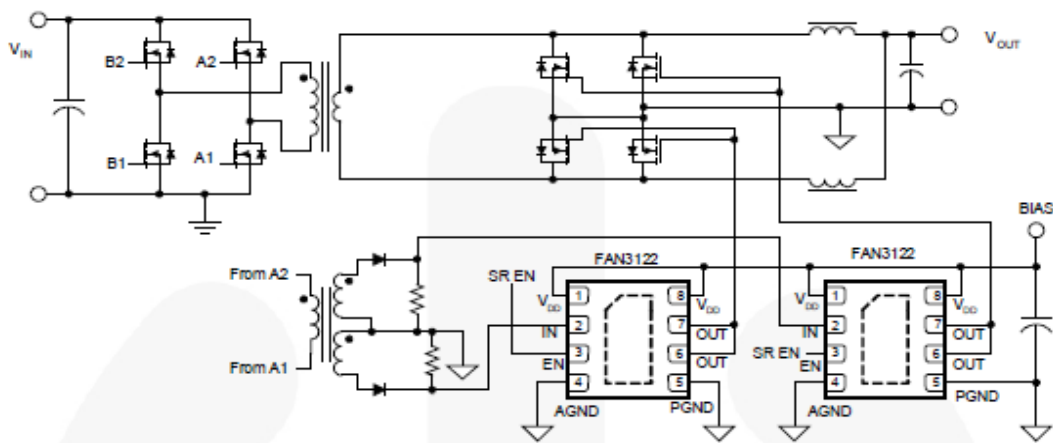


Figure 53. Full-Bridge Synchronous Rectification

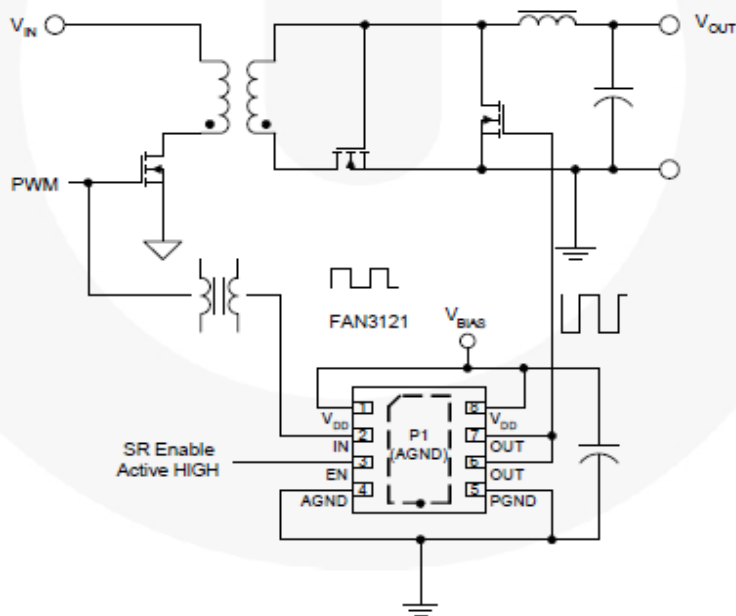


Figure 54. Hybrid Synchronous Rectification in a Forward Converter

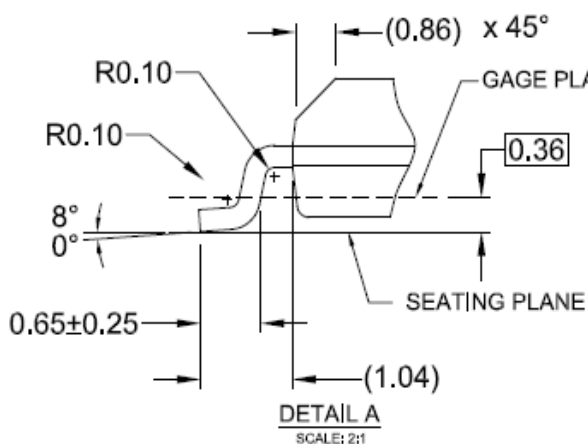
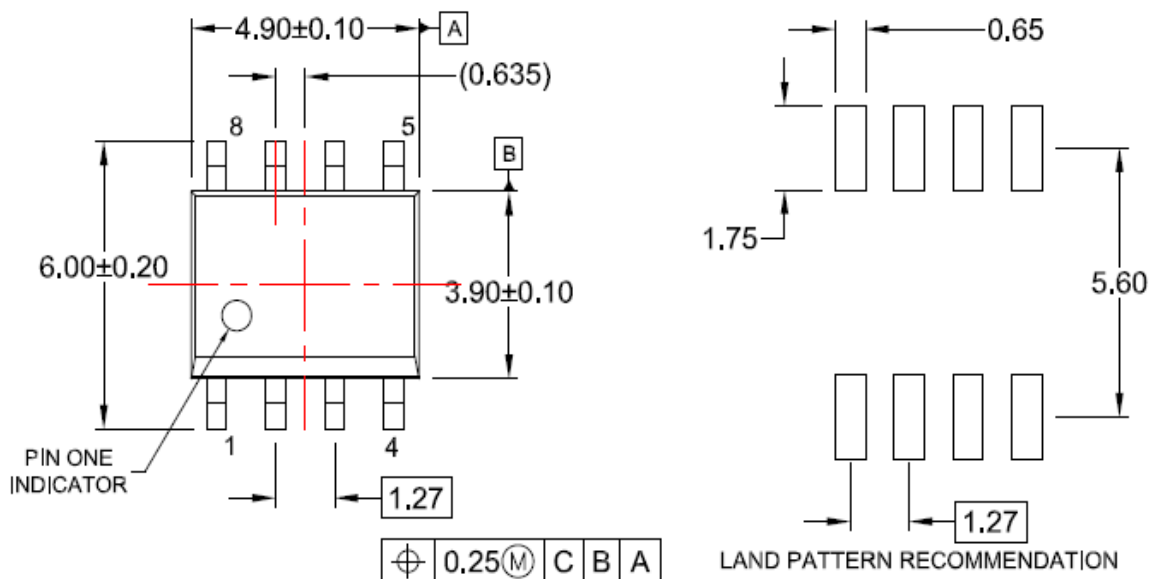
Table 1. Related Products

Part Number	Type	Gate Drive ⁽¹⁶⁾ (Sink/Src)	Input Threshold	Logic	Package ⁽¹⁸⁾
FAN3111C	Single 1 A	+1.1 A / -0.9 A	CMOS	Single Channel of Dual-Input/Single-Output	SOT23-5, MLP6
FAN3111E	Single 1 A	+1.1 A / -0.9 A	External ⁽¹⁷⁾	Single Non-Inverting Channel with External Reference	SOT23-5, MLP6
FAN3100C	Single 2 A	+2.5 A / -1.8 A	CMOS	Single Channel of Two-Input/One-Output	SOT23-5, MLP6
FAN3100T	Single 2 A	+2.5 A / -1.8 A	TTL	Single Channel of Two-Input/One-Output	SOT23-5, MLP6
FAN3180	Single 2 A	+2.4 A / -1.6 A	TTL	Single Non-Inverting Channel + 3.3 V LDO	SOT23-5
FAN3216T	Dual 2 A	+2.4 A / -1.6 A	TTL	Dual Inverting Channels	SOIC8
FAN3217T	Dual 2 A	+2.4 A / -1.6 A	TTL	Dual Non-Inverting Channels	SOIC8
FAN3226C	Dual 2 A	+2.4 A / -1.6 A	CMOS	Dual Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3226T	Dual 2 A	+2.4 A / -1.6 A	TTL	Dual Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3227C	Dual 2 A	+2.4 A / -1.6 A	CMOS	Dual Non-Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3227T	Dual 2 A	+2.4 A / -1.6 A	TTL	Dual Non-Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3228C	Dual 2 A	+2.4 A / -1.6 A	CMOS	Dual Channels of Two-Input/One-Output	SOIC8, MLP8
FAN3228T	Dual 2A	+2.4 A / -1.6 A	TTL	Dual Channels of Two-Input/One-Output	SOIC8, MLP8
FAN3229C	Dual 2 A	+2.4 A / -1.6 A	CMOS	Dual Channels of Two-Input/One-Output	SOIC8, MLP8
FAN3229T	Dual 2 A	+2.4 A / -1.6 A	TTL	Dual Channels of Two-Input/One-Output	SOIC8, MLP8
FAN3268T	Dual 2 A	+2.4 A / -1.6 A	TTL	20 V Non-Inverting Channel (NMOS) and Inverting Channel (PMOS) + Dual Enables	SOIC8
FAN3278T	Dual 2 A	+2.4 A / -1.6 A	TTL	30 V Non-Inverting Channel (NMOS) and Inverting Channel (PMOS) + Dual Enables	SOIC8
FAN3223C	Dual 4 A	+4.3 A / -2.8 A	CMOS	Dual Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3213T	Dual 4 A	+4.3 A / -2.8 A	TTL	Dual Inverting Channels	SOIC8
FAN3214T	Dual 4 A	+4.3 A / -2.8 A	TTL	Dual Non-Inverting Channels	SOIC8
FAN3223T	Dual 4 A	+4.3 A / -2.8 A	TTL	Dual Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3224C	Dual 4 A	+4.3 A / -2.8 A	CMOS	Dual Non-Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3224T	Dual 4 A	+4.3 A / -2.8 A	TTL	Dual Non-Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3225C	Dual 4 A	+4.3 A / -2.8 A	CMOS	Dual Channels of Two-Input/One-Output	SOIC8, MLP8
FAN3225T	Dual 4 A	+4.3 A / -2.8 A	TTL	Dual Channels of Two-Input/One-Output	SOIC8, MLP8
FAN3121C	Single 9 A	+9.7 A / -7.1 A	CMOS	Single Inverting Channel + Enable	SOIC8, MLP8
FAN3121T	Single 9 A	+9.7 A / -7.1 A	TTL	Single Inverting Channel + Enable	SOIC8, MLP8
FAN3122C	Single 9 A	+9.7 A / -7.1 A	CMOS	Single Non-Inverting Channel + Enable	SOIC8, MLP8
FAN3122T	Single 9 A	+9.7 A / -7.1 A	TTL	Single Non-Inverting Channel + Enable	SOIC8, MLP8
FAN3240	Dual 12 A	> +12.0 A	TTL	Dual-Coil Relay Driver, Timing Config. 0	SOIC8
FAN3241	Dual 12 A	> +12.0 A	TTL	Dual-Coil Relay Driver, Timing Config. 1	SOIC8

Notes:16. Typical currents with OUT at 6 V and $V_{DD} = 12$ V.

17. Thresholds proportional to an externally supplied reference voltage.

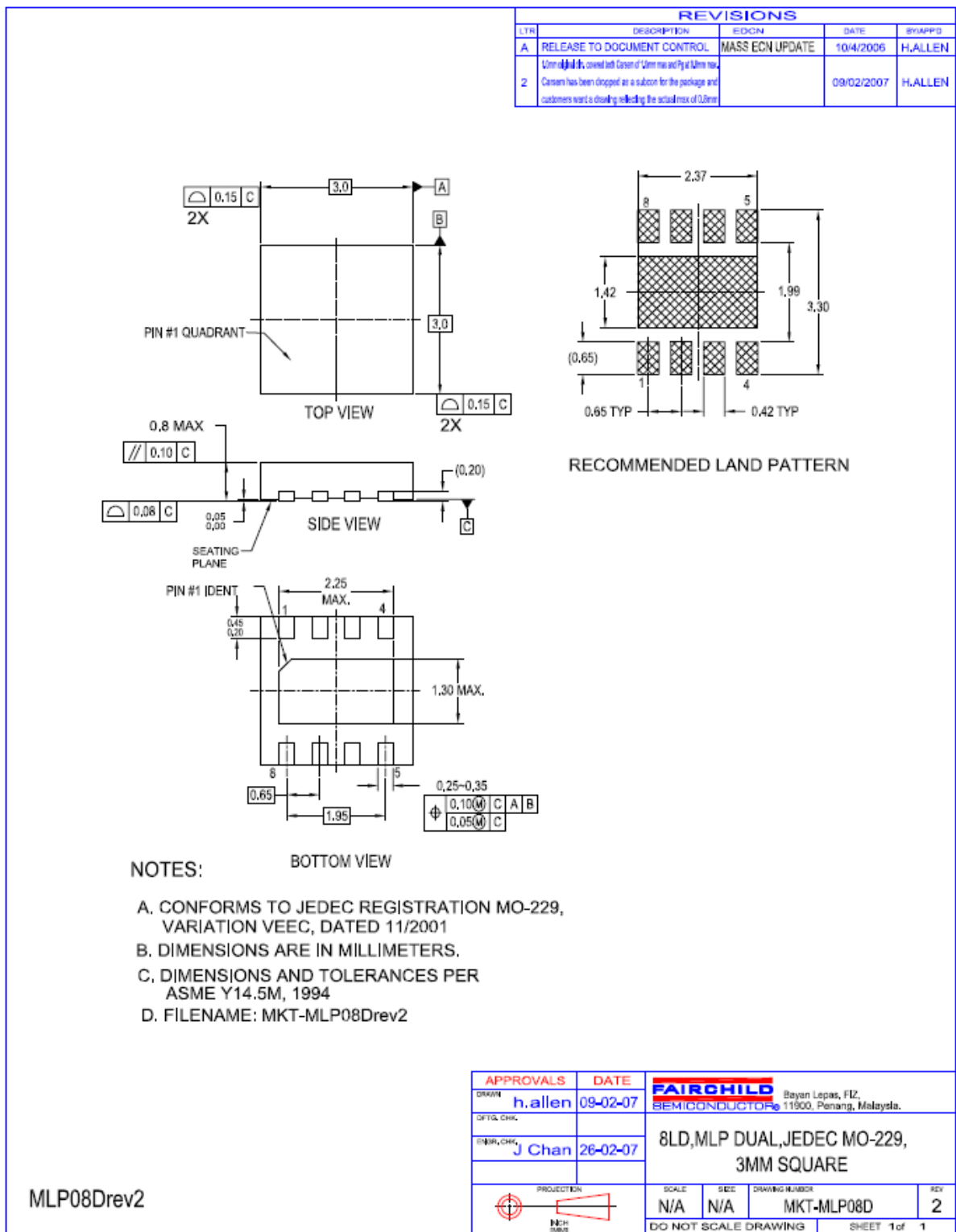
18. Automotive-qualified F085 versions are only offered in SOIC8 packages.



NOTES:

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M
- E) DRAWING FILENAME: M08Arev16







TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

AccuPower™

AttitudeEngine™

Awinda®

AX-CAP®

BitSiC™

Build It Now™

CorePLUS™

CorePOWER™

CROSSVOLT™

CTL™

Current Transfer Logic™

DEUXPEED®

Dual Cool™

EcoSPARK®

EfficientMax™

ESBC™

F³™

Fairchild®

Fairchild Semiconductor®

FACT Quiet Series™

FACT®

FAST®

FastCore™

FETBench™

FPS™

F-PFS™

FRFET®

Global Power Resource™

GreenBridge™

Green FPS™

Green FPS™ e-Series™

Gmax™

GTO™

IntelliMAX™

ISOPLANAR™

Making Small Speakers Sound Louder

and Better™

MegaBuck™

MICROCOUPLER™

MicroFET™

MicroPak™

MicroPak2™

MillerDrive™

MotionMax™

MotionGrid®

MTI®

MTx®

MVN®

mWSaver®

OptoHIT™

OPTOLOGIC®

OPTOPLANAR®



PowerTrench®

PowerXS™

Programmable Active Droop™

QFET®

QS™

Quiet Series™

RapidConfigure™



Saving our world, 1mW/W/kW at a time™

SignalWise™

SmartMax™

SMART START™

Solutions for Your Success™

SPM®

STEALTH™

SuperFET®

SuperSOT™-3

SuperSOT™-6

SuperSOT™-8

SupreMOS®

SyncoFET™

Synco-Lock™

SYSTEM GENERAL®



TinyBoost®

TinyBuck®

TinyCalc™

TinyLogic®

TINYOPTO™

TinyPower™

TinyPWM™

TinyWire™

TransiC™

TriFault Detect™

TRUECURRENT®

µSerDes™



UHC®

Ultra FRFET™

UniFET™

VCX™

VisualMax™

VoltagePlus™

XS™

Xsens™

仙童™

* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. TO OBTAIN THE LATEST, MOST UP-TO-DATE DATASHEET AND PRODUCT INFORMATION, VISIT OUR WEBSITE AT [HTTP://WWW.FAIRCHILDSEMI.COM](http://www.fairchildsemi.com). FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
- A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. 173

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Fairchild Semiconductor:](#)

[FAN3121TMPX](#) [FAN3121TMX](#)