ABSTRACT

KRISHNA, VINEETH. Performance Evaluation of Novel 3.3kV SiC JBSFET for Photovoltaic String Inverter Application (Under the direction of Dr. Subhashish Bhattacharya).

The development and use of Wide Bang Gap devices in power conversion systems has been steadily increasing realizing their advantages over Si power devices. The SiC MOSFET is the most popular SIC devices being used today. But these devices are associated with significant losses with its body diode. In order to mitigate these losses, a novel device, the JBSFET was developed where a JBS diode and a SiC MOSFET were monolithically integrated. The JBS diode, associated with have low reverse recovery losses solves the issue with the SiC MOSFET.

In this work, a gate driver and its power supply were designed and fabricated for a novel 3.3kV JBSFET G3R60MS33N from GeneSiC has been designed and fabricated. The device was then dynamically characterized at a wide temperature range to extract the switching losses associated with it. Then, to validate the performance of this device in a power electronics circuit, a 1500V PV string inverter was designed using these devices. The switching loss data acquired from the double pulse test was then used to develop a thermal model in PLECS simulation software to design a heat sink required for the safe operation for the PV string inverter. Through the operation of this inverter, the advantages of the JBSFET were realized.

Performance Evaluation of a Novel 3.3kV JBSFET for Photovoltaic String Inverter Application

by
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APPROVED BY:

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_____	
Dr. Leonard White	

DEDICATION

To my family, friends and my Ajji and thatha who are the reason for what I am today.

For my loving mother.

BIOGRAPHY

Vineeth Krishna was born in Bengaluru, India. He graduated from B.M.S College of Engineering with a Bachelors of Engineering degree majoring in Electrical Engineering in May 2018.

He joined North Carolina State University in fall 2018 to pursue Master of Science in Electrical Engineering with a specialization in Power Electronics. At his time at NC State, he has been associated with the Future Renewable Electrical Energy Delivery and Management (FREEDM) Systems Center since June 2019. During his time at FREEDM he concentrated on the research areas of Gate driver design, PCB design, Wide Band Gap devices and their characterization.

ACKNOWLEDGMENTS

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CHAPTER 1

INTRODUCTION

1.1 Wide Band Gap (WBG) Devices.

As the demand for energy rises in modern civilization so does the need to construct highly efficient and highly power dense power converter circuits. This is achievable by pushing the limits of power semiconductor devices used in the circuits. Since the inception of transistors, power transistors have been mainly developed using Si technology similar to the technology used to make transistors for digital circuits used in computer processors and other digital electronics circuits.

Si power transistor have already been pushed to the limits but the need for a more efficient and high-power dense converters remain. As the Si power transistor technology was approaching the limits of blocking voltage capabilities and operating frequencies, there was a dire need to shift to Wide Band Gap (WBG) transistor technology. In the 1980s it was proven that SiC was suitable for power semiconductors. The advantages of SiC transistor technology over Si is as follows:

lower specific on-state resistance:

The specific on-state resistances of Si and SiC devices are given by the equations:

$$R_{On,Sp,Ideal}(Si) = 5.93\ x\ 10^{-9} BV^{2.5}$$

$$R_{On,Sp,Ideal}(SiC) = 2.97\ x\ 10^{-12} BV^{2.5}$$

Where, BV is the breakdown voltage of the device being designed Therefore, developing a Si MOSFET for a given breakdown voltage would result in a higher on-state resistance than compared with that of SiC MOSFET. The higher on-state resistance would also result in a thicker drift region within the device. This would also result in higher conduction losses in the Si device than compared with the SiC device.

Higher voltage blocking capabilities:

From the above table, it is evident that SiC as a material has higher Critical electric field, which allows the power devices made from SiC to have higher voltage blocking capabilities than compared to their Si counterparts [1].

Higher operating frequency:

Si power devices can operate at switching frequencies within a few tens of kilohertz, whereas the SiC devices can switch at frequencies of about a few hundred kilohertz. The operation of power devices at higher frequencies can reduce the size of the passive components present in the circuit like inductors, capacitors and transformers as the high frequency of operation results in the circuit having lower voltage and current ripples [2].

Lower cooling requirement: SiC MOSFETs can be utilized in power converters with simpler cooling requirements than compared to Si MOSFETs. As SiC power devices can handle higher temperatures than Si devices and has lower conduction loss compared to a Si device of the same breakdown voltage rating as SiC devices have lower on-state thermal resistance.

These advantages of SiC transistor technology have been realized using SiC MOSFETs in power converters. Today, SiC MOSFETs with voltage blocking capabilities of 3.3kV and operational frequency of few hundred kHz. Another advantage SiC MOSFETs have over Si MOSFETs is that the switching loss emitted by SiC MOSFETs almost remains constant with temperature whereas, the switching loss of Si MOSFETs tend to increase with increase in temperature. This feature of SiC MOSFETs make them suitable for applications with high ambient temperature like that in electric drive trains in EVs and in smart grid applications.

1.2 SiC MOSFET vs JBSFET

One of the drawbacks in SiC MOSFETs can be seen in the operation of bi-directional power converters. In bi-directional converters, the MOSFET is required to operate in the third quadrant, conducting the current through its body diode present in the MOSFET structure as shown in fig 1.1. The body diode of the MOSFET formed due to the nature of the doping regions of the P+ Shield region and the N- drift region which is similar in structure when compared with a P-N diode [3]. Therefore, this third quadrant operation of MOSFETs is similar to that of a normal P-N diode which is also characterized with high reverse recovery losses due to the reverse recovery current flowing through the body diode. The characteristics of the body diode of the SiC MOSFET is shown in fig 1.2. This body diode is also associated with a high forward voltage drop of about

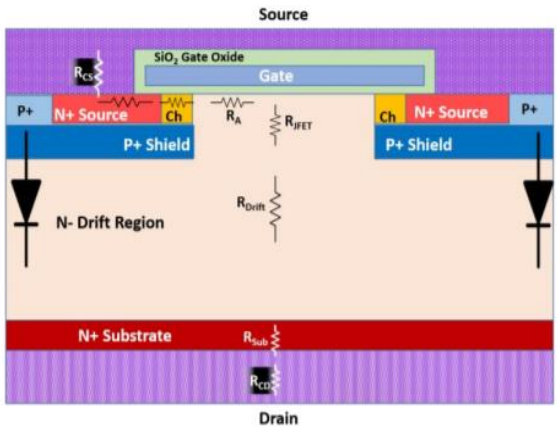


Fig 1.1. Structure of SiC MOSFET [4].

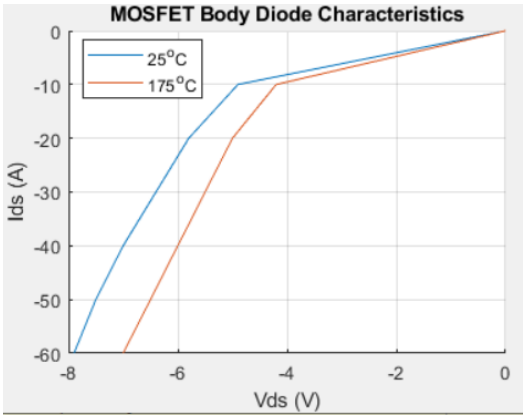


Fig 1.2 Body diode characteristics of the SiC MOSFET.

5.7V at a source-drain current (I_{SD}) of 20A when a -5V gate-source voltage (V_{gs}) is applied to the MOSFET. This high forward voltage drop contributes to the conduction loss of the body diode.

To eliminate the reverse recovery losses, the MOSFET is not allowed to operate in the third quadrant. This is done by connecting an anti-parallel SiC JBS diode across the SiC MOSFET [5]. This causes the current in the reverse direction to flow through the anti-parallel JBS diode rather

than the body diode of the MOSFET. The JBS diode being a Schottky diode has lower losses compared to the p-n junction body diode present in the MOSFET structure. Therefore, resulting in better efficiency.

As we continue to push the operational frequency of SiC devices, the effect of parasitic elements on the degradation of efficiency and the operation of the circuit becomes greater. Even though this anti-parallel connection of JBS diode to the SiC MOSFET increases the superiority of the MOSFET, it does give rise to parasitic elements in the circuit. Given the high frequency of operation, this parasitic inductance would induce high voltage spikes on both the devices.

These parasitic inductances can be reduced by monolithic integration of the two devices. Due to monolithic integration, the effect of parasitic inductances due to the modules of the device and due to the connection of devices reduces. This is the motivation behind the JBSFET. The JBSFET is the monolithic integration of JBS diode and the SiC MOSFET into one single module [6]. The structure of a JBSFET is shown in fig 1.3. In the structure of the JBSFET shown, the diode is formed by the metal contact and the N-drift region of the JBSFET. This structure is like that of a typical Schottky diode [6]. The characteristics of the body diode of the JBSFET is given

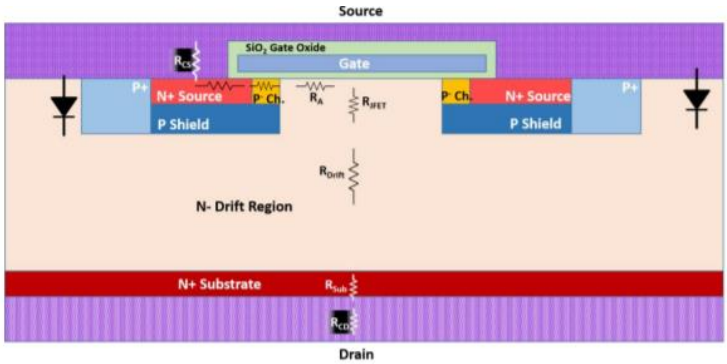


Fig 1.3. Structure of SiC JBSFET [4].

in fig 1.4. The body diode of the JBSFET is associated with a forward voltage drop of 2.3V at a

source-drain current (I_{SD}) of 20A when a -5V gate-source voltage (V_{gs}) is applied to the MOSFET which is significantly lower than its MOSFETs counterpart.

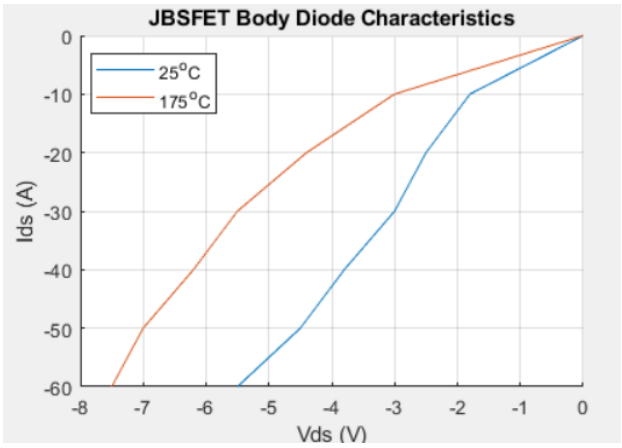


Fig 1.4 Body diode characteristics of the SiC JBSFET.

1.3 Application of JBSFET in photo-voltaic inverters.

One of the areas where the advantages of the JBSFET can be realized is in Photo-voltaic DC/AC converters. The commercially available PV converters used in large PV power plants operate at a DC bus voltage of 1000V. Si IGBTs are the semiconductor devices chosen to build

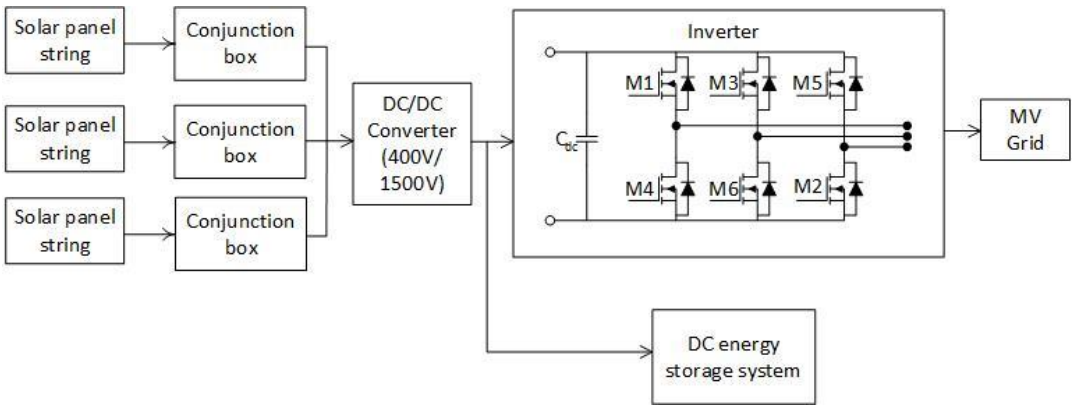


Fig 1.5. Schematic of a photovoltaic power plant.

these photo-voltaic inverters. To completely understand the effect the use of SiC JBSFET can have on the PV power plant, the schematic of the power plant is described in fig 1.5.

To obtain this 1000V DC bus voltage, a large number of solar panels are connecting in series commonly called a string. These strings are then connected in parallel through their respective conjunction boxes in order to increase the DC bus current. These parallel combinations of strings are then connected to an inverter via a DC/DC converter. In order to maximize the amount of power extracted from the solar panels, the MPPT algorithm is used to control the DC/DC converter. This power extracted is then given as input for the inverter or it stored in a battery for later use.

Current literature shows that an increase of the DC bus voltage from 1000V to 1500V can reduce the ohmic losses in the bus bar, it can also reduce the number of strings of solar panels required which would lead to reduction in the amount of auxiliary equipment required in the plant, increase in the MPPT range of the charge controller which increases the amount of power that can be extracted per solar panel [7]. The above advantages of shifting from a 1000V architecture to a 1500V architecture would lead to reduction in size of the PV power plant, reduction in losses present and increase the efficiency/power generated from the power plant.

There has been research in the development of 1500V inverters for photo-voltaic power plants. But the current research regarding this still talk about the utilization of Si IBGTs in developing these inverters. These inverters are realized using much more complex inverter topologies like the 3-level Neutral point clamped inverter (NPC) or a 3-level T-type converter in order to reduce the amount of harmonics present in the output voltage and current [8]. This would

help in reducing the filter requirements for the power plant. The pole configuration of the 3-level inverter topology poles is shown below in fig 1.6.

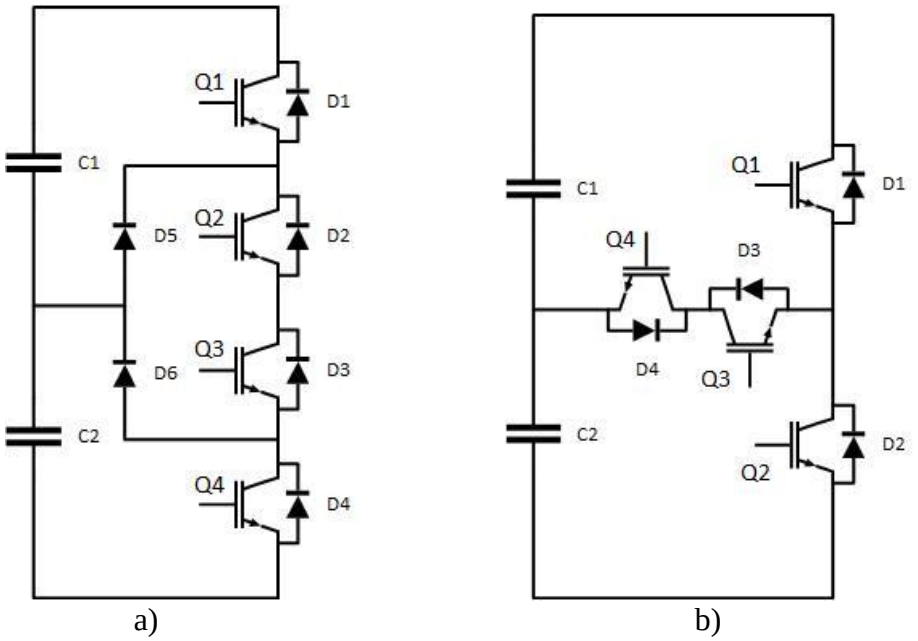


Fig 1.6. Configuration of complex 3-level inverter pole topologies using Si IGBT a.) 3-level NPC converter pole and b.) 3-level NPS (T-type) converter pole.

This makes the SiC JBSFET a good device in this application for PV string inverters. Since, the device can operate at higher operating frequencies, these 1500V photo-voltaic inverters can be realized using the basic six switch inverter topology shown in fig 1.7. Hence, eliminating the need for a complex power stage and complex control algorithms that come along with these complex topologies. Due to the high operating frequency, the SiC JBSFET based inverter can have lower filtering and magnetic requirements present.

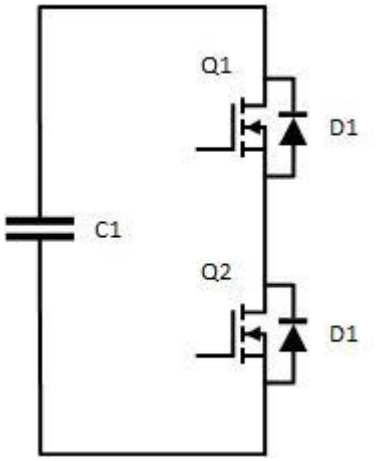


Fig 1.7. Configuration of a 2-level pole using SiC JBSFET.

The losses present in the inverter is also reduced as the number of switches is reduced. In addition to that SiC MOSFETs are known for the lower specific on resistance in comparison to Si IGBT therefore leading to lower conduction losses. During continuous operation of the DC/AC converter, the temperature of the device increases. This increase in temperature does increase the switching loss in a Si device whereas, in a SiC device this loss is somewhat constant. From the above two points it is safe to conclude that the SiC JBSFET can indeed increase the efficiency of the converter.

CHAPTER 2

GATE DRIVER DESIGN AND DOUBLE PULSE TEST

2.1 GATE DRIVER DESIGN

A gate driver is required to provide the turn-on and turn-OFF signal to the JBSFET. Here, since we are using a SiC power JBSFET the voltage level for turn on is V_{gs} = +20V and V_{gs} = -5V is used for switching the transistor off. The schematic of the gate driver circuit is given in fig 2.1. The parameters of the designed gate driver is given in table 2.1.

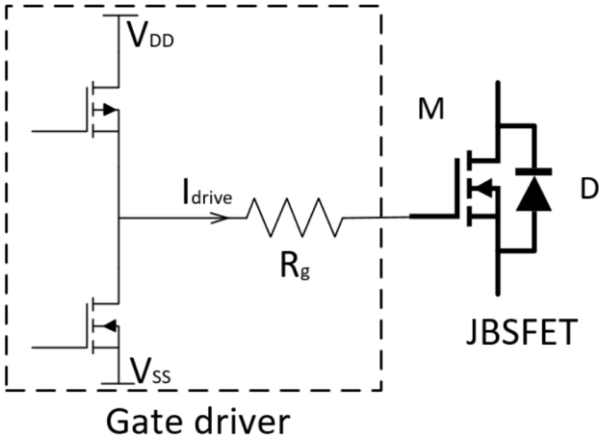


Fig 2.1. Schematic of the gate driver circuit used for switching the JBSFT.

Table 2.1. Parameters of the gate driver

Parameters	Value
Turn-ON Voltage V_{DD} (V)	25
Turn-ON Voltage V_{SS} (V)	-5
Gate Resistance R_g (Ω)	33
Internal Gate Resistance R_{gint} (Ω)	1.6

.

2.1.1 Drive Power

Drive power is the power required by the MOSFET to switch it ON and OFF. It depends on the gate charge characteristics of the MOSFET which, is described in the respective datasheet of the MOSFET. The drive power is calculated by the formula:

$$P_{drive} = Q_{gate} f_{sw} \Delta V_{gs} \text{ W}$$

Where, P_{drive} is the drive power, Q_{gate} is the gate charge of the MOSFET, ΔV_{gs} is the total voltage swing of the gate-source voltage of the MOSFET.

From the device datasheet we have Q gate = 305nC. The switching frequency is chosen to be 10 KHz. And as mentioned earlier, the turn on and off voltages for the MOSFET is V_{gs} = +20V and V_{gs} = -5V. This implies that ΔVgs = 25V. Therefore, the drive power for the MOSFET comes out to be 0.076W.

2.1.2 Gate Resistance

To control the current that is flowing into the gate terminal of the MOSFET, we introduce a gate resistance in the path. The MOSFET already has an internal gate resistance, which is given as 1.6 Ω in the datasheet. The gate resistance also has an influence on the switching $\frac{dV}{dt}$ and $\frac{dI}{dt}$ of the MOSFET. Lower the gate resistance, faster is the turn-ON and turn-OFF process of the MOSFETs, but this also increases the drain-source voltage V_{DS} and drain-source current I_{DS} overshoot. Hence, the gate resistance must be chosen carefully considering these attributes.

2.1.3 Maximum Drive Current

The peak drive current is the maximum current that will flow in or out of the gate terminal of the MOSFET. It is given by the formula:

$$I_{dmax} = \frac{\Delta V_{gs}}{R_{gint} + R_{gext}}$$

Where, R_{gint} and R_{gext} are the internal and external gate resistances, respectively. In this design, R_{g_int} was found to be 1.6Ω for the JBSFET and a R_{gext} of 33 Ohms was chosen. This means that the Maximum drive current is 0.72A.

Due to the parasitics present in the gate drive circuitry, the practical maximum drive current will be 70% of the calculated maximum drive current calculated from the above equation.

2.1.4 Gate Driver IC

One of the main components of the gate driver is the gate driver IC. This IC should be chosen carefully by looking at certain parameters like:

Common-mode Transient Immunity (CMTI): A gate drier IC with high CMTI means that it can handle high switching $\frac{dV}{dt}$ of the MOSFET.

Propagation delay: It is desirable that the IC to have minimum propagation delay. A good gate driver IC has a propagation delay below 200ns.

Output current: The output current of the gate driver IC is what charges the C_{gs} of the MOSFET leading to the turn ON of the MOSFET. Care should be taken that the Maximum drive current is less than the maximum output current of the IC. If there is a need for a higher driver current, current buffers can be utilized.

To meet the above requirements TI ISO5852S gate driver IC [9] was chosen. The IC can withstand a high CMTI of about 100kV/µs at a common voltage of 1500V, has a propagation delay ranging from 70ns to 110ns. The IC can handle maximum source and sink currents of 2.7A and 5.5A and respectively and can handle isolation voltage of 5700V. The fig 2.2 shows the schematic of the gate driver IC in Altium designer. The gate connection to the MOSFET is done with the help of coax pins to reduce the inductance.

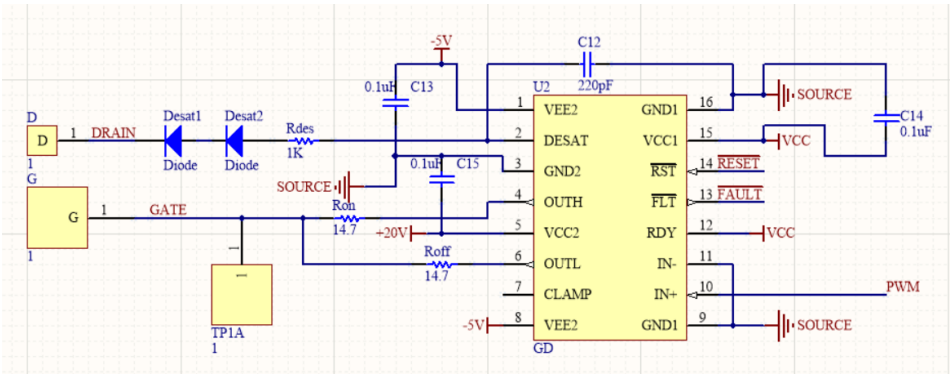


Fig 2.2. Schematic of the TI ISO5852SQDWRQ1 gate driver IC.

2.1.5 DESAT Protection

The DESAT protection feature of the gate driver IC makes it a more suitable choice as this ensure that the MOSFET has certain protection against short circuit.

The DESAT pin on the gate driver IC senses the drain source voltage (V_{ds}) across the device when the device is ON. This is done by connecting the DESAT pin to the drain of the MOSFET. A resistance of 1kOhm is connected in series to limit the transient currents during turn ON. A Schottky diode can be used to clamp the DESAT terminal to ground, which is optional.

When the device is turned ON, the diode conducts a forward current, which is used to sense the V_{ds} across the MOSFET and it also blocks the high voltage when the MOSFET is off. Therefore, the DESAT diode should be chosen such that it can withstand the high blocking voltage. More than one DESAT diode can be connected in series for the DESAT operation, but it should be made sure the sum of the forward voltage drops of the diodes do not exceed 9V for this gate driver IC. If the voltage exceeds 9V, the IC triggers the short circuit protection. The formula for DESAT triggering is given by:

$$V_{ds\_fault} = (9 - nV_f)\, V$$

During turn ON, the current rises first followed by the fall of the voltage across the device. The DESAT should not be allowed to operate in this time frame as it would lead to spurious turn off. In order to prevent this, a blanking capacitor is connected which ensures that there is some amount of banking time period. A blanking capacitor of 220pF is connected as recommended by the datasheet of the gate driver IC.

2.1.6 Optocoupler

Optocouplers are used to provide isolation between the gate driver and the control board. The signal from the controller can be sent through long optical fiber cables to the gate driver. This ensures that the control board can be kept at a safe distance so that it cannot be affected by the fast switching transients of the MOSFET and also ensures that it is not affected by EMI.

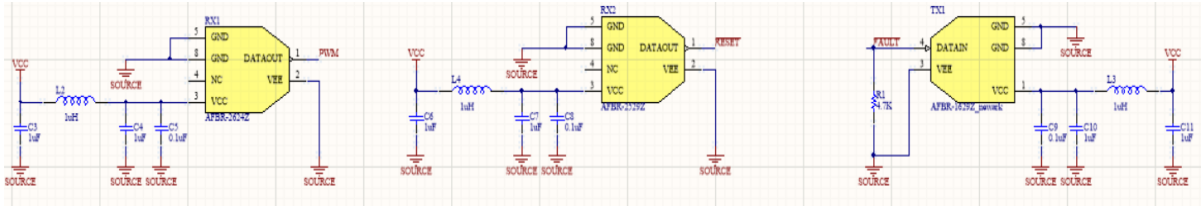


Fig 2.3. Schematic of the optocouplers used in the hate driver circuit.

The above figure (fig 2.3) shows the schematic of the three optocouplers employed for the gate driver. Rx1 and RX2 are receivers which receive the PWM signal and the reset signal from the control board respectively. The AFBR-2624z is the receiver optocoupler used in the gate driver [10]. TX1 is a transmitter which transmits the fault signal under such a situation to the control board. The AFBR-1624z is the transmitter optocoupler used in the gate driver [10].

2.1.7 PCB Layout

The gate driver PCB for the 3.3kV JBSFET was designed using the Altium design software. The layout of the PCB is given in the Fig 2.4. In the PCB, the top layer and the bottom

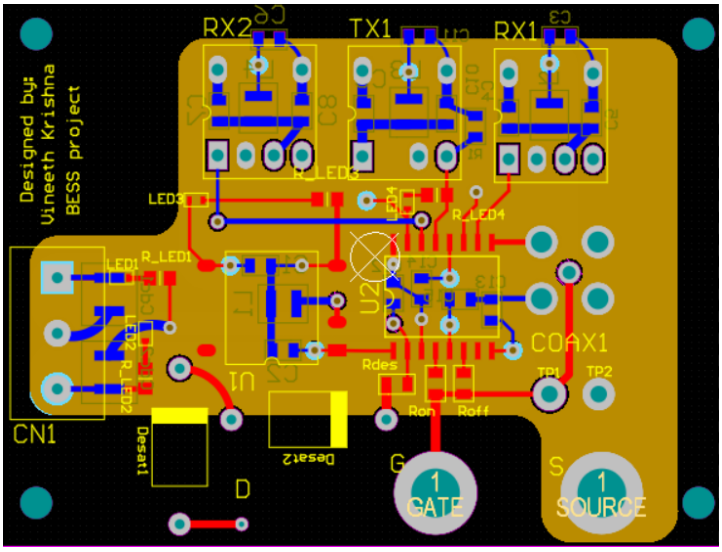


Fig 2.4. PCB layout of the Gate driver PCB in Altium.

layer are used to route the signal from the various parts on the PCB. One middle layer is used to route the source plane. The size of the source plane is maximized in order to minimize the inductance of the path. The second middle layer is used to route the power planes i.e. the +20V, +5V and -5V planes. Like the source plane, these power planes were also maximized in size in order to reduce the parasitic inductance in the PCB.

Gate loop inductance is the inductance due to the current path in the PCB layout. Care should be taken while designing the gate driver PCB to minimize this inductance. Since, SiC MOSFETs operate at high frequencies and have a high voltage handling capability, this leads to high values of $\frac{dV}{dt}$ and $\frac{dI}{dt}$. These high values of $\frac{dV}{dt}$ and $\frac{dI}{dt}$ should be kept in mind while designing a gate driver

PCB. The PCB was fabricated and was soldered with the chosen components. The picture of the complete soldered gate driver PCB is given in Fig 2.5.

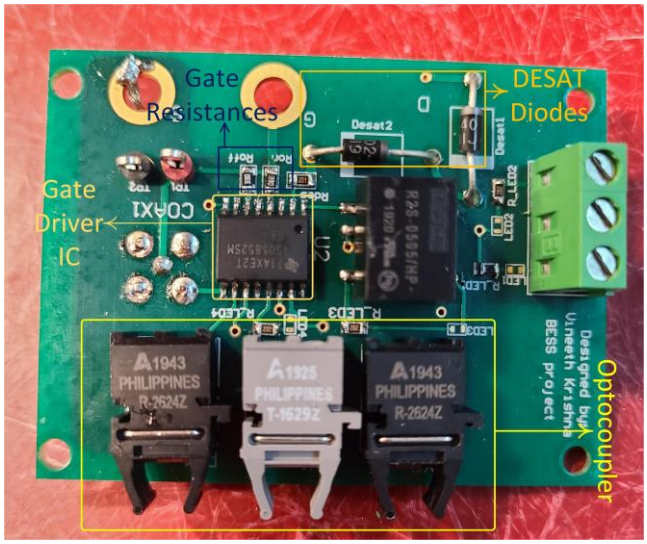


Fig 2.5. Gate Driver PCB soldered with the required components.

2.1.8 Gate Driver Power Supply

The gate driver requires a power supply so that it can produce the switching voltages (-5V/20V) to the gate driver IC in order to the drive the MOSFET and to also provide power to all the other peripherals on the gate driver board. Since, SIC MOSFETs require V_{gs} = +20V and V_{gs} = -5V, the power supply must provide these voltage levels to the gate driver IC in order to drive the SiC MOSFETs. The power supply must also have high voltage isolation and immunity towards high$\frac{dV}{dt}$, which SiC MOSFETs are known for.

To fit the above requirements, MGJ6D122005WMC-R7 [11] a power supply from Murata power solutions which has an isolation capacitance of 13pF has been chosen. It can provide the dual output voltages of +20V and -5V, has high $\frac{dV}{dt}$ immunity up to 80kV/µs and can provide isolation up to 10.2kV DC. The power supply was designed on a separate PCB along with

additional input filters which was recommended by the datasheet of the gate driver power supply the schematic, PCB layout and the fully soldered gate driver power supply PCB are given in the figures fig 2.6, fig 2.7 and, fig 2.8 respectively.

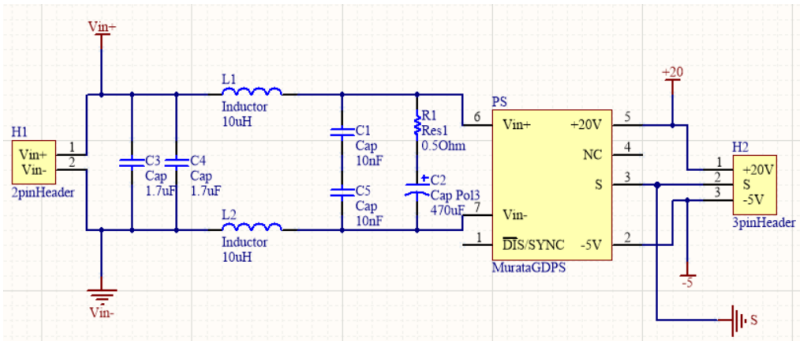


Fig 2.6. Schematic of the gate driver power supply on Altium.

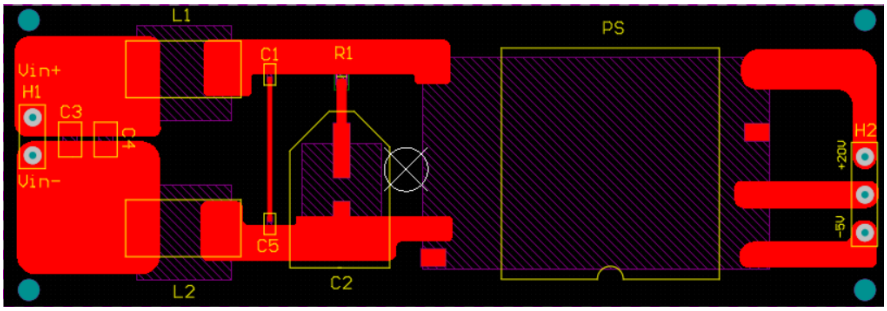


Fig 2.7. PCB layout of the gate driver power supply board on Altium.

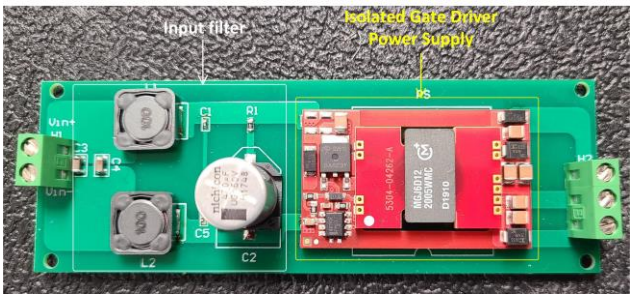


Fig 2.8. Gate Driver Power Supply PCB soldered with the required components.

2.2 Double Pulse Test

To describe the dynamic switching characteristics of the novel 3.3kV JBSFET a double pulse was performed on the device. From this test the switching loss, switching times and the dV/dt of the device can be determined. This test is performed at different operating points (different values of voltage and current) and at different temperatures in order to extract the switching characteristics in detail. The setup of the test is described below:

2.2.1 Circuit diagram

The figure Fig 2.9 describes the circuit diagram for the double pulse test. The circuit consists of a DC source, a decoupling capacitor to minimize the induction of the commutation loop of the circuit, an inductor, a diode which is realized by giving an OFF signal to another JBSFET of the same kind as that of the DUT and the DUT. The inductor and capacitor must be chosen such that they can handle all the operating conditions for which the device will be tested.

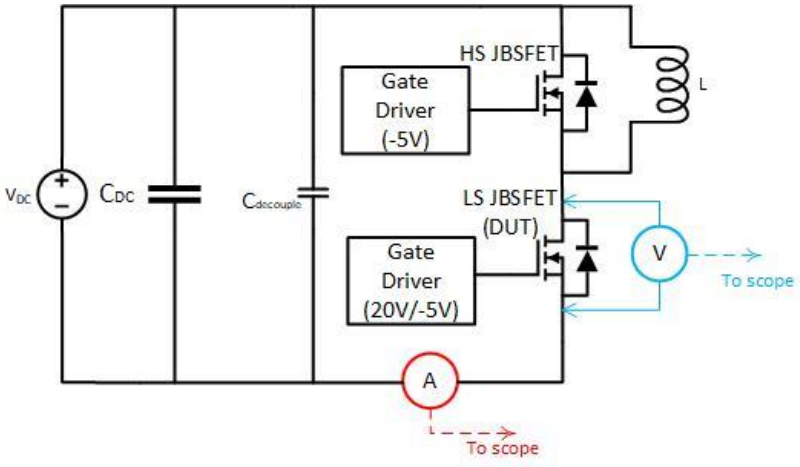


Fig. 2.9 Circuit Diagram of the Double Pulse Test.

2.2.2 Capacitor selection

The Double Pulse test circuit consists of two sets of capacitor namely the decoupling capacitor and the DC link capacitor.

Decoupling Capacitor: The decoupling capacitor used in the circuit has two functions which are to supply the transient current and to minimize the loop inductance present in the circuit. This loop inductance causes voltage overshoot in the device under turn-off condition. According to [12], a decoupling capacitor value of 250 times the device's output capacitance (C_{OSS}) should suffice this function.

According to the datasheet of the device, the JBSFET has a C_{OSS} of 160pF. Therefore, a decoupling capacitor with the capacitance of 40nF should be able to mitigate the device overshoot. In the circuit, two WIMA 1µF film capacitors [13] are connected in parallel to realize a decoupling capacitance of 2µF. Two 1µF capacitors are connected in parallel to minimize the ESR of the capacitor as a high ESR would inject voltage ripple in the circuit.

DC link capacitor: The DC link capacitor limits the variation of the DC bus voltage in the circuit. The DC link capacitance is chosen by using the following formula [14]:

$$C_{DC} = \frac{LI_L^2}{2k_v V_{DC}^2}$$

Where, C_{DC} is the DC link capacitance, I_L is the inductor current, L is the inductance of the inductor used in the DPT circuit, k_v is the voltage ripple coefficient which is typically chosen to be in the range of 1% to 5%, V_{DC} is the DC bus voltage. The capacitance used in the circuit should be chosen such that it is higher than the worst case condition capacitance from the above equation. From the above condition, the worst-case capacitance was calculated to be 126 µF. The capacitance chosen for the circuit is 120 µF.

2.2.3 Circuit operation

In the double pulse test experiment, 2 pulses are given in succession to the device under test which are the instances that the device is turned ON.

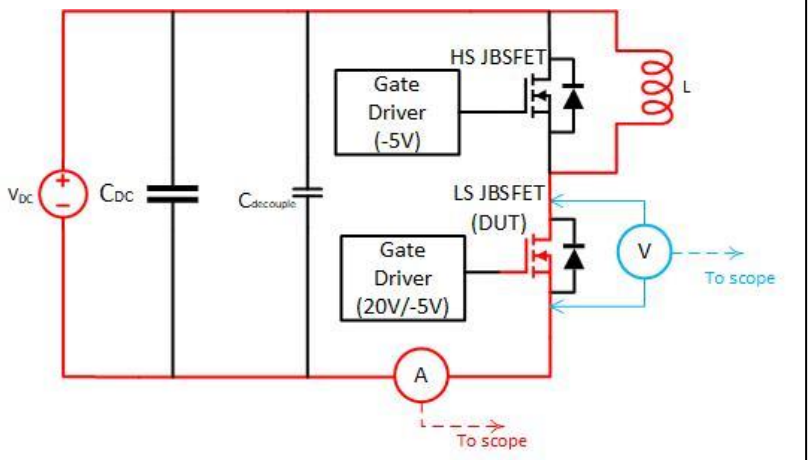


Fig 2.10. State of the DPT circuit when the JBSFET is ON.

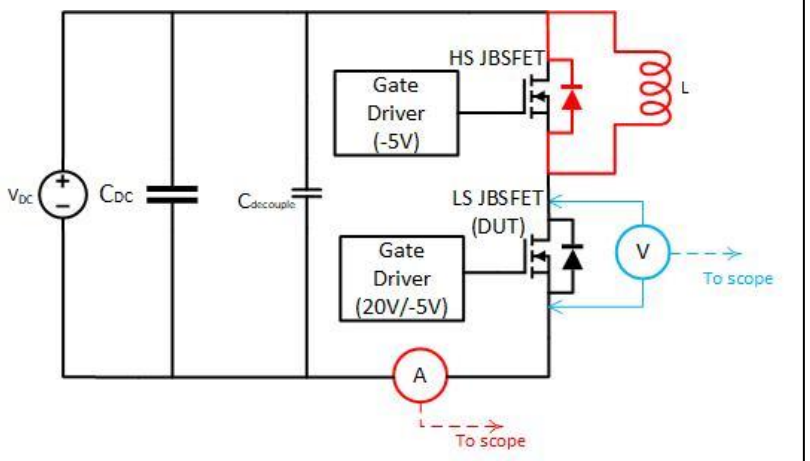


Fig 2.11. Status of the DPT circuit when the JBSFET is OFF

The duration of the pulse is determined by the inductance of the inductor used in the test circuit and the operating point current and voltage. The formula of the pulse duration is given by the following equation:

$$t_{pulse} = \frac{LI_{op}}{V_{op}}$$

Where, t_{pulse} is the time duration of the pulse given to the DUT in order for the current to build up to the operating point current, I_{op} is the operating point current at which the device is being tested and V_{op} is the operating point DC voltage from the DC source at which the device is being tested.

When the first pulse is given, the current in the device is builds up to a value equal to the operating point current. When this value of current is reached the device is turned OFF for a short duration. In this short duration the current flows through the inductor via the free-wheeling diode. This turn-off is the event where the turn-off energy loss of the device is calculated. The device is turned on again after the short duration. In this short duration, the current through the inductor remains constant which is at the value of the operating point current. Therefore, the turn-on energy loss of the device is calculated at this event.

2.2.4 Experimental Results

The Double Pulse Test was performed on the 3.3kV JBSFET at voltages of 500V, 1000V, and 1500V and currents of 10A, 20A, and 30A. The device is subjected to junction temperatures of 25^{o}C, 75^{o}C, and 125^{o}C. An external gate resistance (gate resistance of the gate driver) of 33Ω is used and the device has an internal gate resistance of 1.6Ω. An inductor of 7 mH was used in the experiment which had a parasitic capacitance of 9 nF. The high side switch which acts as a diode in the circuit, also contributes to some capacitance in the circuit, whose value is 145.7 pF. The setup of the experiment is given in fog. 2.12.

The experimental results were observed using the LeCroy scope. The 2kV voltage probes were used to sense the drain-source voltage across the device, 30A current probe was used to record the flow of current through the device. The experimental waveforms recorded for the experiment for one of the operating points is given in the fig. 2.13:

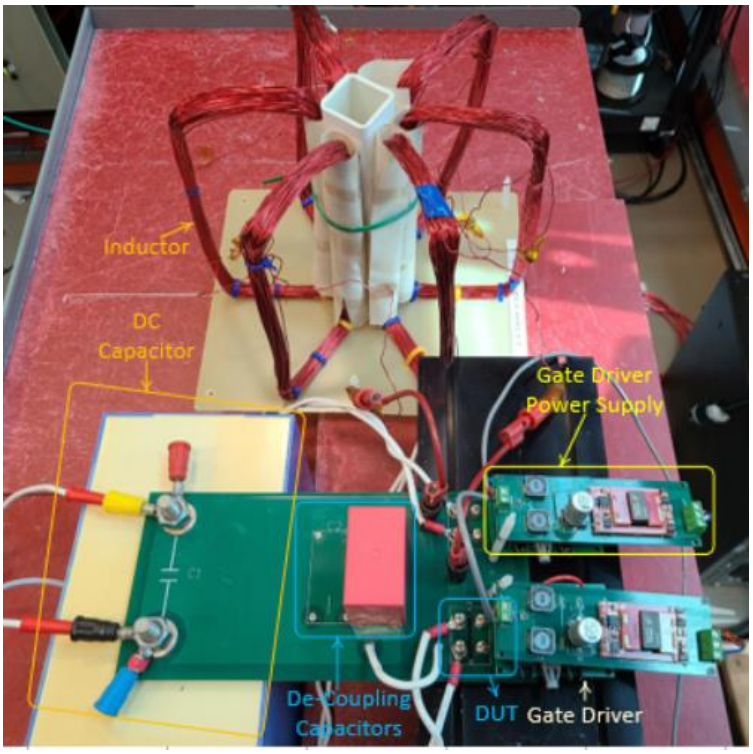


Fig 2.12. Experimental setup for the double pulse test.

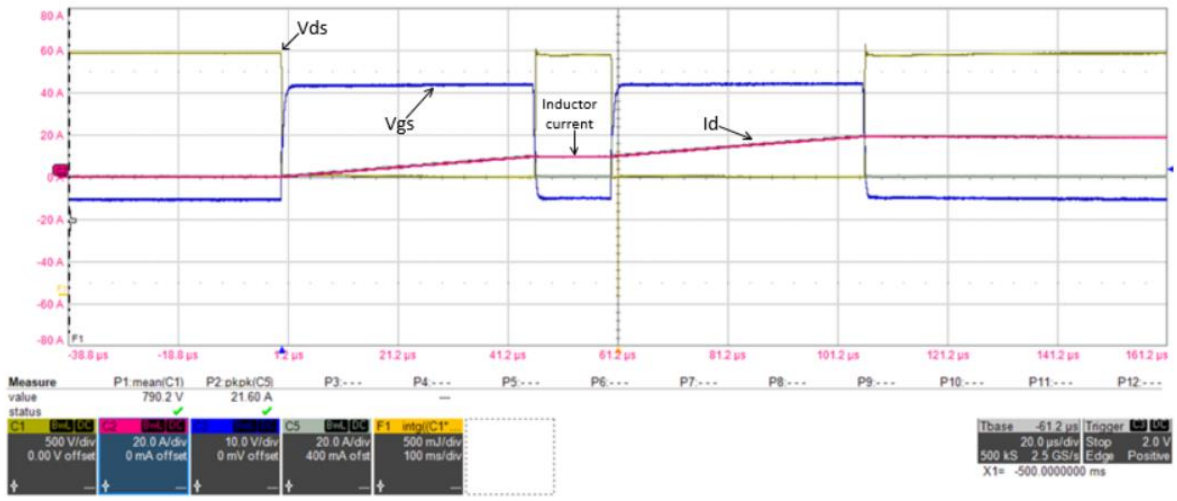
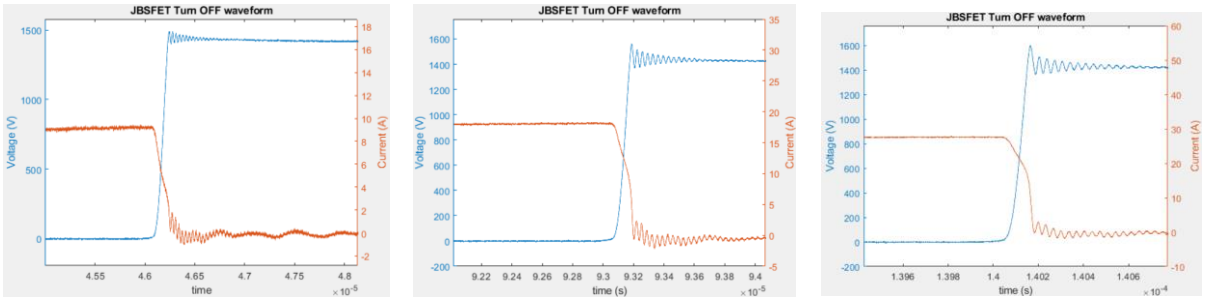


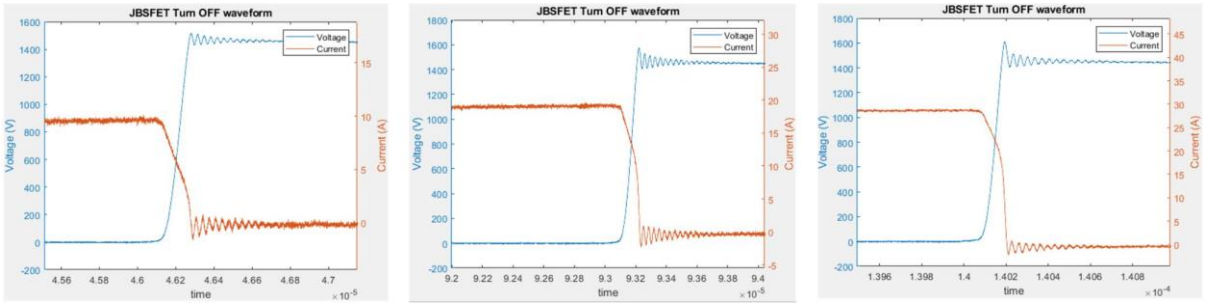
Fig 2.13. Experimental waveform of the double pulse test of the 3.3kV JBSFET at V_{DS} = 1500V, I_{DS} = 10A, T_j = 25°C and R_g = 33Ω.

The drain-source voltage data and the drain-source current data from the double pulse test experiment were extracted and were analyzed in MATLAB. Using this data on MATLAB, the switching loss of the JBSFET at different operating points and temperature was determined. The zoomed in switching waveforms of the JBSFET at V_{DS} of 1500V at 25^{o}C and 125^{o}C and at the values of current of 10A, 20A, and 30A are plotted in MATLAB and are shown in figures fig 2.14, fig 2.15, fig 2.16 and fig 2.17, respectively.



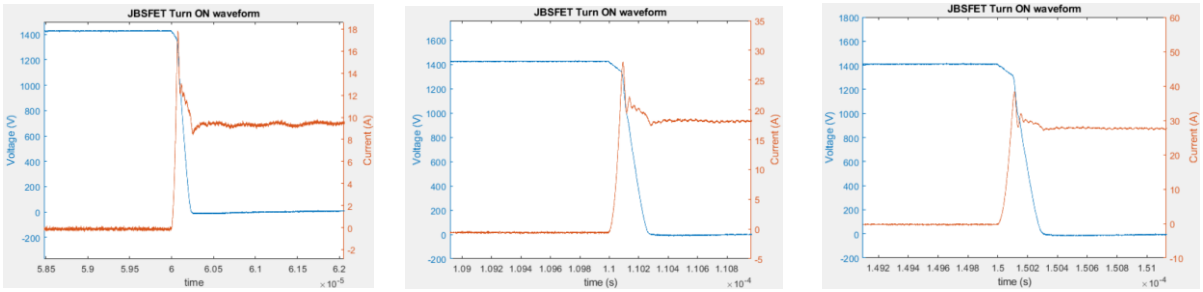
a) b) c)

Fig 2.14. Experimental Turn-OFF waveforms for JBSFET at Vdc = 1500V, Tj = 25^{o}C, Rg = 33Ω for Ids of a.) 10A, b.) 20A and c.) 30A.



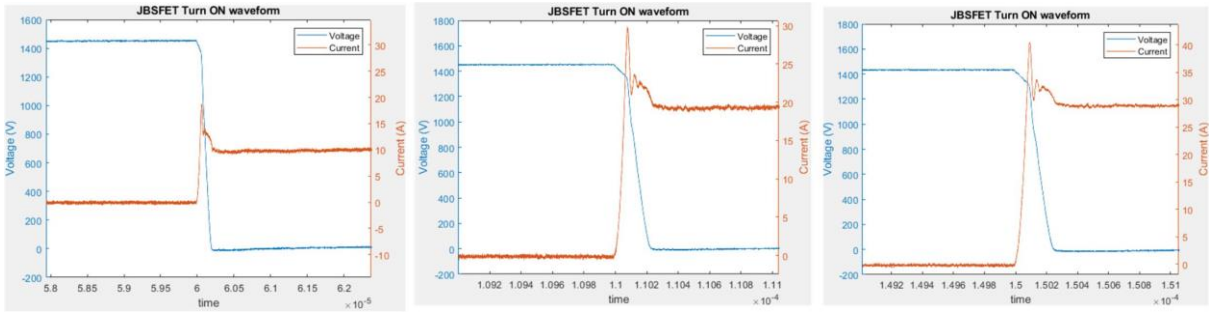
a) b) c)

Fig 2.15. Experimental Turn-OFF waveforms for JBSFET at Vdc = 1500V, Tj = 125^{o}C, Rg = 33Ω for Ids of a.) 10A, b.) 20A and c.) 30A.



a) b) c)

Fig 2.16. Experimental Turn-ON waveforms for JBSFET at Vds = 1500V, Tj = 25ºC, Rg = 33Ω for Ids of a.) 10A, b.) 20A and c.) 30A.



a) b) c)

Fig 2.17. Experimental Turn-ON waveforms for JBSFET at Vds = 1500V, Tj = 125ºC, Rg = 33Ω for Ids of a.) 10A, b.) 20A and c.) 30A.

The turn-off and turn-on energy losses for the device is calculated by the formula:

$$E_{ON/OFF} = \int_{t1}^{t2} V_{DS}(t)\, I_{DS}(t) dt$$

Where, $E_{ON/OFF}$ is the turn-on or turn-off energy loss, $V_{DS}(t)$ is the drain-source voltage of the JBSFET, $I_{DS}(t)$ is the drain-source current flowing through the JBSFET, t1 is the time at which the switching event begins and t2 is the time at which the switching event ends. The turn-off energy loss for the device was calculated for all the operating points and at all temperatures and was tabulated in the table below:

Table 2.2. E_{OFF} losses obtained from the Double Pulse Test.

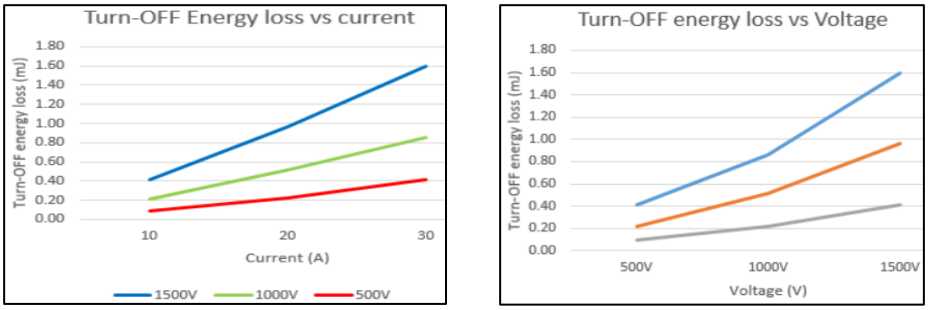
DOUBLE PULSE TEST RESULT ($R_{g(ext)}$ = 33, $R_{g(int)}$ = 1.6)			
Eoff (mJ) for 3.3kV JBSFET at 25°C			
Voltage\Current	**10A**	**20A**	**30A**
500V	0.11	0.28	0.43
1000V	0.25	0.45	0.73
1500V	0.41	0.91	1.40
Eoff (mJ) for 3.3kV JBSFET at 75°C			
Voltage\Current	**10A**	**20A**	**30A**
500V	0.09	0.19	0.42
1000V	0.22	0.50	0.83
1500V	0.42	0.96	1.60
Eoff (mJ) for 3.3kV JBSFET at 125°C			
Voltage\Current	**10A**	**20A**	**30A**
500V	0.09	0.22	0.41
1000V	0.22	0.52	0.86
1500V	0.41	0.96	1.60

The turn-on energy loss of the device was calculated for all operating points and for all the different device junction temperatures and is tabulated in the table below:

Table 2.3. E_{ON} losses obtained from the Double Pulse Test.

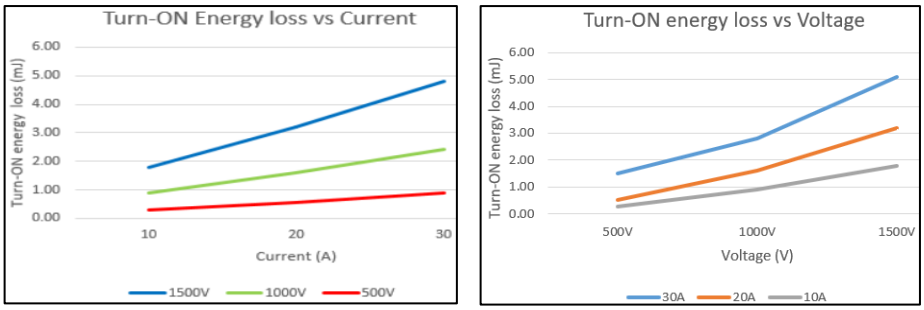
DOUBLE PULSE TEST RESULT ($R_{g(ext)}$ = 33, $R_{g(int)}$ = 1.6)			
Eon (mJ) for 3.3kV JBSFET at 25°C			
Voltage\Current	**10A**	**20A**	**30A**
500V	0.47	0.94	1.50
1000V	0.91	1.40	2.80
1500V	1.90	3.40	5.10
Eon (mJ) for 3.3kV JBSFET at 75°C			
Voltage\Current	**10A**	**20A**	**30A**
500V	0.29	0.48	0.68
1000V	0.94	1.70	2.50
1500V	1.90	3.50	5.20
Eon (mJ) for 3.3kV JBSFET at 125°C			
Voltage\Current	**10A**	**20A**	**30A**
500V	0.29	0.54	0.88
1000V	0.89	1.60	2.40
1500V	1.80	3.20	4.80

The above tables contain the switching turn-OFF energy loss and the switch turn-ON energy loss of the device under various operating conditions. From the above obtained experimental data, we can now see the variation of turn-OFF/ON energy loss with variation of current and voltage. These variations are given in fig.



a) b)

Fig 2.18. Variation of turn-OFF energy loss a) with I_{DS} at different V_{DS}, b) with V_{DS} at different I_{DS} at 125^{o}C T_j.



a) b)

Fig 2.19. Variation of turn-ON energy loss a) with I_{DS} at different V_{DS}, b) with V_{DS} at different I_{DS} at 125^{o}C T_j.

From the above data we can create a thermal model for the device in PLECS simulation software and analyze the losses in the converter as well as the rise in the junction temperature of the JBSFET. This will help in designing an appropriate heat sink for the given system. From the test we also find the turn-ON and turn-OFF times of the device and also the switching slew rate. These values have been found for the device and have been tabulated below:

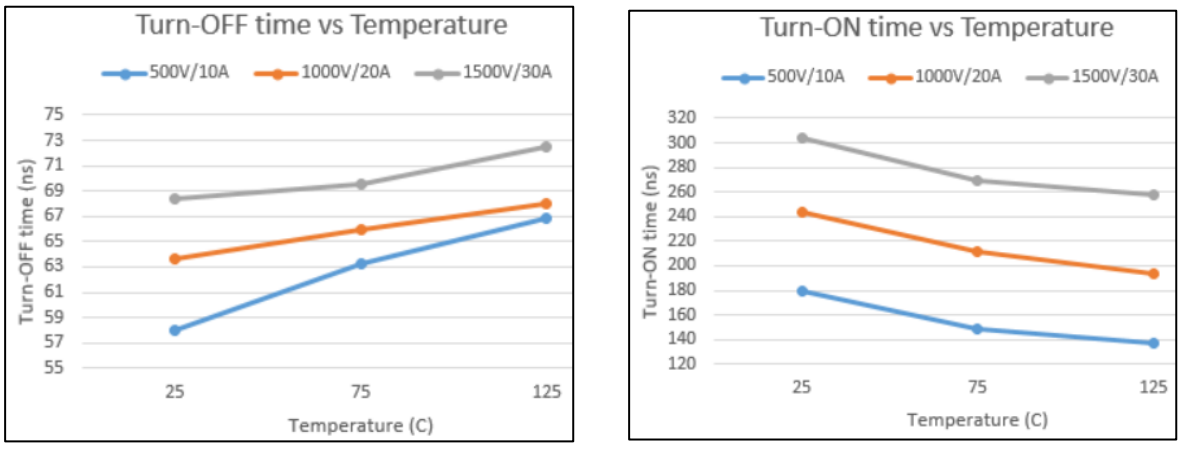
Table 2.4. Turn-off times and dv/dt of the JBSFET at all operating points.

Temperature 25°C		
Operating point	**t_{OFF} (ns)**	**dV/dt (V/ns)**
500V/10A	58	9.55
500V/20A	45.9	13.65
500V/30A	41.7	16.03
1000V/10A	84	11.56
1000V/20A	63.6	16.18
1000V/30A	57.2	18.39
1500V/10A	98.4	14.83
1500V/20A	76.2	20.19
1500V/30A	68.4	22.92
Temperature 75°C		
Operating point	**t_{OFF} (ns)**	**dV/dt (V/ns)**
500V/10A	63.2	7.33
500V/20A	49.9	10.01
500V/30A	45.8	11.13
1000V/10A	98.4	9.75
1000V/20A	66	15.37
1000V/30A	58.8	17.44
1500V/10A	99.2	14.98
1500V/20A	79.4	19.41
1500V/30A	69.6	23.11
Temperature 125°C		
Operating point	**t_{OFF} (ns)**	**dV/dt (V/ns)**
500V/10A	66.8	7.23
500V/20A	51.2	10.52
500V/30A	46.8	12.49
1000V/10A	84.4	11.35
1000V/20A	68	14.81
1000V/30A	60.4	17.43
1500V/10A	101.2	14.5
1500V/20A	83.3	18.56
1500V/30A	72.5	21.62

Table 2.5. Turn-on times and dv/dt of the JBSFET at all operating points.

Temperature 25°C		
Operating point	**t_{ON} (ns)**	**dV/dt (V/ns)**
500V/10A	178.8	2.79
500V/20A	208	2.32
500V/30A	314.4	1.66
1000V/10A	220.8	4.2
1000V/20A	244	3.74
1000V/30A	294.8	3.07
1500V/10A	236.8	6
1500V/20A	276.8	5.12
1500V/30A	303.6	4.62
Temperature 75°C		
Operating point	**t_{ON} (ns)**	**dV/dt (V/ns)**
500V/10A	149.2	2.84
500V/20A	160	2.49
500V/30A	216	1.85
1000V/10A	180.8	5.03
1000V/20A	212	4.28
1000V/30A	249.6	3.59
1500V/10A	214.5	6.71
1500V/20A	247.6	5.85
1500V/30A	269.2	5.32
Temperature 125°C		
Operating point	**t_{ON} (ns)**	**dV/dt (V/ns)**
500V/10A	137.6	3.2
500V/20A	154	2.85
500V/30A	202.4	2.24
1000V/10A	174.9	5.28
1000V/20A	193.2	4.69
1000V/30A	221.6	4.06
1500V/10A	204	7.1
1500V/20A	232	6.2
1500V/30A	258	5.54

From the above data we can find how the turn-ON and turn-OFF times change with change in the operating temperature of the device. The variation of the switching times of the device at an different operating points is shown in the graphs below:



a) b)

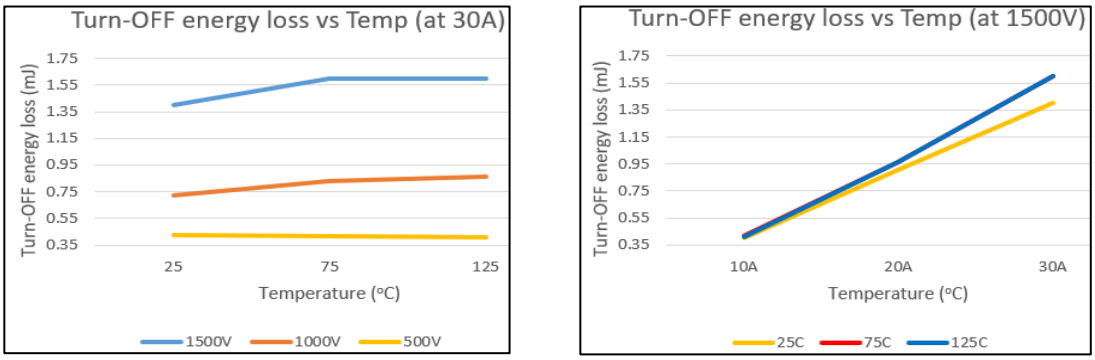
Fig 2.20. Variation of a) turn-OFF time with temperature, b) Variation of turn-ON time with temperature at different operating points.

From the above graphs we can see how the turn-ON time for the device reduces with increase in temperature. The turn-ON time of the device reduces with the increase in temperature as shown in fig.4. This is due to the temperature dependent nature of the transconductance of SiC MOSFETs. As the temperature increases the transconductance of the MOSFET increases as well. This causes the miller voltage of the device to decrease for the given load current as the relationship between the miller voltage and the transconductance is given by:

$$V_{miller} = \frac{I_L}{g_m}$$

Where, V_{miller} is the miller voltage of the MOSFET, I_L is the load current flowing through the MOSFET and gm is the transconductance of the device. This decrease in miller voltage reduces the turn-ON time of the JBSFET. This reduction of the turn-ON time results in the reduction of the switching loss of the JBSFET [15]. This is shown in the graph shown in figure fig 2.21 where,

the turn-ON loss is plotted against the junction temperature of the JBSFET at different drain-source voltages at 30A current and at different drain-source currents at 1500V.



a) b)

Fig. 2.21. Variation of device turn-off energy loss with T_j at a) different V_{DS} with I_{DS} = 30A, b) different I_{DS} with V_{DS} = 1500V.

Similarly, we can see that the turn-off energy loss of the JBSFET increases as the junction temperature of the device increases very slightly. This is shown in the graph shown in fig 2.22 where, the turn-OFF loss is plotted against the junction temperature of the JBSFET at different drain-source voltages at 30A current and at different drain-source currents at 1500V.

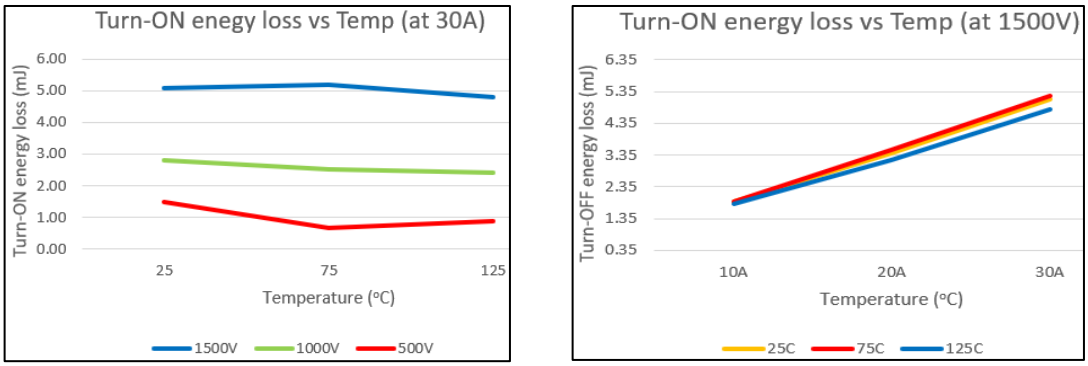


Fig 2.22. Variation of device turn-on energy loss with T_j at a) different V_{DS} with I_{DS} = 30A, b) different I_{DS} with V_{DS} = 1500V.

Therefore, the variation of the total switching energy loss of the JBSFET would not vary much with temperature as compared to a Si MOSFET because the variation in turn-ON and turn-OFF loss opposes each other. This reduces the thermal requirement for a SiC MOSFET or JBSFET compared to that of a Si MOSFET. The total switching energy loss of the JBSFET is plotted against temperature in fig 2.23 for different values of voltages at 30A current.

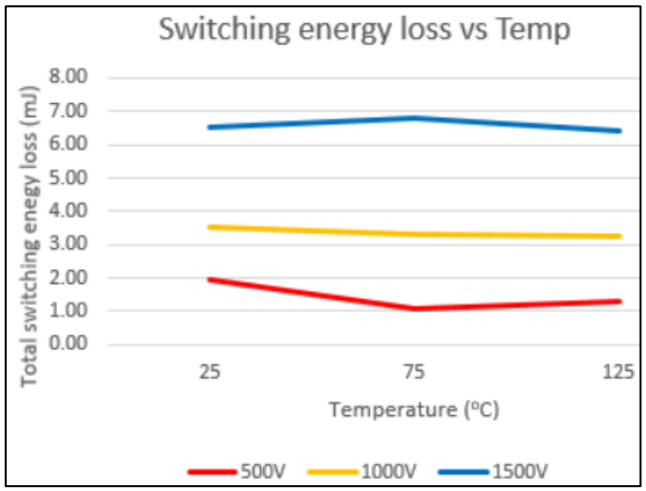


Fig 2.23. Variation of total switching loss against junction temperature for 500V, 1000V, and 1500V at 30A current.

CHAPTER 3

SINGLE-PHASE OPERATION

To verify the working of the inverter, the 3-phase photo-voltaic inverter is operated as a single-phase inverter. This way, we can also test the operation of each of the poles of the inverter. The single-phase inverter was tested by connecting it to an RL load. The schematic of the single-phase inverter is shown in fig 3.1.

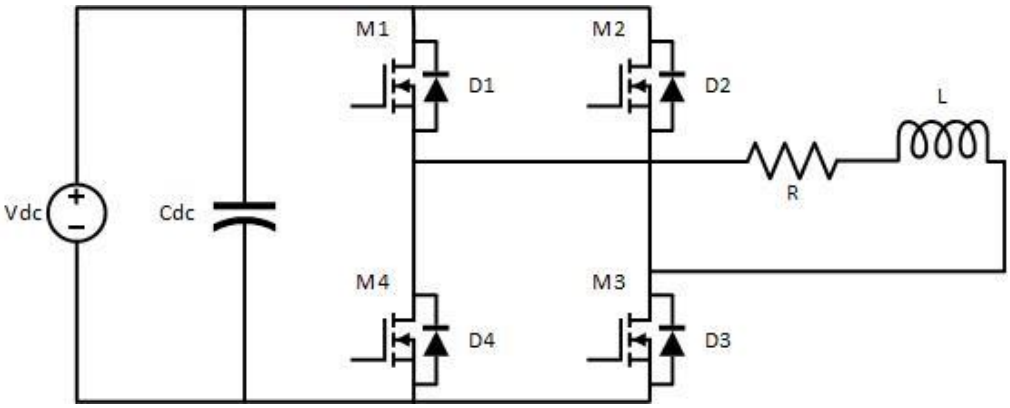


Fig 3.1. Circuit diagram of the single-phase inverter.

The parameters for which the single-phase inverter was tested is shown below:

Table 3.1. Parameters of the single-phase inverter.

Parameter	Values
Input Voltage (V_{in})	1500 V
DC link capacitor (C_{dc})	120 µF
Load Resistance (R_l)	47 Ω
Load Inductance (L_l)	20 mH
Switching frequency (f_{sw})	10 KHz
Line frequency (f_l)	60 Hz
Power factor (pf)	0.98

3.1 Pulse Width Modulation of Single-phase inverter

A DC constant input voltage is converted into a sinusoidal AC output by the use of a full-bridge inverter. The power switches in the single-phase inverter are turned ON and OFF in a certain manner in order to obtain the sinusoidal voltage of desired magnitude and frequency. An AC output voltage of desired magnitude and frequency can be obtained by the use of various PWM schemes. The most common inverter switching schemes are the square wave operation and the sine-triangle PWM.

3.1.1 Square wave operation

In the square wave operation, the gating signals to the JBSFETs of the full-bridge inverter are squares waves whose width is 180^o in time period of the frequency of the fundamental of the output voltage waveform. This is similar to the square wave operation of the half-bridge inverter. The single-phase inverter is basically two half poles operated together where the two half-poles are operated 180^o apart.

Therefore, in a single-phase inverter which comprises of four switches, two opposite switched of the two poles are operated simultaneously. Hence, both the switches are turned ON at the same time and are turned OFF at the same time. For example in fig.1 the switches M1 and M3 are turned operated simultaneously and the switches M2 and M4 are switch simultaneously. The total output voltage of the full-bridge inverter can be found by subtracting the output voltages of the two half-poles. The output voltage of a half-pole is given by:

Since, the two half-poles are operated with a phase difference of 180^o, the total output voltage of the full-bridge inverter is given by:

This mode of operation of the inverter has several disadvantages. One of them being that the output voltage waveforms has harmonics that distort the output voltage waveform. In addition to that the value of the output voltage cannot be controlled. Therefore, this method is recommended if the input DC voltage of the inverter is adjustable as the only method to change the magnitude of the output voltage is by changing the input DC voltage of the inverter.

3.1.2 Sine-triangle PWM

In the sine-triangle PWM, a modulating wave is compared with a carrier wave and the resulting signals obtained from the logical comparison of the two waves form the gating signals of the power switches of the inverter [16]. The modulating wave is of the same shape of that of the ideal output voltage waveform. Here, since the ideal output waveform in a single phase inverter is a sine wave, therefore, the modulating wave is a sine wave which of the same frequency of the output.

The carrier wave is a high frequency triangle wave. The frequency of the triangular carrier wave is the same as the switching frequency of the inverter. The magnitude of the output voltage can be controlled by the ratio of the magnitude of the peak of the modulating wave with that of the carrier wave. This ratio of known as the modulation index of the SPWM scheme [16]. The waveforms of the SPWM scheme is shown in fig 3.2 where $V_{control}$ is the modulation wave and V_{tri} is the triangular carrier wave.

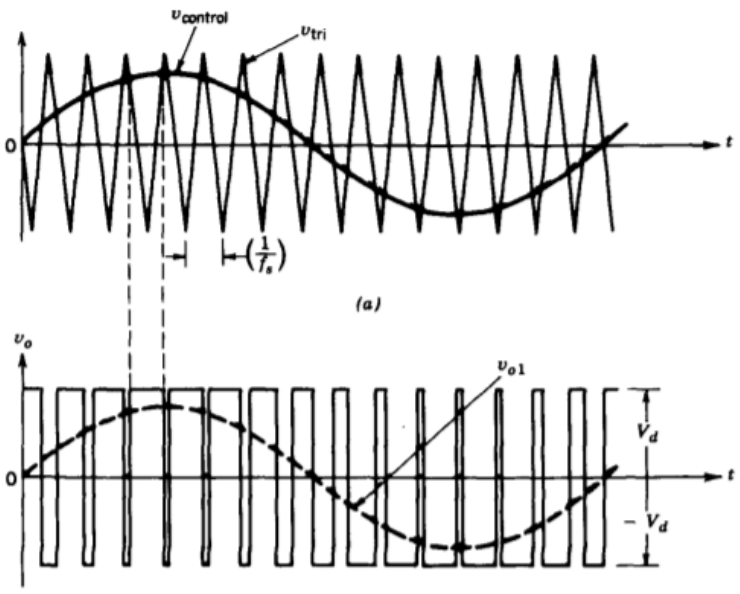


Fig 3.2. The single-phase SPWM modulation and the carrier waves [16].

As mentioned earlier, in SPWM a sine wave modulation wave is compared with a high frequency triangle wave. By this comparison the state of the inverter switches can be determined. When the modulation wave is greater than the carrier wave, the top switch in a inverter pole is ON and when the modulating wave is less than the carrier eave, the bottom switch of the inverter pole is on. This scheme can be summarized as follows:

Table 3.2. Switching logic behind the SPWM scheme.

PWM status	Pole switch status		Pole voltage
	Top switch	Bottom switch	
$V_{modulation} > V_{carrier}$	ON	OFF	$0.5V_{DC}$
$V_{modulation} < V_{carrier}$	OFF	ON	$-0.5V_{DC}$

The resultant pole voltage using SPWM is shown in figure in solid line. As you can see the resulting pole voltage is a square wave with a varying duty cycle where the duty cycle variation is

sinusoidal. Filtering the pole voltage, we can obtain the sinusoidal fundamental pole voltage. The magnitude of the fundamental voltage is given by:

$$V_{o1} = m\frac{V_{DC}}{2}$$

Where, V_{o1} is the fundamental output pole voltage, V_{DC} is the input DC voltage for the pole and m is the modulation index of the SPWM scheme given by:

$$m = \frac{V_{modulation}}{V_{carrier}}$$

Where, $V_{modulation}$ is the peak of the modulating wave and $V_{carrier}$ is the peak voltage of the carrier wave. Since, the modulation wave is a sine wave, the fundamental of the output pole voltage is also of the same shape as that of the modulation wave whose instantaneous value is given by the equation:

$$V_{o1} = \frac{mV_{DC}}{2}\sin\omega t$$

For a full bridge single wave inverter, the two poles are given the PWM signals which are 180^o in phase apart. Therefore, the resultant output voltage of the fundamental of the single-phase inverter is:

$$V_{o1} = mV_{DC}\sin\omega t$$

Where mV_{DC} is the magnitude of the output fundamental voltage. From this we can obtain the rms value of this output voltage by dividing the magnitude of the fundamental output voltage by the crest factor of the output waveform. Since, the output waveform is a sine wave whose crest factor is$\sqrt{2}$, the rms of the output fundamental voltage is given by:

$$V_{o1(rms)} = \frac{mV_{DC}}{\sqrt{2}}$$

The magnitude of the output voltage under SPWM switching scheme is lower in comparison to the square wave switching scheme described earlier. But in SPWM, the lower order harmonics are pushed to higher frequency. Hence, allowing us to easily filter out the harmonics present in the output voltage of the inverter. Unlike the above method, the output voltage of the inverter can be controlled by changing the modulation index of the modulating wave used in SPWM [16]. The SPWM scheme can also be further modified to eliminated certain harmonics present in the output voltage and can also increase the magnitude of the output voltage by modifying the modulation wave of used in SPWM. In this thesis, a basic implementation of the SPWM is used.

3.1.3 Implementation of SPWM in a microcontroller

The SPWM has been realized for the single-phase inverter has been realized with the help of a microcontroller. The microcontroller from Texas Instruments TMS320F28069 [17] which has a 90MHz has been used. The TMS320F28069 microcontroller is shown in the fig 3.3.

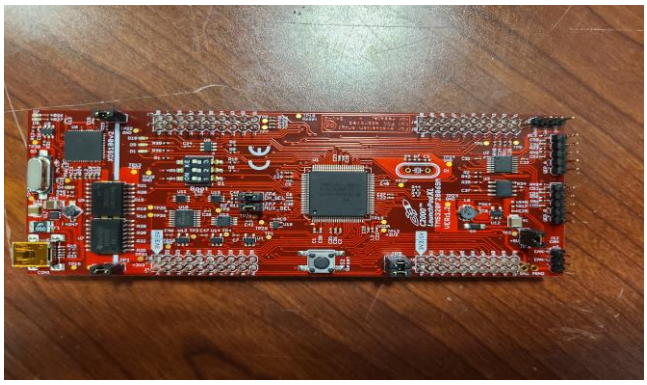


Fig 3.3. TMS320F28069 microcontroller used to implement SPWM algorithm.

The PWM waveforms were obtained with the help of the enhanced PWM (ePWM) registers of TMS320F28069. With the help of the ePWM registers the frequency of the carrier

wave, the duty cycle of the waveforms and the dead-time of the waveforms. Since, the duty cycle of the SPWM waveforms keep varying, interrupts were used to update the duty cycle of the waveforms. The duty cycle of the waveforms were updated at start of every cycle of the carrier frequency. The flowchart of the implementation of the SPWM in the microcontroller is given in fig 3.4.

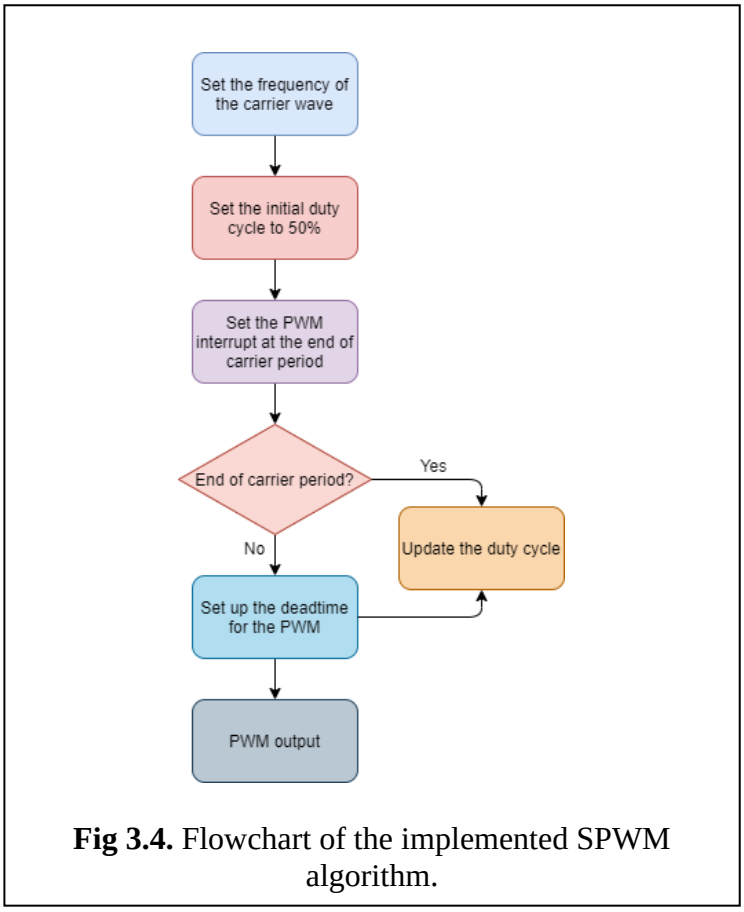


Fig 3.4. Flowchart of the implemented SPWM algorithm.

3.2 Simulation Result

The design of the single-phase inverter was verified by simulating the system in PLECS simulation software. The simulation diagram is given in fig. 3.5.

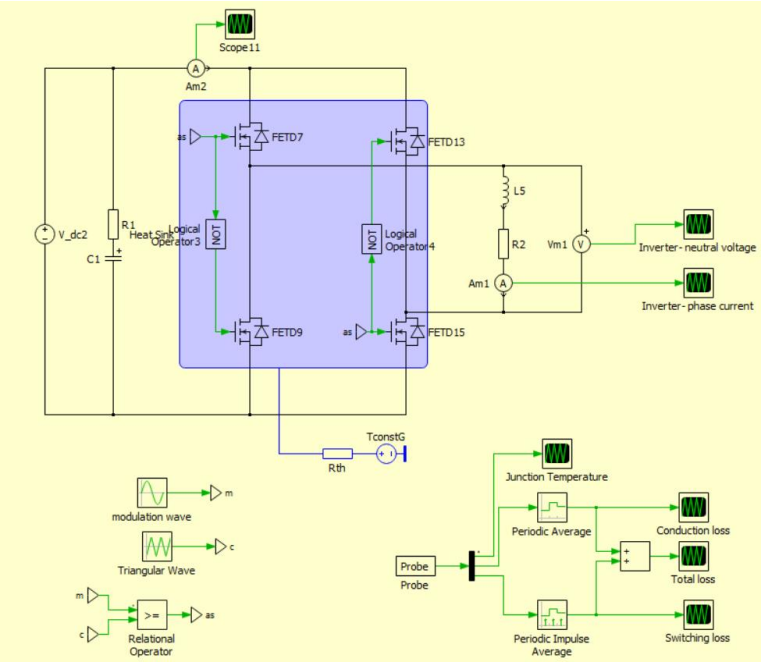


Fig 3.5. Simulation diagram of the single-phase inverter in PLECS.

In the above simulation, the transistors of the inverter are given gate pulses through the sine-triangle pulse width modulation technique. The gate pulses of the JBSFETs of the two poles are 180^{o} apart. From the above simulation the output voltage and current were obtained

3.2.1 Output Phase voltage

The waveform of the output phase voltage is given in the fig 3.6. In the above obtained output voltage waveform, we can see that the voltage is a square wave whose values varies from -1500V to 1500V and is not a clean sinusoidal AC voltage waveform due to harmonics present in

the output voltage. The pulse width of each of the pulse is varying due to the adoption of the sine-triangle PWM technique.

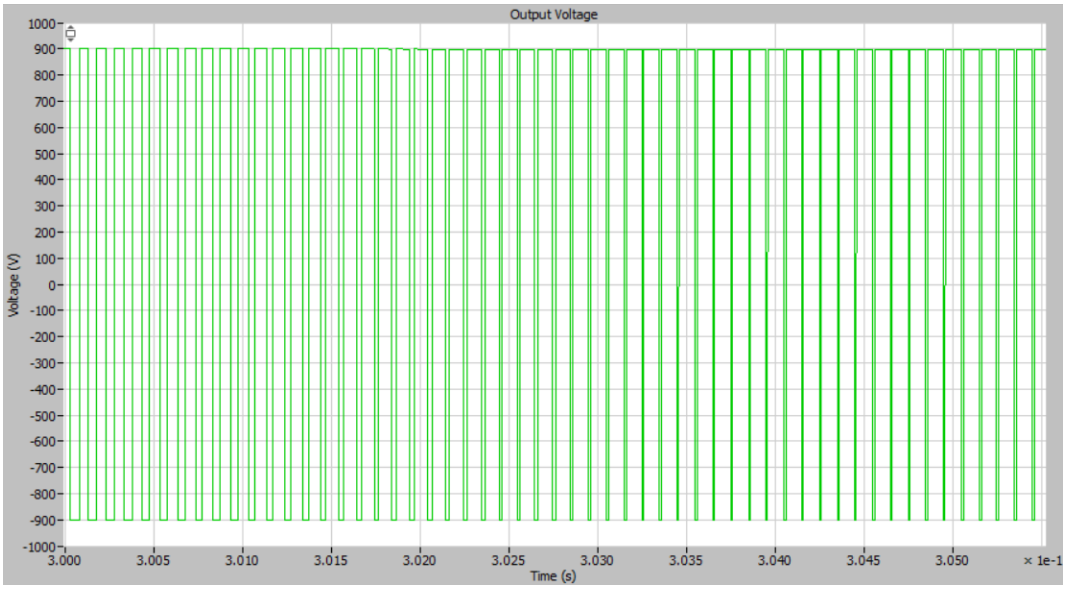


Fig 3.6. Output voltage waveform of the single-phase inverter with V_{DC} = 900 V, m = 0.5, f_{sw} = 10 kHz, f_l = 60 Hz.

3.2.2 Output Phase current

The obtained output phase current is sinusoidal in nature due to the inductor present in the load. This load inductor acts as a filter and filters out the harmonics present in the phase current waveform. The output phase current waveform is shown below:

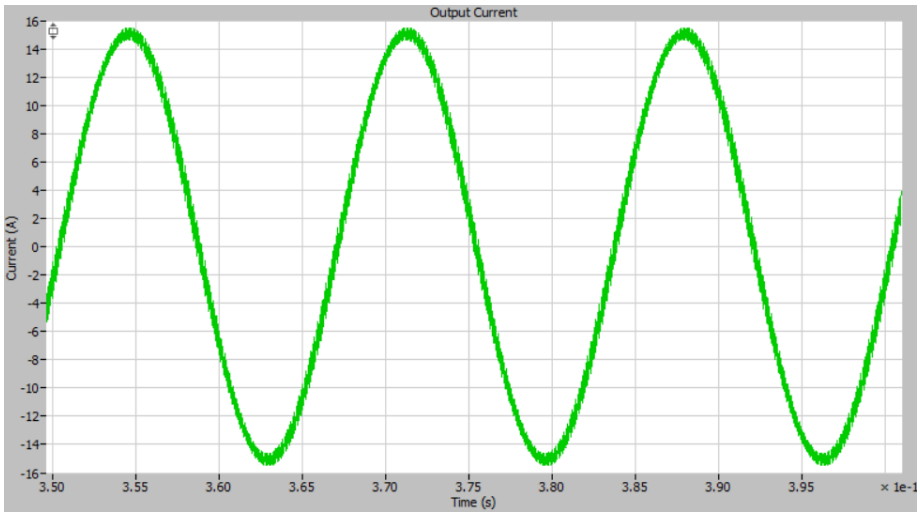


Fig 3.7. Output current of the single-phase inverter obtained at V_{DC} = 900 V, m = 0.5, f_{sw} = 10 kHz, f_l = 60 Hz, where I_{RMS} = 6.65 A.

3.3 Experimental Result

The operation of the single-phase inverter was verified experimentally by operating the three-phase inverter as a single-phase inverter in the setup. To do so only 2 of the poles on the PCB are utilized. The diagram of the single-phase inverter is shown in figure 3.8.

For the experiment, the keysight Scope and voltage probes were used to verify the PWM received by the gate drivers of the JBSFET. The gate drivers receive the PWM signals from the microcontroller through optical fibers. The PWM signal from the microcontroller varies for 0V/5V where 0V is for turn-OFF and 5V is for turn-ON. An electrical to optical converter board (e20 board) is used to convert these electrical PWM signals into optical signals which are then transmitted to the gate drivers through the optical fibers. The gate drivers then receive this PWM signal and then transform this signal to a PWM signal of -5V/20V to switch the JBSFET on and off in accordance with the PWM signal it receives.

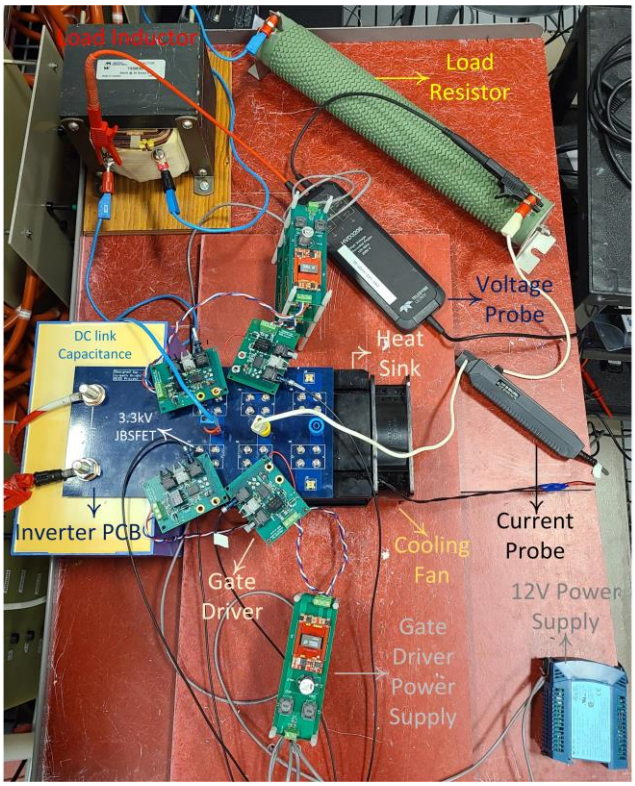


Fig 3.8. Experimental setup of the single-phase inverter.

The load for the inverter was realized by using a Hammond 195m30 [18] 20 mH inductor and a 47 Ω resistor. The LeCroy Scope is used to record the output voltage and current waveforms of the inverter. The HVD3206 [19] high voltage differential probe rated at 2000V is used for recording the output voltage of the inverter. The CP031A [20] 30A LeCroy probe is used for the recording the output pole current. The single-phase inverter was energized using a high voltage magna power supply. The single-phase inverter was tested up to 900V. From operating the inverter, the following results were obtained from the LeCroy scope which is shown in fig 3.9.

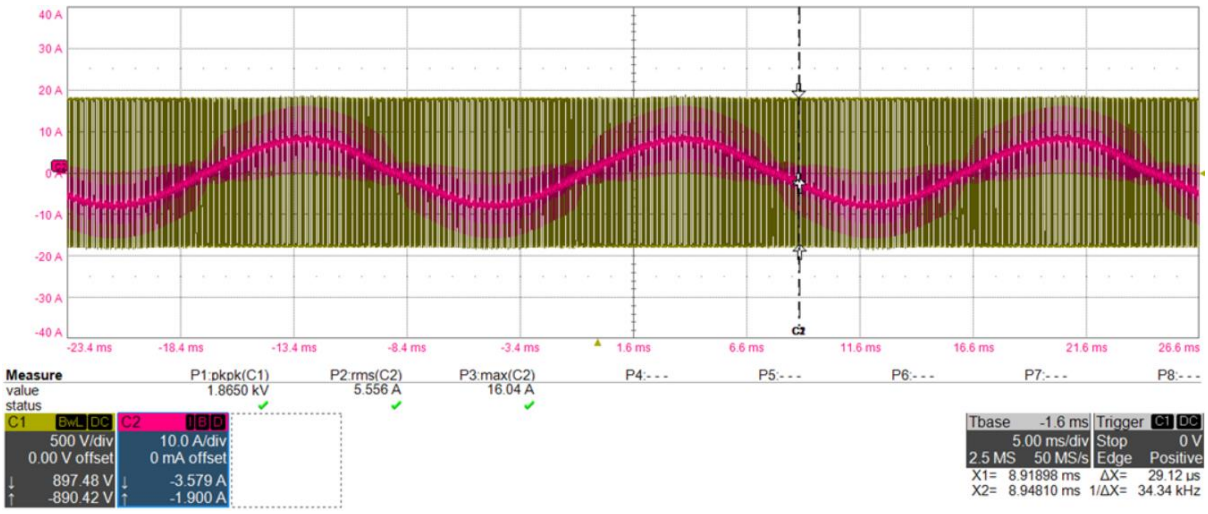


Fig 3.9. Experimental Output voltage and current waveforms of the single-phase inverter tested at V_{DC} = 900 V, m = 0.5, I_{RMS} = 6.65 A, f_{sw} = 10 kHz, f_l = 60 Hz.

CHAPTER 4

THREE PHASE PHOTOVOLTAIC INVERTER

The motivation of development of JBSFET is to reduce the losses associated with the SiC MOSFET in the third quadrant region of operation. As mentioned earlier, the JBSFET has a JBS diode as the anti-parallel diode which dissipates less losses as compared to the body diode of a SiC MOSFET. Due to this the device can be used in numerous amounts of bi-directional power converters. One of the main areas of applications of these devices is the photovoltaic converter.

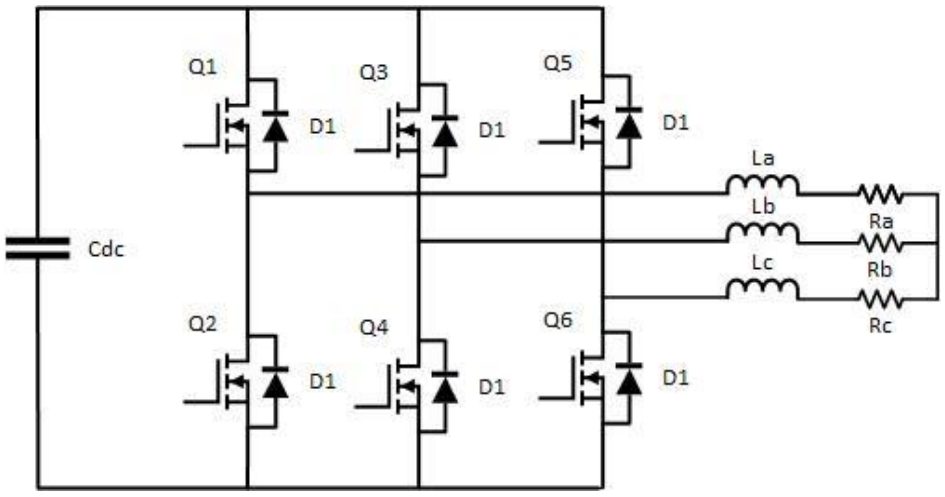


Fig 4.1. Schematic of the three-phase photovoltaic inverter.

The advantages of this device in a 1500V rated photovoltaic converter were described in chapter 1 of the thesis. Thus, JBSFET is utilized in developing a 1500V three-phase photovoltaic inverter whose schematic is given in fig 4.1. The three-phase inverter was developed and was tested up to 1500V with the parameters given in table 4.1.

Table 4.1. System parameters of the three-phase inverter.

Parameter	Values
Input Voltage (V_{in})	1500 V
DC link capacitor (C_{dc})	120 µF
Load Resistance (R_l)	20 Ω
Load Inductance (L_l)	20 mH
Switching frequency (f_{sw})	10 KHz
Line frequency (f_l)	60 Hz
Power factor (pf)	0.95

4.1 PCB Design

To develop the prototype of the designed three-phase inverter, the three-phase inverter was developed on a PCB. The PCB was designed by carefully taking the inverter parameters into consideration. The PCB was designed as per the IPC-2221 design standards which is accepted throughout the world for PCB designs in commercial and industrial applications. The schematic of the PCB is given below:

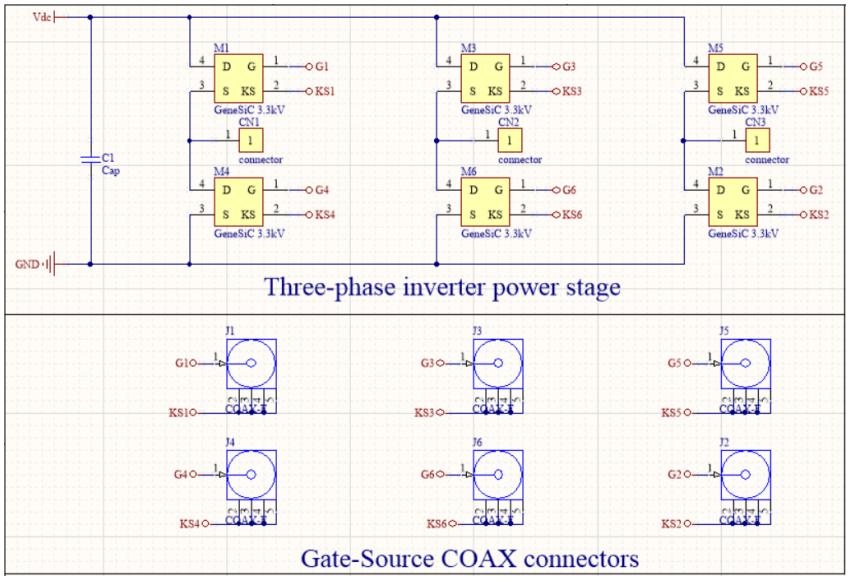


Fig 4.2. Schematic of the photovoltaic string inverter PCB on Altium.

The schematic of the inverter has two parts, the power stage which is the main circuitry of the three-phase inverter and the gate-source COAX connectors to give the PWM switching signals to the JBSFET. The top and bottom layers of the PCB of the photo-voltaic inverter are shown below in fig 4.3 and fig 4.4.

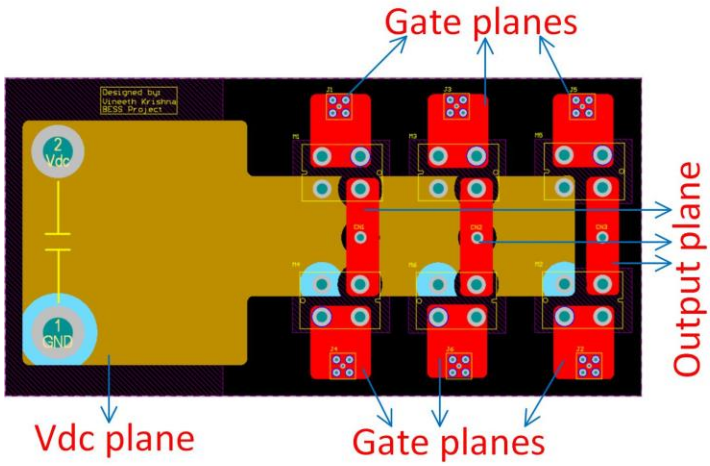


Fig 4.3. Top layers of the inverter PCB depicting the gate planes and the output planes in layer 1 (red) and V_{DC} plane on layer 2 (green).

The three-phase photo-voltaic inverter PCB is a four-layer PCB and careful consideration of the clearances and the stray inductances were taken while designing the planes on the PCB. There are three main planes present in the PCB and the design of these planes and the PCB is discussed as follows:

Power plane: The power planes namely the Vdc plane and the ground plane were maximized to reduce the amount of stray inductance of the plane. Both the planes are drawn exactly on top of each other to further minimize the stray inductance. It is required to have good voltage isolation between the layers so as the two layers would have a large potential difference between them.

Therefore, the planes were drawn in the in-between layers of the PCB (Layer 2 and Layer 3) because of the FR-4 present in between the layers which provides good amount of voltage isolation between the planes.

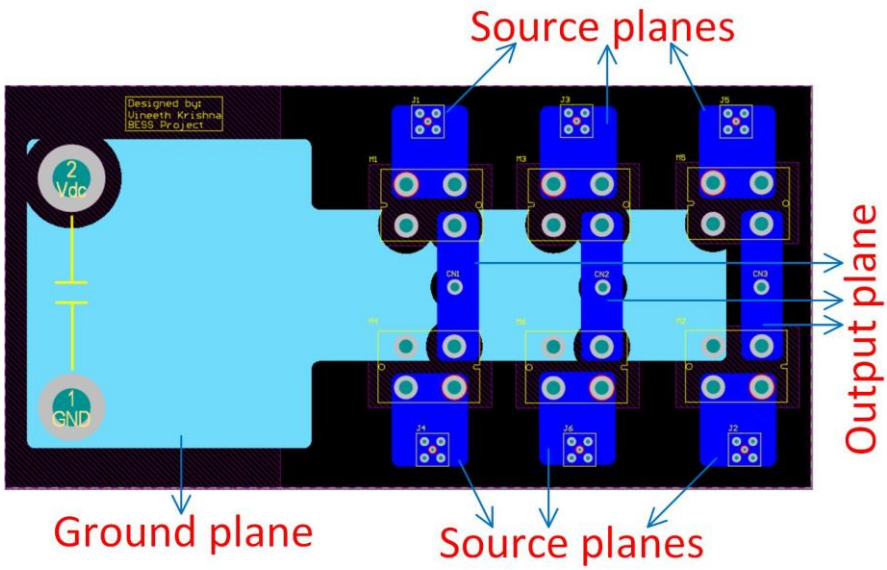


Fig 4.4. Bottom layers of the inverter PCB depicting the Ground plane in layer 3 (Light blue) the source planes and the output planes layer 4 (Blue).

Another careful consideration with regards to designing high voltage PCBs is the corona production. Corona discharge is a common failure mechanism in high voltage printed circuit boards. The corona discharge causes failure of the insulation material in the PCBs. The main causes of corona discharge in a high voltage PCB is the sharp corners of the PCB planes when drawn on the PCBs. In order to mitigate these effects in the PCB, the high voltage planes have been drawn not with a sharp corner but with a rounded corner. This way the area of the corners of the power planes is increases thus mitigating the corona discharge effect.

Signal Plane: The gate plane and the source plane make up the signal planes in the PCB. These two planes in the PCB are used to provide the JBSFET of the inverter with the turn-ON and

turn-OFF signals from the gate driver. The gate-source signal is given from the gate driver to the JBSFET through the COAX pins places on the PCB. This is done so as to minimize the inductance of the gate-source path between the PCB and the JBSFET. To further mitigate the effects of the stray inductance of the gate-source path, the gate and source signal planes were drawn as a polygon pour rather than connecting the gate and source terminals of the JBSFET directly to the COAX connection through a thin PCB trace. The gate and the source planes were also drawn to the same size and are placed directly on top of each other to further minimize the effects of inductance.

Output plane: The output plane of the inverter is the plane from which we obtain the AC output from the inverter PCB. The output plane is formed by connecting the source of the top JBSFET to the drain of the bottom of the JBSFET. The thickness of the trace is maintained such that it is wide enough to carry the required output current and also at the same time have enough distance between the two due to maintain voltage isolation. Each phase of the inverter has two output planes, one on the top layer of the PCB and one at the bottom layer of the PCB. Therefore, the current stress on each output trace is reduced.

4.2 DC link capacitor design

In a photovoltaic string inverter, the DC power is provided by either an energy storage element or a DC/DC converter. The output of either of the stages in a PV power plant may contain some unwanted voltage ripples, which decrements the performance of the inverter. Hence, to mitigate this DC input voltage ripple, a DC link capacitor is utilized as shown in fig. 4.5. In a DC/AC converter, the input power is fed to the inverter through a DC link capacitor. The purpose of using this DC link capacitor is to minimize any ripple in the input DC voltage of the inverter and to also supply the input power to the inverter. Therefore, while selecting a DC link capacitor

for an inverter appropriate calculation must be done in order to choose a capacitor which can minimize the voltage ripple and to supply the three-phase inverter with the DC power.

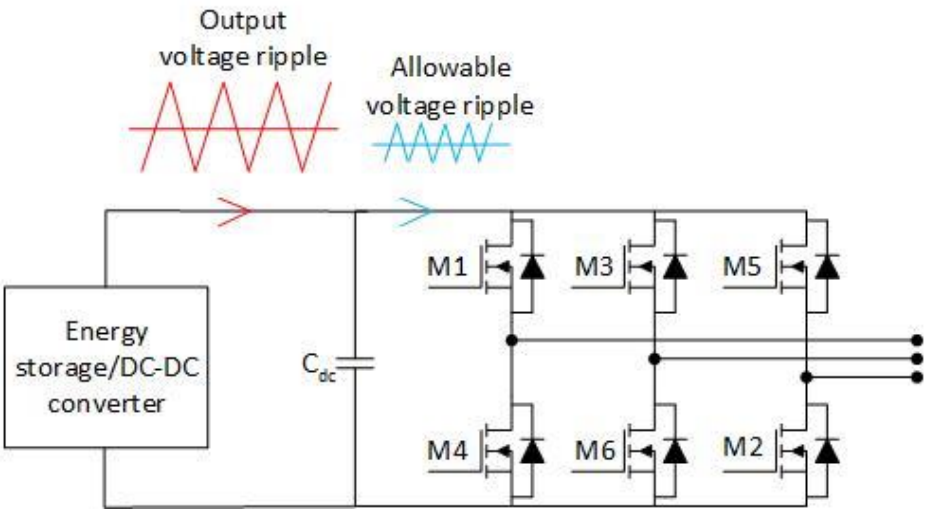


Fig 4.5. Mitigation of voltage ripple by the DC link capacitor in a photovoltaic converter.

In order to choose the capacitor, we must first calculate the rms current of the capacitor. We can obtain this value of capacitor rms current from the rms output phase current of the three-phase inverter, the modulation index of the SPWM used to operate the inverter and the power factor of the load. Knowing the above quantities, the capacitor rms current can be calculated by the equation [21]:

$$I_{CAP(rms)} = I_{ph(rms)} \sqrt{2m\left[\frac{\sqrt{3}}{4\pi} + \left(\frac{\sqrt{3}}{\pi} - \frac{9m}{16}\right)cos^2\varphi\right]}\ A$$

Where, $I_{CAP(rms)}$ is the rms capacitor current, $I_{ph(rms)}$ is the output phase current of the inverter, m is modulation index of the SPWM and cos φ is the power factor of the load of the inverter. Using the above equation, the capacitor rms current was found to be 12.022A. With this value of the capacitor current we can now find the value of the DC link capacitor that is needed to operate the inverter by the following equation [21]:

$$C_{min} = \frac{I_{CAP(rms)}}{V_{ripple} * 2\pi f_{sw}}$$

Where, C_{min} is the minimum value of capacitance of the DC link capacitor, $I_{(CAP)rms}$ is the rms capacitor current, V_{ripple} is the allowable voltage ripple across the capacitor and f_{sw} is the switching frequency of the power devices used in the three-phase inverter. Therefore, from the above equation the minimum value of the DC link film capacitor for a voltage ripple of 5% and 10% and is tabulated in table 4.2.

Table 4.2. Required DC-link capacitor values for the 3-phase converter.

V_{Ripple} (%)	**Capacitor Value**
5	2.5 µF
10	1.2 µF

The chosen capacitor must also be able to maintain the applied Dc bus voltage and the capacitor current. Knowing the ratings the LNK-P9X-120-350 film capacitor from ICAR was chosen which has a capacitance of 120 µF and can handle a DC bus voltage of 3500V and a max rms current $I_{CAP(rms)}$ of 150A [22]. The chosen DC link capacitor is shown in fig 4.6. With the DC-link capacitor chosen for the converter, we can now calculate the inertia of the converter which is given by the formula:

$$H = \frac{CV^2}{2(VA)}$$

Where C is the capacitance of the DC-link capacitor, VA is the input power rating for the converter. The inertia of the designed converter is found to be 7 ms.

Fig 4.6. DC link capacitor of the photovoltaic string inverter.

4.3 Pulse Width Modulation of the Inverter

For the three-phase photovoltaic string inverter to convert the constant DC voltage of the energy storage system into an AC sinusoidal voltage, the JBSFETs in the converter need to switch ON and OFF in a particular fashion through the application of the appropriate gating signals from the gate driver. There are several methods to switch the JBSFETs in a three-phase inverter in order to generate a sinusoidal voltage. The most common methods are the 180^{o} conduction, 120^{o} conduction, and the sine-triangle pulse Width modulation (SPWM).

The SPWM for the three-phase inverter was implemented similarly as to the method described in chapter 3. The only difference being that there are three modulation sine waves which are 120^{o} degree in phase apart from each other at the line frequency of about 60Hz.

4.4 Heat sink design

Due to the continuous operation of the converter, the temperature of the JBSFET increases due to the dissipation of the device power loss. In order to maintain the temperature of the string inverter to a suitable level, a heat sink is utilized to dissipate heat from the inverter efficiently. A

heat sink with a suitable value of thermal resistance is chosen. The steady-state junction temperature of the JBSFET during continuous operation is given by [23]:

$$T_j = T_a + P_{loss}R_{ja}$$

Where, R_{ja} is the junction to ambient thermal resistance, T_j is the junction temperature, T_a is the ambient temperature of the environment and P_{loss} is the rate of heat dissipation or the total power loss of all the six switches of the inverter. The junction to ambient thermal resistance of the system is given by the equation [23]:

$$R_{ja} = R_{jc} + R_{cs} + R_{sa}$$

Where, R_{jc} is the junction to case thermal resistance of the device, R_{cs} is the case to heat sink thermal resistance and R_{sa} is the heat sink to ambient thermal resistance. R_{jc} of the device is determined by the device package and is given as 0.26 $^oC/W$. The case to heat sink thermal resistance R_{cs} is determined by the thermal compound used to attach the device on to the heat sink. R_{sa}

The ambient temperature is chosen as 25^oC and the junction temperature is chosen as 75^oC. Therefore, with the total power loss calculated before, the required total thermal resistance R_{ja} is found to be 0.27. Therefore, the required thermal resistance of the heat sink can be found by the equation Hence, the chosen heat sink must have a thermal resistance of 0.23 or of lesser value. Lower the value of thermal resistance, lower is the rise in the junction temperature which allows the inverter to be operated safely at a safe temperature.

To satisfy the above requirement, the heat sink 392-180AB from Wakefield-Vette shown in figure 4.7 is chosen. The chosen heat sink has a thermal resistance of 0.43 $^oC/W$ [24]. Since, this heat sink is has a higher thermal resistance than required, a cooling fan is used to further reduce the thermal resistance of the heat sink. A cooling fan from Qualtek, FAA1-12038NBMW31 shown

in figure Fig 4.8 with an effective CFM of 87 is chosen [25]. Therefore, with the use of this cooling fan, the thermal resistance of the heat sink effective thermal resistance of the heat sink can be found using its datasheet. Therefore, the thermal resistance of the heat sink reduces to 0.12 which is well below the required value.

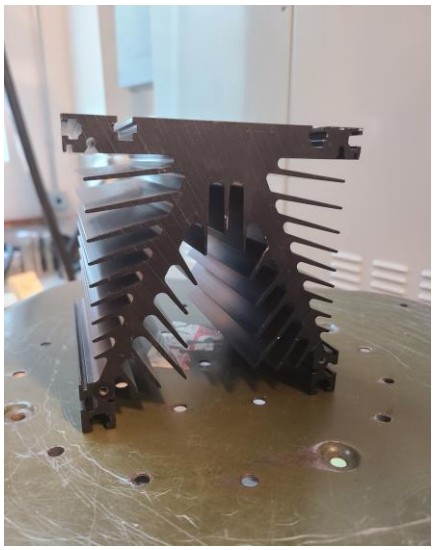


Fig 4.7. Image of the heat sink used to dissipate JBSFET losses.

Fig 4.8. Cooling fan used to further reduce the thermal resistance of the heat sink.

4.5 Simulation results

From the theoretical design of the inverter, a simulation model of the three-phase PV string inverter was designed in PLECS simulation software. Also, from the double pulse test, the turn-ON and turn-OFF losses obtained of the JBSFET from chapter 2 was used to build a thermal model of the device in PLECS. The model of the PV inverter on PLECS is given in fig. The inverter is placed on a heatsink which is marked by the blue boundary in fig 4.9. Through this heat sink we can perform thermal simulation of the three-phase inverter and evaluate the conduction loss and the switching loss of the JBSFETs in the circuit. We can also obtain the rise in the junction temperature of the transistors and the heat sink.

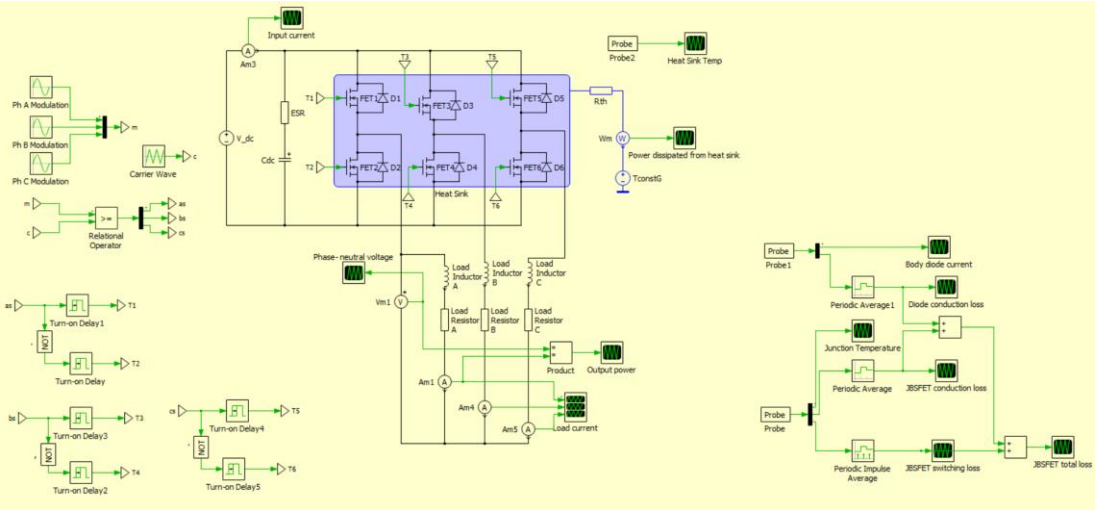


Fig 4.9. Schematic of the photovoltaic inverter in PLECS.

The losses present in the devices are evaluated by the PLECS simulation software by including the thermal description of the JBSFET which was obtained by the double pulse test which was discussed in detail in chapter 2. Through the thermal description and the appropriate periodic averaging, the switching loss and the conduction loss of the JBSFET is obtained. From the above performed simulation of the three-phase PV inverter using a JBSFET, the following results were obtained.

4.5.1 Output phase voltage

The output phase to neutral voltage of the three-phase inverter obtained from the simulation is shown in fig 4.10. In the obtained waveform, the phase to neutral voltage is varying sinusoidal but it is not purely sinusoidal due to the harmonics present in the voltage waveform. The frequency of this waveform is equal to the line frequency which is equal to 60Hz.

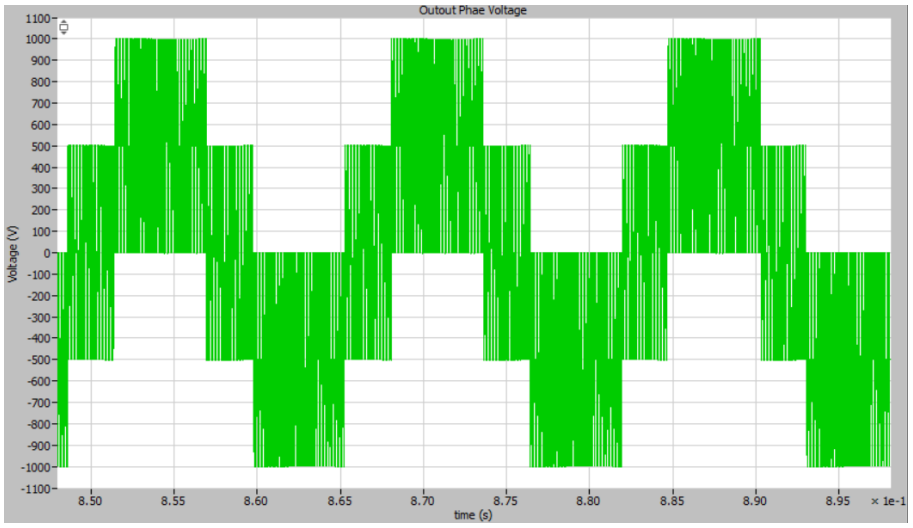


Fig 4.10. Output phase voltage of the PV inverter at V_{DC} = 1500V, m = 0.8, f_{sw} = 10 kHz, f_l = 60 Hz.

This can further be verified by the Fourier spectrum of the above waveform shown in the fig 4.11. Where, the magnitude of the 60Hz frequency component is the highest and

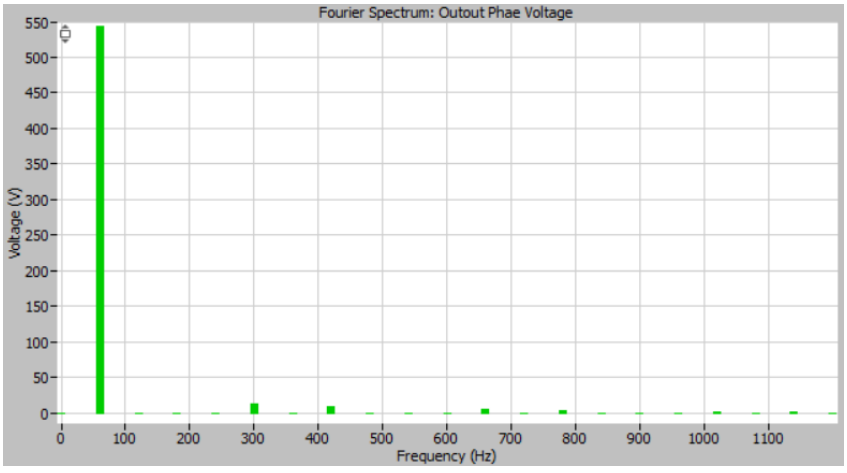


Fig 4.11. Frequency spectrum of the output phase voltage showing the dominant 60Hz frequency component.

whose magnitude is equal to the peak of the fundamental voltage. The relative percentages of the dominant harmonic components of the above waveform are tabulated in table 4.3. From the table

we can see that the harmonics of very less value in comparison to the fundamental of the output voltage.

Table 4.3. Relative percentages of the low-frequency harmonics in the output phase voltage.

Frequency	60 Hz	300 Hz	420 Hz	660 Hz	780 Hz	1020 Hz	1080 Hz
Relative %	100	2.2	1.6	0.9	0.6	0.4	0.4

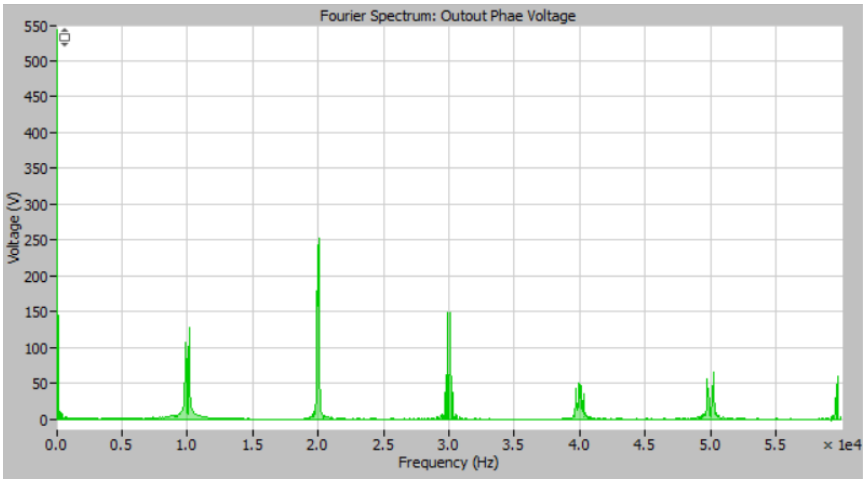


Fig 4.12. Frequency spectrum of the output phase voltage showing the high frequency harmonics present.

From this spectrum, we can also notice one of the advantages of the implementation of sine-triangle PWM for the operation of the inverter. The harmonics in the waveform are pushed to a higher frequency which makes them easier to filter out and obtain a clean sinusoidal voltage waveform. The magnitude of these harmonics is given below in table 4.4.

Table 4.4. Voltage magnitudes of the Fourier spectrum of the output phase voltage.

Frequency	60 Hz	10 KHz	20 KHz	30 KHz	40 KHz	50 KHz	60 KHz
Magnitude (V)	544.38	128.46	253.56	149.53	48.78	66.21	60.78

4.5.2 Output phase current

The obtained current waveform is a clean sinewave unlike the voltage waveform, this is since the load inductor filters out the harmonics present in the current waveform. The magnitude of the output current is at 25A which means that the rms of the output phase current is 17.6A. The phase current waveform is shown in fig 4.13.

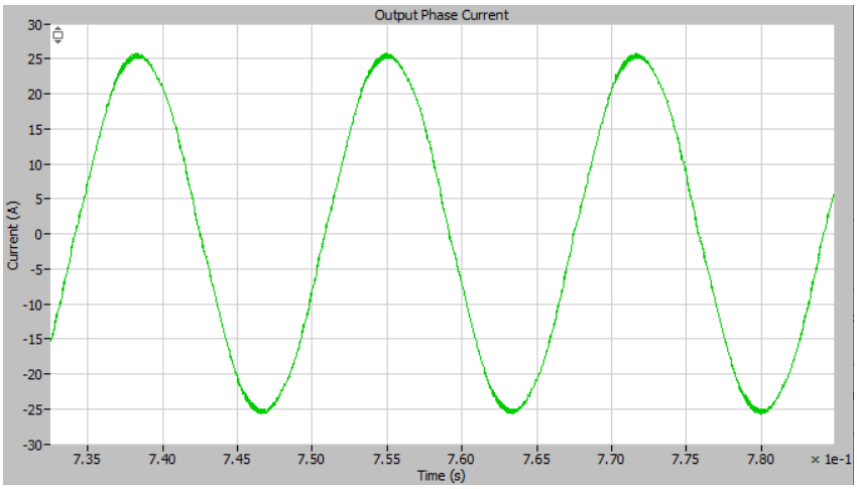


Fig 4.13. Output phase current of the three-phase inverter at V_{DC} = 1500V, m = 0.8 f_{sw} = 10 kHz, f_l = 60 Hz, where I_{RMS} = 17.6 A.

4.5.3 JBSFET losses

From the thermal description of the JBSFET that was created in PLECS, the device conduction loss, switching loss, junction temperature and the heat sink temperature can be determined. The conduction losses associated with the diode are also determined. The losses determined by the simulation are given in figures fig 4.14, fig 4.15 fig 4.16 and fig 4.17. From the above simulation results, the steady-state JBSFET conduction loss, JBSFET switching loss, body diode conduction loss and the total JBSFET loss are tabulated in the table 4.5.

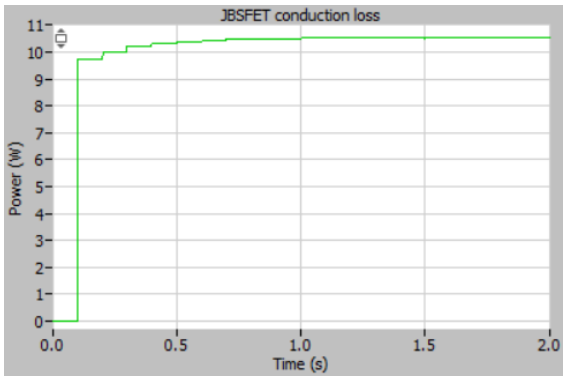


Fig 4.14. JBSFET conduction loss.

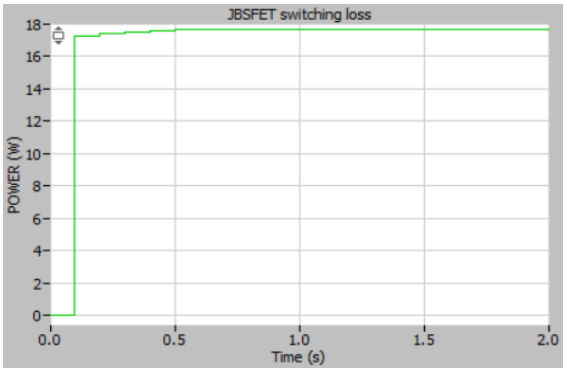


Fig 4.15. JBSFET switching loss.

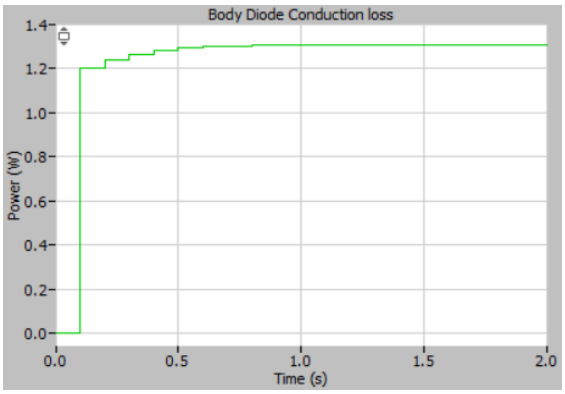


Fig 4.16. Body diode conduction loss.

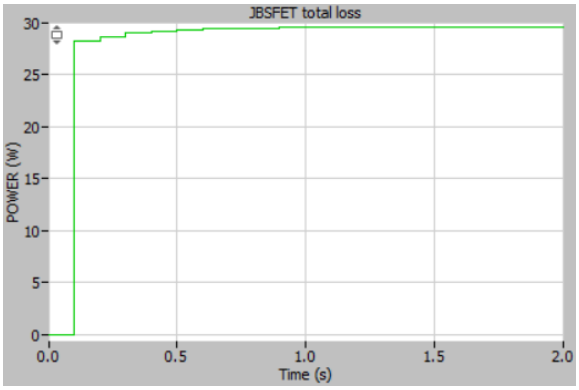


Fig 4.17. Total power loss of the JBSFET.

Table 4.5. JBSFET power loss distribution.

JBSFET loss	Power loss (W)
Conduction loss	10.52
Switching loss	17.67
Body diode loss	1.30
Total loss	29.51

The loss distribution of the JBSFET is given in the pie chart in fig. From the chart, we can notice that the JBSFET switching loss dominates the most which is around 60% followed by the conduction loss and the body diode conduction loss. The body diode has no switching loss as the

body diode in a JBSFET is a SiC JBS diode which is attributed to having zero reverse recovery losses, hence eliminating the diode switching loss. As the inverter is operated continuously, the JBSFETs of the inverter dissipate the power loss in the form of heat. To dissipate this heat effectively in the system a heat sink is used in the converter operation. The temperature rise of the heat sink can also be found by the simulation. From simulation it is found that at steady state, the temperature of the heat sink rises to about 46.24^{o}C as shown in fig 4.18. This junction temperature of the JBSFET also increases which, is shown in fig 4.19.

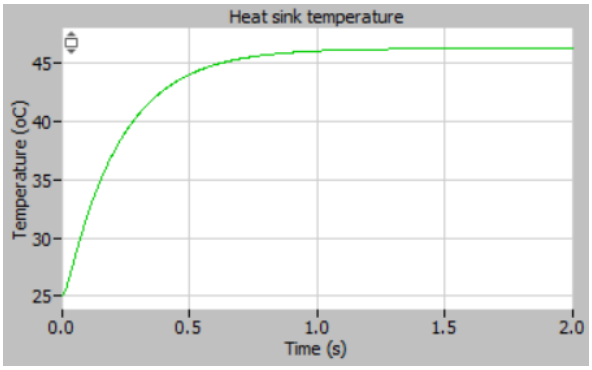


Fig 4.18. Temperature of the heat sink obtained from simulation.

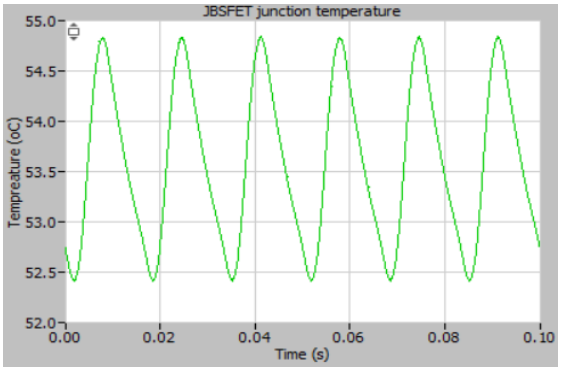


Fig 4.19. Junction temperature of the JBSFET obtained from simulation.

4.5.4 Efficiency calculations

In a three-phase inverter, the losses present in the circuit is mainly due to the power devices present in the circuit. As the losses are dissipated by the device, the temperature of the heat sink increases. Therefore, from the rise in the heat sink temperature, the power dissipated by the heat sink can be determined which is the total power dissipated by the six devices. In the simulation the power dissipated by the heat sink was found and is shown in the figure 4.20.

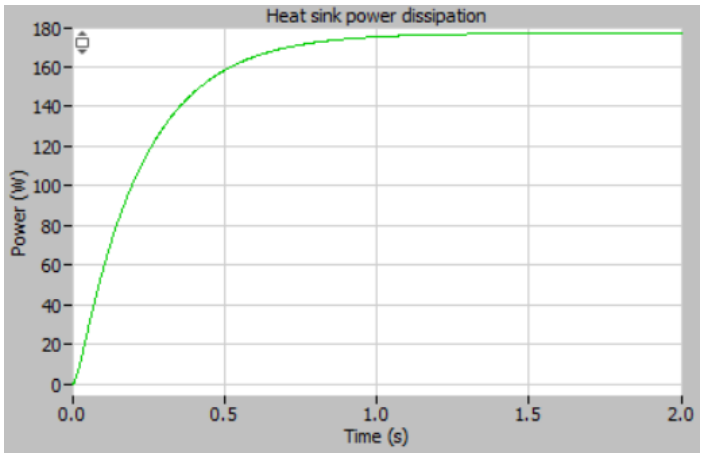


Fig 4.20. Power loss of the inverter dissipated by the heat sink.

The power dissipated from the heat sink was at steady state is found to be 177.069W. As the inverter was operating at 1500V and was drawing an input current of about 13A, the total input power of the system can be calculated by taking the product of the input voltage and current which was found to be 19.5kW. Therefore, the efficiency of the three-phase photovoltaic inverter can be calculated by

$$\eta = \frac{P_{in} - P_{loss}}{P_{in}}$$

Where, P_{in} is the input power of the inverter and P_{loss} is the total power loss of the inverter. The efficiency was calculated as 99.1%. From the above design and simulation, a prototype of the three-phase inverter was developed.

4.6 Experimental results

From the above calculations and design parameters, the three-phase photovoltaic inverter hardware prototype was developed. The experimental setup of the three-phase inverter is shown in the fig 4.21 and 4.22. The input DC voltage to the inverter was steadily increased from 0 to 1500V using the Magna power supply.

The gate pulses for the JBSFETs were given by the TMS320F28069 microcontroller in accordance with SPWM with a modulation index of 0.8 just like the single-phase inverter experiment which was discussed in chapter 3.

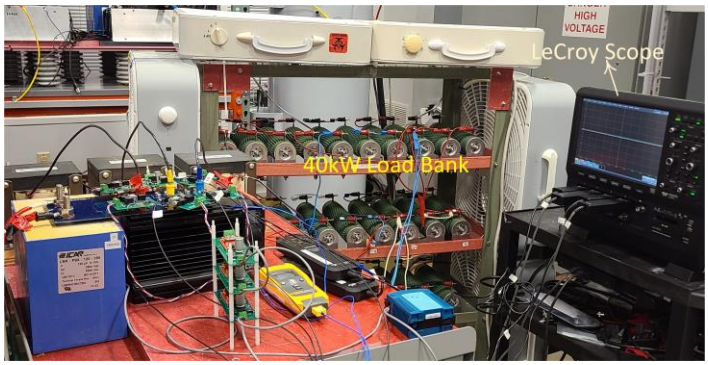


Fig 4.21. Experimental setup of the three-phase inverter with the 40kW load bank and the Lecroy scope.

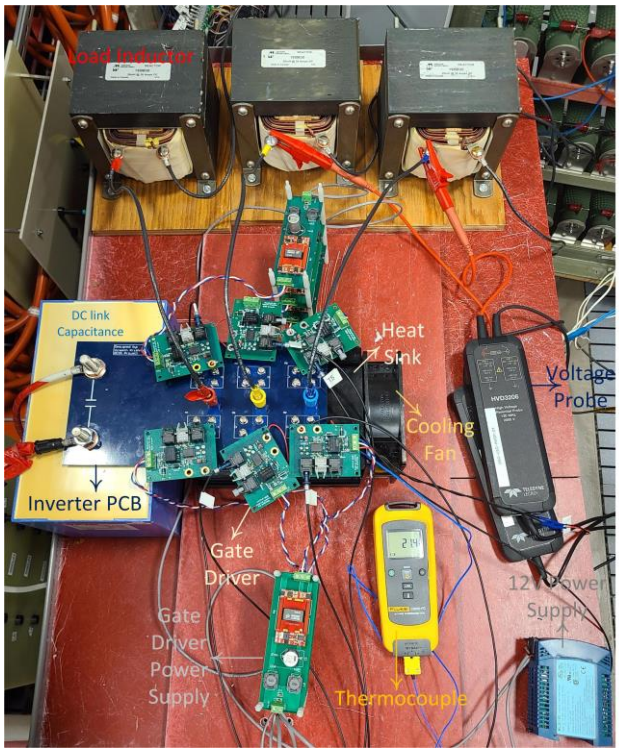


Fig 4.22. Detailed experimental setup of the three-phase photovoltaic inverter.

The load for the inverter was realized using a Hammond 195m30 20mH inductors and a resistor load bank rated at 40 kW. The experimental waveforms were recorded by using a LeCroy oscilloscope. The voltage waveforms were recorded by the use of the HVD3206 high voltage differential probe which is rated at 2000V. The output phase currents were recorded by using the CP031A current probe rated at 30A. The parameters of the measuring probes are given in table 4.5.

Table 4.6. Parameters of the measuring probes used.

Probe	Bandwidth (MHz)	Response time (ns)	Low-frequency Accuracy (%)
HVD3206	120	2.9	1
CP031A	100	3.5	1

The temperature of the heat sink was monitored using a fluke thermocouple. A thermal camera was also used to confirm the readings of the thermocouple and to constantly monitor the at experiment the 2 phase voltages and 2 phase currents were recorded. The experimental waveforms are given in fig .23 and fig 4.24.

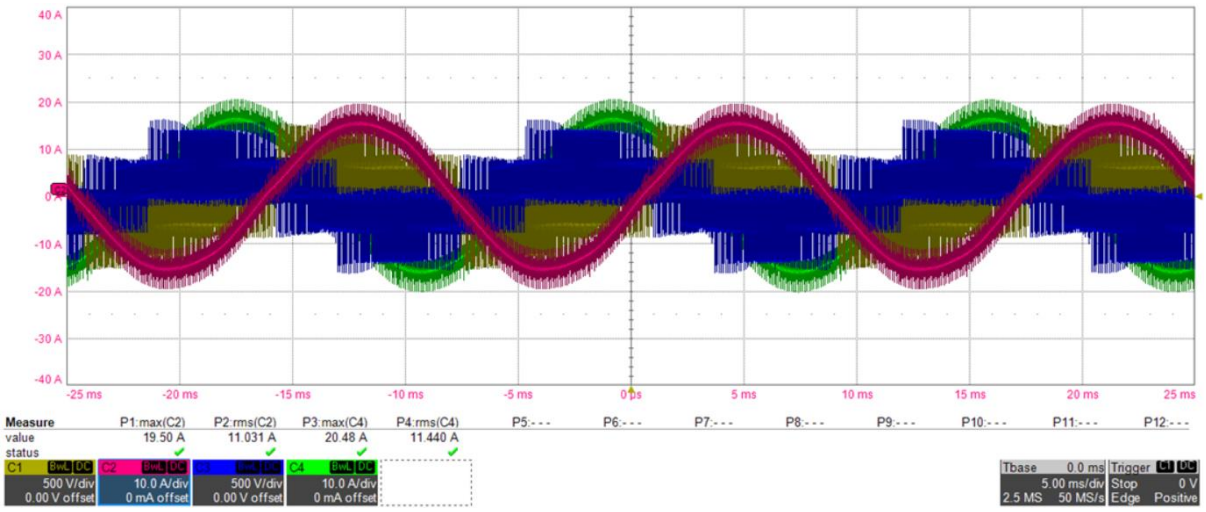


Fig 4.23. Experimental phase voltages and phase current waveforms of the three-phase photovoltaic inverter with at V_{DC} = 1000V, m = 0.8, f_{sw} = 10 kHz, f_l = 60 Hz, where I_{RMS} = 14.6 A.

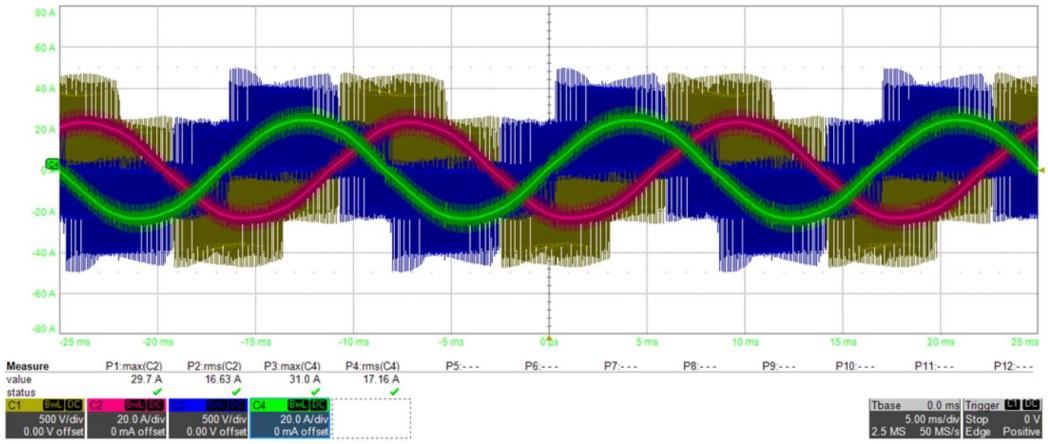


Fig 4.24. Experimental phase voltages and phase currents waveforms of the three-phase photovoltaic inverter with at V_{DC} = 1500V, m = 0.8, f_{sw} = 10 kHz, f_l = 60 Hz, where I_{RMS} = 17.6 A.

The current and voltage waveforms obtained are as expected from the theoretical understanding of the three-phase inverter and are like the waveforms obtained from the PLECS simulation. The Fourier spectrum the voltage waveform was also experimentally verified as shown in fig 4.25 and match with the simulation results at 1500V.

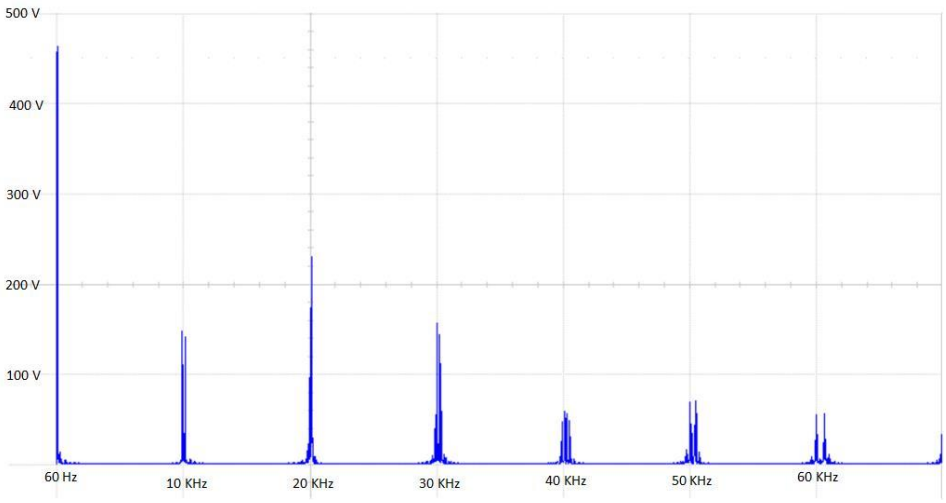


Fig 4.25. Frequency spectrum of the experimentally obtained phase voltage waveform depicting the high frequency switching harmonics for V_{DC} = 1500V.

From the Fourier spectrum we can see that the maximum frequency component is the 60Hz component followed by significant frequency components at the multiples of the switching frequency. The magnitudes of the voltage harmonics are shown in table 4.6 whose values are close to the harmonics obtained from simulation.

Table 4.7. Voltage magnitudes of the Fourier spectrum of the experimental output phase voltage.

Frequency	**60 Hz**	**10 KHz**	**20 KHz**	**30 KHz**	**40 KHz**	**50 KHz**	**60 KHz**
Magnitude (V)	462.74	144.95	228.50	155.60	57.35	63.44	49.3

The 20KHz frequency component is higher than the 10KHz component because the phase voltage of the inverter is equal to the difference of the pole voltage of the inverter and the neutral to pole voltage of the inverter. Both of which have a significant 10 KHz frequency components in their waveforms. The 10KHz components of these two voltages cancel each other out reducing the 10KHz frequency component in the resulting phase voltage.

The thermal image of the setup is shown in fig 4.26. From the figure it can be determined that the temperature of the heat sink is around 46^{o}C. This can also be confirmed by the steady-state temperature of the heat sink measured using a thermocouple. The thermocouple reading of the heat sink temperature is shown in figure 4.27.

Fig 4.26. Thermal image of the photovoltaic inverter system.

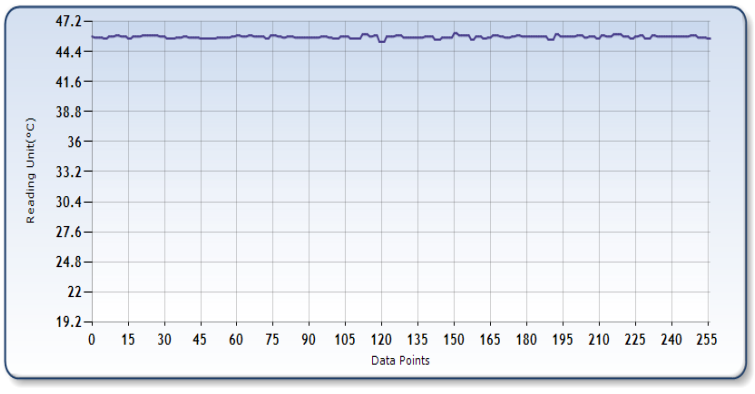


Fig 4.27. Thermocouple readings of the temperature of the heat sink at rated operating V_{DC} = 1500V.

From the datasheet of the heat sink and the temperature of the heatsink, the total power dissipated by the heat sink can be found. The total power dissipated from the heat sink is found to be 180W which is close to the value determined by the simulation. Since, the inverter circuit comprises of six JBSFETs therefore, the total power loss of a single JBSFET is 30W. With the supplied input voltage being 1500V and the input current drawn by the inverter being 12.16A. From these values, the efficiency of the prototype of the photovoltaic inverter. With the input power being 18.24kW and the power loss being 180W, the efficiency of the three-phase photovoltaic inverter was found to be 99% which is close to the efficiency of the system determined through the simulation.

From the thermocouple reading, we can also find the junction temperature of the JBSFET by using the equation:

$$T_j = T_c + P_{loss} R_{jc}$$

Where T_j is the junction temperature of the JBSFET, T_c is the case temperature of the JBSFET, P_{loss} is the power loss of the device and R_{jc} is the junction to case thermal resistance of the device. The R_{jc} of the device depends on the device package and is equal to 0.26 $^oC/W$. The power loss of the device is determined experimentally as 30W and the case temperature of the device is equal to the heat sink temperature as the thermocouple used was placed exactly between the device and the heat sink. Therefore, T_c is equal to 46^oC. Using these values in the above equation, the junction temperature of the JBSFET comes out to be 53.8 ^oC.

The solar string inverter was tested again up to 1800V to test the limits of the JBSFET. The experimental setup was similar to that mentioned before. The inout DC voltage was increased from 0 to 1800V and the inverter was tested at 1800V for 30 mins to test the limitations of the device.

The experimental output waveforms of this test are shown in fig. 4.28 which shows the three line voltages V_{AB}, V_{BC}, V_{CA} and the three line currents I_A, I_B, and I_C.

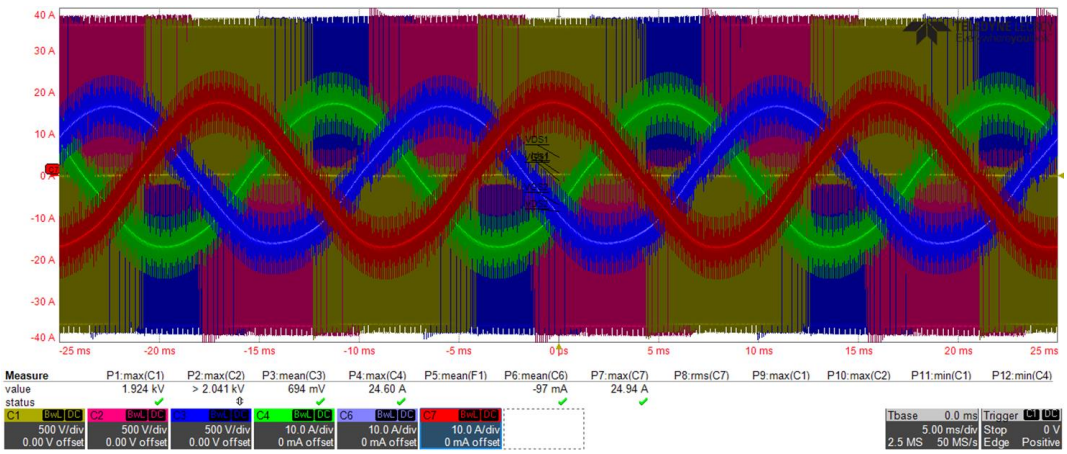


Fig 4.28. Experimental line voltages and phase currents waveforms of the three-phase solar string inverter at V_{DC} = 1800V, m = 0.5, f_{sw} = 10 kHz, f_l = 60 Hz, where I_{RMS} = 12.4 A.

CHAPTER 5

CONCLUSION AND FUTURE WORK

The advancement in power semiconductor technology enables for power electronics to become more rugged, compact and more efficient. This can be seen the advancement in SiC power device technology which resulted in a novel device namely the JBSFET which is a monolithically integrated a SiC MOSFET and a JBS diode in order to minimize the losses in the body diode of the MOSFET. This monolithic integration makes the device more compact less susceptible to the parasitics. The performance of this device was evaluated in this thesis which was done so by obtaining the losses associated with the device and then modelling the losses in PLECS.

The performance of this 3.3kV JBSFET was evaluated by using it to develop a three-phase 1500V photovoltaic string inverter. This system was simulated in PLECS where the losses of the device were also modelled. In the simulation stage itself, the performance of the device was compared to that of a normal SiC MOSFET. From this comparison, the JBSFET was determined to be superior compared to the MOSFET as it had lower losses associated with it.

From designing a three-phase photovoltaic inverter, simulating it with the loss model of the JBSFET, a hardware prototype of the string inverter was developed. Upon experimenting the developed the prototype of the string inverter the obtained results were then compared with the simulation results and were matching. Therefore, the performance of the JBSFET was tested in a three-phase string inverter and thus it can be concluded that the JBSFET can be used to build power electronic converters that are rugged, smaller in size and are more efficient.

As the JBSFET technology advance, the JBSFET can be made more rugged and compact to used it other power electronic circuitry. The JBSFET can also be packed into numerous other packages hence, giving power electronic engineers more freedom in designing a compact circuit.

JBSFETs with higher breakdown voltages can also be developed which can then be used in developing high voltage power electronic circuits which is to be used in grids.

REFERENCES

[1] X. She, A. Q. Huang, Ó. Lucía and B. Ozpineci, "Review of Silicon Carbide Power Devices and Their Applications," in IEEE Transactions on Industrial Electronics, vol. 64, no. 10, pp. 8193-8205, Oct. 2017, doi: 10.1109/TIE.2017.2652401.

[2] A. Q. Huang, "Power Semiconductor Devices for Smart Grid and Renewable Energy Systems," in Proceedings of the IEEE, vol. 105, no. 11, pp. 2019-2047, Nov. 2017, doi: 10.1109/JPROC.2017.2687701.

[3] Baliga, B. J. (2008). *Fundamentals of power semiconductor devices*. Berlin: Springer

[4] Kanale, A. R. (2019). *Dynamic Characterization and Failure Analysis of the 1200V, 10A Silicon Carbide JBSFET*

[5] A. Singh et al., "Development and Validation of a SiC Based 50 kW Grid-Connected PV Inverter," 2018 IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, 2018, pp. 6165-6172, doi: 10.1109/ECCE.2018.8557392.

[6] Baliga, B. J. (2017). *Gallium nitride and silicon carbide power devices*

[7] E. Serban, M. Ordonez and C. Pondiche, "DC-Bus Voltage Range Extension in 1500 V Photovoltaic Inverters," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 3, no. 4, pp. 901-917, Dec. 2015, doi: 10.1109/JESTPE.2015.2445735.

[8] R. Inzunza, R. Okuyama, T. Tanaka and M. Kinoshita, "Development of a 1500Vdc photovoltaic inverter for utility-scale PV power plants," 2015 IEEE 2nd International Future Energy Electronics Conference (IFEEC), Taipei, 2015, pp. 1-4, doi: 10.1109/IFEEC.2015.7361615.

[9] Datasheet: ISO5852S-Q1 High-CMTI 2.5-A and 5-A Reinforced Isolated IGBT, MOSFET Gate Driver With Split Outputs and Active Protection Features.

[10] Datasheet: AFBR-16xxZ and AFBR-26x4Z/25x9Z.

[11] Datasheet: MGJ6-14mm | Datasheet | 10.2kVDC Isolated 6W Gate Drive SM DC-DC Converters | Murata Power Solutions.

[12] Z. Chen, D. Boroyevich, P. Mattavelli and K. Ngo, "A frequency-domain study on the effect of DC-link decoupling capacitors," 2013 IEEE Energy Conversion Congress and Exposition, Denver, CO, 2013, pp. 1886-1893, doi: 10.1109/ECCE.2013.6646938.

[13] Datasheet: WIMA 1µF 3 kV DC/ 750 V ACSNMPW041008JD4KSSD Datasheet (PDF).

[14] Z. Zhang, B. Guo, F. F. Wang, E. A. Jones, L. M. Tolbert and B. J. Blalock, "Methodology for Wide Band-Gap Device Dynamic Characterization," in IEEE Transactions on Power Electronics, vol. 32, no. 12, pp. 9307-9318, Dec. 2017, doi: 10.1109/TPEL.2017.2655491.

[15] Z. Chen, Y. Yao, M. Danilovic and D. Boroyevich, "Performance evaluation of SiC power MOSFETs for high-temperature applications," 2012 15th International Power Electronics and Motion Control Conference (EPE/PEMC), Novi Sad, 2012, pp. DS1a.8-1-DS1a.8-9, doi: 10.1109/EPEPEMC.2012.6397198.

[16] Mohan, N., Undeland, T. M., & Robbins, W. P. (2003). *Power electronics: Converters, applications, and design*. Hoboken, NJ: John Wiley & Sons.

[17] Datasheet: TMS320F2806x Microcontrollers datasheet (Rev. H).

[18] https://www.hammfg.com/part/195M30.

[19] Datasheet: Teledyne Lecroy High Voltage Differential Probes HVD3605, HVD3206 HVD310x

[20] Datasheet: Teledyne Lecroy Current Probes CP031A.

[21] M. J. Mnati, J. K. Abed, D. V. Bozalakov and A. Van den Bossche, "Analytical and calculation DC-link capacitor of a three-phase grid-tied photovoltaic inverter," 2018 IEEE 12th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG 2018), Doha, 2018, pp. 1-6, doi: 10.1109/CPE.2018.8372489.

[22] Datasheet: LNK-P9X-120-350 3500V DC, 120 µF film capacitor.

[23] S. Hazra et al., "High Switching Performance of 1700-V, 50-A SiC Power MOSFET Over Si IGBT/BiMOSFET for Advanced Power Conversion Applications," in IEEE Transactions on Power Electronics, vol. 31, no. 7, pp. 4742-4754, July 2016, doi: 10.1109/TPEL.2015.2432012.

[24] Datasheet: Heat sink 390-180AB 392.pdf.

[25] Datasheet: Qualtek cooling fan FAA1-12038-A Series.