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(54) **METHOD AND CIRCUIT FOR CASCADED PULSE WIDTH MODULATION**

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(52) **U.S. Cl.** **363/71; 363/98; 327/175**

(58) **Field of Classification Search** **363/65, 363/71, 98; 323/283; 327/172, 175, 176, 327/182**

See application file for complete search history.

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(57) **ABSTRACT**

A method of balancing the voltage of DC links in a cascaded multi-level converter (CMC) semiconductor circuit, including the steps of providing a plurality of H-bridge converters per phase in the CMC circuit and utilizing a three phase duty cycle value from the main controller to determine a normalized duty cycle value, a ceiling duty cycle value and a floor duty cycle value. The normalized duty cycle value and an output current of the CMC is used to determine the direction and polarity of a capacitor current, and utilizing the capacitor current to determine a plurality of output capacitor voltages. A voltage summation result and direction is obtained from a ceiling index pointer and a floor index pointer and the voltage summation result, direction from the ceiling index pointer and a floor index pointer are used to create a combined switching table for the H-bridge converters. A pulse width modulator is utilized to balance the voltage of the DC links and thereby eliminate DC-capacitor voltage imbalance.

12 Claims, 13 Drawing Sheets

