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Kermani et al.

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(54) **TESTING ASYNCHRONOUS CIRCUITS**

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(58) **Field of Search** 702/119, 118, 702/117, 123; 340/514; 438/14, 209, 719

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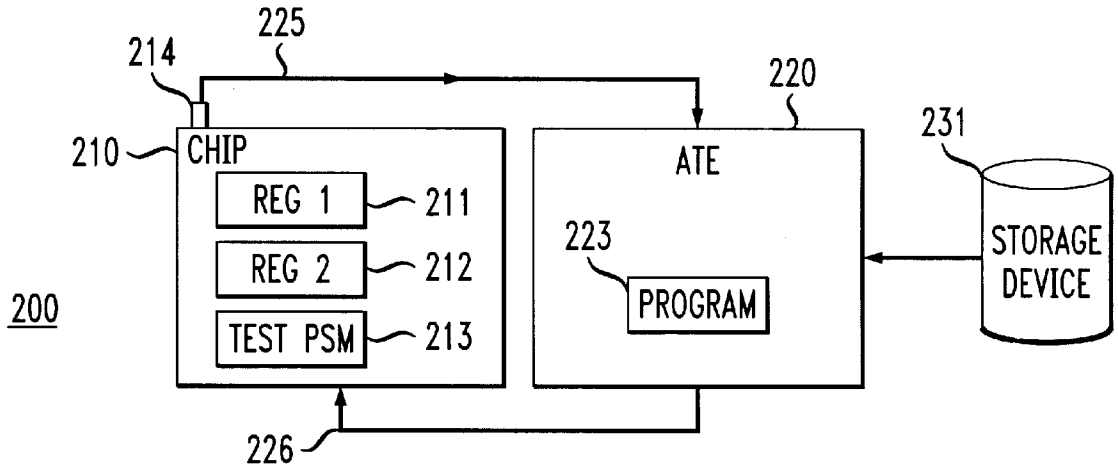
(57) **ABSTRACT**

A method and system for testing a circuit. A test program is downloaded into the circuit, which causes the circuit to provide a serial test output pattern comprising a series of identical signals to indicate whether the circuit passes the test. Signals of the test output pattern are compared against corresponding signals of an expected test output pattern only for non-masked signals of the expected test output pattern, wherein the expected test output pattern is masked for a maximum tolerable time period around an expected test output pattern start time.

17 Claims, 1 Drawing Sheet