ABSTRACT

KUMAR, MOHIT. A Low-Power Integrated Interface Circuit for a Resonant Gas Sensor Based on a Capacitive Micromachined Ultrasonic Transducer (CMUT). (Under the direction of Dr. Omer Oralkan.)

The effect of environment on health is an area of growing concern and an opportunity for research. Although there has been improvement in the health services over the years, the advancements in technology has also introduced new and more contaminants into the environment. Different volatile organic compounds (VOCs) present in the environment play a major role in the environmental contamination. So, there is a need for a VOC gas detection system. Also such a portable gas detection platform has potential of detecting and analyzing breath, which can be used for diagnostic or monitoring applications.

The platform technology used is capacitive micromachined ultrasonic transducers (CMUT). CMUT devices are a suitable candidate for gas sensing because of their potential to sense different gases on the same die. This also enables differential sensing to correct for any long term frequency drift. CMUTs also have relatively high Q-factor because of the vacuum-sealed cavity, which helps in reducing the power consumption.

This thesis discusses the implementation of a low-power system interface for gas sensing applications using CMUT. The system was designed and fabricated in a 0.18-μm BiCMOS process. The CMUT was interfaced with an on-chip oscillator for generating a sinusoidal oscillation at the CMUT resonant frequency. This sinusoidal oscillation is converted to a digital signal using a sine-to-square wave converter and the frequency of the signal was counted using a digital frequency counter. Two oscillators (a BJT-based Colpitts oscillator and an inverter-based oscillator), a sine-to-square wave converter, and a digital frequency counter block were analyzed, designed, and measured for their functionality, power consumption, and accuracy. A complete system-level demonstration was shown from CMUT interface to the final digital output.

With this work we demonstrated that the custom analog front-end (AFE) helps in reducing power compared to the implementation using discrete components. This approach also offers an integrated single-chip solution with a direct digital output. The vision of having a single system interfaced with the CMUT and transmitting the data to the Advanced Self-Powered Systems of Integrated Sensors and Technologies (ASSIST) system on chip (SOC) through the serial peripheral interface (SPI) with ultra-low power seems feasible and will be the goal of the 2^{nd} generation of this front-end.

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A Low-Power Integrated Interface Circuit for a Resonant Gas Sensor Based on a Capacitive Micromachined Ultrasonic Transducer (CMUT)

by
Mohit Kumar

A thesis submitted to the Graduate Faculty of
North Carolina State University
in partial fulfillment of the
requirements for the Degree of
Master of Science

Electrical Engineering

Raleigh, North Carolina

2015

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DEDICATION

To my parents, family, and teachers.

BIOGRAPHY

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ACKNOWLEDGEMENTS

First of all I would like to thank my parents and family for all the encouragement and support.
I would like to thank Dr. Omer Oralkan for giving me an opportunity to work on this project. His continuous guidance and support helped me in finishing this work on-time. I am grateful to Dr. Brian Floyd and Dr. Veena Misra for being in my committee.
I am thankful to Chunkyun Seok (CK) for helping me throughout my work on this project. I am thankful to Kirti Bhanushali for reviewing my thesis. I am also grateful to Joe Matthews and Steve Lipa for their help during the testing phase.
I was lucky to have lab-mates like CK, Oluwafemi, Marzana, Jeanne, Xun, and Xiao. I will miss the interesting discussion we used to have in the lab.

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CHAPTER

1

INTRODUCTION

1.1 Motivation

Health and environmental tracking (HET) plays a crucial role in the diagnosis of diseases as well as maintaining a healthy lifestyle. HET is a preventive measure that assists a healthy and happy lifestyle. There is lack of information that could expose the possible links between environmental hazards and chronic diseases. HET bridges the gap in understanding the effects of environmental pollutants on the health. It assists medical professionals by providing them relevant information for relating the environmental hazards and chronic disease. There are some efforts to understand the effects of environmental pollutants on human health. Fig. 1.1 shows an effort by Centers for Disease Control and Prevention (CDC) [1].

Early detection and analysis of different volatile organic compounds (VOCs) is one of the important steps in environmental tracking. VOCs can be found in different home and personal care products like air fresheners, cosmetics, etc [2]. The severity of health risk depends on the concentration of VOCs in air and how long and often a person breaths them in. Some short-term effects of VOCs include eye, nose, and throat irritation, and vomiting [2]. VOCs make symptoms worse for people with asthma or people sensitive to chemicals [2]. So, there is a need for systems, which can detect these VOCs in the environment. For continuous monitoring we want these systems to be low-power

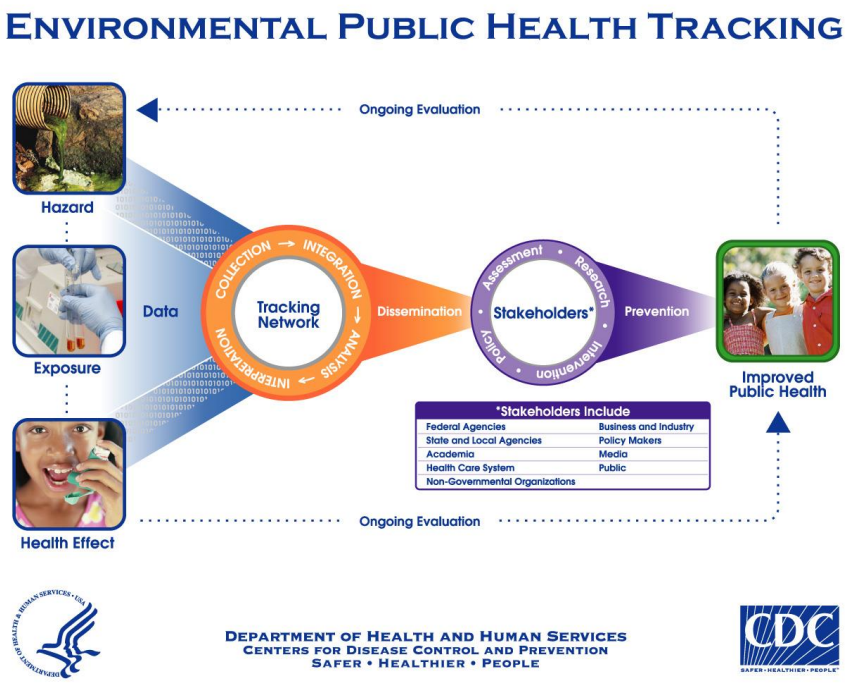


Figure 1.1 CDC's environmental public health tracking program [1].

so that they can be operated with a battery or harvested energy. Wearability is also one of the main requirements if these systems are to be used as a personal environmental tracker.

1.2 Objective

The main objective of this work is to design and test low-power system blocks, which can be interfaced with a capacitive micromachined ultrasonic transducer (CMUT) to implement a gas sensor selective to VOCs. Small form factor and low-power consumption are the two main design constraints. In the bigger picture this work is part of the Health and Environmental Tracker (HET) testbed of the NSF Nanosystems Engineering Research Center (NERC) for Advanced Self-Powered Systems of Integrated Sensors and Technologies (ASSIST) as shown in Fig. 1.2 [3].

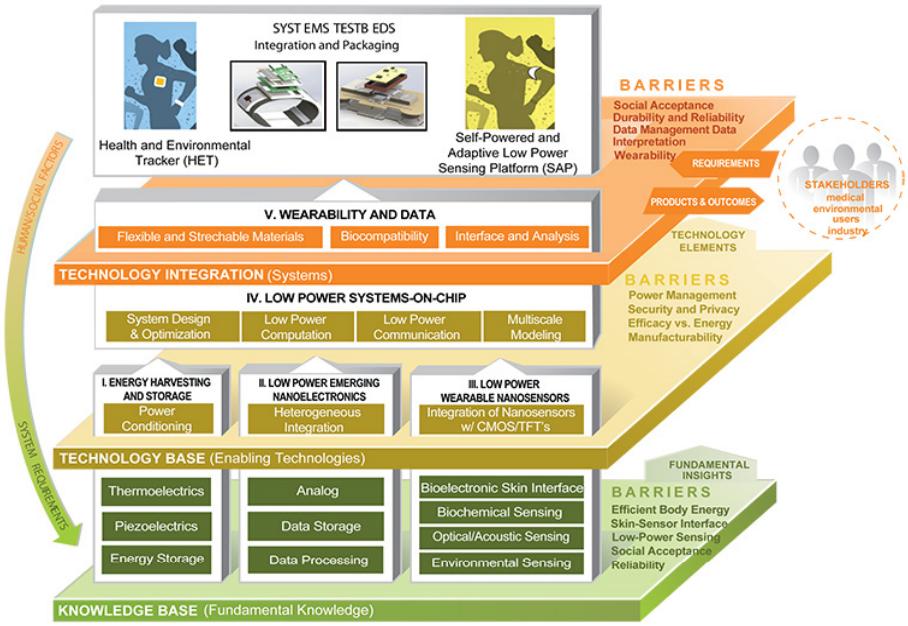


Figure 1.2 ASSIST's research thrusts [3].

1.3 Selecting the Sensor

There are different kinds of sensor architectures, which can be utilized for gas sensing. Resistive and mechanically resonant gas sensors are the two main examples. Optical methods are also widely used, but they require high power consumption. In resistive gas sensors there is change in the resistance of the sensor when the target gas is present in the environment. For resonant gas sensors the impedance profile of the gas sensor changes with the presence of the gas in the environment. Generally metal-oxide based resistive sensors require heating and hence they tend to consume high power compared with resonant sensors. Also it is easier to integrate resonating structures with CMOS circuits compared to metal-oxide based resistive sensors.

1.4 Why CMUT?

CMUTs have many inherent advantages over other MEMS-based resonant sensors [4, 5]. One of the important advantages of using a CMUT-based sensor is the ability to implement an array of

resonators on the same die, which improves selectivity. Differential sensing can also be utilized by using a reference sensor on the same die and using remaining sensors for sensing different gases. The power consumption in resonant sensors is strongly related to the Q-factor of the sensor and the resonant frequency. CMUT has a higher Q-factor compared with the cantilever sensor of same area because of two main reasons. First, the vacuum-sealed cavity reduces the loss and hence helps increase the Q-factor. Second, the structure of the CMUT utilizes parallelism to reduce the motional resistance. This motional resistance is the main source of loss in resonant structures. Also the structure of the CMUT makes the chemical functionalization easier.

1.5 Thesis Organization

This work focuses on integrated circuit design to interface a CMUT for the implementation of a mass loading based gas sensor. The thesis is organized in five chapters. Chapter 2 discuses the system-level idea of gas sensing. Basic CMUT architecture, concepts of polymer functionalization, mass loading, converting impedance changes into frequency, and measuring the frequency are presented from a system-level point of view. Chapter 3 discusses the circuit design for a 5-MHz CMUT. Two oscillators designed to be interfaced with CMUTs are discussed from reducing the power consumption point of view. Accuracy of an on-chip digital frequency counter is discussed. The operation of a parallel-to-serial interface is explained. Chapter 4 discusses the measurement results from the fabricated chip. The conclusion is presented in Chapter 5.

CHAPTER

2

SYSTEM-LEVEL OVERVIEW

In Chapter 1 we discussed the need for the VOC sensors and advantages of using CMUTs for VOC sensing applications. In this chapter we will discuss CMUT operation and converting CMUTs into gas sensors for VOCs. Additionally, the system-level requirements would be evaluated and a complete block diagram from sensing the gas to the final digital equivalent of gas concentration will be presented.

2.1 CMUTs

First CMUT was fabricated in 1993 by the Khuri-Yakub Ultrasonics Group in Stanford University [6]. Initial development of CMUTs was for ultrasonic imaging applications. There has been demonstrations of CMUTs for chemical and gas sensing applications [5, 7–12]. Most of the previous work [7–11] was for detecting very low concentrations of lethal gases. A 72.5 mW/channel oscillator with an operating frequency around 45 MHz was demonstrated [5]. Also there has been a demonstration of low-power BJT-Colpitts oscillator operating at 4.33 MHz and consuming 0.77 mW for environmental monitoring by our group [12]. In this work we aim to provide a complete end-to-end single chip interface from the CMUT to a digital output with low-power consumption.

2.1.1 Basic Working Principle

Fig. 2.1 shows the cross-sectional view of a CMUT developed by the Integrated Microsystems for Imaging, Sensing, and Therapy (iMIST) Lab at North Carolina State University [12]. This device is fabricated using a three-mask process with anodic bonding [13]. A CMUT consists of a thin vibrating plate suspended over a vacuum gap. On application of a DC voltage across the top and bottom electrodes of the CMUT there is deflection in the top plate of the device. Plate deflection will be such that the mechanical restoring force balances out the electrostatic force on the plate. Because of these balancing forces CMUT gets its resonating behavior. One thing to note here is that the deflection of the top electrode changes as there is change in the DC voltage across the CMUT electrodes. This change in deflection changes the resonant properties of the CMUT.

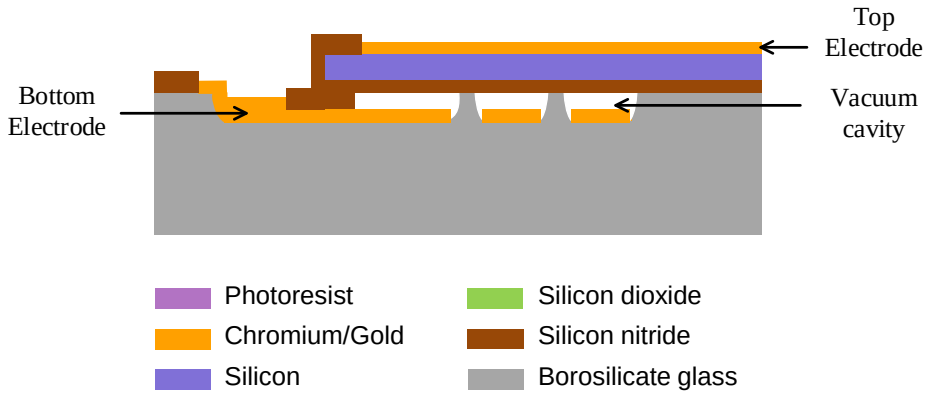


Figure 2.1 Cross-sectional view of a CMUT [12].

2.2 CMUT Electrical Model

In this section first the CMUT electrical equivalent circuit model will be discussed and then the electrical input impedance of the CMUT biased at a particular DC voltage will be shown. This is followed by a CMUT step response showing input current on application of a voltage step to the 1-port CMUT model.

2.2.1 Equivalent Model

The CMUT is an electrostatically actuated mechanical structure. Mechanical properties of the CMUT are modeled in electrical domain as it helps in enabling us to use electrical circuit simulations to analyze the mechanical system. It is easier to analyze some structures in electrical domain because there are many programs available to analyze the circuits. Also there is already more intuitive understanding of circuit elements. Having an electrical model of CMUT also helps in the design and end-to-end simulation of the electrical interface circuit.
CMUT's electrical model is represented by a four-element Butterworth-van-Dyke (BvD) equivalent circuit shown in Fig. 2.2 [14]. CMUT's electrical equivalent model is a little more involved and complicated but for parameter extraction and design studies, the lumped BvD model is more useful. The BvD model has four elements R_E, L_E, C_E, and C_O. The capacitance C_O represents the electrical capacitance present due to the physical parallel plate capacitive structure and R_E, L_E, and C_E are the electrical equivalent of the mechanical parameters present due to the thin deflected plate of the CMUT. R_E represents the loss of the resonator, L_E represents the effective mass, and reciprocal of C_E represents stiffness. As the DC voltage across the CMUT is changed the deflection profile of the plate changes which changes all these parameters, which in turn changes the Q-factor of the CMUT. So CMUTs are generally biased at a DC level giving optimum Q-factor in sensor applications. In addition to these elements a parallel R and C in series with the BvD model can be used to model the electrical contacts.

For the CMUT resonator there are two resonances, series and parallel. Series resonance is when L_E resonates with C_E giving minimum impedance value. Parallel resonance is when L_E resonates with $(\frac{1}{C_E} + \frac{1}{C_O})^{-1}$. A single CMUT resonator consists of multiple thin plates connected electrically in parallel. Series resonance has lower Q-factor because of cell-to-cell non-uniformity. In parallel resonance mode the cell-to-cell non-uniformity is averaged out. Therefore parallel resonance gives higher Q-factor than the series resonance.

2.2.2 Impedance Profile

Fig. 2.3 represents the typical CMUT impedance profile. As mentioned in the earlier part there are two kinds of resonances in CMUTs, i.e., series and parallel. From equation 2.2 we can infer that for series resonance there will be a minimum in the numerator as the imaginary parts due to L_E and C_E will cancel each other. For parallel resonance L_E will cancel series combination of C_E and C_O giving a minimum in the denominator. Fig. 2.3 (a), (b), (c) and (d) shows real part, imaginary part, magnitude, and phase information of a CMUT resonator's impedance. Series and parallel resonant frequencies can also be observed from the magnitude of CMUT's impedance represented

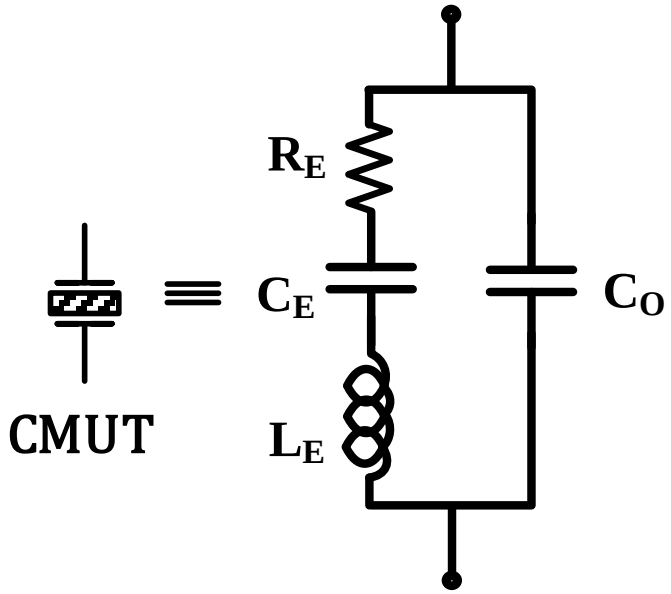


Figure 2.2 Electrical equivalent circuit model of CMUT [14].

in Fig. 2.3(c). Minimum in magnitude of CMUT's impedance corresponds to series resonance and maximum corresponds to parallel resonance.

$$Z_{CMUT} = \frac{(R_E + j\omega L_E + \frac{1}{j\omega C_E}).(\frac{1}{j\omega C_O})}{(R_E + j\omega L_E + \frac{1}{j\omega}(\frac{1}{C_E} + \frac{1}{C_O}))} \tag{2.1}$$

$$f_s = \frac{1}{2\pi\sqrt{L_E \cdot C_E}} \tag{2.2}$$

$$f_p = \frac{1}{2\pi\sqrt{L_E \cdot \frac{C_E \cdot C_0}{C_E + C_0}}} \tag{2.3}$$

2.2.3 Step Response of the CMUT Resonator

Step response is a time-domain approach to analyze the impedance profile and mainly the Q-factor of the resonator. Fig. 2.4 represents the step response when a CMUT is excited with a voltage step and current through the CMUT is plotted. Fig. 2.4 represents the CMUT current for three values of R_E, $R_E = 20\,\Omega$, $R_E = 60\,\Omega$, and $R_E = 100\,\Omega$. For step response the Q-factor can be directly inferred from the number of cycles it takes from the peak sinusoidal amplitude to the e^{-1} of the maximum

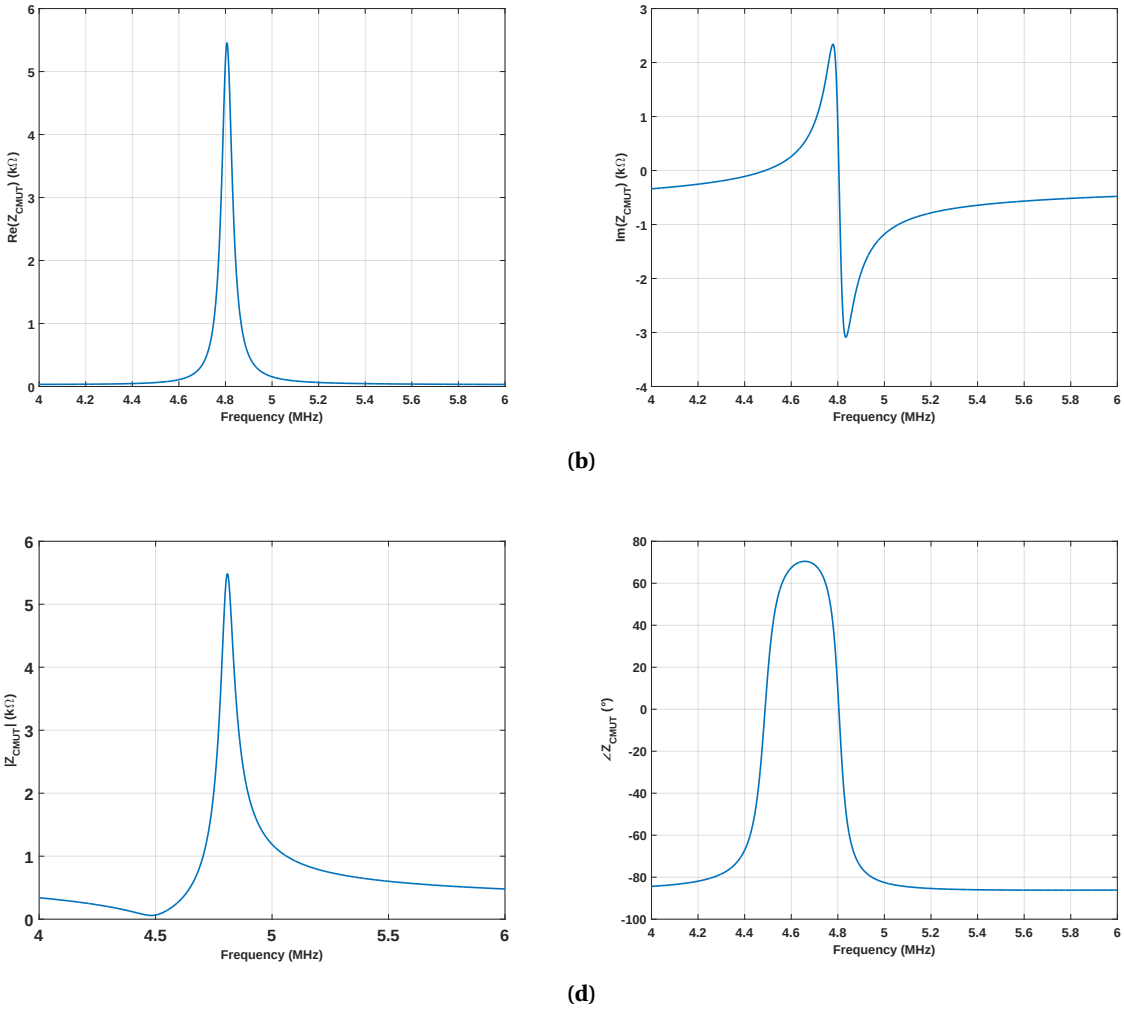


Figure 2.3 CMUT's impedance (R_E=35.84 Ω; L_E=125 μH; C_E=10.07 pF; C_0=68.11 pF) a) Re(Z_{CMUT}) b) Im(Z_{CMUT}) c) $|Z_{CMUT}|$ d) $\angle Z_{CMUT}$.

amplitude. Also we can see as the R_E increases the signal dampens faster because the loss of the resonator increases. In other words Q-factor decreases as R_E increases. Ideally for a resonator we want infinite Q so that once given a small excitation the resonator resonates at its fundamental frequency without any external interface.

Fig. 2.3 represents the impedance profile of a CMUT in frequency domain which can give us information regarding the Q-factor and also fundamental frequency of the CMUT. In frequency domain representation Q-factor represents how fast we are transitioning from the region of reso-

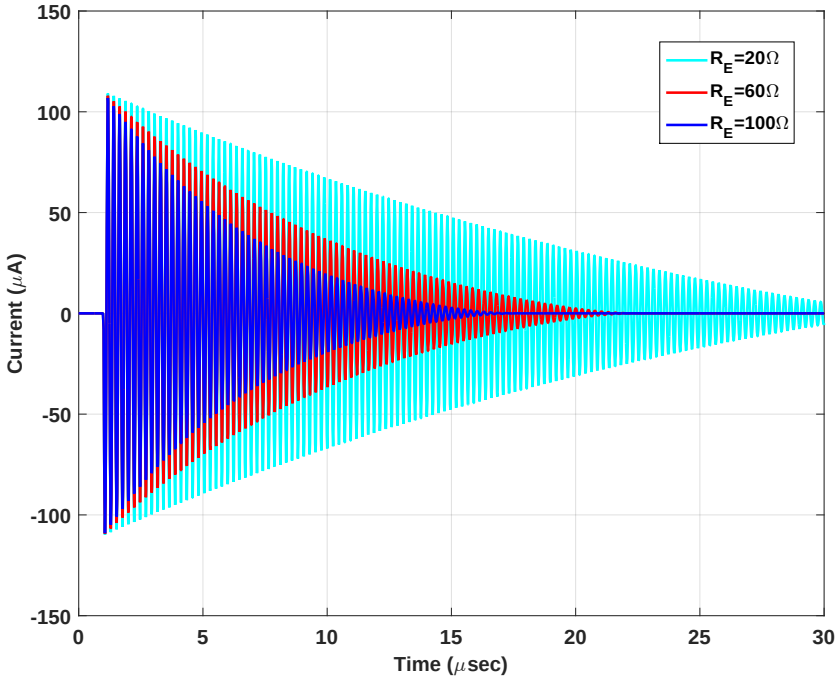


Figure 2.4 Voltage step response showing exponentially decaying sinusoidal current of 1-port CMUT model.

nance, e.g., in Fig. 2.3(c) for parallel resonance it will be from region where magnitude is increasing to region where magnitude is decreasing and the frequency around where the transition is occurring is the fundamental frequency. Similar information can also be obtained from the time-domain response (Fig. 2.4), where higher Q-factor is related to longer decay time of the exponential envelope of the sinusoidal signal and frequency of the sinusoidal represents the fundamental frequency of the oscillation.

2.3 Mass Loading Principle

In Section 2.2 we discussed the CMUT behavior and impedance profile as a resonator. There is one more step involved in converting a CMUT into a gas sensor. The vibrating thin plate of the CMUT is coated with a very thin layer of polymer and this process is called polymer functionalization. The polymer selection is done on the basis that it selectively adsorbs the targeted gas present in the environment. Whenever there is targeted gas present in the environment it will be adsorbed by the

polymer layer, which is equivalent to increase in the mass of the CMUT's plate. This increase in mass is known as mass loading [15]. Equation 2.4 shows the relation between change in mass and the frequency shift. Rearranging we can observe from equation 2.5 that for achieving minimum ∂m we need to increase f_0 and reduce ∂f, which is limited by the noise of the sensor and the circuit. Minimum achievable ∂m is related to the minimum concentration of the gas which can be measured.

$$\partial f = -\frac{1}{2} \cdot \frac{f_0}{m} \cdot \partial m \tag{2.4}$$

$$\partial m = -2 \cdot \frac{m}{f_0} \cdot \partial f \tag{2.5}$$

Increase in mass is equivalent to increase in the inductance (L_E) represented in the BvD model shown in Fig. 2.2. This inductance affects the series and parallel resonance of the CMUTs. Fig. 2.5 shows the basic idea of functionalization and mass loading.

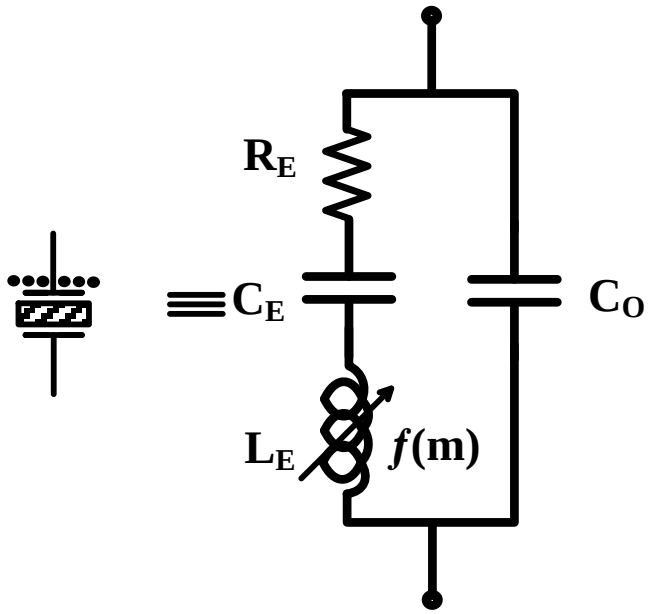


Figure 2.5 Change in inductance with adsorption of gas on the CMUT's plate.

From equation 2.2 we can see that increase in L_E will decrease both the parallel and the series

resonant frequencies. Also the resonant frequency has inverse square root dependency on L_E. Series and parallel frequencies will vary as $L_E^{-1/2}$. Fig. 2.6 represents the variation in series and parallel resonant frequencies with respect to change in L_E. So presence of the target gas in the environment will change the impedance profile (i.e., series and parallel resonant frequencies) of the CMUT.

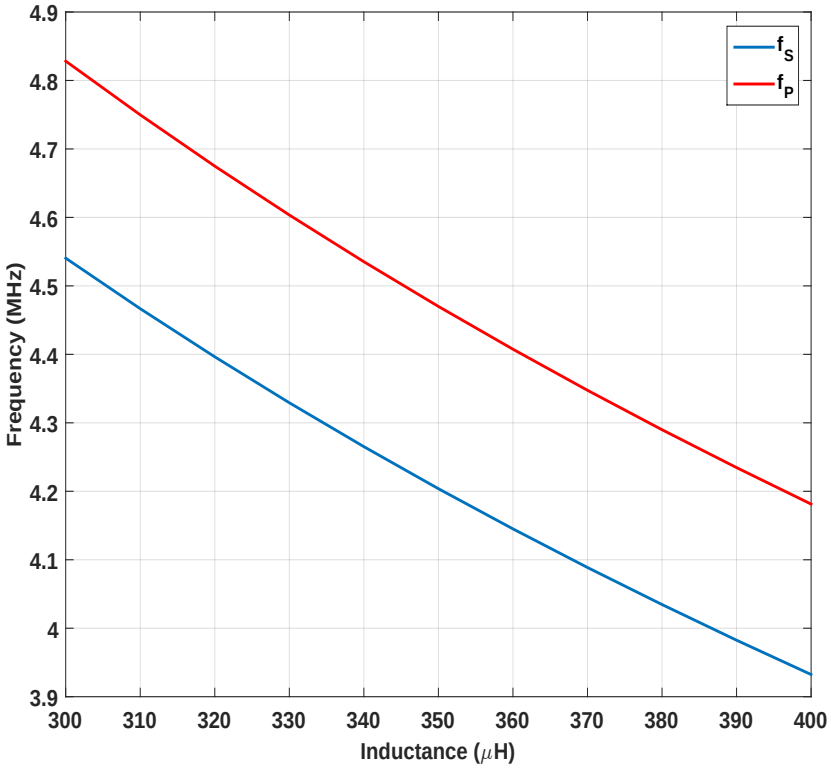


Figure 2.6 Series (f_s) and parallel (f_p) resonant frequencies vs inductance (L_E).

2.4 Impedance-to-Frequency Conversion

In Section 2.3 we discussed about making the CMUT impedance profile a function of the targeted gas present in the environment. For ease of processing, storing, and analyzing the information the impedance information of the CMUT needs to be converted to a voltage or current equivalent. There are different ways of performing this conversion.

1) Using an impedance analyzer.
2) Utilizing the ring down measurement method.
3) Using the CMUT in the feedback loop of an electrical oscillator.
The main advantage of using the CMUT in the feedback loop is that it is easier to do the power-noise optimization. Another advantage is that the changes in the resonant frequency can be tracked in real-time. An impedance analyzer needs a frequency sweep. Ring-down method needs ping and measure approach. An oscillator structure is interfaced with the CMUT to convert the impedance information into a sinusoidal signal. Optimizing an oscillator for power or noise performance is well analyzed.
In the remainder of this section we will discuss the third approach. Two different methods of analyzing the oscillators, i.e., 1-port model and closed loop analysis will be discussed.

2.4.1 1-Port Model

In the 1-port model approach we analyze the CMUT and the active circuit using 1-port impedance models [16]. CMUT is operated near its parallel resonant frequency due to the higher Q-factor (lesser loss). Near the parallel resonant frequency the CMUT can be modeled as a lossy inductor, i.e., positive reactance with resistance in series. Colpitts oscillators oscillate near the parallel resonant frequency and hence are suitable for use with CMUT resonators. Fig. 2.7(a) represents the CMUT's model near the parallel resonant frequency. Now for converting this impedance profile, i.e., $R_e + j \cdot X_e$, to an impedance profile, which can sustain the oscillations, we need R_a and X_a such that [17]

$$|R_a| > R_e \tag{2.6}$$

$$|X_a| = |X_e| \tag{2.7}$$

So the resistance provided by the active circuit (R_a) should be negative and greater in magnitude compared to the CMUT's lossy resistance and the capacitance should be such that the reactance of the active circuit (X_a) will cancel the inductor's reactance (X_e). Once equations 2.6 and 2.7 are satisfied at a certain frequency we have capacitive and inductive reactances canceling out and also the net resistance of the whole system is negative which means the system is acting as a source of energy at that frequency. So there will be a frequency at which the reactance is zero and the resistance will be negative and we will observe oscillations at that particular frequency.

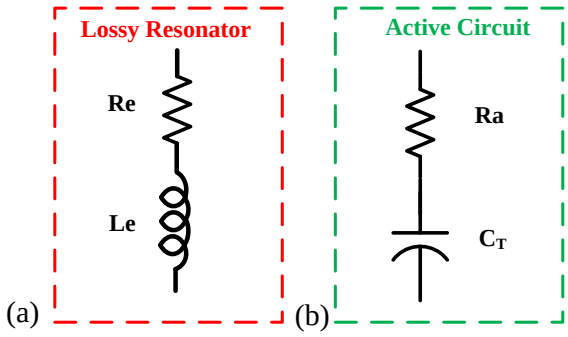


Figure 2.7 (a) CMUT impedance model near the parallel resonance. (b) Active circuit impedance profile required to resonate the CMUT.

2.4.2 Closed Loop Analysis

Feedback is another way of analyzing the conversion of CMUT's impedance into frequency. Stable analog systems are designed with negative feedback and adequate phase margin, but for oscillators we need to meet the Barkhausen criteria. Barkhausen criteria state that at a certain frequency ω_{OSC} loop gain should be more than unity and phase should be an integer multiple of 2π. Equations 2.8 and 2.9 represent the Barkhausen criteria [16, 18]. Once this condition is satisfied at the ω_{OSC} frequency even a small disturbance will cause oscillation. As there is zero phase difference when the signal travels the entire loop and the loop gain >1, so when the signal comes back it is in same phase and higher in magnitude. So this process keeps on going until the signal goes rail-to-rail. But this model is a linear model and as the signal changes the amplifier gain also changes. This generally limits the amplitude swing of the oscillation. So for the Colpitts oscillator we generally see sinusoidal oscillations.

After the impedance information is converted into a voltage oscillating at a certain frequency, the magnitude of the oscillation is still small and we need a circuit to make the amplitude go rail-to-rail before feeding the signal into a digital counter. An amplifier or a comparator can be used to make this oscillation signal rail-to-rail. This helps in processing the signal in digital domain. One should note that if the oscillations are very small in magnitude, then the offset and noise of the following amplifier or comparator will limit the accuracy of the digital frequency counter.

$$|A(j\omega_{OSC})\beta(j\omega_{OSC})| = 1 \tag{2.8}$$

$$\angle(A(j\omega_{OSC})\beta(j\omega_{OSC})) = 2n\pi, n \in 0,1,2,... \tag{2.9}$$

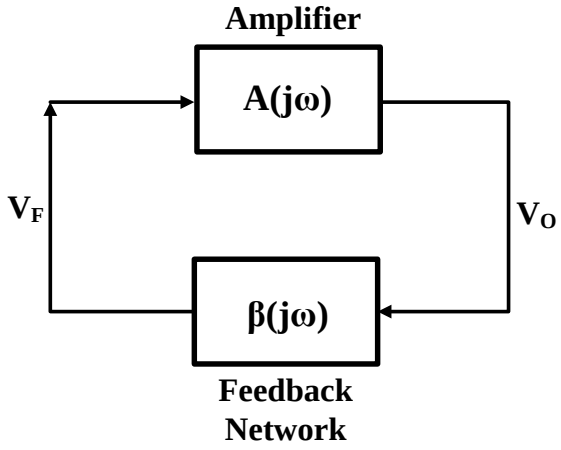


Figure 2.8 Feedback loop representation of oscillators.

2.5 Measuring the Oscillation Frequency

In the last section we discussed about converting the impedance information into a voltage oscillating at a certain frequency and using an amplifier or a comparator to convert this sinusoidal signal into a digital clock. In this section we will discuss how we can measure the frequency of this digital clock. Main idea here is to count the number of edges in a certain duration of time and based on that count and time information a frequency number is calculated. The accuracy of the calculated frequency depends on the measurement time also known as the gate time.

In Fig. 2.9(a) we can observe the gate time is exactly an integer multiple of T_{CLK}. So the number of rising edges of CLK (N) will be an integer multiple of T_{CLK}. In Fig. 2.9(b) we can observe from the graph that we have almost missed one complete clock cycle so number of rising edge count will be one less than an integer multiple of T_{CLK}. Similarly in Fig. 2.9(c) we can observe that we have counted almost one extra rising edge of clock, so our rising edge count will be one more than an integer multiple of T_{CLK}. These observations can be represented by equations 2.10, 2.11, and 2.12 [19–21].

$$t_{gate} = N \cdot T_{CLK} \tag{2.10}$$

$$t_{gate} = N \cdot T_{CLK} + T_{CLK} \tag{2.11}$$

$$t_{gate} = N \cdot T_{CLK} - T_{CLK} \tag{2.12}$$

As the output of the oscillator is not synchronized with the t_{gate} signal, t_{gate} and $Freq$ (frequency

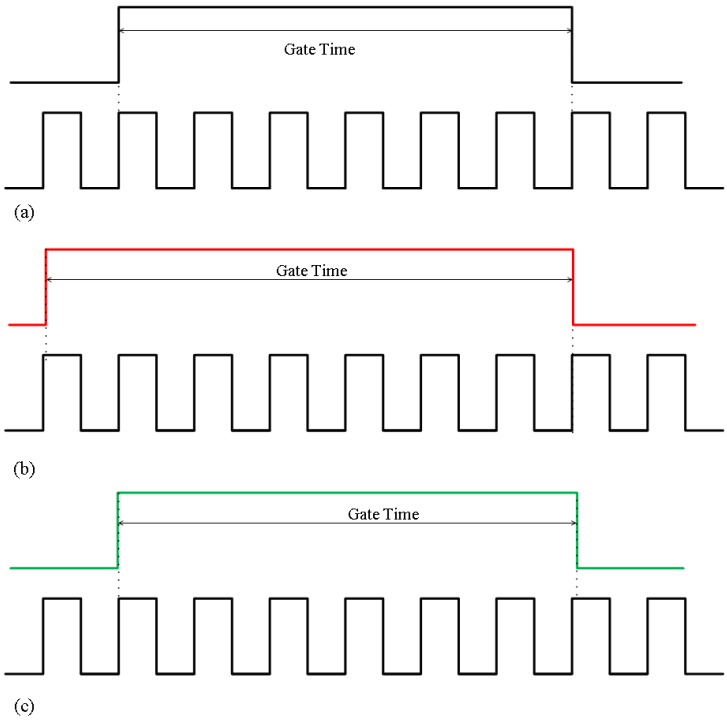


Figure 2.9 (a) Clock is an integer multiple of gate time. (b) One clock cycle is missed during the gate time. (c) One clock cycle is counted extra during the gate time.

of the input digital clock with time period T_{CLK}) can come in any order. Fig. 2.9(a) represents the best case scenario where we can count the clock accurately. Fig. 2.9(b) and Fig. 2.9(c) represent worst case scenarios where we have the maximum error and a little bit of less or extra time respectively will make the error zero again. So we can safely say that

$$t_{gate} = N \cdot T_{CLK} \pm T_{CLK} \tag{2.13}$$

Equation 2.13 can be modified to show the relation between $Freq$ and t_{gate}.

$$t_{gate} = (N \pm 1) \cdot T_{CLK} \tag{2.14}$$

$$Freq = \frac{1}{T_{CLK}} \tag{2.15}$$

$$t_{gate} = \frac{N \pm 1}{Freq} \tag{2.16}$$

$$Freq = \frac{N \pm 1}{t_{gate}} \tag{2.17}$$

For simplicity we can also write this as

$$Freq = \frac{N}{t_{gate}} \pm \frac{1}{t_{gate}} \tag{2.18}$$

This equation is very useful as it shows the relationship between $Freq$, N and t_{gate}. This also shows the error in $Freq$ measurement for a certain gate time. We can see from equation 2.18 that error is inversely proportional to the gate time (t_{gate}). For example a t_{gate} of 10 ms will give an error of ±100 Hz in $Freq$ measurement. Similarly a t_{gate} of 1 s will give an error of ±1 Hz in $Freq$ measurement. The frequency counter is implemented using an asynchronous counter which has a parallel output. So, we need a parallel-to-serial converter which will be discussed in Chapter 3 in more detail.

2.6 Complete System Level Overview

In this chapter we discussed how the complete measurement is performed from a system-level perspective. Fig. 2.10 represents the complete signal flow from the CMUT to the final digital output. In Fig. 2.10 the oscillator input is interfaced with the CMUT and output of the oscillator is fed to a sine-to-square wave converter for making the signal rail-to-rail, which then is fed to the digital frequency counter followed by a parallel-to-serial converter.

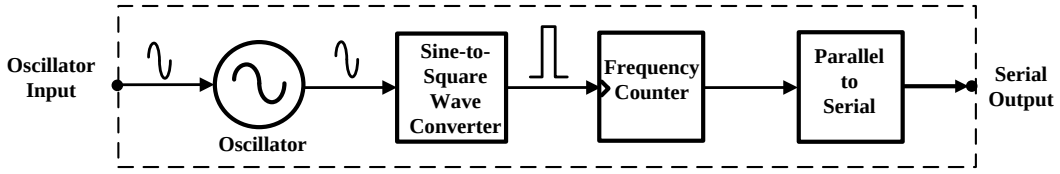


Figure 2.10 Block diagram representing signal flow from the CMUT to the final digital output.

In Chapter 3 we will discuss in more detail the design of the circuits to meet the specifications dictated by the overall system.

CHAPTER

3

CIRCUIT DESIGN

In Chapter 2 we discussed from the system-level point of view how to use a CMUT as a gas sensor and then how we can convert the sensed gas concentration information into a digital output. In this chapter we will discuss in detail the circuit design and associated trade-offs.

3.1 Colpitts Oscillator Design

In this section we will discuss the design of the BJT-based Colpitts oscillator. We will discuss in detail regarding optimizing the design for power consumption. First optimizing the capacitance values for power is discussed, followed by a description of biasing the BJT in correct region of operation. Finally the complete schematic and simulation results of loop gain as well as the transient response will be presented.

3.1.1 1-Port Model

As discussed in Section 2.4.1 in the 1-port model approach we compensate for the loss of the resonator with an active circuitry. The CMUT resonator near its parallel resonant frequency can be modeled using a lossy inductor model. One point to note here is that although we represent the CMUT as a lossy inductor, this model is valid for only very small range of frequencies. For

simulations it is more accurate to use the complete BvD model. Equation 3.1 gives the approximate CMUT impedance near the parallel resonant frequency.

$$Z_{CMUT} = R_e + j \cdot X_e \tag{3.1}$$

$$X_e = \omega \cdot L_e \tag{3.2}$$

In equation 3.1, R_e represents the resonator loss and the X_e represents reactance near the parallel resonant frequency and both are positive quantities. So to satisfy the condition for oscillations, the real part of the impedance looking into the active circuit should compensate for the loss, i.e., $|R_a| > |R_e|$ and the reactances should cancel out, i.e., $|X_a| = |X_e|$. Also as the active circuit is in series with the CMUT, R_a and X_a should be negative to cancel the CMUT impedance. The frequency at which this condition is met is the oscillation frequency. Also if the same circuit is considered using the feedback analysis we will meet the loop gain and loop phase criteria at the oscillation frequency.

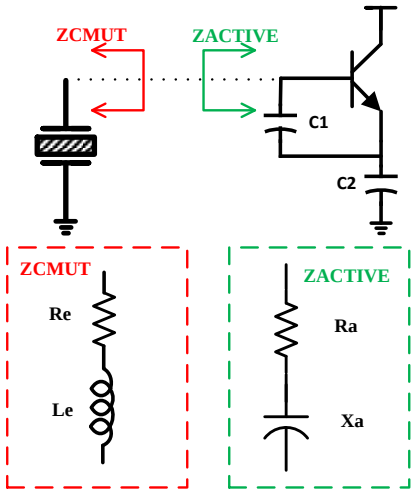


Figure 3.1 Impedance looking into CMUT and active circuit, here $X_a = -\frac{1}{\omega \cdot C_T}$ and $C_T = \frac{C_1 \cdot C_2}{C_1 + C_2}$.

3.1.2 Selecting the Optimum Capacitance Ratio

In the last section we discussed Colpitts oscillator from the one-port point of view [16]. Now we know that we need capacitances in order to cancel the reactive part of the CMUT impedance. In this section we will discuss how to optimally choose the capacitance ratio. Impact of the capacitance

ratio on the power consumption is analyzed. Choosing the right capacitance ratio and the right capacitance values help in reducing the power consumption. The application for the gas sensors is the wearable platforms. So the criteria for oscillator based design is to design for low-power.
The two main capacitances are C_1 and C_2 shown in Fig. 3.1(b). They are important in deciding the negative impedance looking into the active circuitry which can be seen in equation 3.3. Also their series combination, i.e., $C_T = \frac{C_1 \cdot C_2}{C_1 + C_2}$ is the effective capacitance looking into the active side. Negative resistance looking into the active circuit is given by

$$R_a = \frac{-g_m}{\omega^2 \cdot C_1 \cdot C_2} \tag{3.3}$$

From equation 3.3 we can see that the negative resistance looking into the active circuit depends on the product of C_1 and C_2. So we have to minimize this product to achieve the minimum g_m for a frequency near the parallel resonant frequency. C_T will be resonating with the CMUT's reactance. So for a fixed CMUT resonator profile C_T required is also fixed. For achieving the fixed value of C_T any ratio of C_2 to C_1 can be chosen. In the following equations we will see the trade-off in

$$C_T = \frac{C_1 \cdot C_2}{C_1 + C_2} \tag{3.4}$$

$$\text{Assuming } C_2 = k \cdot C_1 \tag{3.5}$$

$$C_T = \frac{C_1 \cdot k \cdot C_1}{C_1 + k \cdot C_1} \tag{3.6}$$

$$\Rightarrow C_T = C_1 \cdot \frac{k}{k+1} \tag{3.7}$$

$$\Rightarrow C_1 = C_T \cdot \frac{k+1}{k} \tag{3.8}$$

$$\text{Hence } C_1 = C_T \cdot \frac{k+1}{k} \tag{3.9}$$

$$C_2 = C_T \cdot k + 1 \tag{3.10}$$

$$\text{Now } C_1 \cdot C_2 = C_T^2 \cdot \frac{(k+1)^2}{k}; \text{here } C_T \text{ is constant} \tag{3.11}$$

$$\text{So we have to minimize } \frac{C_1 \cdot C_2}{C_T^2} = \frac{(k+1)^2}{k} \tag{3.12}$$

$$\text{Differentiating } \frac{d}{dk} \cdot \frac{(k+1)^2}{k} = 0 \tag{3.13}$$

$$\text{we get } k = 1 \Rightarrow C_1 = C_2 \tag{3.14}$$

Plotting equation 3.12 we can observe the minimum is achieved when $k = 1$. The same equation has been plotted in Fig. 3.2 and it shows the minimum value for $k = 1$. Same results are obtained

analytically from equation 3.13.
So we know now that $C_2 = C_1$ will give us the minimum value of $C_1 \cdot C_2$. Now in the next section we will discuss how to find the absolute value of these capacitances.

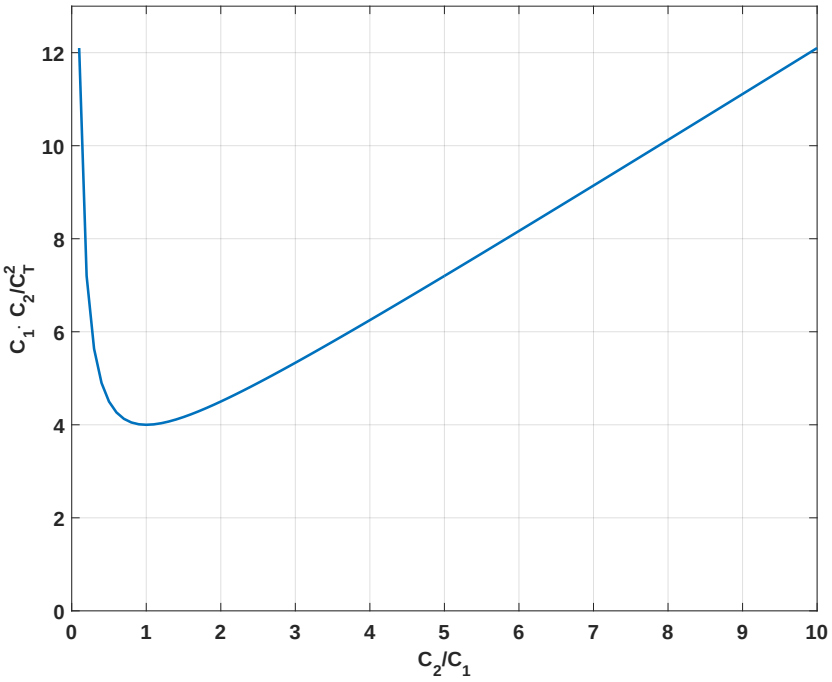


Figure 3.2 Selecting the optimum capacitance ratio for minimizing the g_m.

3.1.3 Selecting the Optimum Capacitance Value

Now we know that $C_1 = C_2$ will give us minimum in the product of equation 3.3. We can simplify the equations more from here to see what will give the minimum g_m value. We need to minimize the g_m value because this directly decides the DC bias current of the BJT and hence power consumption of the oscillator. We know that

$$X_a = -X_e \tag{3.15}$$

$$|R_a| > R_e \tag{3.16}$$

i.e., reactance of the CMUT and the active circuit should be equal and opposite in sign and negative resistance looking into the active circuit should be greater than resistance looking into the CMUT. Also we know that R_a has minimum value R_e. Now modifying equation 3.3 we get

$$g_m = -R_a \cdot \omega^2 \cdot C_1 \cdot C_2 \tag{3.17}$$

$$C_1 = C_2; |R_a| > R_e \tag{3.18}$$

$$g_m > R_e \cdot \omega^2 \cdot C_1 \cdot C_1 \tag{3.19}$$

$$C_1 = C_2 = 2 \cdot C_T \tag{3.20}$$

$$g_m > 4 \cdot R_e \cdot \omega^2 \cdot C_T^2 \tag{3.21}$$

$$\text{Here } \omega \cdot C_T = \frac{1}{X_e} \tag{3.22}$$

$$\text{So } g_m > \frac{4 \cdot R_e}{X_e^2} \tag{3.23}$$

From equation 3.23 we can see the g_m depends directly on the real part of CMUT impedance and inversely proportional to the square of imaginary part of CMUT impedance. Fig. 3.3 represents equation 3.23. From the figure we can observe there is a minimum g_m value. By zooming in the region of parallel resonance, we can calculate the minimum g_m (Fig. 3.4). From this we can calculate first the capacitance values by calculating the X_e in the region, where g_m is minimum and then calculating C_T using equation 3.22 and then C_1 and C_2 using equation 3.20. Also we can get the DC bias current information from g_m and I_E relation shown in equation 3.25. General rule of thumb is to keep g_m at least 4 times of the minimum required value for having proper startup.

$$g_m = \frac{I_C}{V_T} \simeq \frac{I_E}{V_T} \simeq I_E \cdot 40 \tag{3.24}$$

$$I_E \simeq \frac{g_m}{40} \tag{3.25}$$

3.1.4 DC Biasing

Biasing the active circuitry for the right DC operating point is very important. The biasing should be such that it biases the BJT in the correct operating region without loading the loop. Any loading to the loop means we need to burn more power to achieve the oscillation. Also after we have fixed the capacitance values for the resonator and we know the g_m required for the design, we can calculate

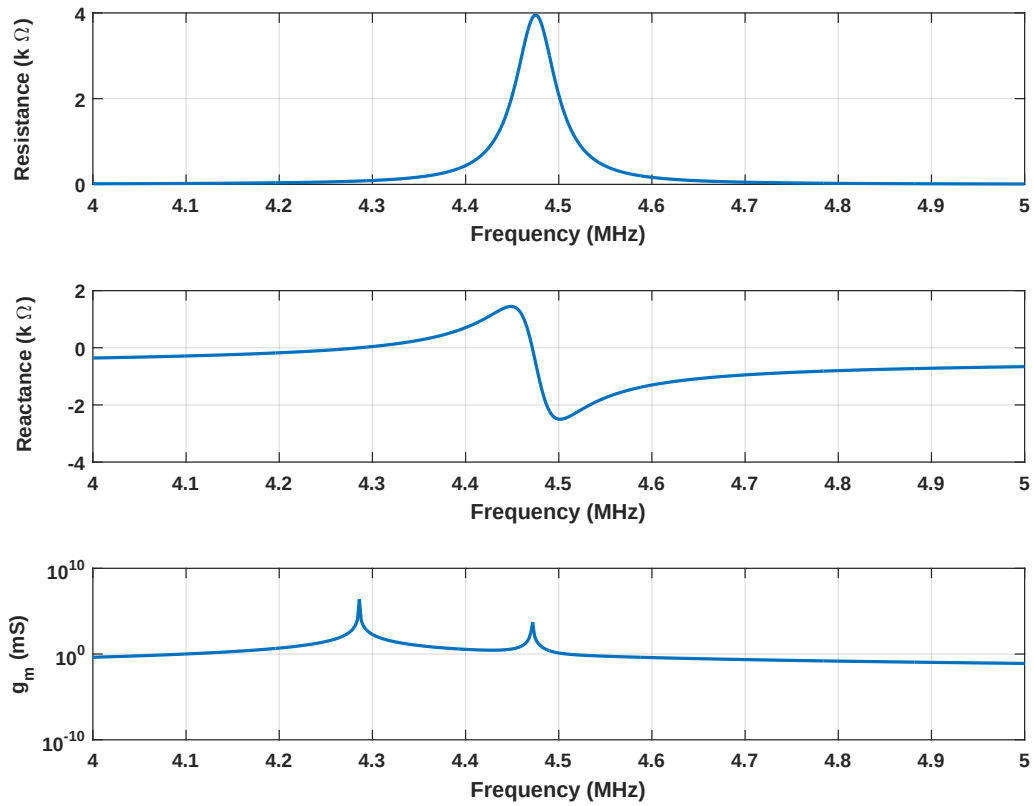


Figure 3.3 Finding optimum capacitances for minimizing the g_m for a given resonator profile.

the bias current required from equation 3.25. Fig. 3.5 shows two ways of biasing. In Fig. 3.5(a) there are two resistances used to bias the oscillator. Here R_{BIAS} is the one which mainly sets the current. Based on this set current value there is a base current (I_b), which flows through R_1. So the base voltage will be $V_{DD} - I_b \cdot R_1$. This voltage should be such that the base-emitter junction is forward biased and the collector-base junction is reverse biased.

There are mainly two problems in using R_{BIAS} as a resistance at the emitter for biasing:

1) As we need a certain V_{BE} for the base-emitter junction to be in forward bias this limits the oscillator swing as a fixed current R_{BIAS} will use up certain voltage difference. So V_{DD} required in this case will be higher than the current biased scheme.

2) Compared to the resistance based bias, a current source will consume less voltage difference. Also

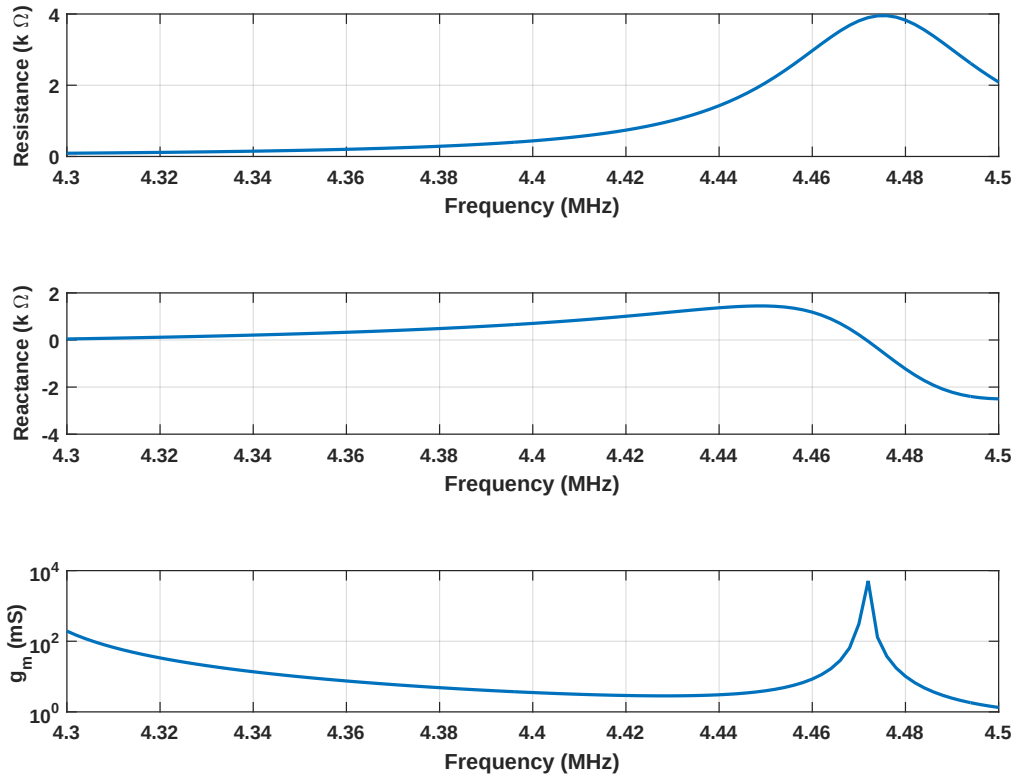


Figure 3.4 Finding optimum capacitances for minimizing the g_m for a given resonator profile (zoomed).

output resistance of the current source (r_o) will be very high so it will not load the BJT in feedback loop much. So all the AC current in the loop flows through the resonating capacitance and then through the CMUT resonator which gives better and more stable oscillations.
So, for better performance and current control the topology mentioned in Fig. 3.5(b) is used. Also the bias resistance at the base is better than using a voltage divider from V_{DD} to V_{Base} and Gnd because it will save board space of one more element and we can use higher resistance by avoiding the divider configuration and hence avoiding the loading of the CMUT resonator. However this loading is very minimal in the first place.

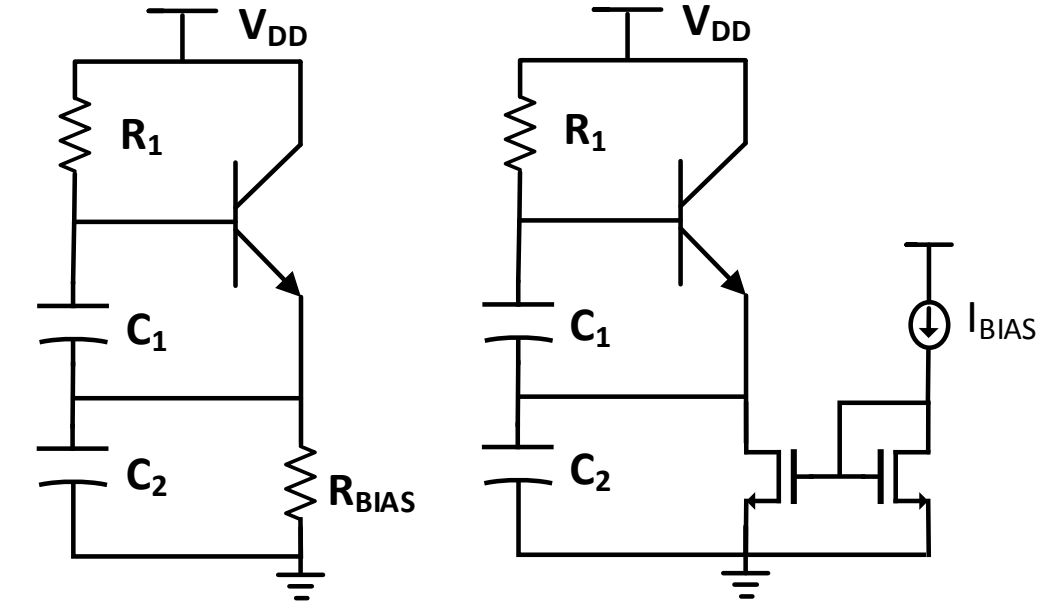


Figure 3.5 (a) Resistive DC biasing. (b) Current source based DC biasing.

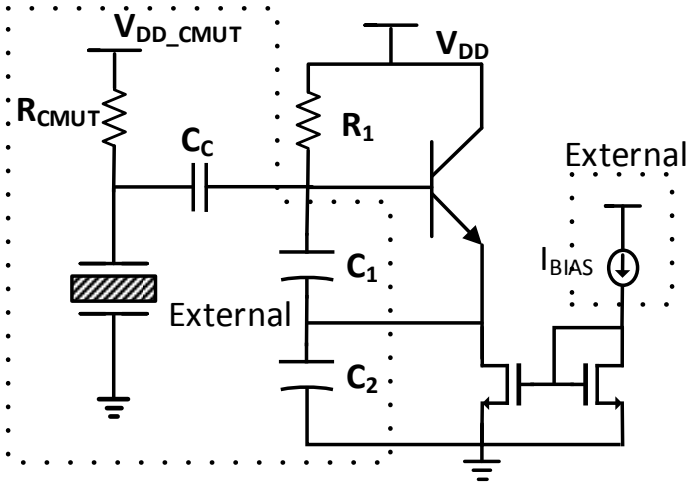


Figure 3.6 Complete schematic with BJT-Colpitts oscillator interfaced with CMUT.

3.1.5 Complete Oscillator Design Interfaced with CMUT

Fig. 3.6 shows the complete BJT-based design. In this implementation the current-based biasing is used. An external current source is used and that current is mirrored inside the chip to bias the BJT. A resistor connected from V_{DD} to the base of the BJT is used to bias the base. This resistance keeps the collector-base junction reverse biased. Also the capacitance values are decided based on the resonator impedance profile. Fig. 3.7 shows the loop gain of the BJT-based Colpitts oscillator. From the figure we can infer that Barkhausen criteria are satisfied, i.e., the loop gain magnitude is greater than one for the frequency where the phase is zero. Generally parasitic capacitive loading at the transducer node has an effect on this loop gain which makes the oscillator difficult to oscillate. Each node's parasitics were used for the final simulation to ensure that the Barkhausen criteria are met. Fig. 3.8 shows the simulation results of the Colpitts oscillator in a circuit simulator (Virtuoso,

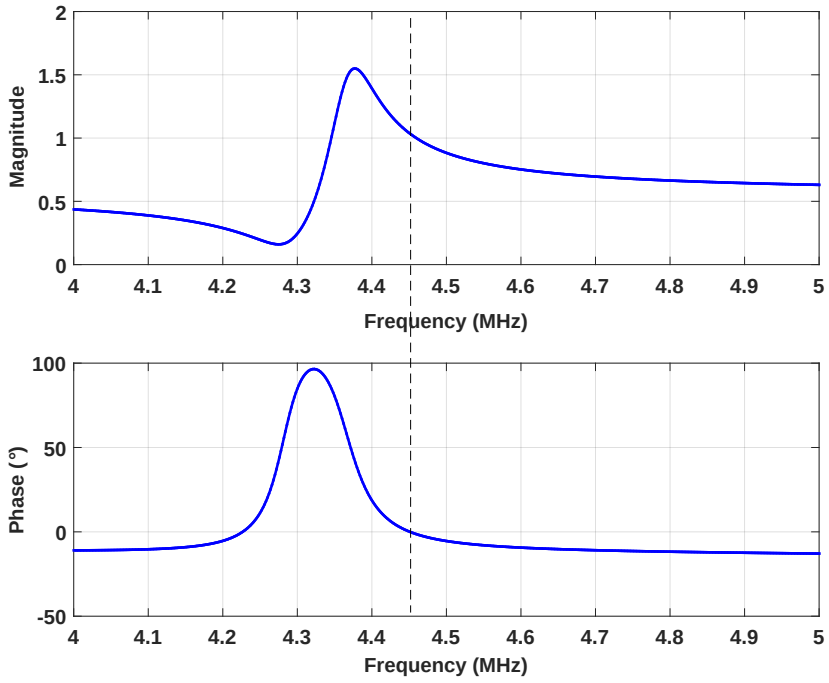


Figure 3.7 Simulated loop gain of BJT-based Colpitts oscillator interfaced with CMUT.

Cadence Design Systems, San Jose, CA). For simulations to be more accurate the maxstep was set to

$\frac{1}{5\cdot10^6\cdot100}$ ($\frac{1}{100^{th}}$ of oscillation time-period). This is just to ensure that we have sufficient number of steps in one oscillation period. For the complete system-level simulation maxstep time was relaxed to $\frac{1}{5\cdot10^6\cdot20}$. This helped in speeding up the simulation time. Also the algorithm was set to traponly as this gives more accurate results for the simulation of a circuit like an oscillator [22].

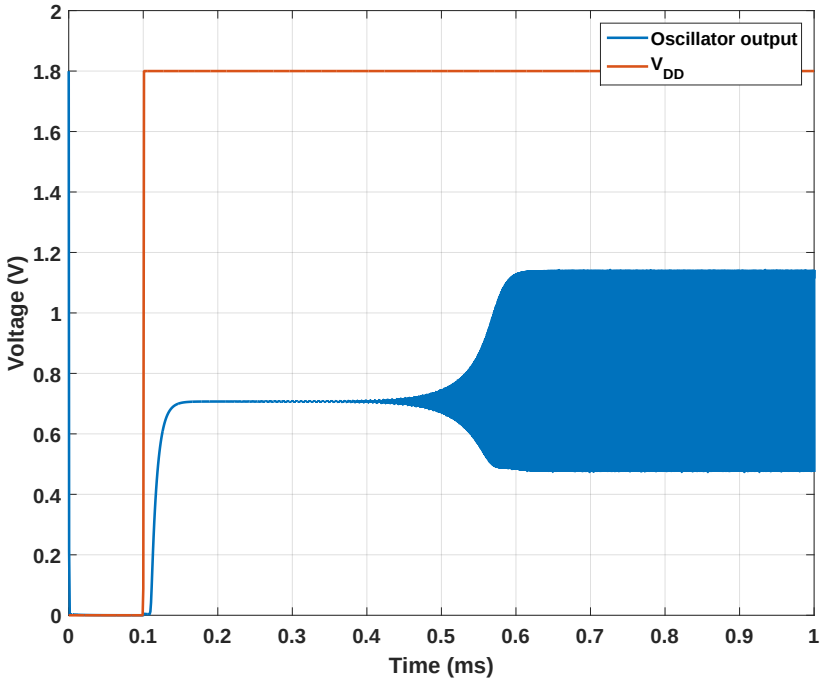


Figure 3.8 Simulated start-up transient of BJT-based Colpitts oscillator.

Fig. 3.9 shows the steady-state waveform of the BJT-Colpitts oscillator. From this we can observe that the oscillation peak-to-peak amplitude is around 0.6 V, which is centered around 0.8-V DC. The simulation results showed a startup time of around 500 μs.

3.2 Inverter-Based Oscillator Design

In this section we will discuss the second oscillator topology used in the IC implementation. The main drawback in Colpitts design is that the optimal capacitive divider is different for different CMUT resonators. With the intention of a single circuitry, which can be applicable for different

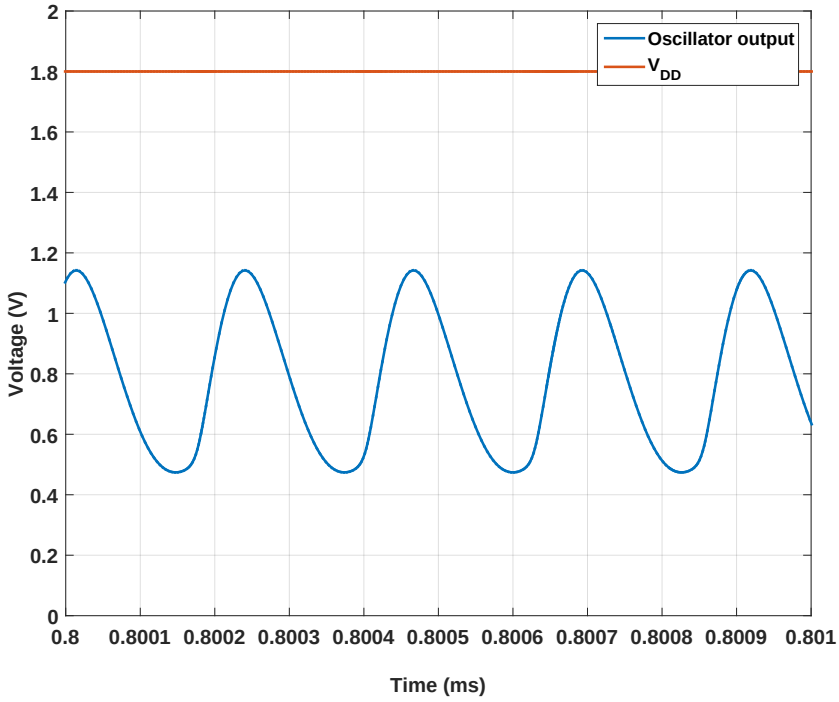


Figure 3.9 Simulated steady-state waveform of BJT-Colpitts oscillator.

CMUT resonators an inverter-based oscillator is designed.
In this section first we will go through the biasing of the inverter to get the maximum gain. Then we will discuss the complete topology of the inverter-based oscillator along with the loop simulation and transient simulation results.

3.2.1 Self Biased Inverter

Inverter is the most common block in digital circuits where it is always in the extreme region of operation, i.e., either fully on or fully off, but for the oscillator design purpose we need to use the inverter in the on-off transition region. If biased correctly both PMOS and NMOS will be in saturation which will give the gain. Fig. 3.10 shows the DC characteristics of an inverter for different process corners, i.e., Fast Slow (FS), Typical Typical (TT) , Slow Fast (SF). We can notice for different corners the transition edge is different. That means if we try to apply a fixed DC voltage to bias the inverter in the on-off transition region, the region of operation may vary from die to die. Also we can notice that the $\frac{dV_{OUT}}{dV_{IN}}$, i.e., input to output gain goes to maximum value when $V_{IN} = V_{OUT}$. So if we can

bias the inverter such that input and output track each other then we do not need to worry about die-to-die variations.

Fig. 3.11 shows one way of achieving $V_{IN} = V_{OUT}$. Here feedback is utilized to impose DC input

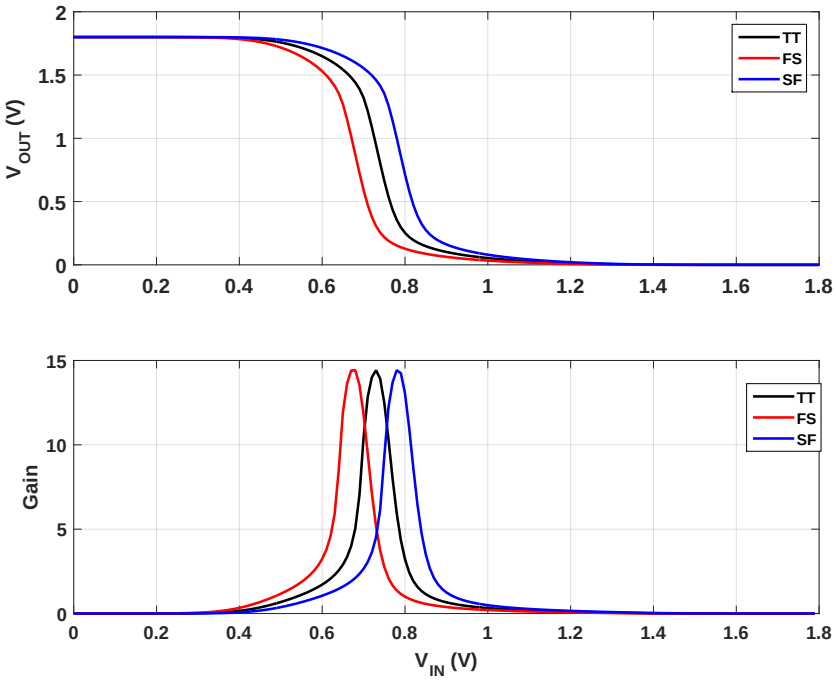


Figure 3.10 Simulated DC characteristics and gain of inverter for different corners TT (typical-typical), FS (fast-slow), SF (slow-fast).

voltage equal to output DC level. R_{FB} shown in Fig. 3.11 makes the DC input and output voltage same. This is important in the sense that any change in the MOSFET threshold voltage (V_t) or any other process, voltage, or temperature variation will make the DC characteristics of the inverter different and the feedback will adapt to those changes and will change the DC operating point of the inverter.

3.2.2 Inverter-Based Oscillator Topology

In this section the topology utilizing the inverter as a gain stage is discussed and the loop gain and the transient simulation results will be presented. Fig. 3.12 shows the complete implementation of

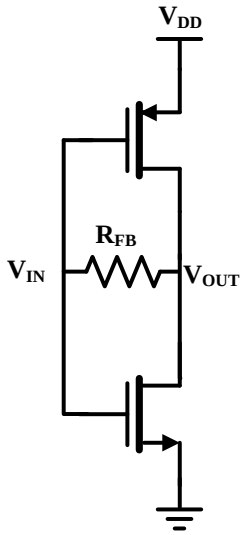


Figure 3.11 Self-biased inverter configuration.

the inverter-based oscillator interfaced with the CMUT. Here R_{FB} is used for adaptive biasing of the first inverter. Matching between the first inverter and the second inverter stages is very important. Matching helps in keeping the DC transfer characteristics of the two inverters same. This was taken care of in the layout by using center of symmetry approach and also placing dummy transistors around the main transistors. This was done to have the same environment for transistors in both inverters and hence better matching. Having better matching avoids using additional feedback resistor for the second inverter stage. With R_{FB} the input and the output of the first inverter is biased to the same DC value. So having same DC characteristics for the two inverters means that the output of the first inverter will bias the second inverter in the same region as the first inverter. Main idea here is to meet the Barkhausen criteria near the parallel resonance of the CMUT. The topology can be considered similar to the one shown in Fig. 2.8. As the back-to-back inverters will have high DC gain, the external C_{FB} reduces the gain at the lower frequencies. Near the CMUT resonant frequencies the C_{FB} should be almost short and the second inverter stage is loaded by the CMUT. We know CMUT's impedance will be high in the parallel resonance regime which will reduce the loading. So near the parallel resonance the magnitude of the loop gain will be very high and there will be a point where the phase shift around the whole loop is zero. At this frequency we will observe oscillations.

Fig. 3.13 shows the simulated loop gain of the inverter. As we can see the loop gain of the configuration is higher compared with the Colpitts oscillator based design. An advantage of this design is that

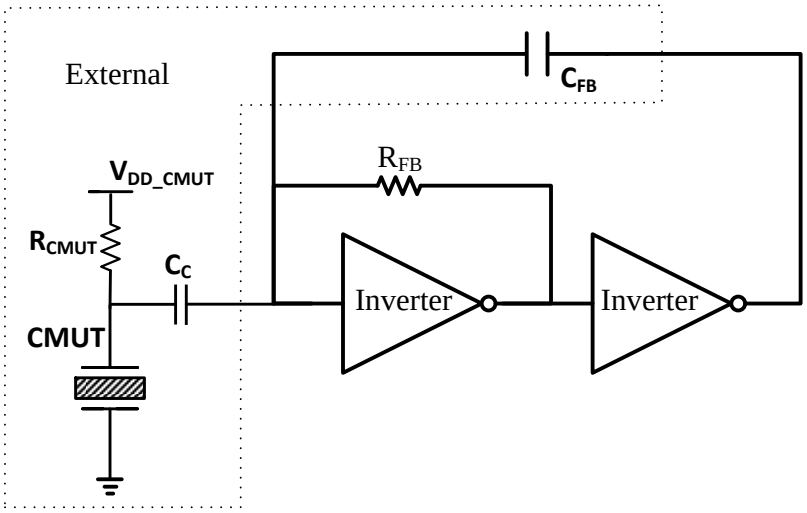


Figure 3.12 Complete schematic showing inverter-based oscillator interfaced with CMUT.

there is no external capacitive divider required to resonate the reactive part of the CMUT. So the same design can be used to resonate CMUTs with different resonating frequencies. From Fig. 3.13 we can observe that the loop gain is 9 for this design.

Fig. 3.14 shows the startup simulation of the oscillator circuit. Because of the higher loop gain the startup time is 20 μs, which is much shorter compared to the Colpitts oscillator's startup time (500 μs). Also the amplitude of the oscillation is much higher than the Colpitts design. Fig. 3.15 shows the steady-state oscillations. A peak-to-peak amplitude of 1.5 V was observed in a simulation for 1.8-V supply voltage.

3.3 Sine-to-Square Wave Converter

The output of the oscillator is an analog signal but the frequency counter needs a digital clock for counting the number of edges. So we need to convert the sinusoidal signal to a rail-to-rail digital signal. The main requirement from this sine-to-square wave converter is low power consumption, high gain, and it should preserve the duty cycle and phase information.

1) Low power consumption : As the whole system is intended for the ultra low-power applications the power consumption of the sine-to-square wave converter should be minimized. Generally for gas sensing systems oscillators are the most power consuming block. So the power consumption of the sine-to-square wave converter stage should be less than the oscillator.

2) High gain : The sine-to-square wave converter should have a sufficient gain around 5 MHz so that

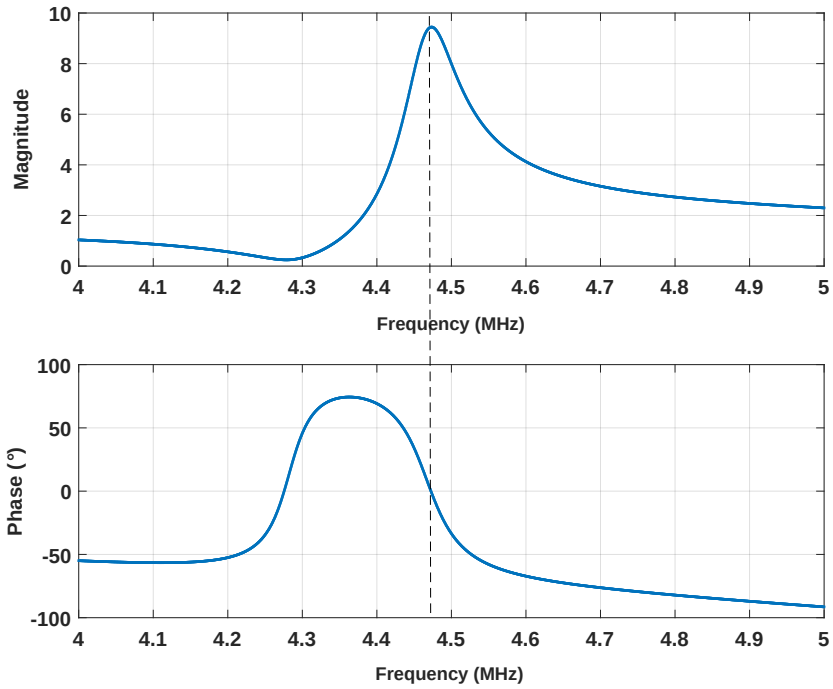


Figure 3.13 Simulated loop gain of the inverter-based oscillator design.

it can make oscillation signals of the order of millivolts to go rail-to-rail. So gain should be higher than 1000 assuming mV range oscillator output.

3) Preserving the duty cycle : The digital frequency counter accuracy depends on the duty cycle of the clock. So the sine-to-square wave converter should not distort the duty cycle of the analog oscillator signal.

Having multiple gain stages is thought to be helpful because as the signal is amplified offset and noise of further stages will have less impact on the duty cycle degradation of the sinusoidal signal. Preserving the duty cycle is important for increasing the accuracy in the digital frequency counter. Fig. 3.16 shows the designed sine-to-square wave converter. One advantage of this design is once the signal goes rail-to-rail the following inverter stages will have only the dynamic power dissipation and there will not be any static power dissipation in the following inverter stages.

Self-biasing inverters were used as single amplifier stages. The designed sine-to-square wave converter has a current consumption of 140 μA. This will be the worst case power consumption and it will reduce with the increasing oscillator signal swing. The gain around 5 MHz is around 70 dB, i.e., around 3000.

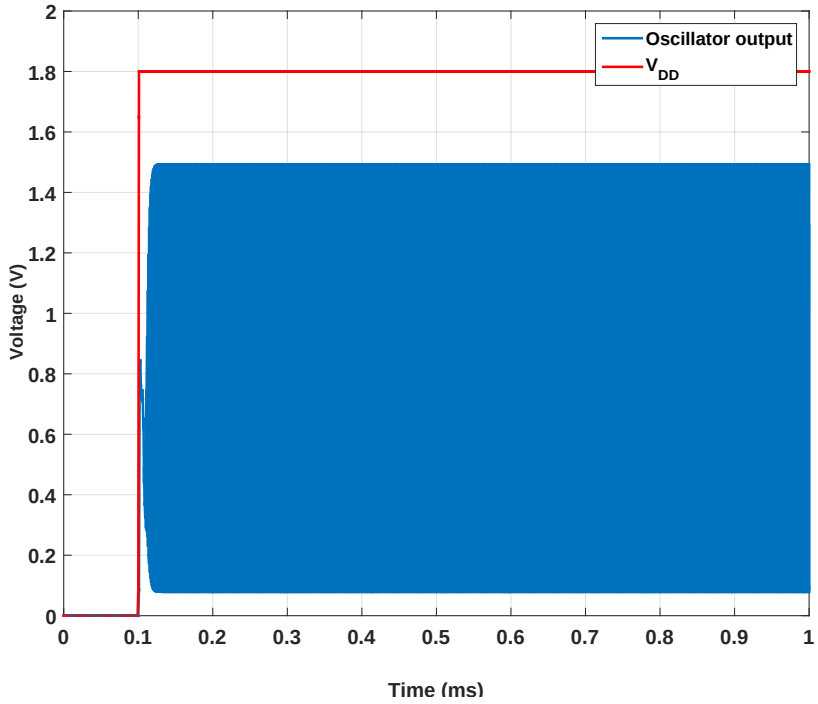


Figure 3.14 Simulated start-up transient of the inverter-based design.

3.4 Digital Frequency Counter

In Section 2.5 we discussed the trade-offs between the gate time and accuracy of measurement (equation 2.13). In this section we will discuss increasing the accuracy with the same gate time. Then we will discuss the implementation. Equation 2.13 is based on counting the clock edge once per cycle, if we count both the positive edge and the negative edge we can modify this equation as

$$t_{gate} = N_{double-edge} \cdot \frac{T_{CLK}}{2} \pm \frac{T_{CLK}}{2} \tag{3.26}$$

$$2 \cdot t_{gate} = N_{double-edge} \cdot T_{CLK} \pm T_{CLK} \tag{3.27}$$

$$t_{new} = N_{double-edge} \cdot T_{CLK} \pm T_{CLK} \tag{3.28}$$

$$Freq = \frac{N_{double-edge}}{t_{new}} \pm \frac{1}{t_{new}} \tag{3.29}$$

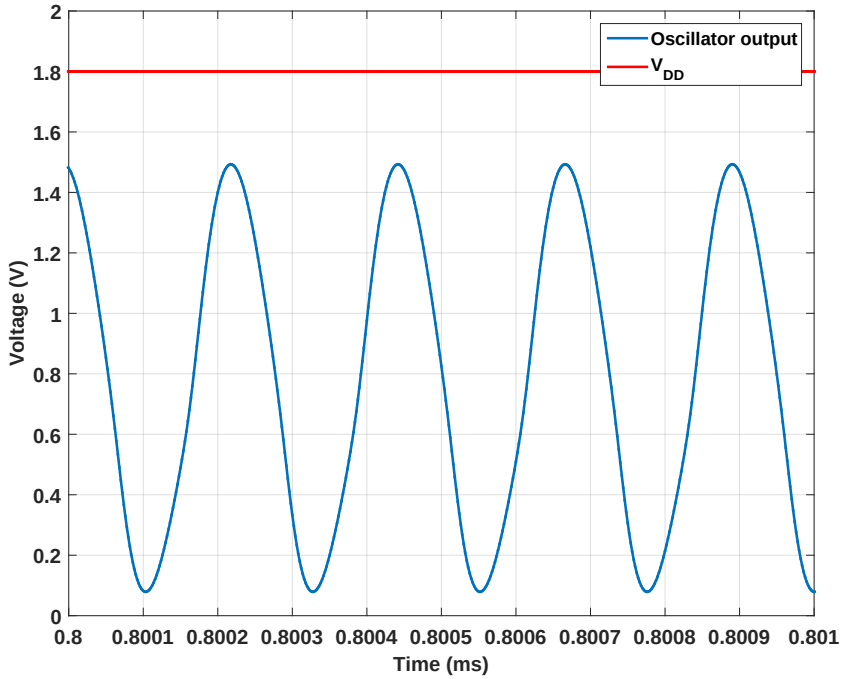


Figure 3.15 Simulated steady-state oscillation of the inverter-based design.

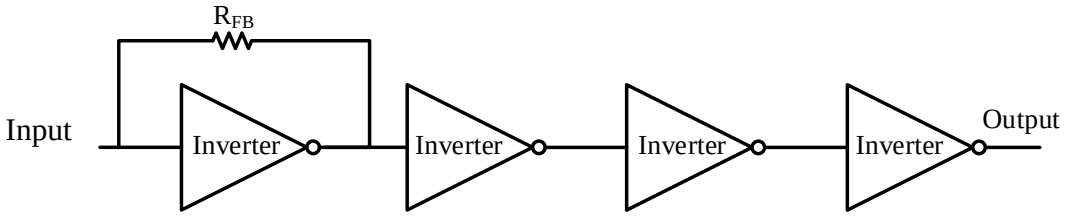


Figure 3.16 Schematic showing the sine-to-square wave converter.

From equation 3.28 and 2.13 we can infer that

$$t_{new} = 2 \cdot t_{gate} \tag{3.30}$$

Here t_{new} is the effective gate time with counting both negative and positive edges. So counting both edges is equivalent to having a gate time twice as long as the original gate time. Here one thing to note is that this equation is valid only if the oscillation signal has 50% duty cycle. That is the

reason we do not want any distortion in duty cycle from our sine-to-square wave converter stage. Fig. 3.17(a) shows the best case scenario for the double-edge counter. Fig. 3.17(b) and Fig. 3.17(c) show the worst case scenario for the double-edge frequency counting scheme. Another way of increasing the accuracy is to upconvert the frequency [23].

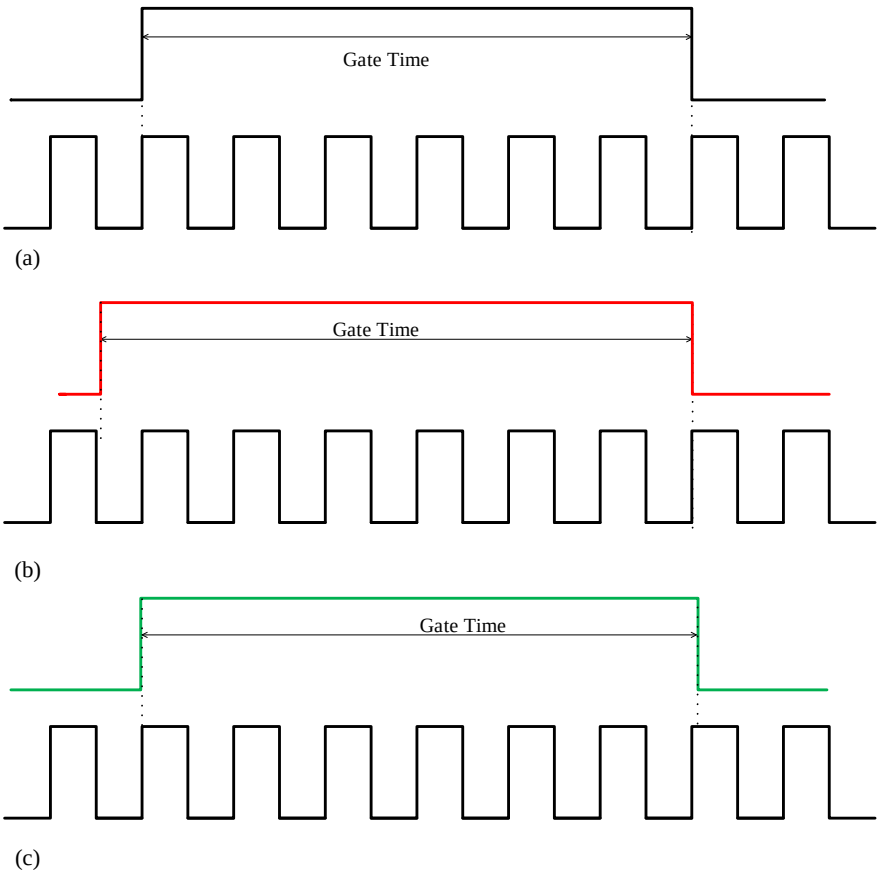


Figure 3.17 Digital frequency counter with both positive and negative edge counts (a) Clock is an integer multiple of gate time. (b) Half clock cycle is missed during the gate time. (c) Half clock cycle is counted extra during the gate time.

A single-edge counter was designed and to represent the least significant-bit (LSB) CLK or $\overline{CLK}$ was used. If CLK is low during the positive edge of the “Enable" (gate time control) then LSB is represented by CLK and if CLK is high during the positive edge of the “Enable” (gate time control) then LSB is represented by $\overline{CLK}$. Fig. 3.18 shows the double-edge digital frequency counter.

This is an asynchronous implementation of a digital frequency counter. As our signal is of very low speed compared with the logic delay of the technology used, the inherent delay from the LSB to MSB is not an issue in counting. At the negative edge of "Enable" (gate time control) the clock level

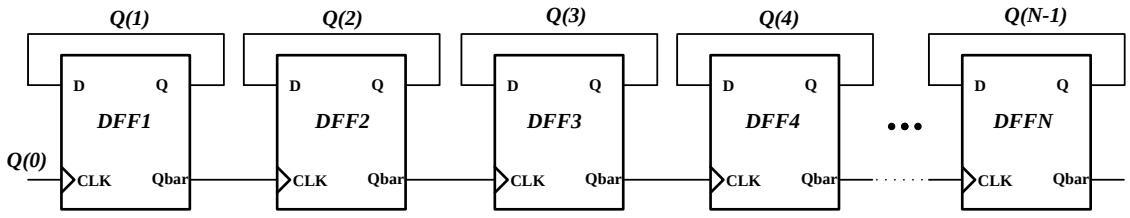


Figure 3.18 Dual-edge digital frequency counter

is latched and hence the counter value is latched and it stays the same until the "Resetb" (reset control) is applied. The "Resetb" (reset control) resets all the states stored in the flip-flops. Once the "Enable" (gate time control) goes low we have the equivalent of frequency count value available in digital format.

3.5 Parallel-to-Serial Conversion

For counting a 26-bit counter is used. This is done so as to count a 5 MHz signal with a gate time higher than 1 sec. Now once we finish the count we will have a 26-bit digital number and to transfer it in parallel fashion we would need 26 pins on the die which is not practical. As this data needs to be transmitted at a much lower rate than the input signal clock, which will be around 5 MHz, it is more efficient to convert this into serial data and with a low-frequency clock transmit the data serially using a single pin. For this reason after the counter a parallel-to-serial converter was used. Fig. 3.19 shows the block diagram of the designed parallel-to-serial converter. Once the "Enable" (gate time control) signal goes down, all the bits from the digital frequency counter are ready, i.e., $Q(0)-Q(25)$, and the final value is stored in the registers. A "Read" (read control) signal can be sent to switch these flip-flops to a series chain and the data can be read out in a serial manner using "F_{CLK}" (read clock).

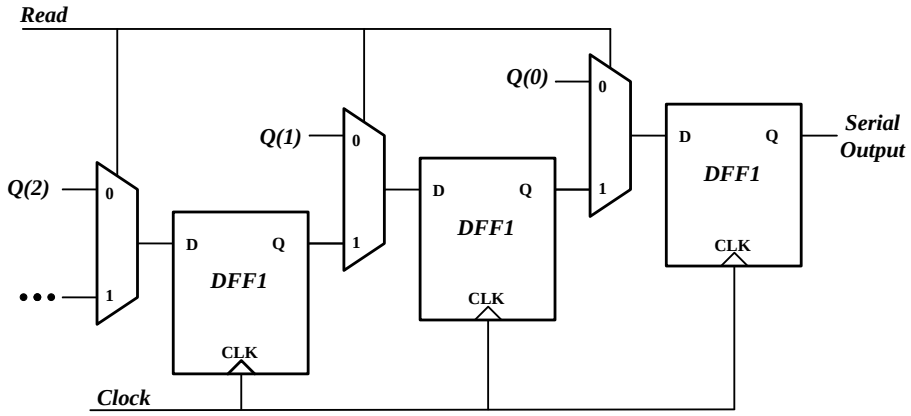


Figure 3.19 Parallel-to-serial interface.

3.6 Complete End-to-End System

Fig. 3.20 shows the complete end-to-end implementation of the whole system. The CMUT is interfaced at the "Oscillator Input" pin, the capacitive divider is connected between "Oscillator Input", "Oscillator Output", and "Gnd". “Oscillator select” control decides whether we want to interface Oscillator1 (BJT-Colpitts Oscillator) or Oscillator 2 (Inverter-based oscillator) to the CMUT. The oscillations are then amplified and fed to the frequency counter. There is an option to test the frequency counter standalone with an external clock “Test Clock”. Once the data is ready it is fed to the parallel-to-serial block, which needs “F_{CLK}” (read clock) and “Read” (read control) to convert the count value to serial data.

3.6.1 Timing Diagram

Fig. 3.21 shows the timing diagram for count and read operations in the system. Here “Output Clock" is the output of the sine-to-square wave converter. “Resetb" is the universal reset and “Resetb" ‘0’ resets all the flip-flops in the system. “Resetb" should be asserted ‘1’ at least some time before “Enable" is asserted ‘1’, just to give enough margin for the reset operation. One clock cycle should be more than enough, i.e., $\Delta t_1 \geq T_{CLK}$. “Enable" (gate time control) is kept high for a certain duration of time known as the gate time. At the negative edge of the “Enable" control the current count value is latched. This latched value is then read by using “Read” (read control) and “F_{CLK}” (read clock) signals. It is required to have one clock cycle difference between the falling edge of the enable signal and the rising edge of the read signal shown by t_2 in Fig. 3.21, i.e., $\Delta t_2 \geq T_{CLK}$.

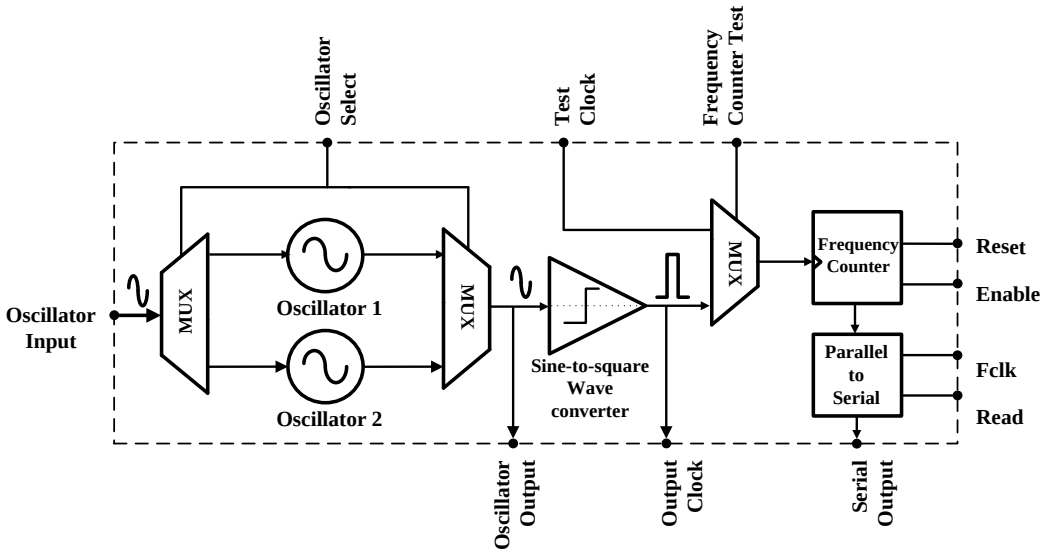


Figure 3.20 Complete end-to-end designed system.

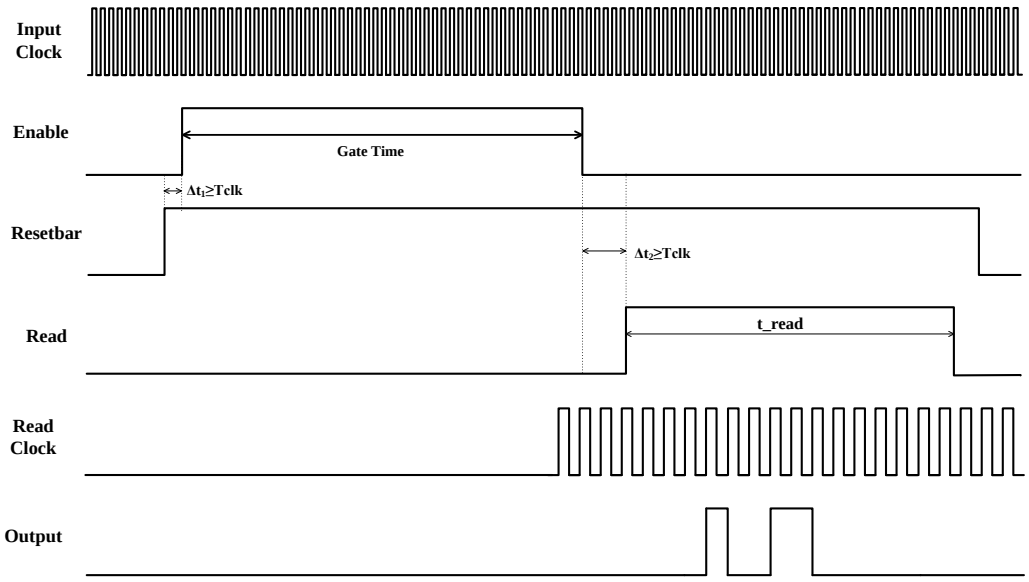


Figure 3.21 Timing diagram showing count and read operations of the system.

3.7 Layout Design

The complete system shown in Fig. 3.20 was designed in a 0.18-μm BiCMOS process (IBM 7WL) provided by MOSIS. Dummies were placed around the main analog blocks to reduce nwell proximity effect and unit element approach was used to have better matching. In order to achieve matching especially in the current mirror and the inverters, layouts were drawn to have the same center of symmetry. Furthermore, inverters were designed with larger sizes, i.e., W and L to have better matching. The digital part of the chip was designed using the digital standard cell library provided by the foundry. RC clamps were used for V_{DD} and V_{SS} protection and normal back-to-back diodes were used for the ESD protection of the input/output pins.
In the next chapter we will discuss the measurement results of the design described in this chapter.

CHAPTER

4

MEASUREMENTS

The complete system described in Fig. 3.20 was implemented in a 0.18-μm BiCMOS process (IBM 7WL) and a set of measurements were performed to test the functionality and performance of the system. This chapter describes the details of the various measurements performed.

4.1 Test Board Design

Fig. 4.1 shows the fabricated chip. An initial test board was designed as shown in Fig. 4.2(a). A 28-pin package (CQFJ, Kyocera Corporation, Kyoto, Japan) was used for placing the CMUT, the AFE chip, and CMUT biasing components and the resonating capacitances closer to each other. This was done to minimize parasitic loading to the CMUT and the oscillator. But the wedge bonder could not bond the aluminum bond wires to the surface mount 0402 pads, so the connections to the passive component side were made using silver epoxy. However, the system failed to produce any oscillations. The higher resistance of the silver epoxy when compared to bond wires is thought to be the reason for no oscillations on the board. This led to the design of a new board with electroless nickel immersion gold (ENIG) finish on the pads. The ENIG finish is used for making the pads wire-bondable as well as solderable. Additionally, the IC die and the CMUT were directly epoxied on the board and wirebonded directly to the pads on the board to reduce the onboard parasitics. The

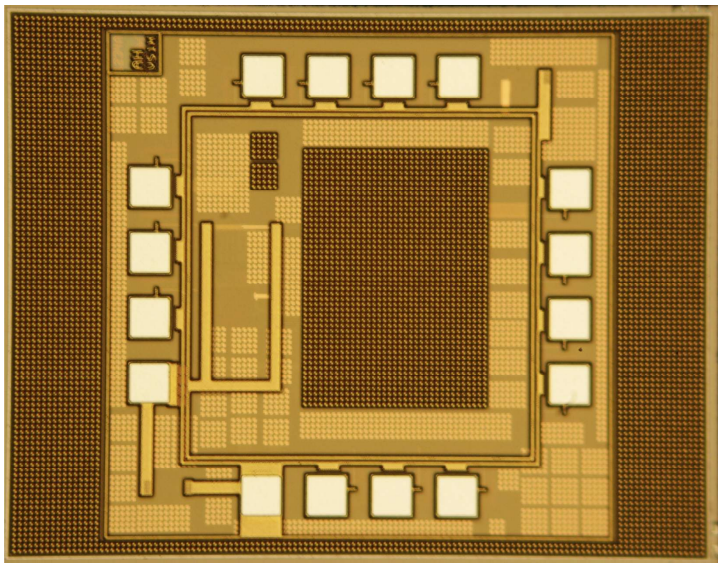


Figure 4.1 Micrograph of the analog front-end (AFE) fabricated in the IBM 0.18-μm process.

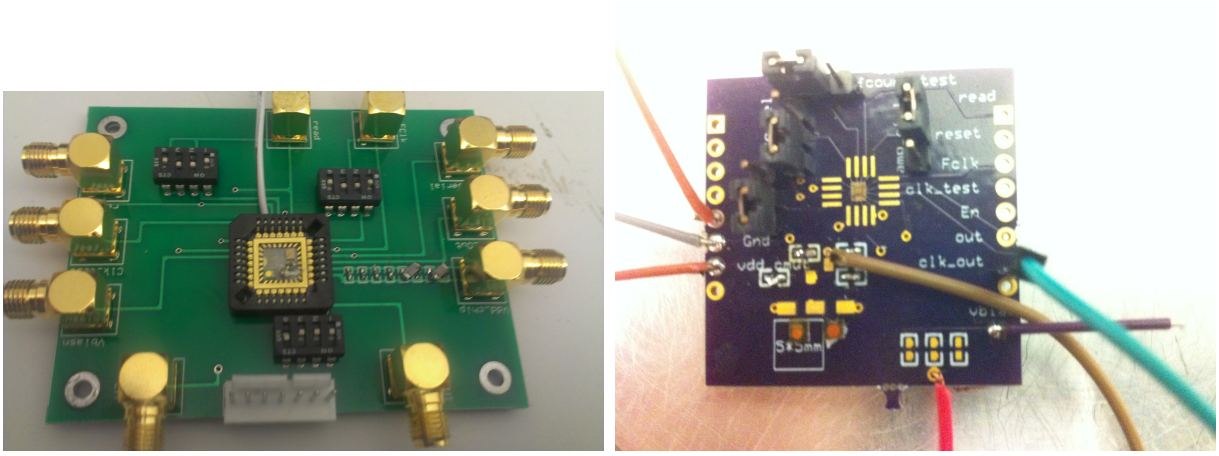
parasitics load both the oscillators, in turn degrade oscillation amplitude and increase the minimum power at which the oscillators could work. A CMUT with a resonant frequency of 3.6 MHz (R_E=34.37 Ω; L_E=327 μH; C_E=6.55 pF; C_0=49.64 pF) was directly biased on the board using a 1-$M\Omega$ resistance and was AC-coupled to the oscillator input on the chip using a 6.5-nF capacitor. The value of this coupling capacitance is not important as long as it provides low enough impedance at the desired frequency of 3.6 MHz. Two resonating capacitors with 60-pF capacitance were used. For testing the Colpitts oscillator design the CMUT was biased at 13.5 V.

4.2 Colpitts Oscillator

The test board shown in Fig. 4.2(b) was used for testing the Colpitts oscillator design. This circuit was biased at 1.8-V V_{DD} and with a DC current of 400 μA for observing the startup behavior, the steady state oscillations, and the Allan deviation.

4.2.1 Startup Measurements

Startup test is performed by turning on the power to the chip and keeping the CMUT at a fixed DC. The observed waveform is shown in Fig. 4.3. The measured startup time was 0.3 s. Startup time is an important parameter for the gas sensing applications, as in order to achieve lower power most wearable sensors are power cycled. Power cycling is implemented by periodically repeating the



(a) **(b)**

Figure 4.2 Printed circuit boards used for testing. a) 1^{st} generation test board b) 2^{nd} generation test board.

cycle of turning on the oscillator, measuring the sensor data, and turning it off. Thus, faster the startup time shorter the duration for which the oscillator is active. Consequently, the average power consumption is reduced.

4.2.2 Steady-State Measurements

Fig. 4.4 shows the steady-state performance of the oscillator output. The amplitude of oscillation is of importance because higher amplitude reduces phase noise. Also because of higher amplitude less amplification will be required to make the signal rail-to-rail and hence power consumption will be reduced. The oscillator has a fundamental oscillation frequency of 3.6 MHz and a peak-to-peak amplitude of 0.9 V.

4.2.3 Allan Deviation Measurements

Allan deviation is used to measure the short-term frequency stability in a system as a function of the averaging time. In this method the sequence of time-domain data is analyzed to measure the frequency stability of the oscillators [24, 25].
Fig. 4.5 shows the Allan deviation of the Colpitts oscillator. Data from the oscillator output was acquired continuously for 1 hour using a universal frequency counter (Model 53230A, Agilent Technologies, Inc., Santa Clara, CA). The acquired data was then processed to determine the Allan deviation. Allan deviation is the time domain method of analyzing the frequency stability of the

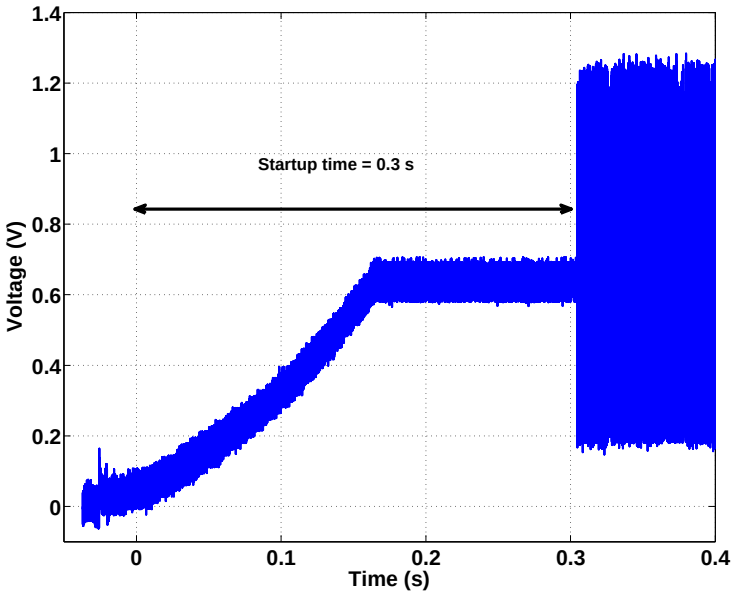


Figure 4.3 Measured startup response of the BJT-Colpitts oscillator.

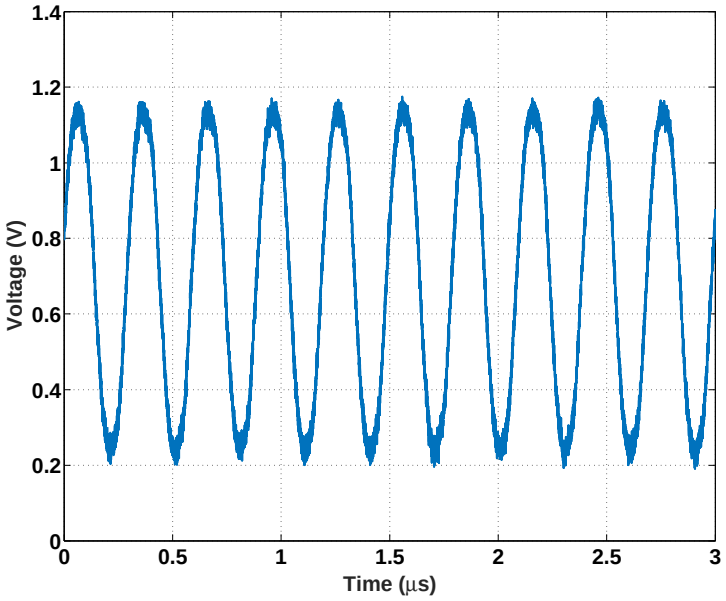


Figure 4.4 Measured steady-state output signal of the BJT-Colpitts oscillator.

oscillators. The Allan deviation, $\sigma(n\tau_0, M)$, for a gate time, $n\tau_0$, is [8]

$$\sigma(n\tau_0, M) = \sqrt[2]{\frac{1}{2n^2(M-2n+1)} \sum_{j=0}^{M-2n} (\sum_{i=j}^{j+n-1} \overline{f}_{i+n} - \overline{f}_i)^2} \tag{4.1}$$

here M is total number of samples, τ_0 is the gate time used for measurements, and $\overline{f}_i$ is the average frequency of n samples. When the data is sampled for a short duration the random noise of the electronic circuit is the dominant factor affecting variations in the period of the sinusoidal. As the measurement time increases, the long-term drift because of variations in the environment and variations in CMUT's impedance profile become the dominant factors. From Fig. 4.5 a minimum Allan deviation of 9.36 Hz is observed in the frequency measurement for around 2-s gate time. This results in a 3-σ variation of 28.08 Hz in the final system measurement. Allan deviation (σ) of 9.36 Hz corresponds to 100 ppb of resolution for toluene sensing results reported in [12]. Table 4.1 shows the

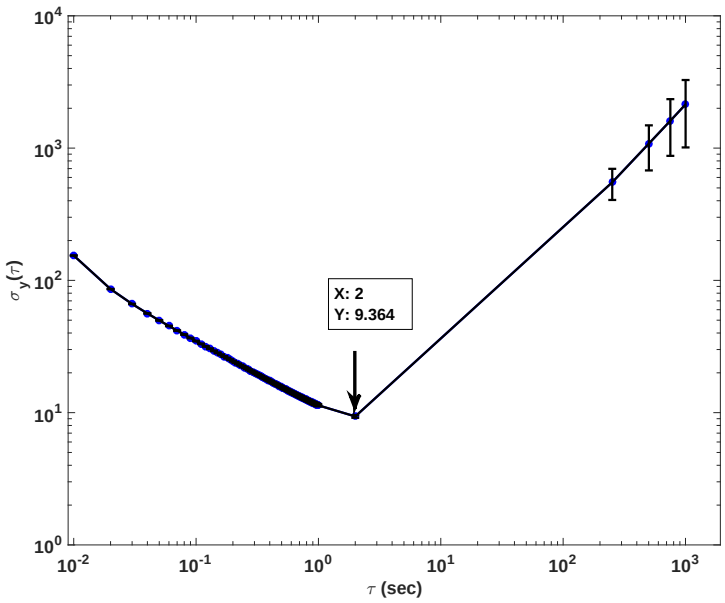


Figure 4.5 Measured Allan deviation of the BJT-Colpitts oscillator.

minimum and nominal power dissipation of the BJT-Colpitts oscillator. Nominal power dissipation is the power consumption of the oscillator at 1.8-V V_{DD} and minimum power dissipation is the

Table 4.1 Power consumption of the BJT-Colpitts oscillator

	V_{DD} (V)	I_{OSC} (μ A)	$Power$ (μ W)
Nominal Vdd	1.8	172.5	310.5
Minimum Vdd	1.5	165	247.5

lowest power at which the oscillator can operate with startup.

4.3 Inverter-Based Oscillator

The board shown in Fig. 4.2(b) was used for testing the inverter-based design as well. For testing the inverter based design the capacitor connected between the oscillator output and the ground was desoldered as it would load the output of the inverter-based design. For the startup, steady state, and Allan deviation tests a nominal supply voltage of 1.8 V was used. Inverter-based design consumed a DC bias current of 142 μA.

4.3.1 Startup Measurements

For startup the CMUT is kept at a fixed DC bias and the circuit was powered down and then powered up. Fig. 4.6 shows the startup measurement obtained from the testing. Startup time of around 0.08 s was observed for this design.

4.3.2 Steady-State Measurements

The steady state measurement was acquired for shorter time duration with higher sampling frequency (2 GS/s) in order to attain a higher sampling accuracy. Sinusoidal oscillations with a frequency of 3.51 MHz and a peak-to-peak amplitude of 1.3 V were observed.

4.3.3 Allan Deviation Measurements

For Allan deviation measurement of the inverter-based oscillator, the oscillator was interfaced with a universal frequency counter (Model 53230A, Agilent Technologies, Inc., Santa Clara, CA) and frequency data was acquired continuously for an hour with a gate time of 10 ms. This data was further processed to obtain the Allan deviation of the inverter-based oscillator design. Fig. 4.8

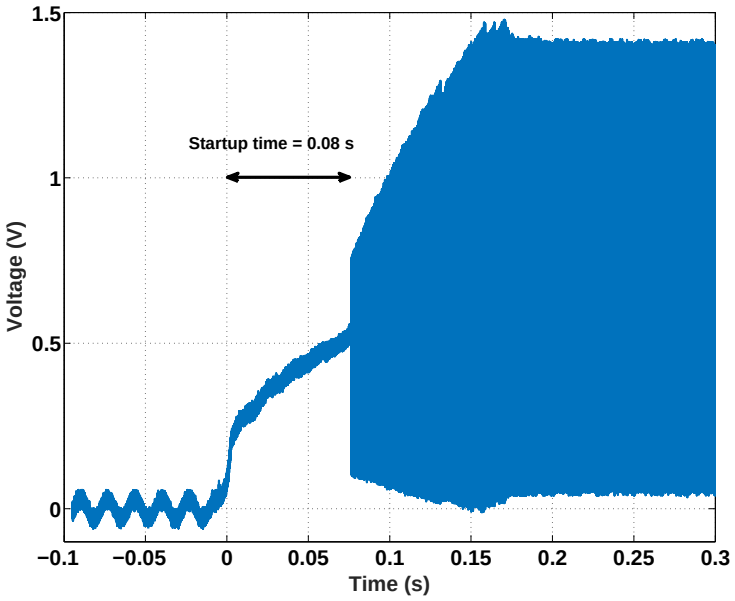


Figure 4.6 Measured startup response of the inverter-based oscillator.

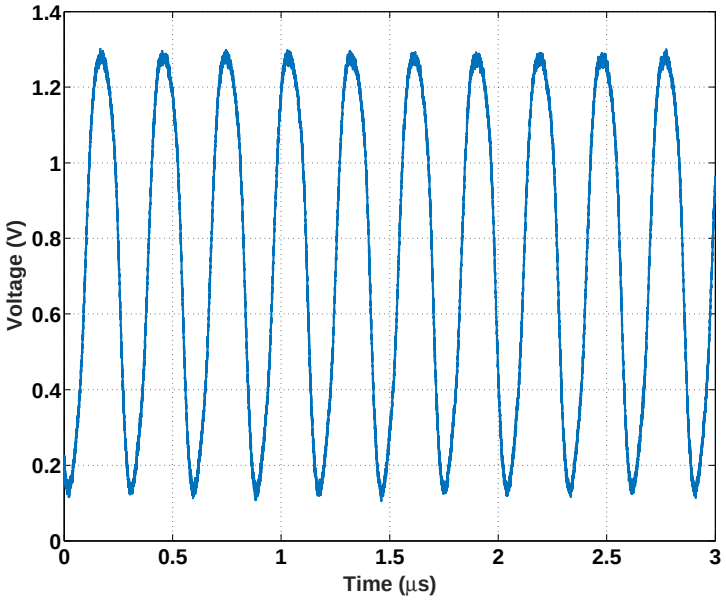


Figure 4.7 Measured steady-state output signal of the inverter-based oscillator.

shows the measured Allan deviation of the inverter-based oscillator. A minimum Allan deviation of 10.78 Hz around the measurement time of 200 ms is observed. This deviation is similar to the one obtained in the Colpitts oscillator design and will result in a 3-σ variation of 32.34 Hz in the final system measurement.

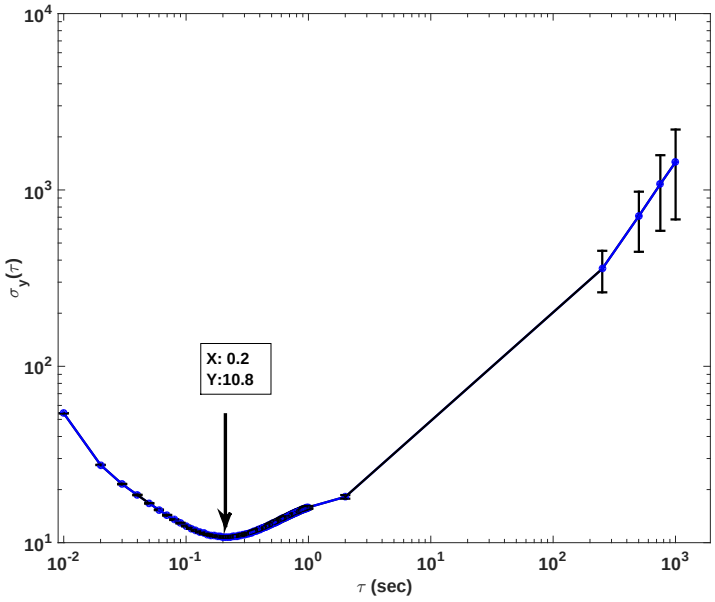


Figure 4.8 Measured Allan deviation of the inverter-based oscillator.

Table 4.2 Power consumption of the inverter-based oscillator

	V_{DD} (V)	I_{OSC} (μ A)	$Power$ (μ W)
Nominal Vdd	1.8	142	256
Minimum Vdd	1.16	40	46.5

Table 4.3 Digital frequency counter measurement results for a 4.333333-MHz clock

Gate Time (ms)	Decimal Equivalent of Count	Frequency Equivalent of Count (Hz)	Absolute Measured Error (Hz)	Maximum Expected Error (Hz)
0.9998240	8665	4333263	70	1000
9.9998320	86665	4333323	10	100
49.9999840	433333	4333331	2	20
99.9984400	866654	4333338	5	10
499.9998400	4333334	4333335	2	2
999.9997000	8666667	4333335	2	1

4.4 Digital Frequency Counter

The testing of the digital frequency counter was conducted on the board shown in Fig. 4.2(b), by applying an external test clock of 4.333333 MHz. The gate time was varied from 1 ms to 1 s to test the functionality of the frequency counter. Once the "Enable" (gate time control) goes low the count value is latched by latching the clock. This data is then read by parallel-to-serial interface when the "Read" (read control) goes high using "F_{CLK}" (read clock). Table 4.3 shows the measurement results for 1.8-V V_{DD}. The digital frequency counter had a power consumption of less than 20 μW.

4.5 Complete System Level Measurements

The chip was designed as a test vehicle for demonstrating the vision of a complete system providing a digital frequency count after it is interfaced with a CMUT resonator. For the sensing applications it is required to have all these features with low power and small form factor. The complete system functionality was successfully demonstrated. Table 4.4 shows the complete end-to-end system measurements. In Table 4.4 the "Decimal Equivalent of Count" represents the serially read binary value. "Calculated Frequency" is the calculated frequency value from the decimal equivalent and gate time. This complete system consumed an average current of 300 μA with a V_{DD} of 1.8 V (540 μW). With a 0.1-s startup time, 1-s measurement time, less than 1-ms read time, and one measurement every minute the power consumed is 10 μW.

In this chapter the performance of the different blocks was individually measured for function-

Table 4.4 Complete end-to-end measurements

Gate Time (ms)	Decimal Equivalent of Count	Calculated Frequency (MHz)
1.04266	7385	3.541423
10.426384	73831	3.540585
52.13184	369131	3.540360
104.26332	738078	3.539490
521.3153	3689744	3.538879
1042.6278	7378896	3.538605

ality and power. Finally a complete system demonstration was shown.

CHAPTER

5

CONCLUSION

Health and environmental tracking plays a crucial role in early diagnosis of diseases as well as maintaining a healthy lifestyle. VOC detection and monitoring is important for achieving these goals.

This work demonstrates CMUTs as a candidate for low-power VOC detection. Different blocks required for the gas sensing system were studied, analyzed, designed, and tested separately for their power and noise performance. Finally a complete end-to-end working system was demonstrated wherein a 3.6-MHz CMUT was interfaced with the custom analog front-end and a digital output was read serially. This system consumed an average current of 300 μA with a V_{DD} of 1.8-V (540 μW). With a 0.1-s startup time, 1-s measurement time, less than 1-ms read time, and one measurement every minute the power consumed is 10 μW.

The eventual goal is to realize a remotely located system with very low-power consumption and with an ability to report the concentration of different gases present in the environment to a system-on-chip (SOC). With the addition of multiplexing between different CMUTs (for improving selectivity) and a SPI interface (for controlling the different settings inside the chip as well as reading the frequency count value serially), this will be a complete solution for the gas sensing application (Fig. 5.1). In this thesis the groundwork for the complete system design is laid out and the final aim seems realizable. The CMUT based gas sensor product does not seem far from the market.

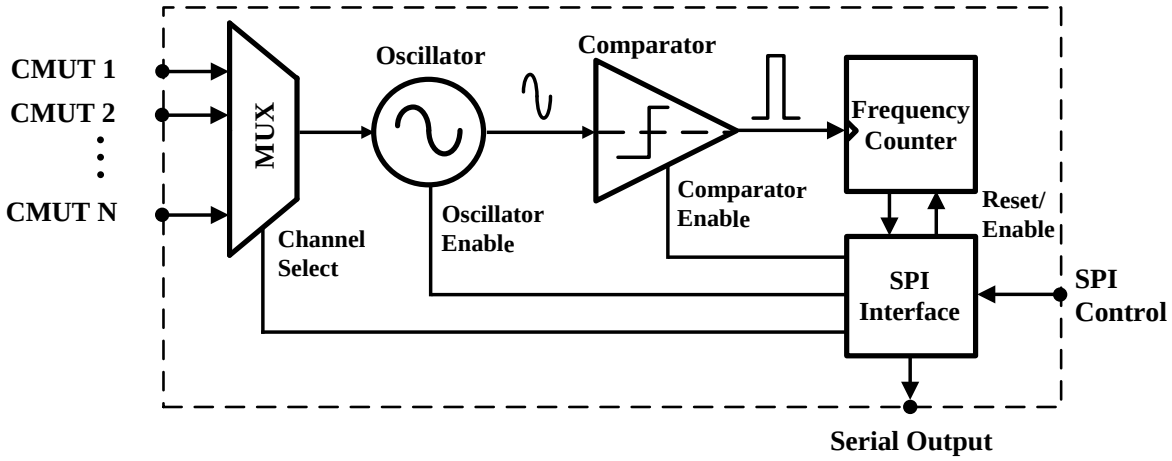


Figure 5.1 Proposed 2^{nd} generation of the CMUTs interface.

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