ABSTRACT

CHOI, YONGJIN. Design of Multimode Signaling Transceiver for High-Density and High-Speed Links. (Under the direction of Paul D. Franzon).

The increasing demand for smaller packages and low-cost platforms in conjunction with an aggressive scaling of the input/output (I/O) bandwidth of multicore microprocessors, requires interconnects of maximized density per unit area. However, crosstalk noise caused by the capacitive and inductive coupling between lines limits the achievable interconnect density.

As an alternative signaling scheme for dense interconnects, we have investigated multimode signaling where n signals are transmitted through a group of n closely coupled lines called a bundle by exploiting n-fundamental modes of the corresponding bundle. In multimode signaling, n-parallel data is first linearly combined with n-modes to produce n-parallel transmitted data. Since mode propagation through wires is linearly independent, the decoded data at the receiver reduces crosstalk.

To investigate the effectiveness of this scheme as a dense interconnect solution, we analyze inter-bundle crosstalk as a function of bundle-to-bundle spacing to guarantee a high-density interconnect as compared to conventional single-ended and differential signaling. The simulated small crosstalk between bundles demonstrates the promise of multimode signaling for high-density interconnects.

To demonstrate the signaling scheme, a multimode transceiver with 0.13μm CMOS process is implemented. The interconnect bundle is comprised of a four-parallel, 6 cm, FR-4 stripline structure with two pairs of wires stacked inside two reference planes. The measured eye-diagrams of a prototype chip demonstrate the speed of 2.4 Gbps per wire at the decoded receiver outputs. Even if the manufactured bundle has various non-ideal conditions such as length mismatch and discontinuities, the signaling scheme is likely to be insensitive from the effects. This implementation example provides insights into the design of multimode signaling transceiver incorporated with the linear combinations of eigenmodes and the reverse operation.

Design of Multimode Signaling Transceiver for High-Density and High-Speed Links

by
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DEDICATION

To my wife, Mijung and my children Wonchul and Wonho

BIOGRAPHY

Yongjin Choi received his B.S. and M.S. degree in Electronics Commmunications from Hanyang University, Seoul Korea in 1990 and 1992. Since 2005 Yongjin Choi has been a Research Assistant at North Carolina State University where he is currently working toward a Ph.D. degree and focusing on developing an alternative signaling scheme for high-density chip-to-chip communication. Before that, he worked for Samsung Electronics, Korea, where he was involved in VLSI logic design and the development of merged memories. He also worked as a summer intern at Intel (2007) for modeling inter-bundle crosstalk and Rambus (2009) for reducing power supply noise. His research interests lie in exploring advanced signaling schemes and circuit design for high-density and high-speed interconnect.

ACKNOWLEDGMENTS

At first, I felt pursuring a Ph.D. was a solitary endeavour. But whenever I was puzzled by various problems, I realized there was always someone out there waiting for me. I am indebted to a great manay people and would like to acknowledge them to help me complete this long journey.

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

Chapter 1

Introduction

High-speed link for chip-to-chip and backplane has made the researchers and the industry to challenge higher speed in a limited interconnect area in a cost-effective way. This chapter goes over the issues of high-density and high-speed interconnects and presents the motivation and contributions of this dissertation.

1.1 Current Trend of High-density / High-speed link

As the desire for high-performance electronic applications increases continuously, the growth of the off-chip bandwidth is required to mitigate the bottleneck of chip-to-board data transmission. But the difficulty of increasing the off-chip bandwidth leads us to assign more pins to signal I/O. For example, multicore processors can provide enhanced performance and reduced power consumption, but need to have high-speed I/O to support high-performance operation. According to Hofstee [13] under the resonable goal of 1-TFlops (floating-point operation per second) multicore processor for the year 2010, 1-TB/s of the off-chip bandwidth is anticipated. If a 20 Gb/s data rate per differential signal I/O pair is assumed as predicted in the International technology Roadmap for Semiconductors (ITRS) [14] for 2010, the number of I/O pairs to meet the 1-TFlops is 400 I/O pairs, that is, 800 I/O pins.

For high-speed serial interconnect, many new standards are being introduced. They includes PCI Express, RapidIO, Fibre Channel, and Infiniband operating under 10 Gb/s. For backplane Ethernet interconnects operating at 10 Gb/s, IEEE P802.3ap has set up the standard of 10Gbit/s over PCB specification [15] recently. Furthermore IEEE 802.3ba Higher Speed Study Group has started working on 40 Gbit/s over 1m backplane Ethernet specification. Therefore we need to find a solution to resolve two issues at the same time, that is, high data transmission speeds in dense interconnects.

1.2 Motivation

The primary motivation of this research is listed as follows:

- **Increasing chip I/O bandwidth demand**: The trend of higher on-chip clock speed and multicore processor gives us a challenge that the conventional I/O signaling can't afford effectively. For example, Tera-Flops multicore processor calls for about thousand I/O pins provided that the differential signaling is employed [13]. The challenge is how higher I/O density and multi-Gbps transmission speeds could be accomplished without increasing packaging costs to accommodate tera-byte data per second.

- **Need for controlling crosstalk**: The dense interconnects due to higher I/O density and the limited routing area lead to severe crosstalk by the coupling between the neighboring lines. To reduce the coupling between differential pairs, as a rule of thumb the inter-pair spacing is four times the line width in PCBs. That implies that differential signaling necessitates proper control of crosstalk in dense interconnects or we need to explore an alternative signaling scheme to deal with the dense interconnects.

- **Coordinated transmission with multi-lines**: Since the dense interconnects are unavoidable for the compactness of electronic systems irrespective of severe crosstalk, we would rather consider exploiting a closely located multiple lines as a unit bundle for signal transmission, which is analogous to Multiple-input

multiple-output (MIMO) for wireless communications in terms of the multiple channel paths. But unlike MIMO, the unit bundle experiences crosstalk noise between the adjacent lines. Hence, the parallel raw data transmitted through the unit bundle needs to be pre-processed before transmission to compensate the effect of the coupling noise.

- **Exploring feasibility of multimode signaling**: As a possible candidate signaling scheme to deal with dense interconnects, we've encountered a short IBM paper published by Nguyen and Scott [16] based on multiconductor transmission line theory (MTL). According to [16] and MTL theory, theoretically crosstalk reduction may become possible in dense interconnects with encoder / decoder scheme. So by pursuing this idea in non-ideal situation, we may propose an alternative signaling scheme to achieve high interconnect density and high transmission speeds.

1.3 Contributions

This research aims to explore the feasibility and the practical issues of an alternative I/O signaling scheme for a highly coupled interconnect. Starting from multiconductor transmission line theory, the multimode signaling scheme was analyzed to prove the concept. This research includes system simulation and analysis, interconnect design, and a prototype chip design and measurements. The resultant contributions of the research are:

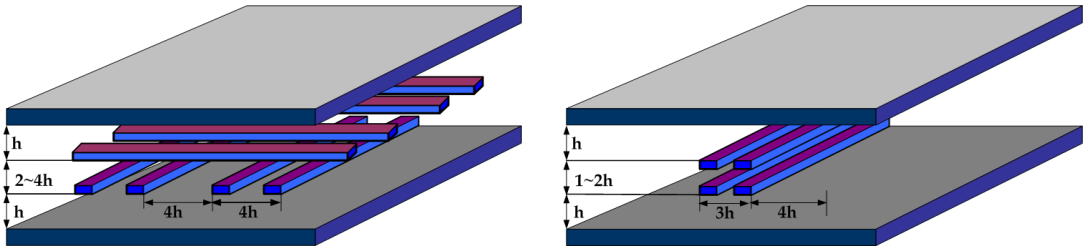
- The analysis of Inter-/Intra-bundle crosstalk to explore the interconnect density limitation of multimode signaling. The analysis results implies that multimode signaling would increase the interconnects density while keeping inter-bundle crosstalk noise low compared to conventional differential signaling.

- Multimode Transmitter / Receiver Chip is being designed with IBM 0.13μm CMOS process. The partially tunable codec incorporated into the transceiver

has a capability of dealing with the nonideal channel effects such as line misalignment and discontinuity. The implementation example provides insights into the design of multimode transceiver.

- The signaling scheme validation by measurements of the designed multimode transmitter/receiver together with four-parallel stripline. The transceiver chip attached to the PCB was tested by activating on-die pseudo-random sequence generators. The measured eye-diagrams at the receiver output illustrate 2.4 Gbps/wire signal transmission through the highly coupled channel.

- Promising to increase interconnect density. Fig. 1.1 represents the interconnect density comparison of a conventional differential pair with multimode interconnect in four-layer structure when sending four signals. Here **h** denotes the dielectric thickness between a reference plane and a signal layer. As shown in Fig. 1.1(a), the horizontal dimension of the differential pair is **16h** to send four signals with four pairs. For the multimode interconnect, the horizontal dimension is **7h**. Therefore, the horizontal density benefit of multimode interconnect is likely more than two times the one of the conventional differential pairs when sending four signals, provided that the pair spacing (**4h**) between differential pairs is the four times of the line width.



(a) (b)

Figure 1.1: Interconnect Density Comparison when sending four signals: (a) Four, differential pairs using two signal layers, (b) Multimode interconnect consisting of a four closely-located wires

- Provide insights on the interconnect scaling by collaborative signal transmission.

- The analysis of non-ideal channel impact such as via discontinuity and line misalignment in multimode signaling.

Chapter 2

Literature Review and Related Works

This chapter describes the different approaches that researchers developing multi-Gbps transceiver are exploring to achieve the higher transmission rates in a smaller interconnects area. Especially this review focuses on the schemes of reducing crosstalk noise, sharing interconnect lines, adaptation of channel coding and collaborative multiline transmission.

2.1 Brief History of Predicting Crosstalk

In this section, a brief literature summary of crosstalk analysis of coupled transmission lines is described. At high speeds, interconnect behaves as transmission lines, therefore reflections and crosstalk should be well analyzed to avoid over-designing high-speed systems. Based on the extensive literature search, Javis paper [17] published in 1963 is likely the first one describing crosstalk between transmission line when the coupling is weak. Defalco paper [1] published in 1973, presented physical basis for crosstalk at an engineering level with a simplified diagram shown in Fig. 2.1. The diagram shows that the induced currents, i_{Cm} and i_{Lm} by mutual capacitances and inductances create the stacked noise pulses at the other end of a quiet line, *far-*

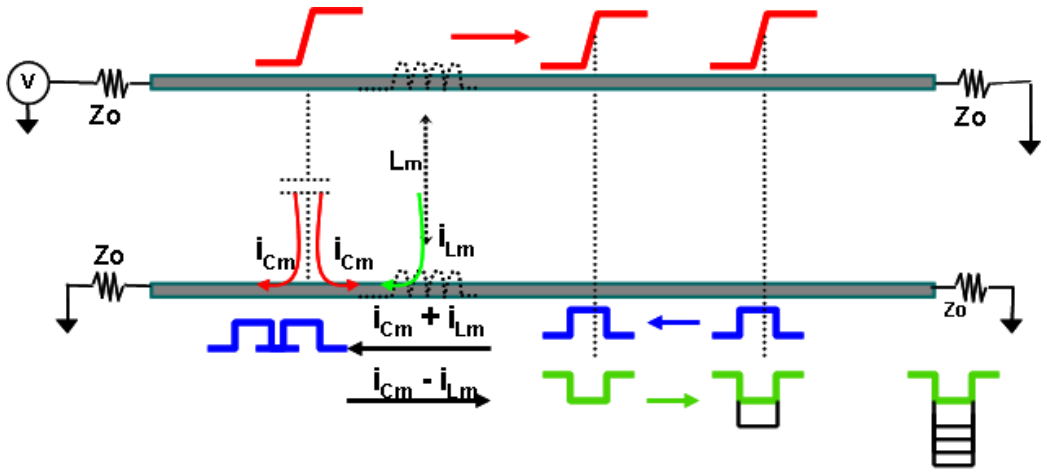


Figure 2.1: Diagram showing crosstalk between two parallel lines [1]

end crosstalk. Depending on the amounts of capacitive and inductive coupling, the far-end crosstalk would have a positive or negative pulses determined by the sign of $i_{Cm} - i_{Lm}$. According to [1,17], for a three-conductor lossless line in an inhomogeneous medium, there is a popular solution used for the prediction of time-domain crosstalk, commonly mentioned until now. Assuming $V_N(t)$ and $V_F(t)$ are the near-end and far-end crosstalk voltages,

$$\begin{aligned} V_N(t) &= K_b[V_S(t) - V_S(t - 2T)] \\ V_F(t) &= K_f \frac{d}{dt}[V_S(t - T)] \end{aligned} \tag{2.1}$$

The backward (K_b) and forward (K_f) coupling coefficients are defined as,

$$\begin{aligned} K_b(t) &= \frac{1}{4T}\left(\frac{Z_C}{R_S + Z_C}\right)\left(\frac{L_m}{Z_C} + C_m Z_C\right) \\ K_f(t) &= -\frac{1}{2}\left(\frac{Z_C}{R_S + Z_C}\right)\left(\frac{L_m}{Z_C} - C_m Z_C\right) \end{aligned} \tag{2.2}$$

where T is the one-way time delay along the line, Z_C is the characteristic impedance,

R_S is a source impedance, and $L_m(C_m)$ is the total mutual inductance(capacitance) defined by the product of the per-unit-length values and the total line length.

However, the crosstalk prediction by Eq. (2.1) is derived based on the three assumptions [18]:

1. The Lines Are Weakly Coupled.
2. The Line Is Symmetrical.
3. The Lines Are Matched at All Ends: $R_S = R_L = R_{NE} = R_{FE} = Z_C$

In practice, dense interconnect will violate the weakly coupled assumption. In addition, since matching all ends of the lines is an impractical condition, the measured crosstalk would deviate from the prediction even if other assumptions are met. The detailed descriptions of the assumptions are described in Paul's paper [18]. As an extension of this popular prediction, far-end crosstalk is said to be zero in stripline structure provided three assumptions are met.

2.2 Active Crosstalk Cancellation

As the signaling speed increases and the higher integration in a limited area is required, the signal integrity issues such as crosstalk noise need to be controlled carefully because the coupled noise due to capacitance and inductance mainly deteriorates the received signals. This situation necessitates a scheme that call for actively cancelling the crosstalk noise in an interconnect. In research performed in telephone subscriber loop by Honig et al. [19], crosstalk noise has been treated as a data-dependent noise rather than as the noise uncorrelated with the transmitted signal, that is random noise. Implementation example considering crosstalk as the data-dependent noise can be found in Zerbe et al. [2] that presented PAM-4 transmitter supporting the near crosstalk cancellation. In [2] the crosstalk cancellation terms generated from the neighboring pins are added to each output transmitter assuming that the coupling is time invariant as shown in Fig. 2.2.

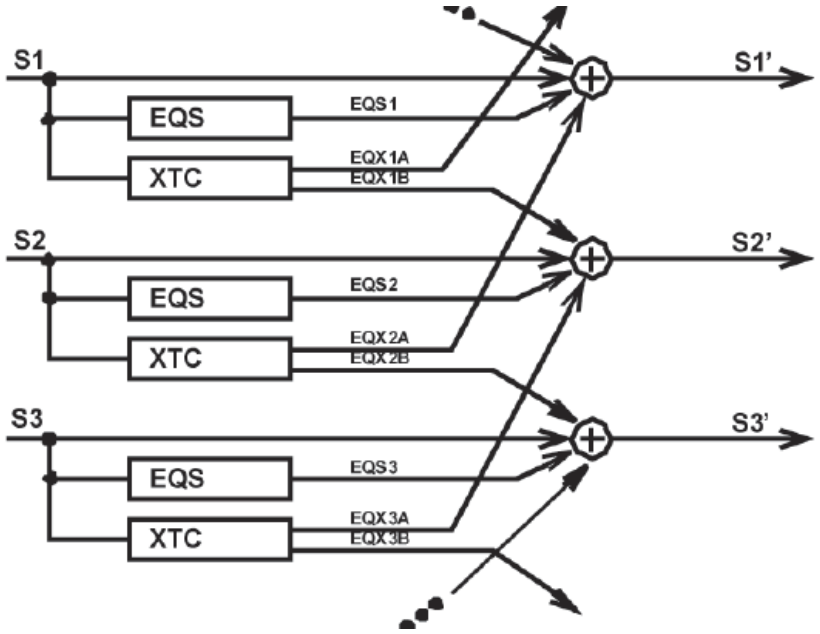


Figure 2.2: Near Crosstalk cancellation [2]

As an effort to equalize the timing jitter resulting from crosstalk, Buckwalter [3] analyzed crosstalk-induced jitter(CIJ) that is insensitive to signal swing and rise time even if FEXT causes CIJ and proposed general equalizer implementations for minimizing the impact of CIJ. The CIJ equalizer located in either a transmitter or a receiver, determines the electromagnetic modes of transitions and adjusts the delay of each transition as shown in Fig. 2.3. Here the difference of a_0 and a_{-1} determines the transitions of the data sequences. Whereas adjusting the timing of the zero-crossing points at the receiver improves CIJ without actually removing FEXT, the amount of variable delay would limit the compensated jitter.

Sham [4] proposed FEXT crosstalk cancellation (XTC) filter on the transmit side as shown in Fig. 2.4. According to the paper, if the channel and its FEXT are modeled as discrete-time sampled responses, the FEXT can be completely removed using the XTC filter if the following condition is met.

$$x_1[n] * h_{EQ1}[n] * h_{FEXT1to2}[n] = x_1[n] * h_{XTC1to2}[n] * h_2[n]$$

Kwang-Il Oh [5] proposed a DDR memory interface transceiver with a crosstalk

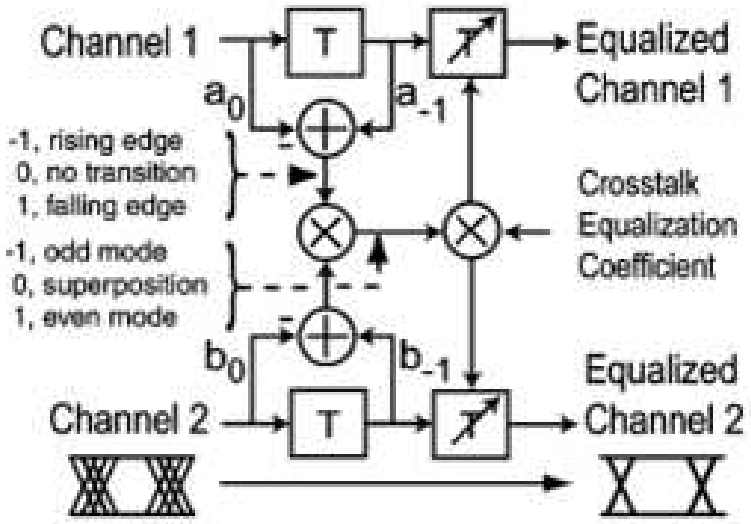


Figure 2.3: Schematic of a two-channel crosstalk-induced jitter equalization [3]

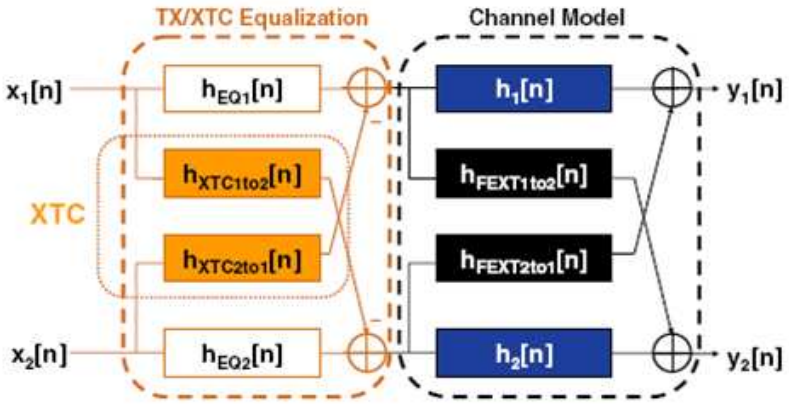


Figure 2.4: Transmit/XTC equalization and channel model [4]

suppression scheme. The transceiver implements a staggered memory bus topology and a glitch canceller to suppress crosstalk-induced distortions. The idea is that to eliminate crosstalk-induced timing distortion, even channels and odd channels are synchronized by two different clock domain. Therefore the channel transitions do not affect the timing jitters as shown in Fig. 2.5. This scheme would work as long as the coupling of parallel memory channel is relatively weak. But if the coupling is

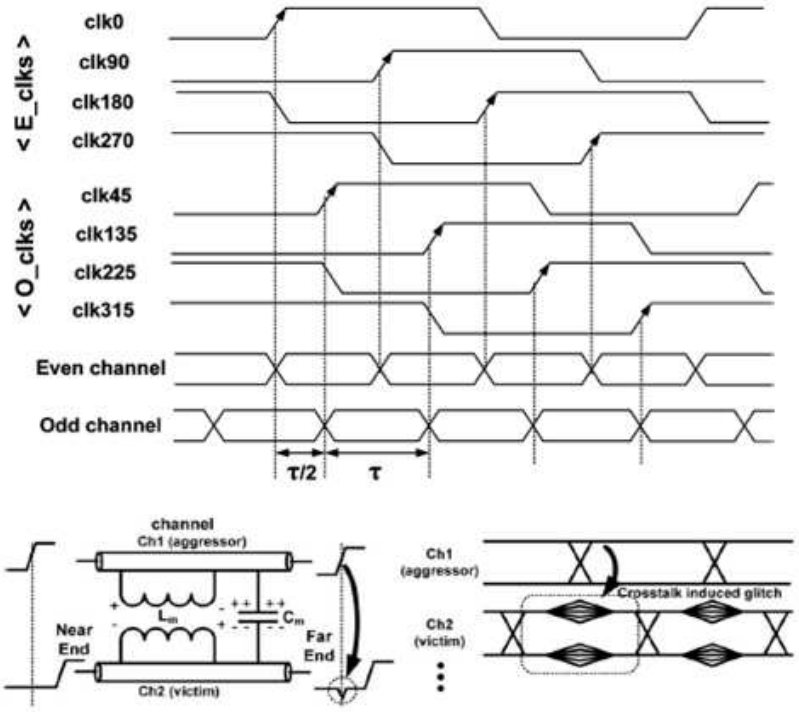


Figure 2.5: Crosstalk suppression by the staggered bus and crosstalk-induced glitch [5]

strong, the amplitude distortions by reflections would limit the performance of the glitch canceller.

2.3 Coding Schemes for Crosstalk Reduction

Another approach to actively cancel the crosstalk is to incorporate channel coding into the signal transmission. A few papers [6, 20] have demonstrated the benifits of channel coding. Hsieh and Sobelman [20] presented trellis coded modulation for a bidirectional multilevel wireline system by simulation only. But the main obstacle when the conventional channel coding is applied into a multi-Gbps link, is that the implementation complexity is too high to make it feasible. Farzan and Johns [6] suggested low-level complexity coding scheme for binary signaling to reduce crosstalk in a dense chip-to-chip interconnects. Fig. 2.6 illustrates the transceiver architecture when two bits are transmitted through three wires. If the induced crosstalk noise is

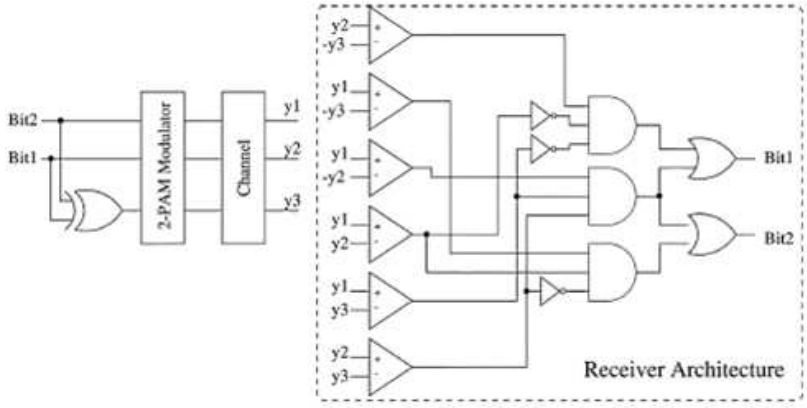


Figure 2.6: Transceiver architecture for the 3LINE-PAM2 method [6]

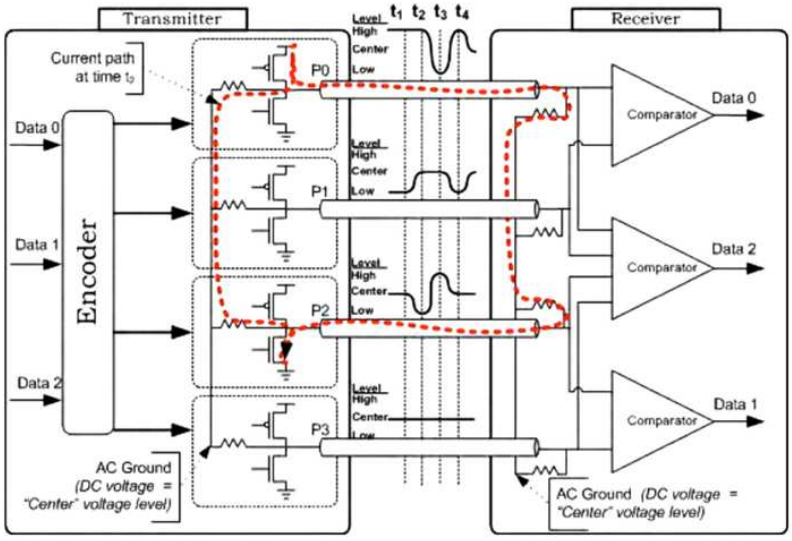


Figure 2.7: Transceiver architecture of [7]

severe, the receiver performance would be limited by the sensitivity of six comparators in the receiver.

Zogopoulos [7] suggests 3-level differential coding scheme to increase the pin utilization from 50 % to 75 % as shown in Fig. 2.7.

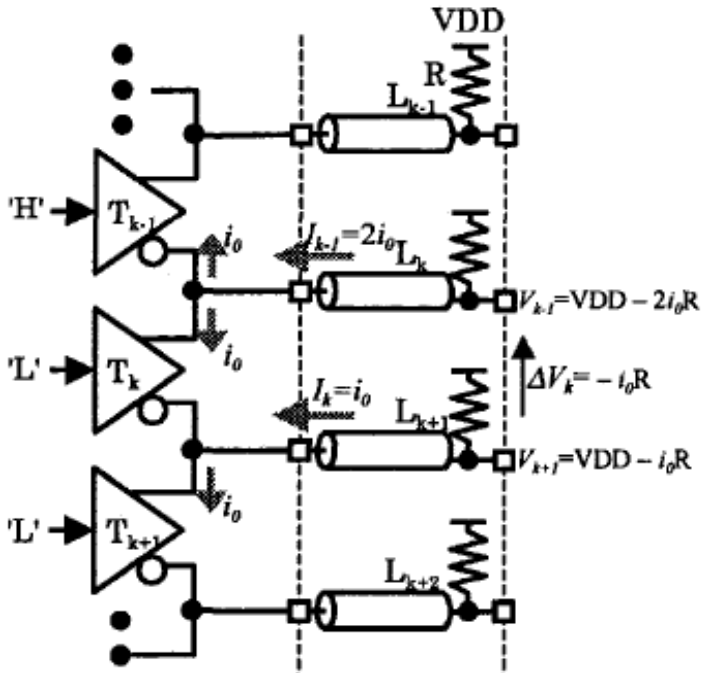


Figure 2.8: Shared data line [8]

2.4 Sharing interconnect lines

While a system using differential signaling benefits from increased noise immunity, the requirement of a pair of lines as an interconnection is the interconnect burden of the differential signaling for maximizing the interconnects density. As an effort to reduce the number of interconnection lines of differential signaling, a few of researchers investigated the possible schemes of increasing interconnects density [8, 21–23]. Hatori et al. [8] suggested a shared data line scheme claiming almost double the data transfer rate (1.1Gbps/pin in 0.25um CMOS) by sharing the adjacent line for data transmission as shown in Fig. 2.8. In this technique, several values of line currents and the received differential voltages are produced depending on the neighbor's transmitted data. But the requirement of two reference voltages in the receiver reduces the differential advantages.

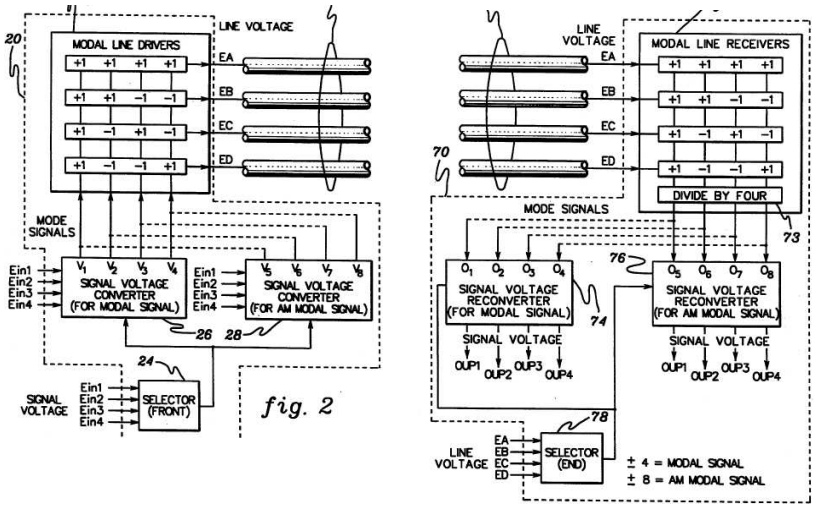


fig. 2

Figure 2.9: IBM patent [9]

2.5 Signal Transmission over Multilines

The previous sections summarize research activities dealing with active crosstalk cancellation and reduction of the number of interconnect lines in a high-speed short distance link. But the demand for dense interconnects is pushing the spacing between signal traces to the minimum manufacturable spacing. Under that severe crosstalk noise, conventional signaling such as differential signaling may not work properly because differential signaling benefits not from removing data-dependent crosstalk noise but from canceling out the common mode noise . After the extensive literature search, a few literatures [16, 24] have been encountered to underline crosstalk cancellation over a multiline link.

Nguyen and Scott [16] proposed to transmit signals through orthogonal modes on a multiple parallel lines system. By orthogonal properties of modes, crosstalk could be eliminated in a dense interconnect. The theory behind this is multiconductor transmission line (MTL) theory [25,26], that is, interconnect consisting of n-lines and reference plane has n-independent modes. Several patents [9,27–29] also demonstrate the very similar idea to [16]. Fig. 2.9 illustrates one IBM patent [9] using modal conversion over parallel multilines.

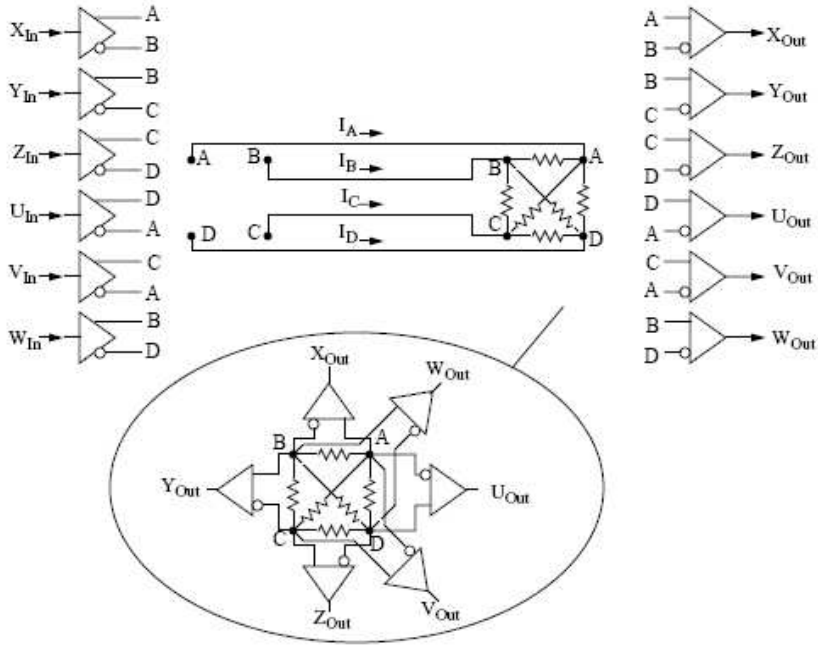


Figure 2.10: Multi-wire Signaling [10]

Broyde and Clavelier [24, 30, 31] emphasized the importance of matched termination in a multiline to ideally obtain zero crosstalk based on the idea of Nguyen and Scott [16]. The matched termination can be obtained from MTL theory in that interwires are also terminated with the calculated impedances. While the behavioral simulation results of Bryode and Clavelier for a lossless MTL look very promising, the practical issues in non-ideal interconnects such as length mismatch/misalignment and discontinuity effect need to be investigated further.

Another approach done by Poulton et al. [10] is multi-wire signaling illustrated in Fig. 2.10 for four-wire case. Six differential transmitter is driving the six-pair of four wires. Since this signaling did not consider the coupling between the neighboring lines, it need to be modified to overcome the severe coupling.

Chapter 3

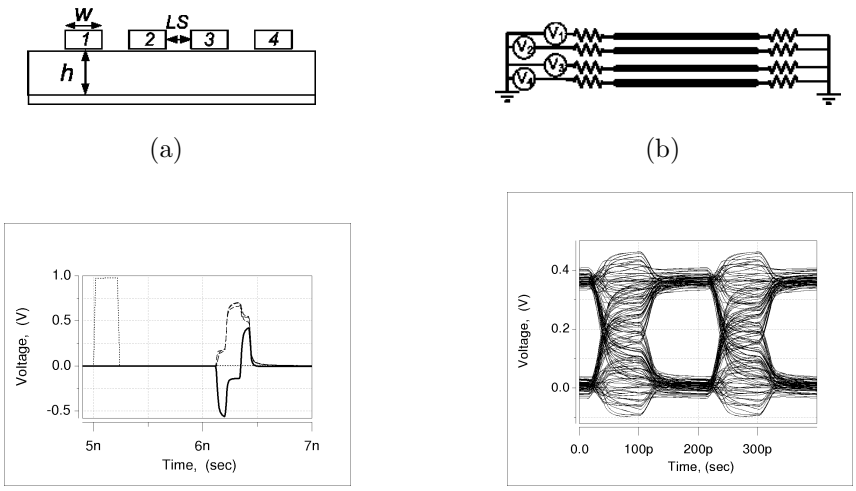
Multimode Signaling

This chapter describes the multimode signaling and the analysis of inter-bundle crosstalk that proves the possible increase of interconnect density. Recognizing that in practice a wide interconnect bus must be divided into bundles each associated with individual bundle transceivers and terminations, we consider the interaction between such bundles. Numerical examples are given for parallel interconnect structures.

3.1 Problem Statement

As the signal speed of interconnect is increasing and the line density is higher, the major obstacle to guarantee signal integrity at the receiving ends is to overcome the increased crosstalk provided that the link attenuations are relatively small such as in chip-to-chip interconnects. To better understand dense interconnect issues, we present a simple example and discuss the potential issues in the following.

For example, consider a highly-coupled parallel microstrip lines shown in Fig. 3.1(a). The widths of the signal traces, w are 5 mil, line spacings, LS 2 mil, dielectric thickness, h 20 mil, and line lengths are 20 cm. The ratio of $LS/h = 0.1$ indicates the strong coupling between lines due to stronger induced electric and magnetic fields. A larger loop with respect to a reference plane causes stronger magnetic field. The line capacitances and inductances extracted from two-dimensional electromagnetic (EM)



(a) (b)

(c) (d)

Figure 3.1: Example highly coupled microstrip lines: (a) Cross-section of microstrip ($n = 4$), $w = 5$ mil, $LS = 2$ mil, and $h = 20$ mil, (b) Time-domain simulation setup, (c) Pulse responses when the raw input amplitude is 1.3v, and (d) Eye diagrams at a receiving ends when the raw input amplitude is 1v

solver such as Hspice EM solver are described by 4×4 matrices, $\mathbf{C}_4$ and $\mathbf{L}_4$:

$$\mathbf{C}_4 = \begin{bmatrix} 63.3 & & & \\ -25.0 & 74.0 & & \\ -2.9 & -23.9 & 74.0 & \\ -1.0 & -2.9 & -25.0 & 63.3 \end{bmatrix} (pF/m) \tag{3.1}$$

$$\mathbf{L}_4 = \begin{bmatrix} 642 & & & \\ 290 & 634 & & \\ 172 & 287 & 634 & \\ 113 & 172 & 290 & 642 \end{bmatrix} (nH/m) \tag{3.2}$$

Note that $\mathbf{C}_4$ and $\mathbf{L}_4$ are symmetrical with respect to the main diagonal. The maximum coupling coefficients k_C and k_L are about 0.37 and 0.45.

Fig. 3.1(b) illustrates a time-domain simulation setup, where all resistances are terminated with 50 Ω. To demonstrate the highly coupled phenomena of this example

microstrip, three pulses are applied to V_1, V_2, and V_4 respectively, having the rise/fall time of 20 psec and the pulse width of 200 psec. As shown in Fig. 3.1(c), the crosstalk signal at the receiving end of the quiet line 3 consists of the forward crosstalk signal caused by capacitive/inductive coupling and the reflected signal from the sending ends due to incomplete termination. In this example, the peak value of the crosstalk is more than 50 % of the received signals.

The increased crosstalk at the receiving ends are attributed to higher coupling between the neighboring lines and reflections due to incomplete terminations. When all four lines are driven by the random sequences simultaneously, we anticipate that the crosstalk noise similar to the crosstalk pulse in Fig. 3.1(c) is added to the received signals. To represent the effect of highly coupling in real situation, Fig. 3.1(d) demonstrates the eye diagram at the receiving end when four voltage sources (V_1, V_2, V_3, and V_4) are replaced with 5 Gbps pseudo-random sequence generators. The horizontal eye openings are reduced by about 50 % bit duration, 100 psec as the stacked crosstalk deteriorates the signal transition areas. The reflected pulses reduce the vertical eye openings. The eye openings will aggravate as the signaling speed increases in a denser inteconnect.

In closely-located parallel lines to reduce reflections at both ends of lines, the matched terminations are required in that inter-line terminations are needed based on a termination matrix. However in practice, the inter-line terminations combined with transmitters or receivers would complicate the implementations of the transceiver designs. Therefore mostly single-ended, incomplete, terminations are used. Furthermore, the coupled reflection pulses to the neighboring lines exacerbate the received signals with nominal single ended terminations of both ends of lines. In the next section, we discuss how the increased crosstalk is controlled by an alternative approach.

3.2 What is Multimode Signaling?

To simultaneously achieve multi-gigabit per second (Gb/s) speed and high interconnect density, we consider an alternative signaling scheme that exploits multi-

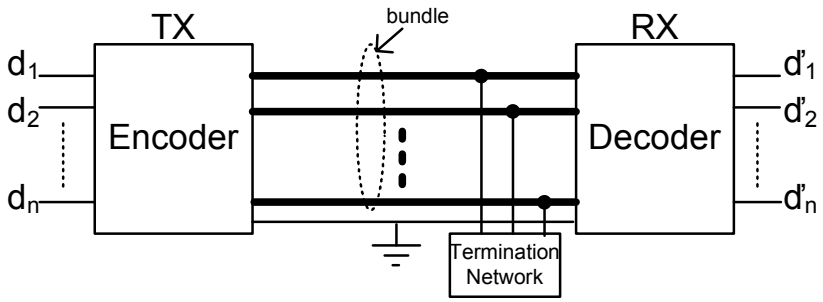


Figure 3.2: Multimode signaling

ple lines as a unit interconnect based on the multiconductor transmission line theory [25,26]. We call this alternative scheme for dense interconnects *multimode signaling* where n parallel signals are transmitted as the linear combination of n fundamental modes through a group of n tightly coupled lines called a bundle as illustrated in Fig. 3.2.

According to the theory, there exist n fundamental modes in a bundle. The term *mode* is defined as a "*wave that can travel independently on a system of infinitely long uniformly coupled transmission lines.*" [32, p204]. For example, when $n = 2$, there exist even (or common) and odd (or differential) modes in that the velocity of even mode is usually slower than odd mode provided that the capacitances in even mode is greater than those in odd mode. The phantom mode signaling suggested by Gabara [21] is the example using both modes. When $n > 2$ and high density interconnect, we can consider fundamental modes of n lines for collaborate data transmission. The basic idea here is not new. Collaborated data transmission through multiple lines has been suggested by Nguyen and Scott [16]. Later Broyde and Clavelier [24] elaborated on their results by emphasizing the importance of a matched termination network connecting wire-to-wire.

In multimode signaling, by exploiting the n modes extracted from the bundle-specific RLGC per-unit-length parameters (matrices of resistances, inductances, conductances, and capacitances) in given n lines along with a ground reference, we can effectively reduce the crosstalk at the receiving end. In Fig. 3.2 the encoder realizes the

linear combination of n modes of the corresponding bundle and the decoder performs an inverse operation of the encoder. A matched termination network defined in [24] has been connected to suppress the reflection at the receiving end. $\mathbf{d} = [d_1, d_2, \ldots, d_n]$ represents n parallel source signals before encoding and $\hat{\mathbf{d}} = [\hat{d_1}, \hat{d_2}, \ldots, \hat{d_n}]$ the decoded ones, resulting in ideally $\mathbf{d} = \hat{\mathbf{d}}$.

3.3 The Derivation of Multimode Signaling

In general, multiconductor transmission line (MTL) refers to $(n+1)$ parallel conductors consisting of n conductors and a reference conductor.The n conductors serve as a path for electrical signals between a transmitter and a receiver, and a reference conductor as a return path. Let us assume that n conductors are of uniform cross section along the z-axis and TEM wave propagation, where E and H fields are perpendicular to the direction of signal propagation. The behavior of line voltages, $V_i(z,t)$ and line currents, $I_i(z,t)$, $i = 1 \ldots n$, of MTL is governed by $2n$, coupled first-order differential equations known as the telegrapher's equations in time domain,

$$\begin{aligned} -\frac{d\mathbf{V}}{dz} &= \mathbf{ZI} \\ -\frac{d\mathbf{I}}{dz} &= \mathbf{YV} \end{aligned} \tag{3.3}$$

where $\mathbf{V} = [V_1(z,t), \ldots, V_n(z,t)]^t$ and $\mathbf{I} = [I_1(z,t), \ldots, I_n(z,t)]^t$ are vectors having a dimension of n, $\mathbf{Z}$ and $\mathbf{Y}$ are $n \times n$ symmetric matrices denoting impedance and admittance per unit length. Note that $[\cdot]^t$ is a transpose of $[\cdot]$. The second-order equations of (3.3) are

$$\begin{aligned} -\frac{d^2\mathbf{V}}{dz^2} &= (\mathbf{ZY})\mathbf{V} \\ -\frac{d^2\mathbf{I}}{dz^2} &= (\mathbf{YZ})\mathbf{I} \end{aligned} \tag{3.4}$$

As described in (3.3) and (3.4), line voltages and currents are coupled each other, implying that the values of voltage and current in a line is affected by adjacent line voltages and currents. As the coupling causes the crosstalks, we need to look

for a scheme that reduces the effective crosstalks between the lines, hence reliably recovering the transmitted signals at the receiver. One approach is to convert the coupled differential equations into the decoupled ones with a matched termination matrix. In order to decouple the differential equations of (3.4), we should diagonalize **ZY** and **YZ** matrices with a similarity transformation. Assume that $n \times n$ matrices **T** and **S** are transformation matrices to diagonalize **ZY** and **YZ** and define **V** and **I** as,

$$\begin{aligned} \mathbf{V} &= \mathbf{T}\mathbf{V}_m \\ \mathbf{I} &= \mathbf{S}\mathbf{I}_m \end{aligned} \tag{3.5}$$

Here we can consider $\mathbf{V}_m$ or $\mathbf{I}_m$ as a parallel data to be sent from the transmitter. The linear combination of the parallel data by (3.5) describes the encoding operation. By substituting (3.5) into (3.4), the resulting differential equations become

$$\begin{aligned} -\frac{d^2\mathbf{V}_m}{dz^2} &= (\mathbf{T}^{-1}\mathbf{Z}\mathbf{Y}\mathbf{T})\mathbf{V}_m \\ -\frac{d^2\mathbf{I}_m}{dz^2} &= (\mathbf{S}^{-1}\mathbf{Y}\mathbf{Z}\mathbf{S})\mathbf{I}_m \end{aligned} \tag{3.6}$$

So if $\mathbf{T}^{-1}\mathbf{Z}\mathbf{Y}\mathbf{T}$ and $\mathbf{S}^{-1}\mathbf{Y}\mathbf{Z}\mathbf{S}$ in (3.6) are simultaneously transformed into the diagonal matrices by the proper selection of **T** and **S**, (3.6) would be converted into the decoupled differential equations. That implies that the effective crosstalks caused by the coupled neighboring lines would be reduced by employing the transformation **T** and **S**. Because of the relationship of $\mathbf{S}^t = \mathbf{T}^{-1}$ [26, p203], it suffices to diagonalize either $\mathbf{T}^{-1}\mathbf{Z}\mathbf{Y}\mathbf{T}$ or $\mathbf{S}^{-1}\mathbf{Y}\mathbf{Z}\mathbf{S}$. So let us diagonalize $\mathbf{T}^{-1}\mathbf{Z}\mathbf{Y}\mathbf{T}$

$$\mathbf{T}^{-1}\mathbf{Z}\mathbf{Y}\mathbf{T} = \gamma^2 \tag{3.7}$$

where γ^2 is $n \times n$ diagonal matrix,

$$\gamma^2 = \begin{bmatrix} \gamma_1^2 & 0 & \cdots & 0 \\ 0 & \gamma_2^2 & \ddots & \vdots \\ \vdots & \ddots & \ddots & 0 \\ 0 & \cdots & 0 & \gamma_n^2 \end{bmatrix} \tag{3.8}$$

If we rewrite (3.7) as $\mathbf{ZYT} = \gamma^2\mathbf{T}$, we can notice that each column of $\mathbf{T}$ is the eigenvector of $\mathbf{ZY}$ and γ_i is the eigenvalue of $\mathbf{ZY}$, $i = 1, \ldots, n$. Here each column vector of $\mathbf{T}$ and $\mathbf{S}$ is called an eigenmode / a fundamental mode vector. For microstrip structure, $\mathbf{ZY}$ has a form of a strictly diagonally dominant matrix that leads to a nonsingular (invertable) property, guaranteeing n elements of eigenvalues. While a frequency-independent $\mathbf{T}$ exists for a lossless MTL, for a lossy MTL it is not possible to find a constant $\mathbf{T}$ except for a few cases that have structural symmetry [26, p345]. Our suggested structure is the case that has a frequency-independent $\mathbf{T}$ even if $\mathbf{T}$ would have different values for a lossless or lossy reference conductor. In the following section we are going to present an example of obtaining transformation matrices $\mathbf{T}$, $\mathbf{S}$ and a termination network $\mathbf{Y}_{tload}$ for a lossless MTL.

3.4 Example 1: Microstrip-lines

For microstrip structure, $\mathbf{ZY}$ has a form of a strictly diagonally dominant matrix that leads to a nonsingular (invertable) property, guaranteeing n elements of eigenvalues. If we assume the lines of the example shown in Fig. 3.1(a) are lossless, that is $\mathbf{Z}_4 = \mathbf{L}_4$ and $\mathbf{Y}_4 = \mathbf{C}_4$, the 4×4 matrix $\mathbf{T}_4$ diagonalizing $\mathbf{Z_4Y_4}$ can be computed:

$$\mathbf{T}_4 = \begin{bmatrix} 0.5 & 0.6 & -0.4 & -0.5 \\ 0.5 & -0.4 & 0.6 & -0.5 \\ 0.5 & 0.4 & 0.6 & 0.5 \\ 0.5 & -0.6 & -0.4 & 0.5 \end{bmatrix} \tag{3.9}$$

Note that the values of matrix elements are rounded up for the implementation purpose. Four column vectors called eigenvectors can be subgrouped as two even mode vectors (1st and 3rd column) and two odd mode vectors (2nd and 4th column) by examining the values and the signs of column elements. In this example, the eigenvalues of $\mathbf{Z_4Y_4}$ are distinct, thereby the eigenvectors being orthogonal basis vectors for signal transmission. Using the eigenvectors as basis vectors is equivalent to processing the n-parallel data linearly combined with $\mathbf{T}_4$ that is simultaneously transmitted through the example microstrip channel. In practice, $\mathbf{T}_4$ functions as an encoder in

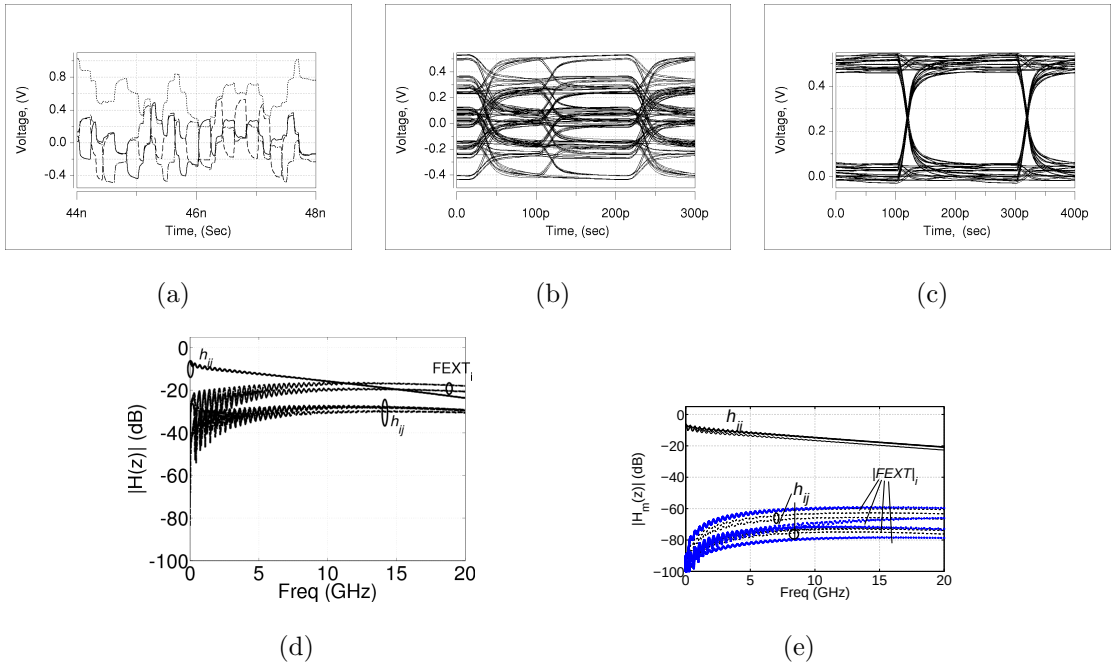


Figure 3.3: Multimode signaling with highly coupled microstrip lines: (a) Received signals, (b) Eye diagram at receiver input, and (c) Decoded eye diagram at receiver

the transmitter. Since the attenuations are relatively small for a chip-to-chip link, the inter-symbol-interference is ignored and we consider recovering the parallel data at the receiver as a system inverse problem with a system matrix, $\mathbf{T}_4$. This implies we can reconstruct the transmitted parallel data by inner product with the inverse matrix of $\mathbf{T}_4$, $\mathbf{T}_4^{-1}$ that is a decoder implemented at the receiver:

$$\mathbf{T}_d = \mathbf{T}_4^{-1} = \begin{bmatrix} 0.6 & 0.4 & 0.4 & 0.6 \\ 0.5 & -0.5 & 0.5 & -0.5 \\ -0.5 & 0.5 & 0.5 & -0.5 \\ -0.4 & -0.6 & 0.6 & 0.4 \end{bmatrix} \tag{3.10}$$

Fig. 3.3(a) illustrates four encoded-multimode signals at the receive inputs and the corresponding eye diagram is shown in Fig. 3.3(b). After decoding operations, the reconstructed signal shown in Fig. 3.3(c) represents the orginal binary sequences that are crosstalk insensitive. In the following section, we describe how the codec of multimode signaling would modify the channel responses as the channel responses of

a highly coupled lines are increasingly significant.

3.5 Channel Response of a Closely-Located Multiline

In general, multiline channel responses can be described in the frequency domain with an $n \times n$ vector channel $\mathbf{H}(z)$, an $n \times 1$ line voltage $\mathbf{\Psi}$, an $n \times 1$ source voltage $\mathbf{X}$, and an $n \times 1$ additive external noise $\mathbf{N}$, such as the noise from neighboring bundles, as

$$\mathbf{\Psi}(z) = \mathbf{H}(z)\mathbf{X} + \mathbf{N} \tag{3.11}$$

where $\mathbf{\Psi}(z) = [V_1(z), \ldots, V_n(z)]'$ and $\mathbf{X} = [V_{1S} \ldots, V_{nS}]'$ with $V_i(z)$ the voltage at position z on the ith line and V_{iS} the ith source voltage. Denoting the $n \times n$ source admittance matrix as $\mathbf{Y_S}$ and the $n \times n$ load admittance matrix as $\mathbf{Y_L}$, the transfer function $\mathbf{H}(z)$ is given by [33]

$$\begin{aligned}\mathbf{H}(z) = (\mathbf{A} + \mathbf{B}\mathbf{Y_L})^{-1} \cdot \\ [(\mathbf{C} + \mathbf{D}\mathbf{Y_L}) \cdot (\mathbf{A} + \mathbf{B}\mathbf{Y_L})^{-1} + \mathbf{Y_S}]^{-1} \cdot \mathbf{Y_S}\end{aligned} \tag{3.12}$$

where $\mathbf{A} = \cosh(\sqrt{\mathbf{ZY}}z)$, $\mathbf{B} = \sinh(\sqrt{\mathbf{ZY}}z)\mathbf{Z}_C$, $\mathbf{C} = \mathbf{Y}_C \sinh(\sqrt{\mathbf{ZY}}z)$, and $\mathbf{D} = \mathbf{Y}_C \cosh(\sqrt{\mathbf{ZY}}z)\mathbf{Z}_C$. Here $\mathbf{Z}$ is the $n \times n$ line impedance per unit length, $\mathbf{Y}$ the $n \times n$ line admittance per unit length, and $\mathbf{Z}_C = \mathbf{Y}_C^{-1}$ the $n \times n$ characteristic impedance of the bundle. The diagonal entries of $\mathbf{H}(z)$, $h_{ii} = \frac{V_i(z)}{V_{iS}}$ represent attenuations between ith source voltage V_i and ith line voltage $V_i(z)$. The off-diagonal entries of $\mathbf{H}(z)$, $h_{ij} = \frac{V_i(z)}{V_{jS}}$, $i \neq j$ denote pairwise channel response between jth source voltage V_{jS} and ith line voltage $V_i(z)$. Notice that reflections are ignored because the magnitude of the coupled crosstalk is significantly bigger than the ones of the reflections for the highly coupled interconnect. Hence the aggregate channel response coupled onto the ith line, CEXT_i, can be defined as

$$\mathrm{CEXT}_i = \sum_{\substack{j=1 \\ j \neq i}}^{n} h_{ij} \tag{3.13}$$

This expression describes the aggregate, interwire-crosstalk in the frequency domain for a highly coupled interconnect because the crosstalk dominates the received responses. When the interconnect is highly coupled such as the previous example, the channel crosstalk responses, CEXT_i is crossing over the self-channel responses as shown in Fig. 3.3(d). That indicates the crosstalk noises are comparable to the received signals in the overall frequency ranges. According to [19], including a pre-, $\mathbf{PT}$ and post-processor, $\mathbf{PT}_d$ at the transmitter and the receiver will modify the vector channel response, $\mathbf{H}_m$:

$$\mathbf{H}_m(z) = \mathbf{PT}_d \cdot \mathbf{H}(z) \cdot \mathbf{PT} \tag{3.14}$$

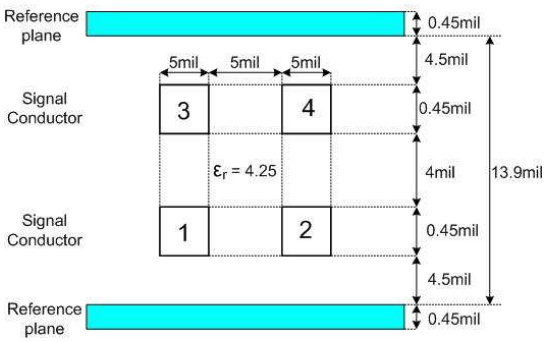
With multimode signaling, we can improve the channel crosstalk by considering the encoder ($\mathbf{T}$) as $\mathbf{PT}$ and the decoder ($\mathbf{T}_d$) as $\mathbf{PT}_d$. Fig. 3.3(e) represents the multimode codec is reducing CEXT_i compared to the conventional single-ended signaling with the previous microstrip example.

3.6 Example 2: Striplines

Let us assume a lossless MTL (n=4) in a homogeneous medium to simplify the example. The geometric structure, L and C of the example are presented in Fig. 3.4. Let us also assume that the conductors are of uniform cross section along the z axis. Parameters are permeability of free space, $\mu_o = 4\pi \times 10^{-7} H/m (= 31.919 nH/inch)$, permittivity of free space, $\epsilon_o = 8.854 \times 10^{-12} F/m (= 224.9 \times 10^{-15} F/in)$, the relative permittivity of FR4, $\epsilon_r = 4.25$ and the relative permeability of FR4, $\mu_r = 1$.

Assuming an operating frequency such that $\omega = 10$ Grad/s, we evaluate the impedance $\mathbf{Z}$ per unit length:

$$\mathbf{Z} = jw\mathbf{L} = j \begin{bmatrix} 3.37 & & & \\ 0.40 & 3.37 & & \\ 1.22 & 0.34 & 3.37 & \\ 0.34 & 1.22 & 0.40 & 3.37 \end{bmatrix} (k\Omega/m) \tag{3.15}$$



$$\mathbf{L} = \begin{bmatrix} 336.5 & & & \\ 40.4 & 336.5 & & \\ 121.6 & 34.7 & 336.5 & \\ 34.7 & 121.6 & 40.4 & 336.5 \end{bmatrix} (nH/m)$$

$$\mathbf{C} = \begin{bmatrix} 163.1 & & & \\ -11.6 & 163.1 & & \\ -57.1 & -5.8 & 163.1 & \\ -5.8 & -57.1 & -11.6 & 163.1 \end{bmatrix} (pF/m)$$

Figure 3.4: Example stripline cross-section with the per-unit-length L and C by Hspice 2D FieldSolver

and the admittance $\mathbf{Y}$ per unit length:

$$\mathbf{Y} = jw\mathbf{C} = j \begin{bmatrix} 1.63 & & & \\ -0.12 & 1.63 & & \\ -0.57 & -0.06 & 1.63 & \\ -0.06 & -0.57 & -0.12 & 1.63 \end{bmatrix} (S/m) \tag{3.16}$$

Then the matrix products $\mathbf{ZY}$ and $\mathbf{YZ}$ are

$$\mathbf{ZY} = \mathbf{YZ} = \begin{bmatrix} -4727.0 & 0.1 & 1.8 & 1.0 \\ 0.1 & -4727.0 & 1.0 & 1.8 \\ 1.8 & 1.0 & -4727.0 & 1.0 \\ 1.0 & 1.8 & 1.0 & -4727.0 \end{bmatrix} m^{-2} \tag{3.17}$$

The eigenvalues γ_i^2 of $\mathbf{ZY}$ or $\mathbf{YZ}$ are $\gamma_1^2 = -4724.2$, $\gamma_2^2 = -4729.7$, $\gamma_3^2 = -4726.2$, and $\gamma_4^2 = -4727.9$. Thus the propagation constants $(\gamma_1, \gamma_2, \gamma_3, \gamma_4)$ and phase velocities

(c_1, c_2, c_3, c_4) of the four modes:

$$\begin{aligned}
&\gamma_1 = \sqrt{-4724.2} = j\beta_1; \quad \beta_1 = 68.73\, rad/m; \quad c_1 = \omega/\beta_1 = 1.4549 \times 10^8 m/s.\\
&\gamma_2 = \sqrt{-4729.7} = j\beta_2; \quad \beta_2 = 68.77\, rad/m; \quad c_2 = \omega/\beta_2 = 1.4541 \times 10^8 m/s.\\
&\gamma_3 = \sqrt{-4726.2} = j\beta_3; \quad \beta_3 = 68.75\, rad/m; \quad c_3 = \omega/\beta_3 = 1.4546 \times 10^8 m/s.\\
&\gamma_4 = \sqrt{-4727.9} = j\beta_4; \quad \beta_4 = 68.76\, rad/m; \quad c_4 = \omega/\beta_4 = 1.4543 \times 10^8 m/s.
\end{aligned} \tag{3.18}$$

Since each column of $\mathbf{T}$ consists of the eigenvectors of γ_i^2, $\mathbf{T}$ can be easily obtained using such as Matlab,

$$\mathbf{T} = [\mathbf{t_1}\ \mathbf{t_2}\ \mathbf{t_3}\ \mathbf{t_4}] = \begin{bmatrix} 0.5 & 0.5 & 0.5 & 0.5 \\ 0.5 & 0.5 & -0.5 & -0.5 \\ 0.5 & -0.5 & 0.5 & -0.5 \\ 0.5 & -0.5 & -0.5 & 0.5 \end{bmatrix} \tag{3.19}$$

where $\mathbf{t_1}$, $\mathbf{t_2}$, $\mathbf{t_3}$, and $\mathbf{t_4}$ denote 4×1 column vectors. From the relationship of $\mathbf{S}^t = \mathbf{T}^{-1}$, $\mathbf{S}$ is

$$\mathbf{S} = (\mathbf{T}^{-1})^t = \begin{bmatrix} 0.5 & 0.5 & 0.5 & 0.5 \\ 0.5 & 0.5 & -0.5 & -0.5 \\ 0.5 & -0.5 & 0.5 & -0.5 \\ 0.5 & -0.5 & -0.5 & 0.5 \end{bmatrix} \tag{3.20}$$

Assuming four inputs (d_1, d_2, d_3, d_4) to the transmitter as $\mathbf{V}_m = [d_1, d_2, d_3, d_4]^t$, the output of the transmitter $\mathbf{V} = [V_1, V_2, V_3, V_4]^t$ at $z = 0$ is,

$$\begin{aligned}
\mathbf{V} = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = \mathbf{T}\mathbf{V}_m &= \begin{bmatrix} 0.5 & 0.5 & 0.5 & 0.5 \\ 0.5 & 0.5 & -0.5 & -0.5 \\ 0.5 & -0.5 & 0.5 & -0.5 \\ 0.5 & -0.5 & -0.5 & 0.5 \end{bmatrix} \begin{bmatrix} d_1 \\ d_2 \\ d_3 \\ d_4 \end{bmatrix} \\
&= 0.5 \begin{bmatrix} d_1 + d_2 + d_3 + d_4 \\ d_1 + d_2 - d_3 - d_4 \\ d_1 - d_2 + d_3 - d_4 \\ d_1 - d_2 - d_3 + d_4 \end{bmatrix}
\end{aligned} \tag{3.21}$$

Note that V_1 denotes a common mode and V_2, V_3 and V_4 denote differential modes and (3.21) implies that the transmitted output is expressed with the column vectors of $\mathbf{T}$ as the basis [34],

$$\mathbf{V} = \sum_{i=1}^{4} d_i \mathbf{t}_i = d_1\mathbf{t}_1 + d_2\mathbf{t}_2 + d_3\mathbf{t}_3 + d_4\mathbf{t}_4 \tag{3.22}$$

From [35, Table I] listing matrix expression for characteristic impedance/admittance of MTL, one expression of characteristic impedance matrix $\mathbf{Z}_C$ is

$$\mathbf{Z}_C = \mathbf{T}\gamma\mathbf{T}^{-1}\mathbf{Y}^{-1} = \begin{bmatrix} 48.9472 & 5.8793 & 17.6964 & 5.0533 \\ 5.8793 & 48.9472 & 5.0533 & 17.6964 \\ 17.6964 & 5.0533 & 48.9472 & 5.8793 \\ 5.0533 & 17.6964 & 5.8793 & 48.9472 \end{bmatrix} \tag{3.23}$$

where $\gamma = diag(\gamma_1, \gamma_2, \gamma_3, \gamma_4)$. The corresponding admittance matrix $\mathbf{Y}_C$ is

$$\mathbf{Y}_C = \mathbf{Z}_C^{-1} = \mathbf{Y}\mathbf{T}\gamma^{-1}\mathbf{T}^{-1} = \begin{bmatrix} 0.0237 & -0.0017 & -0.0083 & -0.0008 \\ -0.0017 & 0.0237 & -0.0008 & -0.0083 \\ -0.0083 & -0.0008 & 0.0237 & -0.0017 \\ -0.0008 & -0.0083 & -0.0017 & 0.0237 \end{bmatrix} \tag{3.24}$$

To remove the reflection at the receiver, we should choose a termination admittance matrix $\mathbf{Y}_{tload}$ equal to $\mathbf{Y}_C$ (or $\mathbf{Z}_{tload} = \mathbf{Z}_C$). With the equation in [25, (1.84)], we could compute the termination load values of Fig. 3.5 as,

$$\begin{aligned} Z_{k0} &= \left(\sum_{i=1}^{4} (Y_C)_{ki} \right)^{-1} \\ Z_{ki} &= 1/(Y_C)_{ki} \end{aligned} \tag{3.25}$$

where Z_{ki} denotes the termination load between the kth line and ith line at the receiver input, Z_{k0} between the kth line and the reference plane, and $(Y_C)_{ki}$ the kth-row and ith-column element of $\mathbf{Y}_C$, $k = 1, \ldots, 4$. Note that (3.25) can be obtained by applying the KCL to each node in Fig. 3.5. The resulting impedance values of

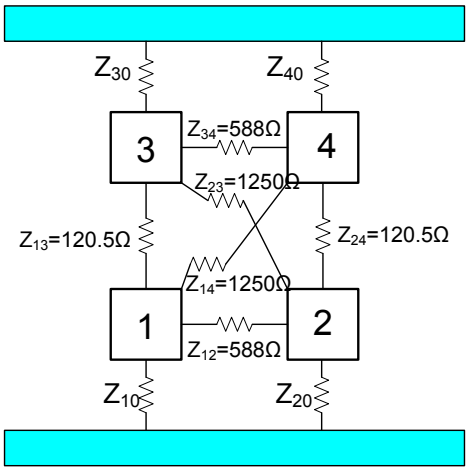


Figure 3.5: Termination network of the example multiconductor

Fig. 3.5 are

$$\begin{aligned} Z_{10} = Z_{20} = Z_{30} = Z_{40} &= 1/(0.0237 - 0.0017 - 0.0083 - 0.0008) = 77.5\Omega \\ Z_{12} = Z_{34} &= 1/0.0017 = 588.2\Omega \\ Z_{13} = Z_{24} &= 1/0.0083 = 120.5\Omega \\ Z_{14} = Z_{23} &= 1/0.0008 = 1250\Omega \end{aligned} \tag{3.26}$$

At the receiver side, we can recover the transmitted inputs $\mathbf{V}_m = [d_1, d_2, d_3, d_4]^t$ by using the relationship $\mathbf{V}_m = \mathbf{T}^{-1}\mathbf{V}$ from (3.5).

To achieve high interconnect density with multimode signaling, it is required to analyze inter-bundle crosstalk when multiple closely-placed bundles are deployed. Knowledge of the inter-bundle crosstalk as a function of bundle-to-bundle spacing will give us an indication of the achievable interconnect density with multiple bundles. In differential signaling, a rule of thumb of differential pair spacing for avoiding severe crosstalk noise is about 4 or 5 times the dielectric height.

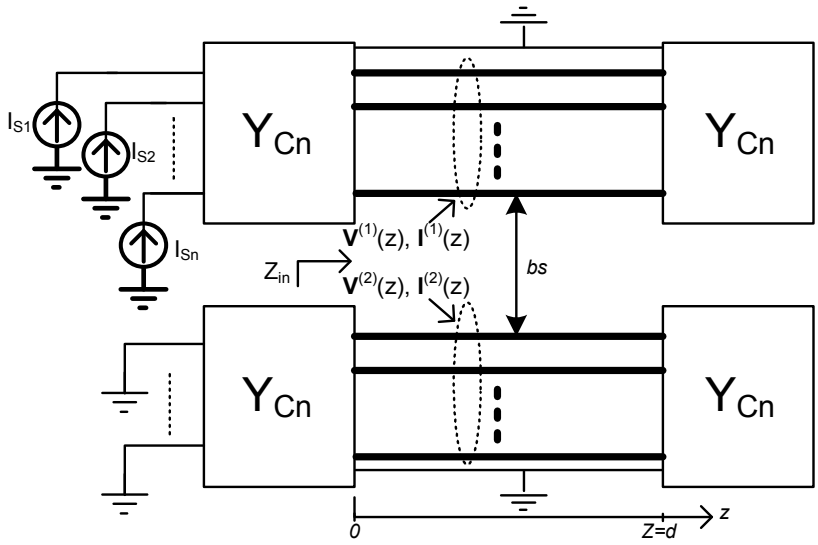


Figure 3.6: Inter-bundle crosstalk between two bundles

3.7 Inter-bundle Crosstalk

In this section, we show how to account for inter-bundle crosstalk in terms of the coupled modal currents when multimode signaling is being employed. This is analogous to the mixed-mode S-parameters describing the mode conversion between differential and common modes in conventional differential signaling. The majority of the analysis is to formulate a two-bundle problem with ABCD parameters and boundary conditions. A simple scheme of examining the effect of bundle spacing on inter-bundle crosstalk is also presented.

Consider two identical bundles (comprising of microstrips or strip lines, for example) placed parallel to each other, where a bundle consists of n uniform coupled conductor lines and a reference ground (Fig. 3.6). The two bundles are separated by the bundle-to-bundle spacing *bs*. Here we assume that an aggressor is bundle 1 and bundle 2 consists of quiet lines. The vector source $\mathbf{I}_S = [I_{S1}, I_{S2}, \ldots, I_{Sn}]^t$ is connected to the left end (the near end) of bundle 1 where $[.]^t$ is the transpose of [.]. All ends of the bundles are terminated with an admittance (impedance) equal to the characteristic admittance (impedance) Y_{Cn} (Z_{Cn}) of a single bundle in isolation,

obtained in the limit of $bs \to \infty$. Under the quasi-TEM assumption, the electrical behavior of the two-bundle system is governed by the telegraphers equation in phasor form [26],

$$\begin{aligned} -\frac{d\mathbf{V}(z)}{dz} &= \mathbf{Z} \cdot \mathbf{I}(z) \\ -\frac{d\mathbf{I}(z)}{dz} &= \mathbf{Y} \cdot \mathbf{V}(z) \end{aligned} \tag{3.27}$$

where $\mathbf{V} = [V_1^{(1)}, \ldots, V_n^{(1)}, V_1^{(2)}, \ldots, V_n^{(2)}]^t$ is the $2n \times 1$ column vector of line voltages and $\mathbf{I} = [I_1^{(1)}, \ldots, I_n^{(1)}, I_1^{(2)}, \ldots, I_n^{(2)}]^t$ the $2n \times 1$ column vector of line currents on the two bundles at position z along the bundles. Here $V_j^{(i)}$ and $I_j^{(i)}$ are the j-th line voltage and current, respectively, on bundle i. Furthermore, $\mathbf{Z} = \mathbf{R} + \mathbf{j}\omega\mathbf{L}$ is the $2n \times 2n$ per-unit-length(p.u.l.) impedance matrix and $\mathbf{Y} = \mathbf{G} + \mathbf{j}\omega\mathbf{C}$ is the $2n \times 2n$ p.u.l. admittance matrix. $\mathbf{R}$,$\mathbf{L}$,$\mathbf{G}$,and $\mathbf{C}$ are $2n \times 2n$ p.u.l. resistance ,inductance,conductance, and capacitance matrices, respectively.

Since generally n conductors have n propagation modes, line voltages and currents can be expressed as a superposition of modal voltages $\mathbf{V}_m$ and currents $\mathbf{I}_m$ by using transformation matrices $\mathbf{T}_V$ and $\mathbf{T}_I$, respectively. Each column of the $2n \times 2n$ $\mathbf{T}_V$ (or $\mathbf{T}_I$) matrix consists of the eigenvectors of $\mathbf{ZY}$ (or $\mathbf{YZ}$). As a first step, to describe the line voltages and currents of the two bundles at both ends ($z = d, z = 0$) of the lines, ABCD parameters (or chain parameters) each of size $2n \times 2n$ can be employed in matrix form:

$$\begin{bmatrix} \mathbf{V}(d) \\ \mathbf{I}(d) \end{bmatrix} = \begin{bmatrix} \mathbf{A}(d) & \mathbf{B}(d) \\ \mathbf{C}(d) & \mathbf{D}(d) \end{bmatrix} \begin{bmatrix} \mathbf{V}(0) \\ \mathbf{I}(0) \end{bmatrix} \tag{3.28}$$

Here the ABCD parameters for the system of two bundles of length d are defined as [26].

$$\begin{aligned} \mathbf{A}(d) &= \mathbf{Z}_C \cosh(\sqrt{\mathbf{YZ}}d)\mathbf{Y}_C & \mathbf{B}(d) &= -\mathbf{Z}_C \sinh(\sqrt{\mathbf{YZ}}d) \\ \mathbf{C}(d) &= -\sinh(\sqrt{\mathbf{YZ}}d)\mathbf{Y}_C & \mathbf{D}(d) &= \cosh(\sqrt{\mathbf{YZ}}d) \end{aligned} \tag{3.29}$$

where $\mathbf{Y}_C(\mathbf{Z}_C)$ is the characteristic admittance (impedance) of the two coupled bundles obtained by $\mathbf{Z}^{-1}\mathbf{T}_v\mathbf{\Gamma}\mathbf{T}_v^{-1}$ [35]. Note that here Γ is a $2n \times 2n$ diagonal matrix

whose elements are the eigenvalues of $\mathbf{YZ}$. To derive the input impedance $\mathbf{Z}_{in}$, we need to rewrite Eq.(3.28) as

$$\begin{bmatrix} \mathbf{V}(0) \\ \mathbf{I}(0) \end{bmatrix} = \begin{bmatrix} \mathbf{A}(d) & -\mathbf{B}(d) \\ -\mathbf{C}(d) & \mathbf{D}(d) \end{bmatrix} \begin{bmatrix} \mathbf{V}(d) \\ \mathbf{I}(d) \end{bmatrix} \tag{3.30}$$

With $\mathbf{V}(d) = \mathbf{Z}_L\mathbf{I}(d)$ and $\mathbf{V}(0) = \mathbf{Z}_{in}\mathbf{I}(0)$, we can obtain $\mathbf{Z}_{in}$ as

$$\mathbf{Z}_{in} = [\mathbf{A}(d)\mathbf{Z}_L - \mathbf{B}(d)][\mathbf{D}(d) - \mathbf{C}(d)\mathbf{Z}_L]^{-1} \tag{3.31}$$

where $\mathbf{Z}_L = [\mathbf{Z}_{Cn}\ \mathbf{0}_n; \mathbf{0}_n\ \mathbf{Z}_{Cn}]$ with $\mathbf{0}_n$ the $n \times n$ zero matrix. From the boundary condition

$$\mathbf{I}(0) = \mathbf{I}_S^t - \mathbf{Z}_L^{-1}\mathbf{Z}_{in}\mathbf{I}(0)$$

$\mathbf{I}(0)$ and $\mathbf{V}(0)$ can be expressed as

$$\mathbf{I}(0) = (\mathbf{U}_{2n} + \mathbf{Z}_L^{-1}\mathbf{Z}_{in})^{-1}\mathbf{I}_S^t \tag{3.32}$$

$$\mathbf{V}(0) = \mathbf{Z}_{in}\mathbf{I}(0) \tag{3.33}$$

where $\mathbf{I}_S^t = [\mathbf{I}_S, 0, \ldots, 0]^t$ is a $2n \times 1$ column vector and $\mathbf{U}_{2n}$ the $2n \times 2n$ unity matrix. Therefore, $\mathbf{I}(d)$ and $\mathbf{V}(d)$ can be obtained from $\mathbf{I}_S$ and the ABCD parameters based on Eq.(3.28).

One approach to measure inter-bundle crosstalk for multimode signaling is to examine the modal conversion between bundles. Since multimode signaling transmits a linear combination of n modes, inter-bundle crosstalk can be considered as equivalent to measuring the coupled mode signals on bundle 2, $\mathbf{I}_m^{j(2)}$, by exciting each mode at bundle 1, $\mathbf{I}_m^{j(1)}$, where j denotes the j-th mode of a bundle ($j = 1, \ldots, n$). From Eq.(3.28), (3.32),and (3.33), we can obtain the line current $\mathbf{I}^{(2)}(d)$ with $\mathbf{I}_S = \mathbf{I}_m^{j(1)}$ and thereby the coupled mode current $\mathbf{I}_m^{j(2)}$ as

$$\mathbf{I}_m^{j(2)}(d) = \mathbf{T}_{In}^{-1}\mathbf{I}^{(2)}(d) \tag{3.34}$$

where $\mathbf{T}_{In}$ is a $n \times n$ matrix in which each column is an eigenvector of $\mathbf{Y}_n\mathbf{Z}_n$. Here $\mathbf{Y}_n$ ($\mathbf{Z}_n$) is the $n \times n$ p.u.l. admittance (impedance) matrix of a single bundle ($bs \to \infty$).

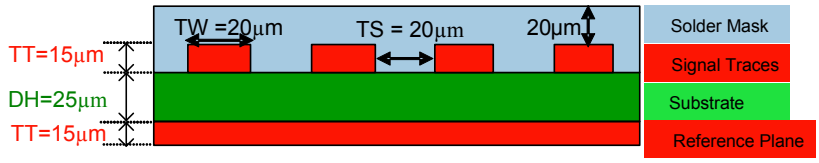


Figure 3.7: Example of a bundle on a package substrate (cross-section)

If we extract $2n \times 2n$ matrices of $\mathbf{Z}$ and $\mathbf{Y}$ with varying bundle spacing (bs) and obtain the coupled mode current at bundle 2, $\mathbf{I}_m^{j(2)}$ from Eq.(3.34), the inter-bundle crosstalk can be quantified as a function of bs. In the next section, the inter-bundle crosstalk of an example interconnect is presented with varying bundle spacing when exciting each mode at bundle 1.

3.8 Numerical Example of Inter-Bundle Crosstalk

For demonstrating the inter-bundle crosstalk analysis in the previous section numerically, we consider an embedded microstrip bundle consisting of four lines as shown in Fig. 3.7. The line width, spacing, and thickness are 20um , 20um, and 15um, respectively. The thickness of solder mask, substrate, and reference plane are 20 m, 25 m, and 15 m, respectively. The bundle RLGC matrices of the example can be obtained from a 2-D electromagnetic field solver such as Ansoft 2D Extractor as illustrated in Fig. 3.8. From the small values of R [Fig. 3.8(a)] and G [Fig. 3.8(c)] we can justify the low-loss assumption of quasi-TEM analysis. The coupling values of capacitance [Fig. 3.8(d)] and inductance [Fig. 3.8(b)] are $C_m/C_{ii} = 0.33$ and $L_m/L_{ii} \approx 0.25$, respectively. Note that capacitance values in the example are frequency-independent because of all conductors having high conductivity and dielectric constants are assumed to be frequency-independent; correspondingly, $\mathbf{G}$ in Fig. 3.8(c) exhibits the expected linear behavior (frequency-independent loss tangents). The frequency dependency of $\mathbf{R}$ and $\mathbf{L}$ is related to the skin effect for conductors of finite conductivity. The four modes of the example bundle are illustrated in Fig. 5 with a propagation constant, $\gamma = \alpha + j\beta$ of each mode, where α is the attenuation constant and β is

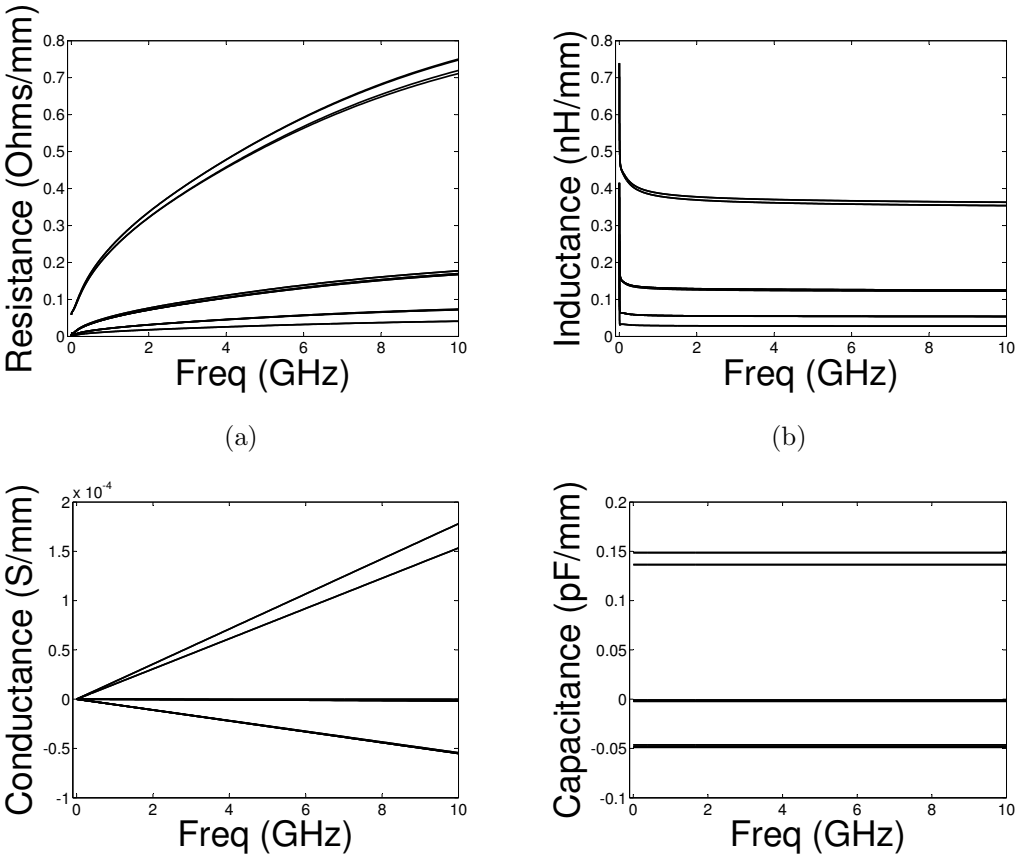


Figure 3.8: Per-unit-length matrices $\mathbf{R}, \mathbf{L}, \mathbf{G}, \mathbf{C}$ of size 4×4: (a) Resistance per-unit-length $\mathbf{R}$; (b) Inductance per-unit-length $\mathbf{L}$; (c) Conductance per-unit-length $\mathbf{G}$; and, (d) Capacitance per-unit-length $\mathbf{C}$

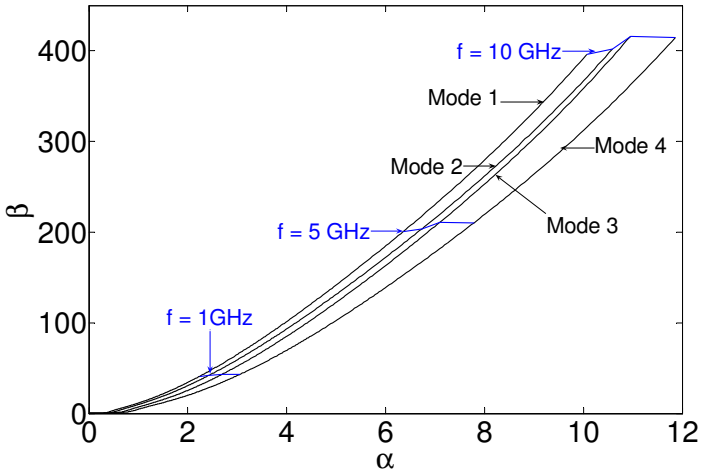


Figure 3.9: Four modes of the example bundle represented by propagation constant, $\gamma = \alpha + j\beta$ of each mode, where α is the attenuation constant and β the phase constant. The blue lines indicate α and β of each mode corresponding to the same frequency.

the phase constant. Each mode can be characterized by the attenuation constants because the differences of phase constants of four modes are very small.

Two example bundles are configured as an interconnect of embedded microstrip lines consisting of eight parallel lines. The line length is set to 2 cm, a nominal diagonal length on typical flip chip ball/land grid array (FCBGA/FCLGA) packages. The simulation setup follows the configuration of Fig. 3.6: Both ends of the bundles are terminated with the characteristic admittance $\mathbf{Y}_{C4}$ of an individual bundle (obtained in absence of the other bundle). The left end of bundle 1 is excited with a current mode eigenvector $\mathbf{I}_S = \mathbf{I}_m^{j(1)}$, a column vector of $\mathbf{T}_{I4}$ (4×4 matrix) among four modes in the frequency domain. By using ABCD parameters and the boundary conditions, the line currents of bundle 2 at z = 2 cm are calculated, that is, the crosstalk noise coupled to bundle 2 with respect to a modal current $\mathbf{I}_m^{j(1)}$. To examine the potential density benefit of multimode signaling, we need to simulate the coupled mode currents with different RLGC matrices corresponding to the varying bundle spacing. Here we consider two cases of bundle spacings: $bs = 100$ um for the weakly coupled case and $bs = 20$ um for the case of strongly coupled bundles. To explore the possibility of the practical application of multimode signaling, the responses with

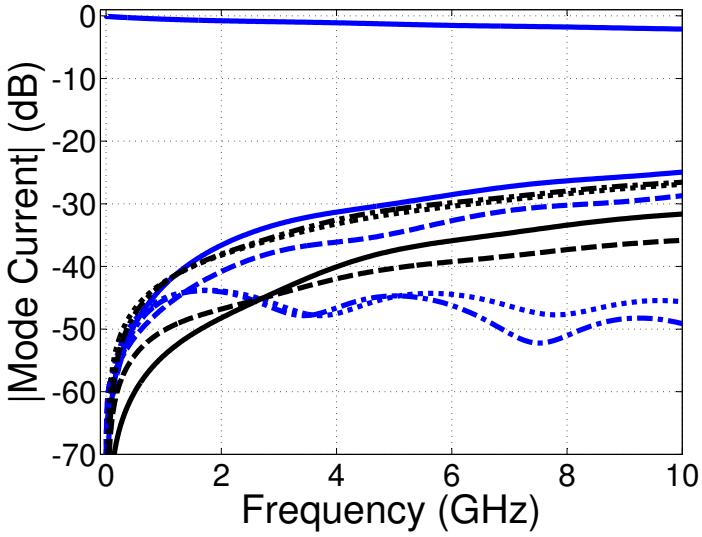


Figure 3.10: The far-end coupled mode currents at bundle 2 due to excitation of mode 1 currents at bundle 1 with frequency-dependent matched termination for bundle spacing of 20 um (blue) and 100 um (black).

non-matched termination such as passive elements directly connected between ends of lines and reference ground have also been computed.

3.8.1 With frequency-dependent termination $\mathbf{Y}_{L4}(f)$

All ends of the bundles are terminated with the characteristic admittance $\mathbf{Y}_{L4}(f)$ of the example bundle derived for each frequency. Fig. 3.10 demonstrates the mode conversion coupled to the adjacent bundle 2 by exciting the mode 1 currents at bundle 1 for two different values of bundle spacing (bs = 20 um and 100 um). This is done by plotting the coupled modal currents on bundle 2,$\mathbf{I}_m^{j(2)}(d = 2cm)$, when bundle 1 is excited with mode 1, 2, 3, or 4. As a representative example the mode 1 current vector,$\mathbf{I}_S = \mathbf{I}_m^{1(1)}$, is excited. The far-end response on bundle 1 is shown by the top line of Fig. 3.10(insertion loss). The black lines are the coupled modal currents on bundle 2 when $bs = 100um$ and the blue lines (except the line at the top) are the coupled modal currents on bundle 2 when $bs = 20um$ for the four current modes. Considering the plots for all four modes, we can see that only a few dB increase result by reducing the bundle spacing from 100 um to 20 um. This implies that

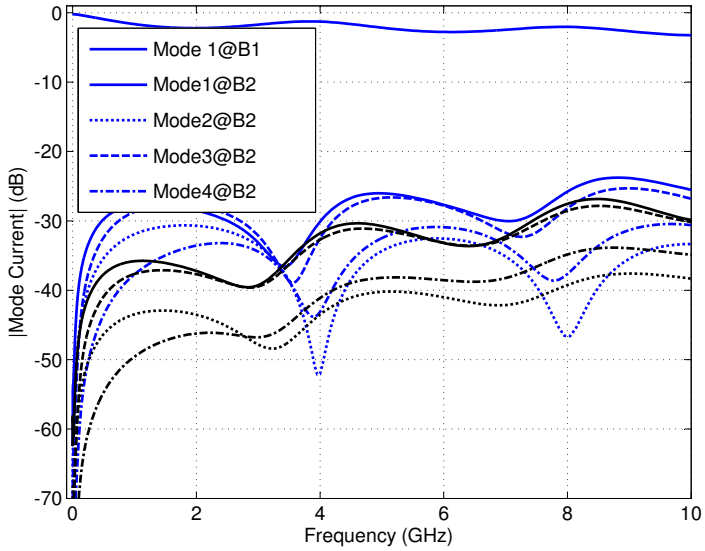


Figure 3.11: The far-end coupled mode currents at bundle 2 due to excitation of mode 1 currents at bundle 1 with frequency-independent termination for bundle spacing of 20 um (blue) and 100 um (black).

the inter-bundle crosstalk noise increases less than two times in magnitude when the bundle spacing is reduced by five times. Crosstalk magnitude is $<$ -25 dB up to 10 GHz.

3.8.2 With frequency-independent termination($\mathbf{Y}_{L4} = \text{const}$)

In practice, it would be difficult to make a termination network $\mathbf{Y}_{L4}$ having a specified wide-range frequency-dependent response using passive elements. Therefore, as a second numerical experiment, $\mathbf{Y}_{L4}$ is set to be a diagonal matrix in which each diagonal element is 1/50 S, thereby anticipating reflections due to an imperfectly matched termination. Fig. 3.11 illustrates the far-end coupled mode currents on bundle 2 by connecting the admittance of 1/50 S between the ends of the lines and reference ground. All other conditions are the same as for Fig. 3.10. We observe resonances at certain frequencies indicating imperfect termination. Depending on the bundle spacing, the far-end coupled mode currents have shifted up by up to about 10 dB. Compared with the matched termination (Fig. 3.10) reflections from the imperfect

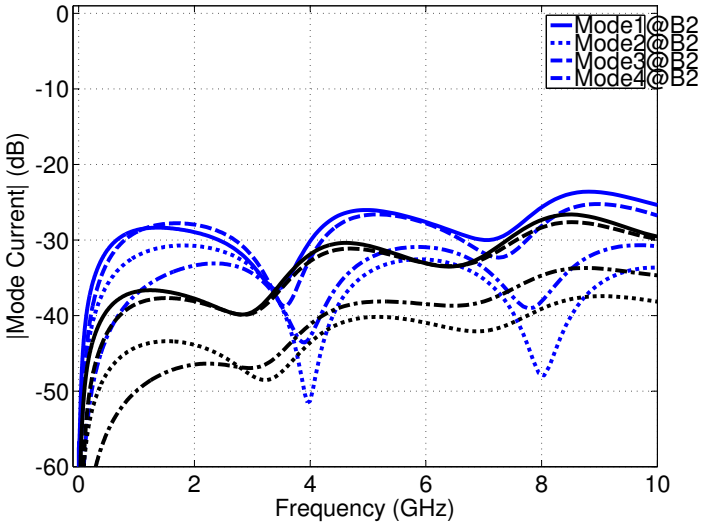


Figure 3.12: The far-end coupled mode currents at bundle 2 due to excitation of the frequency-independent mode 1 current at bundle 1 with the frequency-independent termination for bundle spacing 20 um (blue) and 100 um (black).

termination affect lower frequencies more severely than those above 6 GHz. Crosstalk magnitude in this example remains $<$ -23 dB up to 10 GHz.

3.8.3 With frequency-independent termination and a fixed source current mode 1

In general, the modal currents, the column vectors of $\mathbf{T}_{I4}$ functioning as a source current at bundle 1, are frequency-dependent unless the cross-section of the interconnect structure is cyclic symmetric [26]. But the practical application calls for a frequency-independent $\mathbf{T}_{I4}$ working as an encoder in multimode signaling (Fig. 3.2). In Fig. 3.12, the source mode 1 current $\mathbf{I}_S = \mathbf{I}_m^{1(1)}$ is set to the value when the arbitrarily selected frequency is 5 GHz. Compared to section 3.8.2 above, the fixed $\mathbf{T}_{I4}$ does not affect the coupled noise, as the magnitude variation of mode currents with respect to frequencies is very small in this example.

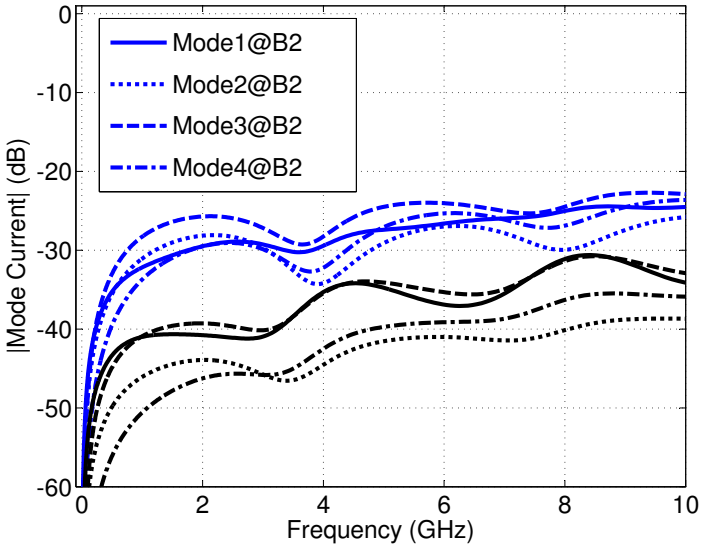


Figure 3.13: The far-end coupled mode currents at bundle 2 due to excitation of the frequency-independent four mode currents summed together at bundle 1 with frequency-independent termination and for bundle spacing 20 um (blue) and 100 um (black).

3.8.4 With frequency-independent termination and exciting four modes summed together

Since the multimode signaling utilizes the linear combination of all the bundle modes, we now consider a source current $\mathbf{I}_S$ that is the sum of all the four current modes. Note that each current mode is taken as frequency-independent. All other conditions are the same as section 3.8.3. The results are shown in Fig. 3.13. We can notice that crosstalk magnitude still remains $<$ -23 dB up to 10 GHz by reducing the bundle spacing up to 20 um.

The near-end inter-bundle crosstalk for two bundle spacing (20 um and 100 um) also presents the similar results, that is, the near-end inter-bundle crosstalk $<$ -20 dB for all four cases described above.

The above four examples with different terminations illustrate the insensitivity of inter-bundle crosstalk when varying the bundle spacing by five times. Therefore, we could increase the interconnect density with multimode signaling when employ-

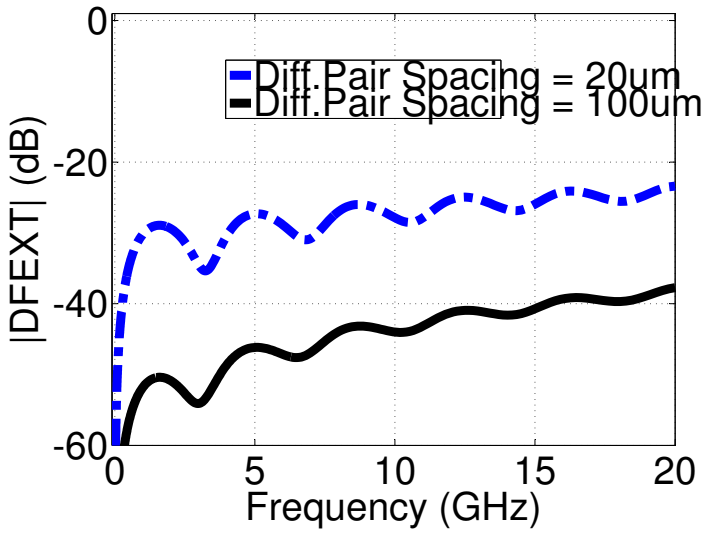


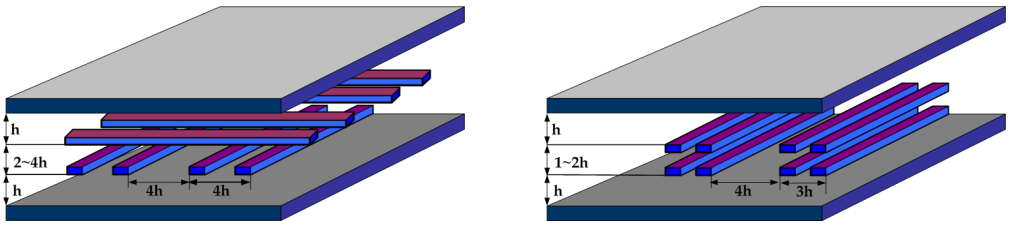
Figure 3.14: The far-end differential crosstalk for differential pair spacing 20 um (blue) and 100 um (black)

ing many bundles simultaneously. The next section describes the density benefit of multimode signaling compared to the conventional differential signaling.

3.9 Density Benefit of Multimode Signaling

To see the density benefit of multimode interconnects compared to the conventional differential signaling, the far-end differential crosstalk (DFEXT) is illustrated in Fig. 3.14 for two values of differential pair spacing (20 um and 100 um). The DFEXT increases over three times in magnitude when reducing the differential pair spacing by five times, describing the sensitivity of the differential signaling to the pair spacing. This implies that the density benefit of multimode signaling is ideally two times of the differential signaling because the differential signaling consumes two lines per signal transmission and the far-end crosstalk noise is about the same for both signaling. Fig. 3.15 represents the density comparison between differential and multimode signaling. Two inner layers are assigned as signal layers between reference planes. The symbol **h** is defined as a vertical distance between lower reference plane and a signal layer, representing a dielectric thickness. Fig. 3.15(a) illustrates

sending four signals with four differential pairs in two inner signal layers. The horizontal dimension is computed as **16h** when we assume the inter-pair spacing is **4h**. Fig. 3.15(b) describes sending eight signals with two bundles, that is eight wires. In this case, the horizontal dimension is **14h** provided that the inter-bundle spacing is **4h**. Since the previous example demonstrates that the inter-bundle crosstalk is insensitive to the bundle spacing, we could improve horizontal density even higher than two times.



(a) (b)

Figure 3.15: Interconnect Density Comparison between differential and multimode signaling: (a) Four, differential pairs using two signal layers when sending four signals, (b) Multimode interconnect consisting of two bundles for sending eight signals

3.10 Conclusion

This chapter summarized the motivation for multimode signaling by introducing highly-coupled microstrip lines. By using the suggested signaling scheme, we could reduce the effective crosstalk and recover the original data. The frequency domain analysis with the signaling scheme indicates that the inter-wire crosstalk is reduced by codec operations. The stripline example describes how we could compute the full termination network for ideal multiline termination. To guarantee the density increase with this scheme, we also analyzed the bundle-to-bundle crosstalk because the spacing between bundles need to be reduced for dense interconnect. WIth different termination schemes, the simulations done in the frequeny domain determined the spacing between bundles is less likely to worsen bundle-to-bundle crosstalk.

Chapter 4

Design of Multimode Signaling Transceiver

This chapter describes the system architecture of multimode signaling transceiver for a chip-to-chip interconnect. The implementation example gives us a guideline how we could incorporate the encoder and decoder into the multimode transmitter and receiver.

4.1 System Architecture

Fig. 4.1 illustrates the system architecture of multimode signaling transceiver. Contrary to conventional I/O transceivers, multimode transceiver incorporates an encoder and a decoder that are implemented with the eigenmodes of a link. The chip-to-chip link between the transceiver consists of a 6 cm four-wire in which stacked-pair wires are sandwiched between reference planes, forming stripline structure as shown in Fig. 4.2. Four wires are chosen for the reasonable amount of circuit complexity and measurement capability. To transmit four parallel high-speed data, (d_1, d_2, d_3, d_4), the four-independent data streams are provided by four, on-die pseudo-random-bit-sequence(PRBS) generators. Here d_1, d_2, d_3, and d_4 are the outputs of four PRBS respectively. In this example architecture, the data rates of input sequences to the

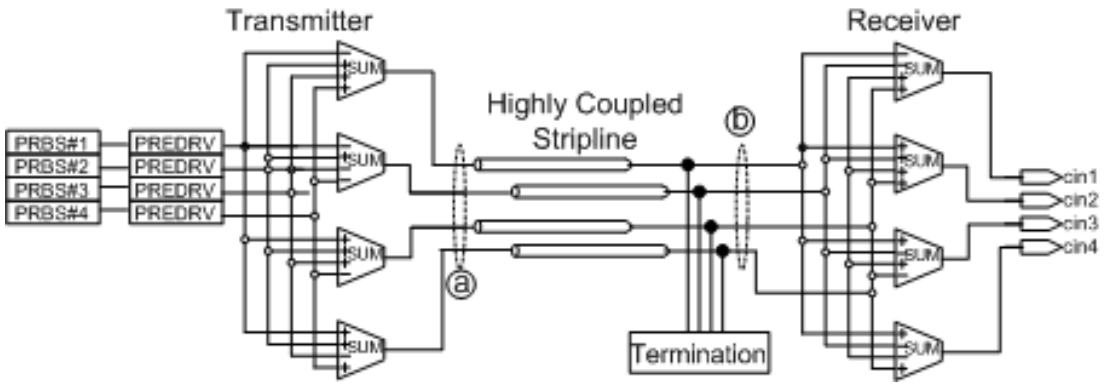


Figure 4.1: System Architecture of multimode signaling transceiver

transmitter is restricted by the external clock directly connected to the PRBS, therefore the operating speed of the transceiver is limited by the external clock frequency. In general, the operating speed of the system would be limited by the reflections when single-ended terminations are connected. The linear combination rules of the parallel PRBS data at the transmitter are governed by the eigenmodes ($\mathbf{t_1}$, $\mathbf{t_2}$, $\mathbf{t_3}$, and $\mathbf{t_4}$) of the example link geometry matrices, $\mathbf{LC}$,

$$\mathbf{T}_4 = [\mathbf{t_1}\ \mathbf{t_2}\ \mathbf{t_3}\ \mathbf{t_4}] = \begin{bmatrix} 0.5 & 0.5 & 0.5 & 0.5 \\ 0.5 & 0.5 & -0.5 & -0.5 \\ 0.5 & -0.5 & 0.5 & -0.5 \\ 0.5 & -0.5 & -0.5 & 0.5 \end{bmatrix} \tag{4.1}$$

where $\mathbf{t_1}$, $\mathbf{t_2}$, $\mathbf{t_3}$, and $\mathbf{t_4}$ denote 4×1 column vectors. Whereas we assume lossless wires to simplify the encoder $\mathbf{T}$ and $\mathbf{T}$ would work for a short link, in general the effective crosstalk would not be zero with the derived encoder, $\mathbf{T}$ if the link is relatively long. The encoded parallel signals, $\mathbf{V}_t$ can be described by

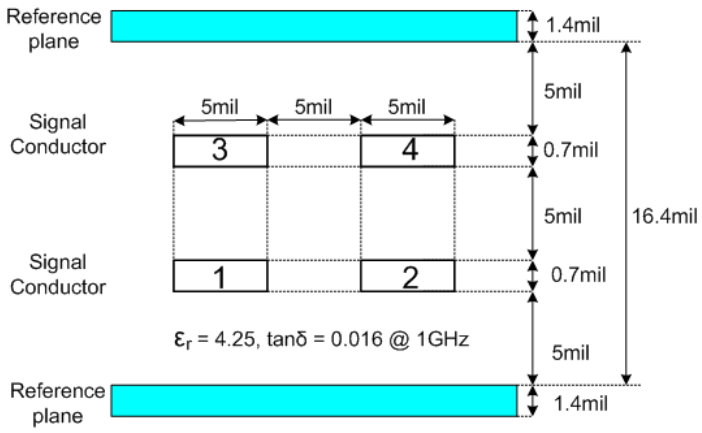


Figure 4.2: Cross-sectional View of stripline link

$$\begin{aligned}\mathbf{V}_t = [V1_t,\ V2_t,\ V3_t,\ V4_t]^{'} &= \mathbf{T}_4\mathbf{V}_m = d_1\mathbf{t}_1 + d_2\mathbf{t}_2 + d_3\mathbf{t}_3 + d_4\mathbf{t}_4 \\ &= 0.5\begin{bmatrix} d_1+d_2+d_3+d_4 \\ d_1+d_2-d_3-d_4 \\ d_1-d_2+d_3-d_4 \\ d_1-d_2-d_3+d_4 \end{bmatrix}\end{aligned} \tag{4.2}$$

where $\mathbf{V}_m = [d_1, d_2, d_3, d_4]^{'}$ represents four parallel data. At the point ⓐ of Fig. 4.1, the transmitted signals, $\mathbf{V}_t$, are linearly combined waveforms having multi-level values. At the probing location ⓑ, the received waveforms represent the resultant signals that have various levels of voltages determined by the reflections. Fig. 4.3 illustrates the simulated waveforms at ⓐ and ⓑ. The termination was implemented with on-die active resistors that are designed with poly and PMOS transistors. The detailed implementation of the termination is described in the later section. The decoded signals, cin1-cin4, are directly on-die probed for validating the signals.

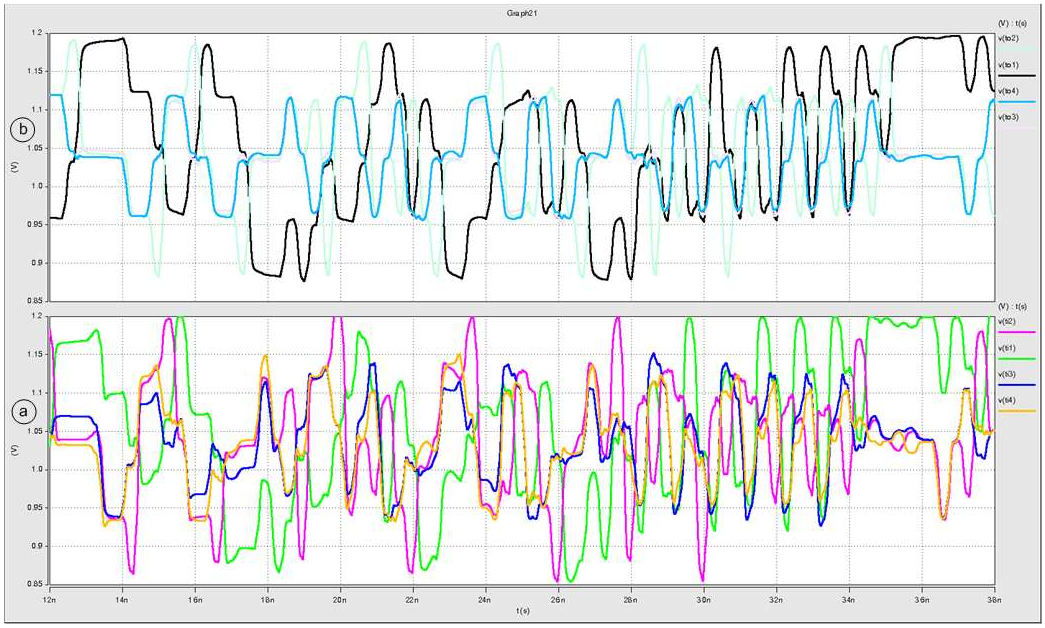


Figure 4.3: Simulated Waveforms of Transmitter outputs (ⓐ) and Receiver Inputs (ⓑ)

4.2 Transmitter

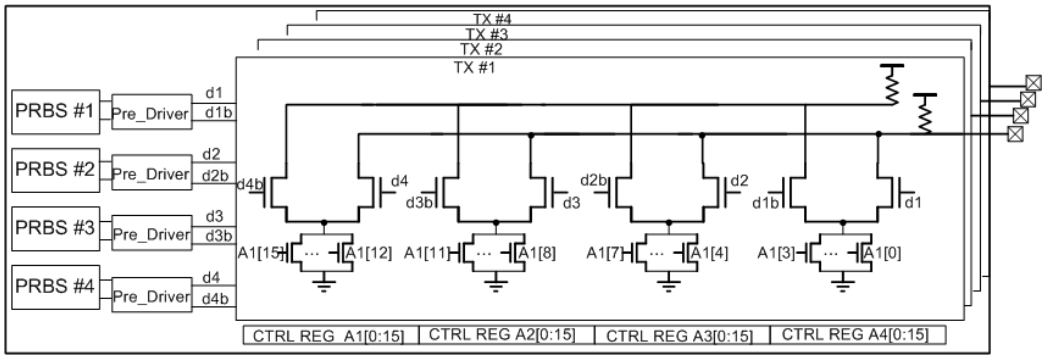


Figure 4.4: Transmitter Architecture of multimode signaling

The transmitter (TX) of multimode signaling as shown in Fig. 4.4 comprises four, on-die pseudo-random sequence generators (PRBS), pre-drivers, control registers, and main-drivers, driving four wires respectively.

The main driver consists of four-pairs of differential-open drain and is driving the

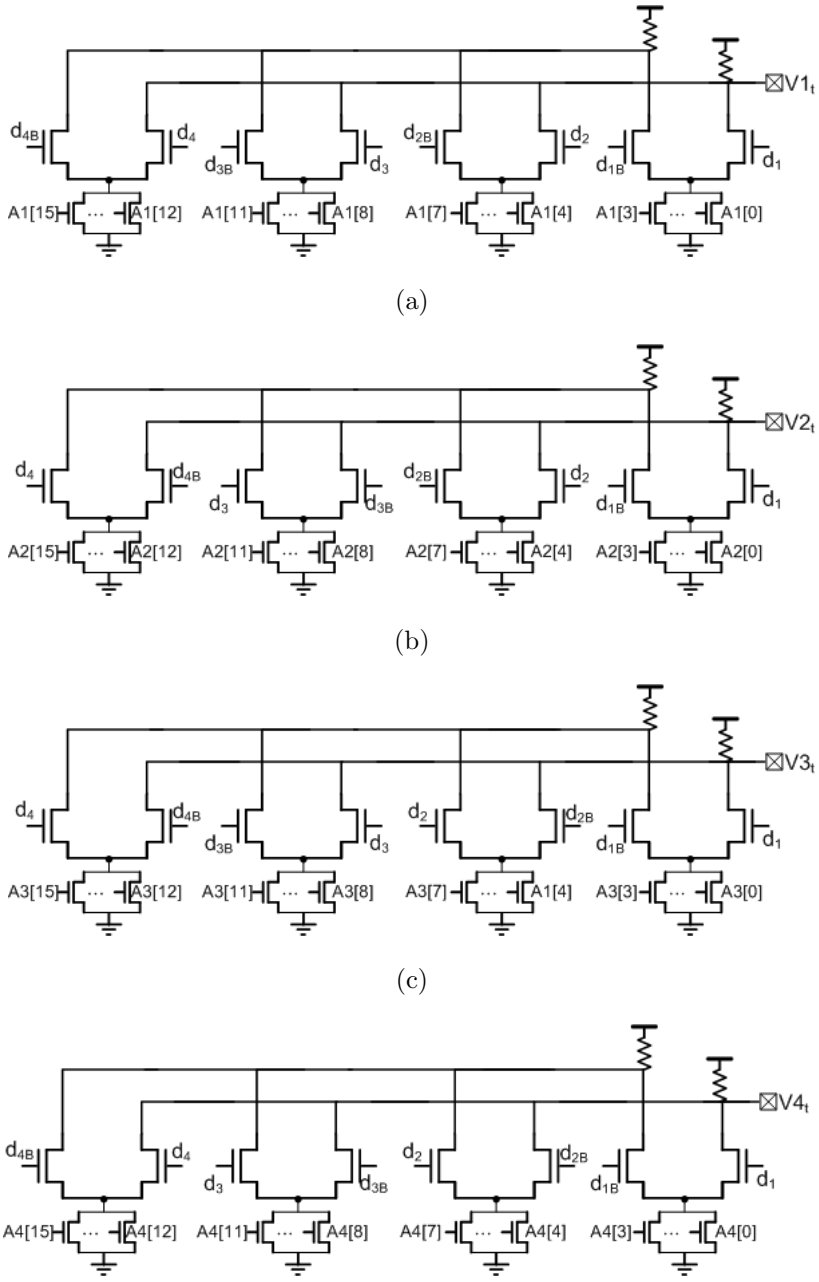


Figure 4.5: Four transmitted outputs of main drivers in a multimode transmitter: (a) $V1_t = d_1 + d_2 + d_3 + d_4$, (b) $V2_t = d_1 + d_2 - d_3 - d_4$, (c) $V3_t = d_1 - d_2 + d_3 - d_4$, and (d) $V4_t = d_1 - d_2 - d_3 + d_4$

wires by the summed currents based on the four input values as shown in Fig. 4.5.

The current summations at the main driver implement the encoder function of linear combination with four input sequence. Tail current control of the main driver is equivalent to the magnitude control of encoder coefficients, which can be changed by control registers. This structure is the extended version of pre-emphasis or digital-to-analog (DAC) circuit topology. By controlling encoder coefficients, we could adapt TX to manufacturing variations of channel geometry such as misalignments between signal traces. To properly connect parallel data to main drivers, we need to implement pre-drivers. The pre-drivers reduce the signal swing of the PRBS outputs for high-speed transition at the main-driver inputs and minimize the kickback noise. Fig. 4.6

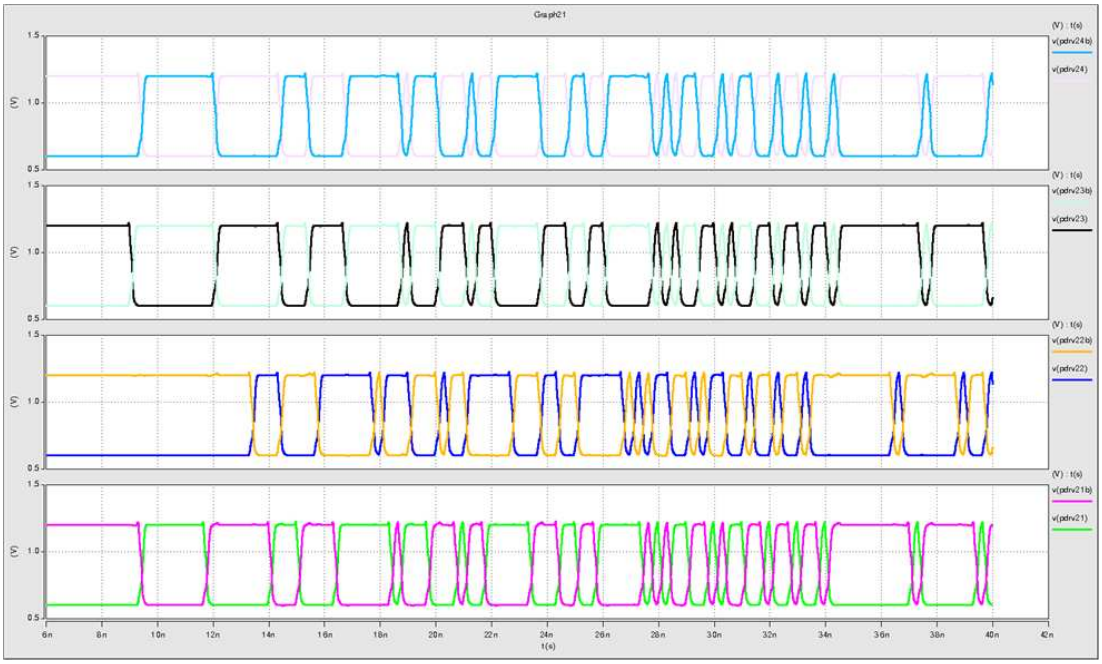


Figure 4.6: Simulated waveforms of transmitter pre-driver outputs

represents the four pair of differential pre-driver outputs showing the reduced voltage swings from 1.2V to 0.6V.

To create a specific length of a pseudo-random sequence generator, we need to know a primitive polynomial corresponding to that length. According to appendix of Lin and Costello [36], we could find a table showing the collection of the primitive

polynomials. From there, the primitive polynomial of $p(x) = x^{10} + x^3 + 1$ is selected to generate the length of $2^{10} - 1$. To implement this polynomial, there is two schemes called many-to-one and one-to-many scheme, depending on how exclusive-OR gates are designed. One-to-many scheme selected in this design implements exclusive-OR gates with the minimum number of inputs, thereby minimizing Q-to-D delays to the flip-flops. Ten flip-flops are sequentially placed to make a shift register.

The flip-flops employed in PRBS call for set/reset options to seed the four PRBS with different values and the balanced Q and Qb outputs for main drivers. By considering the flip-flop requirements mentioned above, the flip-flop topology in [11] shown in Fig. 4.7 was carefully selected.

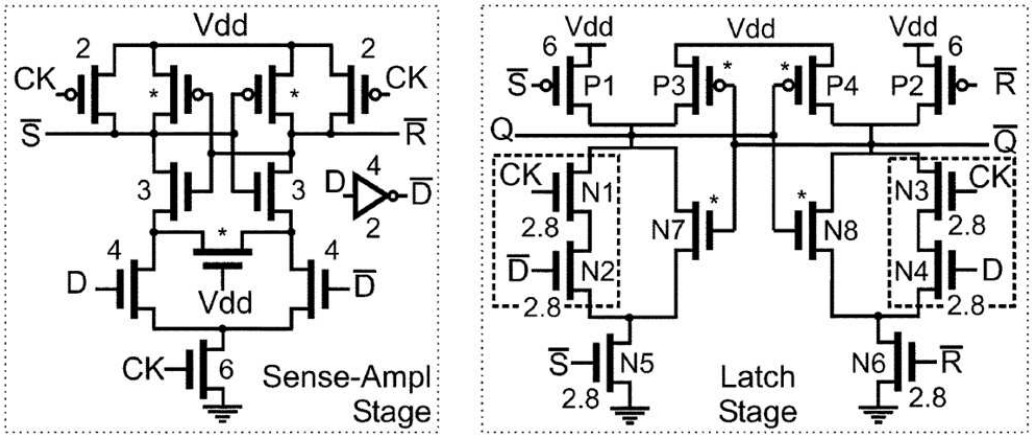


Figure 4.7: Schematic of a designed flip-flop [11]

4.3 Receiver

The receiver (RX) block implemented the decoding operation that converts multimode signals back to binary ones by linear combinations as shown in Fig. 4.8. The receiver is comprised of replicated current mirrors and cascaded differential amplifiers after terminations. At first, the received multi-level current signals are converted into voltages by termination resisters. The termination resistors implemented in this design came from [12]. The active termination consists of three PMOS and a poly

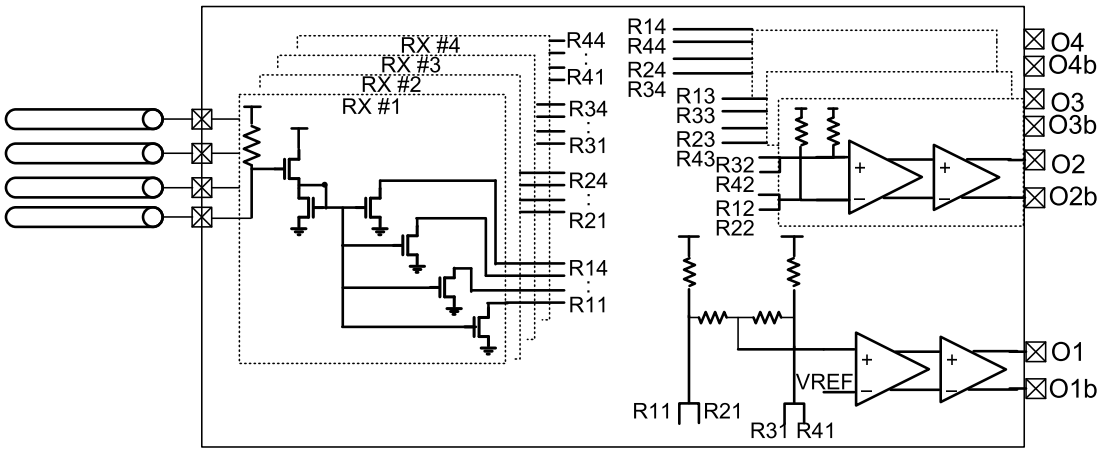


Figure 4.8: Receiver Architecture of multimode signaling

resistor. The parallel-connected PMOS with a poly resistor compensates temperature variation of the poly resistor. As shown in Fig. 4.9, by varying the gate voltage of upper PMOS, the output resistance seen from the pad follows linearly the input voltage variation.

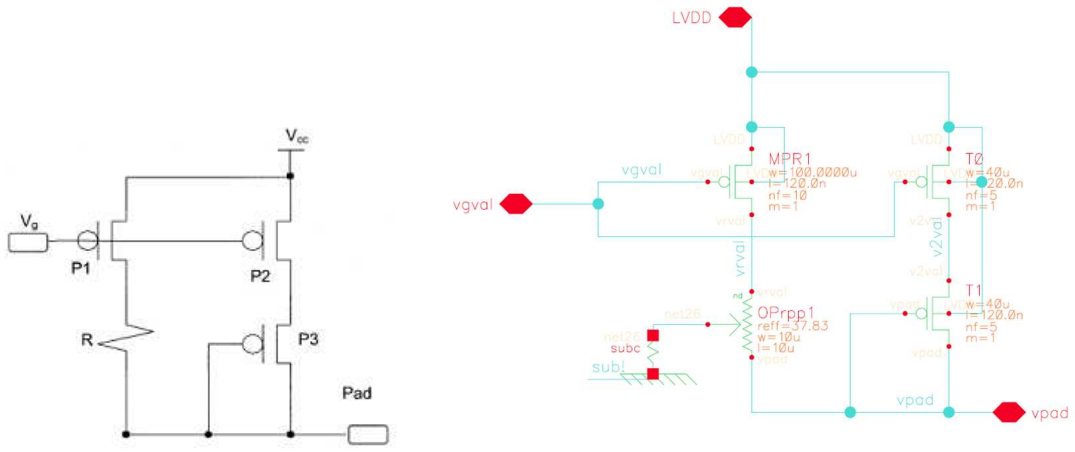


Figure 4.9: On-die active termination [12]

Once the received signals are converted into voltages by on-die active termination, the voltage is converted back to current and mirrored with NMOS for decoding operation. Since the decoding operation needs the replicated inputs, each input is

replicated by current mirrors. For example, the current values at nodes R11, R12, R13, and R14 are the four-replicated currents of the first received signal and the branch currents of R21, R22, R23, and R24 are the replicated currents of the second received one. The decoding operations start with the current summations at the inputs of differential amplifier. For example, R32, R42, R12, and R22 current inputs of differential amplifiers are summed by the resistors, a partial operation of a complete decoding procedure. Then the summed currents are converted into voltages in that voltages can be scaled by varying resistor values, representing decoder coefficients. The decoded signals, O1, O2, O3, and O4 represent PRBS-generated outputs. Since the decoded signal O1 is extracted from the common-mode of all four signals, depending on the amount of the added noise to all four signals, O1 may become very sensitive to the common noise. Fig. 4.10 illustrates a comparison of a decoded waveform (black) with an expected sequence generated from a PRBS at the transmitter.

To manually control encoder/decoder coefficients, four control registers are implemented and programmed sequencially in test mode. The control of encoder/decoder coefficients with programmable registers gives us freedom to explore multimode signaling for different interconnect geometries. But as a future work, we need to suggest a coefficients control scheme for handling channel variations.

4.4 Conclusion

This chapter described the design of encoder and decoder for multimode signaling transceiver. For demonstrating the implementation idea of the signaling scheme, the transmitter utilized pre-emphasis circuit topology, a commonly used sub-block in a conventional transmitter. But controlling tail currents would change the linear ranges of inputs, thereby becoming non-linear relationship between tail currents and differential output currents. Probably other circuit topology solves this issue. In the receiver design of multimode signaling, the received signals are first detected as voltages by termination and then converted to currents using current mirrors for

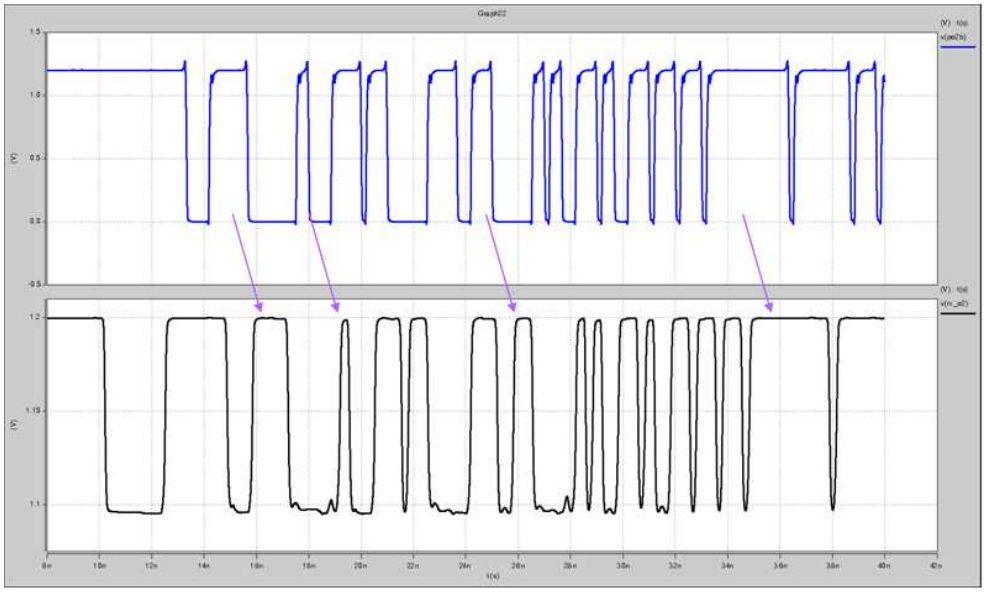


Figure 4.10: Comparison of a decoded waveform(bottom, black color) with a PRBS transmitted sequence(top,blue color)

decoding operation. For better signal quality, we could detect the received signals as a current form by using inductive coupling or active termination.

Chapter 5

Measurements of Multimode Signaling Transceiver

The transmitter and the receiver of multimode signaling were fabricated in IBM 0.13 μm CMOS technology. The aim of this design was to demonstrate the feasibility of this signaling scheme with four-parallel stripline interconnect. Four wires are chosen for the reasonable amount of design and test complexity.

5.1 Test Chip

After deciding transistor parameters and performing simulations in schematic level combined with the channel model, the chip was manually designed by full-custom layout as shown in Fig. 5.1. Decoupling capacitances and ESD diodes were carefully added to make a reliable test chip. Fig. 5.2 represents the microphotograph of LFSR, a transmitter, and a receiver of multimode signaling. T1-T4 denotes the TX outputs and R1-R4 are the RX inputs. White-square pads located inside the die are on-die probing pads. The pads on the perimeter of the die are the bonding pads directly bonded to PCB because we didn't package this die. To reflect the packaging effect, the pads are bonded with the minimum wirebond length being greater than 2 mm. Fig. 5.3 describes the microphotograph of the fabricated transmitter and receiver.

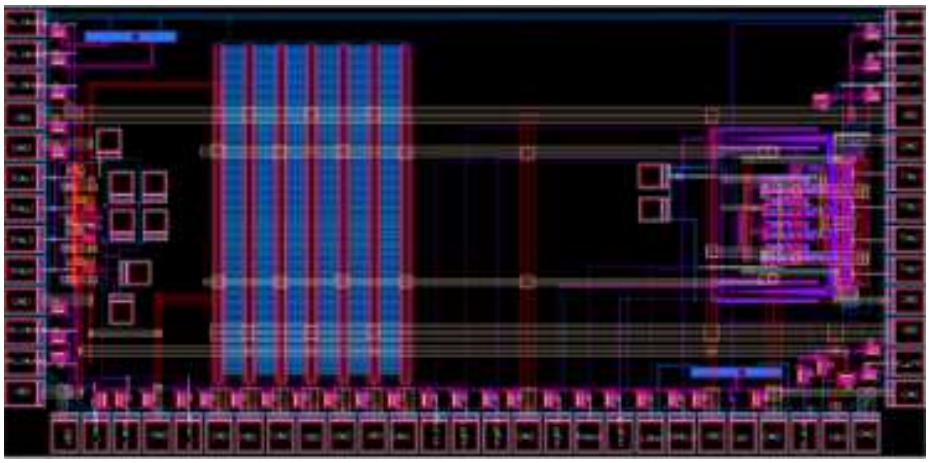


Figure 5.1: Chip layout of transmitter(right side) and receiver(left side)

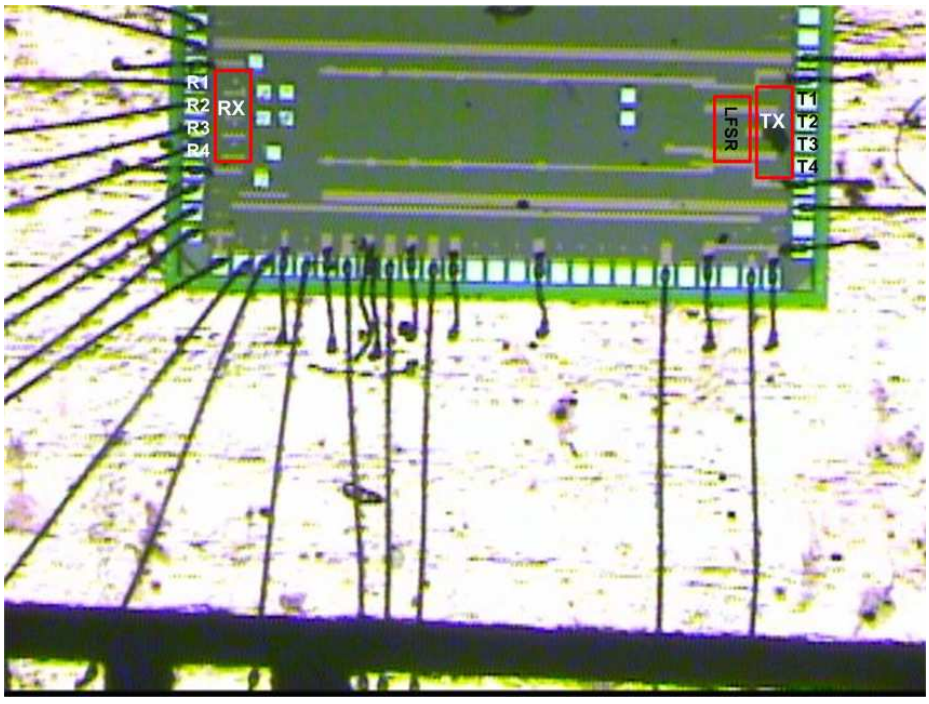
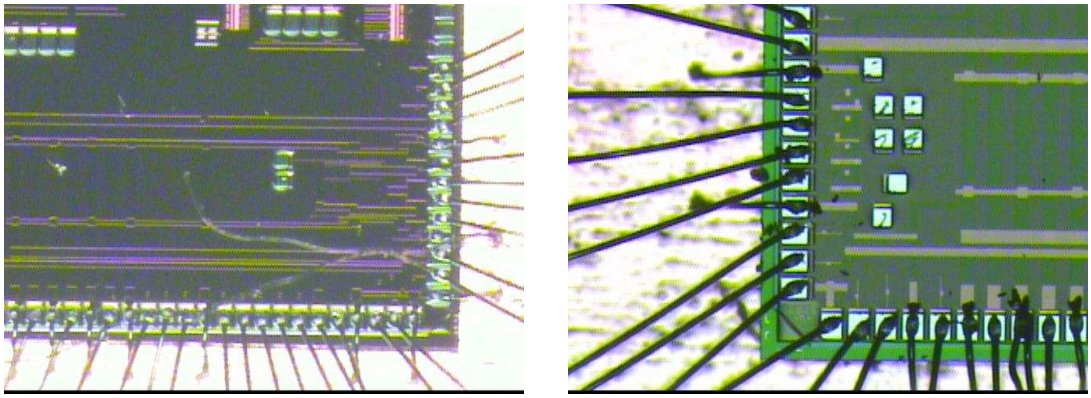


Figure 5.2: microphotograph of the fabricated IBM 0.13 μm CMOS test chip (3 mm $\times$ 1.5 mm)

5.2 Printed Circuit Board for Test Chip

The printed circuit board was designed to attach the die of transceiver. Fig. 5.4 represents the annotated drawn PCB, where external clock is connected with SMA



(a) (b)

Figure 5.3: Chip microphotograph: (a) transmitter, (b) receiver

connector. Fig. 5.5 is the photo of the manufactured PCB. Both die locations are surrounded by decoupling capacitors for reducing power-ground noise when the transceiver is activating. The jumper switches located in the left and the upper middle of the PCB are used to control the transceiver manually. For example, on-die termination resistors located at the inputs of the receiver are controlled by external analog voltage signal connected from a jumper. Some of jumpers are receiving reset/set signals from an equipment(HFS1000) to initialize LFSR. Fig. 5.6 presents the PCB with wire-bonded dies and soldered components. After attaching the die substrate to PCB reference ground with conductive epoxy, the test chips are directly wirebonded to the test board with aluminum wire.

One crucial point when connecting external clock is a termination resistor. Because the location of the termination resistor for the external clock coming from SMA was not assigned when designing PCB, the small size (0402), 50 Ω resistor was placed close to the die and the external clock trace and connected by wire bonding, thankfully. Since the external clock is directly operating PRBS, signal integrity of the clock decides the reliable circuit operation.

Each trace of four-wire bundle was designed with 5 *mil* width and spacing because of the manufacturing limitation of the selected low-cost PCB manufacturer. The

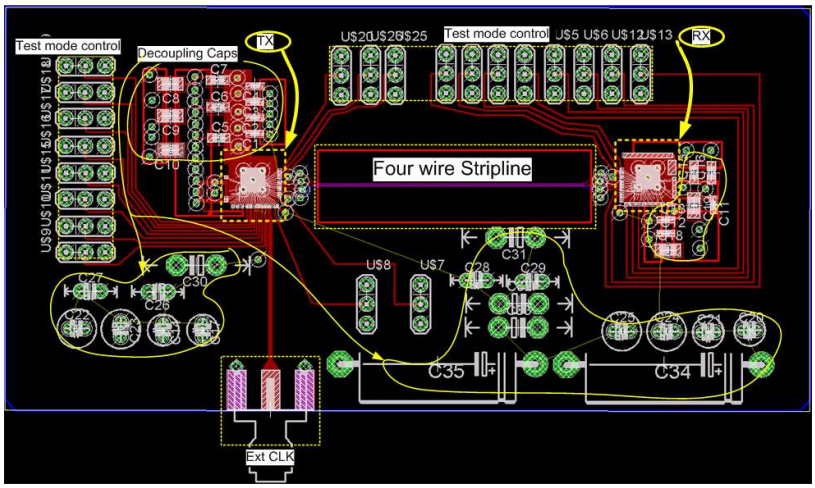


Figure 5.4: Drawn Printed Circuit Board for testing Multimode Signaling Transceiver with four stripline interconnect

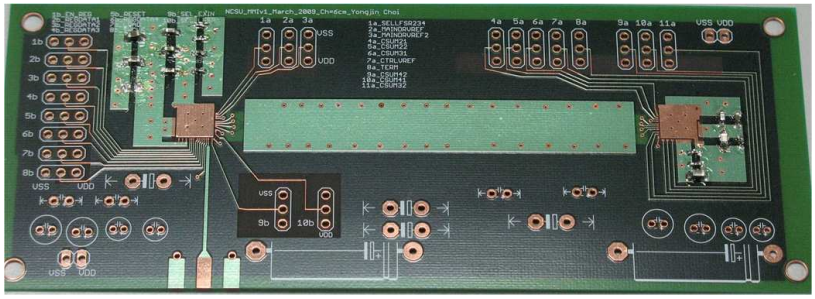


Figure 5.5: Manufactured Printed Circuit Board

measured geometries of traces have 20 % variations as shown in Fig. 5.7(a). Because of the manufactured variations, the measured line impedance performed by TDR shows 67 Ω instead of 50 Ω as illustrated in Fig. 5.7(b). Therefore, the transceiver need to have a training mode for adjusting the codec coefficients in the later version.

5.3 Measurement Results

The purpose of this test was to measure the decoded eye-diagrams of multimode signals transmitted through four-parallel stripline bundle. Illustrated in Fig. 5.8,

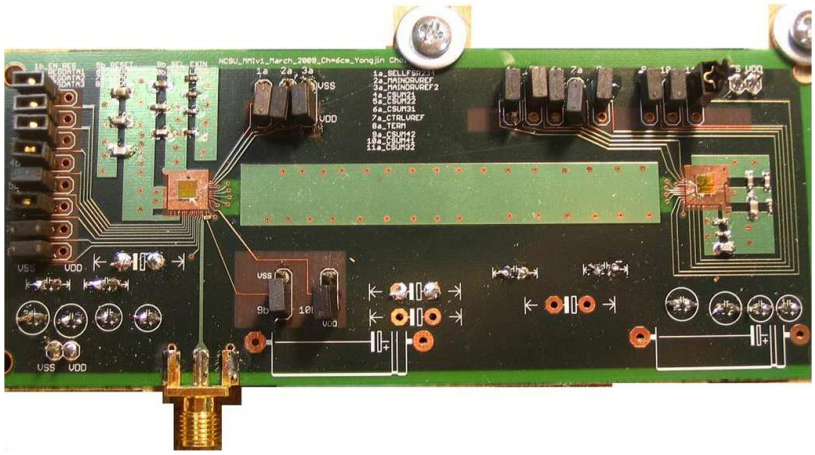


Figure 5.6: Printed Circuit Board with wire-bonded dies and soldered components

a high-impedance prober landed on an on-die pad to detect eye-diagrams. Three, external voltage suppliers gives the analog control capability to sweep the termination resistance values.

Fig. 5.9 presents the measured eye-diagrams with the prober. The input signals to the receiver have the five-level waveforms as shown in Fig. 5.9(a) at 2.4 Gbps/channel. We can interpret that the eye-diagram is distorted by crosstalk and reflection. The decoded eye-diagram at 2.4 Gbps is described in Fig. 5.9(b). The jitter of the eye is relatively small compared to the received jitter. Therefore, we could conclude that the transceiver is properly designed for this example interconnect structure.

The chip measurement summary is presented in Table 5.1. The power consumption of TX is 45 mW/ch $\approx$ 19 mW/Gbps/ch, the power consumption of RX is 18 mW/ch $\approx$ 7.5 mW/Gbps/ch, and the power consumption of LFSR is 18 mW/ch. Since current mode summations for codec operation are the major factor of power consumption, we could reduce the power consumption by using the different circuit topology such as voltage domain operation. As the interconnect density of multimode signaling is two times of the differential signaling, the effective power consumptions can be reduced by a half when considering the horizontal routing dimension. Therefore, the effective power consumption of TX is about 9.5 mW/Gbps/ch per inverse

horizontal dimension. By the same way, the effective power consumption of RX is about 3.8 mW/Gbps/ch per inverse horizontal dimension.

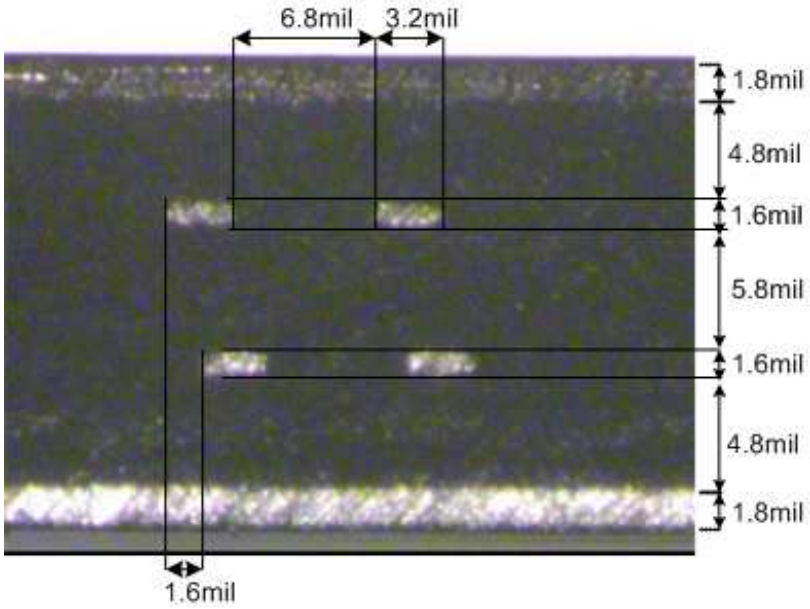
Fig. 5.10 represents the measured bit-error-rate (BER), 10^{-8} of multimode signaling at 1 Gbps. Because of unbalanced probing to the decoded-differential outputs with a high-impedance prober, we could not achieve the better BER around 10^{-12}. If we designed GSSG or GSG probing pads at the RX decoded outputs, we could easily measure BER of 10^{-12} with multimode transceiver.

5.4 Conclusion

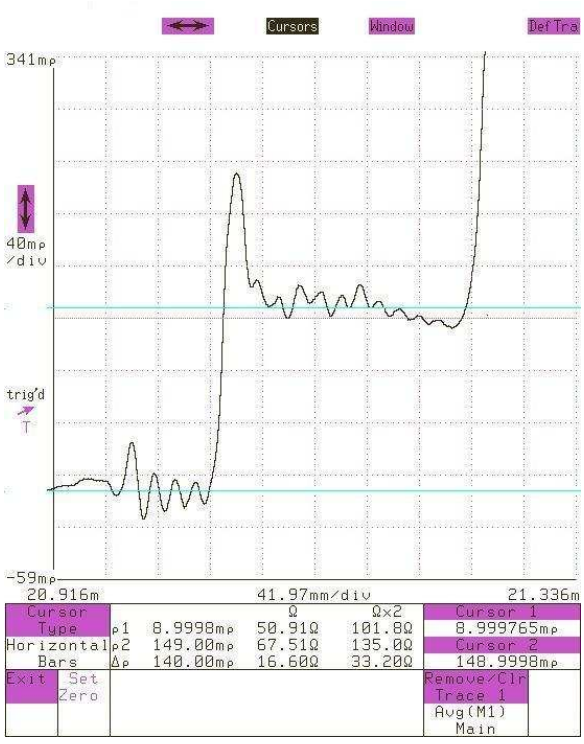
This chapter described implementation procedures of a prototype chip and test PCB for multimode signaling. The manufactured test board had a significant design variation in the signal traces. In addition, the connection of the multi-Gbps external clock into the chip needed to consider transmission effect, that is reflection to suppress by termination. The measured eye-diagrams indicate that the suggested signaling scheme would be a viable alternative in a dense interconnect.

Table 5.1: Chip Measurement Summary

Process	0.13 μm IBM CMOS
Supply Voltage	1.3 V
Data Rate	2.4 Gbps / ch
Active Area	TX: 80 x 100 μm^2/ch RX:100 x 30 μm^2/ch LFSR: 160 x 60 μm^2/ch
Power Consumption	TX: 45 mW/ch $\approx$ 19 mW/Gbps/ch RX: 18 mW/ch $\approx$ 7.5 mW/Gbps/ch LFSR: 18 mW/ch



(a)



(b)

Figure 5.7: Manufacturing variations of traces: (a) measured cross-section, (b) measured trace impedances (67 Ω)

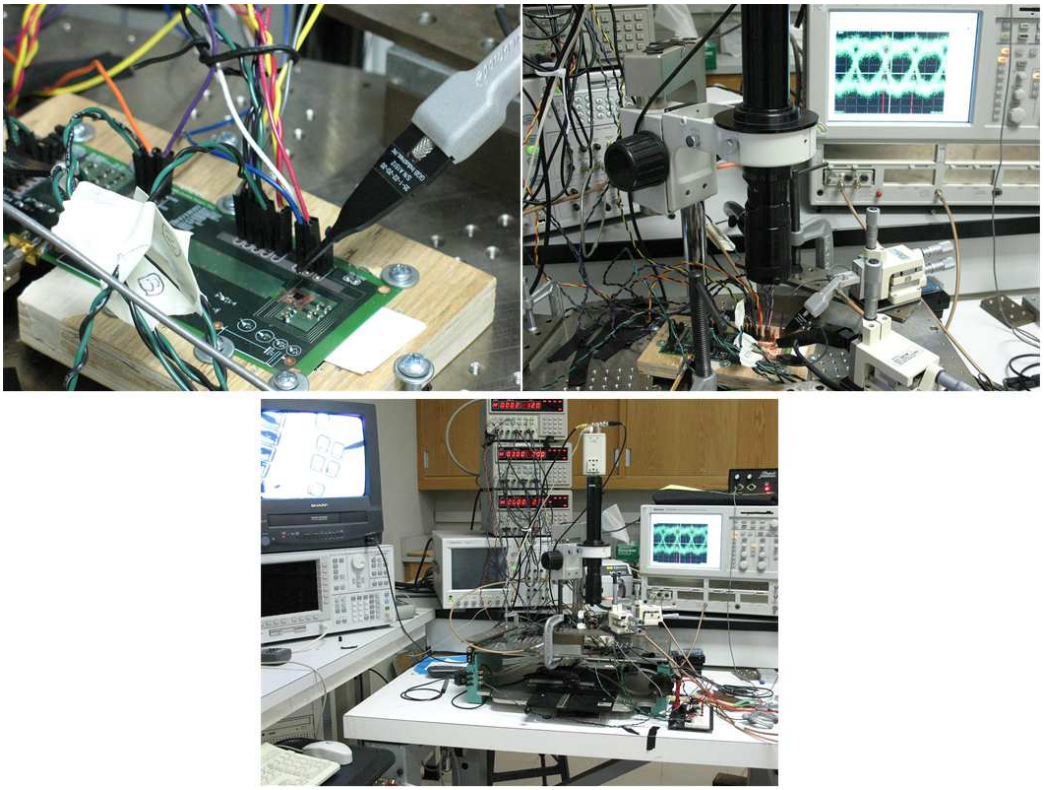
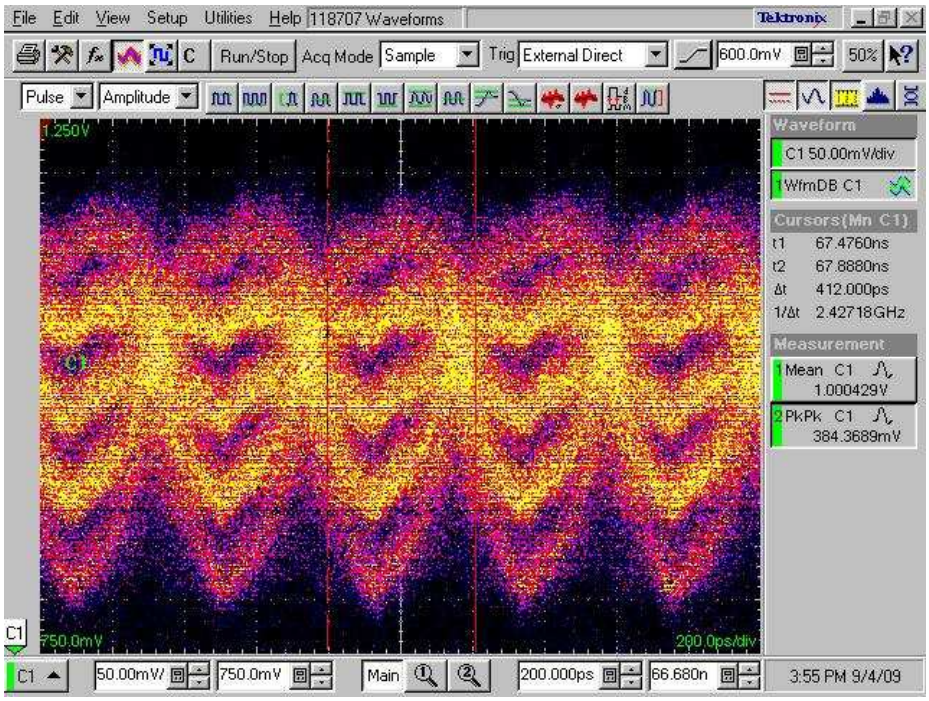
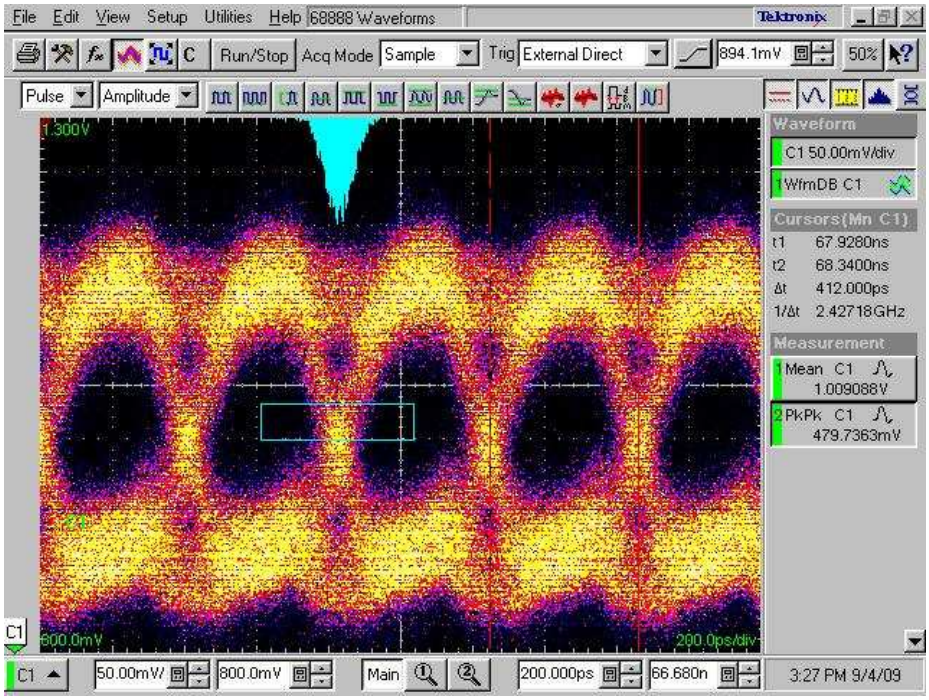


Figure 5.8: Measurement Setup for probing the decoded eye-diagrams



(a)



(b)

Figure 5.9: 2.4 Gbps/line at RX, line length=6cm: (a) Eye-diagram of receiver input, (b) Eye-diagram of decoded receiver output

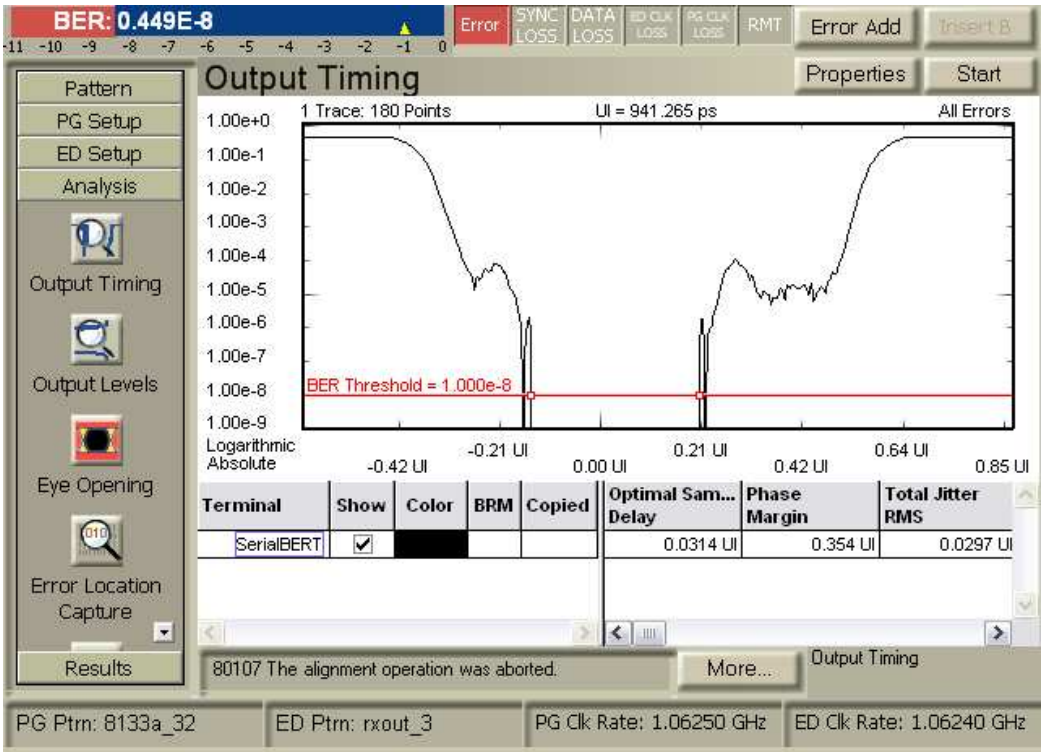


Figure 5.10: Bit-Error-Rate of multimode transceiver at 1 Gbps

Chapter 6

Conclusion and Future Work

6.1 Conclusion

The objective of this research was to determine the scaling advantages that can be achieved using *multimode signaling* and to demonstrate those advantages. As an alternative signaling solution for smaller packages and low-cost platforms in conjunction with an aggressive scaling of the I/O bandwidth, the feasibility of multimode signaling has been investigated.

First of all, the behavior of multiline interconnect was described with the well-established multiconductor theory. The decoupled wave equations converted from coupled multiline wave equations, tells us that parallel signals could be sent through eigenmodes of the corresponding multiline interconnect. The eigenvectors was derived from the product of line inductance and capacitance matrices, provided that the attenuation is ignored to simplify the calculation. The derived eigenvectors functioning as an encoder were linearly combined with parallel data to produce the transmitted signals. The comparison of with and without codec case with the example illustrated the advantage of multimode signaling. The frequency-domain analysis of the multiline with codec indicated that the inter-wire response can be reduced by the codec.

To investigate the effectiveness of this scheme as a dense interconnect solution, we analyzed inter-bundle crosstalk as a function of bundle-to-bundle spacing to guarantee

a high-density interconnect as compared to conventional single-ended and differential signaling. The simulated small crosstalk between bundles with varying a bundle spacing, demonstrated the promise of multimode signaling for high-density interconnects. The density increase example by multimode interconnect was illustrated in Fig. 1.1 when sending four signals. The horizontal density benefit is likely more than two times the one of the conventional differential pairs. Since the inter-bundle crosstalk is likely insensitive to the bundle spacing, the increase of interconnect density could be guaranteed when employing more than two bundles.

To demonstrate the signaling scheme, a multimode transceiver with 0.13 μm CMOS process was implemented. The interconnect bundle consisted of a four-parallel, 6 cm, FR-4 stripline structure with two pairs of wires stacked inside two reference planes. The measured eye-diagrams of a prototype chip demonstrated the speed of 2.4 Gbps per wire at the decoded receiver outputs. Even if the manufactured bundle had various non-ideal conditions such as length mismatch and discontinuities, the signaling scheme was likely to be insensitive from the effects. This implementation example provided insights into the design of multimode signaling transceiver incorporated with the linear combinations of eigenmodes and the reverse operation.

6.2 Future Work

The accomplished outcomes of this research lead us to explore a sequence of the related research topics. Some of them are listed in the following.

- Design low-power, high speed multimode receiver:
  In this research, the receiver was implemented with the replicated current mirrors for decoding operations once the received multi-level signals are converted into voltage mode signals and then back to currents by mirrors. By converting the received signals repeatedly, non-linearity of circuits distorts the signals. Additionally, the current mirror topology limits the high speed operation of the receiver due to the parasitic capacitances in the mirrors. As an alternative circuit topologies, we can consider current mode receivers or inductive receivers. In the

current mode receiver, the received signals are terminated by the on-resistances of the transistors instead of pure poly resistances. That gives us design freedom because the induced signals in the transistors can be easily replicated to the next steps with the reduced distortion. As a different conceptual approach, we may sense the received signals by inductive coupling such as wire-bonding or transformer type coupling called inductive receivers.

- Adjust parallel length mismatch with circuit technique:
  An inherent problem with parallel multiline interconnect is that matching the line lengths is almost impossible because of the limited routing area in a PCB or a package substrate. To overcome this issue with circuit technique, we need to include a time delay block per line that works as adjusting length mismatch by delaying the received signals. Since the length mismatch can be detected before normal operation, we could set the amount of delays per line by comparing test mode signals. Detecting length mismatch by using test mode signals and then controlling the delay cells with the extracted information will be the steps to be performed. When designing delay cells, we need to consider the output linearity of the delay cell with respect to inputs because the received signals are multi-level signals. If we could incorporate the delay cells into the receiver equalizer, that may simplify the receiver design.

- Equalizer Design :
  The multimode transceiver presented in this research was for the chip-to-chip interconnect in that the length is about less than l0 cm and thus attenuation was ignored. But when applying this transceiver design to a longer length than 10 cm, we need to consider an equalizer incorporated into the transceiver because the attenuation is no longer ignored. Since the transmitted waveform shapes are determined by the encoder and parallel data and the relative waveform relationships between lines are making crosstalk resistant, the equalizer would be located after the encoder to guarantee multimode waveform shapes. As an alternative approach, the fractional equalizer can be employed because

it controls signals within a bit duration, thus keeping the overall transmitted waveform shapes.

- Adapting Encoder / Decoder coefficients:
  Exploring the training schemes to adaptively adjust the codec coefficients: Due to the non-ideal channel effects such as via and connectors, the codec coefficients need to be adjusted whenever the channel condition is changed. With the known transmitted signals through multi-lines, we may estimate the channel variation, then relate the variation to the coefficients during the training mode.

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