

Interfacial strain-induced self-organization in semiconductor dielectric gate stacks. II. Strain-relief at internal dielectric interfaces between SiO₂ and alternative gate dielectrics

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(Received 18 January 2004; accepted 26 April 2004; published 19 August 2004)

This article applies bond constraint theory to develop a scaling relationship for the density of bond-strain induced defects such as fixed charge localized at internal dielectric interfaces. The magnitude of this charge scales with the square of the difference between the average number of bonds/atom of the interface constituents such as SiO₂ and Si₃N₄, or ZrO₂ or HfO₂. Consistent with equilibrium phase diagrams of the SiO₂-Zr(Hf)O₂ binary alloy systems, interfaces between: (i) SiO₂ and (ii) ZrO₂, HfO₂, and Zr and Hf silicate alloys exhibit a strain-induced self-organization after annealing to temperatures of ~600–800 °C producing a diphasic interfacial transition region comprised of ZrO₂ encapsulated by SiO₂. This reduces fixed charge by more than 1 order of magnitude. In marked contrast, and also consistent with differences in their equilibrium phase diagrams, strain-induced self-organization does not occur for temperatures up to at least 1000 °C at interfaces between: (i) SiO₂ and Al₂O₃ and (ii) SiO₂ and Si oxynitride alloys due to binary alloy compound phases with congruent melting points that prevent formation of the diphasic interfacial transition region comprised of the end member oxide dielectrics. © 2004 American Vacuum Society. [DOI: 10.1116/1.1771675]

I. INTRODUCTION

This article extends the approach of Ref. 1 to internal interfaces between dielectric films with markedly different local bonding arrangements, including interfaces between SiO₂ and: (i) Si₃N₄, and Si oxynitride alloys (Si₃N₄)_x(SiO₂)_{1-x}, (ii) Al₂O₃, and (iii) transition metal (TM) and lanthanide rare earth (RE) atom oxides, and silicate alloys such as (Zr(Hf)O₂)_x(SiO₂)_{1-x}. These interfaces are important for device scaling as thermally grown Si-SiO₂ gate stacks are replaced by stacks that include ultrathin SiO₂ interfacial layers and deposited high-*K* alternative gate dielectrics.²⁻⁴ The arguments for these replacements have been presented in Ref. 1 as well as in other papers dealing with: (i) Si oxynitride alloys with relative dielectric constants *K* between 5 and 7⁵ and (ii) high-*K* dielectrics where the dielectric constants are increased to at least 20–25.^{2-4,6,7} It will be shown that as *K* is increased that the average number of bonds/atom N_{av} and the average number of bonding constraints/atom C_{av} in these dielectrics increase as well. Differences between the N_{av} in SiO₂, and these replacement dielectrics results in steps N_{av} and C_{av} at internal dielectric interfaces producing strain-induced localized defect densities of fixed charge in excess of 10¹¹ cm⁻².⁸ Localization of these defects at the internal dielectric interfaces has been established by a linear scaling of flatband voltage shifts as

function of dielectric layer thickness, as for example in metal-oxide-semiconductor (MOS) capacitors with stacked SiO₂-Al₂O₃ gate dielectrics.⁹

II. BONDING IN ALTERNATIVE GATE DIELECTRICS

It has been shown in Ref. 7 that noncrystalline gate dielectric materials can be organized into three groups with different amorphous morphologies: (i) covalent random networks (CRNs) exemplified by SiO₂ in which each of the constituent atoms bonds according its normal chemical valence; (ii) modified random covalent networks (MCRNs) in which the network structure is *disrupted* and *modified* by metal ions which display a coordination characteristic of their normal ionic bonding coordination, typically six- to eightfold in elemental oxides and in binary oxide alloys; and finally (iii) random close packed (RCP) ionic structures in which the packing is nondirectional, and is determined primarily by relative ion size. The average coordination of the O atoms is increased from twofold in the CRNs, to approximately threefold in the MCRNs, and then at least fourfold in the RCP structures. This article focuses on CRN and MCRN dielectrics, where a correlation is established in Table I between the average number of N_{av} and *K*. The latter is generally obtained from a combination of capacitance and film thickness measurements, and the original sources of quoted

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TABLE I. Values of: (i) the average number of bonds/atom N_{av} , (ii) the average O atom coordination n_{Ox} , (iii) the Pauling bond ionicity I_b , and (iv) the relative dielectric constant K for representative alternative gate dielectrics.^{2,5} These have been organized into three groups with different amorphous bonding morphologies: CRN, MCRN, and RCP dielectrics. determined interfacial fixed charge $N_{def,exp}$.

Dielectric	N_{av}	n_{Ox}	$I_b(\pm 0.05)$	$K(\pm 10\%)$
				CRN
SiO ₂	2.67	2	0.45	3.9
Si ₃ N ₄	3.43	—	0.28	7.5
(Si ₃ N ₄) _{0.5} (SiO ₂) _{0.5}	3.05	2	0.37	5.6
				MCRN
Al ₂ O ₃	3.60	3	0.57	9.0
(Zr(Hf)O ₂) _{0.25} (SiO ₂) _{0.75}	3.34	2.25	0.52	8.0
(Zr(Hf)O ₂) _{0.5} (SiO ₂) _{0.5}	4.0	3.0	0.59	12.0
(Zr(Hf)O ₂) _{0.25} (Al ₂ O ₃) _{0.75}	4.03	3.25	0.60	13
(Zr(Hf)O ₂) _{0.5} (Al ₂ O ₃) _{0.5}	4.47	3.5	0.63	15
(Y(La) ₂ O ₃) _{0.5} (SiO ₂) _{0.5}	3.74	3	0.6	13
				RCP
Zr(Hf)O ₂	5.33	4	0.7	22
Y(La) ₂ O ₃	4.80	4	0.72	22

values have been included in the table caption for the compounds, and have been obtained by linear extrapolations for the alloys.

Table I is based in large part on the results presented in Ref. 7, and the reader is referred to that article for details regarding the bond ionicity determinations. Table I includes: (i) the average number of bonds/atom N_{av} ; (ii) the average O atom coordination n_{Ox} ; (iii) the Pauling bond ionicity I_b ; and (iv) the relative dielectric constant K . The plot in Fig. 1, based on the data in Table I, establishes a linear correlation between K and N_{av} ; the correlation between K and I_b is much poorer and is not shown.

The table and plot in Fig. 1 include SiO₂, Si₃N₄, a representative Si oxynitride alloy, (Si₃N₄)_{0.5}(SiO₂)_{0.5}, as well as several alternative high- K dielectrics including Al₂O₃, and TM and lanthanide RE atom oxides, and their respective

silicate and aluminate alloys. Based on results presented in Refs. 8 and 10, and summarized below, bond strain in CRN and MCRN dielectrics is proportional to N_{av} normalized to the value of N_{av}^* of a reference, *ideal* dielectric in which the bond strain is minimal, as for example SiO₂, where defect levels are typically $1-5 \times 10^{10} \text{ cm}^{-2}$.⁸⁻¹¹ This defect-scaling relationship based on differences in N_{av} is extended in this article to interfaces between SiO₂ and alternative gate dielectrics in the stacked heterostructures shown schematically in Fig. 2. One focal point of this article deals with strain-induced defects localized at the internal dielectric interfaces of these heterostructures. A second discusses aspects of equilibrium binary oxide phase diagrams that have been correlated with strain-driven interfacial self-organizations during high temperature annealing in inert ambients.¹ Self-organization has been demonstrated as a one crucial mechanism for reducing interfacial defect densities, and is thus an

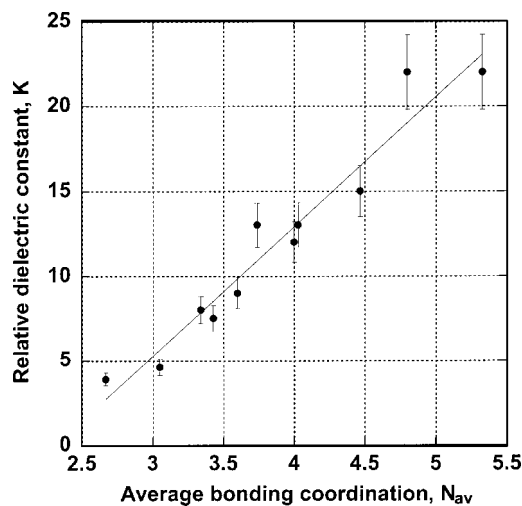


FIG. 1. Relative dielectric constant K as a function of the average number of bonds/atom N_{av} for representative dielectrics, including SiO₂, Si₃N₄, and transition metal and rare earth atom silicates, aluminates, and oxides, in order of increasing N_{av} . The points in this plot are taken from Table I.

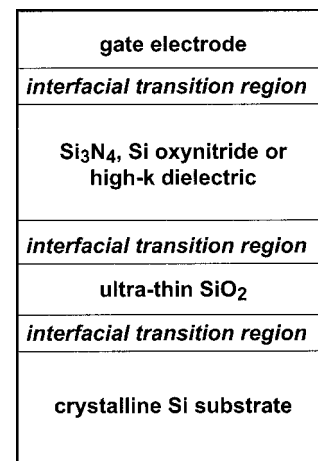


FIG. 2. Schematic representation of a stacked gate dielectric including an SiO₂ interfacial layer, a high- K dielectric, and a metal gate. The interfaces between the: (i) Si substrate and interfacial SiO₂ layer, (ii) SiO₂ and high- K dielectric, and (iii) high- K dielectric and metal gate are indicated.

TABLE II. Values of N_{av} and I_b for representative dielectrics, and defects at interfaces between these dielectrics and SiO₂. The table also includes an entry for the Si–SiO₂ interface where the defects are the density of Si dangling bonds prior to termination of these defects with hydrogen.

Dielectric	N_{av}	I_b	$N_{def,exp}$ (10^{12} cm^{-2}) $\pm 10\%$
		CRN	
Si ₃ N ₄	3.43	0.27	0.75
(Si ₃ N ₄) _{0.5} (SiO ₂) _{0.5}	3.05	0.38	0.20
		MCRN	
Al ₂ O ₃ interface sixfold Al ³⁺	4.80	0.59	6
(ZrO ₂) _{0.32} (SiO ₂) _{0.68}	3.55	0.53	1.3
		RCP	
Zr(Hf)O ₂ *	4.67	2.97	4
		The Si–SiO ₂ interface	
Si	4.00	0.0	2

important factor for the identification of high- K alternative dielectrics that have the potential to meet many of the International Technology Roadmap for Semiconductors (ITRS) scaling metrics required for advanced bulk complementary MOS (CMOS) devices.¹²

III. DEFECTS AT INTERNAL DIELECTRIC INTERFACES

Experiments have revealed significant densities of fixed charge localized at internal interfaces between SiO₂ and alternative gate dielectrics in stacked structures.^{1–4, 9–11} These results are summarized in Table II. The densities of fixed charge $N_{def,exp}$ in Table II have been determined from room-temperature capacitance–voltage (C – V) measurements using conventional techniques such as plotting the flatband voltage V_{fb} as a function of the effective oxide thickness (EOT) contribution from the alternative dielectric interface constituent as shown in Fig. 2. Additional contributions to systematic shifts of V_{fb} as a function of EOT can arise from the filling of interface traps D_{it} , and from charge injection Q_{inj} , as detected by hysteresis.^{2,9} The values in Table II for $N_{def,exp}$ may also include contributions from D_{it} and Q_{inj} ; however, analyses of C – V data on p - and n -type substrates as a function of temperature have demonstrated that the values of D_{it} and Q_{inj} that have been included in Table II are typically 1 order of magnitude smaller than the fixed charge Q_f , so that $Q_f \approx N_{def,exp}$.

IV. APPLICATION OF BOND CONSTRAINT THEORY (BCT) TO INTERNAL DIELECTRIC INTERFACES

A. BCT scaling

In network amorphous solids the bonding coordinations m of the constituent atoms are typically 2, 3, and 4, and the local bonding arrangements are nonplanar.^{13,14} The average

number of bond-stretching and bond-bending constraints/atom C_{av} in these networks is proportional to N_{av} , and is given by

$$C_{av} = 2.5N_{av} - 3. \quad (1)$$

C_{av} is also proportional to N_{av} when the bonding is planar at one of the threefold-coordinated bonding sites as at the N-atom site in Si₃N₄, and is given as

$$C_{av} = 2.5N_{av} - 3 - n/N_{atom}, \quad (2)$$

where n is the number of atoms with a planar bonding arrangement (four in Si₃N₄) and N is the total number of atoms in the chemical formula representation (seven for Si₃N₄).

The condition for an ideal strain-free CRN is that C_{av} be equal to the network dimensionality d , which is equal to three for all the dielectrics addressed in this article. This condition for $C_{av}=3$, corresponds to a value of 2.4 for N_{av} , when the bonding arrangements are nonplanar, and this accounts for the excellent glass formation observed for chalcogenide amorphous semiconductors such as As₂S₃ and As₂Se₃, and chalcogenide alloys such as Ge_{0.2}S_{0.8} and Ge_{0.2}Se_{0.8}.^{13,14} $N_{av}=2.67$ for SiO₂ so that substituting into Eq. (1) yields a value of $C_{av}=3.67$, greater than the network dimensionality of 3.0. This suggests that SiO₂ should be overconstrained, and therefore have a significant number of intrinsic bonding defects. However, bonding directionality at oxygen is weakened by its lone pairs (two if fully ionic), and this weakening is reflected by the broad Si–O–Si bond-angle distribution, $\sim 150^\circ \pm 20^\circ$.¹⁵ Thus the O-atom bond-bending force constant is small, and one bond-bending constraint associated with the Si–O–Si bonding arrangement is broken.^{15,16} The removal of one bonding constraint per O atom reduces the C_{av} for SiO₂ to 3.0, thereby accounting for its outstanding glass formation properties, and its low density of electronically active defects, $\sim 1.5 \times 10^{10} \text{ cm}^{-2}$ or equivalently $0.4\text{--}1.1 \times 10^{16} \text{ cm}^{-3}$. We adopt the working hypothesis that all bond bending constraints are to be counted

equally. This makes SiO₂ an excellent reference material to use in scaling relationships. For clarity, we rescale its N_{av} , as if all its stretching and bending constraints were intact, by setting the value of N_{av}^* equal to 2.4, thereby reflecting the broken bond-bending constraint at the oxygen atoms.

Constraint theory provides a remarkably accurate description of network stress in nonideal CRNs in which $C_{av} > 3$, and its consequences with respect to defect formation.^{8,10} The application of constraint theory to bonding defects is based on the simple idea that the bonding forces in a network amorphous solid can be arranged in a hierarchy from stronger-stretching to weaker-bending valence forces. As shown above in Eqs. (1) and (2), the constraining effects of these forces are a linear function of the average coordination number N_{av} . For overconstrained networks such as Si₃N₄ for which $N_{av} = 3.43$, Si-atom and N-atom bond-stretching constraints are stronger than the respective Si- and N-atom bond-bending constraints, so that strain energy accumulates in the configuration space defined by the bending constraints. The most significant accumulation of strain is at the atomic site with the lower coordination number, in this instance N , which is partially ionic and also has lone pair electrons that weaken the bond directionality. Since the bonding geometry of the threefold coordinated nitrogen atoms is planar, the value of C_{av} as determined from Eq. (5) is 5.0, predicting bonding distortions in the form of bond angle strain at the N-atom bonding sites. This means that the average Si–N–Si bond angle θ is distorted from the ideal local value of 120° by an amount $\delta\theta$, which we take to be proportional to the difference between N_{av} in the nonideal strained network and $N_{av}^* = 2.4$ of an ideal, strain-free network

$$\delta\theta \propto [N_{av} - N_{av}^*]. \tag{3}$$

It is further assumed that defect density is associated with dangling bonds, which are on the Si and N atoms. These dangling bonds are the residue of broken and only partially reconstructed bonds that relieve local strain buildup. As such this density is expected to be proportional to the primarily harmonic strain energy,^{8,10} which is proportional to $[\delta\theta]^2$. Therefore, the density of defects D in a constrained network is expected to obey the following scaling relationship:

$$D \propto [N_{av} - N_{av}^*]^2. \tag{4}$$

A similar scaling relationship is assumed at the internal interface between two different dielectrics. The density of interface defects, designated as N_{def} , is assumed to scale as the square of the *difference* in the average number of bonds/atom of the two dielectrics A and B that define the interface

$$N_{def} \propto [N_{av}(A) - N_{av}(B)]^2 = [\Delta(N_{av})]^2, \tag{5}$$

where $[\Delta(N_{av})]$ is given by $N_{av}(A) - N_{av}(B)$.

B. Application to experimental results for high-k dielectrics

The plot in Fig. 3(a) tests the scaling of Eq. (5) for interfaces between SiO₂ and a Si oxynitride alloy, Si₃N₄ and several high-k dielectrics, yielding a power law factor of 1.7

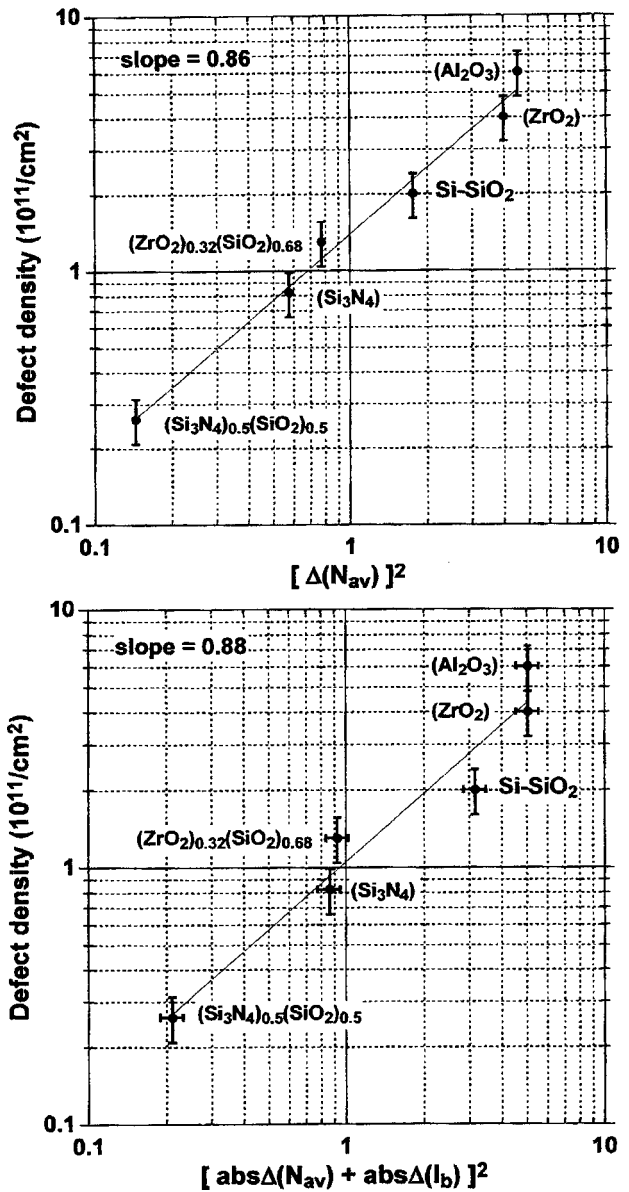


FIG. 3. Log-log plot of the interfacial defect density, as a function of $[\Delta(N_{av})]^2$ in (a) and $\propto [abs[\Delta(N_{av})] + abs[\Delta(I_b)]]^2$ in (b).

± 0.1 . This plot also includes the density of dangling bonds at the Si–SiO₂ interface, indicating that these defects have a similar origin that those at the internal dielectric interface. The value of N_{av} for ZrO₂ is based on the sevenfold coordination of oxygen for the monoclinic phase, and the point for Al₂O₃ assumes that the interface bonding is associated primarily with sixfold coordinated Al³⁺ ions. Finally a value of 2.67 has been used for SiO₂.

The plot in Fig. 3(b) adds an additional contribution from the step in bond ionicity $\Delta(I_b)$ across the interface. This contribution is always additive to $\Delta(N_{av})$ as indicated by the scaling variable in Eq. (6) which includes the addition of the absolute values of $\Delta(N_{av})$ and $\Delta(I_b)$:

$$D'_{int} \propto [abs[\Delta(N_{av})] + abs[\Delta(I_b)]]^2. \tag{6}$$

where $\Delta(N_{av}) = N_{av}(A) - N_{av}(B)$, and $\Delta(I_{av}) = I_b(A) - I_b(B)$. A comparison of Figs. 3(a) and 3(b) indicates that the power law fit factors are essentially the same, so that the inclusion of the smaller $\Delta(I_b)$ term simply shifts the plot to the right.¹⁸

Defects at the $\text{SiO}_2\text{-Si}_3\text{N}_4$ and $\text{SiO}_2\text{-Si}$ silicate alloy interfaces cannot be reduced at annealing temperatures up to 1000 °C,⁸ the temperatures required for dopant activation in ion implanted crystalline Si source and drain contacts, and in polycrystalline Si gate electrodes, whereas defects at $\text{HfO}_2\text{-SiO}_2$ interfaces can be reduced by at least 1 order of magnitude after annealing at 800–900 °C.^{19,20}

The table also includes calculated values determined from the empirical scaling relationship in fitting the data in Fig. 3. These values have been obtained by comparing measured flatband voltages with those obtained from estimates based on the doping of the Si substrate, and the work function of the gate metal atom.^{8–11}

V. STRAIN-INDUCED SELF-ORGANIZATION AT INTERNAL DIELECTRIC INTERFACES

In Ref. 1, it has been demonstrated that strain-induced self-organizations occur in interfacial transition regions during moderately high temperature annealing in inert ambients and results in reduced densities of defects and defect precursors. Several conditions are necessary for self-organization at strained internal dielectric interfaces during a postdeposition anneal. These have been addressed in Ref. 1 for Si– SiO_2 interfaces and are as follows: (i) the precursor bonding environments must be consistent with a self-organization that reduces the total energy with the determinant contribution coming from reduction of bond strain energy and (ii) the bond breaking and atomic rearrangements take place at annealing temperatures that are consistent with limitations imposed by other processing constraints, e.g., the melting temperature of Si, decomposition of SiO_2 at the Si– SiO_2 interface, and/or the chemical and structural phase separation within the *bulk* dielectric film. In addition it is most important that there be no equilibrium phases with congruent melting points between the end-members oxides at an interface between SiO_2 and a transition metal or earth silicate or aluminate dielectric.²¹ The existence of such a phase would change the end products in the chemical phase separation and either not result in a significant reduction in strain energy, or impede the kinetics for the chemical phase separation and drive the effective temperature out of the range of annealing temperatures that meet process integration restrictions. The conditions for chemical phase separation are met for 900 °C interfacial anneals for Si– SiO_2 interfaces.¹ However in this instance the end-member products are Si and SiO_2 , rather than two elemental oxides as in internal dielectric interfaces. The atomic rearrangements associated with this interfacial reaction have been confirmed by soft x-ray photoelectron spectroscopy at the interface bonding level of $\sim 5 \times 10^{14} \text{ cm}^{-2}$,²² and the by cathode-luminescence spectroscopy at the defect bonding arrangement level of $\sim 10^{12} \text{ cm}^{-2}$.²³ The temperature of this interfacial relaxation

is approximately 100 °C lower than the temperature for the onset of visco-elastic relaxation of growth-induced bulk film stress.²⁴

These criteria for an interfacial chemical phase separation are also consistent with the results for $\text{SiO}_2\text{-Si}_3\text{N}_4$ and $\text{SiO}_2\text{-Si}$ oxynitride interfaces, where in both cases the ideal products for a strain-reduction reaction would be SiO_2 and Si_3N_4 . These interfaces display no evidence for strain-driven self-organization and interfacial defect reduction for annealing and/or processing temperatures up to 1000 °C,⁸ consistent with the observation that there is a compound phase Si_2ON_2 with a congruent melting point in excess of 2000 °C between SiO_2 and Si_3N_4 .²⁵

The existence of a 900 °C chemical phase separation of SiO_x into Si and SiO_2 , and the absence of a chemical phase separation at temperatures up to at least 1000 °C at internal dielectric interfaces that include either Si_3N_4 or a Si oxynitride in contact with SiO_2 , suggest that similar correlation should exist for an interfacial chemical phase separation of TM and lanthanide RE silicate and aluminate alloy thin films in contact with SiO_2 and the nature of their appropriate equilibrium phase diagrams.

Those systems that do not have a compound phase with a congruent melting point should display a separation in the TM or RE oxide and SiO_2 , and those that have a compound phase with a congruent melting point should not. The equilibrium phase diagrams for SiO_2 and ZrO_2 , and SiO_2 and HfO_2 indicate stable silicate phases but without congruent melting points for these compound phases.²¹ In addition, the liquidus curves display either stable or incipient liquid immiscibility characteristics, and therefore are consistent with a spinoidal decomposition for silicate alloys formed by non-equilibrium thin film depositions.²¹ Thin film Zr and Hf silicate alloys have been demonstrated to display chemical phase separation at temperatures of at most 900–1000 °C.^{21,26} Based on comparisons between bond-breaking relaxations in SiO_2 at ~ 1000 °C, and interfacial bond-breaking reactions at ~ 900 °C, this suggests that interfacial relaxations should occur at temperatures of at most 800–900 °C, and possibly less, especially if the effective interfacial ZrO_2 or HfO_2 concentrations are higher than about 50%. This expectation has been realized in devices including HfO_2 and Hf silicate alloys, where fixed charge has been reduced by more than 1 order of magnitude for annealing temperatures about 700–800 °C.^{19,20} In contrast devices with Zr and Hf silicate alloys annealed at 500 °C do not show defect reduction.^{3,4} These observed reductions in Refs. 19 and 20 are attributed in this article to an interfacial chemical phase separation of interfacial Zr and Hf silicate alloy bonding groups in contact with SiO_2 into nanoscale ZrO_2 and HfO_2 , respectively, encapsulated by SiO_2 . As in the interfacial self-organization of SiO described in Ref. 1, this nanoscale self-organization also results in a decrease in interfacial bond strain.

In contrast, and also consistent with the equilibrium phase diagram differences between $\text{Al}_2\text{O}_3\text{-SiO}_2$, $\text{ZrO}_2\text{-SiO}_2$ and $\text{HfO}_2\text{-SiO}_2$, there is no reduction of defects at $\text{SiO}_2\text{-Al}_2\text{O}_3$

interfaces up to temperatures of at least 900 °C where the Al_2O_3 films undergo a bulk crystallization. This is consistent with the existence of two compound compositions with congruent melting points in excess of 2000 °C between SiO_2 and Al_2O_3 .²⁷ It is also significant that the magnitude of the fixed charge is well above what is anticipated on the base on the $N_{\text{av}}(B) - N_{\text{av}}(A)$ difference (see Table II), but agreement between the scaling is improved if the interfacial Al are assumed to be sixfold coordinated. This internal interface is being subjected to additional studies in an attempt to determine the chemical bonding arrangements of the interfacial Al atoms.

Compound phases with congruent melting points, such as $(\text{Y}_2\text{O}_3)_1(\text{SiO}_2)_2$ and $(\text{Y}_2\text{O}_3)_2(\text{SiO}_2)_1$, exist in the phase diagrams for the group IIIB TM metal atom silicates of Y and La, and for the lanthanide RE elements in the trivalent bonding states.²¹ This means that internal interfaces between interfacial SiO_2 , and either the oxides or silicate alloys of these group IIIB and lanthanide RM atoms are more than likely not to undergo a self-organization that is driven by bond strain reduction, and therefore will display levels of fixed charge, typically at the 10^{12} cm^{-2} level. Therefore they will not meet target performance and reliability required in aggressively scaled CMOS devices after processing at temperatures up to 900 °C. These estimates of fixed charge for these interfaces are based on the values of $[\Delta(N_{\text{av}})]$ included in Table II and also include the supporting results of Ref. 11, which indicate fixed charge levels in the mid 10^{12} cm^{-2} range at Y_2O_3 - SiO_2 internal dielectric interfaces for *n*MOS (NMOS) and *p*MOS (PMOS) capacitors.

The phase diagrams for ZrO_2 - Al_2O_3 and HfO_2 - Al_2O_3 do not indicate compound compositions between Al_2O_3 and the respective transition metal oxides.^{28,29} Nor do they reveal liquidus features indicative of immiscibility, and a driving force for spinodal decomposition. In addition the eutectic compositions in these systems are in the mid-alloy range, and at a temperature at least 100 °C higher than in the phase diagrams for the respective phase diagrams with SiO_2 . These systems will be investigated by the authors to determine the magnitude of the interfacial charge, as well as the effectiveness of annealing up to at least 900–1000 °C in reducing the magnitude of the interfacial fixed charge. Previously reported studies of Hf aluminate alloys with alloy compositions in the range of 35%–50% HfO_2 indicated chemical phase separation at temperatures in excess of 900–1000 °C.³⁰ Electrical studies were made on capacitors prepared from these alloys, subjected to postdeposition annealing at 800–900 °C prior to Al metallization. These devices showed significant levels of fixed negative charge, similar to those reported for Al_2O_3 devices. These levels were found in both NMOS and PMOS capacitors, confirming that the charge was fixed, and not dominated by electron injection and trapping. This suggests that the interfaces of these devices were Al_2O_3 like, and that the kinetics for a strain-driven self-organization that would reduce fixed charge was not possible for the range of annealing temperatures explored.

VI. DISCUSSION

This article has demonstrated that fixed charge localized at internal dielectric interfaces in stacked gate dielectrics comprised of interfacial SiO_2 , and alternative gate dielectrics including: (i) Si_3N_4 and Si oxynitride alloys, (ii) A_2O_3 , (iii) group IVB and IIIB TM, and lanthanide RE atom oxides, and silicate and aluminate alloys, were derived from bond strain at these internal dielectric interfaces. There are generally two components to this strain; one associated with mechanical bond strain,¹⁰ and the second with the heterovalent nature of interface bonding.¹⁷ Bond constraint theory as applied to dielectrics with CRN and MCRN amorphous morphologies indicates that the average number of bonding constraints/atom scales linearly with the average number of bonds/atom, and that electronically active defects result when the average number of bonding constraints/atom is greater than the network dimensionality. In TM and RE silicate alloys, the broken bonding bending constraint at the O-atom site of the SiO_2 host network is restored.³¹ Since strain energy scales with the square of the bond-angle strain $[\delta\theta]^2$ relative defect concentrations in the thin film dielectrics, and also at their interfaces scale with bond angle strain energy, and hence are proportional to the square of the difference of the average number of bonds/atom relative to a low defect density standard CRN dielectric, e.g., SiO_2 . Following these arguments, it has been shown that defects responsible for localized interfacial fixed charge levels ranging from the mid 10^{11} to mid 10^{12} cm^{-2} range scale with the square of the step in the average number of bonds/atom between SiO_2 , and the alternative dielectric that comprise the stack gate dielectric structure. This relationship applies when the bond strain is due to valence forces as well as bond charge and nuclear charge mismatch.

This article also identifies a mechanism for bond-strain relief by a strain-driven interfacial self-organizations, which has material and interface specific applications. Paralleling results presented in Ref. 1, self-organization is restricted to systems in which chemical phase separation into SiO_2 and an end-member elemental nitride or oxide is possible. One condition for this in mixed TM and RE oxide systems is that there exist no silicate or aluminate phases that have congruent melting points. The article distinguishes among four different internal interfaces: (i) Si- Si_3N_4 and Si-Si oxynitride alloy interfaces at which strain relief does not occur up to processing temperatures of at least 1100 °C, at which defect densities are sufficiently low not to degrade performance and reliability in high power applications with EOT extending to about 1.1–1.2 nm. (ii) SiO_2 - Al_2O_3 in which Al_2O_3 crystallizes at temperature of ~ 900 °C, below which self-organization occurs, and additionally in which there are compound silicate phases with congruent melting points which are expected to inhibit the decomposition reaction. Defect densities at SiO_2 - Al_2O_3 interfaces are in excess of $5 \times 10^{12} \text{ cm}^{-2}$, and require relatively thick interfacial layers of SiO_2 to mitigate the effects of fixed charge on channel transport. Stated differently, these values of fixed charge are too high for device applications in which EOT must be scaled to

less than 2 nm. (iii) group IVB silicates, in particular Zr and Hf silicates, display a strain-driven self-organization at temperatures less than about 800 °C and densities of fixed charge have been reduced by more than 1 order of magnitude permitting EOT scaling to at least 0.8–1.0 nm. This self-organization is consistent with the respective binary oxide equilibrium phase diagrams in which the compound silicate phases, ZrSiO₄ and HfSiO₄, do not have congruent melting points. (iv) Additionally, and based on scaling arguments and a limited set of measurements, group IIIB, Y, and La, and lanthanide RE atom oxides, and their silicate and aluminate alloys are not expected to display strain-driven self-organization at their internal interfaces with SiO₂ with the driving factor limiting defect reduction being a multiplicity of compound silicate and aluminate phases with congruent melting points.

Finally, results to date on TM aluminate systems have not displayed any indication of defect reduction via interfacial stress-relief mechanisms.³⁰ In contrast, studies of Ta aluminate devices displayed significant injection into low lying Ta *d** states, disqualifying them for device applications,³² and Hf aluminate devices display high densities of interfacial traps, also raising questions relative to device applications.³⁰

The results of this article and Part I¹ identify two limitations for aggressively scaled devices. The first is the necessity for an ultrathin interfacial SiO₂ layer to be in contact with the Si substrate in which channel transport occurs. The 900 °C interfacial relaxation provides an interfacial bonding structure that is responsible for continuance of scaling metrics, including low densities of *D*_{it}, channel transport mobilities of electrons and holes, and interface-limited/determined device reliability. The second limitation is on alternative gate dielectrics.

There are approaches for meeting ITRS targets for bulk CMOS devices.¹² The first is in devices containing the optimized Si oxynitride alloys of Ref. 5, in which the nitrogen profile is controlled at the atomic level.^{33,34} These devices have the potential to exhibit tunneling leakage currents of: (i) <5 A cm⁻² at approximately a 1 V of oxide bias for EOT between 1 and 1.2 nm and (ii) ~10⁻² A cm⁻² at approximately a 1 V for oxide bias for EOT of ~1.3–1.5 nm. These currents and EOTs are predicated on an interfacial monolayer nitride silicon oxide region that contributes approximately 0.35 nm to EOT, and which is sufficient to preserve channel transport properties, defect densities, and reliability similar to those of SiO₂ devices, i.e., meeting ITRS scaling metrics.¹² Although these devices will operate with doped polycrystalline Si gate electrodes, performance in bulk CMOS devices would be considerably improved with dual metal gate electrodes.

The second class of dielectrics includes HfO₂ and ZrO₂ and their silicate alloys. There are two important constraints. First, as for the example, given above for optimized Si oxynitride alloy devices, it is necessary to include an interfacial monolayer nitride silicon oxide region that contributes approximately 0.35 nm to EOT, so that ITRS scaling metrics can be met. Second it is necessary to subject both dielectric

interfaces, the Si–SiO₂ interface, and the internal SiO₂–high-*K* interface, to thermal annealing at temperature of approximately 900 °C to promote strain-induced self-organization at each of these interfaces. Finally, it will be necessary to quantify the effects of remote phonon scattering on channel transport,^{35,36,37} and in particular to determine if dual metal gate electrodes can effectively screen channel carrier–phonon coupling and yield current drive meeting ITRS metrics for bulk CMOS devices. Preliminary results by the Intel group suggest that metal gate electrodes are effective in screening remote phonon scattering, but more complete data and analyses are required.¹⁹

Note added in proof: Equation (7), given by

$$N'_{\text{def}} = N'_{\text{def}} [\text{abs}(\Delta(N_{\text{av}})) + \text{abs}(\Delta(I_b))]^2 \quad (7)$$

is a more generalized scaling relationship than Eq. (6), and includes two additive contributions to formation of electrically active interfacial defects: (i) the first from interfacial mechanical bond strain as described by differences in interfacial bonding coordination, $\Delta(N_{\text{av}})$, and (ii) the second from interfacial heterovalent bonding as reflected in differences in interfacial bond ionicity, $\Delta(I_b)$. The additivity of the *absolute values* in Eq. (7) is in accord with the correlation in Table I between increases in the coordination of O atoms, *n*_{Ox}, and hence in *N*_{av} as well, with increases in bond ionicity, *I*_b. A fit to the experimental data using Eq. (7), and not included as a separate figure in this article, gives a slope equivalent to a *slightly reduced and improved* power law factor of 1.15±0.1. The scaling relationship of Eq. (7) has also been used to estimate the density of Si atom dangling bond defects at Si–SiO₂ interfaces. These defects have been attributed to the mechanical bond strain induced by molar volume mismatch at the Si–SiO₂ interface between the crystalline Si substrate and the non-crystalline SiO₂ dielectric.¹ However, charge transfer, associated with the bond ionicity difference between Si and SiO₂ has been shown to contribute to an interfacial dipole.³⁸ Since this electron charge transfer is from Si atoms of the substrate to the O atoms of the dielectric, this transfer can also play a role in the formation of dangling bonds by weakening the Si–Si bonds of the substrate. The density of defects obtained from the fit parameters to Eq. (7) agrees to within experimental error to the total densities of dangling bonds, *P*_b for Si(111), and the sum of *P*_{b0} and *P*_{b1} for Si(100), as determined by electron spin resonance,^{39,40} and as discussed in Ref. 1. Since the density of dangling bond defects determines the effective spacing of these defects at Si–SiO₂ interfaces, bond constraint theory underpins, in a fundamental way, the model proposed in Ref. 1 for the empirical roughness parameter in the universal mobility expressions for both electron and hole transport in the channel regions of field effect transistors.⁴¹ The challenge remaining is to develop a model, underpinned by electronic structure, and elastic and bond constraint theory, that provides a basis for determination of the prefactor terms in Eqs. (6) and (7).

ACKNOWLEDGMENTS

This research is supported in part by the Office of Naval Research (ONR), the Semiconductor Research Corporation (SRC), and Microelectronics Advanced Research Corporation (MARCO). The authors wish to acknowledge helpful discussions with Professor Darrell Schlom at Pennsylvania State University.

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