Electron trapping in metal-insulator-semiconductor structures on *n*-GaN with SiO_2 and Si_3N_4 dielectrics

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Electron trapping in Al-gate *n*-GaN/nitrided-thin-Ga_2O_3/SiO_2 and *n*-GaN/Si_3N_4 MIS capacitors was evaluated by capacitance-voltage ($C-V$) measurements. Significant positive flatband voltage shift (ΔV_{fb}) was observed with increasing starting dc bias in the $C-V$ measurements. For similar equivalent oxide thickness and under the same $C-V$ measurement conditions, ΔV_{fb} in the nitride was 3–10 times larger than in the oxide samples. It is suggested that flatband voltage shifts are due to border traps in SiO_2 and to interface and bulk traps in Si_3N_4 samples. © *2004 American Vacuum Society.* [DOI: 10.1116/1.1806439]

I. INTRODUCTION

Studies of GaN metal-insulator-semiconductor (MIS) structures have focused on reducing the interface trap level density (D_{it}), and several researchers reported on promising *n*-GaN MIS structures with low D_{it}.[1–3] We also reported significantly reduced electron trapping in *n*-GaN/thin-Ga_2O_3/SiO_2 structures in which the dielectric is produced by a two-step process: (i) remote plasma-assisted oxidation (RPAO) of GaN to form a thin interfacial oxide ($\sim$0.6 nm thick) followed by (ii) remote plasma enhanced chemical vapor deposition (RPECVD) of SiO_2.[4,5] Based on initial studies using a variety of dielectrics, extensive research on $C-V$ characteristics at high-temperature,[2,4,6] electron trapping,[7] band offset energies,[8–10] and thermal annealing[11] are required to fully understand the surface passivation of *n*-GaN.

It is well known that Si_3N_4 presents a high density of bulk trap levels, and this seriously limits the usefulness of Si_3N_4 as a gate dielectric on Si without an intermediate SiO_2 layer. As revealed by sequential etching of Si_3N_4 films,[12] they present a nearly uniform spatial distribution of trap levels. In the Si–SiO_2 system, trap levels are located very close to the Si/SiO_2 interface; electron trapping in bulk SiO_2 is negligible compared to that associated with the Si/SiO_2 interface or bulk Si_3N_4. However, GaN/Si_3N_4 structures have been preferred over GaN/SiO_2 to minimize parasitic substrate oxidation during dielectric deposition. Parasitic substrate oxidation, or subcutaneous oxidation, usually results in a high density of interfacial defects.[3,4] Preventing subcutaneous oxidation with a sacrificial Si layer[8] or intentional, controlled oxidation of GaN (as we do[4,5]) prior to SiO_2 deposition should provide more room to reduce the density of interfacial and bulk defects in MIS structures on GaN by using SiO_2 rather than Si_3N_4 as the dielectric. Moreover, SiO_2 provides increased band offset energies with respect to GaN as compared to Si_3N_4. From this point of view, Al_2O_3 is also an attractive dielectric.

In this study, we have evaluated charge trapping in *n*-GaN/nitrided-thin-Ga_2O_3/SiO_2 MIS capacitors (SiO_2 samples) and *n*-GaN/Si_3N_4 MIS capacitors (Si_3N_4 samples) by monitoring positive flatband voltage shifts (ΔV_{fb}) using capacitance–voltage ($C-V$) measurements. For similar equivalent oxide thickness and under the same $C-V$ measurement conditions, ΔV_{fb} in Si_3N_4 samples was 3–10 times larger than in SiO_2 samples. We suggest that flatband voltage shifts are due to border traps in SiO_2 and to interface and bulk traps in Si_3N_4 samples.

II. EXPERIMENTAL PROCEDURES

The *n*-GaN grown on sapphire substrates[13] were etched in 1:5 NH_4OH/H_2O mixture at 80 °C for 15 min. For the SiO_2 samples, the substrate as-loaded into our custom-built cluster tool was oxidized by remote O_2/He plasma at 0.3 Torr for 30 s to form a superficial Ga_2O_3 layer, and then nitrided by remote N_2/He plasma at 0.3 Torr for 90 s; SiO_2 was then deposited by RPECVD using SiH_4 (2 vol % in He) and an O_2/He gas mixture at 0.3 Torr. For the Si_3N_4 samples, silicon nitride was directly deposited on wet-etched GaN by RPECVD using SiH_4 (2 vol % in He) and an N_2/He gas mixture at 0.2 Torr. In all remote plasma processing the substrate temperature was 300 °C, and rf power was 30 W at 13.56 MHz.[4,14] After SiO_2 or Si_3N_4 deposition, the samples were annealed at 900 °C for 30 s in Ar. A 300 nm thick Al layer was evaporated onto the samples and defined in square shape by conventional lithography. Postmetallization annealing was performed at 400 °C for 30 min in forming gas (N_2/H_2). The electrical properties of *n*-GaN MIS capacitors were investigated using an HP 4284A meter. The area of the devices under test was $(1-4)\times10^{-4}$ cm^2.

III. EXPERIMENTAL RESULTS

Figure 1 displays measured and simulated $C-V$ curves for SiO_2 and Si_3N_4 samples with equivalent oxide thickness (EOT) of 10.5 and 10.9 nm, respectively. These $C-V$ curves were measured at 1 MHz and 25 °C in the dark. The gate voltage V_G was swept from positive to negative; before sweeping, V_G was held at the dc starting value for 10 s. In the evaluation of expressions for the theoretical $C-V$ curves,[15,16] the same fundamental constants as in a previous

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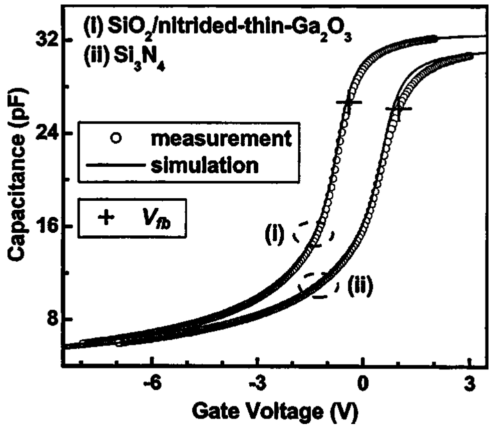

FIG. 1. Measured and simulated $C-V$ data from SiO_2 and Si_3N_4 samples. EOT is 10.5 and 10.9 nm, respectively.

report[1] were used. Assuming that the work function of both n-GaN and the Al gate is 4.1 eV, the flatband voltage V_{fb} is −0.4 and 1.0 V, respectively.

Figure 2 displays additional $C-V$ curves and $1/C^2-V$ data. In the $C-V$ characteristics of both SiO_2 and Si_3N_4 samples, increasing the starting dc bias V_G from 0 to 6 V leads to increasing shift along the gate voltage axis without severe stretchout. Positive-biasing these structures favors electron injection from the GaN substrate into the dielectrics. Accordingly, V_{fb} shifts to the positive voltage direction, corresponding to progressive buildup of negative charge in the MIS structures. The flatband voltage shift ΔV_{fb} for the Si_3N_4 sample is several times larger than that for the SiO_2 sample biased to the same starting voltage. $1/C^2-V$ data from both samples show good linearity and clear deep depletion without inversion below the threshold voltage. For the SiO_2 sample, the net donor concentration N_D calculated from the linear portion of $1/C^2-V$ increases from 4.10 to 4.18 $\times 10^{17}$ cm^{-3} as the starting V_G goes from 0 to 6 V; for the Si_3N_4 sample, it increases from 4.20 to 4.43×10^{17} cm^{-3}. Such increase is due to the emission of trapped electrons and appears as minor stretchout in the $C-V$ curves.

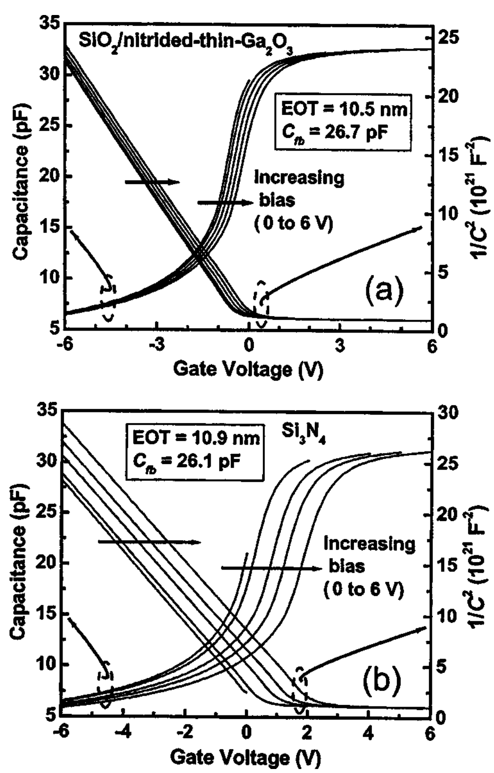

FIG. 2. $C-V$ and $1/C^2-V$ data for (a) SiO_2 and (b) Si_3N_4 samples. From left to right curves, starting dc bias is 0, 2, 4, 5, and 6 V.

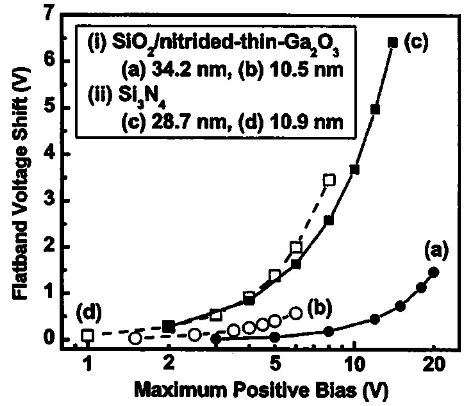

FIG. 3. Flatband voltage shift in SiO_2 and Si_3N_4 samples as a function of maximum (starting) dc bias in the $C-V$ measurements.

Figure 3 displays ΔV_{fb} data from SiO_2 and Si_3N_4 samples of EOT ~30 and ~10 nm as a function of starting V_G (maximum positive bias) in the $C-V$ measurements. It quantitatively reveals the behavior observed in Fig. 2, namely that ΔV_{fb} monotonically increases with increasing starting V_G and that ΔV_{fb} is larger for the Si_3N_4 samples. For both SiO_2 and Si_3N_4 samples, ΔV_{fb} at a given bias is more severe in the sample with thinner dielectric, which is submitted to higher electric field. The data is consistent with electron trapping in successively deeper trap levels, which become accessible as the electric field is increased. It is interesting to note that there is no evidence of ΔV_{fb} saturation, which could be expected as long as V_G is kept below the onset of dielectric degradation. The same observation was made in another report of electron trapping in MIS structures on GaN.[7]

Figure 4 shows hysteresis windows in $C-V$ data from SiO_2 and Si_3N_4 samples. In all measurements the gate voltage was first swept from positive to negative and then back. For both samples, the data indicate that a low maximum V_G results in a small hysteresis window. Increasing the maximum V_G leads to the ΔV_{fb} already shown and to significant hysteresis windows. Figures for the SiO_2 sample under the bias range ±20 V are ΔV_{fb}=1.5 V (trace) and 0.7 V (retrace), indicating that approximately half of the electrons trapped under positive bias remained so during retrace. If all the activity takes place at the dielectric/GaN interface, ~5 $\times 10^{11}$ q cm^{-2} (where q is the elementary charge, 1.6022 $\times 10^{-19}$ C) is released between trace and retrace. When the bias range was ±60 V for an n-GaN MIS structure featuring a ~100 nm thick SiO_2 dielectric film, ΔV_{fb}=4 V (trace) and 2 V (retrace).[7] Figure 4(b) reveals that the Si_3N_4 sample un-

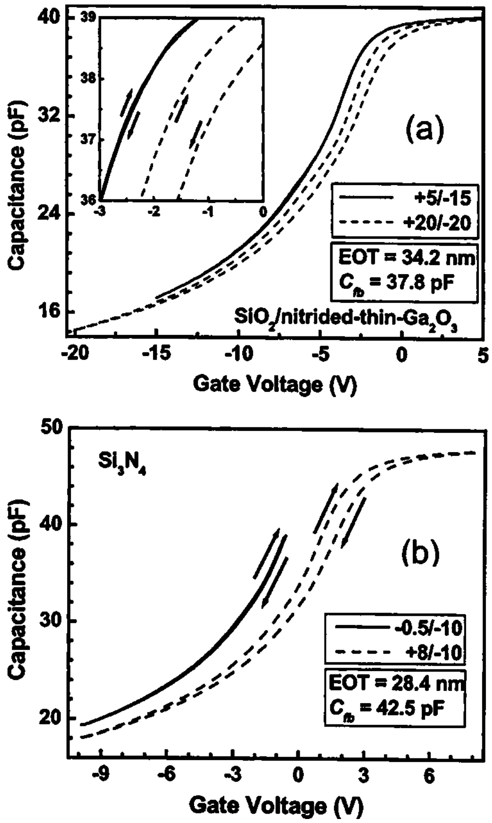

FIG. 4. Hysteresis window in $C-V$ data from (a) SiO_2 and (b) Si_3N_4 samples.

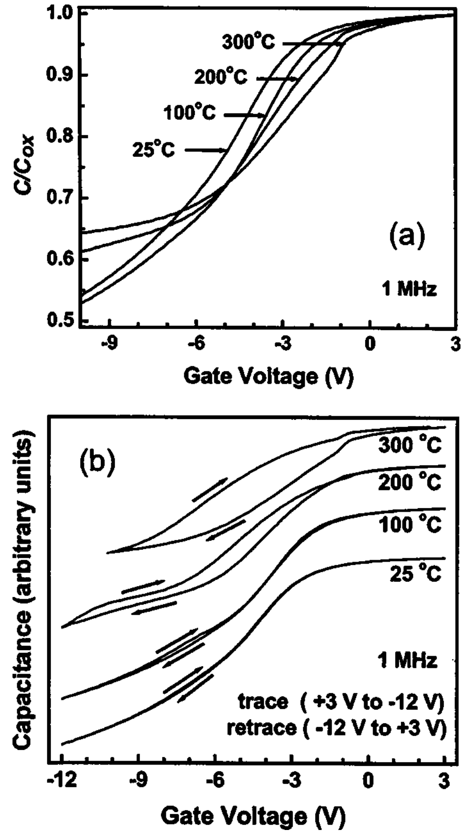

FIG. 5. (a) $C-V$ characteristics of MIS capacitors featuring SiO_2 as the dielectric with measurement temperature as parameter, including (b) hysteresis window behavior. C_{ox} is the capacitance of the MIS structure biased to accumulation.

der the bias range +8 to −10 V yields $\Delta V_{fb}=2.6$ V (trace) and 1.9 V (retrace). Again, if all the activity takes place at the dielectric GaN interface, $\sim 5\times 10^{11}\ q\ cm^{-2}$ is released between trace and retrace.

Figure 5(a) shows $C-V$ characteristics of MIS capacitors featuring SiO_2 as the dielectric with measurement temperature as parameter. Increasing temperature leads to: (i) increasing flatband voltage shift in the positive voltage direction; (ii) $C-V$ curve stretchout; and (iii) increasing measured capacitance at the negative voltage end of the sweep range. We attribute observations (i) and (ii) to enhanced activity of electronic states spatially located close to the dielectric/GaN interface, as discussed in the next section. Observation (iii) could be due to minority carrier generation, as under reduced gate voltage sweep rate at room temperature.[7] Finally, Fig. 5(b) shows that the $C-V$ hysteresis window increases with increasing temperature. Such increase is attributed to enhanced release (detrapping) of electrons when the gate is biased below V_{fb} (end of trace, beginning of retrace) at high temperature.

In principle, the observed temperature-dependence of the flatband voltage allows us to estimate the pyroelectric charge coefficient of GaN (Ref. 6) as $\sim 3\times 10^{9}\ q\ cm^{-2}\ K^{-1}$. However, $C-V$ curve stretchout and hysteresis window indicate that electron capture and emission associated to (near-) interface traps increase at high temperature and are not negligible in the measured positive flatband voltage shift. Therefore, the actual pyroelectric charge coefficient of GaN should be smaller than the number just presented.

IV. DISCUSSION

A seemingly possible explanation for the observed electron trapping is the presence of electronic states at the GaN/dielectric interface. However, we note that the substrate is doped to $N_D > 4\times 10^{17}\ cm^{-3}$, and as a result the semiconductor Fermi level is $\sim$0.1 eV below the conduction band edge. We further consider that SiO_2 samples as presented in Fig. 1, showing $V_{fb}<0$, should have nearly all interface states occupied under thermal equilibrium (i.e., $V_G=0$). Therefore, little further trapping should be possible *at the GaN/nitrided-thin-Ga_2O_3 interface* due to substrate electron injection. The situation is different for Si_3N_4 samples as in Fig. 1. In this case, $V_{fb}=1$ V corresponds to a finite energy interval next to the GaN conduction band edge in which interface states possibly existing in the samples are unoccupied under thermal equilibrium.

The considerations above call for an assessment of D_{it} in Si_3N_4 samples. Figure 6 displays D_{it} data as obtained from both Si_3N_4 and SiO_2 samples at room temperature using the high-low frequency $C-V$ (1 kHz–1 MHz) and the ac conductance techniques. D_{it} at 0.3 eV below the conduction

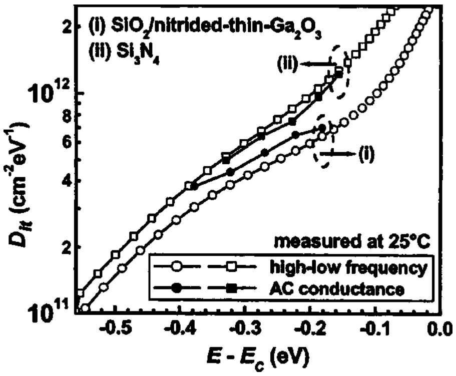

FIG. 6. D_{it} as determined in SiO_2 and Si_3N_4 samples using the high-low frequency and the ac conductance techniques at room temperature.

band edge E_c is ~ 5 and $\sim 6 \times 10^{11}$ cm^{-2} eV^{-1}, respectively, for the SiO_2 and Si_3N_4 samples. D_{it} in the latter gives room to significant electrical activity, compatible with our observations of electron trapping. The D_{it} figures in the limited energy range available due to measurement at room temperature are similar to the D_{it} reported for an oxide/nitride/oxide gate stack on GaN.[2] Already at $E\text{-}E_C < -0.4$ eV the high-low frequency $C-V$ technique provides underestimated D_{it} because 1 kHz is not low enough to allow the response of interface states. No use is made of the Terman technique because interface states continuously distributed in energy could be interpreted as increased N_D, resulting in severe underestimation of D_{it}.

As a further step to understand electron trapping in the Si_3N_4 samples and seeking an explanation for trapping in the SiO_2 samples, we assume for the moment that ΔV_{fb} is entirely due to charge trapping at the semiconductor–dielectric interface and convert the data in Fig. 4 to dielectric trapped charge density Q_{ox} by using $Q_{ox} = C_{ox} \Delta V_{fb}$, where C_{ox} is the capacitance of the MIS structure biased to accumulation. We also convert maximum gate bias to electric field in the dielectric E_{ox} using $E_{ox} = V_{ox}/t_{ox,eq} = (V_G - V_{fb} - \psi_s)/t_{ox,eq}$, where V_{ox} is the voltage drop across the dielectric, $t_{ox,eq}$ is EOT, and ψ_s is the semiconductor band bending (negligible under accumulation). The resulting $Q_{ox}(E_{ox})$ data is shown in Fig. 7. At constant electric field, Q_{ox} depends on the thickness of the

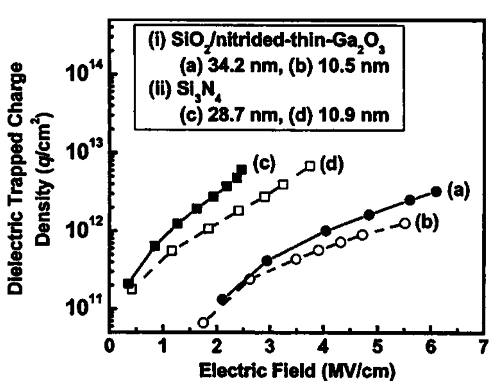

FIG. 7. $Q_{ox}(E_{ox})$ data obtained from the results in Fig. 3 under the assumptions discussed in the text.

Si_3N_4 samples; in SiO_2 samples such dependence, if existent, is not as strong. Due to the sample preparation conditions, the GaN/Si_3N_4 and $GaN/nitrided\text{-}thin\text{-}Ga_2O_3/SiO_2$ interfaces should be independent of dielectric thickness, and so should electron trapping at these interfaces. Therefore, we conclude that electron trapping in the Si_3N_4 samples is occurring *both* at the *interface* with GaN and in the *bulk* dielectric film.

To explain electron trapping in SiO_2 samples we invoke the concept of border trap presented by Fleetwood *et al.*[17] In essence, these are traps spatially *close* to but *not at* the dielectric/semiconductor interface. Physical separation disconnects the border traps from electrical activity at the interface up to the point that energetic carriers are capable of traversing the region of separation. Given our experimental results and considerations made so far, we attribute to border traps the electron trapping in SiO_2 samples. Further, we suggest that the nitrided-thin-Ga_2O_3/SiO_2 interface (distant ~ 0.6 nm from the true semiconductor/dielectric interface, GaN/nitrided-thin-Ga_2O_3) as the physical location of the border traps. This could be confirmed using the approach of Johnson *et al.*[18] High electric fields and/or high temperature would make such states available to electrons injected from the substrate. It is not possible at present to assign the energy distribution of trap levels, neither at the GaN/Si_3N_4 nor at the nitrided-thin-Ga_2O_3/SiO_2 interface. Studies of the temperature dependence of current–voltage $(I-V)$ characteristics may be useful for such assignment.[19]

Under the recurring evidence of poor electrical quality of GaN/Si_3N_4 interfaces and an indication of charge trapping at nitrided-thin-Ga_2O_3/SiO_2 interfaces, we now use constraint theory as in Ref. 20 to justify the present results and in an attempt to identify what could be a more successful dielectric/semiconductor interface structure for MIS devices on GaN. In essence, one seeks a structure showing an average coordination number N_{av} that matches constraints to degrees of freedom. If both bond-bending and stretching forces are present, the optimal average coordination number is $N_{av}^* = 2.4$. Overconstrained networks, i.e., those with $N_{av} > N_{av}^*$, suffer from strain energy accumulation, which leads to defects. Experiments have shown that $N_{av} \sim 3$ represents an upper boundary between low defect density $(\sim 10^{16}$ $cm^{-3})$ and increasingly defective materials.[21] We calculate $N_{av} = 3.6$ for the GaN/Si_3N_4 interface and $N_{av} = 3.2$ for the GaN/nitrided-thin-Ga_2O_3/SiO_2 structure. These are essentially weighted averages of the bulk N_{av} for the materials involved. The difficulty in making a high-quality interface to GaN is consistent with its $N_{av} = 4.0$. Si_3N_4, Ga_2O_3, and SiO_2 have N_{av}, respectively, equal to 3.4, 3.0, and 2.7. Therefore, considering constraint theory alone, an abrupt GaN/SiO_2 interface could be preferred. However, it has been pointed out that there is an inherent mismatch of electronic and nuclear charge between GaN and deposited dielectrics such as SiO_2, resulting in poor interfaces.[22] The plasma oxidation step that produces a thin Ga_2O_3 layer on GaN was then proposed to result in the redistribution of electronic charge necessary to produce an adequate interface. Under that interpretation, our present results suggest that high-quality interfaces are produced within a narrow plasma oxidation processing window, which would be the one providing electronic charge redistribution without excessive strain energy accumulation. Plasma nitridation of the thin Ga_2O_3 layer was adopted in this study based on experimental evidence of enhanced MIS capacitor performance,[4,5] so a deleterious role for nitrogen is not supported, although again a narrow optimal processing window may be the case.

V. CONCLUSIONS

We have presented extensive $C-V$ characterization of MIS capacitors on n-GaN featuring nitrided-thin-Ga_2O_3/SiO_2 and Si_3N_4 dielectrics prepared by remote plasma assisted processing. Increasingly positive flatband voltage shift was observed with increasing starting dc bias in the $C-V$ measurements. This was attributed to trapping of electrons injected from the substrate. Our results showed that n-GaN/Si_3N_4 structures possess a significantly higher density of electron trap levels than n-GaN/nitrided-thin-Ga_2O_3/SiO_2 structures. Electron trapping in the former was attributed to interface and bulk traps, and in the latter to border traps at the nitrided-thin-Ga_2O_3/SiO_2 interface. An inferior performance of Si_3N_4 as compared to nitrided-thin-Ga_2O_3/SiO_2 in passivating the GaN surface was shown to be expected using bonding constraint theory considerations.

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