ABSTRACT

MURTHY, PRANAV. Design of a Full Power Test System for Semiconductor Switching Characterization. (Under the direction of Dr. Douglas C Hopkins.)

Switching characterization of power semiconductors is commonly determined by Double Pulse Test. This method does not completely reflect real application circuit conditions like parasitic inductance and self heating of the device. Designing an application circuit specifically for switching loss calculation is expensive especially for high power circuits. In this thesis, an Energy Re-circulation based circuit is designed to test 6kV, 100A Super Cascode Power Modules switching characteristics under full power conditions. The circuit uses inductor and capacitor to store energy and re-circulate at higher power levels than available from the supply. A complete system with cooling solution for test devices, controller for current regulation, bus bar for circuit connection and their assembly is presented.

Design of a Full Power Test System for Semiconductor Switching Characterization

by
Pranav Murthy

A thesis submitted to the Graduate Faculty of
North Carolina State University
in partial fulfillment of the
requirements for the Degree of
Master of Science

Electrical Engineering

Raleigh, North Carolina

2021

APPROVED BY:

Dr. Subhashish Bhattacharya

Dr. Wensong Yu

Dr. Douglas C Hopkins
Chair of Advisory Committee

DEDICATION

To my mother for being the greatest source of strength and encouragement in my life.

BIOGRAPHY

Pranav Murthy received his Bachelor's degree in Electrical Engineering from University of Mumbai in 2018. He joined North Carolina State University to pursue a Master's degree in 2018 and has been working under the guidance of his advisor, Dr. Douglas C Hopkins, since August 2019. His research interests include high voltage and high-density converter design for power supplies.

ACKNOWLEDGEMENTS

I would like to thank my advisor, Dr. Douglas C Hopkins, for his support and guidance throughout my graduate studies. I am very grateful to Dr. Hopkins for providing me an opportunity to work with him at the PREES lab and introducing me to Power Electronics Packaging. His advice and encouragement has helped me think critically about technical problems and become a better engineer. I would also like to thank my committee members, Dr. Subhashish Bhattacharya and Dr. Wensong Yu, for serving on my committee and providing valuable guidance and feedback.

I would like to thank my parents for supporting and enabling me to pursue my dreams. This would have not been possible without their blessings.

Lastly, I would also like to thank all my friends, colleagues and lab mates at PREES for their friendship and mutual support which made this journey more enjoyable. Special thanks to Utkarsh and Tzu-Hsuan for always being available for technical discussions and helping me to learn package processing in the lab.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

CHAPTER

1

INTRODUCTION

1.1 Overview

Power semiconductors are considered to be the most important components in modern power processing equipment from grid applications, electric vehicles, motor drives to low power household applications. Therefore it is important to accurately analyse and design compact and efficient systems. Semiconductor testing plays an important role in characterization and determining reliability of new devices. Silicon Carbide MOSFETs are considered as leading candidates to replace IGBTs in medium voltage (2.5kV - 15kV) applications. Authors in [1] have demonstrated the use of low voltage JFETs and MOSFETs to build Supercascode switch structures which have low ON resistances and capable of fast switching at high voltages.

In order to investigate new power electronic circuit topologies it is important to have accurate loss models of these semiconductor devices. Typically, characterization tests for new MOSFETs include Static and Dynamic tests. Static tests in [2],[3],[4],[5] are performed using curve tracers such as Keysight B1015A which can completely define the device output and transfer characteristics, on state resistance, threshold voltages, and junction capacitances. A dynamic test includes Double Pulse Testing which switches a MOSFET under inductive load to determine switching characteristics. This, however, does not accurately predict the switching behavior in an application because of different operating conditions. These differences can be circuit parasitics in the commutation loop, device parasitic capacitance and distortions caused by probes and cables[6],[7]. Building an identical test system to the application circuit only to evaluate devices at rated conditions would be expensive and time-consuming especially for high power application.

This thesis explores how circuits based on Energy Re-circulation topology can be used to perform full power tests [8]. The operation and virtual design of a 6kV,100A test circuit will be discussed in detail here. Because of the 2020 pandemic, the Full Power Test circuit demonstration was limited to a virtual circuit design.

1.2 Thesis Outline

This thesis is divided into 4 parts

- **Chapter 2** provides background to Full Power Test circuit and how it is related to the other test methods.
- **Chapter 3** discusses the working of the circuit and formulate equations for system sizing
- **Chapter 4** discusses the design of passive components and selection of switching frequency

- **Chapter 5** details the design of current controller, cooling system, bus bar and shows the assembly of the system

CHAPTER

2

BACKGROUND AND LITERATURE REVIEW

This chapter discusses the Static and Dynamic methods used to characterise electrical behaviour of switching power semiconductors. The drawbacks of the classical methods are listed and compared to the advantages of the Full Power Test method.

2.1 Static Characterization

A static characterization test is used to determine the DC and AC behaviour of a MOSFET. This includes output and transfer characteristics, on state resistance, threshold voltage and junction capacitances. References [2],[3],[4],[5] show the static characterization process on newly developed high voltage SiC MOSFETs using a Curve Tracer, Impedance analyser and hot plate to test over a range of temperature. This test is important to understand the working principle and operating limits of the Device Under Test (DUT). The next section describes how switching performance is evaluated for a DUT.

2.2 Dynamic Characterization

A Double Pulse Test (DPT) is commonly used to characterize dynamic behaviour of MOSFETs. This test is carried out by switching a clamped inductive load on and off at a set current. It can be used to measure turn on and turn off time, current and voltage rise times, and energy lost in transitions. Figure 2.1 shows a typical DPT setup with a MOSFET and Schottky diode.

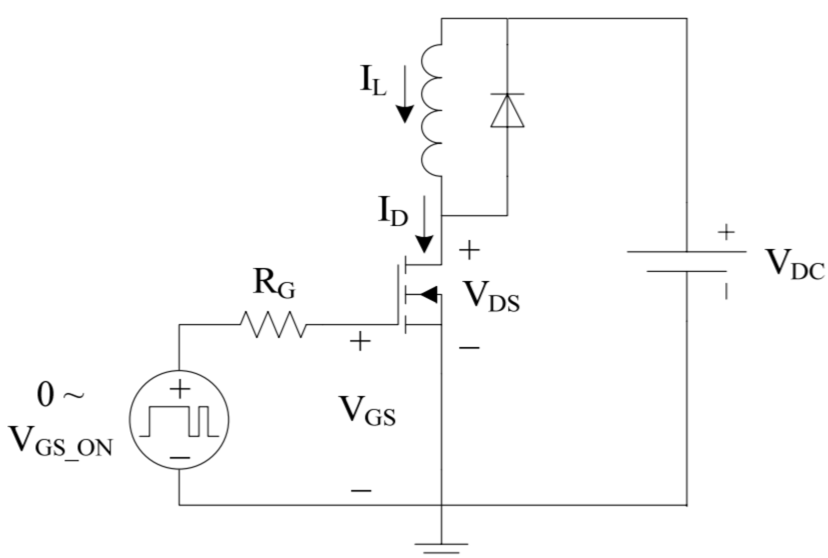

Figure 2.1: Typical Double Pulse Test Circuit

The MOSFET is switched on to build up current in the inductor to a target value and then turned off. The current freewheels through diode D for a short time and the MOSFET is switched back on. The inductor L is sized such that the load current remains nearly constant during freewheeling when the current commutates from MOSFET to diode or the opposite. The two transitions of switching off and turning back on at the rated current are recorded to determine energy lost during transition. The Figure 2.2 shows a typical gate pulse and current waveform of a DPT.

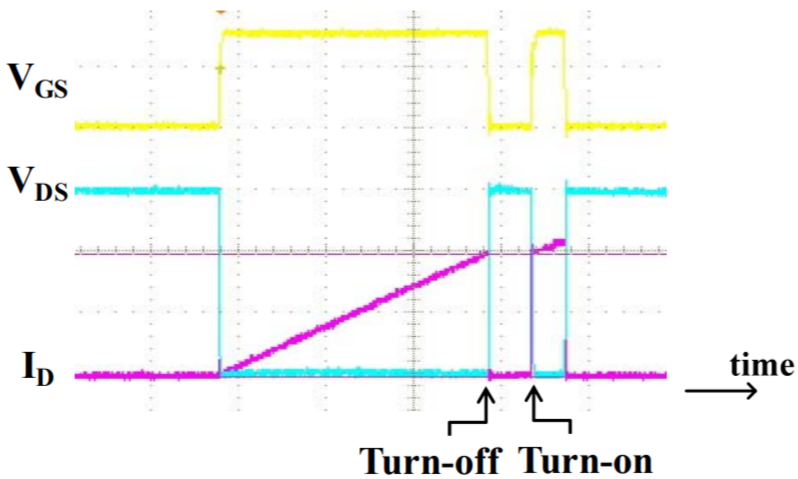

Figure 2.2: Typical Double Pulse Test Waveform

A shunt resistor at the source terminal of MOSFET or a Rogowski coil can be used to sense the device current. The test circuit is designed such that the parasitic loop inductance and stray capacitances are kept to a minimum. Pulse width is usually short enough to not cause significant self heating of the device. A change in gate driver resistance and device temperature affects the $\frac{di}{dt}$, $\frac{dv}{dt}$ and $V-I$ characteristics [9]. The switching loss is affected by the test circuit layout, gate driver and parasitic inductance in the commutation loop, which may not resemble the application circuit[7]. Self-heating of devices during DPT of high voltage and high current devices leads to error in loss measurement [10].

2.3 Full Power Test

The classical methods of semiconductor testing have some shortcomings in accurately predicting switching losses as discussed in the previous section. A straightforward way to evaluate losses accurately would be to build an identical test system for this purpose. Although, it might become very difficult and expensive especially for high power applications.

In [8] a new class of switched mode circuit called Energy Re-circulation and Storage Circuits (ERSC) is introduced. This circuit pumps in and stores energy in inductor and capacitor to create higher flow of power than the source provides, and dissipates it in the device under test. Figure 2.3 shows a Boost-Buck ERSC in which the energy re-circulates between L and C and the power supply only provides for the losses in semiconductors. Switch S1 is modulated independently to control I_1 and switch S2 controls voltage V_c and I_2.

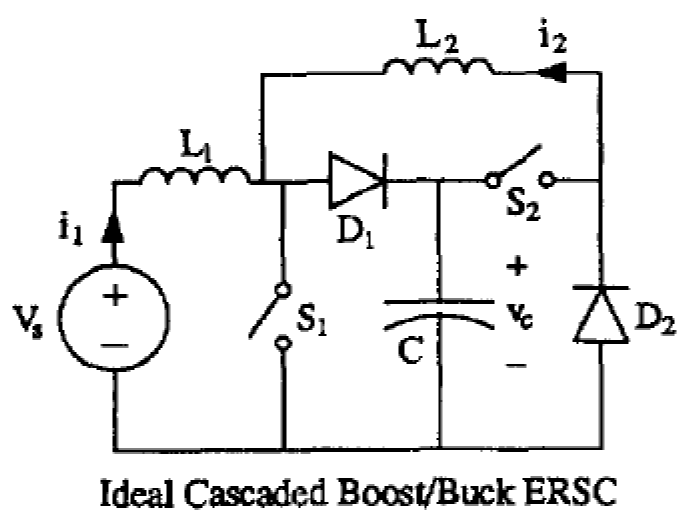

Figure 2.3: Ideal ERSC Buck Boost [8]

The main circuit under consideration for this thesis is obtained by modifying the Boost-

Buck converter to an Asymmetric half bridge converter as shown in Figure 2.4. This change limits capacitor to a fixed voltage and only inductor current can be ramped up. Inductor current increases when both S1, S2 are ON and it decreases when both switches are off. When only one of the switches is ON, the current freewheels with the diode.

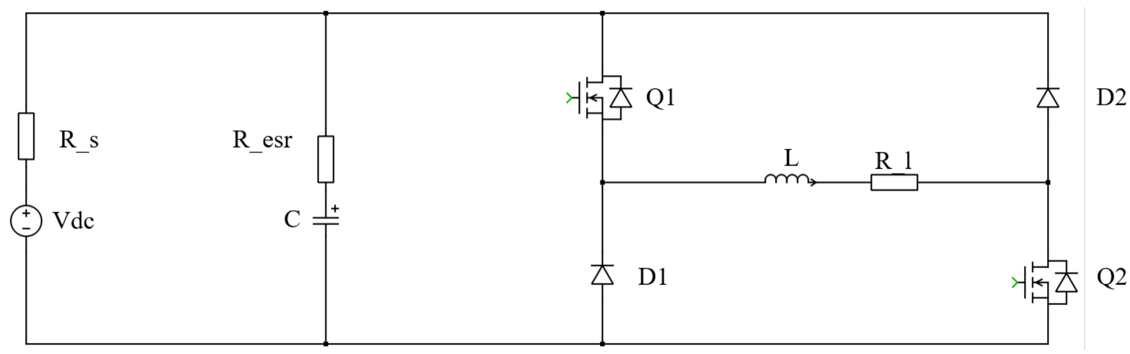

Figure 2.4: Full Power Test Circuit

A similar circuit is used in [11] to perform device characterization of low voltage IGCTs (1.5kV) and diodes (3.3kV) under real working conditions. Figure 2.5 shows the test circuit with two opposing switching cells connected by an inductor known as the Opposition Method. A current control loop is used to vary the load from 0 to 2kA at different switching frequencies. The device power losses are measured using calorie meter and power analyzer.

By expanding this circuit to a Full bridge topology, [6] demonstrates a full power emulation with GaN devices under hard and soft switching conditions. Figure 2.6 shows the circuit used for this test.

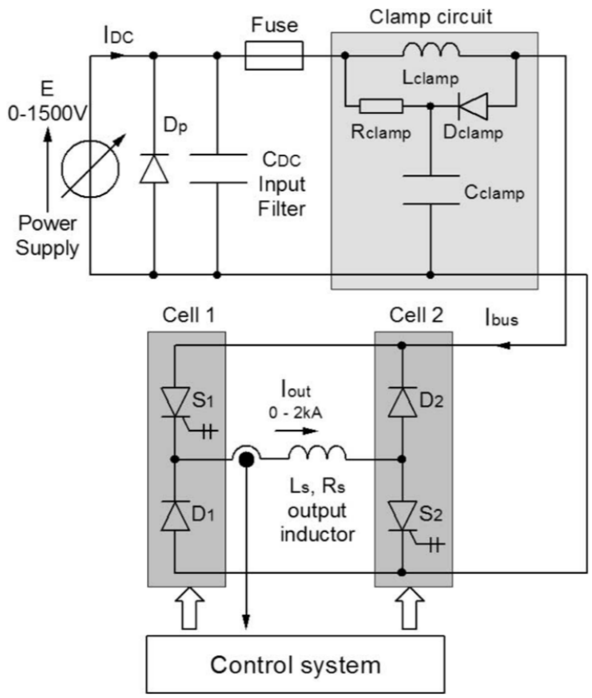

Figure 2.5: IGCT Test circuit [11]

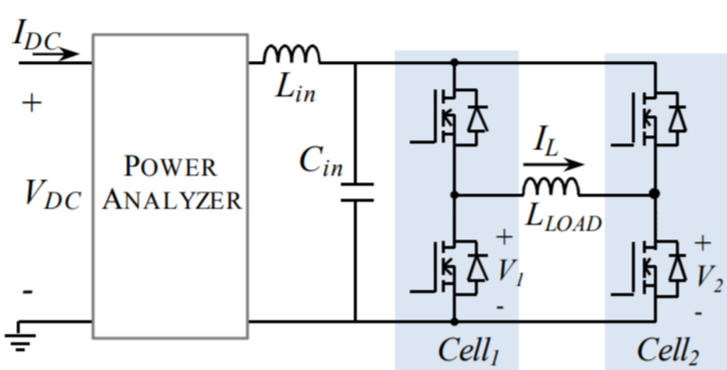

Figure 2.6: Opposition Method cell [6]

CHAPTER

3

CIRCUIT OPERATION

This chapter discusses the design and operation of the Full Power test circuit used in this thesis.

3.1 Operating principle

Figure 3.1 shows the test circuit power stage derived from the ERSC Boost-Buck converter. A single MOSFET and diode connection form a switching cell which are connected in opposition to form this circuit. A DC link capacitor stores the recirculating energy. The DC power supply is used to supply the losses of the circuit. Resistor R_{sup} is for current limiting the power supply.

In this thesis a 'Virtual Design' of a 6kV,100A setup for Full Power test of the 100A Super

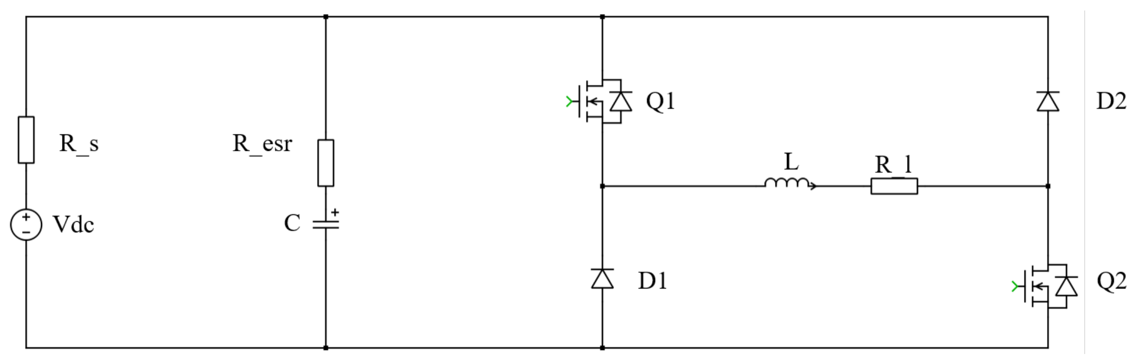

Figure 3.1: Full Power Test Circuit

Cascode Power Module (SCPM) [1] will be presented in Chapter 4.

3.1.1 Modes of operation

Assuming the control loop has reached steady state for the set value of current the following modes can be identified.

Mode 1 (Fig.3.2): Current build up - MOSFETs Q1 and Q2 are conducting and inductor current, I_L starts rising from its lowest value I_{min}. The inductor current ripple, ΔI is controlled by adjusting the overlap time, t_o for which Q1, Q2 are both ON. Voltage across inductor is $(V_{cap} - I_L(2R_{ds\,ON} + R_l))$ where, V_{cap} is the voltage across capacitor, $R_{ds\,ON}$ is the ON resistance of the MOSFET and R_l is the Equivalent Series Resistance (ESR) of the inductor.

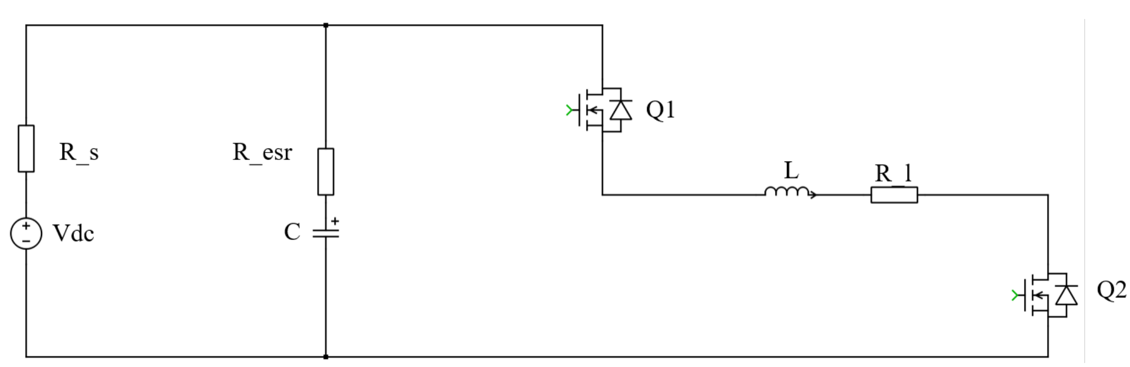

Figure 3.2: Mode 1

Mode 2 (Fig.3.3): Re-circulation - As the current reaches it highest value I_{max}, switch Q1 is turned off and current commutates from Q1 to D1. If the device losses are low, inductor current is held almost constant in this state. Switch Q2 remains ON.

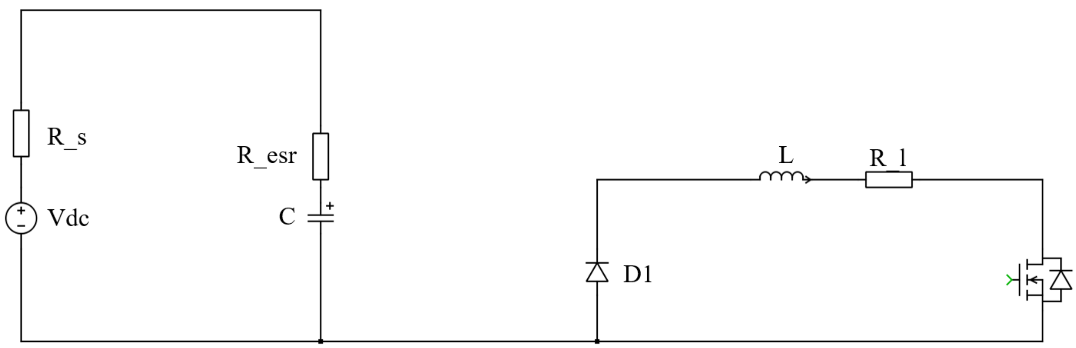

Figure 3.3: Mode 2

Mode 3 (Fig.3.4): Current reduction - Switch Q2 is turned off and diodes D1, D2 starts conducting. Voltage across inductor L becomes $(-V_{cap} + 2V_f + I_l * R_{ds\,ON})$ where, V_f is the forward voltage drop of the diode. The current starts reducing as $(\frac{-V}{L}\frac{di}{dt})$ and charges the capacitor.

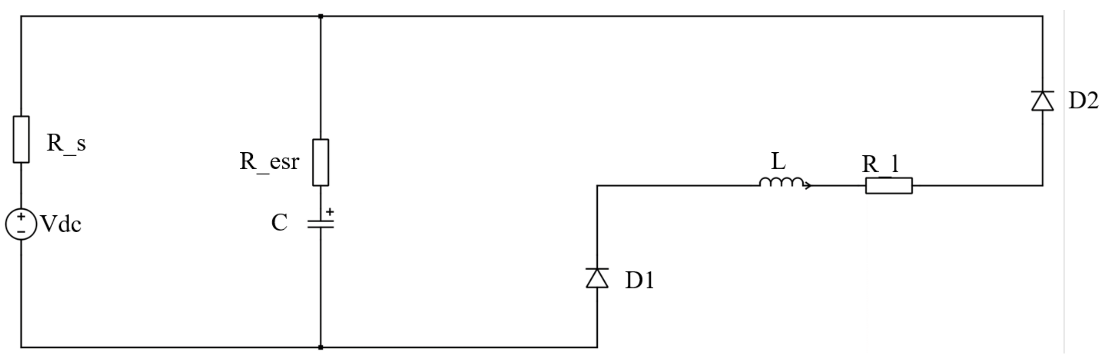

Figure 3.4: Mode 3

Mode 4 (Fig.3.5): Re-circulation - After the inductor current reaches I_{min}, switch Q1 is turned back ON. The current commutates from Q2 to D2 and re-circulates through Q1 and

D2.

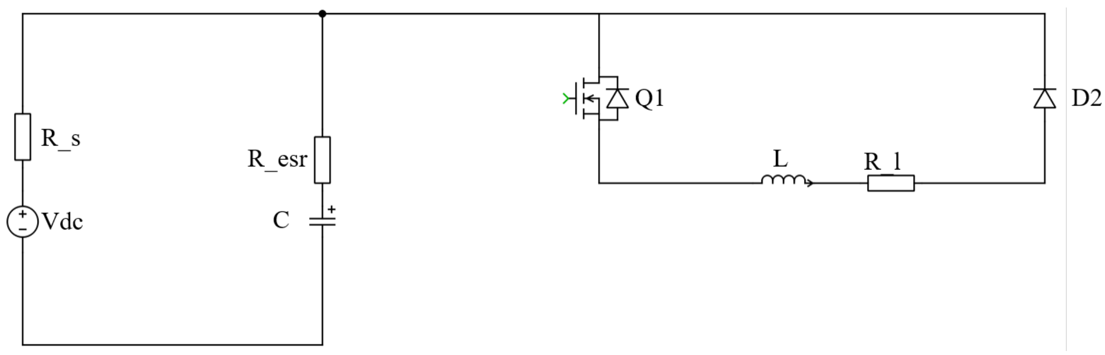

Figure 3.5: Mode 4

3.1.2 Switching pattern

In this circuit the current can be built up to any desired level by forcing a net positive volt-sec product across the inductor using a current control method. The switch Q2 is set to a fixed duty of 0.5 and the switch Q1 is controlled by the regulator. The Fig.3.6 shows build up of current when $d1 + d2 > 1$ where d1 and d2 are duty cycles of switches Q1 and Q2 respectively.

At steady state, when the average inductor current reaches a set value, the duty d1 settles to a value slightly above 0.5 to compensate for the losses in the circuit. This time difference in duty cycle between $d1$ and $d2$ is defined as ϵ, which can be calculated by using the formula[12]:

$$\epsilon = \frac{P_{loss}}{P_{in} * f_{sw}} \tag{3.1}$$

The gate pulses of Q1 and Q2 are phase shifted in time, defined as Φ (sec), which reduces the value of inductance required for a certain allowed ripple.

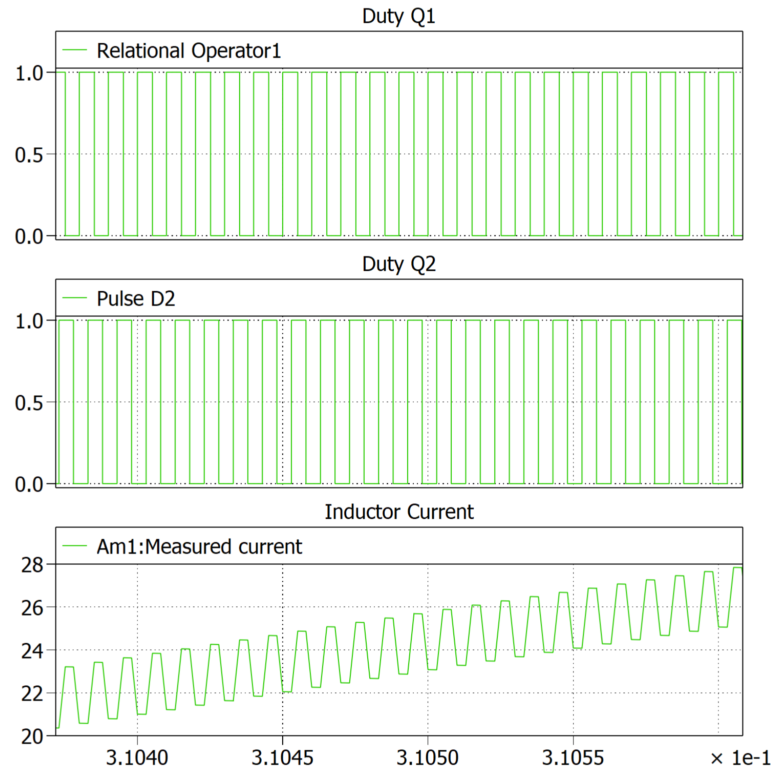

Figure 3.6: Inductor current build up

3.2 Component sizing

Power stage loss estimation: The capacity of a power supply will be determined by the total circuit and DUT losses to be compensated. The circuit is expected to have conduction and switching losses in the semiconductors and parasitic resistance in the passives. The total power recirculating in the circuit at steady state will be $E * I_L$ where E is the DC link voltage and I_L is the average inductor current. Only a fraction of this will be lost as active power. Therefore the power source should be sized according to the sum of all the expected losses and some margin above it.

The current through the MOSFETs Q1,Q2 can be approximated to a square wave shape since ΔI is small compared to I_L.

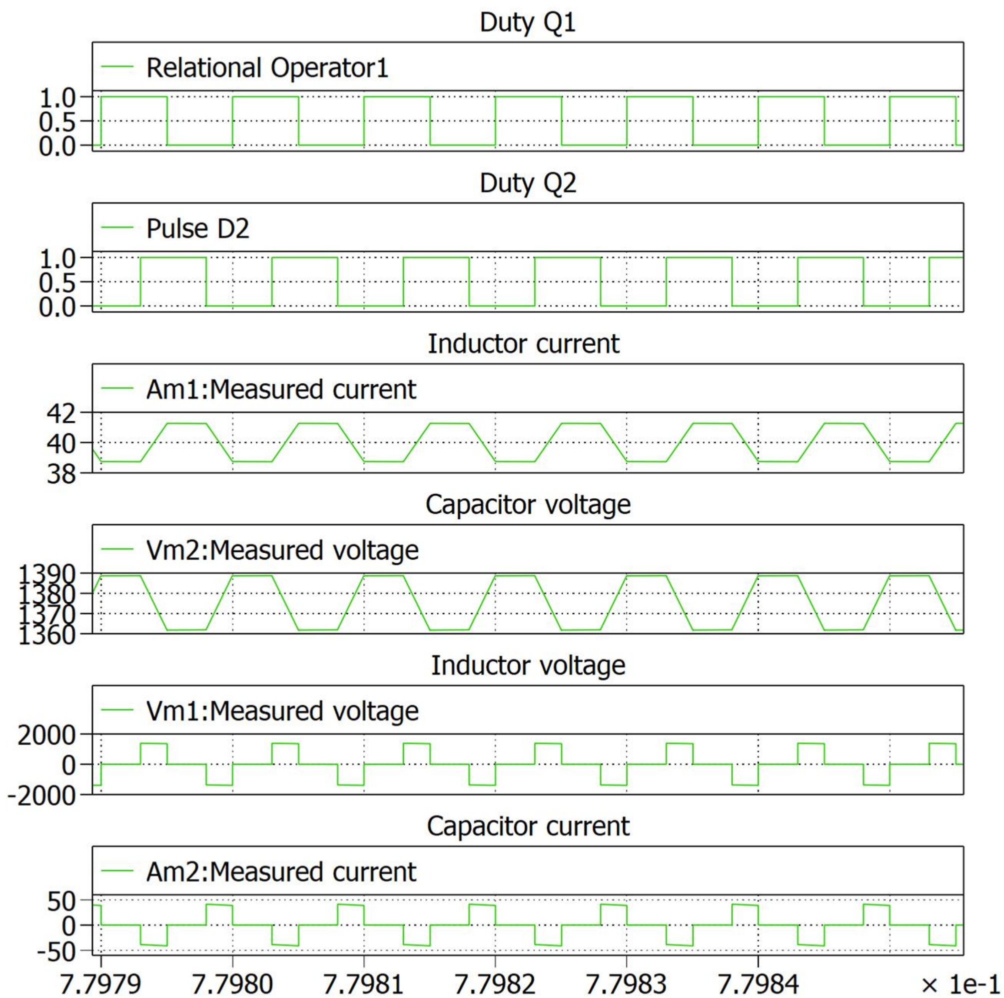

Figure 3.7: Steady state waveform

$$I_{rms} = I_{max} * \sqrt{D} \tag{3.2}$$

$$I_{avg} = I_{max} * D \tag{3.3}$$

where, I_{rms} is the Root Mean Square (RMS) of the current through MOSFETs, I_{max} is the highest value of current through Q1,Q2 and D is the duty cycle of the switches.

Therefore, the MOSFET conduction and switching losses can be estimated as:

$$P_{cond} = I_{rms}^2 * R_{dsON} \tag{3.4}$$

$$P_{sw} = (E_{on} + E_{off}) * f_{sw} \tag{3.5}$$

where, f_{sw} is the switching frequency and E_{on}, E_{off} are the ON and OFF switching energy of the MOSFET.

Diode losses can be estimated as:

$$P_{cond} = V_f * I_{avg} + I_{rms}^2 * R_d \tag{3.6}$$

$$P_{sw} = Q_c * V_{out} * f_{sw} \tag{3.7}$$

where, Q_c is the total junction charge at voltage V, R_d is the equivalent resistance and V_f is the forward voltage of the diode.

Assuming an air core inductor, the copper losses due to its DC resistance can be calculated as:

$$P_{ind} = I_{L avg}^2 * R_L \tag{3.8}$$

where, R_L is the equivalent series resistance of the inductor.

Switching Frequency: In this test the SCPM is selected for evaluation which is based on fast switching Silicon Carbide JFETs. The switching frequency for test can be selected based on the type of application circuit that the SCPM is intended to be used in. The maximum switching frequency for test under full power will depend on total module losses and the cooling capacity of the cold plates.

Inductor: As seen from figure 3.7, for a fixed current ripple, inductance L is directly dependent on the overlap time (t_o) between Q1 and Q2. For a given test condition where E is the maximum DC link voltage and ΔI is the maximum allowed ripple current, the required inductance value can be defined as:

$$L = \frac{E * t_o}{\Delta I} \tag{3.9}$$

Capacitor: A DC link capacitor is connected to store energy during re-circulation. The minimum required size of a capacitor is given by:

$$C = \frac{I_{max} * t_o}{\Delta V} \tag{3.10}$$

where, ΔV is the maximum allowed ripple voltage and I_{max} is the peak inductor current during operation.

Overlap time t_o directly influences the required inductance and capacitance, therefore it should be minimised to reduce the size of the test setup.

CHAPTER

4

COMPONENT DESIGN

This chapter discusses the design and sizing of the main components introduced in the previous chapter. Due to limited access of the High Voltage lab in FREEDM caused by COVID-19, a virtual design is proposed for a 6kV, 100A test system.

The specifications of the Full Power Test circuit is listed in Table 4.1.

Table 4.1: Full Power Test Specification

Maximum DC Bus Voltage	6000V
DC Current	100A
Maximum input power	6kW

4.1 Super Cascode Power Module

The 6kV,100A Super Cascode Power Module [1] consists of two parallel strings of active switches where each string is made of 6 JFETs (USCi UJN1202Z) and a MOSFET (USM141) in series. The electrical and thermal characteristics of the module are summarised in the Table 4.2.

Table 4.2: SCPM Specifications

Rated Voltage	6kV
Rated Current	100A
Drain-Source ON resistance, $R_{DS\,ON}$	48mΩ
Thermal resistance (Junction to case)	0.45 C/W

The maximum voltage for continuous testing of the SCPM is chosen to be 5kV to resemble a real application circuit where a semiconductor switch is typically derated by 20% [13]. Figure 4.1 shows the test schematic of the SCPM in LTSpice where R_l is the load resistance and L_1 is the parasitic inductance of the SCPM module and V_{supply} is the DC power supply. The rest of the elements in the schematic from JFETs J1-J12 and M1, M2 form the Super Cascode, and resistors R1-R11, capacitors C1-C5 and diodes D1-D5 form the voltage balancing network for the cascode. A switching test at 5000V, 100A resistive load and 50% duty cycle is simulated to observe the switching characteristics under full load. Figure 4.2 and 4.3 show voltage and current waveform from LT Spice simulation where the module has a 21ns rise time and 47ns fall time of drain to source voltage.

This simulation is used to calculate the switching energy loss of each JFET in the SCPM string and Table 4.3 summarises the total switching loss (Turn on + Turn off) at JFET junction temperature of 25°C and 150°C. The total switching loss of the power module is two times the total loss in each string. The ON resistance of JFET J6 at $T_j = 150$°C is noted to be 55mΩ.

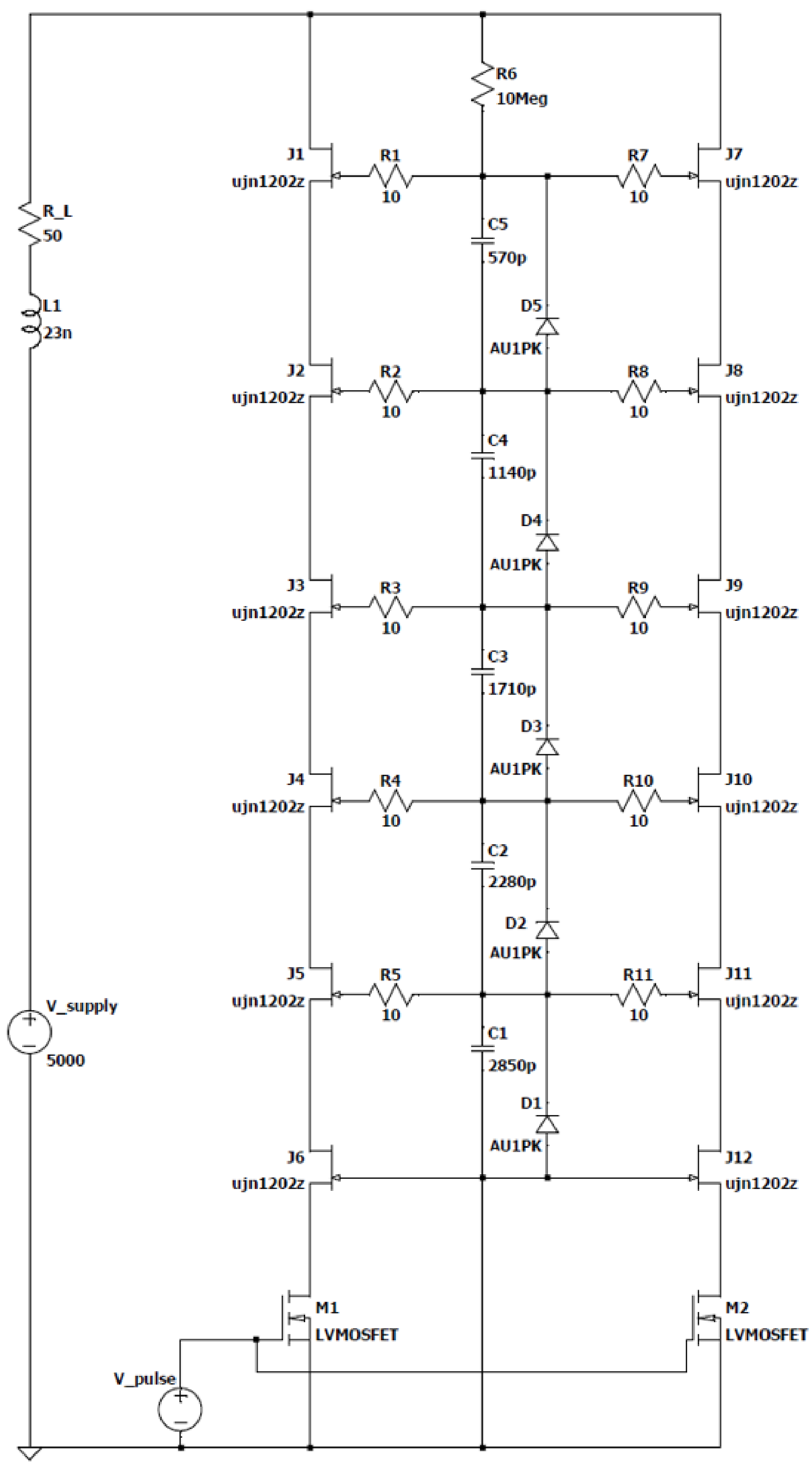

Figure 4.1: SCPM Test Schematic

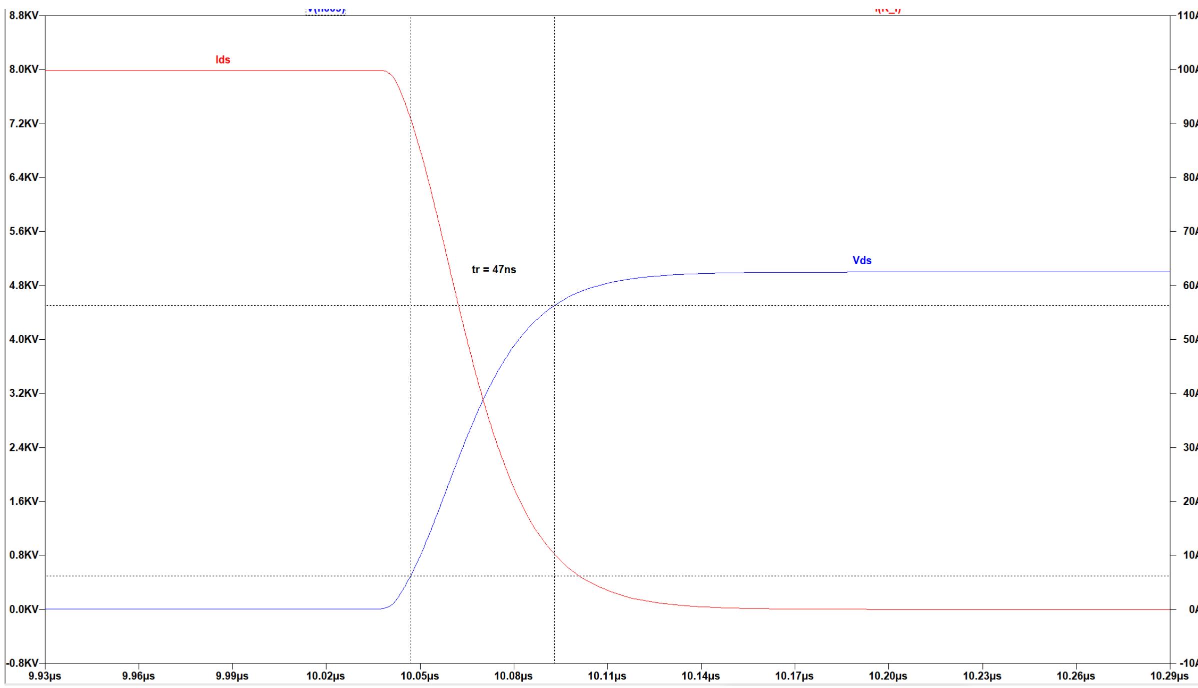

Figure 4.2: SCPM switching OFF time

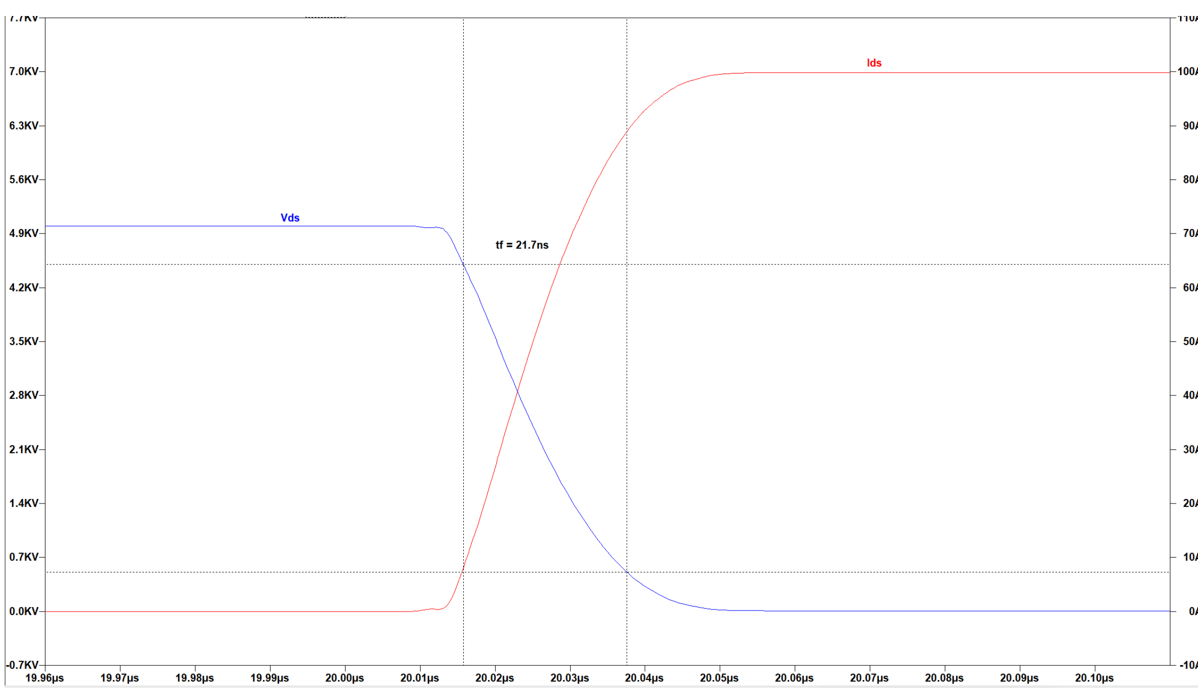

Figure 4.3: SCPM switching ON time

Table 4.3: Switching Loss Energy of SCPM string

Switching loss at 5000V, 100A							
	J1	J2	J3	J4	J5	J6	M
E_{sw} (μJ) at $T_j = 25°$C	227.7	433.2	596.6	715	820	800	5.1
E_{sw} (μJ) at $T_j = 150°$	269	427.8	591	718.3	812	791	6.55

The switching loss of JFETs does not change significantly with rise in junction temperature, however, the drain to source resistance increases by around 3 times.

Diode Module: The FPT has two diodes D1 and D2 that are specially fabricated to operate in the high voltage circuit. The diode module package is same as the SCPM package with four strings in parallel and each made of five CREE CPW51700Z050B 1700V, 50A diodes in series. The module is rated for 8.5kV, 200A.

4.2 Switching frequency

The selection of switching frequency for test is a user defined variable which allows one to test the SCPM at particular frequency that matches the intended application circuit. To design a cooling system for this test circuit, maximum power loss estimation of the SCPM is required. Considering the worst case test condition of 5000V,100A the following discussion details the maximum power loss in the module and highest frequency that the SCPM can switch at under this condition.

In steady state condition, the duty cycle of SCPM S2 is 0.5. From equation (3.2) the RMS current through S2 is $100 * \sqrt{0.5} = 70.7$A. Each module has two strings of identical elements, therefore it can be assumed that the current distribution in each string will be half of the total current (35.35A). The JFETs are placed in the module on a Cu/AlN/Cu Direct Bonded Copper (DBC) substrate with junction to case thermal resistance of 0.45°C/W [1]. The Table 4.3 shows from simulation that the switching loss in a single string are not equal and the loss increases from top JFET (J1) to bottom JFET (J6). It is also noted in [14] that due to the nature of the balancing circuit, JFET J6 thermally limits the module in current, voltage and frequency.

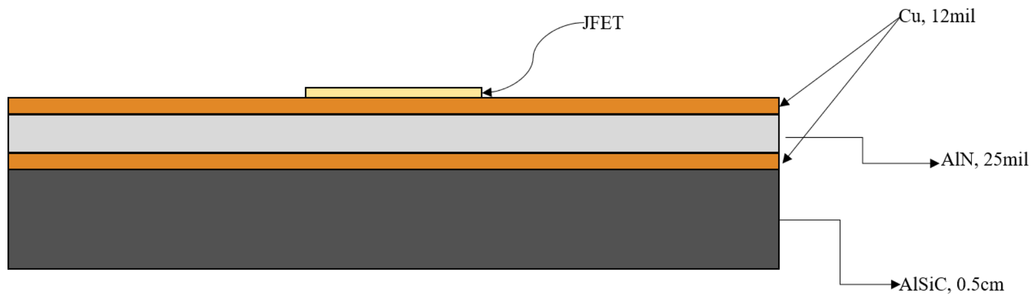

Figure 4.4: SCPM Cross section along J6

Figure 4.4 shows the cross section of the SCPM across JFET J6. Assuming the junction temperature of JFET J6 ($T_{j_{J6}}$) is limited to 150°C and the baseplate temperature (T_B) is held at 70°C by the cooling system, the maximum power dissipation under the J6 die is given by -

$$P_{max\,J6} = \frac{T_{j_{J6}} - T_B}{R_{th}} = 177.7W$$

where, $R_{th} = 0.45$°C/W is the thermal resistance from junction of J6 to baseplate. This power is the sum of switching loss and conduction loss of J6. The conduction loss can be calculated as -

$$P_{cond\,J6} = I^2_{RMS} * R_{DS\,150C} = 68.7W$$

where, $I_{RMS} = 35.35$A is the Root Mean Square current through JFET J6 and $R_{DS\,150C}$ =55mΩ is the ON resistance of J6 at 150°C

The maximum switching frequency can be calculated as-

$$P_{sw\,J6} = P_{max\,J6} - P_{cond\,J6}$$

$$f_{sw\,max} = \frac{P_{max\,J6} - P_{cond\,J6}}{E_{sw\,J6}} = 136kHz$$

where, $E_{sw\,J6}$ is the switching energy of J6 from Table 4.3

This is an approximate calculation of the maximum switching frequency of the module under full power. Other source of losses such as balancing circuit, gate drive and common mode current are not considered here. The SCPM was designed and Double pulse tested under the rated voltage and current conditions in [1] but not at continuous power and switching frequency. A 3-D lookup table with switching and conduction losses at different operating voltage, current and temperature is required to accurately model the SCPM circuit in steady state.

4.3 Inductor

The inductor is the main energy storage element in a Full Power Test System and its sizing depends on operating DC bus voltage and current ripple. From Section 3.1.1 it is known that during Mode 1 of the switching cycle, both switches Q1 and Q2 are turned ON. The inductor current rise is defined by the equation $V = L\frac{\Delta i}{\Delta t}$ where V is the voltage across the inductor, L is the inductance, ΔI is the ripple current and Δt is the time for which voltage is applied. The maximum voltage across inductor is equal to DC link voltage of 5000V DC. Ripple current is a design parameter which is chosen to be 5% of the 100A maximum test current. And the total overlap time between ON time of top and bottom switch can be chosen to set an inductance value. Since this a design parameter free to be chosen, it should be set to as low as possible to reduce the total inductance required, and therefore, reduce the inductor size and copper material requirement.

By trial and error method of selecting the overlap time, t_o it is observed from LT Spice simulation that a minimum t_o of $2(t_r + t_f)$ produces a good square wave with low distortions. This is used as a reference point to select $t_o = 200ns$ which gives the required inductance size as 200μH. The Fig 4.6 shows the results from a FPT LT Spice simulation with $200ns$ of overlap time where $V(a) - V(b)$ is the voltage across the inductor and $I(L1)$ is the current.

This inductor can be built using an air core in favor of ease of design process and lower

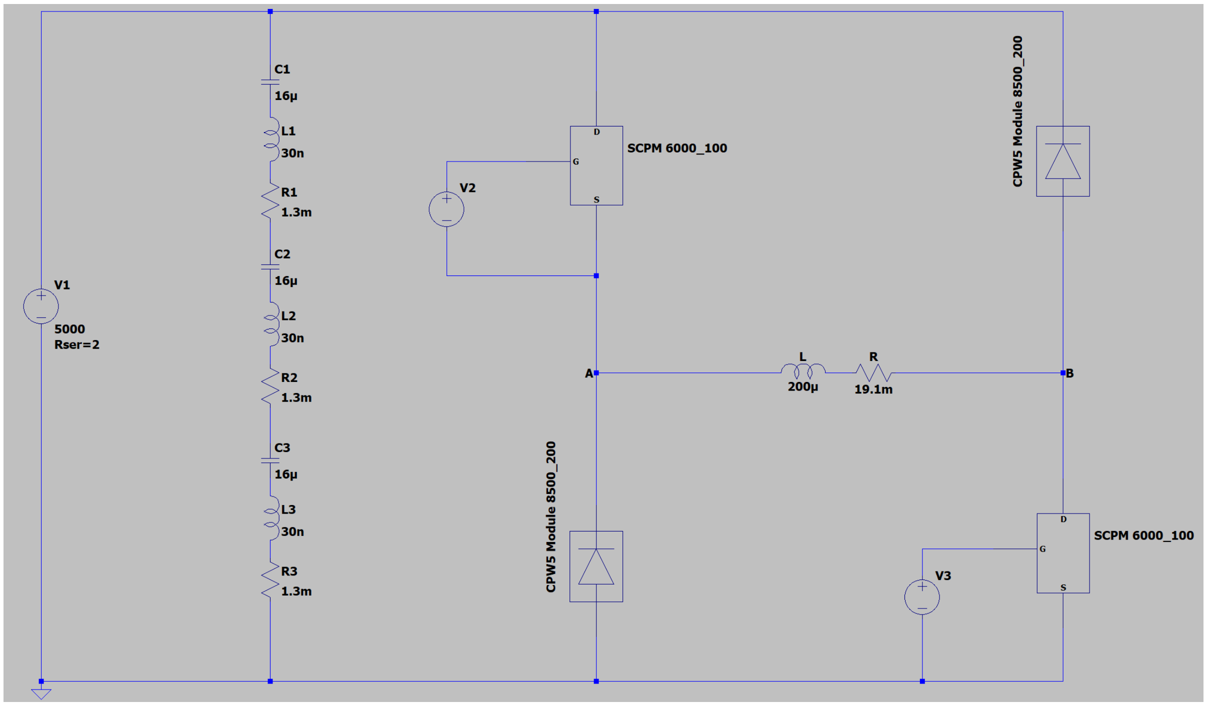

Figure 4.5: LT Spice Schematic of Full Power Test

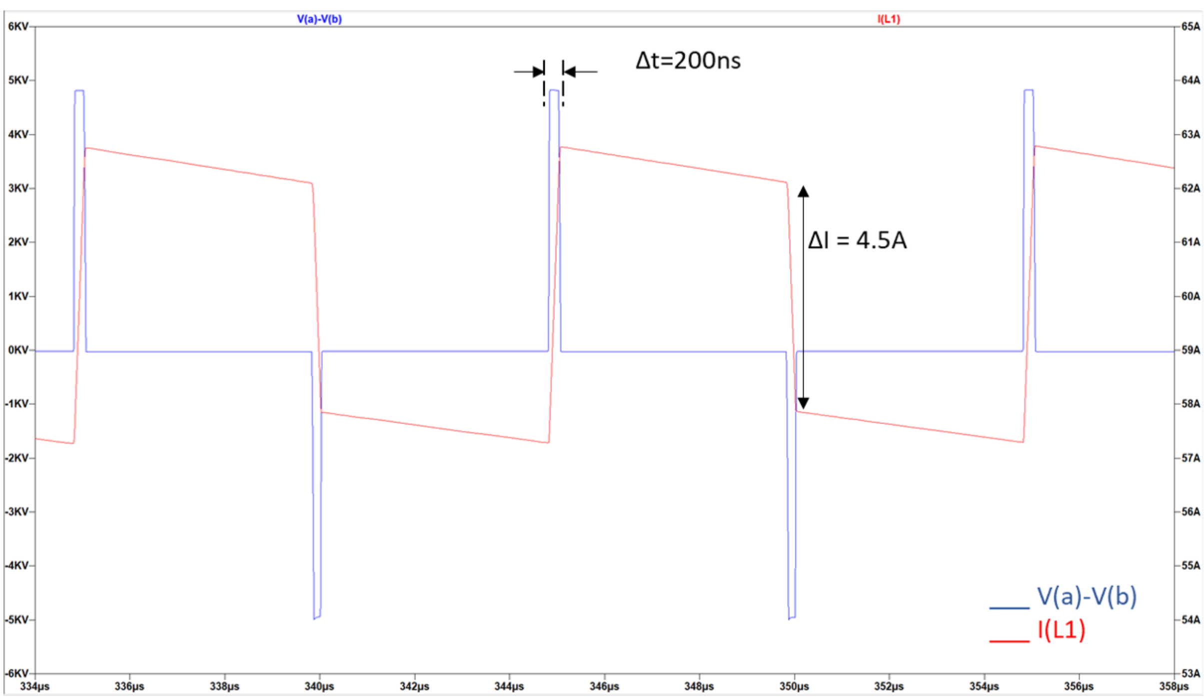

Figure 4.6: FPT Results from LT Spice

losses compared to magnetic core inductors. A Belden 37502 AWG 2 wire is chosen to build the air core inductor. This wire can carry upto $255A$ DC at 30°C ambient condition, the insulation can withstand a voltage of up to 7kV and the wire resistance is $0.16\Omega/1000ft$ [15]. The inductance required for test can be built as a single layer of coil by wrapping the wire around a bobbin like a plastic tube or similar non-magnetic structure for mechanical support. The inductance of a single layer air core inductor is approximated by Wheeler's formula [16] as

$$L = \frac{r^2 * n^2}{9r + 10l} \tag{4.1}$$

where, r is the radius of coil in inches, l is the length of coil in inches and n is the number of turns. Assuming the coil diameter of $40cm(15.7in)$, 28 turns of AWG 2 wire gives an inductance of $203\mu H$. The coil is assumed to be tightly wound with minimum or no gap between turns.

Finite Element Magnetic Method (FEMM 4.2) software [17] is used to simulate a 2-D cross section of the coil to verify the inductance estimated by Wheeler's formula. The software calculates the coil inductance using flux linkage and current density in the coil cross section. Figure 4.7 shows the cross section of the coil and its dimensions. Figure 4.8 from FEMM shows a coil inductance of 203μH with 29 turns thus confirming the initial estimate from equation (4.1). The coil requires 3.64 meters of wire length and the resistance will be approximately $19.1m\Omega$.

4.4 Capacitor

A DC link capacitor bank connected in parallel to the power supply provides the ripple current for the inductor and stores energy during re-circulation. The value of capacitance required can be calculated from equation (3.10). For a DC link voltage of $6000V$, peak current of $100A$ and allowable voltage ripple of 2%, a capacitance of $167nF$ is required. The

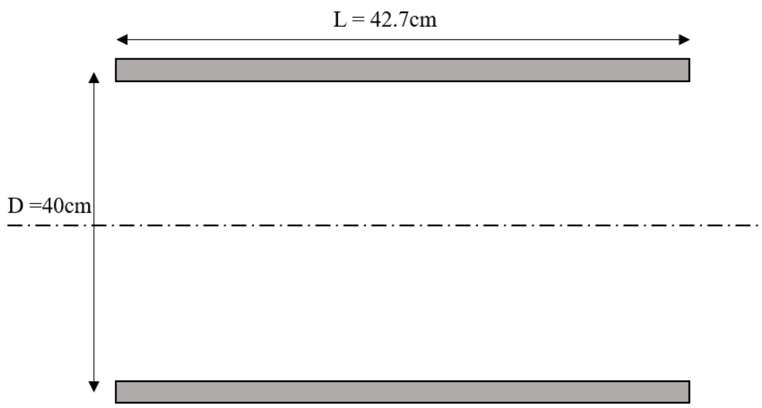

Figure 4.7: Inductor coil cross section

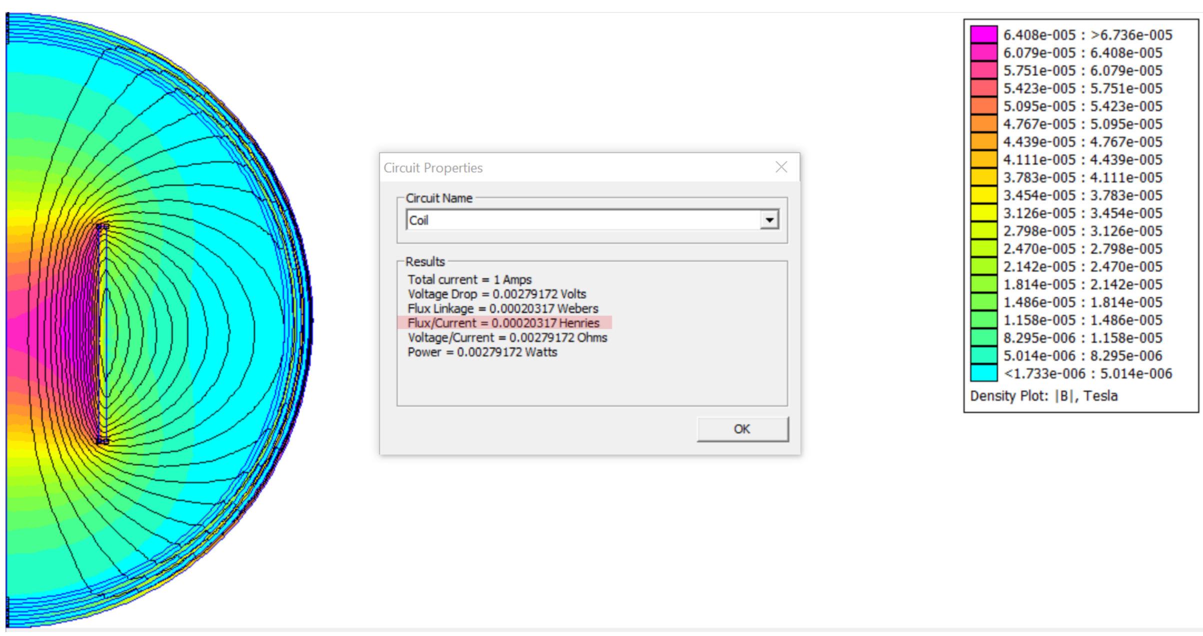

Figure 4.8: FEMM Simulation Results

capacitor should be able to supply RMS current of 20 A at $100kHz$ and have low equivalent series resistance (ESR). A film capacitor with the required capacitance with high voltage rating was not available readily. Therefore 3 capacitors LNK-P2X-16-220 from ICAR are chosen and connected in series to form a capacitor bank with total capacitance of $5.33\mu F$. The electrical properties of the selected capacitor are summarised in the Table 4.4[18]. The manufacturer specify a ±10% of tolerance on the capacitance values. This variation of capacitance in a series combination can result in voltage imbalance across the capacitors. Therefore it is recommended to connect a resistance R = 10/C in parallel to the capacitors [19]. Power resistors MG750 of $625k\Omega$, 10kV, 5W from Caddock Electronics are selected for voltage balancing[20].

Table 4.4: Capacitor Specifications

Attribute	Value
Capacitance	16 μF
Voltage rating	2200V DC
Maximum RMS current	45 A
Equivalent Series Inductance(ESL)	30 nH
Equivalent Series Resistance(ESR)	1.3 mΩ

4.5 Power supply

The power supply at the input acts as an auxiliary source which supplies power to compensate for the losses in the re-circulation circuit. It is sized based on the expected power loss in the circuit for a given test condition and oversized with some safety margin. The Table 4.5 lists all the estimated losses during peak test condition of $5000V, 100A$ and $136kHz$ switching frequency. Junction temperature of the all the devices are assumed to be at 25°C.

At steady state SCPM duty cycle $D = 0.5$, Inductor average current $I_{avg} = 100A$, RMS current through SCPM $I_{rms} = 70.7A$, ON resistance of SCPM $R_{ds} = 48m\Omega$, Diode module forward voltage $V_f = 1.6V * 5$ (5 diode in a string), DC resistance of Inductor $R_l = 19.1\text{m}\Omega$.

From equation (3.2)-(3.8), device datasheet and LT Spice simulation results in Section 4.1 the losses are estimated.

Table 4.5: Estimate of maximum power loss during test

Component	Power (W)
SCPM switching loss	2030
SCPM conduction loss	480
Diode conduction loss	800
Inductor R-L loss	191
Total Loss	3501

A $6kW, 8kV$ Magna XR series power supply with 2U rack mount form factor is chosen for test. The supply is oversized to accommodate for unaccounted losses and expand test system capability to higher power modules in the future.

CHAPTER

5

VIRTUAL TEST SETUP

This chapter discusses the design of a current controller, cooling system, bus bars and assembly of all the components to form the Full Power Test system.

5.1 Current control

This section introduces the design of current controller for the Full Power Test circuit. The steady state operation can be described by four switching instances as discussed in Section 3.1.1 and identified in the Figure 5.1. Power electronic circuits are commonly modelled using small signal approximation and state space averaging, but this method of analysis is not applicable to ERSC circuits since they are not normally loaded like other power electronic circuits [21].

Figure 5.1 shows the circuit waveform where Q1 and Q2 are switched at duty cycle D1 and D2 respectively. Assume the sum of duty cycles is equal to 1 and there is initial current $I_m in$ in the inductor. The phase shift ϕ between D1 and D2 controls the ripple current at every switching instant as defined by

$$\frac{(D1-\phi)*Ts*E}{L}$$

where E is the DC link voltage. The average voltage across inductor in each cycle is zero therefore the average current remains constant.

Consider a second case with $D_1 + D_2 > 1$ where D1 is 0.5 and D2 is 0.6. Figure 5.2 show the increase in average inductor current after every switching cycle. From the switching circuit modes and the waveform, it can be observed that the current in inductor effectively depends on average voltage across nodes A and B defined as,

$$< V_{AB} >= |D_1 - D_2|E$$

The FPT circuit can be modelled as a simple inductor connected to a pulse width modulator that produces voltage pulses. The current ripple is controlled by an independent variable called ϕ which does not affect the control loop. For test purposes, the lower device Q2 is selected as Device Under Test and its duty cycle is maintained constant and duty cycle of switch Q1 is controlled by a closed loop current controller.

Figure 5.4 shows the current control block diagram of the FPT circuit. A summation block compares a reference current and the inductor feedback current to produce an error signal $i_e(t)$. The current feedback is obtained from a current sensor with gain H. The compensator blocks converts this error signal to a control signal $d(t)$. The compensator Gc is a PI controller defined as

$$G_c = G_{c0} * (1 + \frac{\omega_l}{s})$$

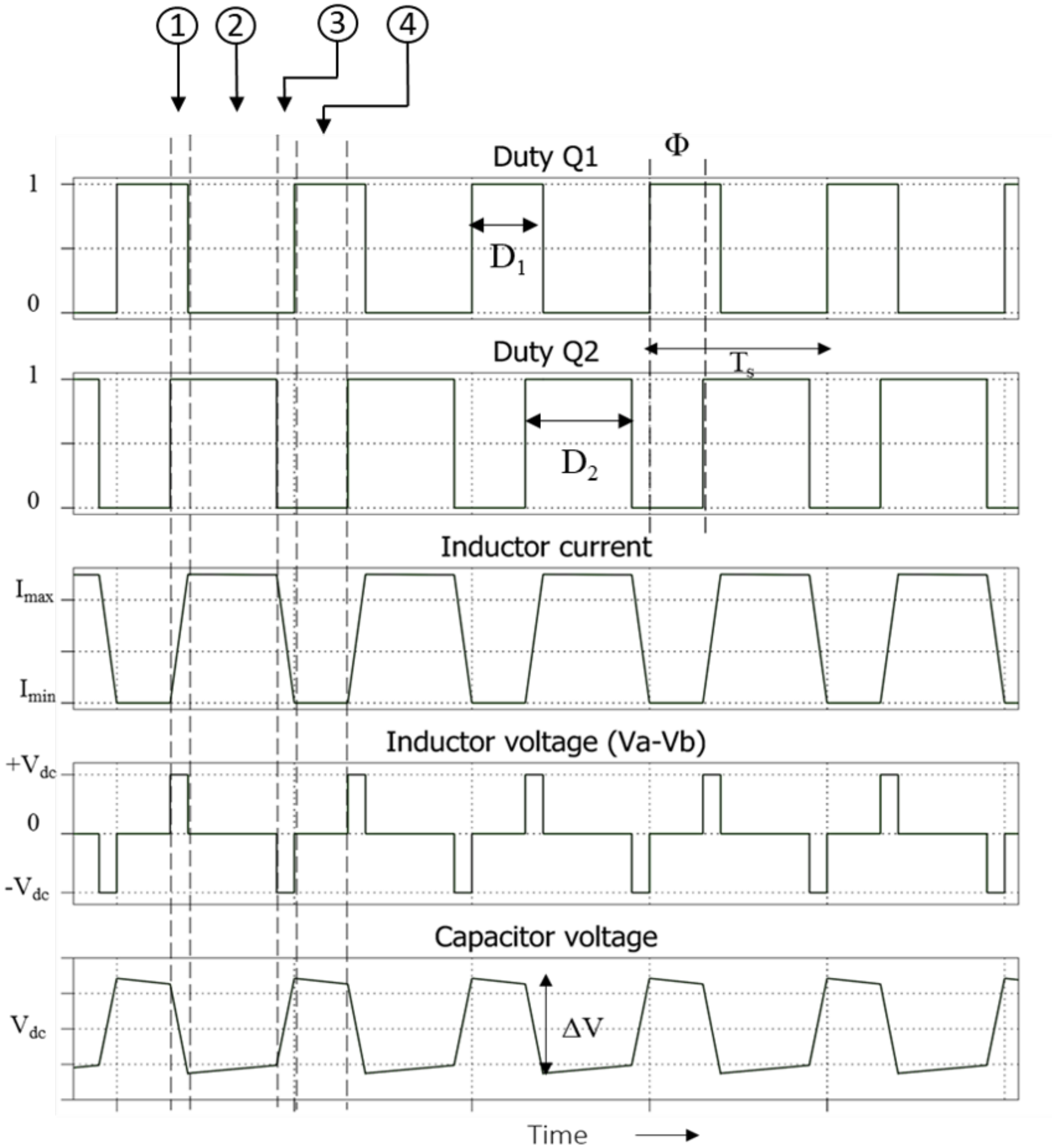

Figure 5.1: Circuit waveform with $D_1 + D_2 = 1$

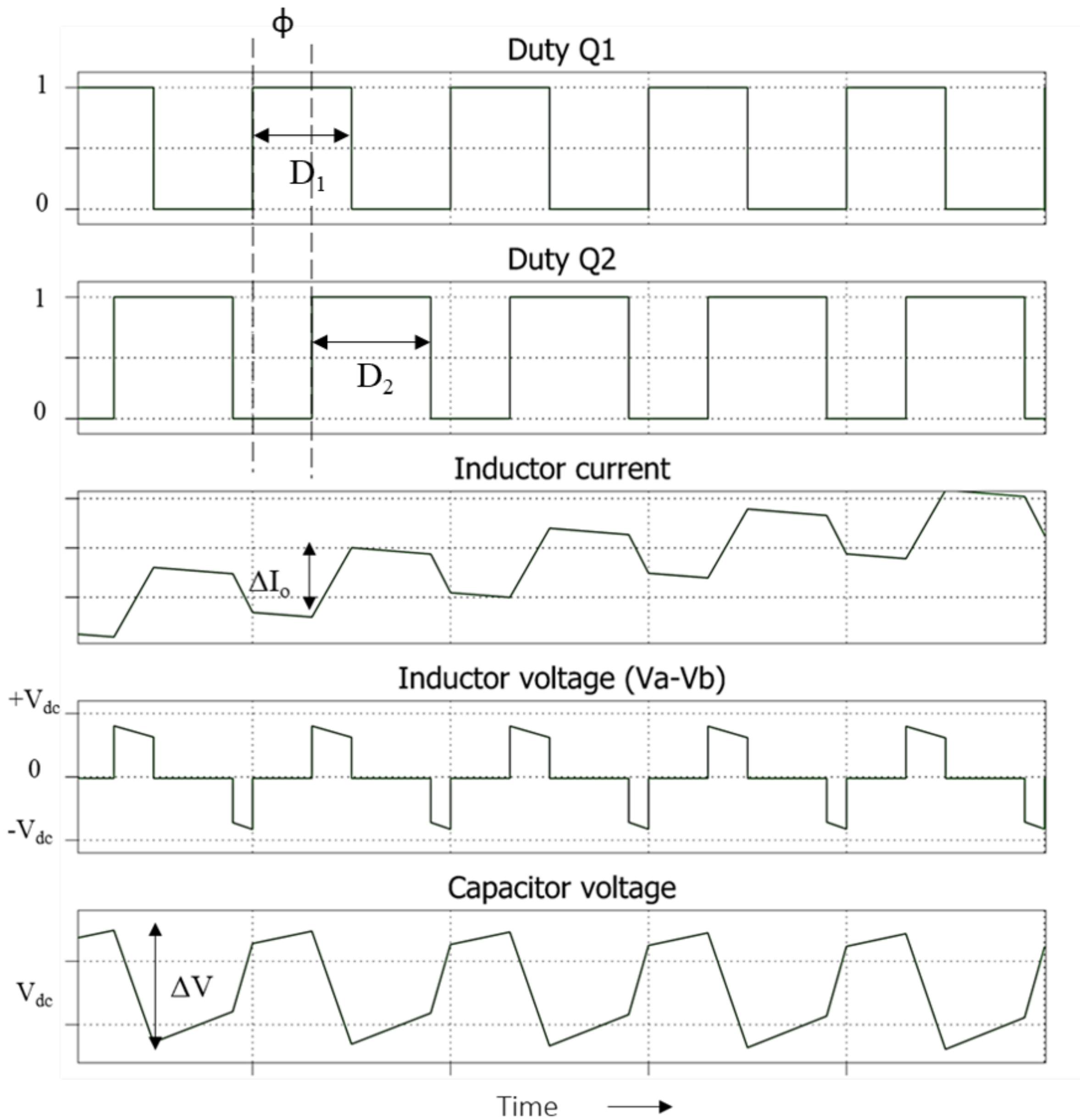

Figure 5.2: Circuit waveform with $D_1 + D_2 > 1$

where G_{c0} is the DC gain and ω_l is the compensator pole. Figure 5.3 shows the block diagram of the Pulse Width Modulator(PWM) where input signal $d(t)$ is compared with a sawtooth waveform of frequency f_s. The gain of PWM block is defined as E/V_{ramp} where E is the DC link voltage and V_{ramp} is the peak voltage of sawtooth waveform.

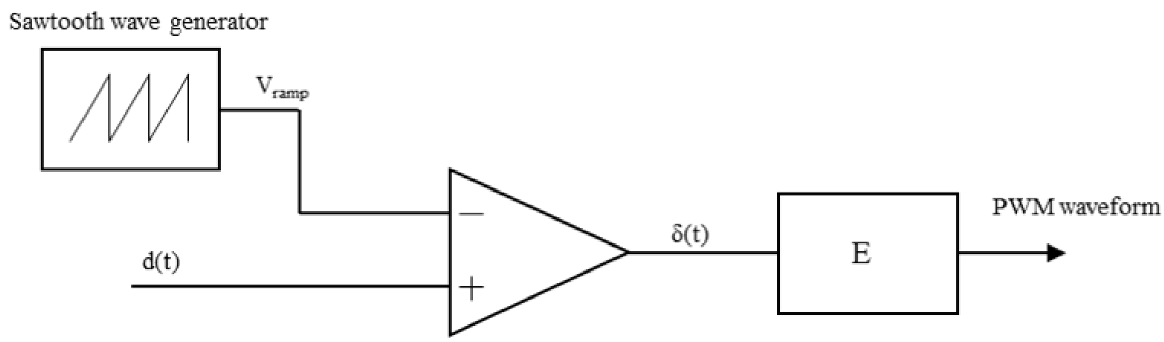

Figure 5.3: Pulse Width Modulator Block diagram

The circuit model, G is defined as $1/(sL+R)$ where s is the Laplace transform variable, L is the inductance and R is the resistance of coil.

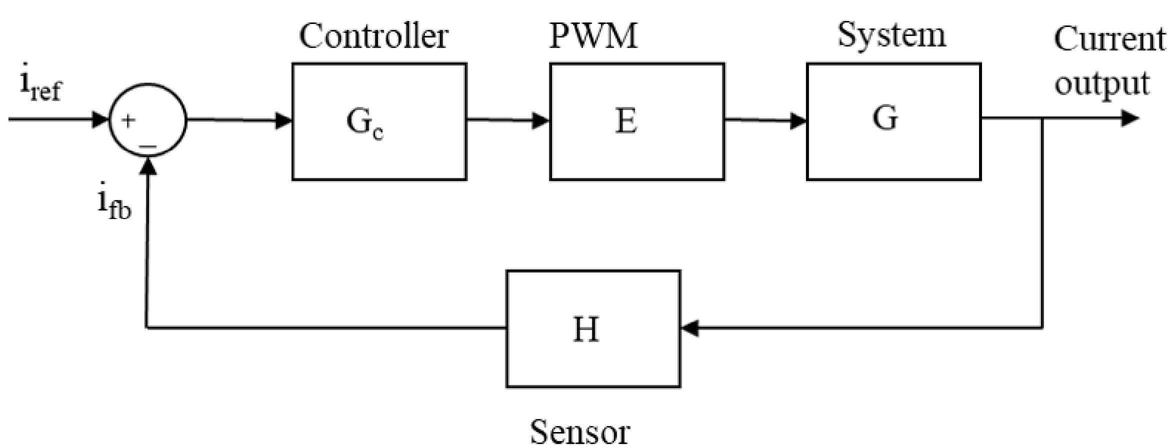

Figure 5.4: Current control block diagram

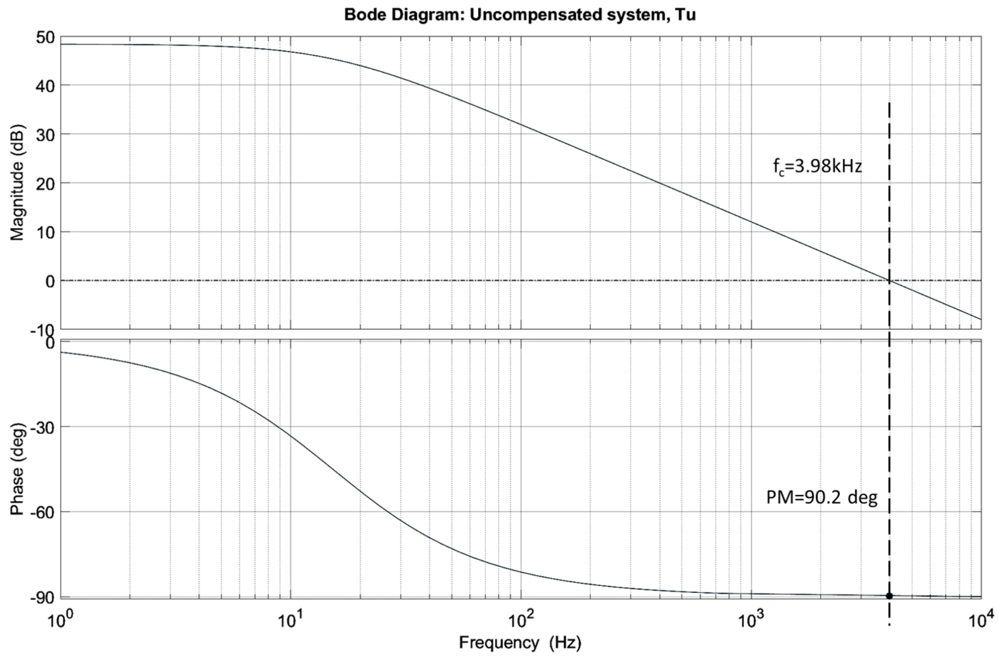

Figure 5.5: Bode Plot: Uncompensated loop

The compensator design process begins with defining the system loop gain as

$$T_{loop} = \frac{G_c * E * G * H}{V_{ramp}}$$

Based on the components designed in Chapter 4 and current sensor selected (detailed at the end of this section), $L = 200\mu H$, $R_l = 19.1m\Omega$, $H = 1/1000$, $E = 5000$ and $V_{ramp} = 1$. The uncompensated system loop gain is defined as:

$$T_{loop\,UC} = \frac{T_u}{1 + s/\omega_o} \tag{5.1}$$

where, $T_u = E * H/R$ and $\omega_o = R/L$. Figure 5.5 shows phase and magnitude plot of $T_{loop\,UC}$ with a low frequency gain of $48.3dB$ and the crossover frequency at $3.98kHz$.

Assuming the lowest switching frequency of test at $10kHz$, a loop crossover frequency of $1kHz$ is required for the compensated system. The compensated system equation can be written as:

$$T_{loop} = \frac{G_{c0} * H * E}{R} * \frac{1}{(1 + s/\omega_o)} * (1 + \omega_l/s)$$

At high frequency when $\omega/\omega_o >> 1$ and $\omega_l/\omega << 1$ the transfer function can be approximated to

$$T \approx \frac{T_u * G_{c0}}{f/f_o}$$

At the new crossover frequency $f = f_c$,

$$T(s) \approx 1$$

$$\frac{T_u * G_{c0}}{f_c/f_o} = 1$$

$$G_{c0} = \frac{f_o}{T_u * f_c}$$

For $f_c = 1kHz$, $f_o = 15.1Hz$, $T_u = \frac{5000}{1000*19.1*10^{-3}} = 261.78$

$$G_{c0} = 0.2513$$

The pole of compensator, ω_l, is placed at frequency ten times lower than crossover frequency so as to not reduce the phase margin.

The compensated bode plot and startup response of FPT is shown in 5.6 and 5.7 respectively. This controller is tuned for a DC link voltage of 5000V and its coefficients must be recalculated when DC link voltage changes.

A current transducer, IT-200-S from LEM is selected for sensing the inductor current. It has a bandwidth of $150kHz(-3dB)$ and sensing range of up to $200A$ peak and a gain of 1/1000 [22].

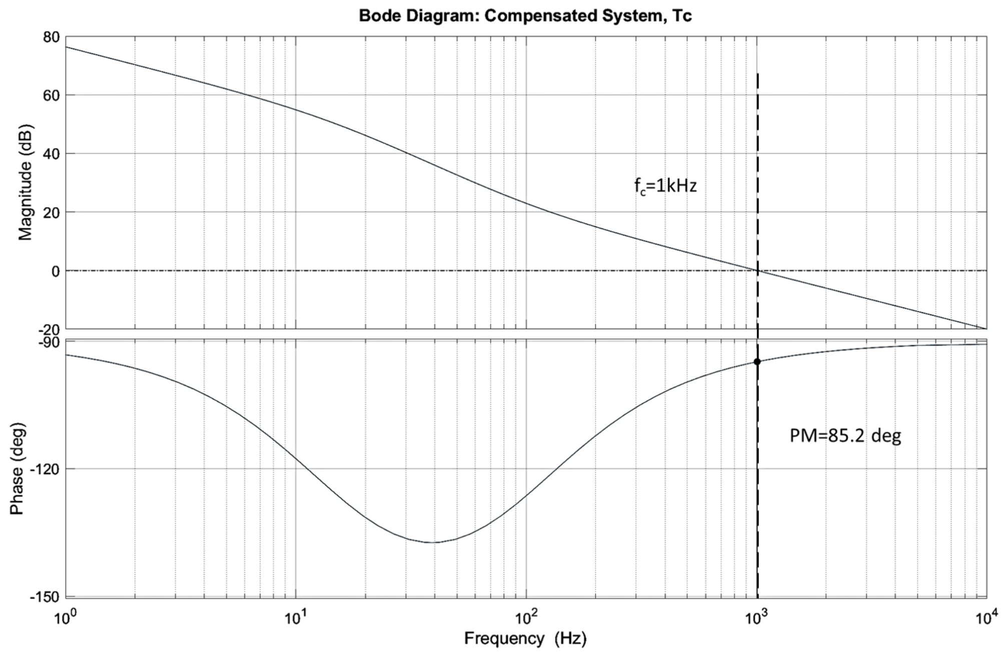

Figure 5.6: Bode plot of Compensated system

5.2 Cooling system

This section explores the design of a cooling system for the Full Power Test circuit. The total power loss in each SCPM at a test condition of 5kV, 100A and 136kHz switching frequency is approximated to be $1015W$ of switching loss and $240W$ of conduction loss. Similarly, each diode module has 400W of conduction loss. The cooling system consists of two cold plates and a heat exchanger where each cold plate holds an SCPM and a diode module.

Fig 5.8 shows the single line diagram of the water cooling system where two cold plates are connected in parallel in a closed loop. The pump pushes the water against the friction loss in pipes and pressure loss in the components at a constant flow rate. A heat exchanger cools the heated water with copper coils and powerful fan. The total heat to be removed from each cold-plate is 1655W but the system is oversized assuming $2000W$ of heat per plate.

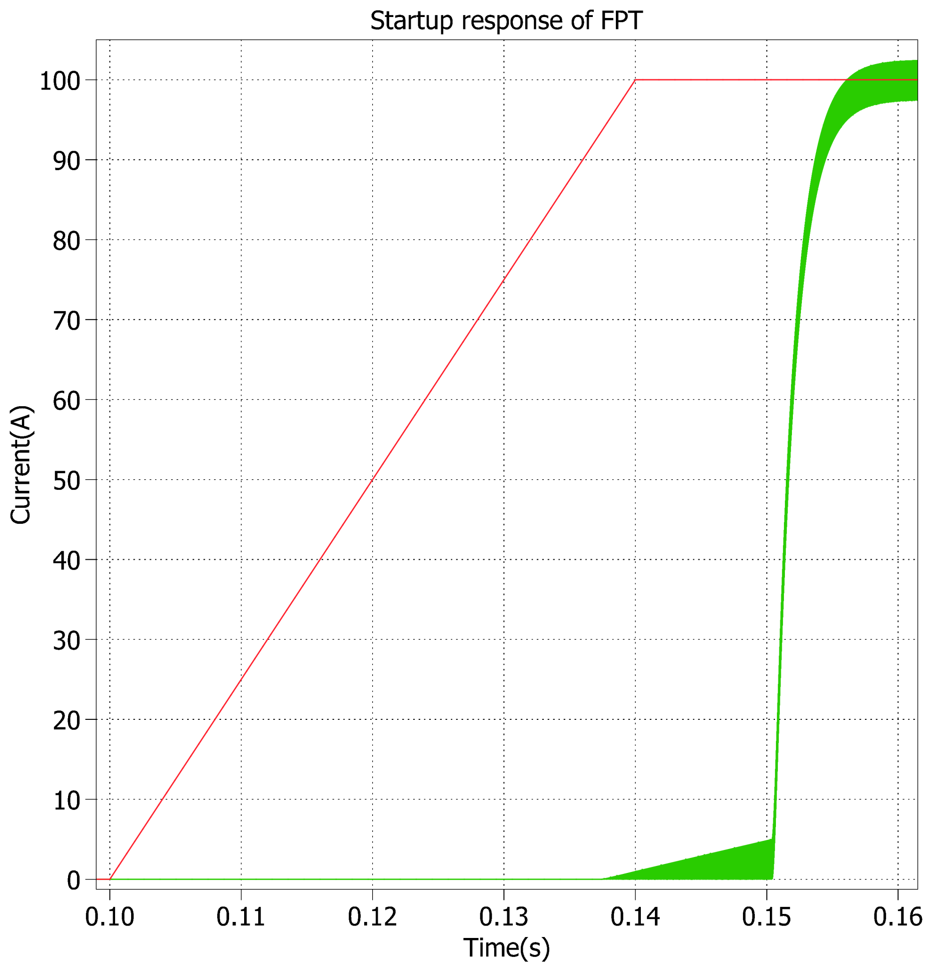

Figure 5.7: Startup response for Step input

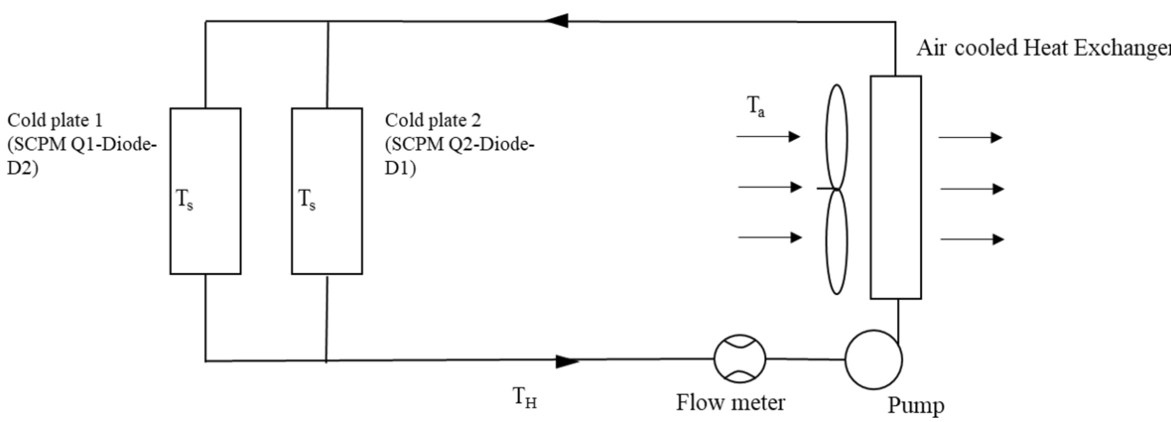

Figure 5.8: Cooling system

The thermal resistance of the cold plate is defined as

$$\Theta_{CP} = \frac{T_s - T_H}{Q} \tag{5.2}$$

where, $T_s = 70°C$ is surface temperature of cold plate, T_H is the temperature of water coming out of the cold plate and *Q=2000W* is the total heat absorbed in the cold plate. The hot water from both cold plate outlets is mixed before entering the heat exchanger. The thermal resistance of the heat exchanger can be defined as

$$\Theta_{HX} = \frac{T_H - T_a}{2Q} \tag{5.3}$$

where, $T_a = 25°C$ is the ambient room temperature. Similary, the thermal resistance of the system can be defined as

$$\Theta_{sys} = \frac{T_s - T_a}{2Q} = 0.01125°C/W \tag{5.4}$$

From Equation 5.2, 5.3 and 5.4 the relation between thermal resistances can be derived as

$$\Theta_{sys} \leq \frac{\Theta_{CP}}{2} + \Theta_{HX}$$

For the cooling system to work, thermal resistances of the elements should be selected such that is satisfies the above equation.

A cold plate ATS-CP-1001-DIY from Advanced Thermal Systems is selected which has a thermal resistance of *0.0062 C/W* at 1GPM (gallon per minute) of fluid flow and a total area of $45.11 sq.in (198 mm X 147 mm)$ that can house the two power modules on it [23]. The two power modules cover a total area of $29.72 sq.in (137 mm X 70 mm X 2)$ on the cold plate. Assuming uniform heat dissipation from the modules, the effective cold plate resistance can be obtained by normalizing with total area as

$$\Theta_{CP} = 0.0062 * \frac{Total\ plate\ area}{Heating\ element\ contact\ area} = 0.00941°C/W$$

A heat exchanger ATS-HE-25 is selected which has a thermal resistance of *0.00588 C/W* at 2GPM [24]. A *1/2 inch* diameter PVC tube from Swagelok is used to connect all the systems in the cooling loop. From the SolidWorks assembly of the system, it is estimated that a total of *10.4 feet* of PVC tube will be required to connect the water loop.

A positive displacement type water pump is required for this closed loop cooling application. The size of pump depends on the total friction losses in the pipes and pressure drops in the connected equipment (cold plate and heat exchanger). The cold plate and heat exchanger each drop $0.85psi$ (pounds per square inch) and $4psi$ respectively [23],[24]. The total pressure drop per feet of pipe P_d, can be estimated using Hazen-Williams equation[25].

$$P_d = \frac{4.52 * Q^{1.85}}{C^{1.85} * D_h^{4.86}} \tag{5.5}$$

where Q is the fluid flow rate (GPM), C = 155 is the friction factor coefficient of the PFA pipe [25], D_h is the inner diameter of pipe. This equation estimates a 0.217 psi friction loss in the pipe. Therefore the total pump capacity should be at least equal to sum of pressure drops in the loop.

A 18V BLDC (Brushless DC) pump INTG3-560 series from GRI pumps is selected. It has $9psi$ of pumping capacity at 2GPM which is sufficient for this application. A flow meter from Advanced Thermal Systems is also attached at the exit of the heat exchanger to monitor water flow rate.

5.3 Bus bar design

A bus bar design and analysis for the Full Power Test Circuit is detailed in this section. Parasitic inductance of the path in a switching loop can cause an overvoltage across the switching element as defined by

$$V_o = L_p * \frac{di}{dt}$$

The important electrical parameters of the bus bar are its Resistance, Inductance (self and mutual) and Capacitance. The self inductance of a bus bar of length l, width w, and thickness t can be calculated using the equation[26]

$$L_{self} = 2l(\log(\frac{2l}{w+t} + 0.5 + 0.2235(\frac{w+t}{t}))) * 10^{-7} \tag{5.6}$$

The mutual inductance of two bars placed d distance apart with insulating material in between them and carrying currents i_1, i_2 is calculated as [27]

$$L_{mutual} = \frac{\mu_0 \mu_r l t}{\pi\sqrt{4(d+t)^2 + kw^2}} cos\phi \tag{5.7}$$

where, μ_0 and μ_r is the permeability of vacuum and insulating material respectively, ϕ is the angle between direction of currents and k is the correction coefficient.

Figure 5.9 shows a circuit of the Full Power Test with parasitic inductances from the bus bar. L_p and L_n are the inductance of the postive and negative terminals connecting DC link capacitors to the switch legs (Q1-D1). $L_{bus1}, l_{bus2}, l_a, l_b$ are the inductances of the paths between the switch legs as indicated in the figure.

Authors in [26] have presented a comprehensive guideline to bus bar design which is used for this design. Figure 5.10 shows the layout of bus bar connecting the power modules to DC link capacitor. The layer in blue (P_p) is the positive V_{dc} bar that connects drain of Q1, cathode D2 and positive terminal of capacitor. The red layer (P_n) connects to negative terminal of capacitor, source of Q2 and anode of D1. The two separate straight bars (P_a, P_b)

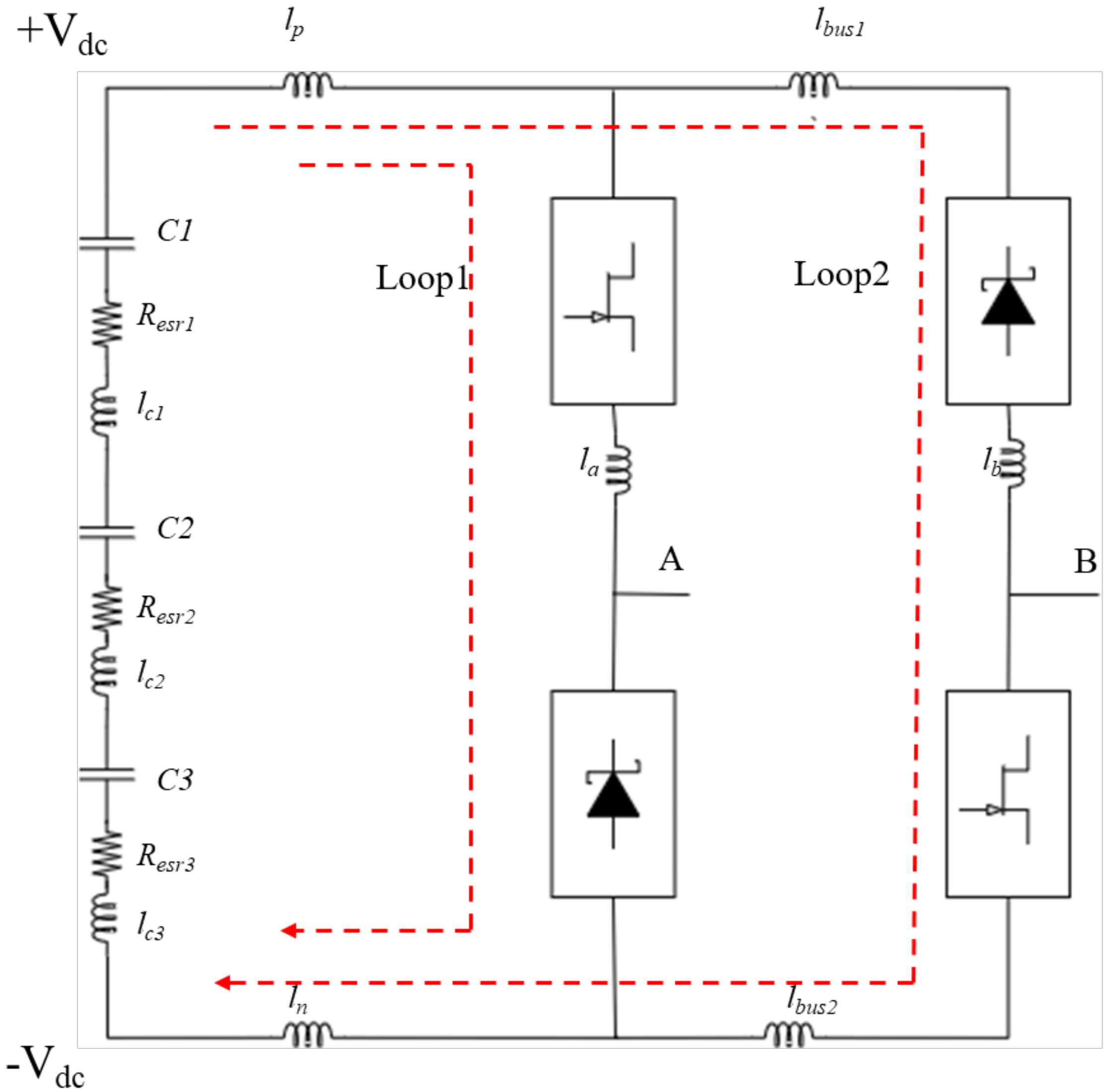

Figure 5.9: Parasitics in Full Power Test circuit

in yellow form nodes A and B which connects to load inductor.

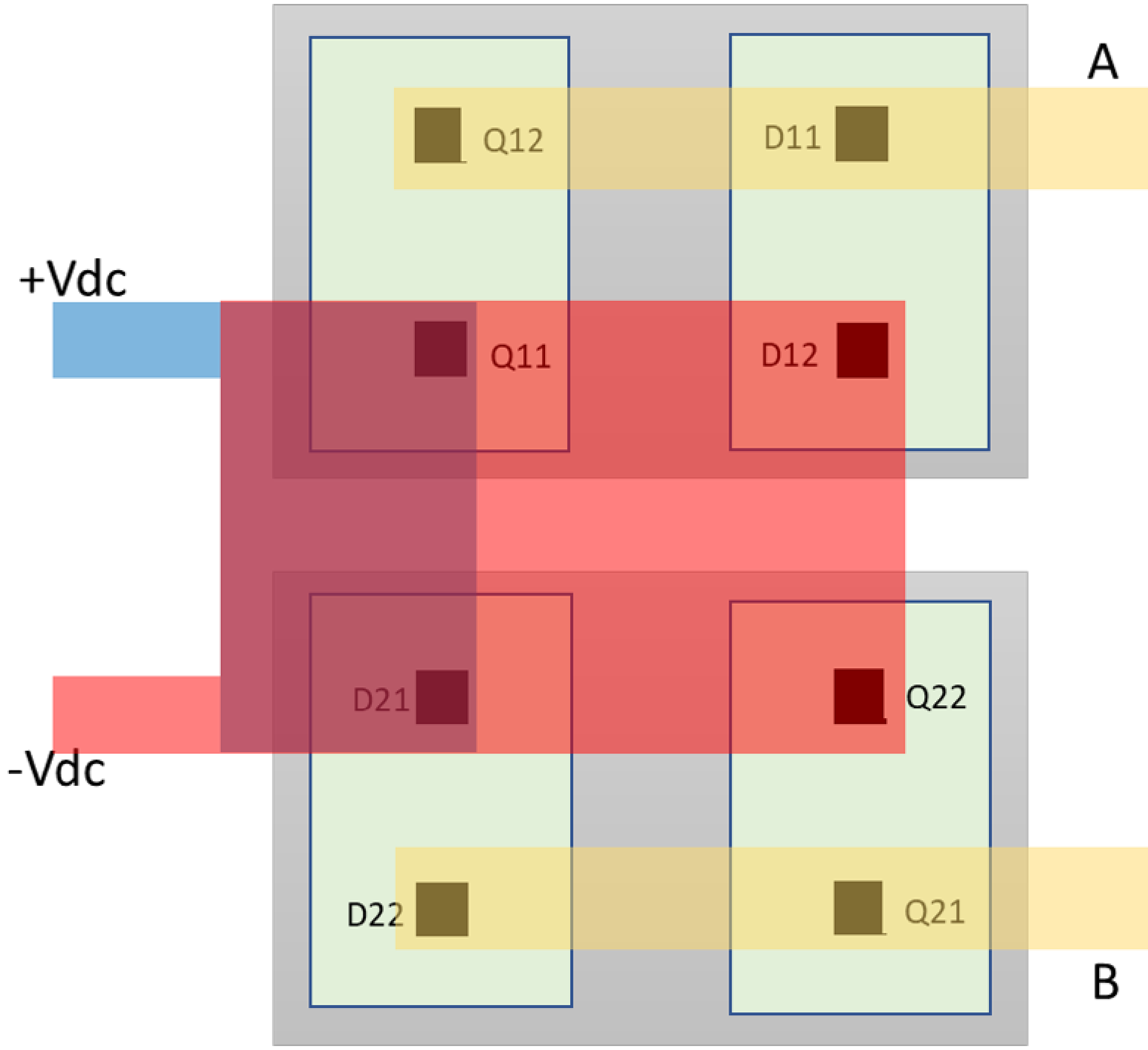

Figure 5.10: Bus bar layout for FPT

A low inductance bus bar can be obtained by having greater overlap area between bars carrying currents in opposite direction [28]. The separation between bus bars should be as small as possible to get maximum flux cancellation during overlap [29]. Also, having thicker and wider bars will reduce self inductance.

The components are assembled in the orientation as shown in Figure 5.10 and the bus bars are designed in SolidWorks. The minimum thickness of the bar is defined by the amount

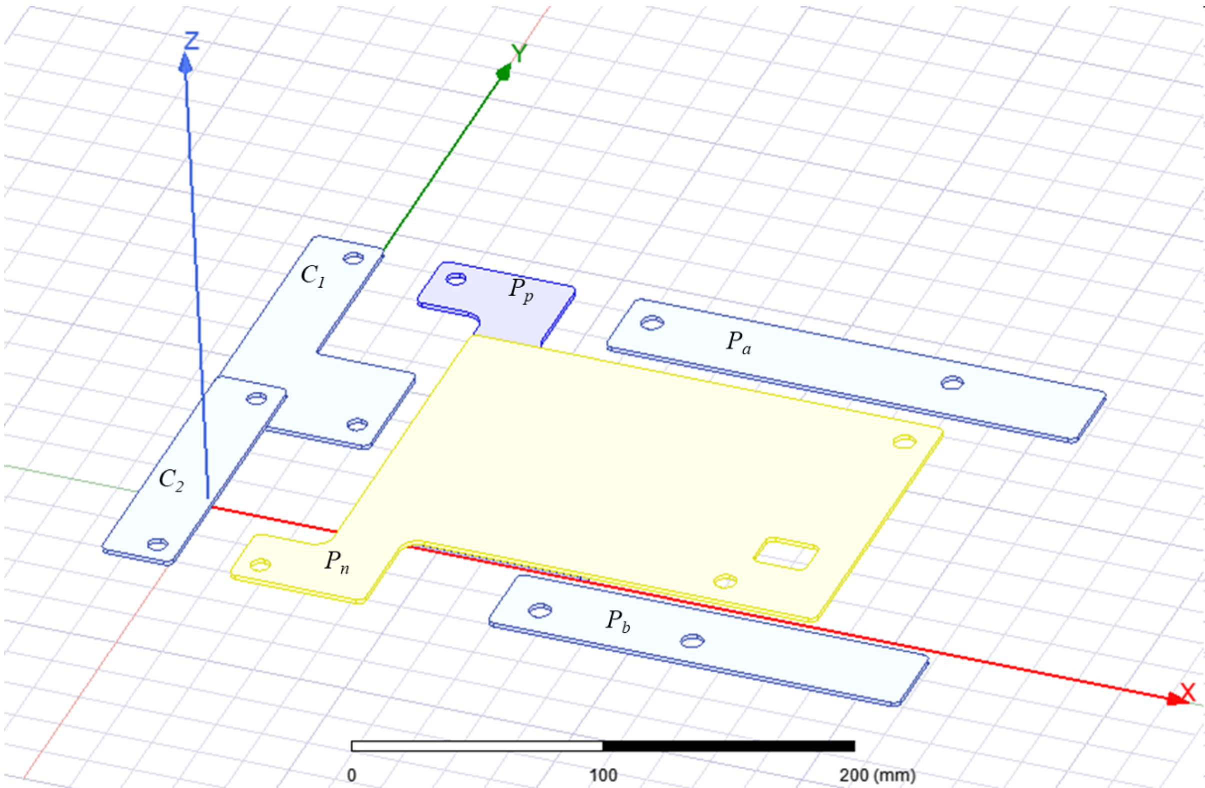

Figure 5.11: Bus bar layout in Q3D

of current without exceeding the maximum working temperature of the dielectric. Reference [30] provides bus bar ampacities of typical sizes of conductors for $30°C$ rise in temperature over ambient. According to the standard ratings of copper No.110, a $1/16in(1.5875mm)$ thick and $3/4in$ wide piece of copper can handle up to $105A$ DC current. This is selected as the starting point for thickness of plate in the simulations. A rule of thumb for good bus bar design is to have current density (J) lower than $5A/mm^2$[31]. Figure 5.11 shows the busbar assembly in Q3D where C_p and C_n are the sections which connect capacitors $C1, C2$ and $C2, C3$ respectively.

Ansys Q3D is used to calculate the parasitic inductance and current density in the bus bars. The thickness of bus bar is increased from $1/16in.(1.5875mm)$ to $2mm$ to ensure the current density is lower than $5A/mm^2$. The sharp edges are rounded off to avoid high electric field concentration and eddy current heating losses. The insulation layer thickness between the bus bars should be minimised to get better mutual inductance coupling[29] but should also electrically isolate them from each other. Common choices for insulation are Nomex, Mylar, Tedlar, Kapton, epoxy powder coating. A $5mil$ Kapton layer is selected as insulation between plates P_p and P_n of the bus bar assembly. It has $5000V/mil$ of dielectric withstand capacity and working temperature up to $400°C$ [32].

The inductance of Loop 1 defined as $l_p + l_a + l_n$ is simulated by replacing SCPM Q1 and diode D1 from bus bar assembly with short circuit using copper bars. Similarly, inductance of Loop 2 formed by P_p, P_n and P_b is defined as $l_p + l_bus1 + l_b + l_bus2 + l_n$ and simulated at 20MHz. Table 5.1 summarises the AC inductance of the different parts of bus bar assembly.

Table 5.1: Partial inductance of bus bars

Entity	Inductance (at 20MHz)
$Loop1$	$154.97nH$
$Loop2$	$149.27nH$
l_a	$50.43nH$
l_b	$18.42nH$
C_p	$45.24nH$
C_n	$41.61nH$

The total inductance of DC link capacitor section is, $L_dc = l_{c1} + l_{c2} + l_{c3} + C_p + C_n = 176.85nH$, where C_p and C_n are the inductances of copper segments that connect the capacitors. Figures 5.12 and 5.13 shows current density plots for bus bar P_p and P_n at worst case condition of $100A$ DC. The normal operating current in the bars is around $20A$ RMS. This simulation is carried out under constant current and does not include skin effect. The plots provide feedback about current distribution in the bus bar and helps in iterative design process. It can be seen from the figures that the maximum current density stays well below the limit of $5A/mm^2$. This confirms the bus bar is capable of carrying the required current under the required conditions.

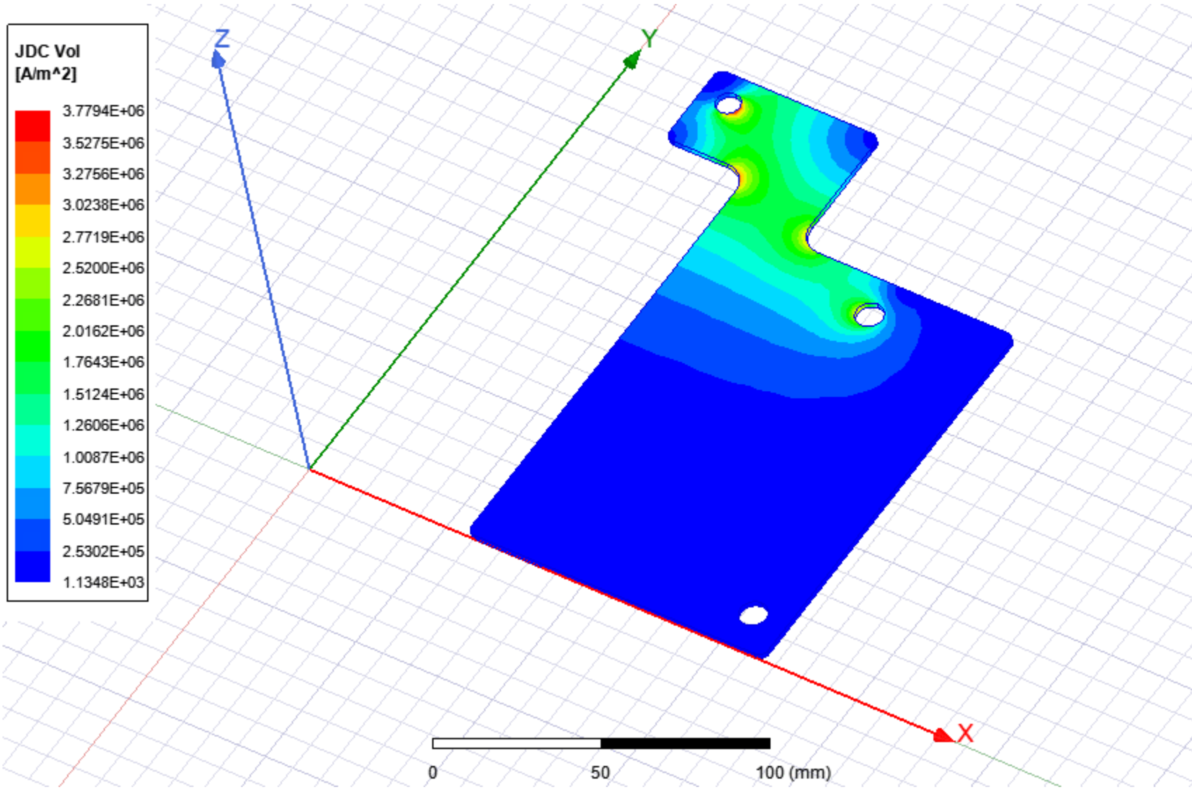

Figure 5.12: Current density plot of plates P_p at 100A DC

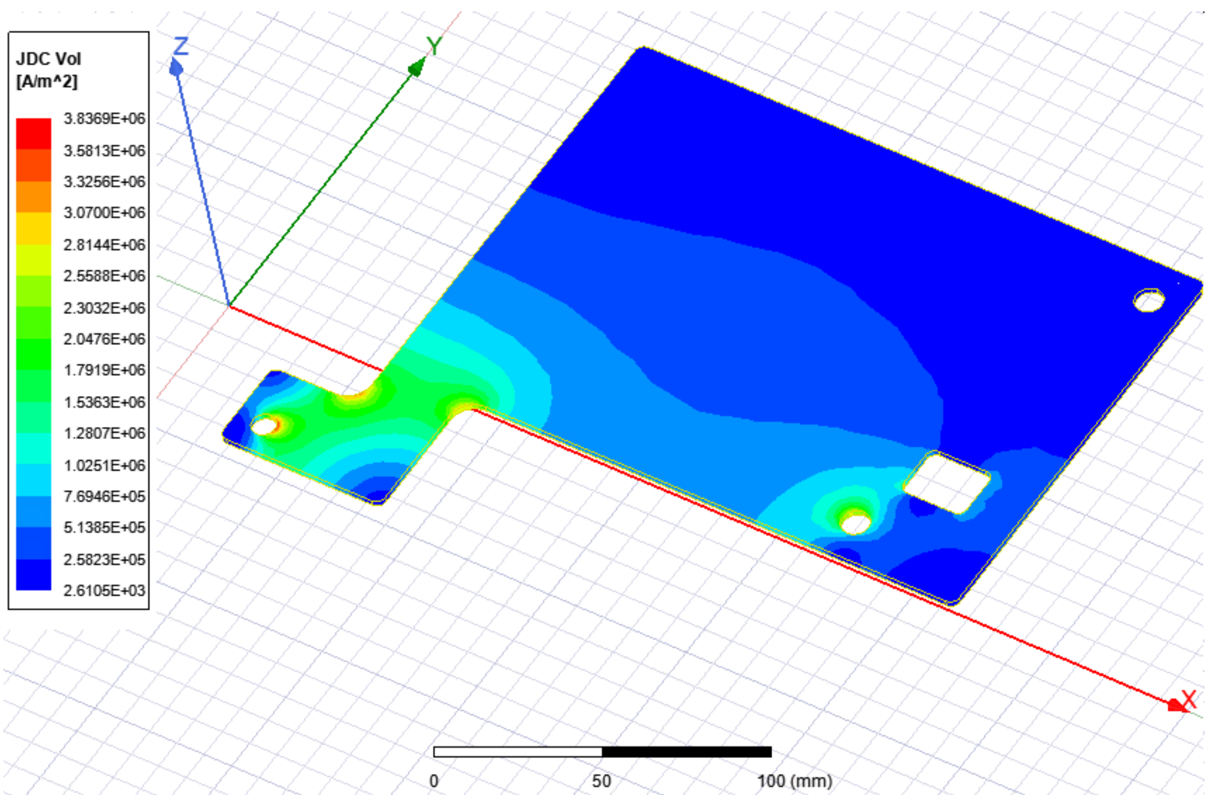

Figure 5.13: Current density plot of plates P_n at 100A DC

5.4 System Assembly

Figure 5.14 shows a SolidWorks assembly of the Full Power Test System. The heat exchanger and pump is placed on ground level and the cold plates are about $59cm$ above the ground. A server rack frame can be used to mount the plates and capacitor.

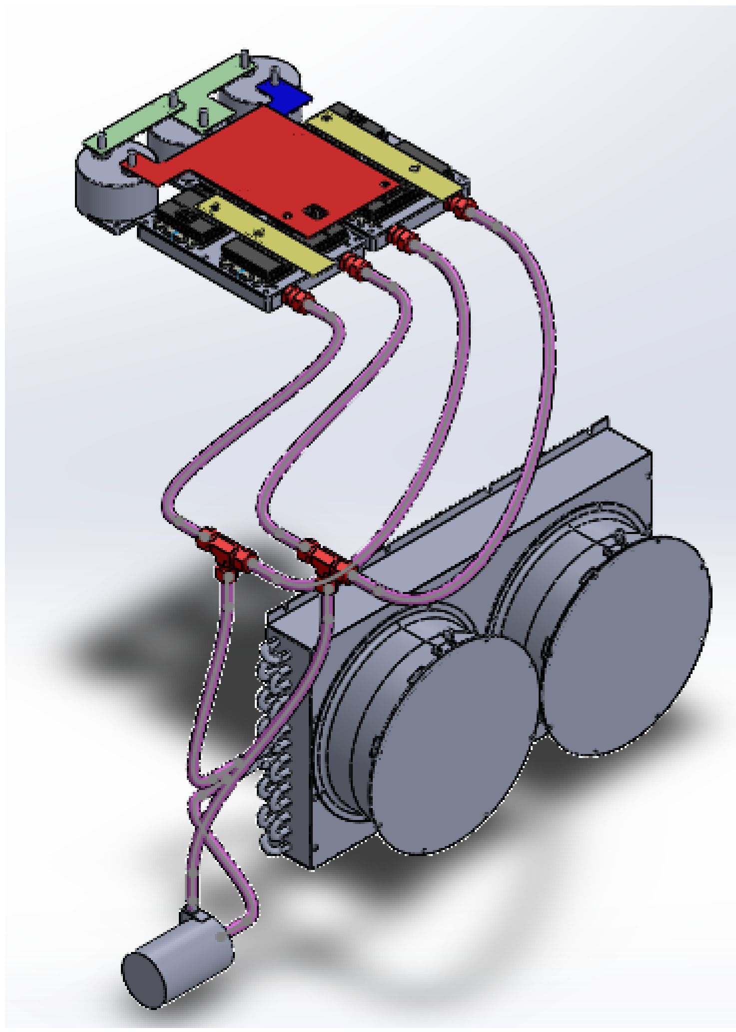

Figure 5.14: FPT SolidWorks assembly

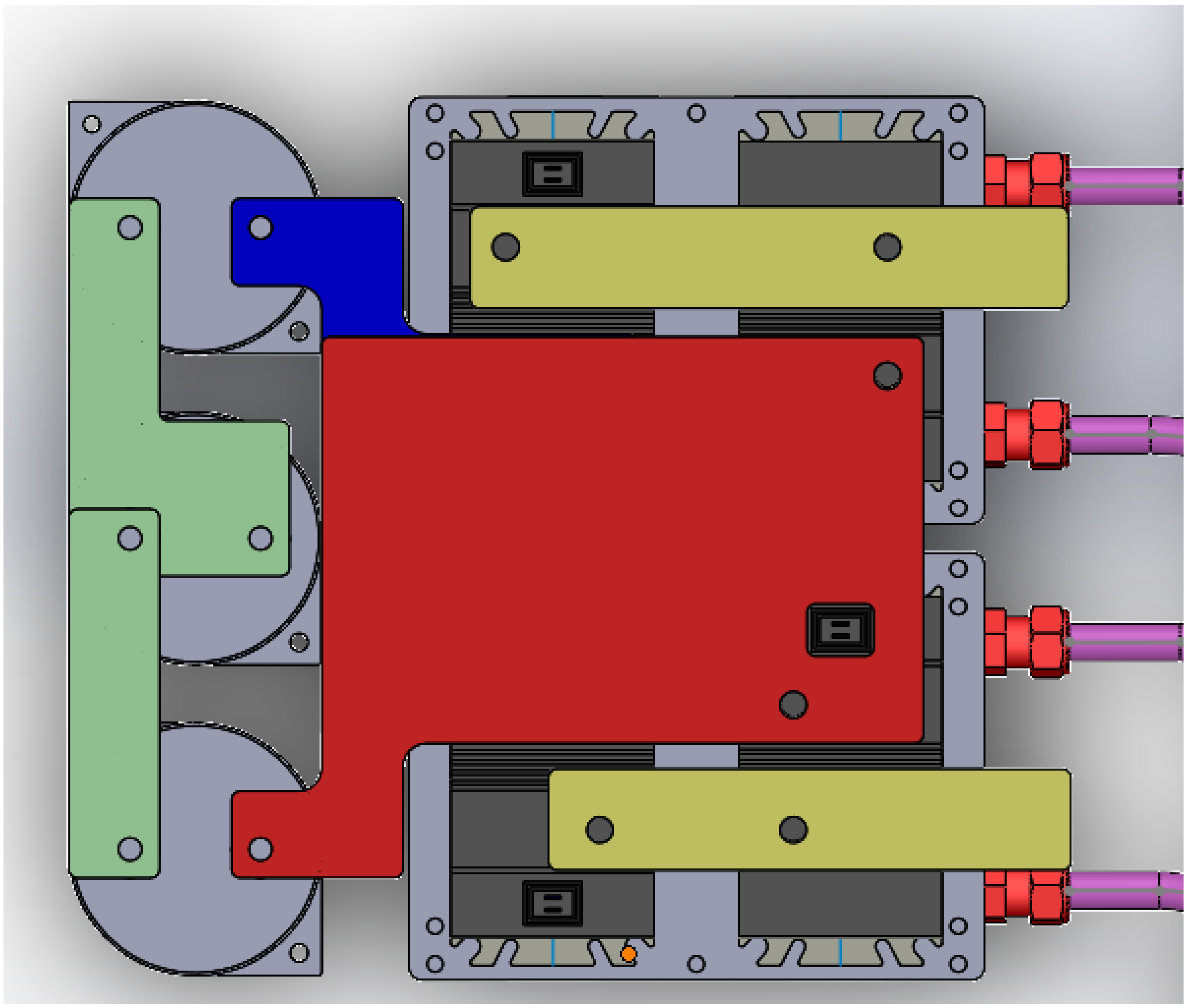

Figure 5.15: Close up of Top View

CHAPTER

6

CONCLUSION AND FUTURE WORK

A 6kV, 100A Virtual Full Power Test system is designed and verified in simulation for evaluating switching characteristics of the Super Cascode Power Module.

6.1 Scope of future work

The test system hardware can be built from the proposed design and evaluated against SCPM switching loss results obtained from Double Pulse Test method. A thermal description model of the SCPM for PLECS simulation can be generated from monitoring SCPM base plate temperature, switching loss and current during test.

Bibliography

[1] B. Gao et al. "6.0kV, 100A, 175kHz super cascode power module for medium voltage, high power applications". In: *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*. 2018, pp. 1288–1293.

[2] Zheng Chen. "Characterization and Modeling of High-Switching-Speed Behavior of SiC Active Devices". Masters Thesis. Virginia Polytechnic Institute and State University, 2009.

[3] A. Marzoughi, R. Burgos, and D. Boroyevich. "Characterization and Performance Evaluation of the State-of-the-Art 3.3 kV 30 A Full-SiC MOSFETs". In: *IEEE Transactions on Industry Applications* 55.1 (2019), pp. 575–583.

[4] A. Marzoughi, R. Burgos, and D. Boroyevich. "Characterization and comparison of latest generation 900-V and 1.2-kV SiC MOSFETs". In: *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*. 2016, pp. 1–8.

[5] A. Marzoughi et al. "Characterization and Evaluation of the State-of-the-Art 3.3-kV 400-A SiC MOSFETs". In: *IEEE Transactions on Industrial Electronics* 64.10 (2017), pp. 8247–8257.

[6] J. Brandelero et al. "A non-intrusive method for measuring switching losses of GaN power transistors". In: *IECON 2013 - 39th Annual Conference of the IEEE Industrial Electronics Society*. 2013, pp. 246–251.

[7] B. Cougo, H. Schneider, and T. Meynard. "Accurate switching energy estimation of wide bandgap devices used in converters for aircraft applications". In: *2013 15th European Conference on Power Electronics and Applications (EPE)*. 2013, pp. 1–10.

[8] D. C. Hopkins and D. W. Root. "Synthesis of a new class of converters that utilize energy recirculation". In: *Proceedings of 1994 Power Electronics Specialist Conference - PESC'94*. Vol. 2. 1994, 1167–1172 vol.2.

[9] Christina Marie DiMarino. "High Temperature Characterization and Analysis of Silicon Carbide (SiC) Power Semiconductor Transistors". Masters Thesis. Virginia Polytechnic Institute and State University, 2014.

[10] C. Salcines, A. Kruglov, and I. Kallfass. "A Novel Characterization Technique to Extract High Voltage - High Current IV Characteristics of Power MOSFETs from Dynamic Measurements". In: *2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*. 2018, pp. 1–6. DOI: `10.1109/WiPDA.2018.8569160`.

[11] P. Ladoux et al. "Test bench for the characterisation of experimental low voltage IGCTs". In: *2004 IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No.04CH37551)*. Vol. 4. 2004, 2937–2942 Vol.4.

[12] Silverio Alvarez e Hidalgo. "Characterisation of 3.3kV IGCTs for Medium Power Applications". Sept. 2005. URL: https://oatao.univ-toulouse.fr/7446/.

[13] *Power MOSFET Basics - Understanding Voltage Ratings*. AN851. VISHAY SILICONIX. 2017. URL: https://www.mouser.com/pdfdocs/Vishay_AN861.pdf.

[14] Bo Gao. "Scalable Medium Voltage and High Voltage Super Cascode Power Modules". PhD thesis. North Carolina State University, 2018.

[15] *37502 Technical Datasheet*. 37502. Belden Wire & Cable. 2020. URL: https://catalog.belden.com/techdata/EN/37502_techdata.pdf.

[16] H. A. Wheeler. "Simple Inductance Formulas for Radio Coils". In: *Proceedings of the Institute of Radio Engineers* 16.10 (1928), pp. 1398–1400. DOI: 10.1109/JRPROC.1928.221309.

[17] D. C. Meeker. *Finite Element Method Magnetics*. Version 4.2 (28Feb2018 Build). URL: http://www.femm.info.

[18] *LNK-P2X-16-220 Datasheet*. ICAR. URL: https://www.icar.com/genera_scheda_lnk.php?codice=LNK-P2X-16-220&lang=en.

[19] Illinois Capacitor. *Voltage Balancing Resistors*. URL: https://www.illinoiscapacitor.com/pdf/papers/voltage_balancing_resistors.pdf.

[20] *Type MG Precision High Voltage Resistors*. Caddock. URL: http://www.caddock.com/Online_catalog/Mrktg_Lit/TypeMG.pdf.

[21] Jr. Daniel W. Root. "SYNTHESIS OF SWITCH-MODE POWER ELECTRONIC CIRCUITS FOR ENERGY RECIRCULATION AND STORAGE". Masters Thesis. Auburn University, Sept. 1993.

[22] *Current Transducer IT 200-S ULTRASTAB*. LEM. 2014. URL: https://www.lem.com/sites/default/files/products_datasheets/it_200-s_ultrastab.pdf.

[23] *Cold-Plate-ATS-1001-DIY*. $R2_0619$. Advanced Thermal Systems. 2019. URL: https://www.qats.com/DataSheet/Cold-Plate-ATS-CP-1001-DIY.

[24] *Heat Exchanger*. $R11_1020$. Advanced Thermal Systems. 2020. URL: https://www.qats.com/DataSheet/Heat-Exchangers.

[25] *Technical Guide*. Bulletin 0002-T1/USA. Parker Hannifin Corporation. 2003. URL: https://www.parker.com/Literature/Literature%5C%20Files/Partek/cat/english/TechBulletin.pdf.

[26] A. D. Callegaro et al. "Bus Bar Design for High-Power Inverters". In: *IEEE Transactions on Power Electronics* 33.3 (2018), pp. 2354–2367. DOI: 10.1109/TPEL.2017.2691668.

[27] H. Gui et al. “Design of Low Inductance Busbar for 500 kVA Three-Level ANPC Converter”. In: *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*. 2019, pp. 7130–7137. DOI: 10.1109/ECCE.2019.8912605.

[28] J. M. Guichon et al. “Busbar Design: How to Spare Nanohenries ?” In: *Conference Record of the 2006 IEEE Industry Applications Conference Forty-First IAS Annual Meeting*. Vol. 4. 2006, pp. 1865–1869. DOI: 10.1109/IAS.2006.256790.

[29] C. Chen et al. “Modeling and optimization of high power inverter three-layer laminated busbar”. In: *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*. 2012, pp. 1380–1385. DOI: 10.1109/ECCE.2012.6342654.

[30] Copper Development Association Inc. *Ampacities and Mechanical Properties of Rectangular Copper Busbars: Table 1. Ampacities of Copper No. 110*. URL: https://www.copper.org/applications/electrical/busbar/bus_table1.html.

[31] J. M. Allocco. “Laminated bus bars for power system interconnects”. In: *Proceedings of APEC 97 - Applied Power Electronics Conference*. Vol. 2. 1997, 585–589 vol.2. DOI: 10.1109/APEC.1997.575624.

[32] Storm Power Components. *Insulating Films*. URL: https://stormpowercomponents.com/insulation/insulating-films/.