ABSTRACT

LI, XIAOMIN. High Efficiency Integrated Switched Capacitor Converters for High Voltage Low Power Applications. (Under the direction of Dr. Alex Q. Huang).

This dissertation focuses on the topology analysis, efficiency enhancement design, and silicon implementation of an integrated Switched Capacitor DC-DC converter (SC-DCDC) for high voltage and low power applications. A new and comprehensive methodology for optimizing SC-DCDC based on the area constraint is proposed in this work. The optimization methodology identifies the relative sizes of each single capacitor and power switch device first. After that an optimized ratio between the total capacitor area and the total power switch area is found. Finally the total area and switching frequency are optimized to achieve the highest power conversion efficiency. Two new figure of merits based on the output impedance are proposed: SSL impedance metric and FSL impedance metric. These figure of merits can be used to compare performance among converters with different topologies. A guideline is also provided for choosing the best performance converter topology for a specific application and a given silicon process technology.

The optimal design methodology is applied to the architecture design procedure of a switched capacitor based liquid crystal lens (LCL) driver IC. The LCL driver provides an adjustable 3V to 15V RMS square wave output voltages to drive a liquid crystal lens that can be modeled as a 5nF capacitive load. This application is typically powered by a 3V lithium ion button battery cell or energy harvesting devices. A reconfigurable 2×/3×/4×/5× series-parallel hysteresis SC-DCDC is developed to maintain high power efficient over a wide range of output voltage. Several high performance circuitries used in the low power high voltage applications are proposed, including: a reduced voltage ripple H-bridge gate drive; a

low power high speed level shifter; a low power comparator with two stages hysteresis; a low kickback noise dynamic-comparator, a high accuracy low power active clamp and a converter output fast sink control scheme.

The designed LCL driver IC was successfully implemented with a 0.5μm 5V V_{GS}, 12-45V V_{DS} BCD technology. Silicon measurement results showed the LCL driver achieves a record high peak power efficiency of 93.6%.

High Efficiency Integrated Switched Capacitor Converters for High Voltage Low Power Applications

by
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DEDICATION

To my parents

Shuizhi Li and Ruqi Li

and my wife

Yuan Fang

BIOGRAPHY

The author, Xiaomin Li was born in the city of Maoming, Guangdong, P.R. China and received a Bachelor of Science degree from the Department of Electronic Science and Technology, University of Science and Technology of China, Hefei, P. R. China in 2005. From September 2005 to July 2010, he was an analog IC design engineer with Ricoh Electronic Device, Shanghai, China, where he worked on power management integrated circuit design. He started to pursue a Ph.D. degree in 2010 at the Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, North Carolina, USA.

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CHAPTER 1

1 Introduction

1.1 High Voltage Low Power Applications Background

Electrically driven liquid crystal lens (LCL) [1][2] with tunable focusing has become a well know technique for vision care [3][4], three-dimensional displays, zoom systems, optical tweezers, microscopes and imaging systems due to its advantages compares to conventional lenses. The salient features of low power consumption, thin thickness and simple structure without any mechanical movement are promising for portable devices. The operating principle of a LCL is the orientation distributions of liquid crystal directors can be changed by applied voltages. This mechanism makes an incident plan wave propagates in a piece of liquid crystal experience a lens-like phase difference.

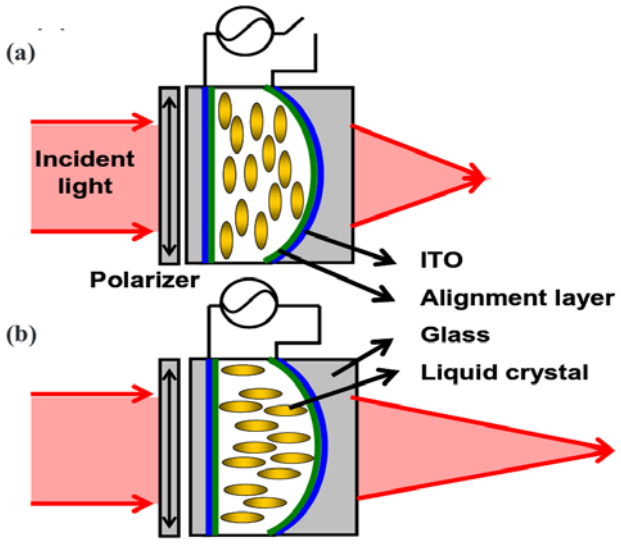

Figure 1.1. The operating principle of the structure of LC lens at (a) voltage-off state and (b) voltage-on state (V>>Vth) [1]

A typical liquid crystal (LC) cell structure is shown in Figure 1.2[4]. There are three electrodes in the LC cell, two of them are made of transparent indium tin oxide (ITO) films and the other is made of an aluminum (Al) film. Without an applied voltage, liquid crystals are sandwiched between two glass substrates and aligned homogeneously with a small pretilt angle. ITO electrodes locates separately at the bottom and on the top of the LC cell, one is on the inner side of substrate 1, the other one is on the inner side of substrate 3. The Al electrode locates on the outer side of substrate 2 and has a circular hole in its center. A thin glass is place between the upper ITO electrode and the Al electron to separate them from each other. The LC cell driven by an AC voltage V1 across the Al electrode and the bottom side ITO electrode, and another AC voltage V2 across the two ITO electrodes. V1 and V2 are in phase and their switching frequencies are around 1 KHz.

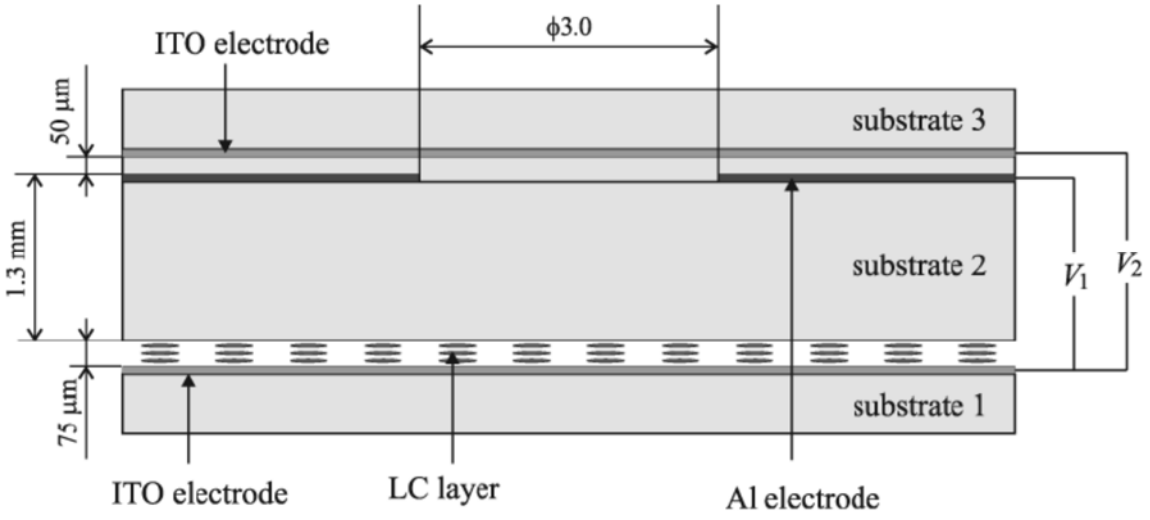

Figure 1.2. Structure of LC lens cell [2]

The applied electric field in the LC layer re-orientates the LC directors. Generally, a stronger electric field results in a larger tilt angle of LC directors. In order to drive a LC cell to work as a positive lens, V2 initially set to zero and V1 is adjusted to a value at which lens-like phase profile of the incident light wave is formed. Then tuning V2 from 0 to a high voltage to control the focal length of the LC lens while V1 acts as a bias voltage and remains unchanged. To drive the LC cell to work as a negative lens, a similar process is performed and one just needs to exchange V1 and V2.

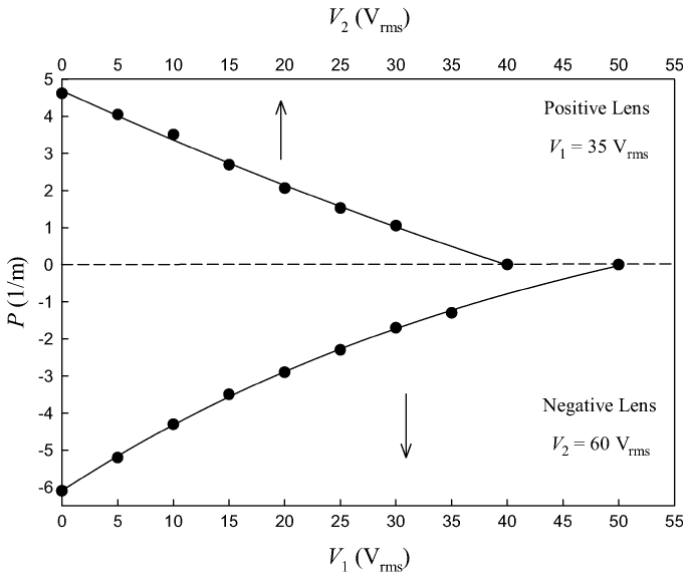

Figure 1.3. Lens power changing with controlling voltages [2]

The AC voltages applied to a LCL should have minimal DC components. As prolonged DC operation may cause electrochemical reactions inside the LC cell which will cause significantly reduced life. The initial indications of lens degradation because of excessive DC current is an electro-plating of liquid crystal components onto the surface electrodes.

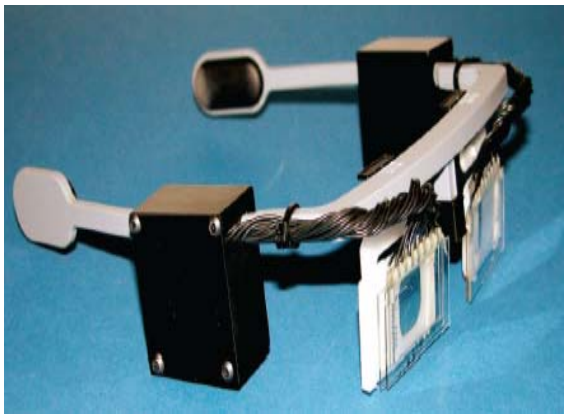

Figure 1.4. Liquid Crystal Lens glasses prototype [3]

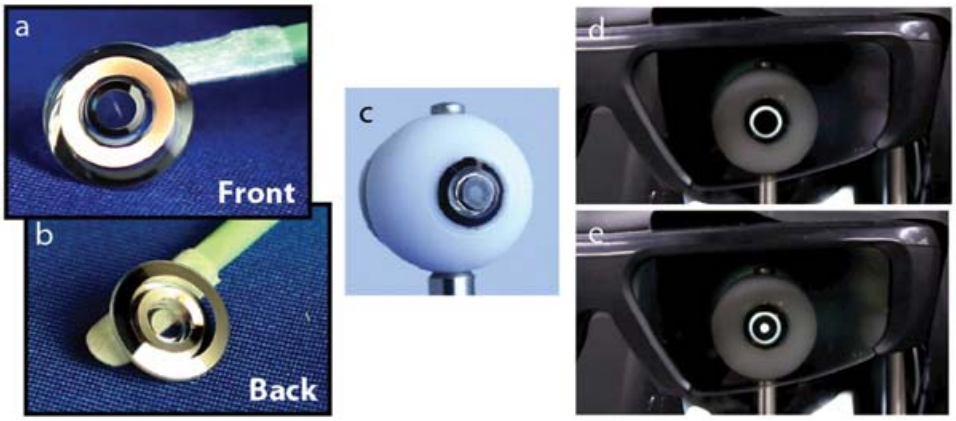

Figure 1.5. Liquid Crystal switchable telescopic contact lenses [4]

1.2 Research Motivation

Figure 1.6 shows a typical portable liquid crystal lenses driving system. Normally liquid crystal lens driver is powered by a compact low voltage batteries in mobile applications. Input signal of the LCL driver is a user defined low voltage reference. Output of the LCL driver is a high voltage AC square-wave with VRMS equals to multiple times of input reference voltage.

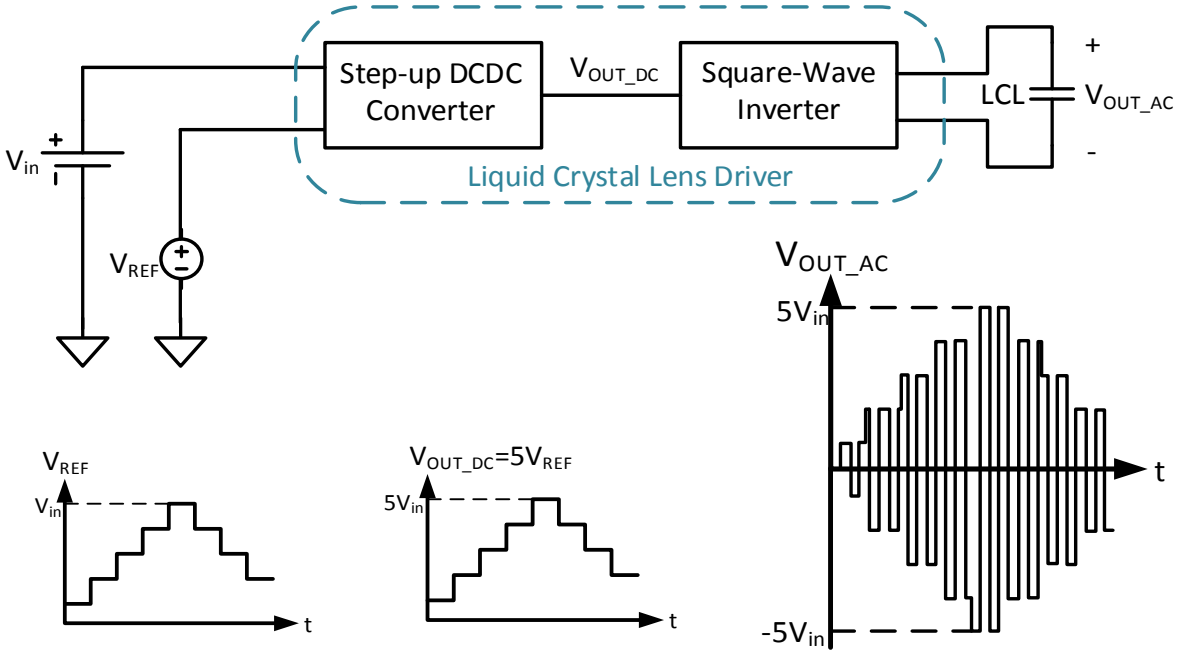

Figure 1.6. Liquid Crystal Lens Driver and Output Waveforms

The key challenge of the implementation of a liquid crystal lens driver is to achieve the following requirements to make it suitable for portable applications.

1) High power conversion efficiency. This is crucial for mobile application as high power efficiency can extend battery operating time.
2) Very compact size. In order to fit the liquid crystal lens driver into a normal glasses arm, the size of the power supply and driver should be very compact.
3) Wide output voltage range. The range of output voltage of liquid crystal driver needs to be wide enough to cover a wide range of lens power correction requirement.

4) High voltage step-up ratio. The liquid crystal lens driver should achieve a high voltage step-up ratio thus low voltage single cell battery can be used to minimize the power supply size.
5) Ultra-low power. The lens driver will only output a low power as liquid crystal lenses are low-power devices.

In order to fulfill above requirements, this research focuses on low profile, high power conversion efficiency converter topologies study and their optimization; novel control methods for low power operation; advanced low power circuits and robust high voltage driver techniques.

1.3 Contribution of This Research

In this dissertation, several key contributions are achieved and are summarized as following:

1) A complete, detail methodology for switched capacitor converter optimal design based on the area constraint is proposed.
2) Two new figure of merits based on output impedance: a SSL impedance metric and a FSL impedance metric are proposed and can be used to compare performance among converters with different topologies.
3) A compact liquid crystal lens driver IC was design and implemented to achieve a high power conversion efficiency over a wide output power range. A record 93.6% power conversion efficiency is measured.

4) Proposed several high performance circuitries used in the liquid crystal lens driver IC and can be used in other low power, high voltage applications. Those proposed new integrated circuitries includes:
    a. Reduced voltage ripple H-bridge gate drive
    b. Low power high speed level shifter
    c. Low power comparator with two stages hysteresis
    d. Low kickback noise dynamic comparator
    e. High accuracy low power active clamp
    f. Converter output fast sink control scheme

1.4 Dissertation Outline

This dissertation has been organized as follows: In chapter 2, a new design methodology is developed which permits the optimization of the relative capacitor and power switch sizes to meet a constraint of limited chip area. And two new figure of merits are developed to compare different converter topologies. Chapter 3 provides a guideline to find out the best area ratio between capacitor and power switch. And an overall optimization procedure is developed to find out the minimal total impedance of a SC converter for a given process technology and total chip area. Circuit architecture and control method are also discussed in this chapter. In chapter 4, detailed circuit implementations are discussed and several new high performance circuitries for low power high voltage applications are proposed. In chapter 5, physical implementation of the liquid crystal lens driver IC is presented. Measurement

results from the fabricated integrated circuit prototype are analyzed. Finally, chapter 6 summarizes the key conclusions and future works.

CHAPTER **2**

2 Monolithic Switched Capacitor Converters Analysis and Optimization

2.1 Switched Capacitor Converters vs. Inductor-based Switched Converters

As described in Chapter 1, the voltage gap between a low voltage source and a high voltage load requires a step-up DC-DC converter to efficiently interface them together. In typical liquid crystal lens driver systems, input sources are portable lithium ion batteries whose terminal voltages range from 2.7V to 4.5V. And the output voltage needs to be varied from 5V to 30V in order to provide a wide range of lens power adjustment.

Both inductor-based boost converters and switched capacitor converters can be used to implement the step-up DC-DC voltage conversion. Figure 2.1 shows an inductor-based boost converter and a 1:5 Dickson switched-capacitor converter. The inductor-based boost converter contains only two power switches, one inductor and one output capacitor. By varying its switching duty ratio, boost converter can attain any output voltage higher than the input voltage and ideally can achieve 100% power efficiency. The switched capacitor power converters are another type of DC-DC power converters that only use a network of switches and capacitors. Unlike traditional inductor based converters, switched capacitor converters do not rely on magnetic energy storage. This fact makes switched capacitors inherently smaller, since the magnetic components are usually much large than capacitors. Moreover, the state-

of-the-art high density on-chip capacitors, such as deep-trench capacitors [5] can greatly reduce chip die size due to increased capacitance per unit chip area. Thus switched capacitor converters are ideal for integration implementation to minimize system size. This is particularly true to low power portable applications such as the LCL drivers.

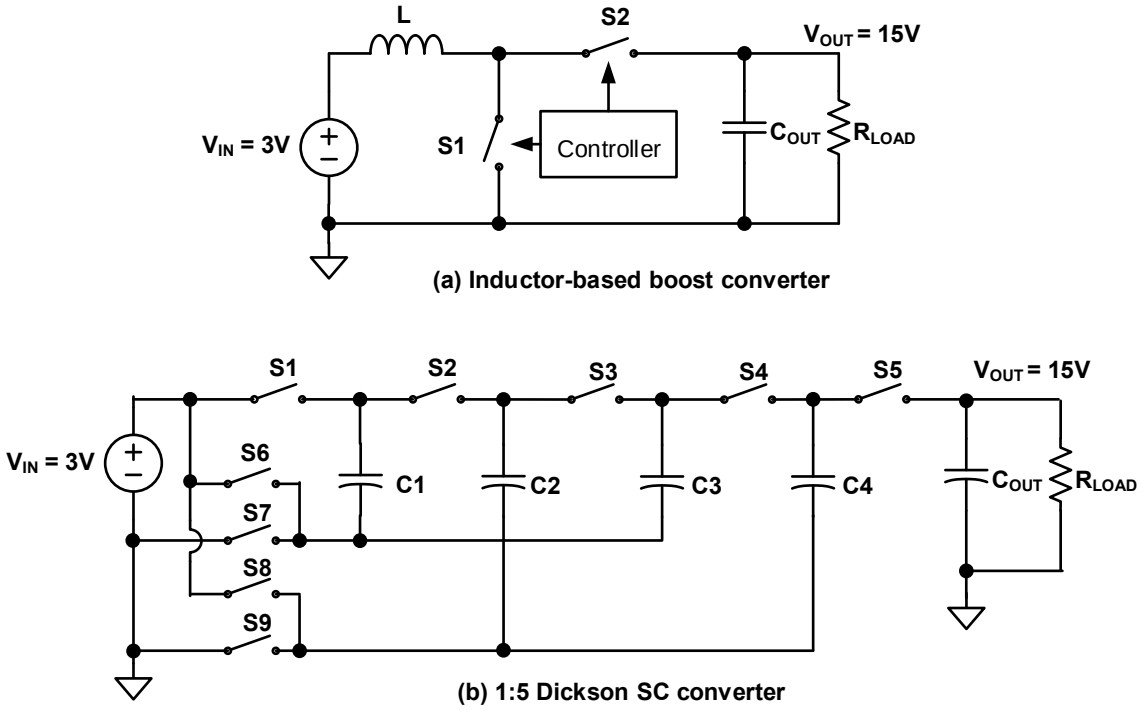

Figure 2.1. Step-up DC-DC converters

However, switched capacitor converters are only capable of generating a finite numbers of conversion ratio. Unlike inductor based converters, which can generate continue conversion ratios, switched capacitor converters can only achieve high power conversion efficiencies in the given conversion ratios. The peak efficiency of switched capacitor converter is given by:

$$\eta_{MAX} = \frac{V_{OUT}}{N \times V_{IN}} \tag{2.1}$$

Where N is the conversion ratio, V_{IN} is the input voltage and V_{OUT} is the output voltage. An ideal steady state behavior model of a switched capacitor converter is shown in Figure 2.2 [6]. It consists of an ideal DC transformer with a turns ratio equals to the voltage conversion ratio, and an output resistance R_{OUT}. With a non-zero output current, the switch capacitor converter will introduce a voltage drop across the input and output of the converter. This voltage drop is proportional to the output resistance. Thus R_{OUT} sets the maximal output voltage, constrained by the maximal output current, and also determines the conversion efficiency and open-loop load regulation properties.

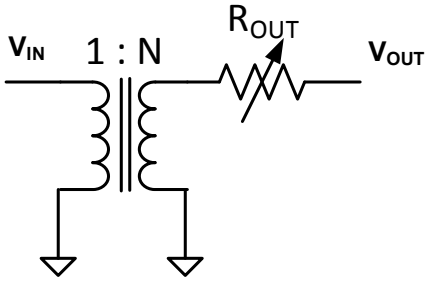

Figure 2.2. Ideal model of switched capacitor converter

2.2 Review of Switched Capacitor Converter Output Resistance Modeling

In order to provide a guideline for comparing different switched capacitor converter topologies, a review of switched capacitor converter modeling is provided in this section. There are two asymptotic limits to the output resistance of switched capacitor converter, the slow switching limit (SSL) and the fast switching limit (FSL) [6]. In SSL operation, the

output impedance R_{SSL} is calculated by assuming that charge transfer among the input source, flying capacitors and the output source are impulsive. Also power switches and all other conductive interconnections are ideal. In FSL operation, the output impedance R_{FSL} is calculated by assuming capacitor voltages remain constant. And R_{FSL} is dominated by the resistance associated with power switches and other parasitic resistances in the converter.

Both output resistance R_{SSL} and R_{FSL} of a switched capacitor converter can be analyzed by charge flow technique [6][7][8]. The powertrain capacitors and transistors inside the converter switch periodically to achieve the charge transfer. By inspecting the converter topology, charge flow vectors of flying capacitor a_c and charge flow vectors of switches a_r can be extracted based on Kirchoff's Current Law (KCL).

For a two phases switched capacitor converter with N powertrain capacitors, the capacitor charge multiplier vectors α_c^1 and α_c^2 are defined as:

$$\begin{bmatrix} \alpha_c^1 \\ \alpha_c^2 \end{bmatrix} = \frac{1}{q_{out}} \cdot \begin{bmatrix} q_{c1}^1 & q_{c2}^1 & \cdots & q_{cN}^1 \\ q_{c1}^2 & q_{c2}^2 & \cdots & q_{cN}^2 \end{bmatrix} \tag{2.2}$$

where each component in α_c^1 is the charge transfer in each capacitor in phase 1 of the switching period divided by the total charge delivered to the output during a full period. And the components in vector α_c^2 are defined similarly.

Assume the switched capacitor converter is a two phase circuit with nominally 50% duty cycle, the R_{SSL} is given by

$$R_{SSL} = \sum_{i \in caps} \frac{\left(a_{c,i}\right)^2}{f_{SW} C_i} \tag{2.3}$$

where $a_{c,i}$ is called the charge multiplier element which is given by (2.2), f_{SW} is the switching frequency, and C_i stands for the capacitance of each flying capacitor. If a charge is going into a capacitor, the sign of the charge multiplier element related to this capacitor is positive; if a charge is coming out of a capacitor, the sign of the charge multiplier element related to that capacitor is negative. (2.3) indicates the SSL output resistance can be calculated by knowing the data of capacitor charge multiplier vectors, capacitor values and the switching frequency.

Switch charge multiplier vector a_r can be defined similar to the capacitor charge multiplier. For a two phases switched capacitor converter with M switches, the switch charge multiplier vectors α_r^1 and α_r^2 are defined as:

$$\begin{bmatrix}\alpha_r^1\\ \alpha_r^2\end{bmatrix} = \frac{1}{q_{out}} \cdot \begin{bmatrix} q_{r1}^1 & q_{r2}^1 & \cdots & q_{rM}^1 \\ q_{r1}^2 & q_{r2}^2 & \cdots & q_{rM}^2 \end{bmatrix} \tag{2.4}$$

where each component in α_r^1 is the charge transfer in each switch in phase 1 of the switching period divided by the total charge delivered to the output during a full period. And the vector α_r^2 is defined similarly.

For a two phases switched capacitor converter with 50% duty cycle, the R_{FSL} is given by:

$$R_{FSL} = 2 \sum_{i \in switches} R_i \left(a_{r,i}\right)^2 \tag{2.5}$$

where $a_{r,i}$ is the charge multiplier element; it is the ratio between the charge flow in each power switches and the total output charge per each switching cycle. R_i stands for the resistance of each power switches. As shown in (2.5), R_{FSL} is frequency independent.

Assuming power flows from the input source to the output load, if a switch conducts positive current while on and blocks positive voltage while off, its related charge multiplier element is positive, and this switch much be implemented by an active transistor device; if a switch conducts positive current while on and blocks negative voltage, then its related charge multiplier element is negative, and this switch can be implemented by an diode [9]. (2.5) indicates FSL output resistance can be determined by knowing the data of a_r and the resistance of each switch.

A real switched capacitor converter is actually operating in a state between the SSL and FSL. While deriving a general algebraic expression for the output impedance of a switched capacitor converter is difficult, R_{OUT} is often approximated as a Euclidean norm approximation of R_{SSL} and R_{FSL} [9]:

$$R_{OUT} \approx \sqrt{R_{SSL}^2 + R_{FSL}^2} \tag{2.6}$$

2.3 Fully Integrated Components in Switched Capacitor Converter

Fully integrated switched capacitor converters are favorable in those applications that a minimized system size are required. Since switched capacitor converters only consist capacitors and power switches, they are possible to be fully integrated by using standard semiconductor processing technologies. For high voltage applications, fully on-chip SC converter may need to be implemented by more complicate technologies that provides high voltage devices such as HV-MOSFET and DMOS [10].

2.3.1 Implementation of On-chip Capacitors

There are four types on-chip capacitors widely used in existing silicon integrated circuit technologies: Metal-Insulator-Metal (MIM) capacitors, Metal-Oxide-Metal (MOM) capacitors, Gate Oxide capacitors (GO) and Deep Trench capacitors (DT). MIM capacitors are widely available in many standard CMOS technology at a cost of an additional thin insulation layer. The positive and negative planes of capacitor are formed by two planar metal layers. And the high dielectric isolation layer makes MIM capacitor highly linear. Unlike MIM capacitors, MOM capacitors don't need the additional insulation layer, thus cost wise they are cheaper since they save a layer of mask. MOM capacitors are normally formed by metal stacks in vertical parallel plate arrangements with via. Insulation material of MOM capacitors are normally oxide which has lower dielectric than that in MIM capacitor, thus capacitor density of the MOM capacitor is relatively low [11]. GO capacitor uses the same gate oxide which used in transistors to form the capacitor. Since the gate oxide can be very thin in an advanced technology node thus GO capacitors density is higher than that of MIM capacitors. However, GO capacitors have a strong voltage dependence and a high substrate parasitic capacitance. Thus GO capacitors are not suitable for implementing flying capacitors in switched capacitor converters. DT capacitors are non-standard structure capacitors that have limited availability in today's process technologies. The capacitance density of the DT capacitor is roughly two orders of magnitude higher than other on-chip capacitors [12][13][14]. And the vertical structure of the DT capacitor virtually eliminates substrate coupling capacitor. Thus DT capacitor is the best candidate for fully on-chip implementation of switched capacitor converters. The main drawbacks of DT capacitor are availability and

high cost. The voltage ratings of all four types on-chip capacitor are fixed by the technology process. Thus those switched capacitor converters with topologies requiring multiple voltage ratings are more difficult to be fully integrated or have a lower device utilization as the capacitor with highest voltage rating need to be used.

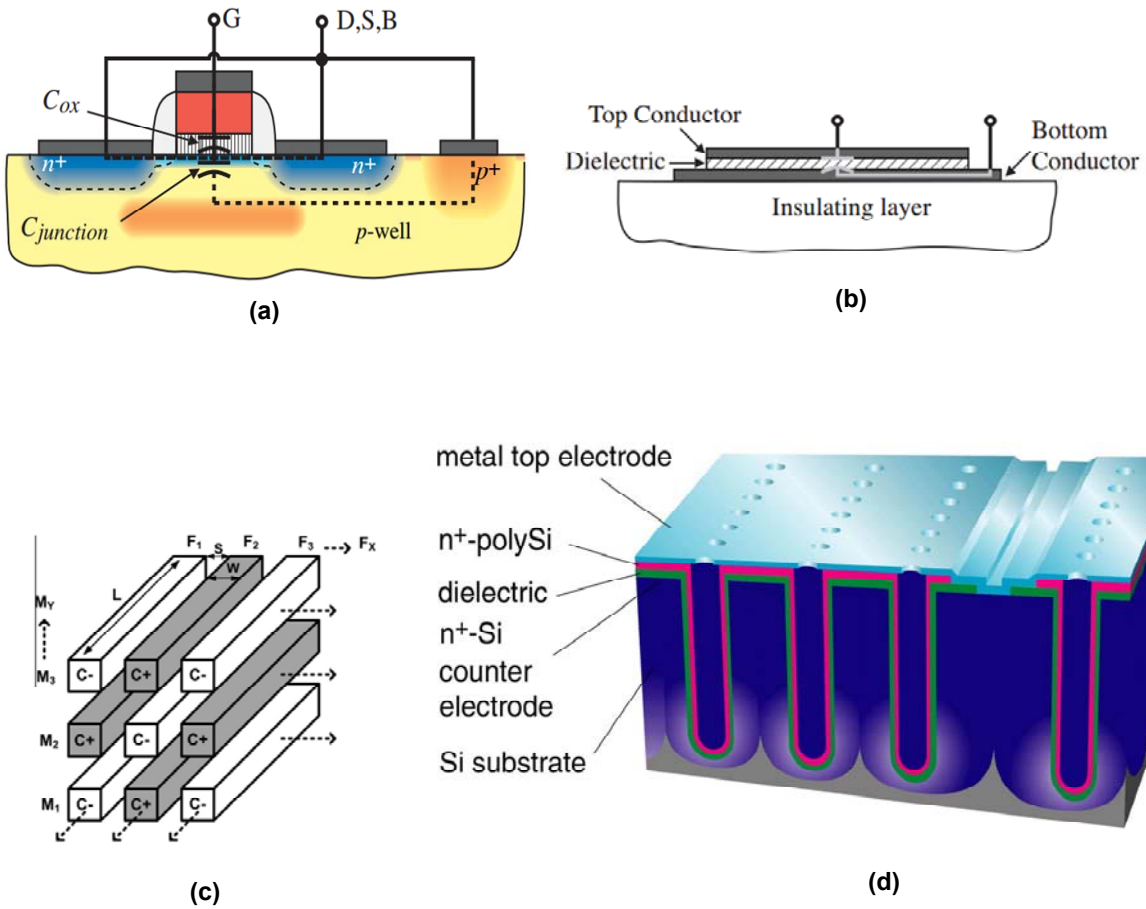

Figure 2.3.a) GO Capacitor, adopted from [15]; b) MIM Capacitor, adopted from [15]; c) MOM Capacitor, adopted from [16]; Deep Trench Capacitor, adopted from [17]

The capacitance density $C_{\square}$ of an on-chip capacitor is determined by its insulator material electric breakdown field, rating voltage and dielectric constant. The relationship is given by:

$$C_{\square} = \frac{C}{A} = \frac{\varepsilon_0 \varepsilon_r E_{BR}}{k V_{c,rate}} \tag{2.7}$$

where C is the capacitance, A is the on-chip capacitor area, ε_0 is the electric constant, $\varepsilon_r$is the dielectric constant of the insulator material, E_{BR} is the insulator material electric break down field and $V_{c,rate}$ is the capacitor rating voltage. Rewrite (2.7), a capacitor charge density can be defined by:

$$Q_{\square} = C_{\square} V_{c,rate} = \frac{C}{A} V_{c,rate} = \frac{\varepsilon_0 \varepsilon_r E_{BR}}{k} \tag{2.8}$$

where capacitor charge density $Q_{\square}$ is a constant for a given capacitor insulator material. It can be easily measured from an actual device or calculated from a process design note.

An overview of different types of on-chip capacitors are summarized in Table 2.1.

Capacitor	MIM	MOM	GO	DT
$C_{\square}$ [$fF/\mu m^2$]	1-5	0.5-1	3-10	100-1000
$V_{c,rate}$ [V]	High	High	Low	Medium
α_{par}	High	Low	Very High	Very Low
Cost	Medium	Low	Low	Very High

Table 2.1. Summary of on-chip capacitors

2.3.2 Implementation of On-chip Power Switches

Power switches are the most important active devices in a switched capacitor converter. If a switch conducts positive current when turn on and blocks positive voltage when turn off, it must be implemented by using an active power transistor. If a switch conducts positive current when turn on and blocks negative voltage when turn off, it can be implemented by using either a diode or an active transistor. However, a diode normally has

higher DC drop voltage than an active transistor thus inherently has higher power loss. Thus if conversion power efficiency is the major concern, all power switches should be implemented by active transistors. As the switches are either fully turn on or turn off during power conversion, a Figure-of-Merit can be used for comparing different power transistors devices.

$$\text{FOM} = R_{ON} Q_{gate} \tag{2.9}$$

where R_{ON} is the conducting resistance and Q_{gate} is gate charge static of the transistor.

For low voltage application, standard thin oxide MOSFET transistors can be used to implement the power switch. Those transistors use minimal gate length to minimize their input capacitances hence lower Q_{gate}. And they are operating in linear region thus their conducting resistance is given by:

$$R_{ON} = \frac{1}{\mu C_{OX} \frac{W}{L} (V_{GS} - V_{th})} \tag{2.10}$$

where μ represents the inversion channel mobility. Since the carrier of N-type device is electron, whose mobility is 2-3 times higher than holes, the carrier of P-type device, N-type devices have lower conduction resistance than P-type devices. Thus N-type devices are superior to P-type devices when used as power switches.

For high voltage application, switches may need to block off-state voltage higher than 5V. In that case, the unipolar lateral double-diffusion MOS (LDMOS) devices are widely used to block higher drain-source voltages [18]. LDMOS is a lateral drain-extended MOS transistor. In this device, a short channel is form by simultaneously double diffusing the source and channel dopants to achieve low channel resistance and high frequency operation.

A lightly doped drift region is used to provide high drain-source voltage blocking capability. And by changing the drift region length and doping concentration, it is able to fabricate different LDMOS devices with different voltage blocking capability.

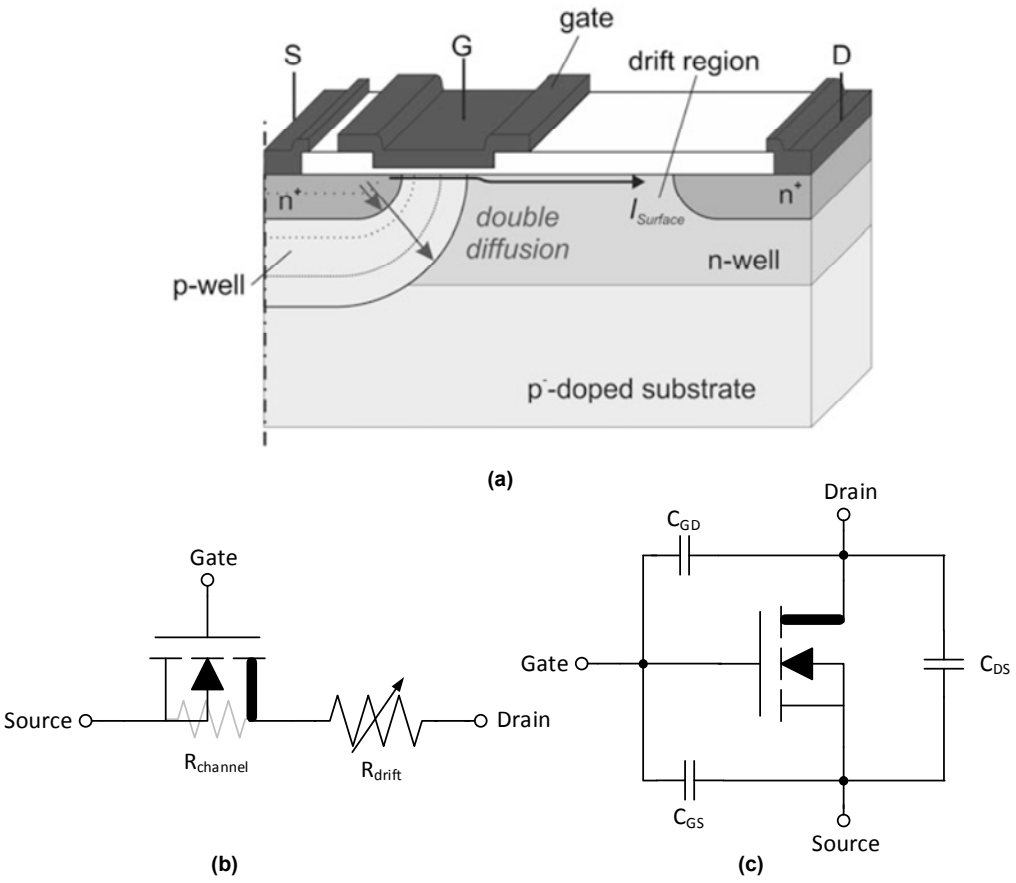

Figure 2.4.a) Cross-section of LDMOS transistor, adopted from [19]; b) Equivalent circuit of LDMOS transistor showing on resistances; c) Equivalent circuit of LDMOS transistor showing parasitic capacitances.

A cross-section of LDMOS and its parasitic resistances and capacitances are shown in Figure 2.4. The main components of on resistance $R_{DS,ON}$ include a channel resistance R_{ch} and a drift region resistance R_{drift}. Similar to low voltage devices, the channel resistance R_{ch} of LDMOS devices operating in linear region is given by:

$$R_{ch} = \frac{L_{ch}}{\mu C_{OX} W_{ch} (V_{GS} - V_{th})} \tag{2.11}$$

where L_{ch} and W_{ch} represent the channel length and width. The channel resistance is independent of device blocking voltage and only related to geometric, material constants and biasing potentials.

When current spreading effects from the channel into the drift region are neglected, the resistance of the drift region R_{drift} can be calculated:

$$R_{drift} = \frac{L_{drift}}{q \cdot \mu_{drift} \cdot W_{drift} \cdot N_{drift} \cdot d_{drift}} \tag{2.12}$$

where L_{drift}, W_{drift} and d_{drift} stand for length, width and depth of the drift region, respectively. And μ_{drift} is the drift region carrier mobility, N_{drift} is the average doping concentration in drift region. Drift region resistance can be reduced by increasing the doping concentration. However, the blocking capability of a LDMOS transistor also depend on its drift region doping concentration. The relationship between blocking voltage and drift region resistance is given by (2.13) [20].

$$\frac{R_{drift} \cdot A}{\Omega \cdot cm^2} = \mathrm{K} \cdot \left(\frac{cm}{d_{drift}}\right) \cdot \left(\frac{BV}{V}\right)^N \tag{2.13}$$

where K is an coefficient ranges from 10^{-15} to 10^{-9} depending on device structure. Punch-Through devices have K values roughly an order of magnitude lower than Non-Punch-Through devices [20]. BV is the blocking voltage of LDMOS device. N is an empirical correlation power factor ranges from 2 to 4. Modern LDMOS process uses "Reduced Surface Field" (RESURF) technology to lower the number N to achieve low drift region resistance in

high blocking voltage devices [21]. From (2.13), drift region resistance increases rapidly when blocking voltage increased.

The channel and drift resistances are the major contributors to the total on resistance, therefore the $R_{DS,ON}$ of LDMOS is equal to:

$$R_{DS,ON} = \frac{L_{ch}}{\mu C_{OX} W_{ch}(V_{GS} - V_{th})} + \frac{L_{drift}}{q \cdot \mu_{drift} \cdot W_{drift} \cdot N_{drift} \cdot d_{drift}} \tag{2.14}$$

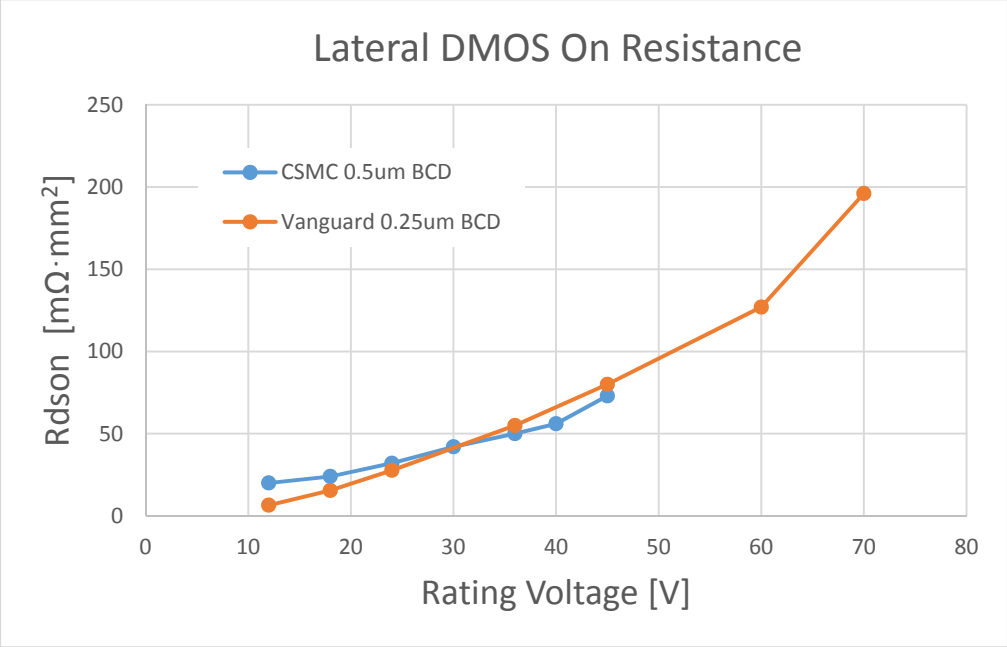

Figure 2.5. LDMOS devices ON resistance

Optimized sizing of power transistors in switched capacitor converters requires the understanding of the relationship between device blocking voltage and the on-state resistance. As shown in (2.11) and (2.12), both channel resistance and drift region resistance are non-linearly related to the blocking voltage. While analytically find out the equations to calculate on resistance from blocking voltage is difficult, the relationship between these two parameters can be found on design specs from fab manufacturers. Figure 2.4 shows two sets

of on resistances of LDMOS devices under different device rating voltages. For those LDMOS devices with low voltage ratings, their channel resistances dominated; and for those LDMOS devices with high voltage ratings, their drift region resistances dominated. Thus, for those LDMOS devices with low and high voltage ratings, the non-linearly relationships of both channel resistance and drift region resistance versus rating voltage make the on resistances of LDMOS devices non-linearly related to their rating voltages. For those LDMOS device with medium voltage ratings, channel resistance non-linearity and drift region resistance non-linearity can be cancelled out with each other. The empirical correlation indicates a linear relationship between on resistance and rating voltage for those LDMOS devices. Thus, a normalized on-resistance $R_{\square}^{*}$ per unit of silicon area can be defined by (2.15) for medium voltage rating LDMOS devices.

$$R_{\square}^{*} = \frac{R_{\square}}{V_{r,rate}} \tag{2.15}$$

where $R_{\square}$ is the LDMOS device on resistance per unit of silicon area, and $V_{r,rate}$ is the rating voltage of the LDMOS device. $R_{\square}^{*}$ is therefore a constant for a given technology and independent of device voltage rating.

2.4 Component Size Optimization for Switched Capacitor Converters

In order to design a fully integrated switched capacitor converter to achieve maximal power conversion efficiency, one needs to optimize sizes of those capacitors and switches used in the converter to minimize the converter output resistance. As minimal converter output resistance corresponds to maximal power conversion efficiency for a given power delivered. According to section 2.2, the SSL output impedance depends on capacitance of

flying capacitors, and FSL output impedance depends on resistance of power switches. Thus in a fully integration application, optimizing flying capacitors sizes can be done by minimizing SSL output impedance for a given total on-chip capacitor area. Analogously, optimizing the power switches sizes can be done by minimizing FSL output impedance for a given total on-chip switch area.

2.4.1 On-chip Capacitors Sizing

As discussed in section 2.3.1, the silicon area occupied by a capacitor is given by rewriting (2.8):

$$A_{c,i} = \frac{C_i V_{c,rate,i}}{Q_{\square}} \tag{2.16}$$

where C_i is the capacitance of flying capacitor, $V_{c,rate,i}$ is the rating voltage of flying capacitor, and $Q_{\square}$ is the voltage independent capacitor charge density. In order to minimize the capacitor area, the capacitor voltage should be maximized and ideally should equal to its rating voltage $V_{c,rate,i}$. The total die size of flying capacitors can be calculated by:

$$A_{c,tot} = \sum\nolimits_{i \in caps} \frac{C_i V_{c,rate,i}}{Q_{\square}} \tag{2.17}$$

The relative capacitor sizes can be optimized based on the total capacitor area constraint. To solve the equality-constrained optimization problem, a Lagrange multiplier method can be used [6]. The SSL output impedance will be minimized while the constraint on total capacitor area (2.17) is held constant. The Lagrange function can be defined by:

$$\mathcal{L}(C_i, \lambda) = \sum_{i \in caps} \frac{\left(a_{c,i}\right)^2}{C_i} + \lambda \left(\sum\nolimits_{i \in caps} \frac{C_i V_{c,rate,i}}{Q_{\square}} - A_{c,tot} \right) \tag{2.18}$$

where the first term represents the SSL output impedance scaled by switching frequency, and the second term represents the capacitor area constraint in (2.17). The SSL output impedance can be minimized when

$$\nabla_{C_i,\lambda}\mathcal{L}(C_i,\lambda) = 0 \tag{2.19}$$

Thus,

$$\frac{\partial \mathcal{L}}{\partial C_i} = -\frac{\left(a_{c,i}\right)^2}{C_i^2} + \lambda\frac{V_{c,rate,i}}{Q_\square} = 0 \tag{2.20}$$

$$\frac{\partial \mathcal{L}}{\partial \lambda} = \sum\nolimits_{i\in caps}\frac{C_i V_{c,rate,i}}{Q_\square} - A_{c,tot} = 0 \tag{2.21}$$

Solve C_i from (2.20),

$$C_i = \frac{|a_{c,i}|\sqrt{Q_\square}}{\sqrt{\lambda V_{c,rate,i}}} \tag{2.22}$$

Substitute (2.22) into (2.21) and rearrange it,

$$\frac{1}{\sqrt{\lambda}} = \frac{A_{c,tot}\sqrt{Q_\square}}{\sum_{i\in caps}|a_{c,i}|\sqrt{V_{c,rate,i}}} \tag{2.23}$$

Substitute (2.23) back to (2.22), one can obtain the optimized capacitance C_i^*.

$$C_i^* = \frac{A_{c,tot}Q_\square}{F_C}\cdot\frac{|a_{c,i}|}{\sqrt{V_{c,rate,i}}} \tag{2.24}$$

$$F_C = \sum\nolimits_{i\in caps}|a_{c,i}|\sqrt{V_{c,rate,i}} \tag{2.25}$$

where F_C is the topology capacitance factor and solely depends on converter topology. Substitute (2.24) into (2.3), one can obtain the optimized SSL output impedance.

$$R_{SSL}^{*} = \sum_{i \in caps} \frac{\left(a_{c,i}\right)^2}{f_{SW} C_i^{*}} = \frac{F_C^2}{f_{SW} A_{c,tot} Q_{\square}} \tag{2.26}$$

(2.26) indicates that the optimized SSL output impedance is proportional to the square of topology capacitor factor F_C. Thus the topology with the smallest F_C has the smallest SSL output impedance.

2.4.2 On-chip Power Switches Sizing

As discussed in section 2.3.2, the silicon area occupied by a power switch device with medium voltage rating is given by (2.15), thus a single switch size can be given by:

$$A_{sw,i} = \frac{R_{\square}^{*} V_{r,rate,i}}{R_i} \tag{2.27}$$

where R_i is the on resistance of power switch device, $V_{r,rate,i}$is the voltage rating of the power switch device, and $R_{\square}^{*}$ is the voltage independent on resistance per unit of silicon area. In order to minimize the total power switch area, a power switch device with lowest rating voltage that can meet the topology requirement should be chosen. The total die size of power switch devices can be calculated by:

$$A_{sw,tot} = \sum\nolimits_{i \in switches} \frac{R_{\square}^{*} V_{r,rate,i}}{R_i} \tag{2.28}$$

The relative power switch devices sizes can be optimized based on the total switch devices area constraint. Lagrange multiplier method can be used again to solve the equality-constrained optimization problem. The FSL output impedance will be minimized while the constraint on total power switch devices area (2.26) is held constant. The Lagrange function can be defined by:

$$\mathcal{L}(R_i, \lambda) = 2 \sum_{i \in caps} R_i \left(a_{r,i}\right)^2 + \lambda \left(\sum\nolimits_{i \in switches} \frac{R_{\square}^* V_{r,rate,i}}{R_i} - A_{sw,tot} \right) \tag{2.29}$$

where the first term represents the FSL output impedance, and the second term represents the power switch devices area constraint in (2.28). The FSL output impedance can be minimized when

$$\nabla_{R_i,\lambda} \mathcal{L}(R_i, \lambda) = 0 \tag{2.30}$$

Thus,

$$\frac{\partial \mathcal{L}}{\partial R_i} = 2\left(a_{r,i}\right)^2 - \lambda \frac{R_{\square}^* V_{r,rate,i}}{R_i^2} = 0 \tag{2.31}$$

$$\frac{\partial \mathcal{L}}{\partial \lambda} = \sum\nolimits_{i \in switches} \frac{R_{\square}^* V_{r,rate,i}}{R_i} - A_{sw,tot} = 0 \tag{2.32}$$

Solve R_i from (2.31),

$$R_i = \sqrt{\frac{\lambda R_{\square}^* V_{r,rate,i}}{2\left(a_{r,i}\right)^2}} \tag{2.33}$$

Substitute (2.33) into (2.32) and rearrange it,

$$\sqrt{\lambda} = \frac{\sqrt{2R_{\square}^*} \sum_{i \in switches} \sqrt{V_{r,rate,i}} \left|a_{r,i}\right|}{A_{sw,tot}} \tag{2.34}$$

Substitute (2.34) back to (2.33), one can obtain the optimized resistance R_i^*.

$$R_i^* = \frac{F_{sw} R_{\square}^*}{A_{sw,tot}} \cdot \frac{\sqrt{V_{r,rate,i}}}{\left|a_{r,i}\right|} \tag{2.35}$$

$$F_{sw} = \sum_{i \in switches} |a_{r,i}| \sqrt{V_{r,rate,i}} \tag{2.36}$$

where F_{sw} is the topology switch factor and solely depends on converter topology. Substitute (2.35) into (2.5), one can obtain the optimized FSL output impedance:

$$R_{FSL}^{*} = 2 \sum_{i \in switches} R_i^{*} \left(a_{r,i}\right)^2 = \frac{2 R_{\square}^{*} F_{sw}^2}{A_{sw,tot}} \tag{2.37}$$

(2.37) indicates that the optimized FSL output impedance is proportional to the square of the topology switch factor F_{sw}. Thus the topology with the smallest F_{sw} has the smallest FSL output impedance.

2.5 Comparing 1:N Step-up Switched-Capacitor Converter Topologies

Many options are available to implement a switched capacitor converter with certain voltage conversion ratio. Four popular switched capacitor converter topologies: Dickson topology, Series-Parallel topology, Ladder topology and Fibonacci topology with 1:5 conversion ratio are shown in Figure 2.6. Although these four different topologies provide the same voltage conversion ratio, they use different numbers of capacitors and power switches. Moreover, different topologies have different voltage rating requirements for their internal components. Generally a topology with lower voltage rating devices is easier to be fully integrated on chip.

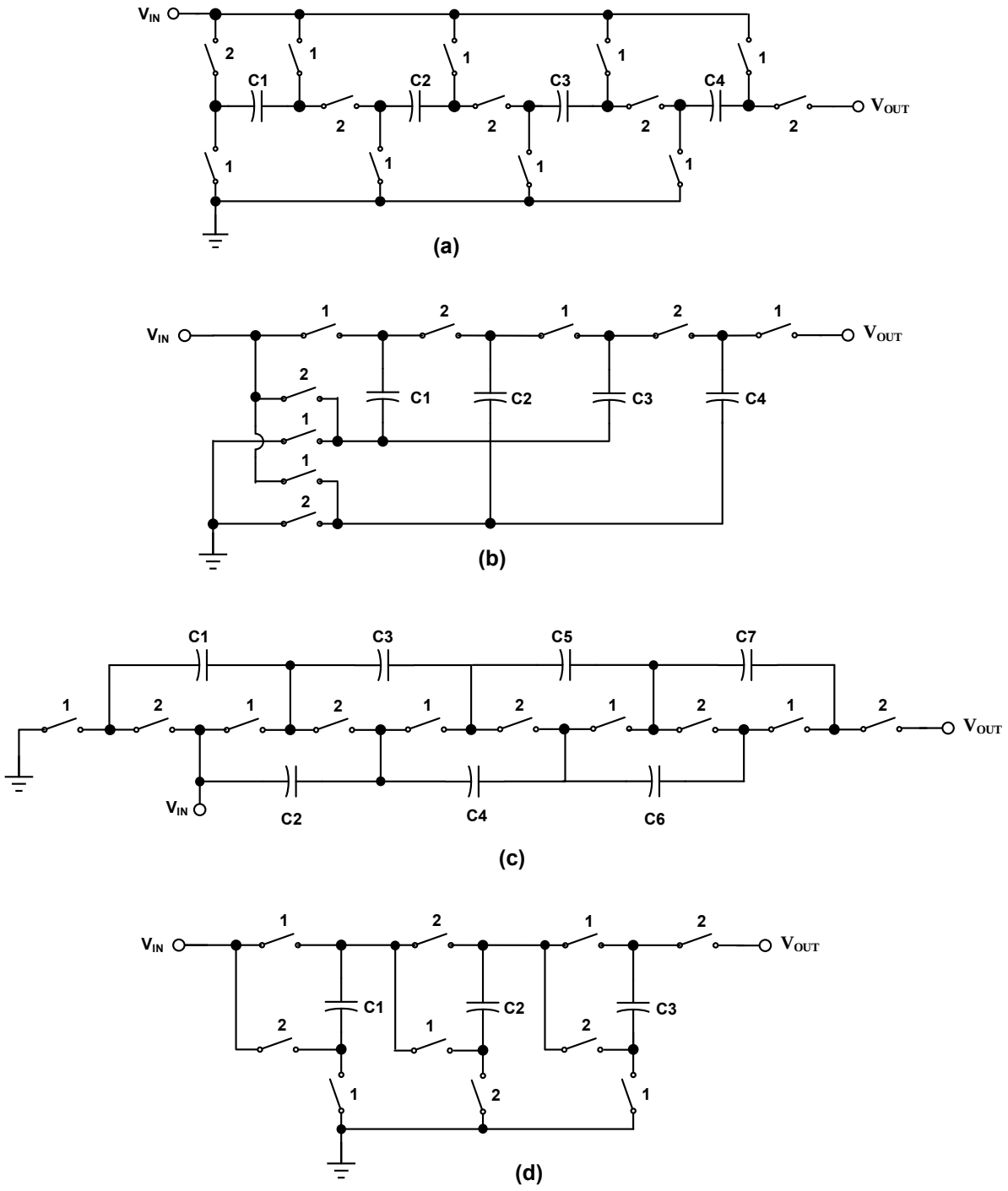

Figure 2.6. Four popular switched capacitor converter topologies with 1:5 conversion ratio. a) Series-Parallel; b) Dickson; c) Ladder; d) Fibonacci

In general, all four topologies listed in Figure 2.6 can be used to create a 1: N conversion, where N is an integer. For Fibonacci topology, N can only be one of Fibonacci sequence numbers larger than 2. Series-parallel and ladder topologies can be created for a general M: N conversion. However, creating M: N conversion needs to charge capacitors in series to ground, which will greatly increase power loss since the lower plate parasitic capacitors exists [22]. Thus in general only topologies with 1: N conversion ratio is considered in this section.

For a given application and an available technology, choosing the correct converter topology can greatly simplify the chip design and is also the key to improve power efficiency. Previous work [9] compared several switched capacitor converter topologies based on power handling capability metrics. However, those power handling capability metrics provided in [9] didn't reflect the on-chip silicon area constraint. Thus they are not suitable for comparing fully integrated converters with different topologies. In section 2.4, both SSL output impedance and FSL output impedance are optimized with silicon area restriction. And as shown in (2.26) and (2.37), for a given technology and device silicon area, the optimized R_{SSL}^{*} and R_{FSL}^{*} are solely depended on the square of topology capacitor factor and the square of topology switch factor, respectively. Thus for two phase converters with 50% duty cycle, two output impedance metrics, given by (2.38) and (2.39) respectively, can be used as new figure of merits to compare SC topologies.

$$M_{RSSL} = \frac{F_C^2}{V_{IN}} = \frac{\left(\sum_{i\in caps}\left|a_{c,i}\right|\sqrt{V_{c,rate,i}}\right)^2}{V_{IN}} \tag{2.38}$$

$$M_{RFSL} = \frac{F_{sw}^2}{V_{IN}} = \frac{\left(\sum_{i \in switches} |a_{r,i}| \sqrt{V_{r,rate,i}}\right)^2}{V_{IN}} \quad (2.39)$$

where M_{RSSL} is the SSL impedance metric, and M_{RFSL} is the FSL impedance metric. Both of those two metrics are solely depend on converter topology. Thus one can use those two metrics to compare the performance of different converter topologies.

2.5.1 Series-Parallel Topology

A generic two phases 1: N series-parallel topology switched capacitor converter is shown in Figure 2.7. The converter consists of N-1 stages to provide a 1: N voltage conversion ratio. Each stage contains one capacitor and three switches. During the charging phase (noted with 1 in Figure 2.7), charging switches S_{CUi} and S_{CDi} are conducting and charge the flying capacitors with input source, and pumping switches S_{Pi} are open. During the pumping phase (noted with 2 in Figure 2.7), all charging switches S_{CUi} and S_{CDi} are open, and pumping switches S_{Pi} are conduct and all flying capacitors are series connected with input source to charge the output load. All flying capacitors and all but not the last pumping switches need only to block a voltage equals to input voltage, which is the lowest voltage. The last pumping switch which connected with output need to block a voltage equals to $N - 1$ times of input voltage. And the charging switches in the stage of $N - 1$ also need to sustain $N - 1$ times of input voltage.

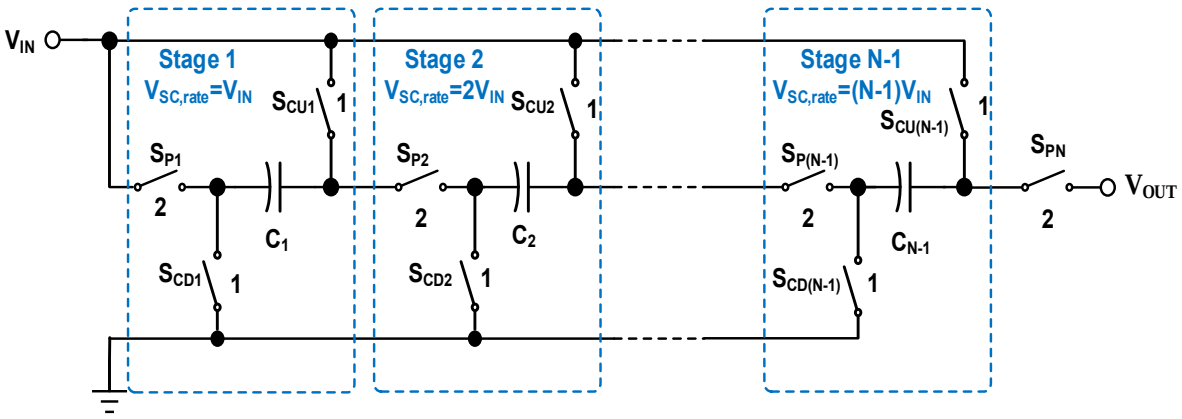

Figure 2.7. A generic 1:N series-parallel topology

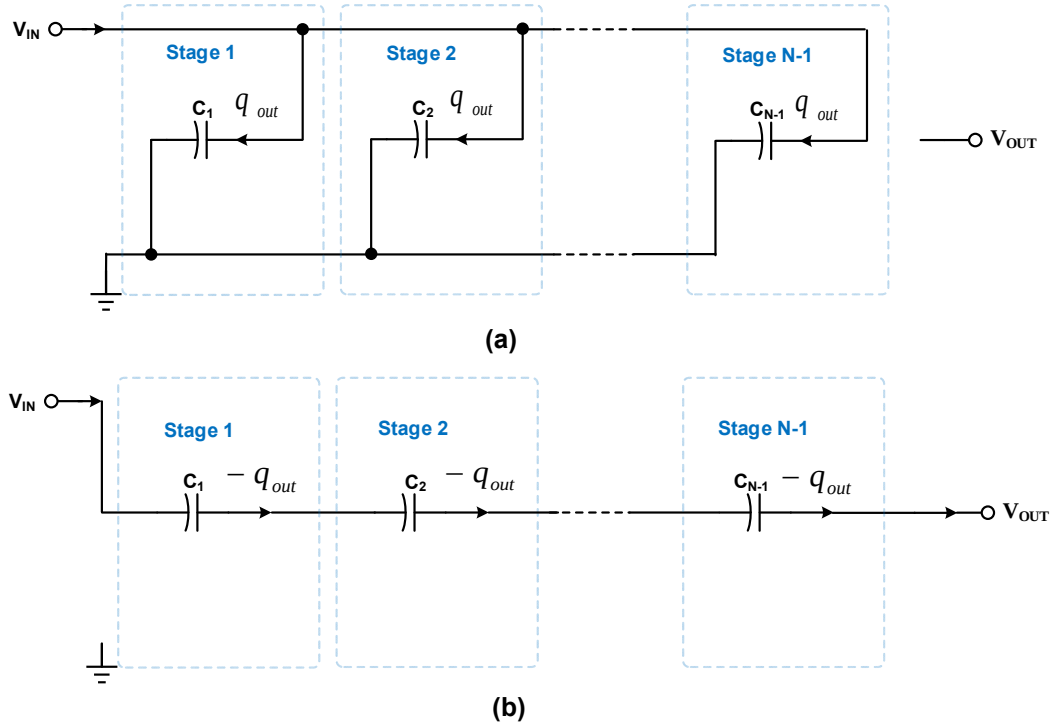

Figure 2.8. Capacitor charge flow in Series-Parallel converter. (a) charging phase (b) pumping phase

By inspection of Figure 2.8, the capacitor charge multiplier vectors and capacitor blocking voltages of a series-parallel converter is given by Table 2.2.

Capacitor	C_1	C_2	C_3	⋯	C_{N-1}
α_c^1	1	1	1	⋯	1
α_c^2	-1	-1	-1	⋯	-1
$V_{c,rate}\,[V_{IN}]$	1	1	1	⋯	1

Table 2.2. Series-Parallel topology capacitor charge multiplier vector and blocking voltages

Thus, the series-parallel topology capacitor factor can easily be found as:

$$F_C = \sum_{i \in caps} |a_{c,i}| \sqrt{V_{c,rate,i}} = (N-1)\sqrt{V_{IN}} \tag{2.40}$$

The SSL impedance metric can easily be computed from (2.40):

$$M_{RSSL} = (N-1)^2 \tag{2.41}$$

The switch charge multiplier vector and switch blocking voltages of a series-parallel converter can also be observed from Figure 2.9 and are listed in Table 2.3.

Switch	$\boldsymbol{S_{CU1}}$	$\boldsymbol{S_{CD1}}$	⋯	$\boldsymbol{S_{CU(N-1)}}$	$\boldsymbol{S_{CD(N-1)}}$	$\boldsymbol{S_{P1}}$	$\boldsymbol{S_{P2}}$	⋯	$\boldsymbol{S_{P(N-1)}}$	$\boldsymbol{S_{PN}}$
$\boldsymbol{\alpha_r^1}$	-1	1	⋯	-1	1	0	0	⋯	0	0
$\boldsymbol{\alpha_r^2}$	0	0	⋯	0	0	1	1	⋯	1	1
$\boldsymbol{V_{r,rate}\,[V_{IN}]}$	1	1	⋯	N-1	N-1	1	1	⋯	1	N-1

Table 2.3. Series-Parallel topology switch charge multiplier vector and switch blocking voltages

Thus, the series-parallel topology switch factor and FSL impedance metric can be computed from Table 2.3:

$$F_{sw} = \sum_{i \in switches} |a_{r,i}| \sqrt{V_{r,rate,i}} = \left(2 \sum_{i=1}^{N-1} \sqrt{i} + N - 1 + \sqrt{N-1} \right) \sqrt{V_{IN}} \quad (2.42)$$

$$M_{RFSL} = \left(2 \sum_{i=1}^{N-1} \sqrt{i} + N - 1 + \sqrt{N-1} \right)^2 \quad (2.43)$$

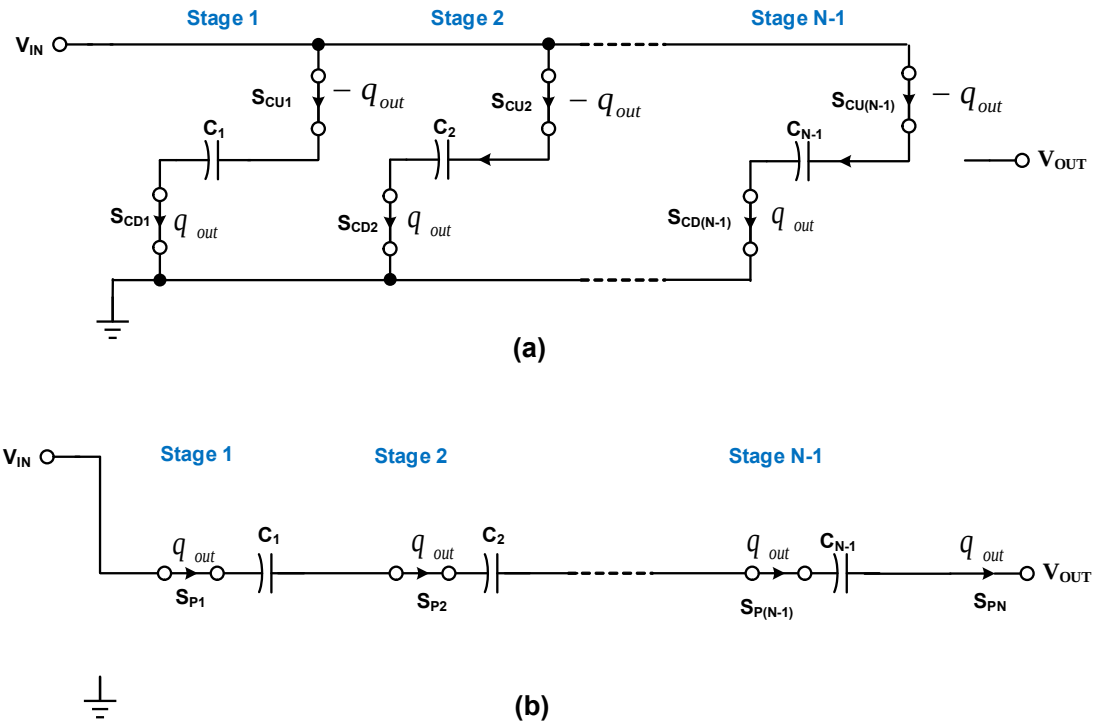

Figure 2.9. Switch charge flow in Series-Parallel converter. (a) charging phase (b) pumping phase

2.5.2 Dickson Topology

An 1:N generic two phases Dickson topology [23][24] is shown in Figure 2.10. Similar to the series-parallel topology, Dickson topology also uses a number of N-1 capacitors to generate the 1:N conversion ratio. But unlike the series-parallel topology, the capacitors used in a Dickson topology need to have different blocking voltages. A 1:N Dickson topology converter uses N+4 power switches, includes four switches generate

voltage biasing for capacitor bottom plates and N switches series connected between input and output source. All series-connected power switches are phase alternately. Odd-numbered switches turn on in phase one, and even-numbered switches turn on in phase two.

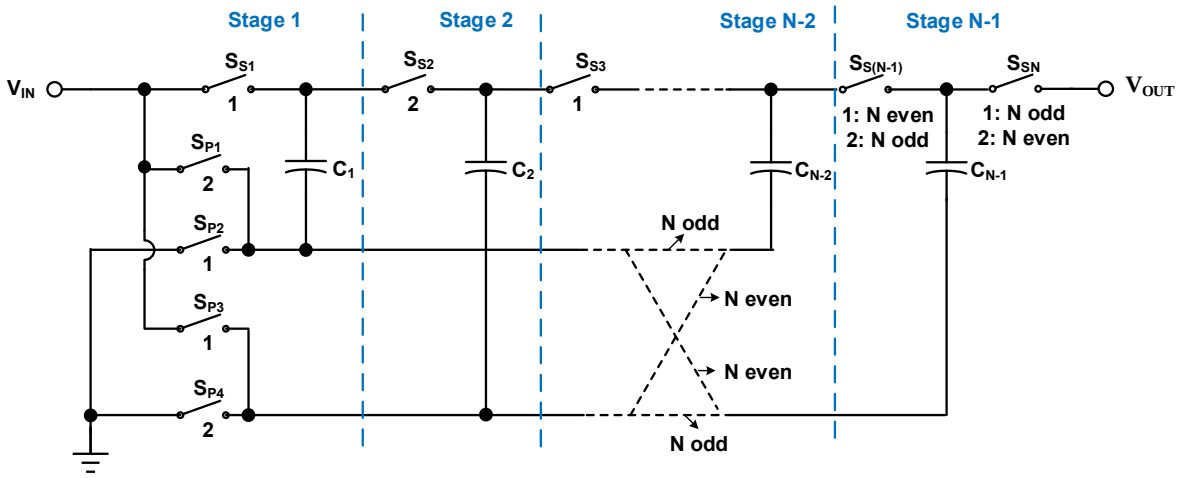

Figure 2.10. A generic 1: N Dickson topology

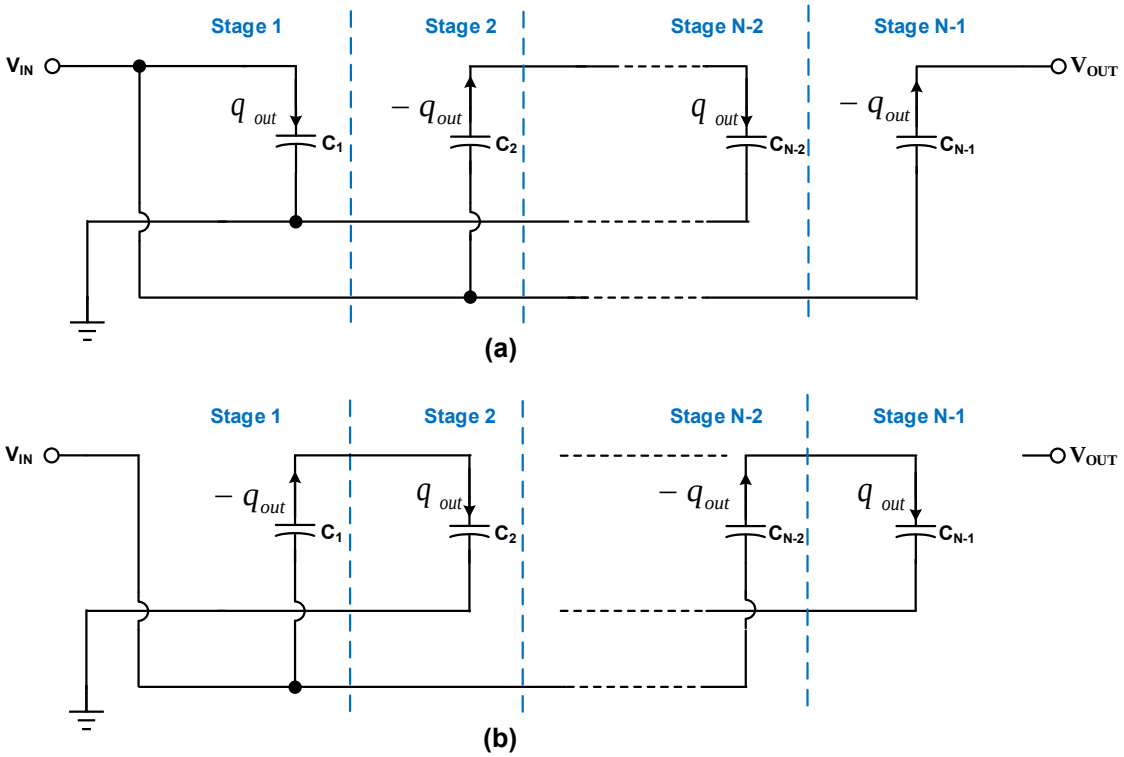

Figure 2.11. Capacitor charge flow in Dickson converter (N: odd) (a) phase 1, (b) phase 2

Figure 2.11 shows all flying capacitors charging and discharging alternately. The capacitor charge multiplier can be found by inspection. The C_{N-1} has a charge multiplier of $|a_{c,N-1}|$ equals to 1 as it pumps charge to the output during phase one. And in phase two, the C_{N-2} transfers the same amount of charge to the C_{N-1}. Thus the C_{N-2} has a charge multiplier of magnitude 1, but with an opposite sign to the charge multiplier of C_{N-1}. Charge multipliers of other capacitors can be found by the same method and are given in Table 2.4:

Capacitor	C_1	C_2	C_3	C_3	⋯	C_{N-1}
α_c^1	1	-1	1	-1	⋯	$\begin{cases} 1 & N\ odd \\ -1 & N\ even \end{cases}$
α_c^2	-1	1	-1	1	⋯	$\begin{cases} -1 & N\ odd \\ 1 & N\ even \end{cases}$
$V_{c,rate}\ [V_{IN}]$	1	2	3	4	⋯	N-1

Table 2.4. Dickson topology capacitor charge multiplier vector and capacitor blocking voltages

Thus, the Dickson topology capacitor factor and FSL impedance metric can be computed from Table 2.4:

$$F_C = \sum_{i \in caps} |a_{c,i}| \sqrt{V_{c,rate,i}} = \sum_{i}^{N-1} \sqrt{i}\, \sqrt{V_{IN}} \tag{2.44}$$

$$M_{RSSL} = \left(\sum_{i}^{N-1} \sqrt{i} \right)^2 \tag{2.45}$$

Figure 2.12 shows an 1:N (N is an odd number) Dickson converter charge flows in the switches during both phases. The switch blocking voltages and charge multipliers can be found by inspecting Figure 2.12 and are given in Table 2.5.

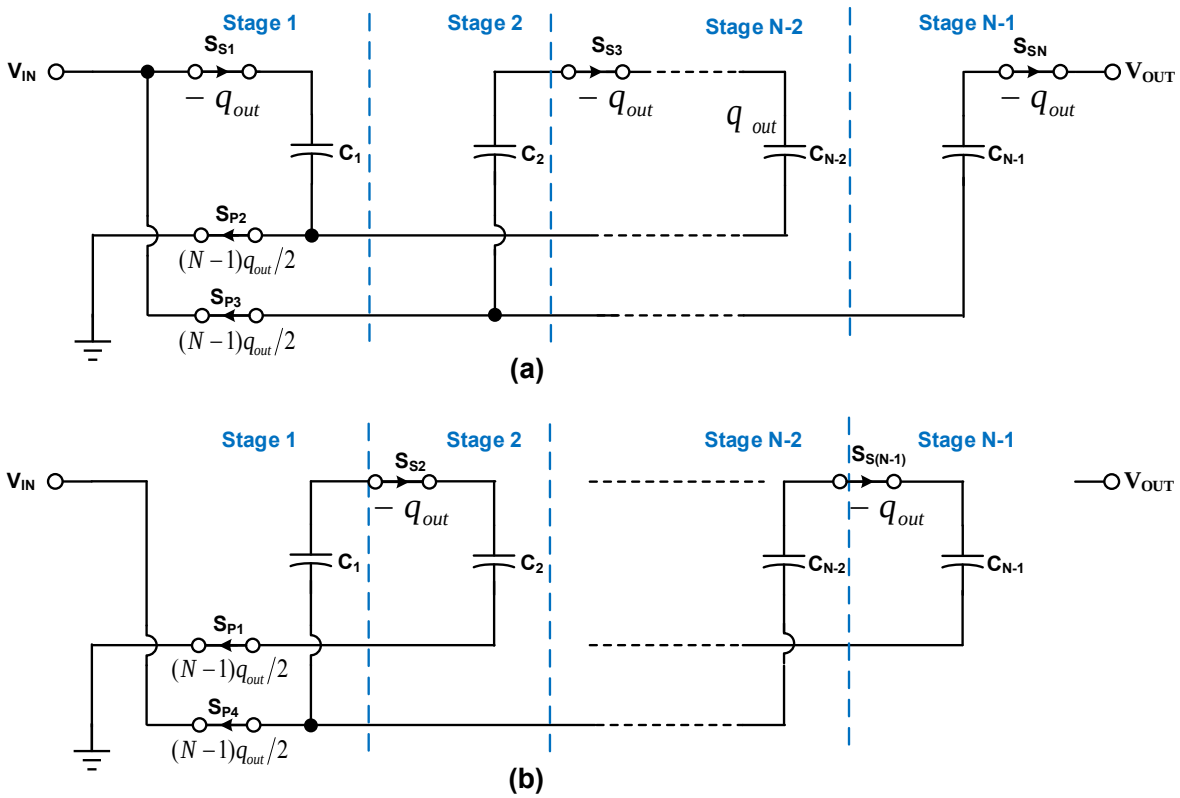

Figure 2.12. Switch charge flow in Dickson converter (N: odd) (a) phase 1, (b) phase 2

Switch	S_{P1}	S_{P2}	S_{P3}	S_{P4}	S_{S1}	S_{S2}	S_{S3}	⋯	$S_{S(N-2)}$	$S_{S(N-1)}$	S_{SN}
N: odd number											
α_r^1	0	$\frac{N-1}{2}$	$\frac{N-1}{2}$	0	-1	0	-1	⋯	-1	0	-1
α_r^2	$\frac{N-1}{2}$	0	0	$\frac{N-1}{2}$	0	-1	0	⋯	0	-1	0
$V_{r,rate}\ [V_{IN}]$	1	1	1	1	1	2	2	⋯	2	2	1
N: even number											
α_r^1	0	$\frac{N}{2}$	$\frac{N}{2}-1$	0	-1	0	-1	⋯	0	-1	0
α_r^2	$\frac{N}{2}$	0	0	$\frac{N}{2}-1$	0	-1	0	⋯	-1	0	-1
$V_{r,rate}\ [V_{IN}]$	1	1	1	1	1	2	2	⋯	2	2	1

Table 2.5. Dickson topology switch charge multiplier vector and switch blocking voltages

From Table 2.5, the Dickson topology capacitor factor and FSL impedance metric can be easily calculated:

$$F_{sw} = \sum_{i \in switches} |a_{r,i}| \sqrt{V_{r,rate,i}} = (2N + \sqrt{2}(N-2)) \sqrt{V_{IN}} \tag{2.46}$$

$$M_{RFSL} = (2N + \sqrt{2}(N-2))^2 \tag{2.47}$$

2.5.3 Ladder Topology

A two phases ladder topology [9][25] is shown in Figure 2.13. Unlike series-parallel and Dickson topologies, ladder topology needs to use 2N-3 capacitors to generates an 1:N conversion ratio. Thus this topology is not favorable while designing a SC converter using discrete components as it requires more capacitors than other topologies. However, in a step-up converter application, all capacitors and power switches used in a ladder topology converter need only to block a voltage equals to the input voltage, which is normally a low voltage. Thus a ladder topology converter generates a high output voltage can be easily implemented by using fully on-chip low voltage devices.

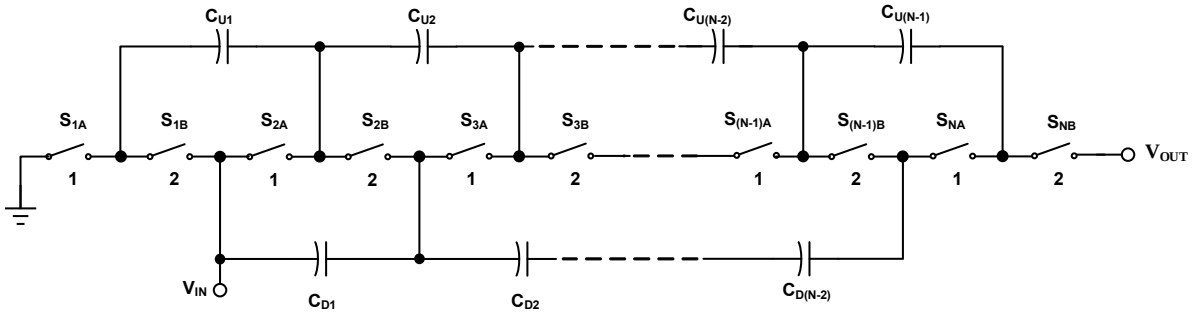

Figure 2.13. A generic 1: N ladder topology

As shown in Figure 2.13, those 2N-3 capacitors used in a ladder topology converter can be divided into two groups of series connected capacitors. The lower group of capacitors

defines a set of DC potentials at integer multiples of the input voltage, and the upper group of capacitors fly alternately to pump the charge from input to output. Figure 2.14 shows the capacitor charge flow in a ladder topology converter. Similar with Dickson topology, the capacitor charge multipliers can be found, starting from the capacitor closest to the output. In phase two, the $C_{U(N-1)}$ pumps the charge to the output source and resulting in its charge multiplier of $|a_{c,N-1}|$ equals to 1. $C_{U(N-1)}$ also charged by $C_{D(N-2)}$ with the same amount of charge during the phase one. Thus, charge multipliers of $C_{U(N-1}$ and $C_{D(N-2)}$ have an identical absolute value but opposite sign. Charge multipliers of other capacitors can be found by the same way and are given in Table 2.6.

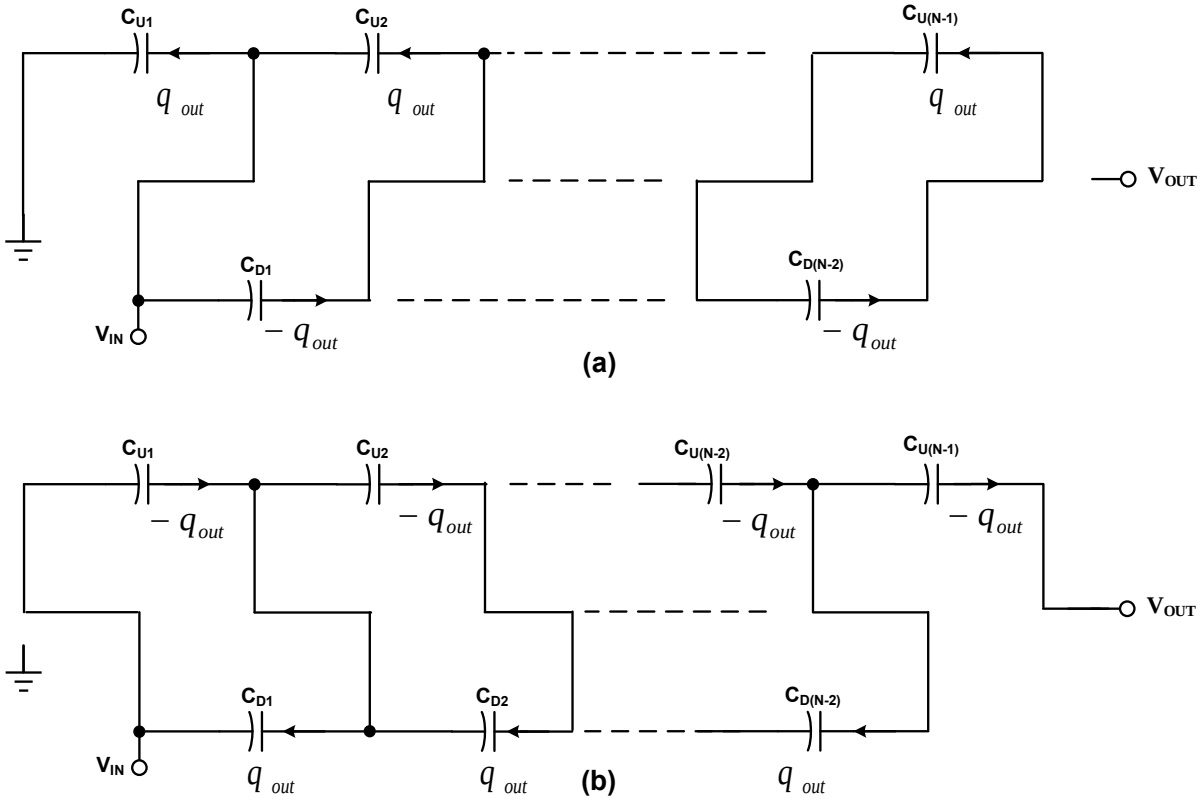

Figure 2.14. Capacitor charge flow in ladder converter (a) phase 1, (b) phase 2

Capacitor	C_{U1}	C_{D1}	C_{U2}	C_{D2}	⋯	$C_{U(N-2)}$	$C_{D(N-2)}$	$C_{U(N-1)}$
α_c^1	1	-1	1	-1	⋯	1	-1	1
α_c^2	-1	1	-1	1	⋯	-1	1	-1
$V_{c,rate}\ [V_{IN}]$	1	1	1	1	⋯	1	1	1

Table 2.6. Ladder topology capacitor charge multiplier vector and capacitor blocking voltages

The ladder topology capacitor factor and SSL impedance metric can be computed from Table 2.6:

$$F_C = \sum_{i \in caps} |a_{c,i}| \sqrt{V_{c,rate,i}} = (2N-3)\sqrt{V_{IN}} \tag{2.48}$$

$$M_{RSSL} = (2N-3)^2 \tag{2.49}$$

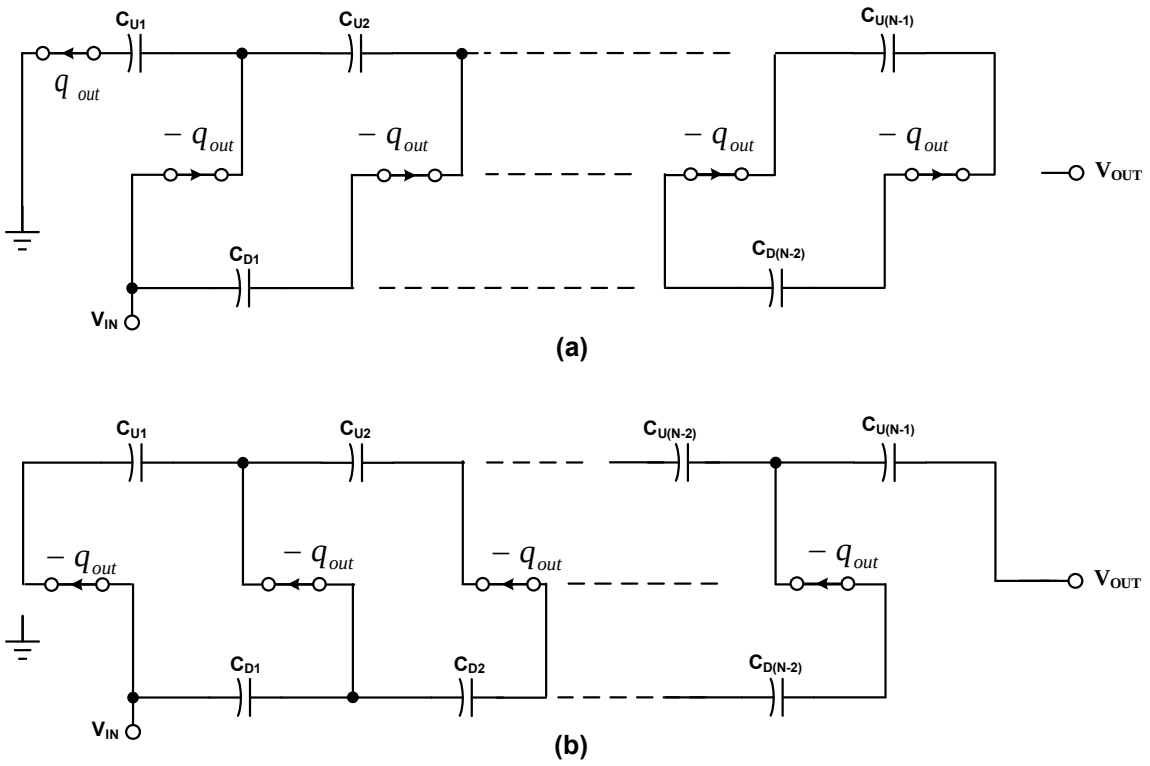

Figure 2.15. Switch charge flow in ladder converter (a) phase 1, (b) phase 2

From the switch charge flow shown in Figure 2.15, one can easily find out the switch charge multiplier by looking at its adjacent capacitor charge multiplier. The ladder topology switch blocking voltages and charge multipliers is given in Table 2.7.

Switch	S_{1A}	S_{1B}	S_{2A}	S_{2B}	⋯	S_{NA}	S_{NB}
α_r^1	1	0	-1	0	⋯	-1	0
α_r^2	0	-1	0	-1	⋯	0	-1
$V_{r,rate}$ $[V_{IN}]$	1	1	1	1	⋯	1	1

Table 2.7. Ladder topology switch charge multiplier vector and switch blocking voltages

From Table 2.7, the ladder topology capacitor factor and FSL impedance metric can be easily computed:

$$F_{sw} = \sum_{i \in switches} |a_{r,i}| \sqrt{V_{r,rate,i}} = 2N\sqrt{V_{IN}} \tag{2.50}$$

$$M_{RFSL} = 4N^2 \tag{2.51}$$

2.5.4 Fibonacci Topology

Unlike other topologies discussed earlier, the Fibonacci topology can only generate a 1:N conversion ratio which N belongs to a Fibonacci number. Thus it's a non-linear converter topology. Literature [7] proved Fibonacci topology performs the highest conversion ratio for a given numbers of capacitors. Figure 2.16 shows a generic K stages Fibonacci converter. A K-stages Fibonacci converter exhibits a conversion ratio of $N = F_{K+2}$, where F_{K+2} is the $(K+2)^{th}$ Fibonacci number. Each stage consists of one capacitor and three power switches. In previous work [9] the charge multipliers and blocking voltages

of capacitors and switches are provided. Table 2.7 relists Fibonacci topology capacitor charge multipliers and capacitor blocking voltages; Table 2.8 relists Fibonacci topology switch charge multipliers and switch blocking voltages.

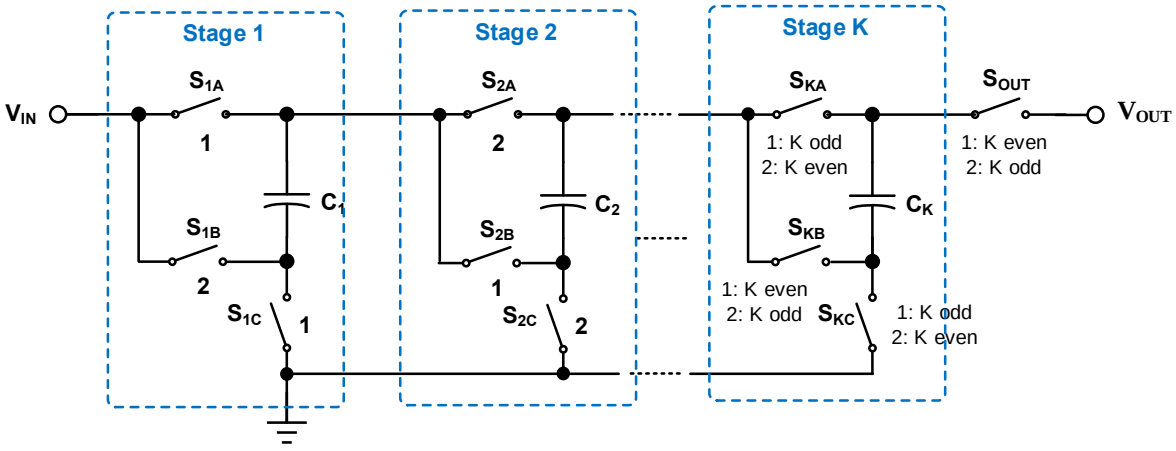

Figure 2.16. A generic K stages Fibonacci topology

Capacitor	C_1	C_2	⋯	C_{K-3}	C_{K-2}	C_{K-1}	C_K
$\lvert\alpha_c^i\rvert$	F_K	F_{K-1}	⋯	3	2	1	1
$V_{c,rate}\ [V_{IN}]$	1	2	⋯	F_{K-2}	F_{K-1}	F_K	F_{K+1}

Table 2.8. Fibonacci topology capacitor charge multiplier vector and capacitor blocking voltages

Switch	S_{1A}	S_{1B}	S_{1C}	S_{2A}	S_{2B}	S_{2C}	⋯	S_{KA}	S_{KB}	S_{KC}	S_{OUT}
$\alpha_r^1 + \alpha_r^2$	F_{K+1}	F_K	F_K	F_K	F_{K-1}	F_{K-1}	⋯	1	1	1	1
$V_{r,rate}\ [V_{IN}]$	1	1	1	2	2	1	⋯	F_{K+1}	F_{K+1}	F_K	F_K

Table 2.9. Fibonacci topology switch charge multiplier vector and switch blocking voltages

The Fibonacci topology capacitor factor and SSL impedance metric can be computed from Table 2.8:

$$F_C = \sum_{i \in caps} |a_{c,i}| \sqrt{V_{c,rate,i}} = \sum_{i}^{K} F_{i+1} \sqrt{F_{K-i+1}} \sqrt{V_{IN}} \tag{2.52}$$

$$M_{RSSL} = \left(\sum_{i}^{K} F_{i+1} \sqrt{F_{K-i+1}} \right)^2 \tag{2.53}$$

Numeric SSL impedance metric is calculated:

$$M_{RSSL} = \{1, 5.828, 26.48, 96.97, \cdots\} \tag{2.54}$$

The Fibonacci topology FSL impedance metric is difficult or impossible to be calculated in a closed-form expression. Thus a sequence of numeric result of FSL impedance metric is given:

$$M_{RFSL} = \{16, 77.941, 343.55, 1198.4, \cdots\} \tag{2.55}$$

2.5.5 SSL Impedance Metric and FSL Impedance Metric Comparison

In Figure 2.17 and Figure 2.18 the SSL impedance metric and the FSL impedance metric of four different topologies are plotted. Among those four topologies, series-parallel topology has the best (lowest) SSL impedance metric, which means series-parallel topology has the smallest SSL impedance for a given total capacitor area. Thus in a SSL operating condition, series-parallel converter has the highest power conversion efficiency for a given output power. On the other hand, ladder topology has the best (lowest) FSL impedance metric, which means for a given total switch area, the ladder converter has the smallest FSL impedance. Thus ladder converter can achieve the highest power conversion efficiency in a FSL operating condition.

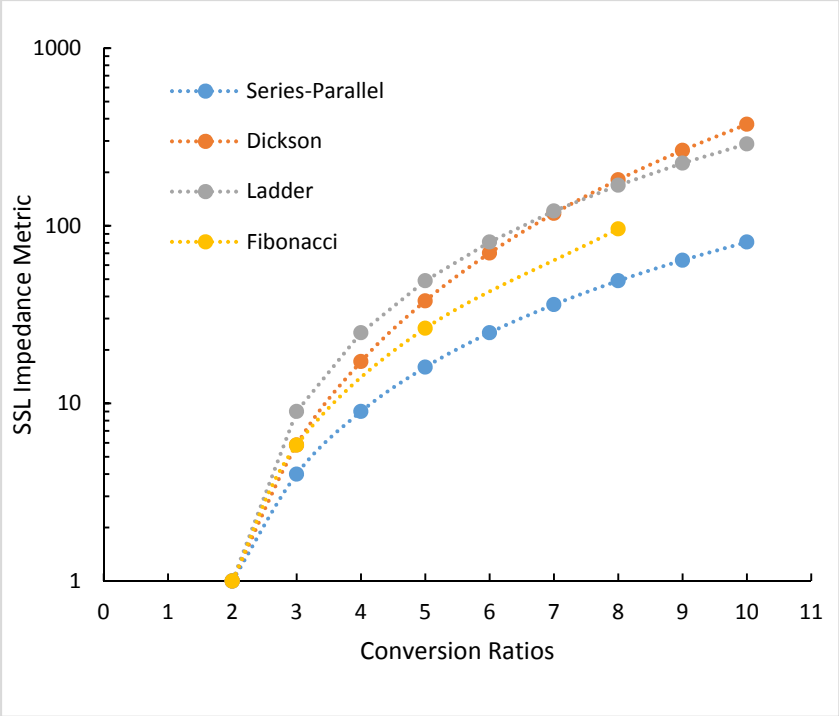

Figure 2.17. SSL Impedance Metric among 4 different topologies

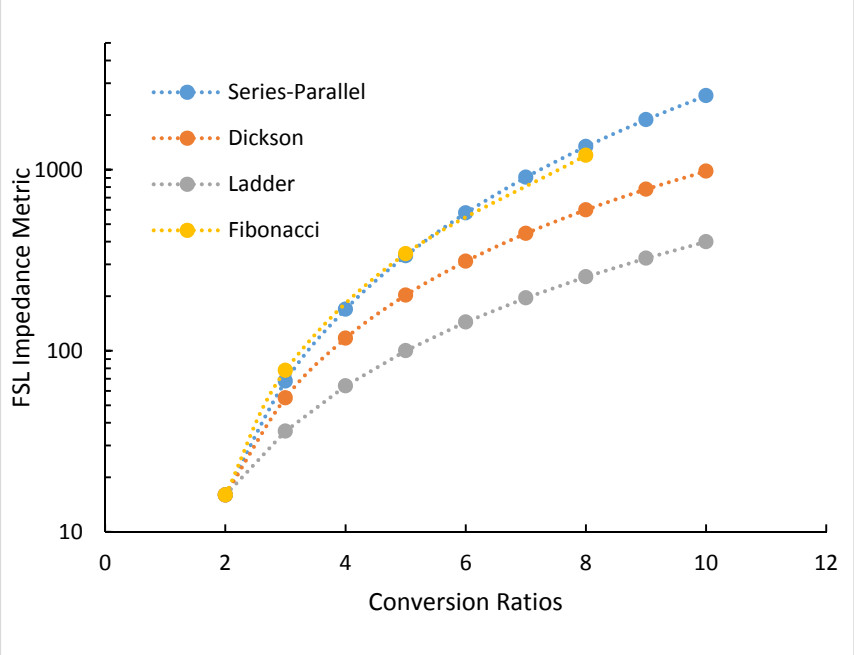

Figure 2.18. FSL Impedance Metric among 4 different topologies

In the case that both capacitors and switches are integrated into a single-chip power conversion system, optimizing the ratio between capacitor area and switch area for a given total area are also important. As shown in Figure 2.17 and Figure 2.18, for a given conversion ratio, FSL impedance metric is significantly larger than SSL impedance metric. However, optimization of the ratio between capacitor area and switch area for a given total system area to minimize the total converter output impedance is implementation dependent and will be discussed in next chapter.

Figure 2.17 and Figure 2.18 also indicate all of the four different topologies has the same impedance metrics when the conversion ratio reduced to two. It's because all topologies will collapse to a basic voltage doubler in this case, which is shown in Figure 2.19.

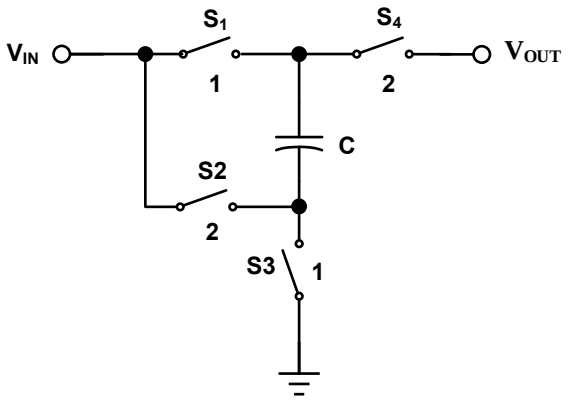

Figure 2.19. Voltage Doubler

Capacitor and switch blocking voltages information discussed in this section provides a feasibility guideline for choosing a topology to be used in a fully integrated high voltage converter application. All switches and capacitors in a Ladder topology converter need only to block a voltage equals to the input voltage in a 1: N conversion application. Thus a ladder

converter can be implemented with a standard low voltage technology. For a series-parallel topology, while all of its capacitors need only to block low voltages, its power switches need to be implemented by high voltage power transistors to provide high voltage blocking capability. Thus an integrated series-parallel converter with high output voltages usually need to use HV-CMOS technology or a DMOS technology. The capacitor blocking voltages of both Dickson and Fibonacci topologies are not fixed and increase with the increase of the conversion ratio. Thus they are not ideal for fully integrated applications. As in a standard process, on-chip capacitors only have a few voltage rating options, and on-chip capacitors with high voltage rating is very rare.

CHAPTER 3

3 Architecture Design of Liquid Crystal Lens Driver

3.1 SC-DCDC Converter Topology Choice

Chapter 2 discusses the fundamentals of switched capacitor converters, including a method of determining their output impedance and optimizing their performance in SSL and FSL operating conditions. Several switched capacitor topologies are compared based on the SSL impedance metric and the FSL impedance metric. As discussed in section 2.55, a series-parallel topology has the smallest SSL output impedance for a given capacitor area; while a ladder topology has the smallest FSL output impedance for a given switch area. Both of these two topologies are easy to be fully integrated. One needs to choose a topology to achieve the minimal total output impedance for a given total area.

In order to compare the total output impedance of different converter topologies, a relationship between the total output impedance and converter topology metrics must be found. Since both optimized SSL impedance and optimized FSL impedance have been developed in chapter 2, they can be combined to perform an overall comparison. For a given total area A_{tot}, the capacitor area A_C and the switch area A_{SW} can be given by:

$$A_C = KA_{tot} \tag{3.1}$$

$$A_{SW} = (1 - K)A_{tot} \tag{3.2}$$

where $0 \leq K \leq 1$, substitute (3.1) and (3.2) into (2.26) and (2.37), the optimized impedance are given by:

$$R_{SSL}^{*} = \frac{F_C^2}{f_{SW} Q_{\square} A_{tot}} \cdot \frac{1}{K} = \frac{a}{K} \tag{3.3}$$

$$R_{FSL}^{*} = \frac{2R_{\square}^{*} F_{sw}^2}{A_{tot}} \cdot \frac{1}{1 - K} = \frac{b}{1 - K} \tag{3.4}$$

where F_C and F_{sw} are topology dependent; $Q_{\square}$ and $R_{\square}^{*}$ are technology dependent, and coefficients a and b are defined by:

$$a = \frac{F_C^2}{f_{SW} Q_{\square} A_{tot}} \tag{3.5}$$

$$b = \frac{2R_{\square}^{*} F_{sw}^2}{A_{tot}} \tag{3.6}$$

Rewrite (2.6), the converter total output impedance can be calculated by:

$$R_{OUT} = \sqrt{R_{SSL}^{*2} + R_{FSL}^{*2}} = \sqrt{\frac{a^2}{K^2} + \frac{b^2}{(1 - K)^2}} \tag{3.7}$$

R_{OUT} is minimized by equaling its partial derivative respect to K with zero:

$$\frac{\partial R_{OUT}}{\partial K} = \frac{\partial}{\partial K} \sqrt{\frac{a^2}{K^2} + \frac{b^2}{(1 - K)^2}} = 0 \tag{3.8}$$

This partial differential equation can be solved via a Maple™ program and the result is given by:

$$K_{opt} = \frac{b(a^2 b)^{1/3} + a^2}{a^2 + b^2} - \frac{a^2 b}{(a^2 + b^2)(a^2 b)^{1/3}} \tag{3.9}$$

Substitute (3.9) into (3.7), the minimized converter output impedance is given by:

$$R_{OUT\_MIN} = \sqrt{\frac{a^2}{\left(\frac{b(a^2b)^{1/3}+a^2}{a^2+b^2} - \frac{a^2b}{(a^2+b^2)(a^2b)^{1/3}}\right)^2} + \frac{b^2}{(1-\frac{b(a^2b)^{1/3}+a^2}{a^2+b^2} + \frac{a^2b}{(a^2+b^2)(a^2b)^{1/3}})^2}} \quad (3.10)$$

For a given technology information and total area, (3.10) can be used to compute the converter minimal output impedance. The total output impedances of a series-parallel converter and a ladder converter are computed numerically for comparison. And three different capacitor implementations are consider: using off-chip capacitor, using MIM capacitor and using deep-trench capacitor. The capacitor densities and rating voltages are listed in Table 3.1.

Capacitor Type	*Off-Chip AVX 0402*	*MIM CSMC*	*Deep-Trench [26]*
$C_{\square}$ [nF/mm^2]	*2750*	*1.5*	*116*
$V_{c,rate}$ [V]	*6.3*	*5.5*	*18*
$Q_{\square}$[nC/mm^2]	*17325*	*8.25*	*2088*

Table 3.1. Capacitor density

A converter with 1:5 conversion ratio and 5V input voltage is consider. And this converter is assumed to be integrated with a CSMC BCD technology. The total area is fixed for comparison: in an off-chip capacitor implementation, the total area summed by on-chip switch area and off-chip capacitor area is set to $10mm^2$; in a fully on-chip implementation, the total size of on-chip capacitor and switcher are also set to $10mm^2$. The normalized

LDMOS on-resistance $R_{\square}^{*}$ per unit of silicon area in CSMC BCD technology can be extracted from Figure 2.5 and equals to $1.39m\Omega \cdot mm^2/V$. The square of capacitor topology factor and the square of switch topology factor for a 1:5 converter are also list in Table 3.2.

Topology	*Series-Parallel*	*Ladder*
$F_C^2\ [V_{IN}]$	*16*	*49*
$F_{SW}^2\ [V_{IN}]$	*334.6*	*100*

Table 3.2. Topology factors of converters with 1:5 conversion ratio

Thus, coefficients a and b can be calculated and listed in Table 3.3.

Topology	*Series-Parallel*			*Ladder*		
Capacitor Type	*Off-Chip*	*MIM*	*Deep-Trench*	*Off-Chip*	*MIM*	*Deep-Trench*
$a[\Omega]: f = 1MHz$	*461.76*	*969697*	*3831.4*	*1414.14*	*2969697*	*11733.7*
$a[\Omega]: f = 100KHz$	*4617.6*	*969697*	*38314*	*14141.4*	*29696970*	*117337*
$b[\Omega]$		*0.4651*			*0.139*	

Table 3.3. Converter output impedance coefficients

The total output impedances of converters with different capacitor implementations are plotted. Figure 3.1-Figure 3.3 indicates the majority area should be allocated to implement capacitors. This is caused by the fact that the SSL impedance is much higher than the FSL impedance if the converter operating in a relatively low frequency (less than 1MHz). Moreover, Figure 3.1-Figure 3.3 shows the series-parallel topology has a lower total output

impedance than the ladder topology in an area constraint. Thus series-parallel topology should be chosen for system miniaturization.

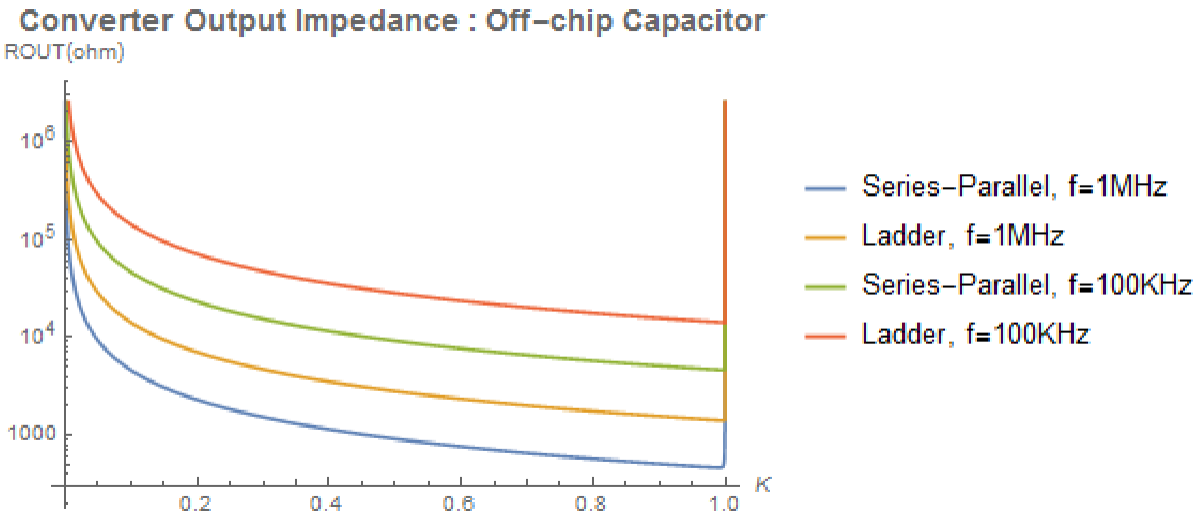

Figure 3.3.1. Total converter output impedance: off-chip capacitor implementation

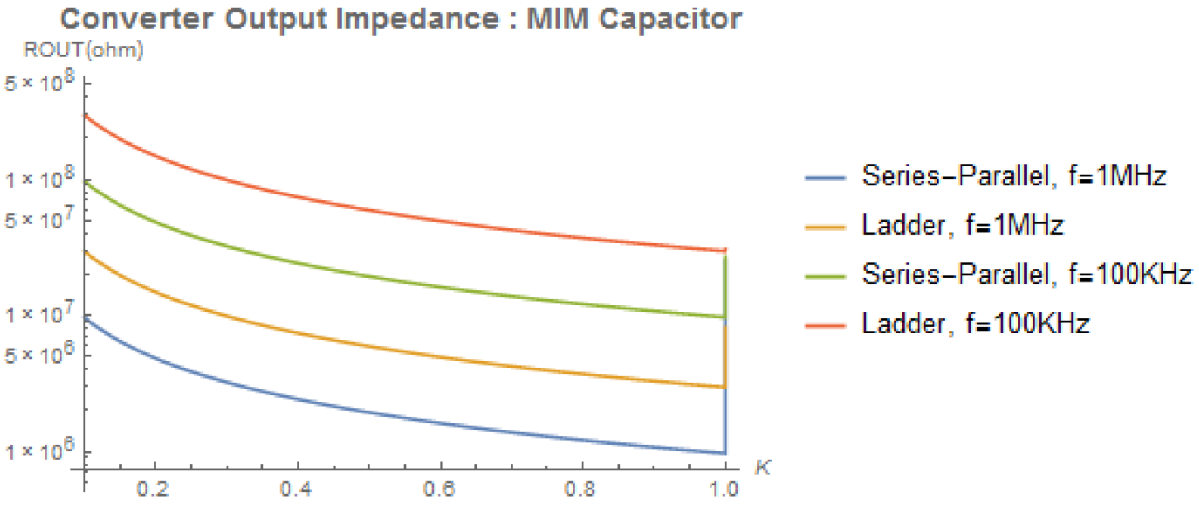

Figure 3.3.2. Total converter output impedance: MIM capacitor implementation

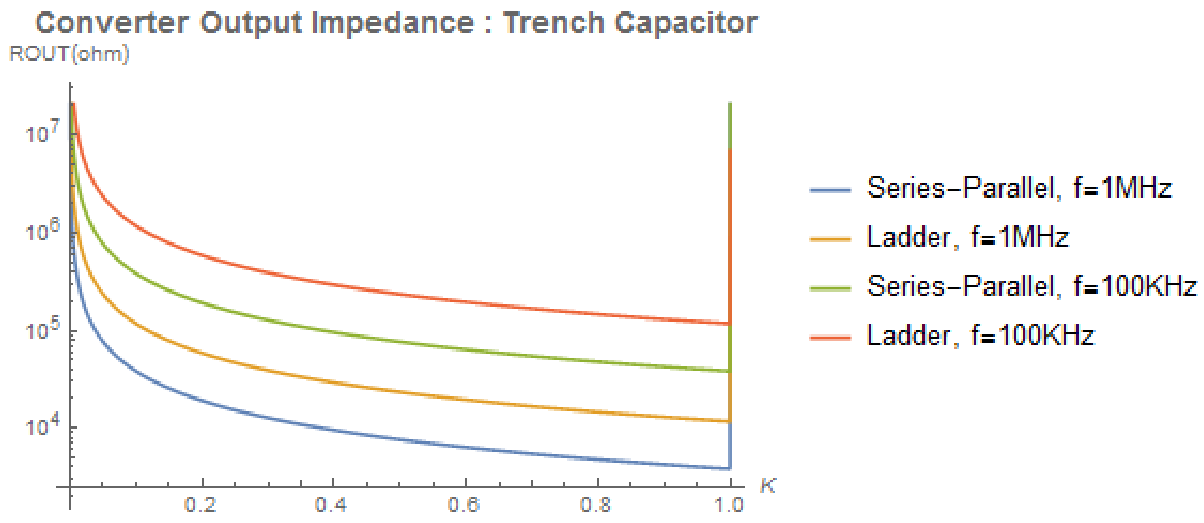

Figure 3.3.3. Total converter output impedance: deep-trench capacitor implementation

3.2 Overall System Optimization

After the relative sizes of the flying capacitors and the switches are determined, the next step is to optimize the total area A_{tot} and switching frequency f_{SW} for the converter. As discussed in section 3.1, the capacitor area is the primary constraint in converter performance, the ratio between capacitor area and total area can be computed by the method provided in section 3.1. In this section, the overall converter efficiency will be optimized for a given total capacitor size and a fixed output current. The converter optimization procedure is to find out the converter loss components and then use numerical method to find out the highest conversion efficiency over the design space.

There are four loss components associate with a high voltage fully integrated switched capacitor converter. The first one is the converter output impedance loss. This loss is due to the power loss in the component of the output impedance related to charge transfer.

As discussed in section 3.1, the optimized total output impedance R_{OUT_MIN} is given by (3.10). Thus the total output impedance loss can be calculated as:

$$P_{ROUT} = I_{OUT}^2 R_{OUT\_MIN}$$

$$= I_{OUT}^2 \left\{ \frac{a^2}{\left(\frac{b(a^2b)^{1/3} + a^2}{a^2 + b^2} - \frac{a^2 b}{(a^2 + b^2)(a^2 b)^{1/3}} \right)^2} + \frac{b^2}{\left(1 - \frac{b(a^2b)^{1/3} + a^2}{a^2 + b^2} - \frac{a^2 b}{(a^2 + b^2)(a^2 b)^{1/3}}\right)^2} \right\} \tag{3.11}$$

where a and b are given by (3.5) and (3.6), respectively.

The next loss component is the switching loss associated with the power switches parasitic capacitors during converter switching. This loss component can be expressed as:

$$P_{SW} = f_{sw} \sum_{i \in switches} [(C_{GS} + C_{GD}) V_G^2 + C_{DS} V_{DS}^2) \tag{3.12}$$

where C_{GS}, C_{GD} and C_{DS} are gate-source capacitance, gate-drain capacitance and drain-source capacitance, respectively. Those three capacitance are non-linear and they are given by:

$$\begin{cases} C_{GS} = (\int C_{gs} \cdot v_g)/V_G \\ C_{DS} = (\int C_{ds} \cdot v_g)/V_G \\ C_{GD} = (\int C_{gd} \cdot v_{ds})/V_{DS} \end{cases} \tag{3.13}$$

Calculating those parasitic capacitances are quite complicate thus normally gate charge is used to calculate the switching loss. LDMOS transistors gate charge information is

given in a technology specification or can be measured in the lab. Thus, the converter switching loss associated can also be written as:

$$P_{SW} = f_{sw} \sum_{i \in switches} Q_{sw} V_G \tag{3.14}$$

where Q_{sw} is the LDMOS transistor gate charge during switching and V_G is the gate drive voltage.

The third loss component is due to the bottom-plate parasitic capacitance of the on-chip capacitors. This parasitic capacitance is highly related to the implementation of on-chip capacitor. For a most commonly used metal-insulator-metal (MIM) capacitor, the parasitic capacitance between its bottom metal plane and the substrate can be as high as 5% of its capacitance [27]. In a fully integrated converter, this loss component is dominant [28] and sets the power conversion efficiency limit of the converter. Charge recycling technique [29] can be used to minimize the parasitic bottom plate capacitor power loss. But this technique is limited to a certain converter topology. Thus deep-trench capacitor is favorable in implementing a fully on-chip SC due to its high capacitance density and low parasitic capacitance.

In a 1:N series-parallel converter, the bottom plate capacitor is charged and discharged during every switching cycle, as shown in Figure 3.4. The bottom plate capacitor loss can be calculated by:

$$P_{CAP} = \alpha C_f V_{IN}^2 \sum_{k=1}^{N-1} k^2 \tag{3.15}$$

where α is the ratio between the parasitic capacitor and the main capacitor.

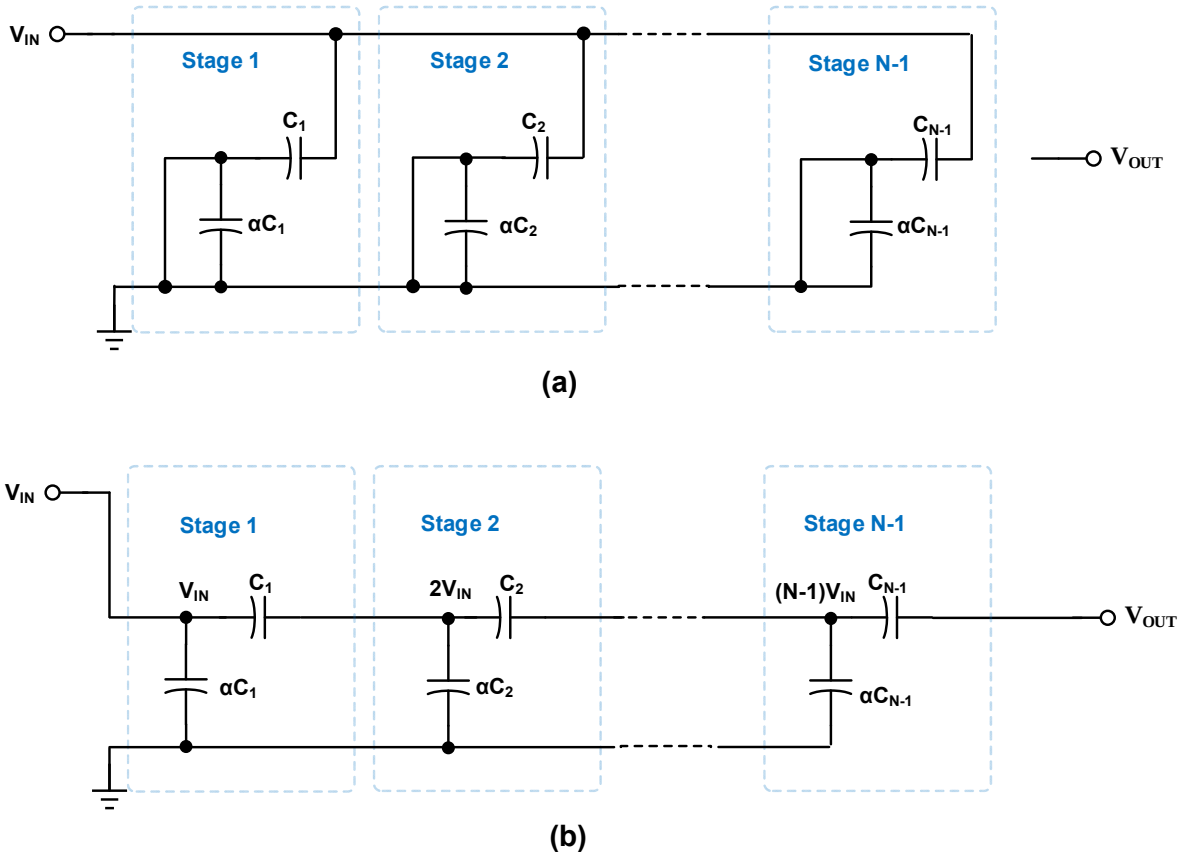

Figure 3.3.4. Bottom plate parasitic capacitors in a 1: N series-parallel fully integrated converter

The final loss is the equivalent series resistance (ESR) loss. This loss is due to the combination of the ESR of capacitors and metal wiring. For on-chip capacitors, their ESR depends on technology implementation and not obviously related to die area. The ESR loss is given by:

$$P_{ESR} = I_{OUT}^2 R_{ESR} \tag{3.16}$$

After investigating all loss components, the power conversion efficiency of switched capacitor converter is given by:

$$\eta = \frac{V_{OUT} I_{OUT}}{V_{OUT} I_{OUT} + P_{LOSS}} \tag{3.17}$$

where P_{LOSS} is the total power loss, for fully integrated converter, P_{LOSS} is given by:

$$P_{LOSS} = P_{ROUT} + P_{SW} + P_{CAP} + P_{ESR} \tag{3.18}$$

For those switched capacitor converters using off-chip flying capacitors, bottom plate loss P_{CAP} can be neglected, P_{LOSS} is given by:

$$P_{LOSS} = P_{ROUT} + P_{SW} + P_{ESR} \tag{3.19}$$

Finding the optimal point in the design space of f_{sw} and A_{tot} can be done by numerical optimization using contour plots [9]. Two design cases based on the available standard technologies are consider here, one is for fully on-chip implementation, the other one is to place flying capacitors off-chip. For a standard Bipolar-CMOS-DMOS technology, high density on-chip capacitors are typically not available. The capacitance density of commonly used Metal-Insulator-Metal capacitor ranges only from 2-5nF/mm^2. Thus the total on chip capacitor size is normally less than 10nF. Figure 3.5 shows the efficiency contours of a 1:5 series-parallel converter implemented by a total value of 4nF on-chip MIM capacitors assuming the MIM capacitor has a 5% parasitic bottom plate capacitance. The maximal power efficiency is limited to less than 72% by parasitic bottom plate capacitance of the on-chip capacitor.

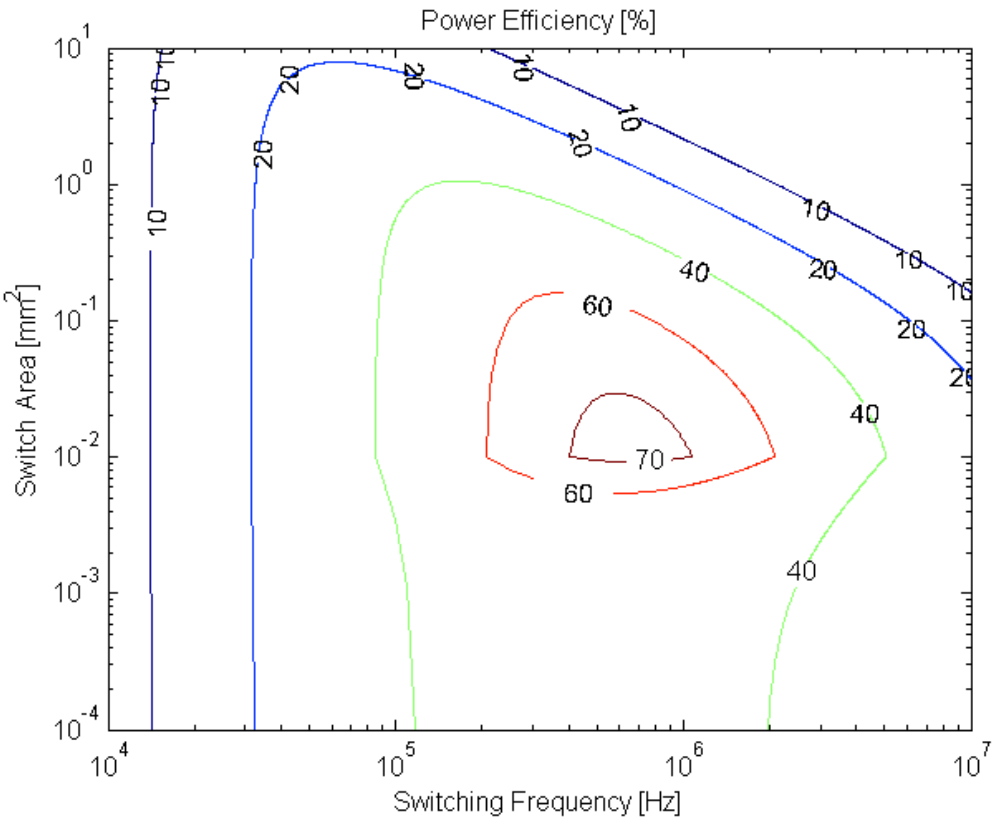

Figure 3.3.5. Efficiency curve of a 1:5 series parallel converter with on-chip MIM capacitors

In the second case, the flying capacitors are placed off-chip, thus the bottom plate capacitor loss is negligible. Figure 3.6 shows the efficiency contour of a 1:5 series-parallel converter with 400nF off-chip flying capacitors. In this case, the power conversion efficiency is much higher than fully on-chip implementation and can reach a peak conversion efficiency >98%.

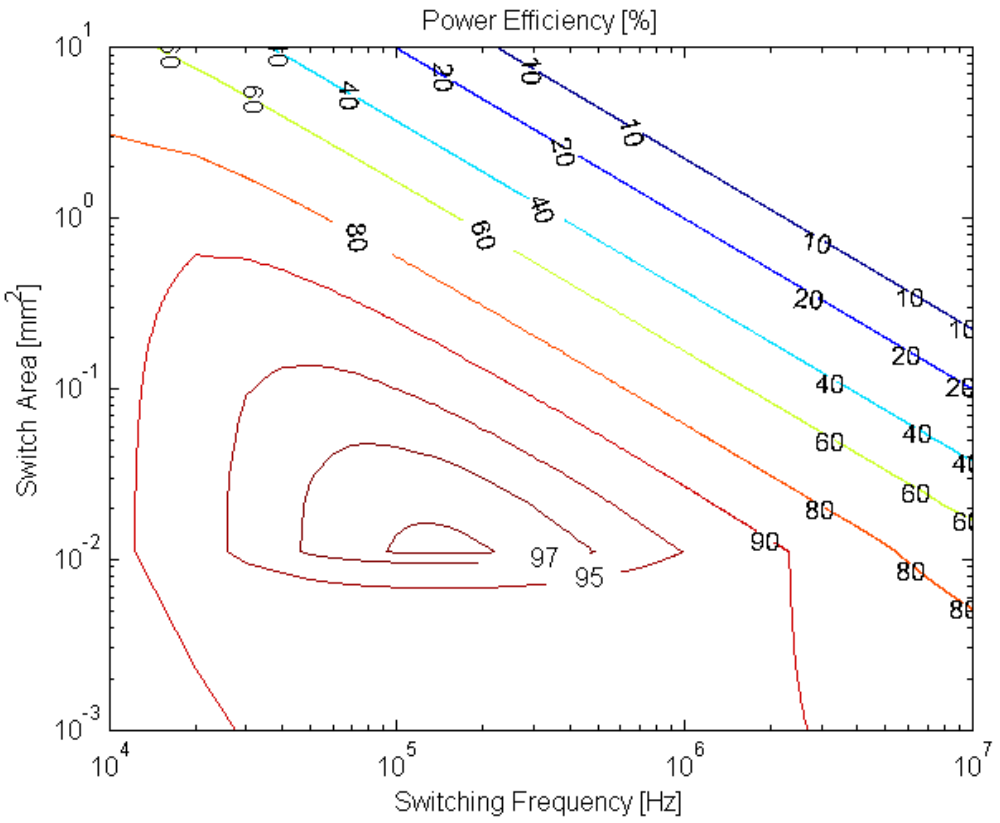

Figure 3.3.6. Efficiency curve of a 1:5 series parallel converter with off-chip capacitors

In order to achieve the highest power conversion efficiency, a series-parallel switched capacitor converter with off-chip flying capacitor should be used to build the liquid crystal lens driver.

3.3 Reconfigurable SC Converter with Multiple Conversion Ratio

As discussed in section 2.1, a switched capacitor converter can only achieve its maximal power conversion efficiency when its output voltage equals to the conversion ratio times the input voltage. This feature makes switched capacitor converter not suitable to maintain high power conversion efficiency over a wide output voltage range. In order to

improve power conversion efficiency over wide input and output voltage range, switched capacitor converter with multiple voltage conversion ratio are favorable [30] [31] [32]. A proposed 2×3×4×5× Reconfigurable Series-Parallel switched capacitor DCDC converter is shown in Figure 3.7.

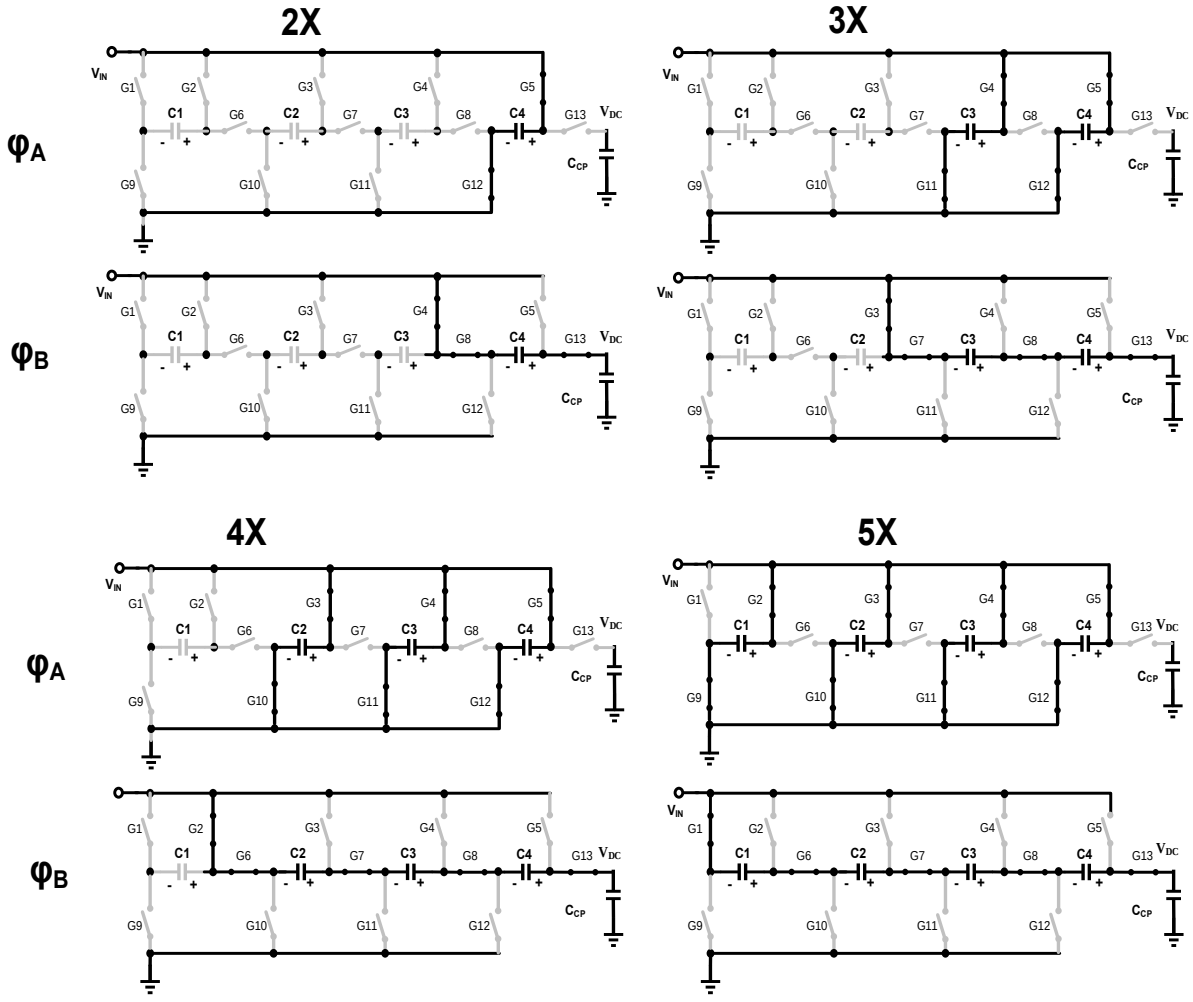

Figure 3.3.7. Operation of 2×3×4×5× reconfigurable Series-Parallel SC-DCDC

There are 4 flying capacitors and 13 transistors in the 2×3×4×5× Reconfigurable Series-Parallel SC-DCDC converter. It can realize five different conversion ratios (modes)

using topology transformation. φA and φB are two non-overlapping alternate clock phases. In φA, all flying caps are parallel connected and charged to VIN; while in φB, flying caps are series connected to input source and transfer charge to the output. The detail operation of the 4 conversion modes is explained below:

5X mode: During charging phase, G2-G5 and G9-G12 are ON while other transistors are OFF. C1, C2, C3, and C4 are in parallel with the input source, and each will be charged to the input voltage. The output is disconnected from the input. During discharging phase, G1, G6-G8, and G13 are ON while others are OFF. C1, C2, C3, and C4 are in series with the input source, and discharge energy to the output capacitor.

4X mode: During charging phase, G3-G5 and G10-G12 are ON while others are OFF. C2, C3, and C4 are in parallel with the input source, and each will be charged to the input voltage. The output is disconnected from the input. During discharging phase, G2, G6-G8, and G13 are ON while others are OFF. C2, C3, and C4 are in series with the input source, and discharge energy to the output capacitor.

3X mode: During charging phase, G4-G5 and G11-G12 are ON while others are OFF. C3 and C4 are in parallel with the input source, and each will be charged to the input voltage. The output is disconnected from the input. During discharging phase, G3, G7-G8, and G13 are ON while others are OFF. C3 and C4 are in series with the input source, and discharge energy to the output capacitor.

2X mode: During charging phase, G5 and G12 are ON while others are OFF. C4 is in parallel with the input voltage, and each will be charged to the input voltage. The output voltage is disconnected from the input. During discharging phase, G4, G8 and G13 are ON

while others are OFF. C4 is in series with the input source, and discharge energy to the output capacitor.

The voltage conversion modes can be auto-adjusted by different input voltage based on Table 3-4.

Target V_{OUT}	Conversion Ratio
$4V_{IN}<V_{OUT}<5V_{IN}$	1:5
$3V_{IN}<V_{OUT}<4V_{IN}$	1:4
$2V_{IN}<V_{OUT}<3V_{IN}$	1:3
$V_{IN}<V_{OUT}<2V_{IN}$	1:2

Table 3.4. Conversion ratio selection

Assume input voltage is 3V, the expected power conversion efficiency is shown in Figure 3.8.

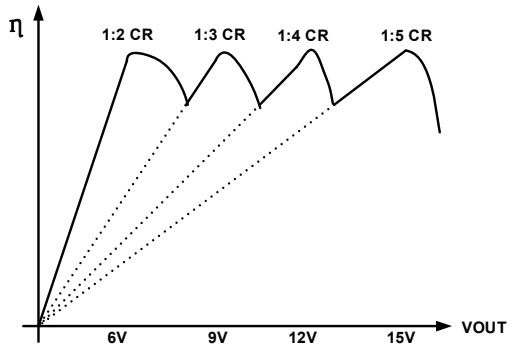

Figure 3.3.8. Power conversion efficiency vs. output voltage

3.4 Dual Loop Regulation of SC Converter

Liquid crystal driver application requires output regulation of the step-up switched capacitor converter to deliver a constant output voltage against variations in line voltage and

load current. Referring to the static model in Figure 2.2, the output voltage of a switched capacitor converter is determined by the output impedance R_{OUT}, and the conversion ratio N. The output impedance can be further broken down to SSL output impedance and FSL output impedance. Thus, by modifying one or more of the three parameters: R_{SSL}, R_{FSL} and N, the converter output voltage can be regulated.

Numerous closed loop control methodologies were proposed in the literature, such as cascade control [33], switch resistance modification control [32], pulse width modulation control (PWM) [34][35], frequency modulation control (FM) [36], hysteresis control [10][37][38], constant on-time control [39][40] and adaptive on-time control [41]. Cascade control, switch resistance control, PWM control and FM control are implemented by amplifier based feed-back controllers. Cascade control uses a low dropout regulator (LDO) followed by the SC converter to regulate its output voltage. By modifying the on-resistance of LDO pass device, the R_{FSL} is modified based on the feedback controller. Output voltage ripple in a cascade controlled SC converter is very small due to a superior PSRR provided by the LDO circuitry. The major disadvantage of this approach is that one more power transistor and a filtering capacitor are required, making this approach area inefficient. The switch resistance modification control is similar to the cascade control, but it doesn't have the additional LDO circuitry. Instead, this approach directly modifying the on resistance of the SC converter power switch by the feedback controller. Pulse width modulation control is very popular in inductor based converter. The major limitation of using PWM control in a SC converter is it requires the converter operating in a condition closed to FSL. Thus the switching frequency needs to be relative high and the converter isn't very power efficient in a

low power application. Frequency modification control has a high efficiency at light load conditions. However, its controller is amplifier based. Thus the controller power consumption is limited by the closed-loop bandwidth. On the other hand, hysteresis control, constant on-time control and adaptive on-time control are using comparator based controller. Thus they are inherently stable. They are also very efficient in a light load condition. The major drawback for hysteresis and constant on time control is the output ripple is relatively large. The adaptive on-time control can maintain low output ripple under different input voltages at a cost of an additional circuitry. A summary of SC converter control methodologies is listed in Table 3.5.

Control Methodology	Cascade	R_{SW} Modification	PWM	FM	Hysteresis	Constant On-time	Adaptive On-time
Major Parameter Modified	R_{FSL}	R_{FSL}	R_{SSL}	R_{SSL}	R_{SSL}	R_{SSL}	R_{SSL}
Controller	AMP-Based	AMP-Based	AMP-Based	AMP-Based	CMP-based	CMP-based	CMP-based
Output Ripple	Excellent	Good	Good	Good	Fair	Fair	Good
Line Regulation	Excellent	Good	Good	Good	Excellent	Excellent	Excellent
Load Regulation	Excellent	Good	Good	Good	Excellent	Excellent	Excellent
Light Load Eff	Fair	Fair	Poor	Good	Excellent	Excellent	Excellent
Controller Iq	Poor	Poor	Fair	Fair	Excellent	good	good
Simplicity of Compensation	Fair	Poor	Fair	Fair	Excellent	Excellent	Excellent
Constant Frequency	Excellent	Good	Excellent	Poor	Poor	Poor	Poor
Auto-tuning	Poor	Poor	Poor	Fair	Excellent	Excellent	Excellent

Table 3.5. Control methodologies summary

Regulating a SC converter output voltage by varying its output resistance requires a voltage drop across the resistive elements. This is similar to the case of a linear regulator and the maximal power efficiency is limited. As discussed in section 3.3, a SC converter with reconfigurable conversion ratios can vary the parameter N thus can achieve a high power efficiency over a wide output range. Thus a hybrid control scheme is a good candidate for the liquid crystal lens driving application. The hybrid control scheme has two control loops. In the outer control loop, an adaptive controller is used to select the optimal conversion ratio according to a reference signal. In the inner loop, a hysteresis controller is selected due to its simple architecture and excellent light load efficiency. Figure 3.9 shows the dual loop control scheme of the proposed reconfigurable switched capacitor converter.

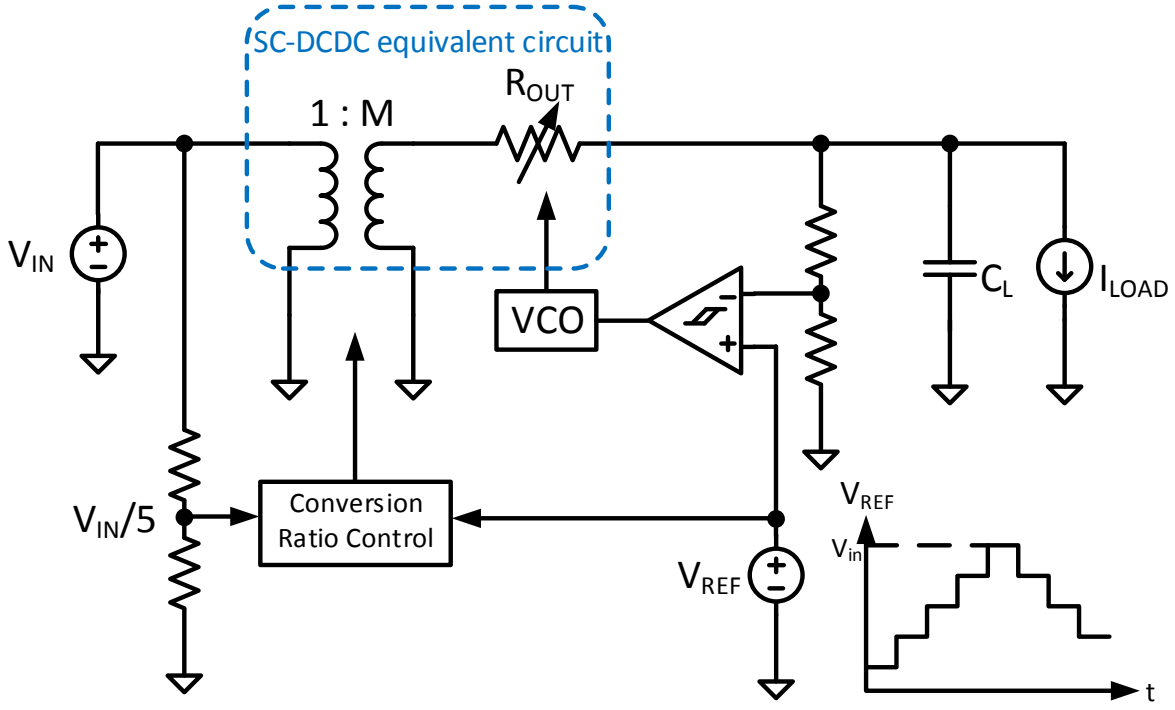

Figure 3.3.9. Dual loop control scheme of the proposed reconfigurable SC converter

3.5 Improved H-bridge Gate Driver to Reduce Output Ripple

Liquid crystal lens needs to be driven by an AC signal with a minimal DC component. Thus an inverter stage is required to convert the DC signal from the switched capacitor converter output to an AC signal. H-bridge inverter is a widely used circuitry that provides the DC to AC voltage conversion. Figure 3.10 shows a conventional integrated H-bridge inverter. It consists of four switches. Two high side switches can be implemented with P-type LDMOS devices (PA and PB) to ease the gate drive requirement. And two low side switches can be implemented with N-type LDMOS devices (NA and NB). The simplified equivalent circuit of the liquid crystal lens is just a capacitor. Thus the load of the H-bridge inverter is purely capacitive. A capacitor is used as the liquid crystal lens model in the following analysis.

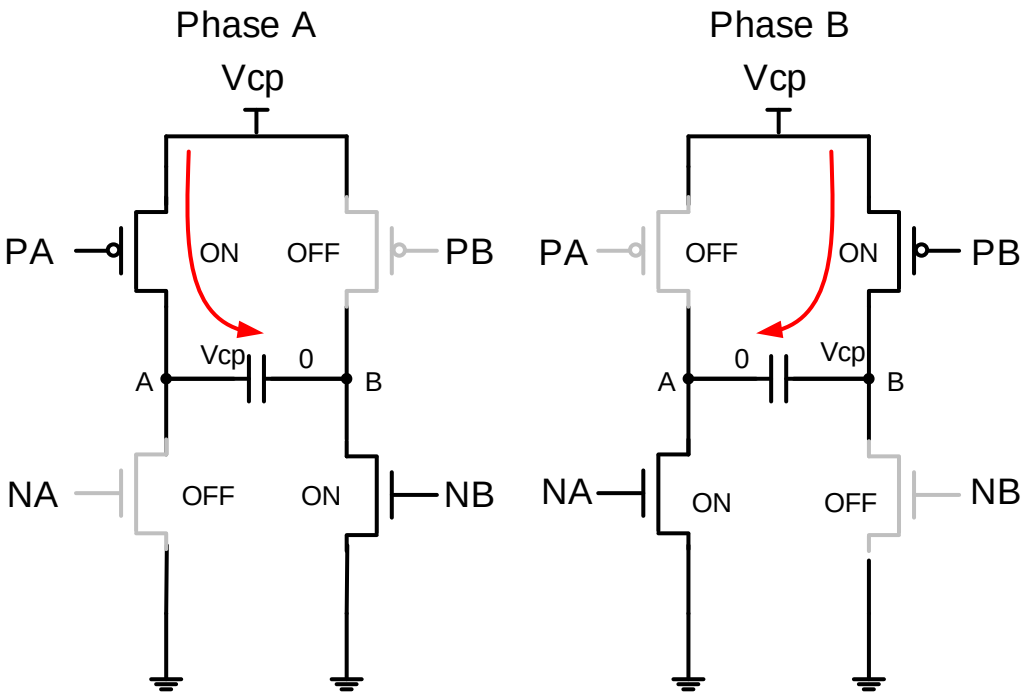

Figure 3.3.10. Conventional two phases H-bridge drive

During the phase A, switches PA and NB are on, and switches PB and NA are off. The switched capacitor converter charges the left hand side plate of the load capacitor to a potential of V_{CP}; while during the phase B, switches PB and NA are on, and switches PA and NB are off, the right hand side plate of the capacitor is charge to V_{CP}. However, during the transient state from phase A to phase B, while PB is turning on and NA haven't fully discharge left hand side plate of the capacitor to a ground potential, a partial of charge stored in the inverter load capacitor can be pumped back to the switched capacitor converter output capacitor via the body diode of PA, and a voltage overshoot can be observed.

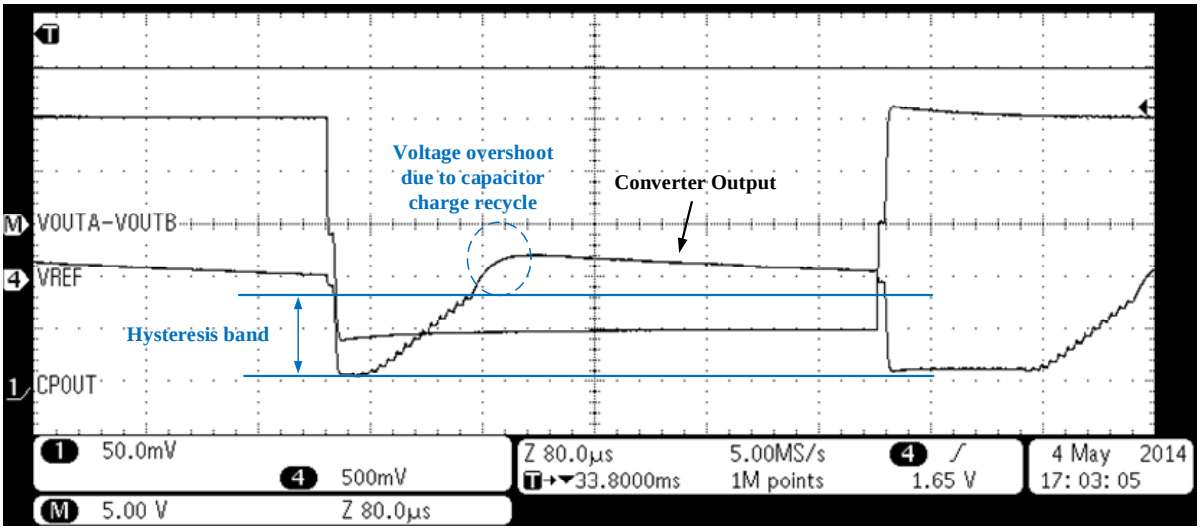

Figure 3.3.11. Output voltage overshoot

A reduced ripple H-bridge driving scheme is proposed and shown in Figure 3.12. Two intermediate phases are inserted into the conventional two phases driving scheme. During the transaction between A node goes low and B node goes high, two low side switches are turn on before P2 turn on. Thus at this moment the charge stored in the inverter

load capacitor is completely discharged to ground instead of partially pumped back to the SC converter output capacitor, and the voltage overshoot can be avoid. A similar operation is found during the transaction between A node goes high and B node goes low.

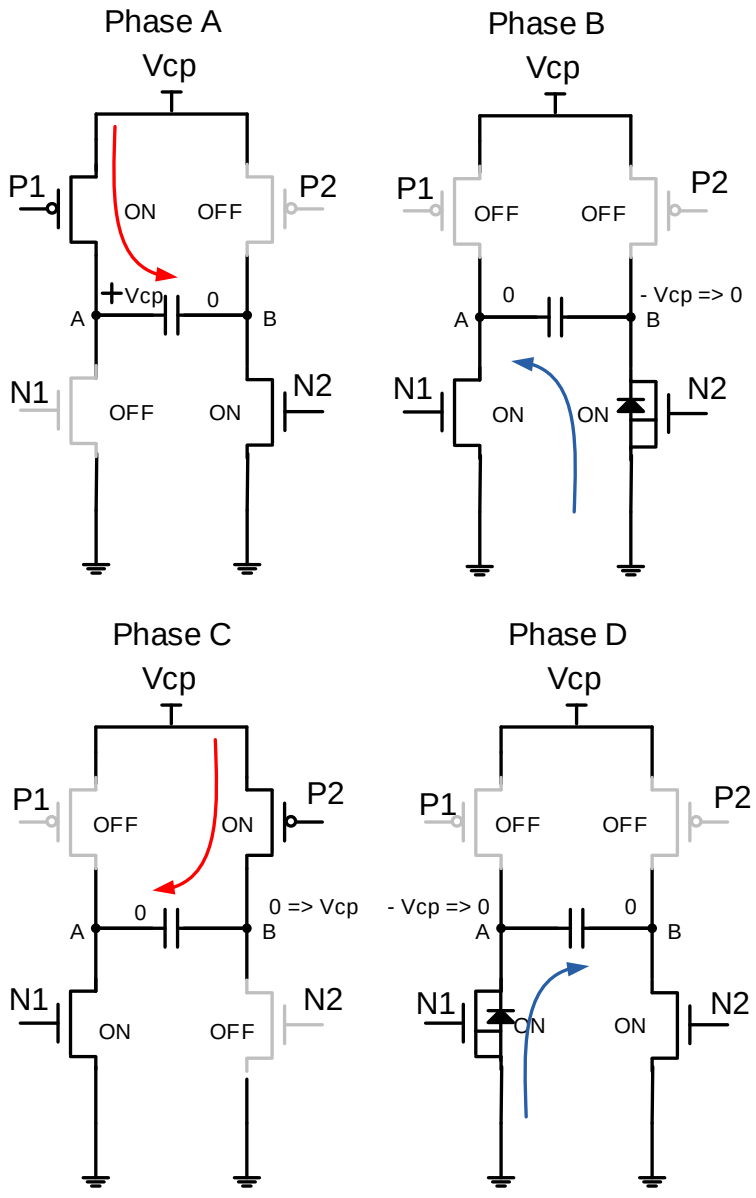

Figure 3.3.12. Ripple reduction H-bridge gate drive

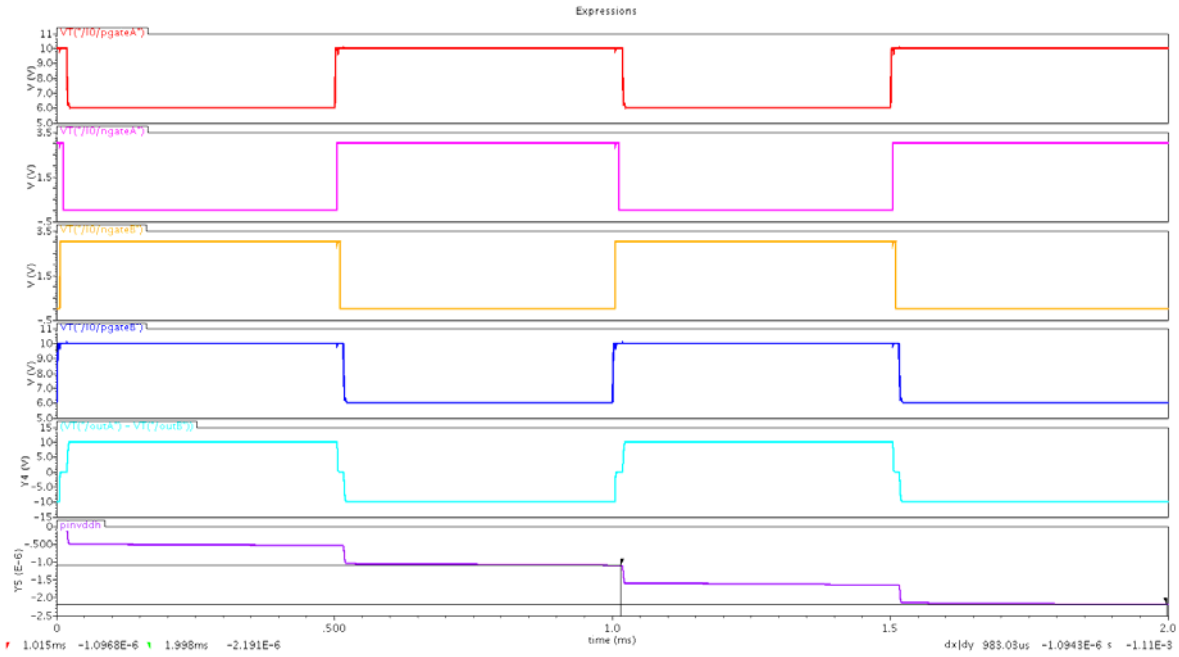

Figure 3.3.13. H-bridge gate drive waveform

Figure 3.13 shows the gate drive signals of those four switches to ensure the four phase operation of the reduced ripple H-bridge inverter.

3.6 Proposed Liquid Crystal Lens Driver Architecture

The proposed liquid crystal lens driver is shown in Figure 3.14. It consists of three parts: a reconfigurable 2×3×4×5× Series-Parallel switched capacitor converter, a H-bridge inverter and a low power control circuitry. As discussed in section 3.3-3.5, the switched capacitor converter can provide an output voltage up to five time of the input voltage and maintain high efficient over a wide output range. The reduced ripple H-bridge inverter converts the DC output voltage from the SC converter to a square wave AC voltage to drive the liquid crystal lens. The control circuitry provides a dual loop control for the switched capacitor converter and a gate drive control for the H-bridge inverter.

Section 3.1 shows the off-chip capacitor implementation has the lowest converter output impedance when the total area is constraint. Thus all capacitors in SC converter power stage are placed off-chip to achieve the highest power conversion efficiency. All power switches and the controller circuitry are integrated on-chip. In order to reduce power consumption, the controller circuitries are in a low voltage domain. Two sets of level shifters are used to provide gate drive voltages for those high voltage power devices used in the SC converter and the H-bridge inverter. The detail circuit implementation is discussed in next chapter.

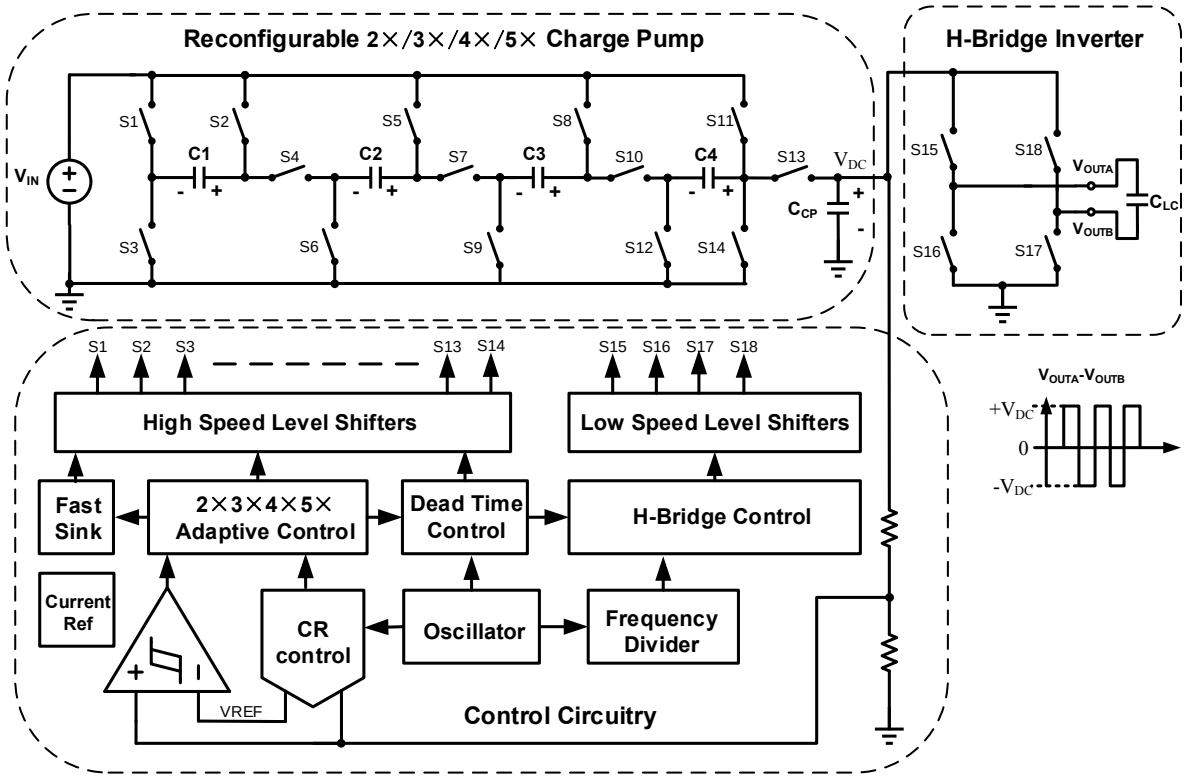

Figure 3.3.14.Proposed liquid crystal lens driver architecture

CHAPTER 4

4 Circuit Implementation of the Liquid Crystal Lens Driver

4.1 Switched Capacitor Converter Power Stage

The power stage of a reconfigurable 2×3×4×5× Series-Parallel switched capacitor converter is shown in Figure 4.1. In order to simplify the high side gate driver design, high side power switches are implemented with PMOS or HV-PMOS devices and low side power switches are implemented with NMOS or N-type LDMOS devices. Buck terminals of high side switches S2, S3, S4, S5 and S13 need to be connected to a dynamic N-Well, since they need to be connected to the higher potential nodes. All series connected pumping switches except the one connected to the output can be implement by using low voltage PMOS devices, since their blocking voltages equal to the input voltage. Sizing of those power devices are based on the guideline given in chapter 2 and chapter 3.

The gate drive signals for SC converter operating in the 5× mode are shown in Figure 4.2. While the SC converter operating in other modes, gate drive signals are similar and can be easily found. A Sufficient dead-time delay should be provided between the high side gate drive signals and the low side gate drive signals. Those dead-time delays are mostly determined by level shifter and gate drive circuit delays. An adaptive dead-time control [42] can reduce the power device body diode conduction loss at a cost of extra circuitry. But in a

liquid crystal lens driver application, the output current is very low thus the body diode conduction loss is not significant. Thus a fixed dead-time circuitry is used to simplify the controller design and reduce control circuitry power consumption.

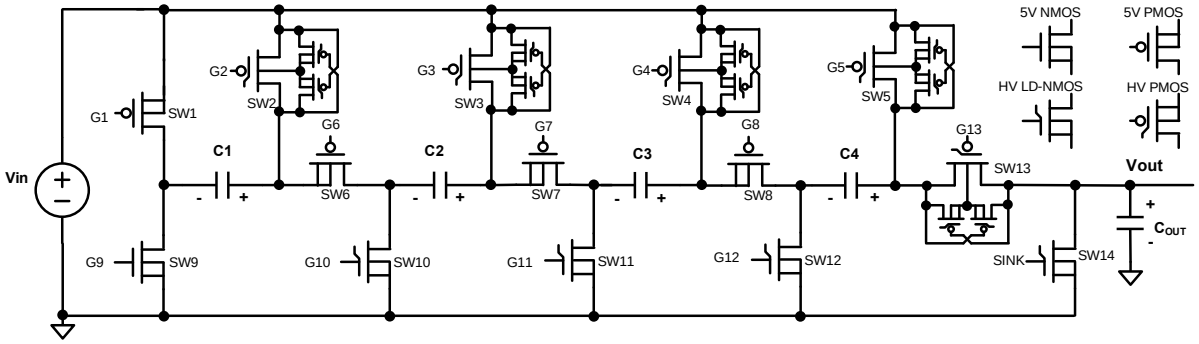

Figure 4.1. Schematic of reconfigurable 2x3x4x5x SP-SC converter power stage

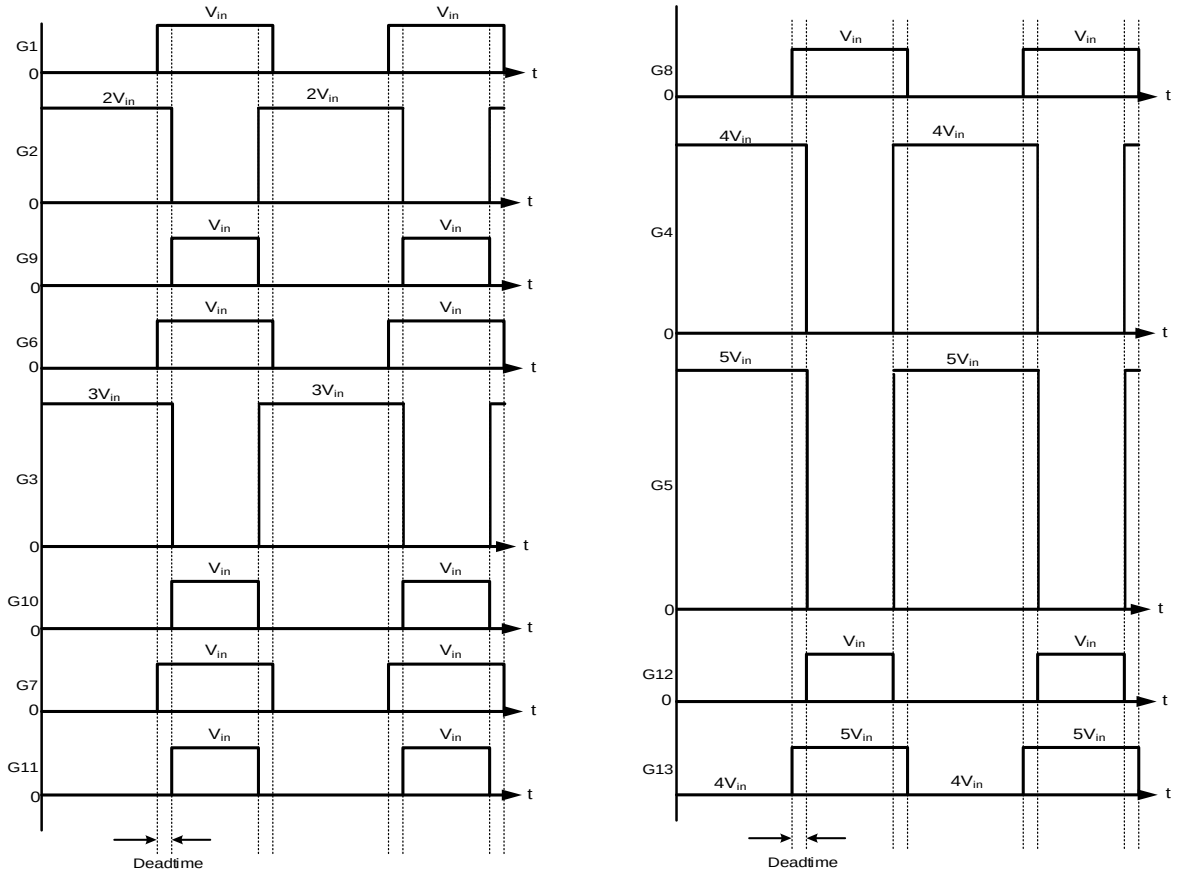

Figure 4.2. Gate drive signal of power switches in 5× mode

4.2 Level Shifter and High Side Gate Driver

As discussed in section 2.3.2, the voltage rating of the gate-to-source voltage of a HV-PMOS device is identical to that of a low voltage device since their gate oxide thickness are same. Thus a level shifter circuit with limited output swing is crucial to safely driving the high size HV-PMOS devices.

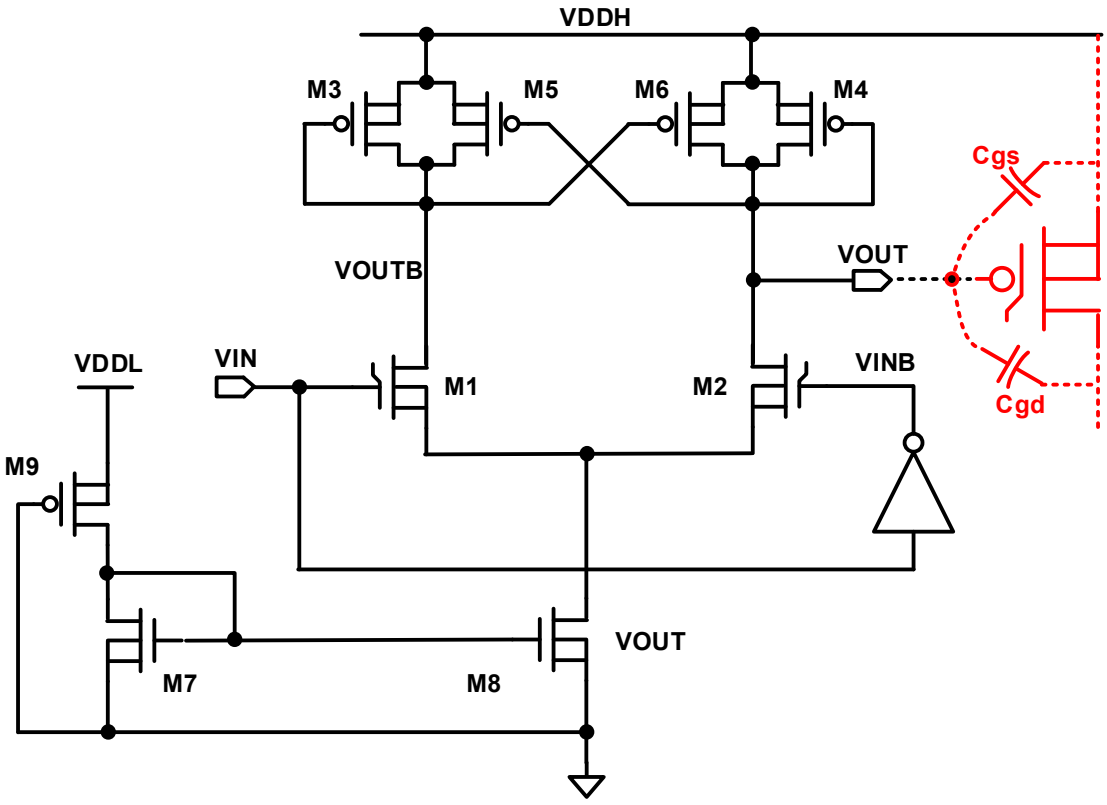

Figure 4.3.Conventional process independent level shifter

A level shifter circuit with process independent output swing limit is shown in Figure 4.3[43]. In this circuitry, transistors M3 and M4 are diode connected and transistors M5 and M6 form a cross-couple pull up cell. The lowest output voltage of the level shifter is fixed by the positive supply minuses the voltage drops across M3 or M4:

$$V_{OUT} = V_{DDH} - \left(\sqrt{\frac{2I}{\beta_p}} + |V_{tp}| \right) \tag{4.1}$$

where the drain current I is generated by a PMOS transistor M9 connected to VDD which is perfectly matched to the PMOS loads M3 and M4 of the level shifter. In this case, current I generated by M9 is given by:

$$I = \frac{\beta_p}{2} \left(V_{DDL} - |V_{tp}| \right)^2 \tag{4.2}$$

Substitute (4.2) into (4.1), the output voltage of the level shifter reduced to:

$$V_{OUT} = V_{DDH} - V_{DDL} \tag{4.3}$$

Rewrite (4.3) we can get the output voltage swing:

$$V_{swing} = V_{DDH} - V_{OUT} = V_{DDL} \tag{4.4}$$

(4.4) shows the output voltage swing of the level shifter equals to V_{DDL} and independent of electrical parameters variations. The residual relative deviation of the voltage swing can result from the mismatch of the current flow through M9 and M4. In fact, if the drain voltage values of M9 and M4 devices are not perfectly matched, the output impedances will lead to a slight current difference. Moreover, the physical mismatch of current mirror M7 and M8 increases such differences. The resulting relative deviation, however, is negligible with respect to the full voltage swing of V_{OUT}.

The major drawback of this level shifter circuit is it can be very power hungry if its operating frequency is high. Since the output of level shifter is used to drive high-side HV-PMOS switches, which input capacitance are high, large charge / discharge currents are

required to achieve a high switching speed. Those charge / discharging currents directly related to the static current of the level shifter circuit and make it become very power hungry when operating in a high frequency condition.

An improved level shifter circuit which can dramatically reduce the static power consumption is shown in Figure 4.4. Transistors M1, M2 and M13 form a static current source similar to the one used in a conventional level shifter but consumes much less power. Transistors M11, M12 and M14 form a burst current generator to provide a burst current to speed up charging or discharging parasitic capacitors C_{par1} and C_{par2}. V_{IN1} and V_{IN2} are two inputs of the burst current generator and they are provided by a clock edge pulse generator. And transistors M16 and M17 form a high voltage class B buffer to provide a dynamic current to charge and discharge the output capacitor (power switch device input capacitor). A small current source is used in the HV class-B buffer stage to keep M17 working in a weak inversion mode. Transistor M7, M8, M9, M10 form a split crossed couple pair to provide voltage levels compatibility for M17. Level shifter output voltage is given by:

$$V_{OUT} = V_{DDH} - \left[\sqrt{\frac{2I}{K_p}\left(\frac{1}{\sqrt{\left(W/L\right)_4}} + \frac{1}{\sqrt{\left(W/L\right)_8}}\right)} + \left|V_{tp4}\right| + \left|V_{tp8}\right| - \left|V_{tp17}\right|\right] \quad (4.5)$$

Assume $(W/L)_{12}$ is two times of $(W/L)_{13}$, in this case, current I flow through M4 and M8 is given by:

$$I = \frac{K_p}{4}\left(\frac{W}{L}\right)_{15}\left(V_{DD} - \left|V_{tp15}\right|\right)^2 \quad (4.6)$$

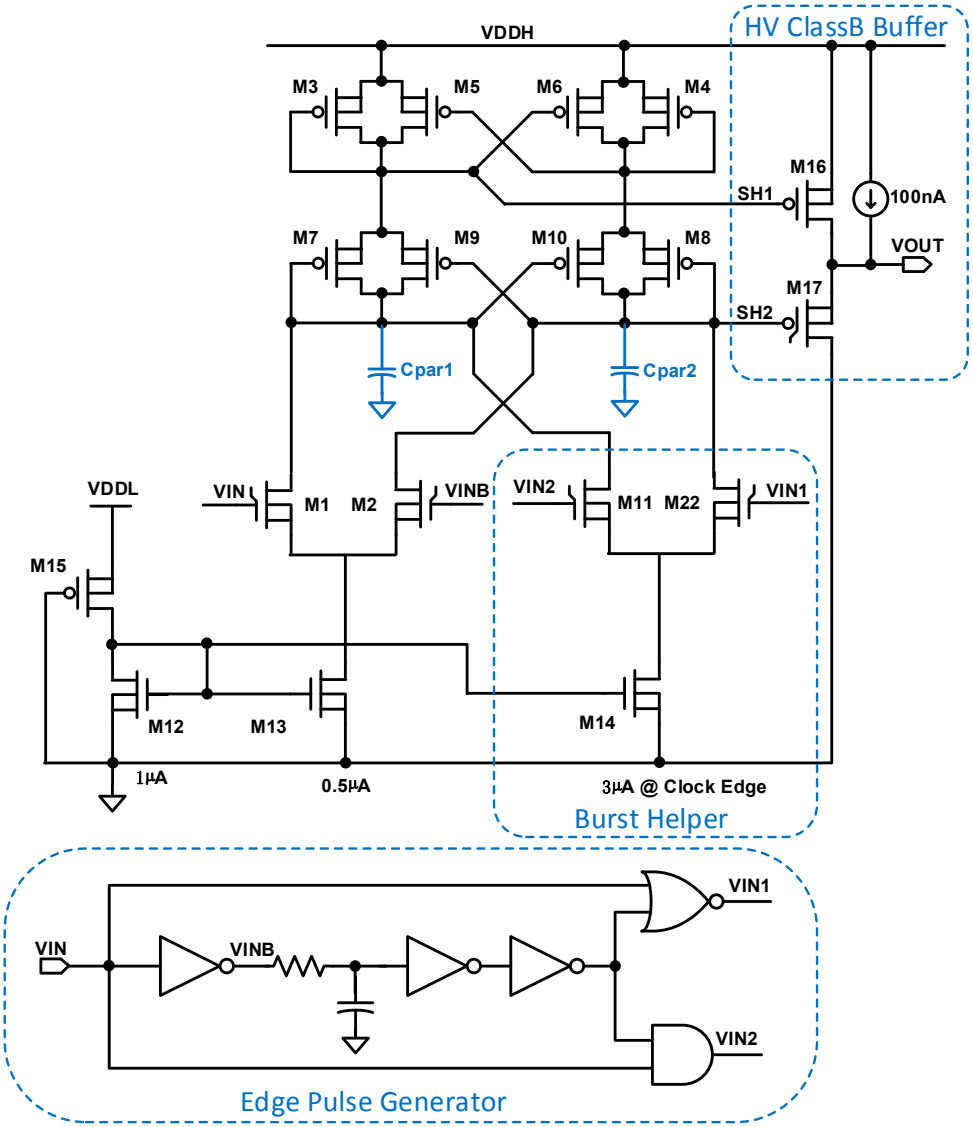

Figure 4.4. Proposed level shifter circuit

Sizing $(W/L)_4 = (W/L)_8 = (W/L)_{15}$, and substitute (4.6) into (4.5), the output voltage of the level shifter can be calculated by:

$$V_{OUT} = V_{DDH} - V_{DDL} + |V_{tp17}| - |V_{tp8}| \tag{4.7}$$

Rewrite (4.7) the voltage output swing equals to:

$$V_{swing} = V_{DDL} + |V_{tp8}| - |V_{tp17}| \tag{4.8}$$

(4.8) shows the threshold voltage mismatch between the low voltage PMOS device M8 and the HV-PMOS device M17 will introduce a deviation of output swing and differ slightly from V_{DDL}. Moreover, the difference between the drain voltage operating condition of M15, M4, M8 as well as the physical mismatch of current mirror M12~M14 result in a negligible relative deviation of the full voltage swing of V_{OUT}.

Figure 4.6 shows simulation results of the improved level shifter circuit are. Since the level shifter static current stays in a very low level during most of the switching period and only goes high in a short period of time near the clock switching edge, the total power consumption of the level shifter is significantly reduced. Simulation result shows driving the same HV-PMOS power switch with a size of W=640µm, L=3.5µm and a 200ns propagation delay time, the proposed low power level shifter only consumes 1.75µA static current. While the conventional level shifter consumes 48.2µA static current. That's a 96.4% reduction of the static power consumption.

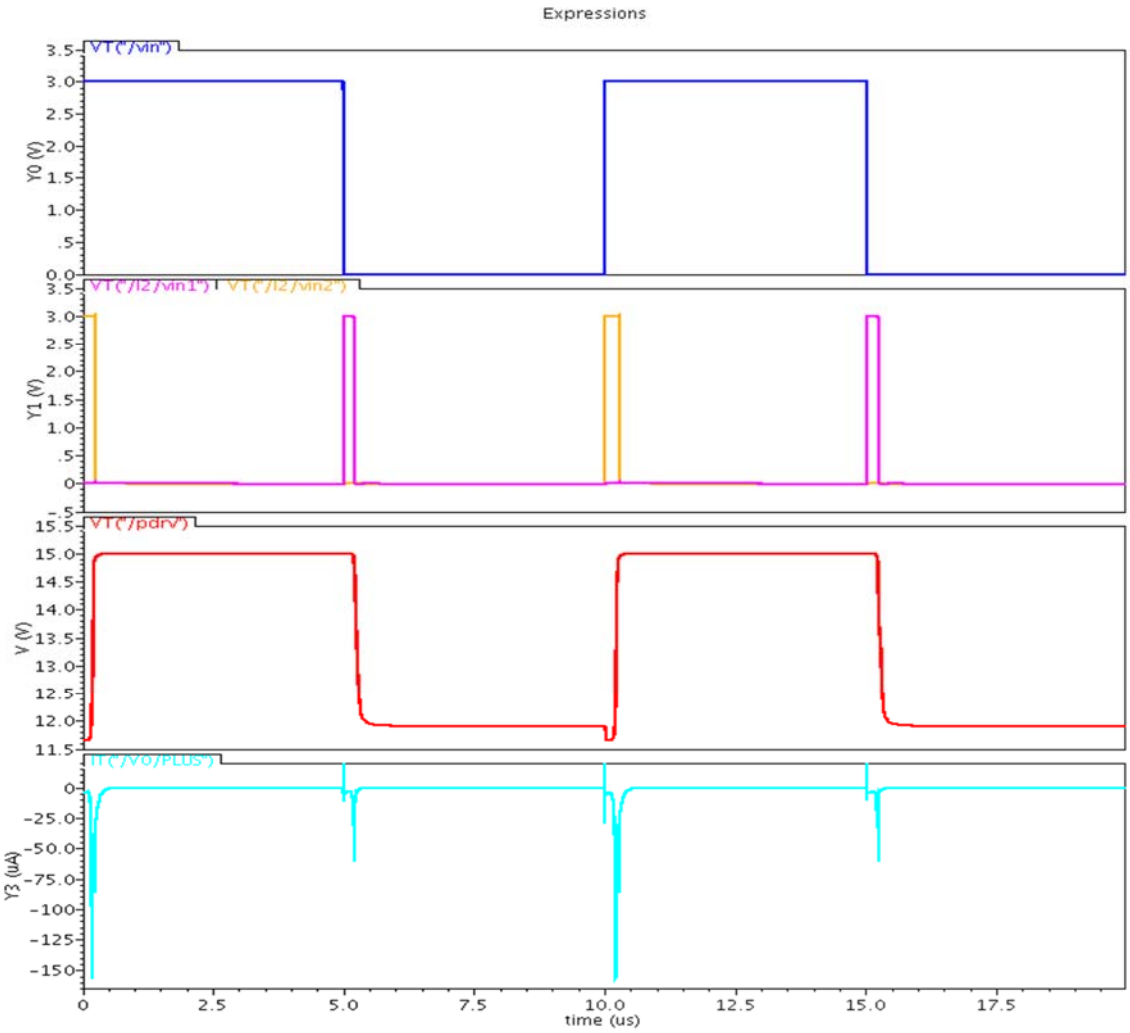

Figure 4.5. Simulation result of improved level shifter

4.3 Fast Sink Function

When the load current of a switched capacitor converter is very small, it will take a very long time to discharge the SC converter output capacitor to reduce the converter output voltage. However, in some low power applications, such as in a liquid crystal lens driver system, the regulated SC converter output voltage needs to response rapidly to follow the

reference signal. Thus if the reference voltage is reduced, a current sink mechanism needs to be provided to speed-up discharging the converter output capacitor.

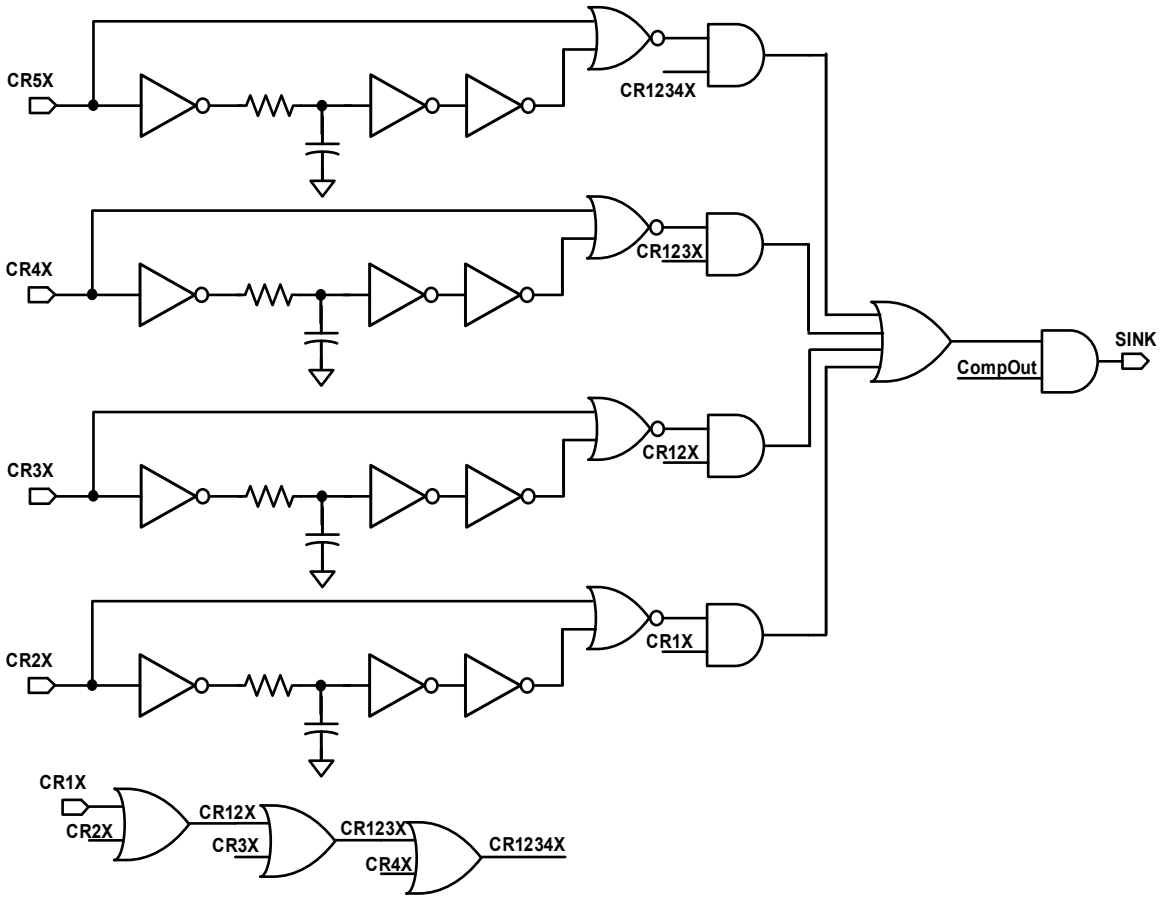

Figure 4.6. Fast sink logic

Figure 4.6 shows a fast sink logic circuitry. When the reference signal falls, the fast-sink logic detects the reference signal falling edges and generates a voltage pulse to turn on the sink transistor SW14 shown in Figure 4.1. The pulse width of the fast sink voltage signal is defined by:

$$t = 6C_{OUT}R_{ON} = \frac{6C_{OUT}}{\mu_N C_{OX}\frac{W}{L}(V_{GS} - V_{th})} \tag{4.9}$$

where C_{OUT} is the output capacitor of SC converter and R_{ON} is the on resistance of the sink transistor.

A simulation result of the fast-sink circuit is shown in Figure 4.7. With the fast-sink function enabled, the falling time is 48us, which is 219 times faster than that without fast-sink enabled.

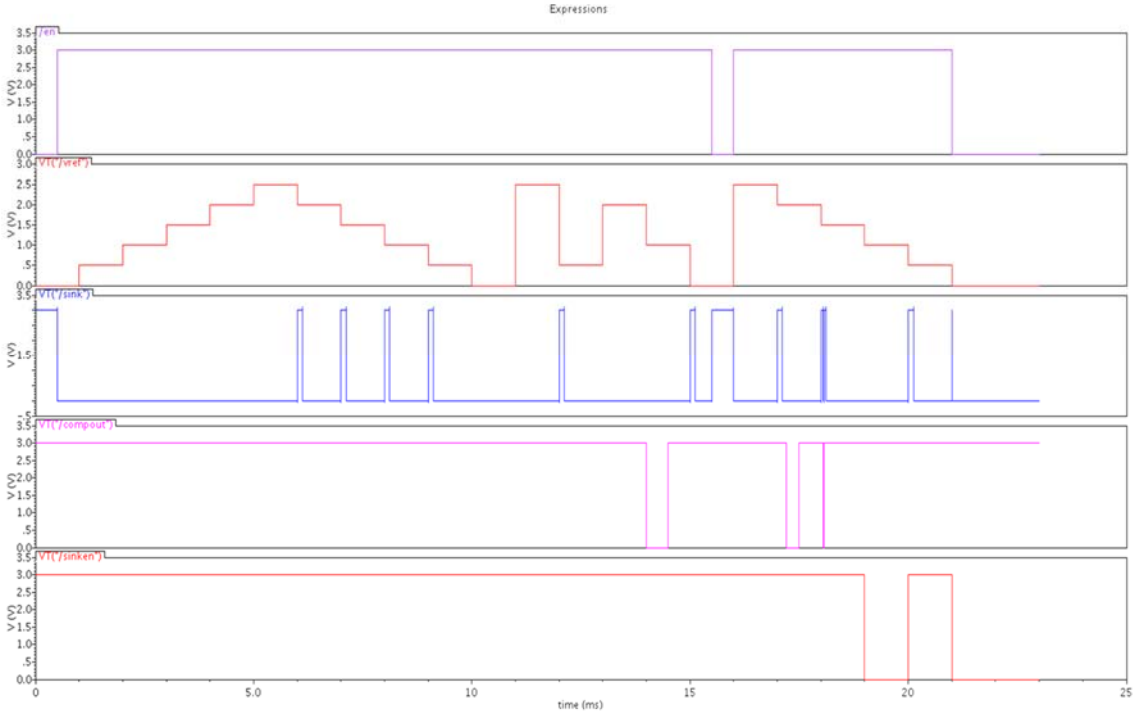

Figure 4.7. Fast-sink simulation results

4.4 Proposed Low Power Comparator

As discussed in section 3.4, the core building block in a hysteresis controller is a comparator. The major parameters of a comparator are propagation delay, input voltage offset, hysteresis voltage and current consumption. Several techniques are used in the proposed rail-to-rail voltage comparator shown in Figure 4.8 to reduce the propagation delay and maintain a low input voltage offset without increasing current consumption. At first, a

multi-stage topology should be used in designing a low power comparator. Since the comparator propagation delay is inverse proportional to the comparator bandwidth, a multi-stage comparator will have a larger bandwidth compares to single-stage comparators with the same power consumption, thus has a shorter propagation delay. In Figure 4.8, the first two comparator stages should have a low gain and consumes less current, and the last stage of the comparator should have a higher biased current to enhance the slew rate limit. Second, a cascade stage are used and series connected to the comparator input pair. Since the sizes of comparator input transistors are need to be relative large to reduce the random input voltage offset, the gate capacitance of those input transistors are also relatively large. Cascade stages N3/N4 and P3/P4 can help to reduce the miller effect of the input capacitance thus increase the input stage bandwidth. From the ESD protection point of view, the gate connections of cascade stage devices should not directly connected to power supply or ground, but should be connected to VDD/GND via tie high or tie low cells. Finally, voltage clamps form by N16, N17 and N19 are used to reduce the voltage swing of intermediate stages output nodes and reduce the propagation delay.

Hysteresis circuit plays an important role in a comparator circuitry to prevent output instability. However, in an ultra-low power comparator, its hysteresis circuit can fail to operate normally. The reason for the failure is caused by the hysteresis signal transfer via the feedback loop is too slow thus the output signal sent out of the comparator before the hysteresis circuit can react. Thus a comparator with two hysteresis stages is favorable in an ultra-low power design. As shown in Figure 4.9, the second stage of hysteresis contains a

Schmitt trigger and an inverter. The Schmitt trigger is placed in the signal output path and the inverter is placed in the hysteresis signal path. And the rising threshold of the Schmitt trigger

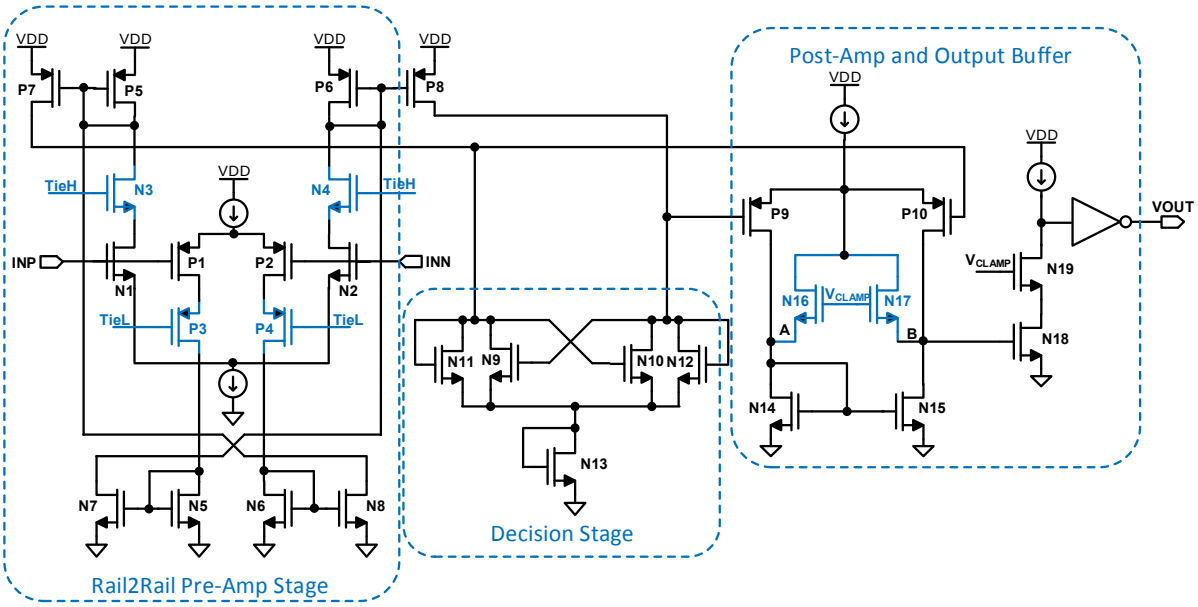

Figure 4.8. Schematic of a low power comparator

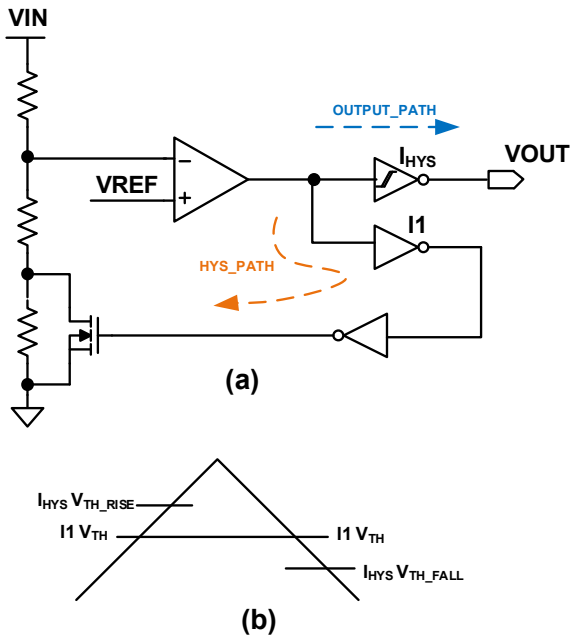

Figure 4.9.Two stages hysteresis (a) schematic (b) input thresholds

is higher than the inverter input threshold, while the falling threshold of Schmitt trigger is lower than the inverter input threshold. Thus the inverter is always toggled before toggling the Schmitt trigger and the feedback signal is always ahead of the output signal. With the two hysteresis scheme, the comparator is ensured free of output jitter.

4.5 Conversion Ratio Controller

The conversion ratio controller is used to adaptively generate the optimized conversion ration according to different reference voltages. The optimized conversion ratio versus input voltage was given in Table 3.4.

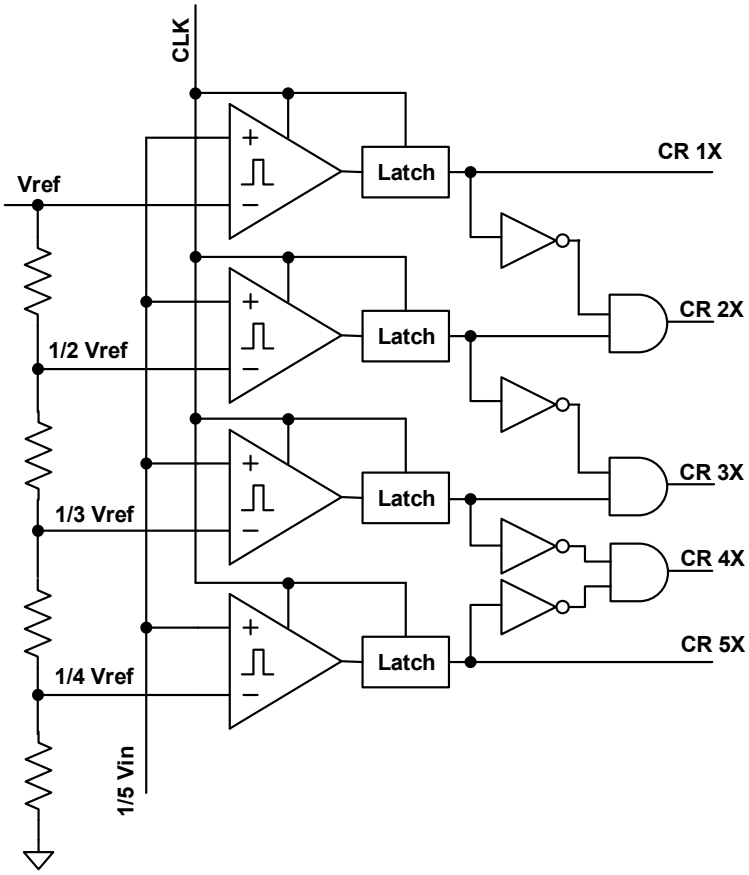

Figure 4.10.Schematic of conversion ratio controller

Figure 4.10 shows the schematic of the proposed conversion ratio controller. Similar with a flash ADC circuitry, the conversion ratio controller uses four comparators to differentiate the reference voltage and generates the mode selection signal. In order to reduce current consumption, those comparators can be implemented by dynamic-comparators, which will be discussed in next section.

4.6 Dynamic Comparator

Due to its low power consumption and high speed, dynamic comparator is widely used in high speed ADC applications [44] [45] [46]. A low noise and low voltage dynamic comparator circuit is shown in Figure 4.11. The dynamic comparator is based on a latch circuitry to provide a positive feedback for signal regeneration. This dynamic comparator uses a double tail topology to reduce the minimal operating voltage requirement. All critical nodes in the comparator are well defined in the pre-charge phase thus and voltage mismatch is reduced. Due to its symmetric topology, the comparator offset voltage is highly depend on layout matching. And a large size of input pair M1/M2 is favorable to minimize random input offset. However, the large input transistor pair also introduces a large parasitic gate capacitance and will incurs large common mode kick-back noise during the switching time in the evaluation phase. This problem can be very severe if the current flow through the resistor divider network is low, which is normal in a low power design. Thus a circuit used to reduce the common mode kickback noise is required. Transistors M4-M8 form a voltage clamp to reduce the voltage swing of the source of input pair, thus they can greatly reduce the common mode kick-back noise.

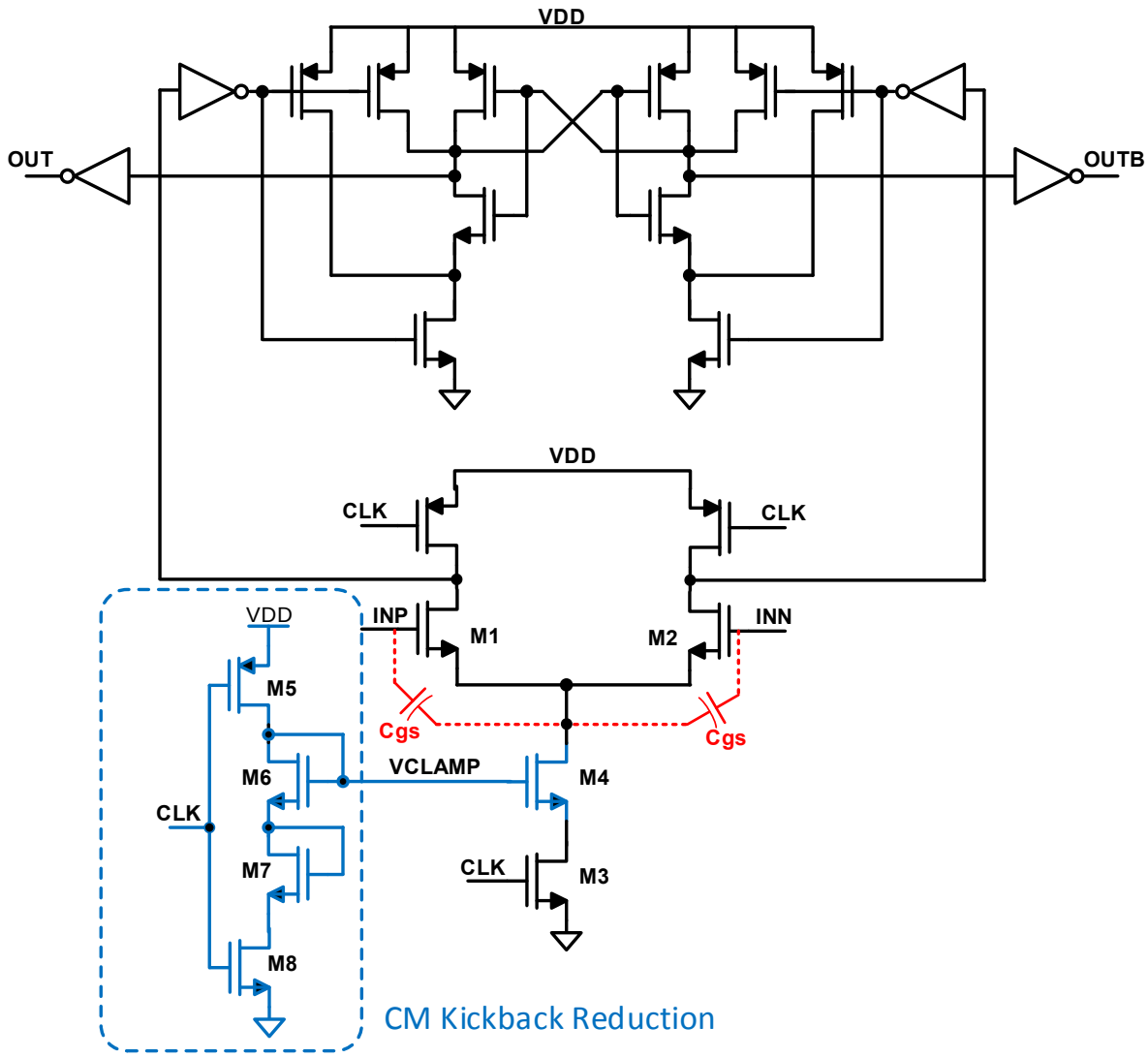

Figure 4.11. Proposed dynamic comparator

4.7 Active Voltage Clamp

In a power converter with multiple voltage domains, such as in a series-parallel topology converter with multiple stages, voltage clamp plays an important roles in protecting low voltage devices during the period of system shut-down. The power-train capacitor voltages may drift unanticipatedly when the converter is stop switching and may incur over-

voltage levels in some voltage domains. Thus a voltage clamp should be placed in each series-parallel stage to avoid over-stressing any devices.

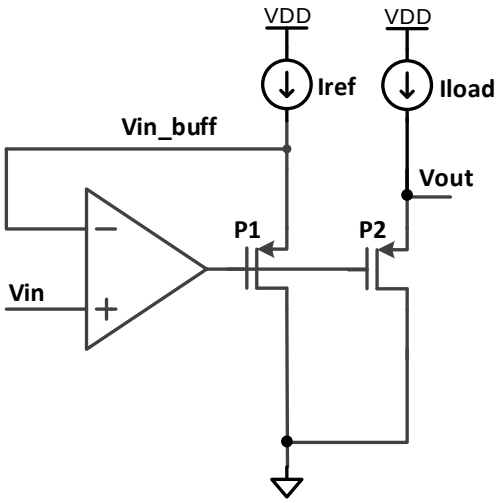

Figure 4.12.Conventional active voltage clamp

An active voltage clamp circuit can be used to precisely clamp the output voltage to a desired reference value. Figure 4.12 shows a conventional active voltage clamp circuitry. The offset voltage V_{OS} between the output node and reference node of this voltage clamp can be calculated by:

$$V_{OS} = V_{OS\_AMP} + \left(\sqrt{\frac{2I_{LOAD}}{K_p(W/L)_2}} - \sqrt{\frac{2I_{REF}}{K_p(W/L)_1}} \right) + \Delta V_{tp} \tag{4.10}$$

where V_{OS_AMP} is the input offset voltage of the voltage amplifier, ΔV_{tp} is the threshold mismatch between P1 and P2, I_{REF} is a reference current, and I_{LOAD} is the voltage clamp output current.

In a low power design, I_{REF} is very small, i.e. $\leq 100nA$. The device size of P2 needs to be much larger than the device size of P1 if the voltage clamp output current I_{LOAD} is

large, or the voltage clamp voltage offset will become too large. Moreover, the variance of I_{LOAD} will introduce large offset due to mismatch of overdrive voltages between P1 and P2. In order to address this problem, a new low power active voltage clamp with improved output accuracy is designed and shown in Figure 4.13.

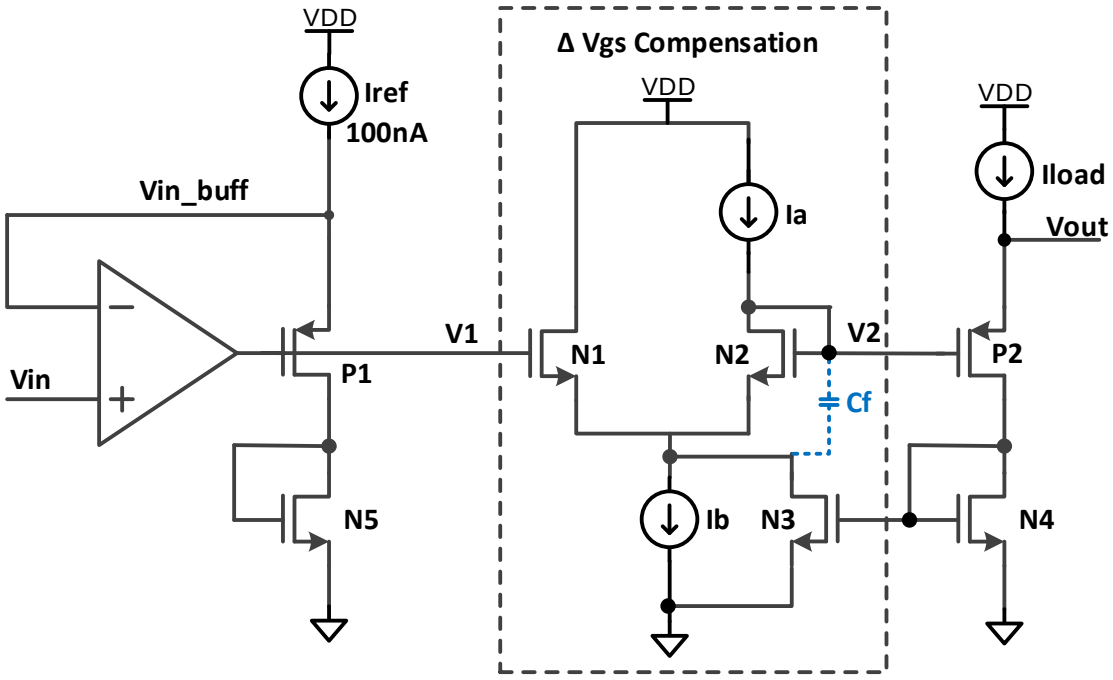

Figure 4.13. Proposed low power active voltage clamp with improved output accuracy

In the proposed active voltage clamp, transistors N1 and N2 form a ΔV_{gs} compensation pair. Two current sources I_a and I_b are used. And I_b is set to slightly larger than I_a, I_a equals to I_{REF}. The current mirror formed by N3 and N4 has a 1:1 ratio. If the threshold voltage mismatches between P1and P2; N1and N2 are neglected, and the input voltage offset of the amplifier also neglected, the active clamp offset voltage V_{OS} can be calculated by:

$$V_{OS} = \left(\sqrt{\frac{2(I_b - I_a + I_{LOAD})}{K_n(W/L)_{N1}}} - \sqrt{\frac{2I_{REF}}{K_n(W/L)_{N2}}}\right) - \left(\sqrt{\frac{2I_{LOAD}}{K_p(W/L)_{P2}}} - \sqrt{\frac{2I_{REF}}{K_p(W/L)_{P1}}}\right)$$

$$\approx \left(\sqrt{\frac{2I_{LOAD}}{K_n(W/L)_{N1}}} - \sqrt{\frac{2I_{REF}}{K_n(W/L)_{N2}}}\right) \tag{4.11}$$

$$- \left(\sqrt{\frac{2I_{LOAD}}{K_p(W/L)_{P2}}} - \sqrt{\frac{2I_{REF}}{K_p(W/L)_{P1}}}\right)$$

Sizing transistors N1, N2, P1 and P2 as:

$$\frac{(W/L)_{N1}}{(W/L)_{P2}} = \frac{(W/L)_{N2}}{(W/L)_{N2}} = \frac{K_p}{K_n} \tag{4.12}$$

And substitute (4.12) into (4.11), the voltage clamp offset voltage is reduced to:

$$V_{OS} = 0 \tag{4.13}$$

Thus, by using the ΔV_{gs} compensation pair, the proposed active voltage clamp can greatly reduce the offset voltage. A feedforward capacitor C_f shown in Figure 4.13 can be used to reduce the transient voltage overshoot caused by the delay of N3/N4 current mirror pair.

4.8 Current Reference Circuit

A reliable and accurate current bias circuit is crucial for all other analog circuit blocks. A low voltage current reference circuit based on a constant Gm topology [47] is designed and shown in Figure 4.14. The constant Gm topology provides an output reference current immune to process, supply voltage and temperature (PVT) variations and can be tuned by an external resistor. In order to make the reference circuit can work in a low input supply

voltage, the conventional cascade structure are replaced by a negative feedback baby amplifier to increase the transistor output impedance. The baby amplifier formed by P3, P4, N3 and N4 is used to ensure the drain-to-source voltages of current mirror devices P1 and P2 are equal. Thus current mirror accuracy is improved without sacrificing the input voltage headroom. A compensation capacitor is necessary since parasitic capacitance introduced by the bonding pad trends to destabilize feedback loops.

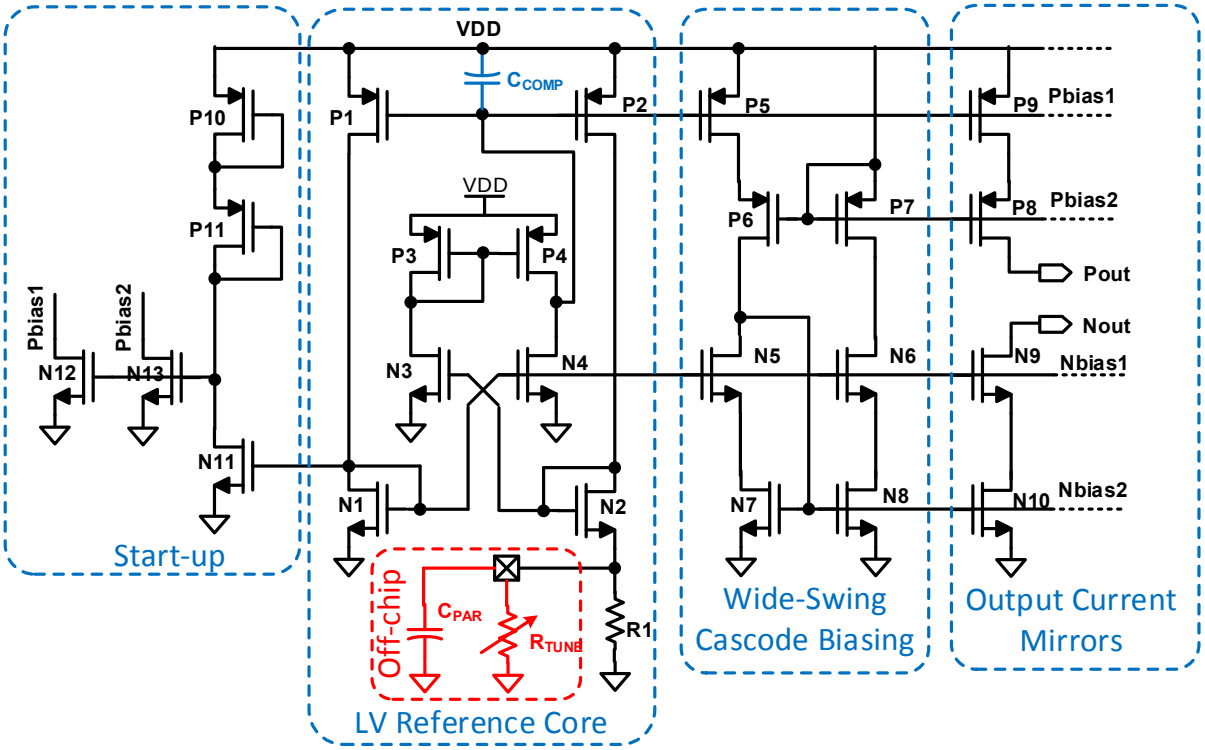

Figure 4.14. Current reference circuit

CHAPTER 5

5 Physical Design and Experimental Results

5.1 Physical Design of the Liquid Crystal Lens Driver

A liquid crystal lens driver chip is designed and fabricated. In order to achieve the highest power efficiency for the given compact size, the power-train capacitors of the switched capacitor converter are placed off-chip. And all power switches and control circuitries are integrated into a single chip with CSMC 0.5μm 12V-45V scalable BCD technology. The die size of the liquid crystal IC is 1890×1770μm^2. Figure 5.1 shows the layout of the chip and Figure 5.2 shows a chip microphotography. All power switch devices are placed on the edge of the chip to minimize the metal resistance between powertrain devices and the output pads. Low voltage domain circuitries and high voltage domain circuitries are separated in the layout to provide a better protection for low voltage devices. Also analog building blocks and digital logic blocks are placed apart from each other to reduce substrate minority injection and cross-talk noise. All critical analog circuits are laid out carefully with common-centroid technique. All sensitive paths also shield by low impedance metal wires which connected to their reference potentials.

Figure 5.3 shows the evaluation board. The driver IC is packed into a 5mm×5mm 32 pins QFN package. External components include four 100nF ceramic capacitors used as SC converter flying capacitors and one 1μF ceramic capacitor used as the output capacitor.

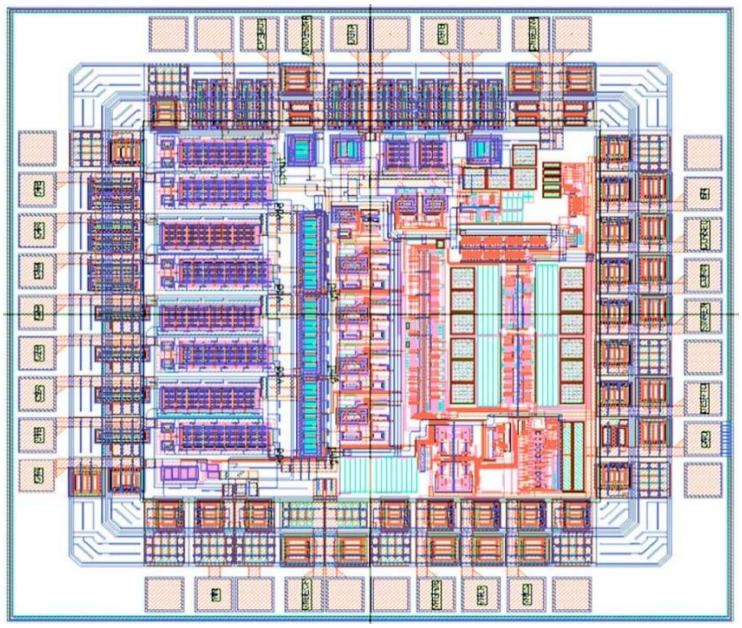

Figure 5.1. Layout of the LCL driver IC

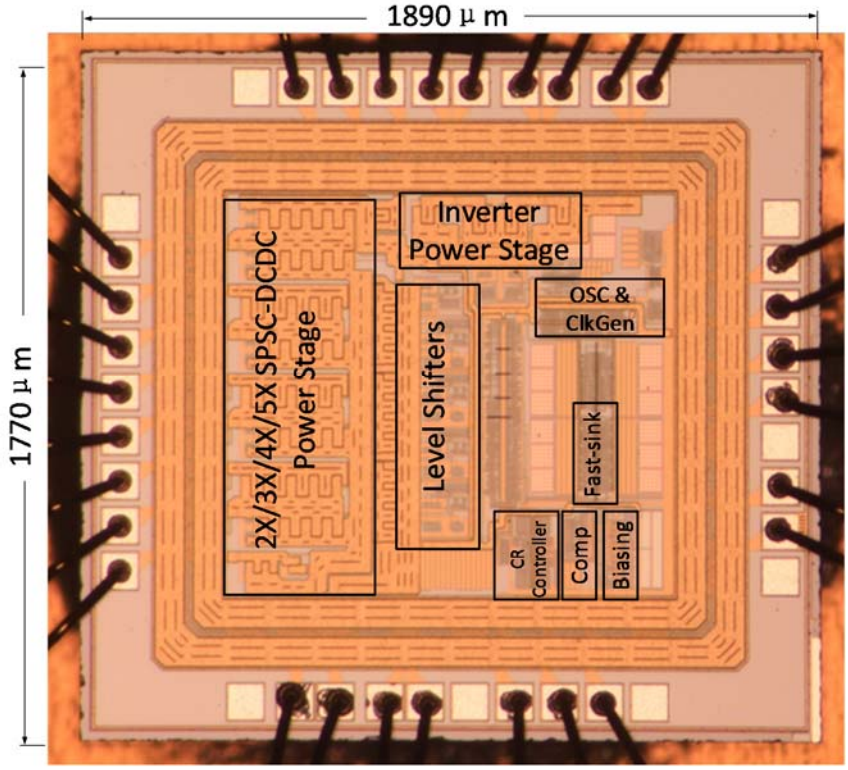

Figure 5.2. Chip microphotography of the LCL driver IC

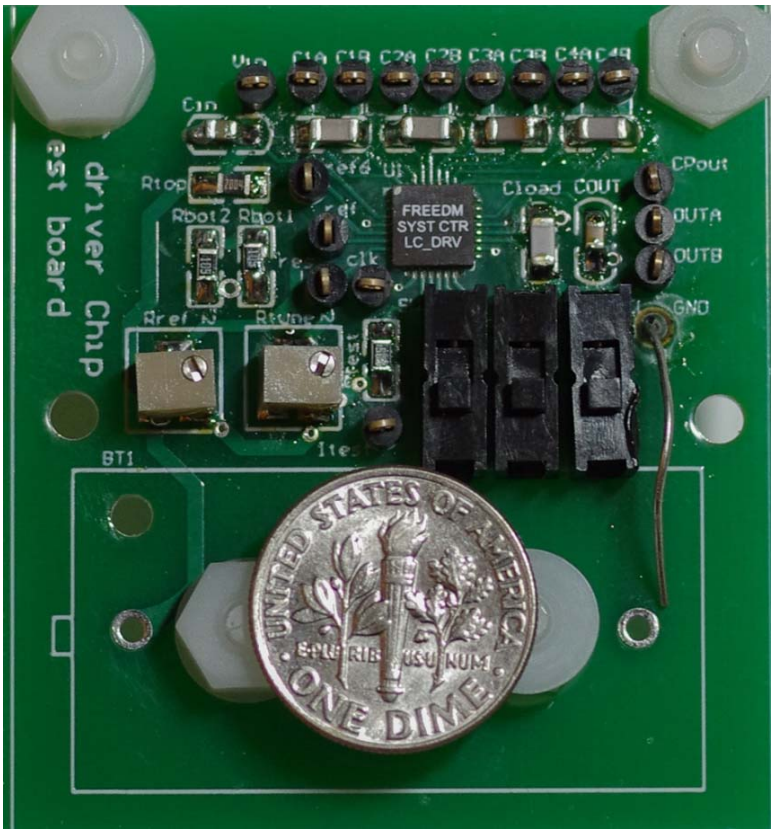

Figure 5.3. LCL driver evaluation board

5.2 Measurement Results

Figure 5.4 - Figure 5.7 show the measured output waveforms of the proposed liquid crystal lens driver at a condition of a 3V input voltage and a 5nF load capacitor to imitate the liquid crystal lens. The output voltage, V_{CPOUT}, of the switched capacitor DC-DC regulator varies from 3 V to 14.9 V. And the output of the liquid crystal lens driver is a square wave AC signal switching at around 1KHz and with a RMS voltage equals to V_{CPOUT}. The output voltage ripple is 116mV. The output voltage falling time from a higher output state to a lower output state is 10.5 ms and 48 μs without and with fast-sink function enabled, respectively.

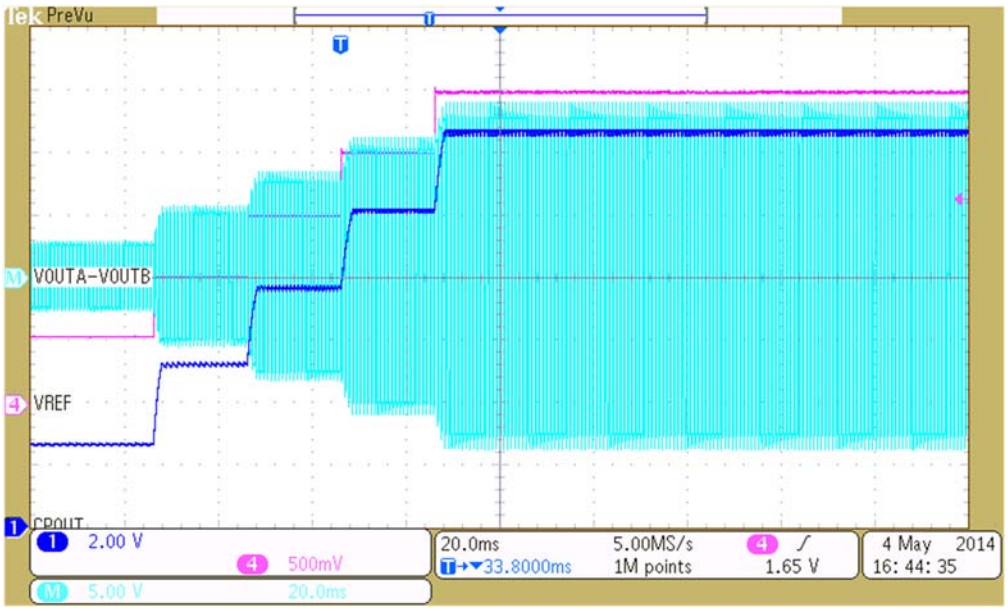

Figure 5.4. Measured output voltage in a step-up sequence 2×3×4×5×

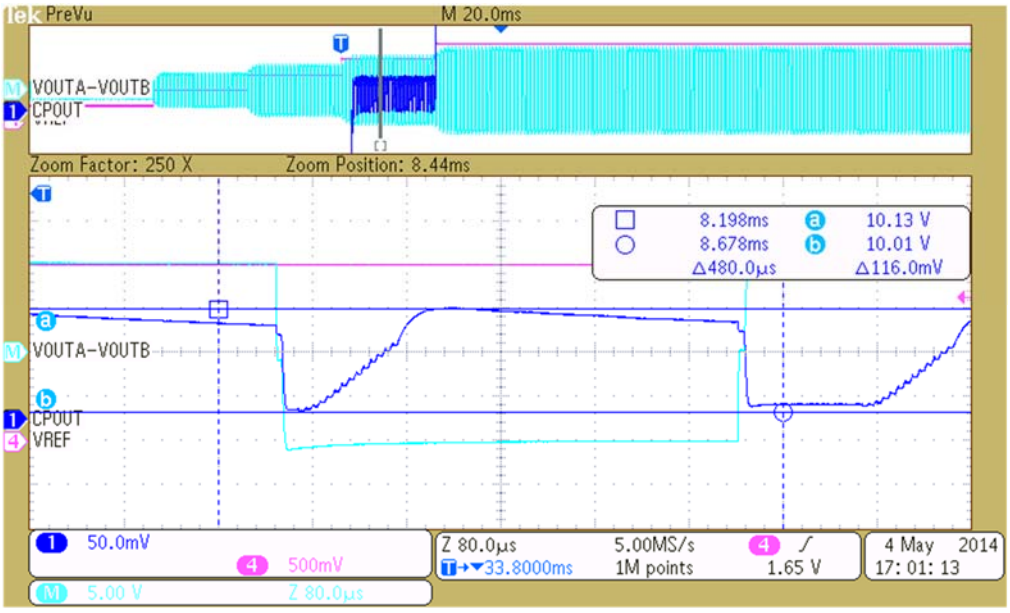

Figure 5.5. Measured output voltage ripple

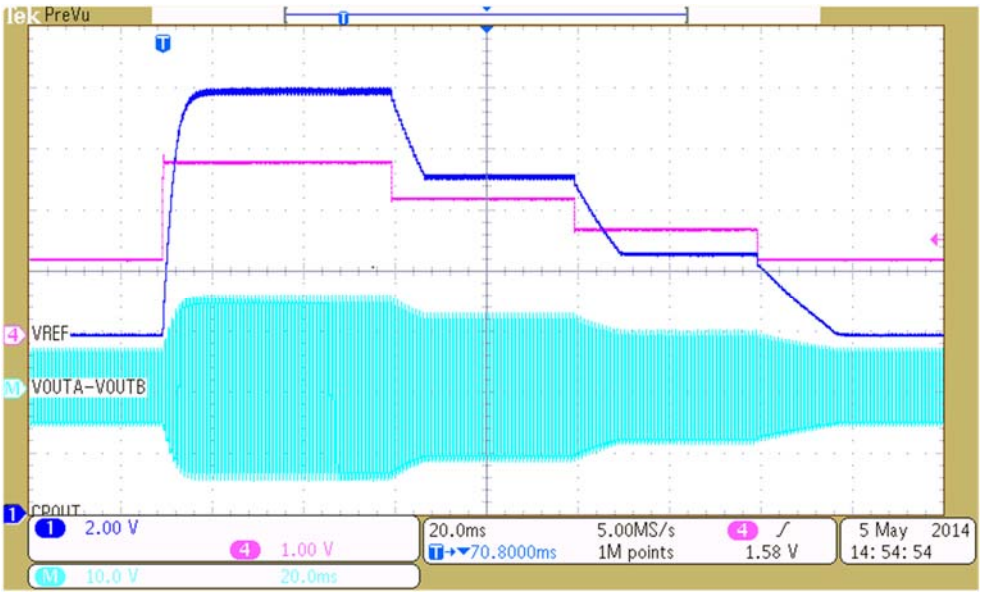

Figure 5.6. Measured output voltage in a step-down sequence 5×4×3×2× without fast sink

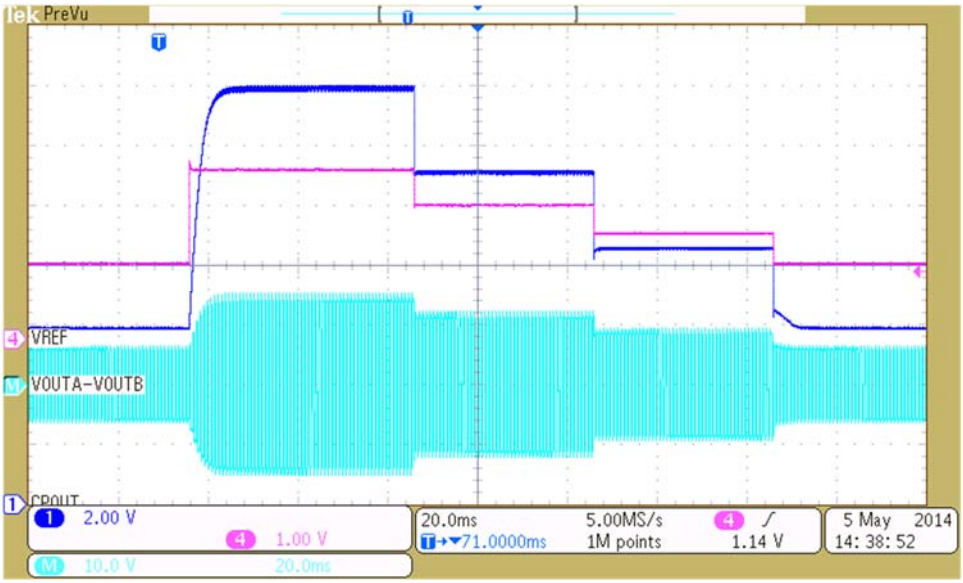

Figure 5.7. Measured output voltage in a step-down sequence 5×4×3×2× with fast sink

Figure 5.8 shows the measured squared wave AC voltage output of the LCL driver. The output switching frequency is determined by the internal ring oscillator and the frequency divider and can be set to between 500 Hz and 10 KHz. The RMS value of the AC output voltage equals to the DC output voltage of the switched capacitor converter. And the symmetric circuit of H-bridge drive provides a zero DC component of the AC output.

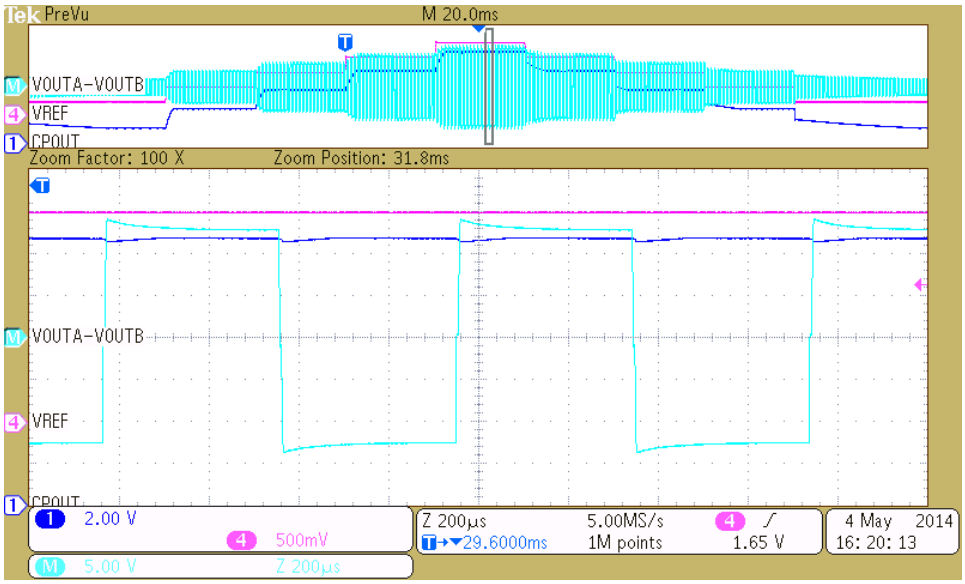

Figure 5.8. Measured AC voltage output of the LCL driver

Figure 5.9 shows the measured power conversion efficiency curve of the proposed liquid crystal lens driver under different load power conditions. The measured peak efficiency is 93.6%. The dual-loop controller optimizes conversion ratios of the switched capacitor converter according to different output voltages and maintains a high power efficiency over a wide range of output power. The efficiency valleys are measure near the boundary of different voltage conversion ratios. Compared with recent published works, the developed SC achieved a record high efficiency in an inexpensive 0.5µm BCD process.

Figure 5.9. Measured power efficiency curve

	VLSI 15 [39]	JSSC 14[48]	ISSCC 13[49]	This Work
Conversion Type	Step-up (2, 2.5, 3, 4)	Step-down (1/3, 1/2, 2/3)	Step-down (1/3, 1/2, 2/3)	Step-up (2, 3, 4, 5)
Input Voltage $[V]$	1.4-3	2.5	1.5	3
Output Voltage $[V]$	4.8V	0.2-1.6	0.4-1.1	3-14.9
Output Power $[mW]$	2.4-48	0.37-3	0.008-1.1	0.18-5.6
Process	0.35µm CMOS	0.35µm CMOS	130nm CMOS	0.5µm BCD
Capacitors	Off chip	MIM	Ferroelectric	Off chip
Chip Area $[mm^2]$	3.8	4.33	0.366	3.34
Peak Power Efficiency	82%	85%	93%	93.6%

Table 5.1. Performance comparison of the proposed IC and recent published works

CHAPTER 6

6 Conclusions

A complete, detail methodology for switched capacitor converter optimal design based on the area constraint is proposed in this work. At first the optimization methodology specifies the relative sizes of each single capacitor and power switch device. After that an optimized ratio between the total capacitor area and the total power switch area is found. Finally the total area and switching frequency are optimized to achieve the highest power conversion efficiency.

Two new figure of merits based on output impedance: a SSL impedance metric and a FSL impedance metric are proposed and can be used to compare performance among converters with different topologies. A guideline is also provided for choosing the best performance converter topology for a specific application and a given silicon process technology with a limit on total system area.

A compact liquid crystal lens driver IC was design to achieve a high power conversion efficiency over a wide output power range. A record peak power conversion efficiency of 93.6% is measured. This is the first demonstration of an integrated power supply for driving liquid crystal lens. And several high performance circuitries used in low power high voltage applications are proposed, including: a reduced voltage ripple H-bridge gate drive; a low power high speed level shifter; a low power comparator with two stages hysteresis; a low

kickback noise dynamic comparator, a high accuracy low power active clamp and a converter output fast sink control scheme.

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