Work-function difference between Al and *n*-GaN from Al-gated *n*-GaN/nitrided-thin-Ga_2O_3/SiO_2 metal oxide semiconductor structures

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In most previous reports on Al-gated *n*-GaN/SiO_2 metal–oxide–semiconductor (MOS) structures, the work–function difference between Al and *n*-GaN (ϕ_{ms}) has been chosen as 0 V by assuming that the work function of the Al gate and *n*-GaN are both 4.1 eV. In this letter, ϕ_{ms} is determined as ~0.1 V using Al-gated *n*-GaN/nitrided-thin-Ga_2O_3/SiO_2 MOS capacitors by measuring flatband voltage as a function of oxide thickness. Formation of an ultrathin (~0.6-nm-thick) Ga_2O_3 layer on *n*-GaN prior to the deposition of SiO_2 is important to prevent uncontrolled parasitic oxidation of the *n*-GaN surface and possibly reduces the interface dipole between *n*-GaN and SiO_2. © *2004 American Institute Of Physics*. [DOI: 10.1063/1.1767599]

In most previous reports on Al-gated *n*-GaN metal–oxide–semiconductor (MOS) structures,[1,2] the work-function difference between metal and semiconductor (ϕ_{ms}) has been chosen as 0 V by assuming that the work function of the Al gate and *n*-GaN are both 4.1 eV. The theoretical capacitance-voltage (*C–V*) curves for Al-gated *n*-GaN MOS capacitors have been drawn with this assumption. Although the exact value of ϕ_{ms} must be known to determine the fixed oxide charge density (Q_f) and little is known about the work function of GaN, there has been no effort to measure ϕ_{ms} using *n*-GaN MOS structures. In this letter, we report ϕ_{ms} as determined from the flatband voltage of Al-gated *n*-GaN/nitrided-thin-Ga_2O_3/SiO_2 MOS capacitors with various gate oxide thicknesses by applying $V_{fb} = \phi_{ms} - Q_f t_{ox}/\varepsilon_{ox}$, where V_{fb} is the flatband voltage, ε_{ox} is the dielectric constant of SiO_2, and t_{ox} is the oxide thickness.[3] Two underlying assumptions are (i) absence of mobile and bulk oxide charge, and (ii) equal Q_f in samples with different t_{ox}. The nitrided-thin-Ga_2O_3 layer (~0.6 nm thick) was prepared on *n*-GaN prior to the deposition of SiO_2 to prevent parasitic subcutaneous oxidation during the latter.[4,5]

A homoepitaxial Fe-doped insulating GaN buffer/unintentionally doped GaN template/Si-doped GaN structure was grown on sapphire by metalorganic chemical vapor deposition. The bulk carrier density of the Si-doped GaN layer was 3.3×10^{17} cm^{-3}. The *n*-GaN samples were etched in a 1:5 $NH_4OH:H_2O$ solution at 80 °C for 15 min, oxidized by remote O_2/He plasma at 0.3 Torr for 30 s to form a thin (~0.6 nm) Ga_2O_3 film at the surface, and the resulting structure was nitrided by remote N_2/He plasma at 0.3 Torr for 90 s.[5,6] *In situ* SiO_2 deposition was then performed by remote plasma-enhanced chemical vapor deposition (RPECVD) with 2%-SiH_4 in He and an O_2/He gas mixture.[5,6] For all remote plasma processing, substrate temperature was 300 °C and rf power was 30 W at 13.56 MHz. After SiO_2 deposition, the samples were rapid-thermal annealed at about 900 °C for 30 s in Ar. A 300-nm-thick Al layer was evaporated onto samples with various thicknesses of SiO_2 and gates were defined using a conventional lithographic process. Postmetallization annealing was performed at 400 °C for 30 min in forming gas (N_2/H_2). Electrical properties of the MOS capacitors on *n*-GaN were investigated using an HP 4284A precision inductance-capacitance-resistance meter. The area of devices under test was $(1–4)\times10^{-4}$ cm^2.

Figure 1 shows measured and simulated *C–V* curves for capacitors with various equivalent oxide thickness (EOT). The *C–V* curves were measured at 1 MHz and 25 °C in the dark, and the gate voltage (V_G) was swept from positive to negative. The measured *C–V* curves show clear deep depletion behavior, and are well described by simulated *C–V* curves without inversion. The net donor concentration (N_D) in *n*-GaN was calculated as $(3.9–4.2)\times10^{17}$ cm^{-3} from the range of the *C–V* curves in which the plot of $1/C^2–V$ showed linear behavior. In the evaluation of expressions for the theoretical *C–V* curves,[3] the same fundamental constants as in a previous report[1] were used. Simulated ideal *C–V* curves (without interface states and Q_f) were shifted to the negative voltage direction until they showed good agreement with experimental data. Discrepancy between measured and simulated *C–V* curves is ascribed to stretch-out of the measured data due to emission of electrons trapped in interface

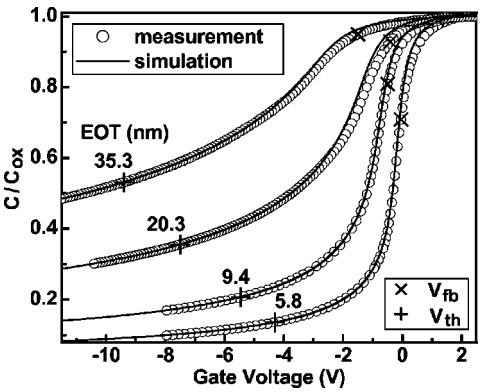

FIG. 1. Measured and simulated *C–V* curves for *n*-GaN/nitrided-thin-Ga_2O_3/SiO_2 MOS capacitors with various equivalent oxide thicknesses. Capacitance is normalized by oxide capacitance (C_{ox}). Flatband voltage (V_{fb}) and threshold voltage (V_{th}) from simulations are also shown.

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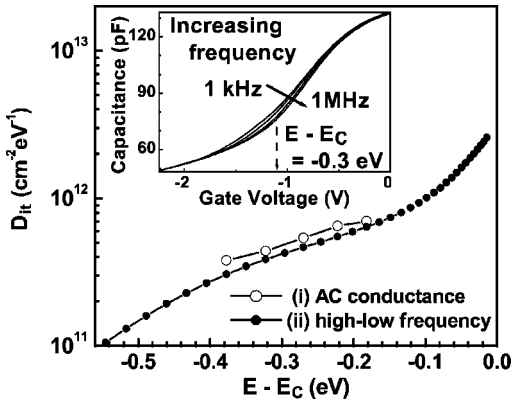

FIG. 2. Density of interface states (D_{it}) as a function of energy from the GaN conduction band edge (E_c) for an *n*-GaN MOS capacitor with 9.4 nm of EOT, as determined by the (i) ac conductance, and (ii) high–low frequency methods. The inset shows the frequency dependence (1, 10, 100 kHz, and 1 MHz) of the $C-V$ characteristics.

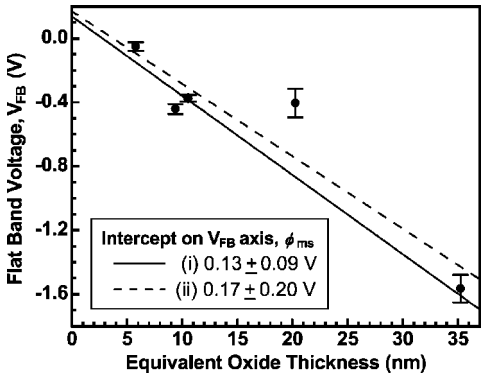

FIG. 3. Linear fits to flatband voltage (V_{fb}) vs EOT data (i) excluding, and (ii) including the sample with 20.3 nm EOT. The intercept on the V_{fb} axis, or ϕ_{ms}, is determined as (i) 0.13 ± 0.09 V, and (ii) 0.17 ± 0.20 V, respectively. When the plot of V_{fb} vs thickness of SiO_2, or EOT subtracted by 0.6 nm, was fit excluding the 20.3-nm-thick sample (not shown), ϕ_{ms} was 0.10 ± 0.09 V. Displayed error bars are standard deviations of measured V_{fb} for *n*-GaN MOS capacitors in each sample. Standard deviations of EOT were below ±1% of EOT for each sample.

states. The $C-V$ hysteresis window (retrace from negative to positive V_G) at flatband capacitance was −0.5 V for the sample with 20.3 nm of EOT, and 10–50 times lower for the other samples.

Figure 2 shows the density of interface states (D_{it}) as a function of energy from the conduction band edge (E_c) for the sample with 9.4 nm of EOT. D_{it} was evaluated using (i) the ac conductance, and (ii) the high–low frequency methods.[3,5] The inset shows the frequency dependence of $C-V$ characteristics. V_G (−1.1 V for this sample) at which the $C-V$ curves at 1 kHz and 1 MHz showed the maximum capacitance difference (ΔC_{max}) was used to determine the energy level at which the minimum D_{it} can be extracted without underestimation.[5] For V_G below −1.1 V ($E-E_C<-0.3$ eV), the extracted D_{it} rapidly decreases due to the increased time constant for electron emission from interface states. The actual D_{it} is higher than estimated using this high-low frequency method because 1 kHz is not sufficiently low to allow a response from slow interface traps. D_{it} directly determined from ΔC_{max}, however, is useful to compare different samples. While the minimum D_{it} of the sample with 20.3 nm of EOT is 9×10^{11} cm^{-2} eV^{-1}, the minimum D_{it} of other samples is in the range of $(2-6)\times10^{11}$ cm^{-2} eV^{-1}.

Figure 3 shows linear fits to the V_{fb}-EOT data (i) excluding, and (ii) including the point at 20.3 nm EOT. Displayed error bars are the standard deviations of V_{fb} measured for different capacitors on each sample. The standard deviation of EOT is below ±1% of EOT for each sample. Note that the sample showing 20.3 nm of EOT presented higher D_{it} and wider hysteresis window than other samples. Sequential etching of SiO_2 could be considered to produce samples with different EOT and the same D_{it}. From the linear fits to the data (i) excluding, and (ii) including the point at 20.3 nm EOT, ϕ_{ms} and the effective number of oxide fixed charge (N_f) were determined as (i) 0.13 ± 0.09 V and $(1.01\pm0.11)\times10^{12}$ cm^{-2}, and (ii) 0.17 ± 0.20 V and $(0.97\pm0.22)\times10^{12}$ cm^{-2}, respectively. Q_f extracted from the slope is the effective Q_f, which is the sum of true Q_f and interface trapped charge.[7] In the case of MOS capacitors on an *n*-type substrate at V_{fb}, most of the interface states will be occupied by electrons. Such electrons in acceptor-type interface states appear as negative Q_f. The effective Q_f is positive, so that the true N_f is the sum of effective N_f and the number of electrons in acceptor-type interface states. The extracted values of Q_f are several times higher than the minimum D_{it} (in the range of low-to mid-10^{11} cm^{-2} eV^{-1}) and typical Q_f for the same RPECVD SiO_2 films on Si. Considering such high value of Q_f, we speculate that the major amount of Q_f is located at the $Ga_2O_3-SiO_2$ interface rather than at the $GaN-Ga_2O_3$ interface or in bulk SiO_2. When the plot of V_{fb} versus thickness of SiO_2 film, or EOT subtracted by 0.6 nm, was fit excluding the 20.3-nm-thick sample (not shown), ϕ_{ms} and effective N_f were 0.10 ± 0.09 V and $(1.01\pm0.10)\times10^{12}$ cm^{-2}.

Controversy remains concerning Fermi level pinning at the *n*-GaN/SiO_2 interface (Ref. 8 and references therein). Irreproducible *n*-GaN-SiO_2 interfaces are due to parasitic subcutaneous oxidation of the GaN surface during SiO_2 film deposition.[4,5] Such uncontrolled interfacial Ga_2O_3 formation during SiO_2 film deposition and postdeposition annealing steps results in interface defects. The controlled ultrathin Ga_2O_3 layer is crucial to prepare *n*-GaN MOS devices with a low density of interface defects.[5,6] A direct *n*-GaN-SiO_2 interface (without detectable Ga_2O_3) was prepared by annealing the substrate at 860 °C for 15 min in a NH_3 atmosphere and depositing an ultrathin Si sacrificial layer, which was then oxidized.[9] Using ultraviolet photoemission spectroscopy (UPS), the conduction band offset and interface dipole of this direct *n*-GaN–SiO_2 interface were deduced as 3.6 and 1.8 eV, respectively. There is no report on an MOS capacitor using this direct *n*-GaN-SiO_2 interface. If the work function of Al and the electron affinity of SiO_2 are taken as 4.1 and 1.1 eV, respectively, ϕ_{ms} for the direct *n*-GaN–SiO_2 MOS structure with Al gate should be −0.6 V. The difference in ϕ_{ms} between −0.6 V for the direct *n*-GaN–SiO_2 structure and ~0.1 V for our *n*-GaN/nitrided-thin-Ga_2O_3/SiO_2 MOS capacitors [which is close to the value assumed (0 V) in most previous work concerning MOS capacitors on *n*-GaN] can be ascribed to a reduced interface dipole between the ionic *n*-GaN substrate and the covalent SiO_2 film due to the interfacial Ga_2O_3. A detailed discussion will be possible after we determine the conduction band offset between *n*-GaN and nitrided-thin-Ga_2O_3/SiO_2 by UPS following the approach in Ref. 9.

In summary, ϕ_{ms} for Al-gated *n*-GaN/nitrided-thin-Ga_2O_3/SiO_2 MOS capacitors was determined as $\sim$0.1 V from a linear fit to the V_{fb}-EOT plot. The minima D_{it} were in the range of $(2-6)\times10^{11}$ cm^{-2} eV^{-1}, exception being made to the sample with 20.3 nm EOT. The major amount of Q_f should be located at the $Ga_2O_3-SiO_2$ interface. The formation of an ultrathin ($\sim$0.6-nm-thick) Ga_2O_3 layer on *n*-GaN prior to the deposition of SiO_2, which is crucial to prevent uncontrolled parasitic oxidation of the *n*-GaN surface,[5,6] can possibly reduce the interface dipole between the ionic GaN substrate and the covalent SiO_2 film.

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