ABSTRACT

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A key challenge to any DC power system is protection. In addition to the natural absence of a zero voltage crossing, the power electronics technology in these systems brings with it greater di/dt during a fault and dv/dt during actuation, threatening sensitive components. All of these aspects pose a challenge to conventional circuit protection which typically responds relatively slowly and rely on the zero voltage crossing to quench drawn arcs. Solid State circuit breakers (SSCBs) offer a solution to these problems though they come with their own challenges and limitations.

This thesis gives an in-depth exploration of solid-state circuit breaker technology and introduces a design philosophy that allows for current and voltage scaling up to medium voltage range and addresses the challenges of efficiency and energy absorption during a short circuit event. Special attention is given to the problem of thermal energy absorption and designing for improved heat storage capacity in the SSCB module. A novel method for estimating average power dissipation in the SSCB during short circuits is proposed to expedite the iterative thermal design process and several design trade-offs are identified.

Additionally, SSCB technology incorporating recent advances in super cascode power modules is explored. A design example of a 10 kV, 100A solid state circuit breaker is provided and a scaled down prototype is demonstrated capable of withstanding a 7X over-current for 1 μs and short circuit interruption in approximately 60 ns.

Investigation of Short Circuit Capacity of Power Modules for Solid State Protection

by
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DEDICATION

To my parents for their unending love, support, and encouragement to always do my best in all things. To my loving wife, Allison, who has been an inspiration since the day I met her and who has been an endless source of comfort and encouragement. And lastly to Dean, for demanding pets incessantly over the course of writing thixzsery3dzfzddddddddddddddd

BIOGRAPHY

Bahji Ballard is a PhD student at North Carolina State University studying under Dr. Hopkins at the FREEDM research center. He received his BA in Computer Engineering from the University of Texas at Dallas where he worked under Dr. Babak Fahimi in the Renewable Energy and Vehicular Technology (REVT) lab. Here he developed a GaN half bridge module while participating with a team of undergraduates in the IEEEs 2013 International Future Energy Challenge. Before graduate school he worked with a small power electronics start up developing energy harvesting footwear. His current research focuses on solid state circuit breakers in medium voltage and thermal transient handling in SSCB modules. In his spare time, he enjoys music, video games, and jumping on stuff.

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1

INTRODUCTION

The impetus for Solid-State circuit protection is capitalizing on wide band gap (WBG) semiconductor devices to disrupt conventional power system protection with solid-state alternatives in response modern electric power consumption demand.

1.1 Background

1.1.1 Power System Protection

Protection is an essential component of power systems to prevent catastrophic damage to hardware and, potentially, even loss of life due to electrical faults in the system. A protection system must be able to detect faults and isolate them with a high degree of reliability. Reliability in this context has two facets: dependability and security. Dependability is the

measure of how often a system fails to operate when it is expected too, while Security is a measure of how often a system operates when it is not expected too. Real world protection systems favor a conservative design, trading off dependability for security. Protection systems are made up of current interruption devices, or circuit breakers (CBs), sensing devices, and logic devices. In high voltage power systems these elements are typically discrete devices while at lower voltages they are integrated as in cabinet switchgear or moulded case breakers as seen on Fig. 1.1.

(a) (b) (c)

Figure 1.1 (a) Typical Moulded Case Circuit Breaker (b) MV Switch-gear Cabinet (c) 138 kV Oil Circuit breaker

The primary function of the CB is to stop a fault current, isolating and de-energizing the faulted portion of a circuit, as fast as possible to minimize the stress on the rest of the system. Additionally the device needs to be able to withstand the fault current for some quantity of time to account for the delay times used for coordination. Conventional interruption devices, i.e. fuses and circuit breakers, do this through mechanical means. A fuse intentionally burns itself out in a controlled way while a conventional circuit breaker has physical contactors that are mechanically pulled apart. An arc forms during contact separation and this arc must be extinguished before current is fully interrupted, typically by drawing it out over some distance in air. For very high voltage equipment mediums other than air are required to extinguish the arc within a reasonable distance such as oil or SF6 gas.

A protection system is broken up into tiered zones of protection based on proximity to

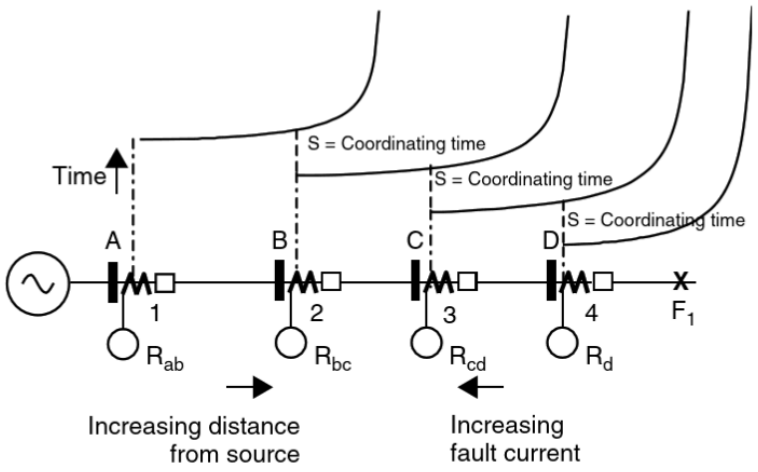


Figure 1.2 Circuit Breaker Coordination Principles [31]

the source, with CBs at the boundaries of each zone. Zones will overlap slightly to ensure full coverage of the system. CBs need to be coordinated in order to provide better selectivity, isolating as little of the overall system as possible. This coordination is created by introducing a short delay between fault detection and device actuation where the delay is shorter the farther the device is from the current source, as seen in Fig. 1.2. CBs are sized based on the short circuit capacity present in the power system and coordination timing required.

1.1.2 Wide Band Gap Semiconductors

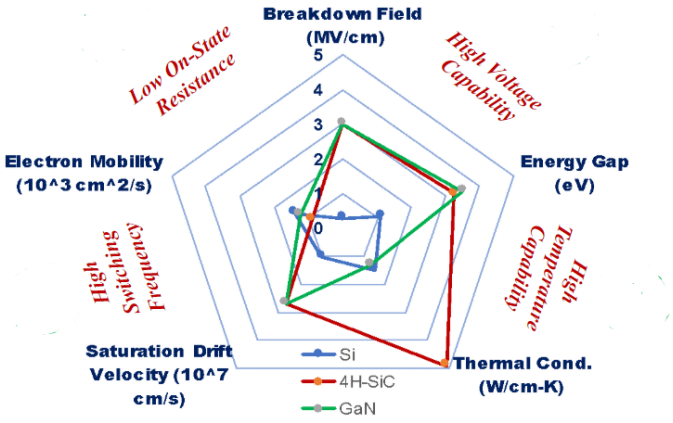


Figure 1.3 Semiconductor Material Properties Comparison

Silicon is a mature semiconductor material system used in a broad range of applications [4]. In the power electronics space, innovations dating back two decades have allowed for the development of power semiconductor devices (referred to simply as devices) that exceed what was thought to be the theoretical limits of the material [40]. However, in application spaces such as power conversion and solid state circuit breakers (SSCBs), there is still demand for even greater performance that silicon devices struggle to meet [56].

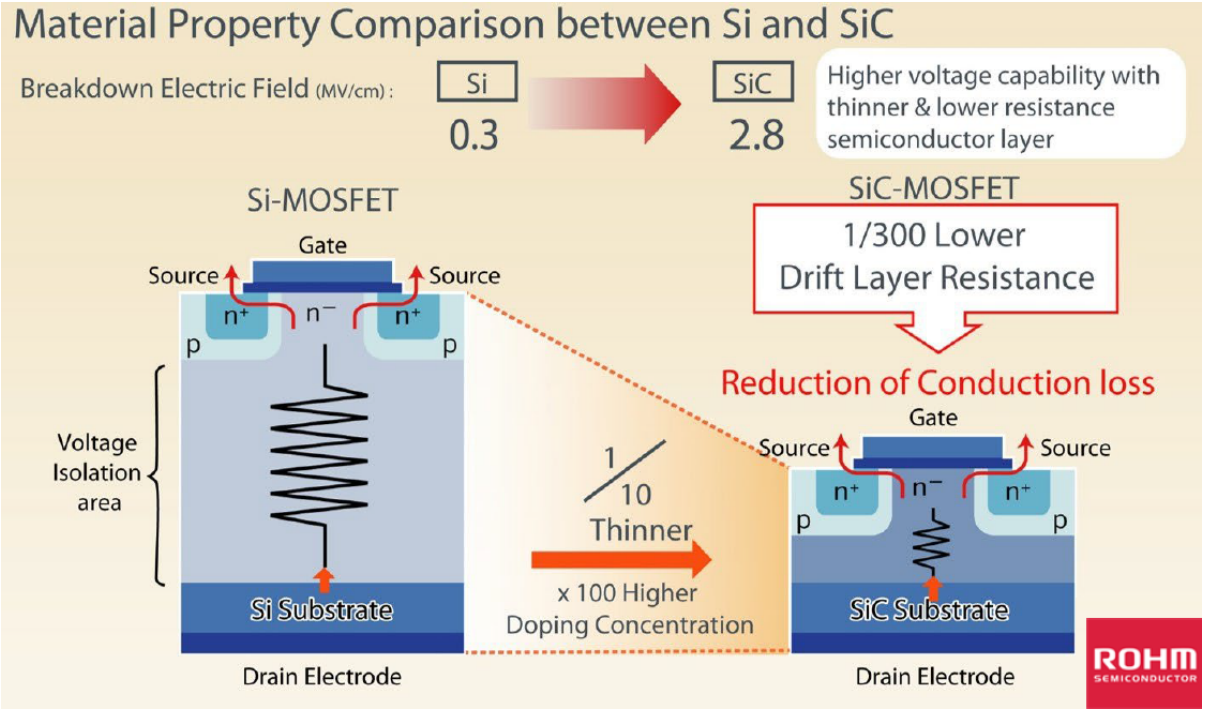


Figure 1.4 Drift layer comparison between Si and SiC (extracted from [41])

The material properties of WBG semiconductor materials, plotted on Fig. 1.3, offer the promise of performance where silicon falls short. The large electric field breakdowns of Gallium Nitride (GaN) and Silicon Carbide (SiC) would enable devices to be made significantly thinner for equivalent breakdown voltage ratings resulting in devices with significantly lower on-state resistance (R_{ON}), as illustrated in Fig. 1.4. The reduced conduction losses combined with higher overall breakdown voltage ratings would also improve the feasibility of SSCBs for higher voltage systems. The thermal conductivity (K) of SiC, in particular, is comparable to that of Copper, enabling SiC devices to dissipate more heat and operate at

greater power densities [58]. The technology is beginning to mature and there are now commercially available WBG devices, motivating research into sundry applications including SSCBs.

1.2 Motivation: Solid-State Circuit Protection

When the American power grid was built, the two most common types of electrical loads were motors and lighting, both of which consumed AC power [3]. Today, the digital revolution has introduced an ever growing number of DC load, i.e. computers, data centers, electric vehicles, even lighting. While electric motors are still prevalent, DC motors have become preferred in a number of applications [61]. Estimates show that DC loads currently make up over 50% of total electricity consumption in the US and 80% of electricity will pass through power electronic conversion hardware by 2030 [17]. The changes haven't been isolated to loads; solar, wind and distributed energy storage all output DC power which must be inverted to AC before it can be input to the current electrical grid. As a result, there is growing demand for DC power systems and micro-grids to improve efficiency [55]. Power electronics, i.e. switching converters and solid-state transformers, are required to take the place of traditional magnetic transformers that cannot operate in DC. However the removal of transformers from a power system reduces the system inductance present which increases the ramp rate (dI/dt) in the event of a short circuit. In addition, switching converters are more sensitive to over-current than transformers. Therefore, protection systems must respond to faults faster to prevent catastrophic failure of equipment.

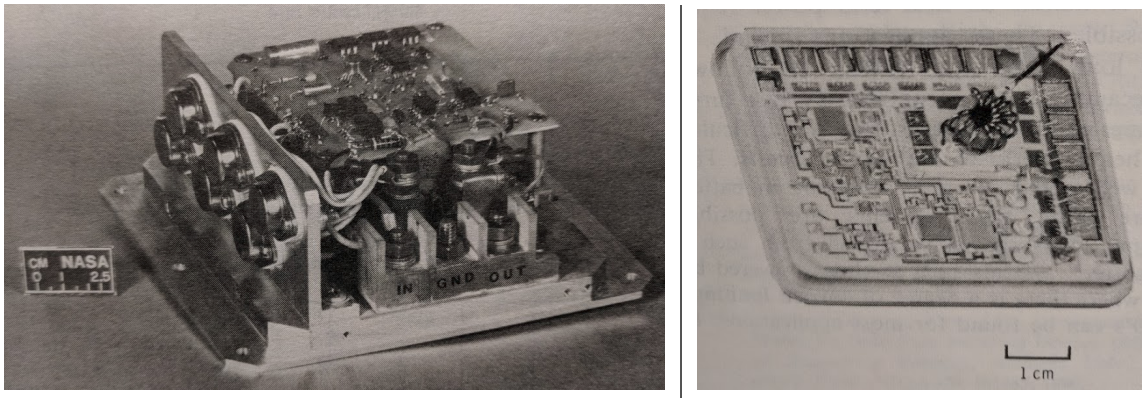
Mechanical circuit breakers actuate on the order of tens of milliseconds, with only specialized equipment for specific voltages and applications such as GFCIs performing faster, which is too slow to protect power electronic equipment [55]. Additionally, mechanical breakers take advantage of the zero voltage crossing present in an AC signal. A DC signal does not provide a zero voltage crossing, necessitating over-sizing the beaker to

reliably extinguish the arc that forms during actuation. Solid-state circuit protection offers a potential solution. A solid-state circuit breaker (SSCB) uses power semiconductors to interrupt current, replacing the mechanical contactors of a conventional solution. The current is interrupted within the bulk of the semiconductor material which allows for arch-less actuation. Semiconductors are controlled electronically meaning delay times can be set and changed in situ through digital controls. Depending on the semiconductor device used, actuation times of tens of nanoseconds are possible, orders of magnitude faster than conventional breakers. There are, however, engineering trade-offs and challenges to a solid-state solution. The majority of a circuit breaker's operating life is spent acting as a conductor until it needs to actuate. Semiconductor materials have lower conductivity than the metal contactors, generating additional power loss, and making the device more susceptible to thermal runaway during a fault. The development of SSCBs using WBG devices seeks to mitigate the efficiency loss to capitalize on the fast actuation needed to ensure the protection of sensitive power electronics in DC micro-grid systems, improving reliability and efficiency.

1.3 State of the Art

One of the earliest applications for Solid-state circuit protection was solid state power controllers (SSPC) for aerospace. SSPCs combine the functions of connecting loads to a main bus and providing protection from short circuits. NASA funded several development programs for high-voltage, high-power, SSPCs for use on the space shuttle in the mid 1980s. Initially silicon controlled rectifiers (SCRs) were used as the switching element but were later replaced by MOSFETs and gate turn-off transistors (GTOs) to reduce weight and power consumption. Several solid metal chasis modules were fabricated and a "hybrid circuit" module was pioneered, seen in Fig. 1.5(b), that is now recognizable as a power module on ceramic substrate [57]. Similar power controller modules were developed for

the International Space Station (ISS) to regulate power flow between its 120V main and auxiliary bus and 28V payloads [26].



(a) (b)

Figure 1.5 NASA Solid-State Power Controller Modules: (a) MOSFET based module (b) "hybrid circuit" module [57]

As the field of aerospace advanced with the development of "More Electric Aircraft" (MEA) and "All Electric Aircraft" (AEA), on-board electrical systems standardized around common system ratings such as 270V DC and 540V DC at ranging from 30 to 100A based on weight considerations [35, 45, 50]. The latest developments in SSPCs and SSCBs for AEA have focused on SiC modules to provide lower conduction losses, higher thermal conductivity, and better reliability and voltage scalability [1, 13, 21, 25, 55]. In [28], an all-SiC power module for 270 Vdc MEA systems capable of breaking a 250 A fault in 10 μs, and a 450 A fault in 70 μs, is presented.

In recent years SSPC and SSCB technology has been extended to other micro-grid applications such as distributed energy systems (DES), all electric vehicles, and data centers [10, 24, 37, 49, 53, 62]. In [47], effective fault discrimination by a self powered SSCB, first published in [54], is validated on a 340V DC residential community microgrid. The self powered SSCB, further refined in [29, 30, 43, 67], uses a forward-flyback DC/DC converter based gate drive to both detect and autonomously interrupt a fault current within a few microseconds. The most recent extensions include digital control with adjustable time-current profile

and PWM current limiting to protect against nuisance trips caused by inrush currents [29, 68]. In [52], a DC circuit breaker using SiC Static Induction Transistors was proposed as a high-speed over-current protection solution for a 400V DC distribution system for data centers. An accompanying novel gate voltage waveform control was proposed to address over-voltage and transient oscillation during the interruption process. A bidirectional solid-state circuit breaker was proposed in [60] to address the need for bidirectional current flow on many DC power systems. The 600 V, 60 A SSCB was presented along side a novel gate driver capable of both self-triggered, temperature-compensated over-current protection and external triggering.

Growing demand for medium voltage micro-grids and DC distribution systems has engendered further interest in SSCBs in the medium voltage and even high voltage range though few practical or cost effective solutions currently exist [16, 38, 42, 48]. A 1000 V SSCB using cascaded 1200 V SiC JFETs capable of interrupting 125 A within 2.5 μs was proposed in [51] with attention given to voltage sharing among cascaded switches. In [12], a 10 kV DC SSCB based on series-connected Press-Pack IGBTs capable of interrupting 5.1 kA within 5.5 ms was proposed for the protection of high voltage DC voltage source converters. In [65, 66], a 15 kV/200 A SSCB based on parallel-connected SiC ETOs was demonstrated at 4.5 kV/200 A, however interruption time was not reported due to available current sensors having too low a bandwidth. [36] appears to demonstrate a 10 kV SSCB interrupting 1000 A in approximately 5 μs with reliability tested with 10,000 operations at 1 kA, however only conceptual drawings of the physical breaker are provided. Recently published variations on the hybrid circuit breaker provide additional solutions for high voltage circuit protection including the transient commutation current injection circuit [69], Load Commutation Switches [27], and Electronically Assisted Circuit Breakers [14], however this work is limited in scope to SSCBs.

1.4 Goals and Outline

The goal of this work is to develop a general design process for solid state circuit breakers scalable to the medium voltage range. Special attention is given to the thermal design.

In chapter 1 the background and motivation for the thesis is provided. Chapter 2 discusses the design approach for SSCBs including sizing considerations for transient energy absorption components. Chapter 3 explores the challenges of thermal design and outlines an approach for developing a directed initial design. Chapter 4 presents an example SSCB design using Super Cascode Power Modules (SCPMs) and a proof of concept for SCPM short circuit interruption. Chapter 5 discusses the conclusion and future work.

CHAPTER

2

SSCB DESIGN

The goal is to define a scalable methodology for designing Solid-State Circuit Breakers (SSCBs) that can provide comparable levels of reliability, security, and selectivity offered by the mechanical protection devices they would replace. Scaling an SSCB into the Medium voltage range is now possible with WBG power semiconductor devices. Our approach will outline opportunities for optimization to improve the cost per performance ratio.

2.1 Topology

The solid state circuit breaker is a two terminal device placed directly in the line. Typically, mechanical circuit breakers for AC and DC power systems are considered differently. However, because an SSCB is capable of microsecond or less actuation, an AC fault current is

effectively a DC fault during actuation. Additionally, even though a circuit breaker could be designed to monitor unidirectional fault current, the device may be required to conduct and operate with reverse current flow. For instance, Li-ion battery systems require charge and discharge cycles and, in larger systems, a fault on the grid side of the CB would draw fault current in the reverse direction. Therefore, an SSCB must support bi-directional current flow. In the absence of a commercially available, four quadrant switch, a switching block composed of multiple semiconductor devices must be used. Various bidirectional switching block configurations are shown in Fig. 2.1. The added part count required to support bi-directional current flow further constrains efficiency due to conduction losses, and requires proper scaling to address. For the purposes of this work, the first configuration from Fig. 2.1, the back to back switch, is selected for its low part count and concomitant efficiency.

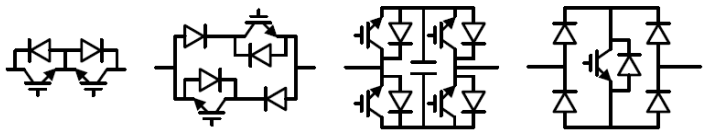


Figure 2.1 Bidirectional Switch Blocks [38]

The full SSCB topology consists of multiple parallel branches, each representing a layer of energy absorption that will activate as the previous layer reaches capacity during a short circuit event. The first layer is the semiconductor device layer, which drives the actual current interruption. In many cases this layer will comprise of a network of devices in some series/parallel combination in order to meet all the design requirements of the circuit breaker. The remaining layers make up a network of transient energy absorbing components, depicted in Fig. 2.2 as an RC snubber in parallel with each half of the bidirectional switch block and an MOV in parallel with the entire switching component. The specific design for each of these layers is discussed in detail in section 2.4. Another important component is the inclusion of some minimum inductance, depicted in Fig. 2.2 as L_{min},

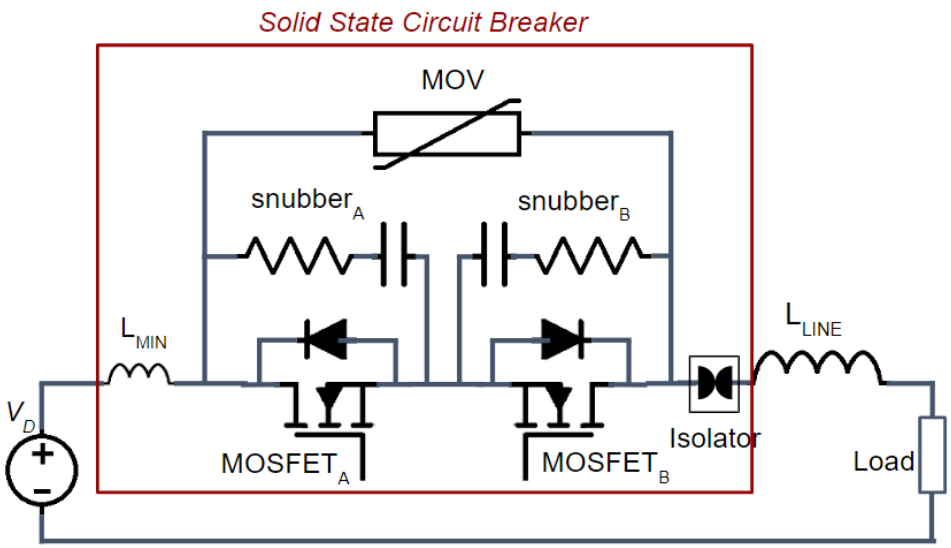


Figure 2.2 SSCB Topology

which serves to set a maximum di/dt the circuit breaker can safely respond to. L_{min}, can be evaluated as:

$$L_{min} = V_D \times \frac{t_{min}}{I_{sc,max}} \tag{2.1}$$

Where V_D is the system bus voltage, t_{min} is the minimum actuation time, and $I_{sc,max}$ is the maximum short circuit current. This inductance can be deliberately accounted for in the stray inductance of the SSCB module itself. Finally, many safety standards, such as IEEE C37.14 and IEEE C37.20, require secondary disconnect devices to provide physical isolation by the end of a circuit breaker actuation. Semiconductors devices, even when open, do not provide this physical isolation, therefore a secondary disconnect device must be added to the final SSCB topology.

2.2 SSCB Operating Modes

To properly define the design requirements of an SSCB, it is important to understand the circumstances of the different operating modes of the application. The operating mode that will occupy the majority of the operational lifetime is the on-state, i.e. conducting the

nominal rated current continuously. As a result, steady state conduction loss is a critical design characteristic, and one where the SSCB struggles the most to compete against mechanical breakers. This fact contrasts with switching converter applications where the switching losses are comparable, or even dominant over conduction losses.

The second operating mode is that of interrupting a short circuit current, i.e. actuation. In this mode the device must endure the short circuit current for the required delay time, then drive the current to zero and stand off the system bus voltage indefinitely. The magnitude of the short circuit current and reactive energy can vary greatly depending on the context of the system the SSCB is protecting, as well as the circumstances of a given fault itself. For the purposes of defining design characteristics it is helpful to define the worst case boundaries where the short circuit current and reactive energy are the highest. These boundaries will drive the design and are defined by short circuits in two cases denoted in Fig. 2.3.

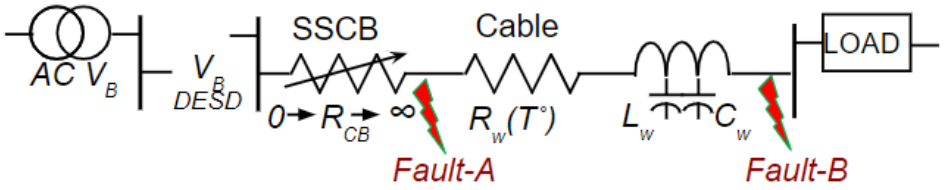


Figure 2.3 Worst Case Faults

Fault A represents a worst case, low impedance fault. Envision a circuit breaker connected essentially at the output bushings of a building transformer, or on the terminals of a Li-ion battery in an electric vehicle or other distributed energy storage device (DESD). There is very little resistance or inductance and a high capacitance that can support a very high di/dt. This condition produces the greatest thermal stress in the circuit breaker and requires that the circuit breaker actuate as fast as possible.

Fault B represents a highly inductive and capacitive fault current. Such a fault can occur anywhere in the protected system, however the worst case is represented by a fault at a

point in the system farthest from the source where the system inductance results in a low di/dt. This type of fault produces the largest reactive stress on the circuit breaker with a relatively smaller thermal stress. This case also requires that the circuit breaker delay before actuating, either to allow the fault to clear itself or for a circuit breaker closer to the fault to trip, in order to provide better selectivity and security through coordination. Therefore, this case is referred to as a "slow" trip.

The expected stress and resulting behavior of the circuit breaker is dependant on where a given fault falls between these two worst cases, which is generally inferred based on the magnitude of the short circuit current. The larger the short circuit, the "faster" the trip response necessary. Defining this behavior is discussed in the subsequent section.

2.3 Fuse Curve Characterization

The behavior of a circuit breaker in actuation mode is defined with a trip curve, also known as a fuse or i^2t curve; an example for a conventional circuit breaker is given in Fig. 2.4. This curve plots the total actuation time of the device against current and is typically plotted on a log-log scales on account of the wide range of current and time covered by the curve, particularly in high voltage systems. The trip curve can be subdivided into three regions, denoted on Fig. 2.4, based on the type of response. The first region denotes the slow over-current trip response with an inverse time relationship. The second region denotes the minimum dwell time required to prevent nuisance trips with currents exceeding the maximum rated short circuit current incurring a fast over-current response. The third region marks the current values the breaker must carry during its actuation process and is limited at it's maximum rated current for that time.

Because a circuit breaker's function is to protect a system in the event of a short circuit, it is imperative that the circuit breaker does not fail within its behavioral parameters. One of the primary threats to this condition is a thermal runaway condition brought about

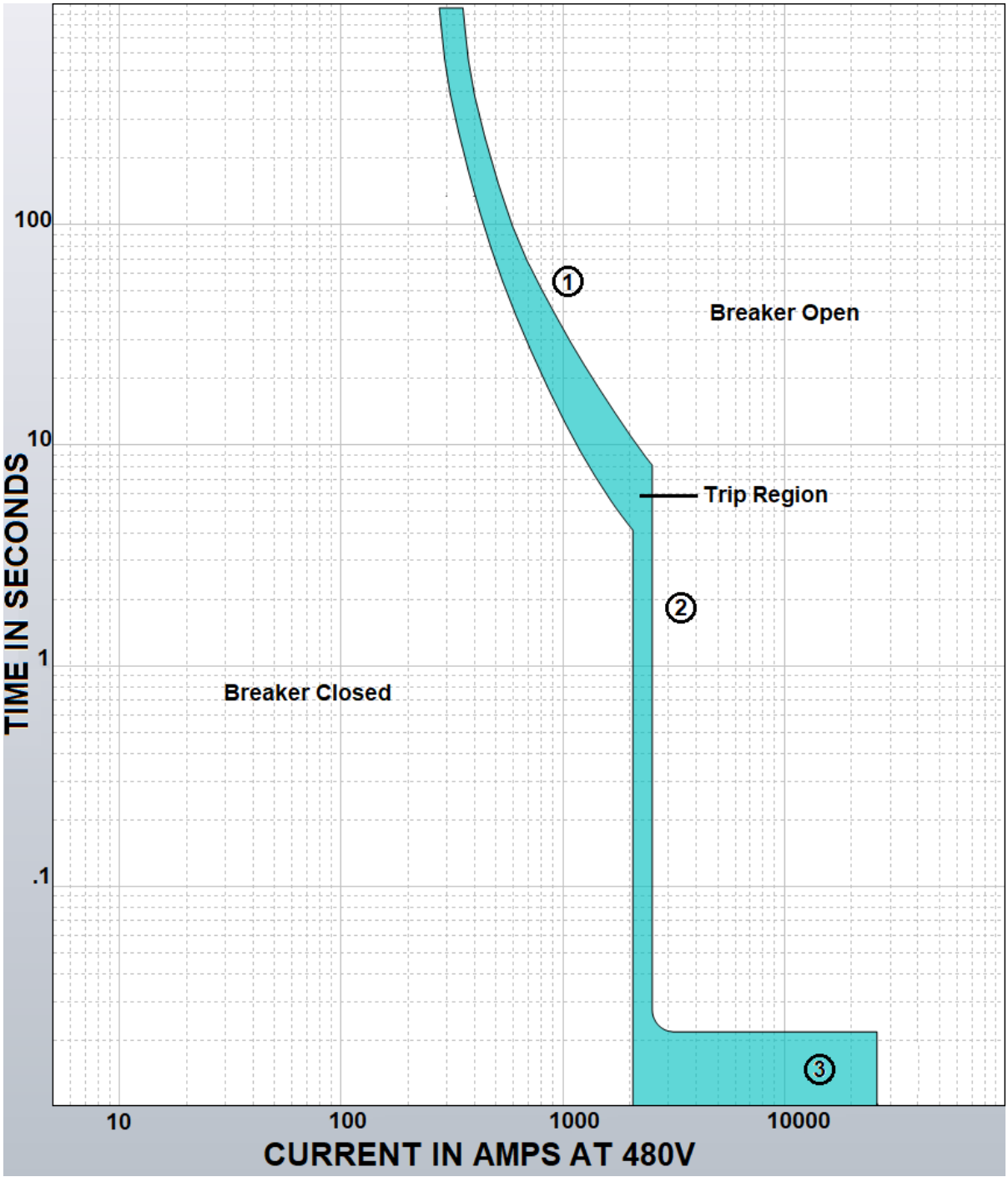


Figure 2.4 Example of a Typical Molded Case Circuit Breaker Trip Curve (extracted from [9])

by rapid joule heating in the devices during a short circuit event. In conventional protection devices, such as fuses and moulded case breakers, this heating effect, in part, drives successful operation of the device, therefore excluding device failure as a possibility. The physical design of the device itself defines it's behavior and the security of the device is consequentially ensured. In contrast, the actuation on an SSCB is controlled digitally by a gate drive circuit and controller, and therefore, the behavior of the device can be defined by the user. For conventional circuit breakers the fuse curve is a behavioral curve and a ratings curve by consequence, however, for an SSCB, the curve is strictly a ratings curve defining the safe operating area (SOA), with any behavior curve that fits within this SOA allowed.

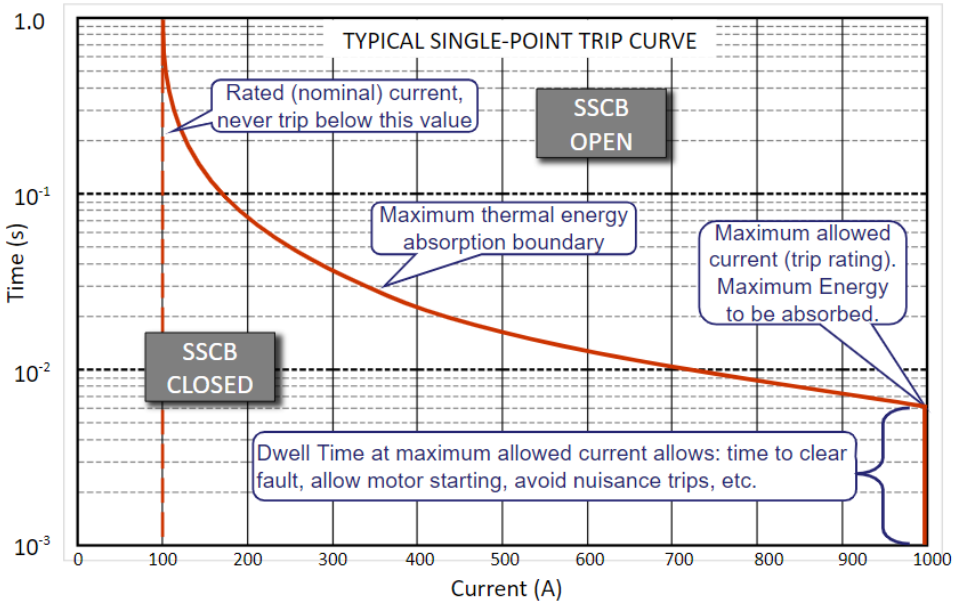


Figure 2.5 Example of SSCB Trip Curve

Semiconductor devices are susceptible to thermal runaway when $dR/dT < 0$ in voltage driven systems and when $dR/dT > 0$ in current driven systems. Assuming the short circuit current is provided by some source and the resistance of the SSCB is negligible compared to the system impedance, the circuit breaker is effectively a current driven system during a short. Therefore, SSCBs using semiconductor devices with a positive temperature coefficient are vulnerable to thermal runaway. To ensure that the SSCB does not fail, the SOA

of the SSCB must be defined to keep the devices within their own SOA. The resulting trip curve for an SSCB, illustrated in Fig. 2.5, plots the maximum amount of time the SSCB can sustain a given current before the devices within exceed their critical Junction temperature ($T_{j,c}$). This time is primarily dependant on the ambient temperature and physical power stage design. The intersection of the maximum rated short circuit current and minimum dwell time marks the point of maximum energy dissipation, labeled on Fig. 2.5. This design point drives the thermal design of the power stage, which is discussed in further detail in chapter 3.

2.3.1 Semiconductor Device Short Circuit Behavior

Recent literature has been published reporting the short circuit capability of WBG semiconductor devices, particularly SiC devices [8, 15, 32, 33, 46, 63]. Different devices are tested to failure and the measured power density is integrated over the duration of the test to calculate energy absorbed by the device during short circuit. This figure provides a means for quantitative comparison of short circuit ruggedness between different types of devices.

The differences in device ruggedness is a result of the saturation current, $I_{d,sat}$, behavior in each structure. For instance, in [33] the $I_{d,sat}$ behavior is compared between a commercially available SiC MOSFET and normally-off SiC JFET rated at 1200V/0.1 Ω on a 400V DC bus. The resulting short circuit behavior is presented in Fig. 2.6. $I_{d,sat}$ in the MOSFET is limited predominantly by the channel resistance, which has a negative temperature coefficient, allowing high initial currents. At higher temperatures, scattering mechanisms become dominant, reducing $I_{d,sat}$. In the JFET, $I_{d,sat}$ is only limited by the scattering mechanisms in the bulk region which has a positive temperature coefficient, and $I_{d,sat}$ was reduced by one order of magnitude within the first 200 µs. The MOSFET was reported to withstand 13.5 J cm^{-2} at $Vg = 15V$, while the JFET withstood 44.6 J cm^{-2}. The paper concludes that SiC JFETs may be better optimized for short circuit protection applications.

These results provide an argument for improved reliability in SSCBs using devices with

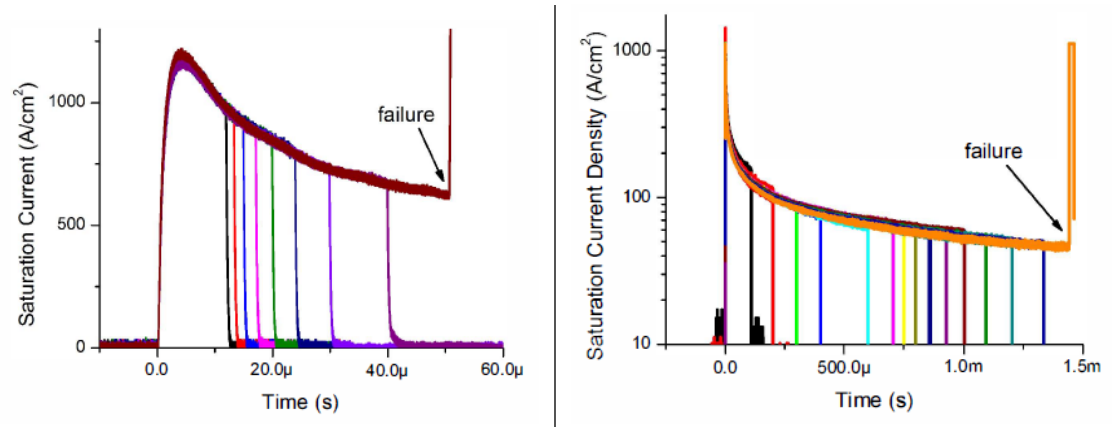


Figure 2.6 Short-circuit behavior in: (a) 12 kV MOSFET (b) 12 kV JFET [33]

greater short circuit ruggedness such as JFETs. However, a distinction should be made between semiconductor device short circuit capacity and the short circuit capacity of an SSCB. The device short circuit capacity discussed in [33] relies on the current limiting behavior of $I_{d,sat}$ as the devices reach high temperatures. As stated previously, to ensure the SSCB does not fail over multiple short circuit interruptions, the devices in the SSCB should not be stressed beyond $T_{j,c}$. Therefore, the short circuit capacity of the SSCB is dependant on current derating and the transient thermal absorption of the SSCB packaging, rather than the intrinsic short circuit capacity of the devices.

2.4 SSCB Design by Layer

During a short circuit interruption, the energy stored in the system inductance must be dissipated in the course of actuation resulting in a voltage overshoot at the terminals of the circuit breaker. In general semiconductor devices are fairly sensitive to over voltage and can only absorb a limited amount of energy in the bulk of the device. Therefore, additional components must be included in parallel with the semiconductor devices to provide layers of energy absorption. In addition, the thermal energy generated by the short circuit current must also be absorbed by the physical material of the SSCB. The thermal absorption takes

place predominantly in the device layer and packaging, the design of which is discussed in detail in chapter 3. As depicted in Fig. 2.7, the response rate of the energy absorption for each layer is traded with cost of material in order to optimize the response against cost. The design of the physical SSCB can be considered one layer at at time.

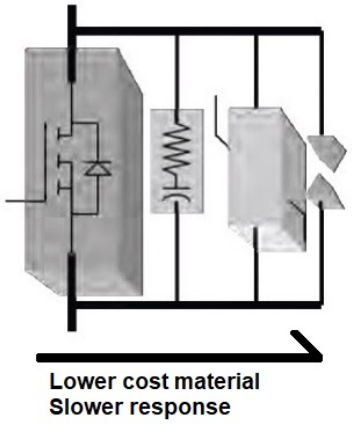


Figure 2.7 Layers of Energy Absorption in an SSCB

2.4.1 Semiconductor Device Layer

The semiconductor devices in the SSCB form the first layer of energy absorption as the electrodynamic change in the devices drive the current change. The capacitance within the devices capture a small amount of the energy from the system relative to the stored energy (worst case for Fault B). The primary role of the device layer is conducting the current during normal on-state and blocking the system voltage after actuation. During the blocking state the circuit breaker voltage rating will then be based on the system bus voltage plus some safety margin to account for voltage overshoot. The subsequent layers of the SSCB suppress the overshoot. However, it is still important to include a safety margin on the semiconductor devices to ensure security. The voltage requirement can be met either by a single component or by strings of components in series, which is discussed in Chapter 4.

The number of devices required in series for an SSCB is:

$$N_s = \frac{V_{bus}(1+X_s)}{V_{DS}} \tag{2.2}$$

where V_{bus} is the system voltage, V_{DS} is the blocking voltage of a selected device, and X_s is the percent safety margin. When forming strings of devices in series, the number of devices will need to be rounded up to the nearest integer, which often accounts for the safety margin. Thus, the resistance of a string of devices is:

$$R_s = N_s R_{DS(on)} \tag{2.3}$$

where $R_{DS(on)}$ is the on-state resistance of the device at the typical ambient temperature of the in-situ SSCB. As stated in Section 2.2, the $R_{DS(on)}$ is a critical characteristic for normal conduction, as this affects overall efficiency. Efficiency is defined as:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{in} - P_{loss}}{P_{in}} \tag{2.4}$$

In a SSCB, the power in is defined by:

$$P_{in} = V_{bus} I_{nom} \tag{2.5}$$

Where I_{nom} is the nominal current through the SSCB during normal conduction operation. The power loss is define by:

$$P_{loss} = I_{nom}^2 R_T \tag{2.6}$$

where R_T is the total resistance of the device layer in the SSCB. In order to support bidirectional current flow, a composite circuit of semiconductor switches will be needed in the absence of a truly bidirectional field effect transistor (FET). The simplest approach, illustrated in Fig. 2.2, is to use two identical switching units configured back to back, each with

anti-parallel diodes. There are other bidirectional arrangements, however this method produces the lowest part count in a system that can already require a large number of devices. During nominal conduction in either direction current will flow through one switching unit and the anti-parallel diode of the opposite switching unit. Therefore the total resistance of the device layer is defined as:

$$R_T = \frac{N_s R_{DS(on)}}{N_p} + R_D \tag{2.7}$$

where R_D is resistance of the anti-parallel diode, or network of diodes, in parallel with the reverse conducting half of the device layer. A conservative approximation can be made assuming that the diode resistance is equivalent to the resistance of the forward conducting network of devices, which simplifies equation (2.7) to:

$$R_T \approx 2\frac{(N_s R_{DS(on)})}{N_p} \tag{2.8}$$

Substituting equations (2.5), (2.6), (2.8), and (2.4) we get:

$$\eta = \frac{V_{bus} I_{nom} - \frac{2I_{nom}^2 N_s R_{DS(on)}}{N_p}}{V_{bus} I_{nom}} = 1 - \frac{2 I_{nom} N_s R_{DS(on)}}{V_{bus} N_p} \tag{2.9}$$

Solving for N_p we get:

$$N_p = \frac{2 I_{nom} N_s R_{DS(on)}}{V_{bus}(1-\eta)} \tag{2.10}$$

Reducing $R_{DS(on)}$ in this way increases the overall volume of semiconductor material used, which has the added benefit of providing more thermal mass for absorbing thermal energy during a short circuit event and more area for thermal spreading and dissipation after actuation. Enhanced thermal dissipation allows the devices in the SSCB to cool down to initial conditions faster, enabling shorter re-closing times.

For most SSCB designs, the efficiency requirement will be the dominant factor in determining necessary volume of semiconductor material. However, SSCB designs with a large maximum short circuit relative to nominal current or long dwell time may require

additional semiconductor material to mitigate excessive heat dissipation. Proposed is a rule of thumb; if the maximum short circuit current experienced by a single device in the SSCB is more than 1.5X the device rated current at high temperature, then the surge current requirements will dominate the design over the efficiency requirement. In this case additional design iteration may be needed, adding more semiconductors in parallel until the desired dwell time at maximum short circuit current is achieved.

2.4.2 Snubber Layer

The snubber layer is the fastest transient energy absorption layer. The snubber regulates the di/dt and dv/dt in the circuit and transfers power dissipation from the semiconductor devices to the snubbing resistor during the initial overshoot caused by actuation. Conservatively, the snubbing resistor must be sized to dissipate the total energy stored in the system inductance in the worst case and the peak dV/dt is proportional to the ratio of snubber capacitance to resistance. In this case the snubber capacitor will be:

$$C_s > \frac{(L_{line} + L_{min}) I_{sc,max}^2}{V_{bus}^2} \tag{2.11}$$

Where $I_{sc,max}$ is the maximum short circuit current. The accompanying snubber resistor will be:

$$R_s = \frac{V_{bus}}{I_{sc,max}} \tag{2.12}$$

2.4.3 MOV Layer

An MOV is a non-linear resistor that follows a power law relationship:

$$I_{MOV} = kV^{\alpha} \tag{2.13}$$

where k is a constant related to the geometric structure of the MOV and α is a constant dependant on the material properties proportional to the non-linearity in conduction. α values typically range from 5 to 20, resulting in characteristics similar to a TVS diode, clamping the voltage due to a decreasing resistance. The MOV should be selected so that the maximum varistor voltage (V_n) is greater than the supply voltage to avoid conduction through the MOV during normal operation of the SSCB, and the clamping voltage (V_c) is less than rated voltage of the devices used in the device layer to protect them from burning out.

The difference between V_n and V_c defined by the non-linearity of the MOV. This non-linearity is larger for MOVs with higher V_c. As a result, ensuring $V_n > V_{bus}$ for higher voltage SSCB designs requires that the device layer can tolerate larger dV/dt on account of the higher V_c. A solution to this problem can be found by including a high current switch in series with the MOV, such as a large Si IGBT illustrated in Fig. 2.8. In this case it is permitted for $V_n < V_{bus}$ resulting in some leakage through the MOV which would then be blocked by the switch. During actuation, switch would be turned on in time with the action of the snubber layer to allow for conduction through the MOV, completing the transient energy absorption.

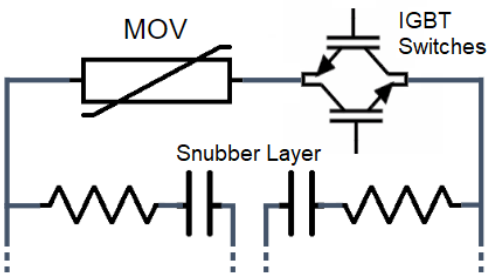


Figure 2.8 Bidirectional IGBT switching block in series with MOV

The MOV should be physically sized to dissipate the total energy in the system without failing to account for the limited life cycle of MOVs. The transition point between the snubber and MOV layers is dependant on the size of the snubber capacitor and the amount

of stray inductance on the parallel paths of each layer. This design point can be used to optimize the sizing of both the snubber resistor and MOV. This is reserved for future work.

Because an MOV is a variable resistor, there is an ample opportunity to integrate the MOV into the snubber circuit, shrinking the capacitance and further optimizing the proportion of material used within both layers. Complex snubber circuits with stages of MOV-C snubbers, such as the topologies presented in Fig. 2.9, may provide a hyper optimized energy absorption circuit. This presents a pathway for future work Similar to [39].

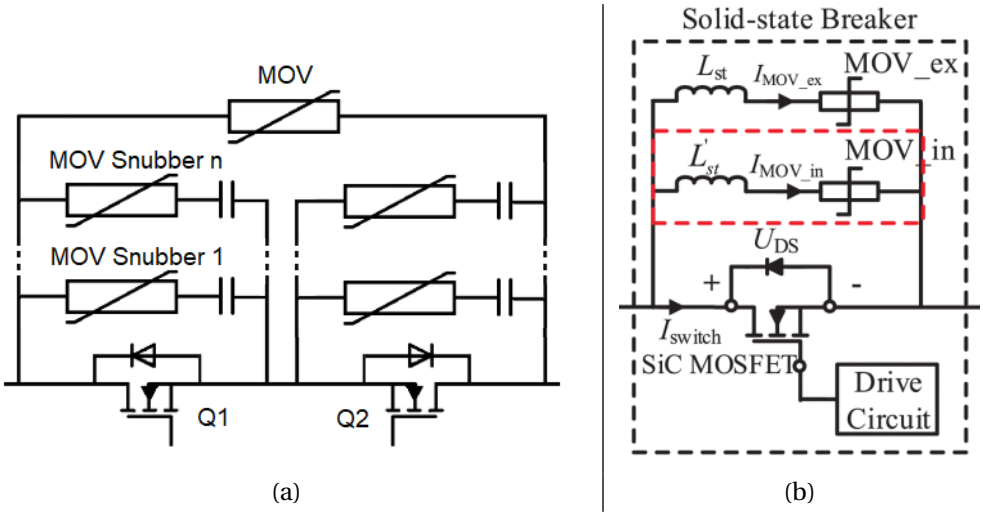


Figure 2.9 Staged MOV snubber configurations in an SSCB: (a) Multiple MOV RC snubbers in parallel with each switch (b) two MOV RL snubbers in parallel with the SSCB [39]

2.4.4 Fail-safe Layer

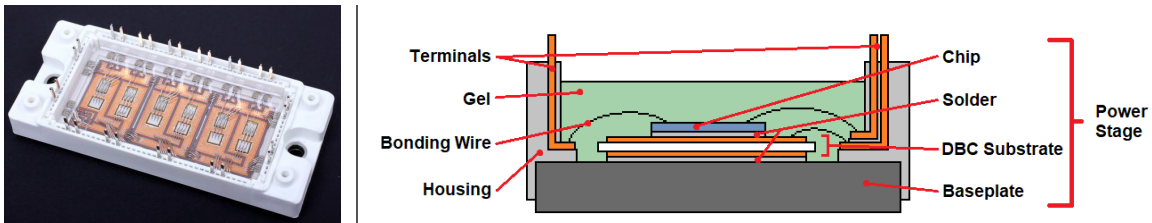
A fail safe layer is used to ensure that the system is protected should an excessive fault condition occur beyond the ratings of the SSCB. A simple fail-safe layer is a spark gap that breaks over should excessive voltage occur across the circuit breaker. In this case excessive current would pass to the next circuit breaker in coordination, which will be responsible for isolating the fault. An alternative fail-safe mechanism could be a fuse in series with the SSCB, however this method provides limits selectivity and coordination.

CHAPTER

3

POWER STAGE THERMAL DESIGN

For the purposes of this work, the power stage is defined as the portions of the power module packaging solution that include power semiconductor devices and supporting material, as illustrated in Fig. 3.1. First, devices are attached to a patterned ceramic substrate. Second, the substrate is mounted onto a metal baseplate. Finally, the structure is attached to a heat sink or heat exchanger. Attachment methods solder, sintered silver, and metal loaded epoxies. The power stage provides mechanical support and a thermal path for heat dissipation from the devices. For SSCB applications, the power stage must be designed, not only to dissipate nominal conductive thermal energy, but also transient thermal energy generated during a short circuit event. The temperature rise of the devices during a short circuit event will be determined by the ratio of thermal dissipation in the devices to the thermal absorption of the power stage. The temperature evolution for the worst case short



(a) (b)

Figure 3.1 (a) Sample Power Module with internals exposed and (b) illustration of components in power module assembly

circuit current will define the limit of the SSCB's ratings curve. Therefore, the area under the ratings curve can be expanded by maximizing the thermal capacity and minimizing the thermal impedance of the power stage.

3.1 Power Stage Thermal Behavior

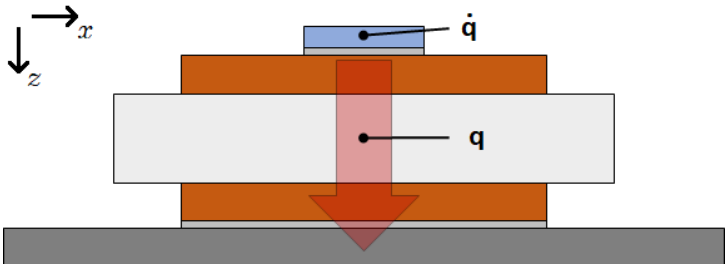


Figure 3.2 Thermal Model of Power stage

It is important to understand the thermal behavior of the power stage during the course of a short circuit event. The power stage can be modeled thermally as a composite wall structure of dissimilar materials with heat generated in a given device, $\dot{q}$, and flowing vertically towards the heat sink as a heat flux, q, as illustrated in Fig. 3.2.

The thermal generation in the device is described by:

$$\dot{q} = \frac{I_D^2 R_{DS,on}(T)}{V} \tag{3.1}$$

Where V is the volume of a given device in the SSCB, I_D is the current through the device and $R_{DS,on}(T)$ is the temperature dependant resistance of the device. The distinction should be made between the above values and the current through and resistance of the entire SSCB, I_{SSCB} and R_{on} respectively. The model assumes the surfaces other than the backside are adiabatic and any thermal generation other than from the device is negligible.

Assuming one dimensional heat transfer, the steady state overall heat transfer rate through the power stage is described by:

$$q = \frac{\Delta T}{\sum_1^n R_{th,n}} \tag{3.2}$$

where ΔT is the temperature differential across the structure, and $\sum_1^n R_{th,n}$ is the sum of thermal resistance for each layer in the structure. The thermal resistance of a given layer is:

$$R_{th} = \frac{L}{kA} \tag{3.3}$$

where k is the thermal conductivity of the material ($\mathrm{W\,m^{-1}\,K^{-1}}$), A is the effective cross-sectional area orthogonal to the heat flux, and L is the characteristic length of the material, the thickness in this case. A more in-depth explanation of this solution is provided in Appendix A.

By assuming the backside of the power stage is held constant at the ambient temperature, equation (3.2) can be used to determine the temperature rise of the device in steady state. A short circuit event introduces a step function to $\dot{q}$ with a corresponding temperature distribution response across the power stage in the z direction, $T(z,t)$. This temperature response is of interest for evaluating the maximum time, t_{max}, before the junction of the device reaches a critical temperature, $T_{j,c}$, defined by the manufacturer for safe operation. This t_{max} for corresponding short circuit currents defines the thermal limit of the SSCB.

Time dependant heat transfer through the power stage can be analyzed through two separate time regimes. The early regime assumes that all the thermal energy generated is

absorbed by the device alone and the quantity is dependant on $T(z,t)$ within. Evaluating t_{max} is simple as many analytical solutions for $T(z,t)$ exist. For instance, assuming a surface is exposed to a uniform, constant heat flux, $T(z,t)$ is described by:

$$T(z,t) = \frac{q''}{k}\left(\frac{\alpha t}{\pi}\right)^{1/2} exp\left(-\frac{z^2}{4\alpha t}\right) - \frac{q''}{k} z\ erfc\left[\frac{z}{2(\alpha t)^{1/2}}\right] + T_i \tag{3.4}$$

Where T_i is the initial temperature, q'' is the constant heat flux, and α is the material property thermal diffusivity ($m^2\,s^{-1}$). A system is determined to operate in the early regime if the Fourier number, F_o, is >> 1. The F_o is a dimensionless quantity that describes the ratio of heat conducted through a body to the heat stored within that body.

$$F_o = \frac{\alpha t}{L^2} \tag{3.5}$$

t is the time interval of the transient, α is thermal diffusivity, and L_c is the characteristic length of the body. It should be noted that, for calculating F_o for a given device in a SSCB, L_c will be the thickness for a device that generates heat near the surface, and half the thickness for a device that generates heat near the center of the body. This distinction is dependant on device structure. For a SSCB operating in the early regime, the power stage is unable to provide heat extraction during the short circuit event and can only extend t_{max} by reducing the steady state temperature rise per equation (3.2), which defines the initial condition for the thermal transient.

The late regime assumes that $T(z,t)$, across a given body has mostly settled and the temperature can be approximated as isothermal and can be analyzed with a lumped capacitance model. A thermal system can be assumed to operate in the late regime when $F_o > 1$ and the Biot number, $Bi << 1$. The Bi is a dimensionless quantity that describes the ratio of heat transfer through a body to that at the surface of the body:

$$Bi = \frac{hL_c}{k} \tag{3.6}$$

Where h is the surface heat transfer coefficient ($\mathrm{W\,m^{-2}}$), and k is the material thermal conductivity ($\mathrm{W\,m^{-1}\,K^{-1}}$).

Applying this case to a SSCB, it is assumed the device rises in temperature uniformly and the temperature rise of the device, $T(t)$, is directly proportional to the energy absorbed by the device:

$$\frac{dE}{dt} = mC_p\frac{dT}{dt} \tag{3.7}$$

where m is the mass of the device and C_p is the material property specific heat. The heat transfer rate into the rest of the power stage is equal to the difference of the power dissipation and energy absorption rate in the device.

$$Q = I^2R_{ON}(T) - mC_p\frac{\Delta T}{t} \tag{3.8}$$

In this case the power stage is able to actively participate in heat transfer during the thermal transient and can therefore extend t_{max} as compared to the early regime case. However, calculating $T(z,t)$ is far more complicated than the early regime case as the spacial boundary condition extends across dissimilar material regions. During the thermal transient, the heat flux through each layer is distinct based on the temperature distribution across each layer. While the heat flux into a layer is larger than the heat flux leaving it, heat accumulates, raising the temperature, which subsequently drives a larger heat flux into the next layer. The growth of the heat flux and corresponding thermal accumulation in each layer directly contributes to the evolution of the surface temperature of the device, $T(0,t)$. Additionally, the thermal generation is not constant. Per equation (3.1), $R_{DS,on}$ is temperature dependant. Therefore, a recursive relationship is formed between $T(0,t)$ and $\dot{q}$, where the evolution of $T(0,t)$ grows $\dot{q}$, which in turn drives the temperature evolution.

This heat transfer problem is explored in literature more generally as time dependant heat transfer through a composite wall structure of dissimilar materials. Exact solutions for the composite structure case have been presented that apply the method of separation of

variables to the heat conduction partial differential equation. However, to solve the resulting orthogonal expansion requires the computation of eigenvalues and corresponding eigen functions for each layer, which is described as a lengthy and difficult matter [6, 44, 59]. Furthermore, to compare the temperature evolution across variations in the composite structure for iterative design, the eigen values and functions would have to be recomputed for each structural variation.

An alternative approach to design can be found through the use of approximate thermal models and numerical solutions evaluated by simulation. These approaches are discussed further in the following section.

3.2 Transient Thermal Modeling of the Power Stage

Transient thermal models are built by approximating regions of material in the thermal system as electrical resistances and capacitances and arranging them in a network that is representative of the system being modeled. Therefore, electrical network analysis can be employed to solve for the temperature distribution in the system with temperature being analogous to electrical potential, and heat flux to current.

$$q = \frac{\Delta T}{R_{th}} \qquad \sim \qquad I = \frac{\Delta V}{R} \tag{3.9}$$

This analogy is sometimes referred to as the electro-thermal analogy. Such networks can be solved quickly which is conducive for rapid iterative design however the assumptions and approximations made concomitantly should be taken into consideration as well.

A more accurate solutions can be evaluated via a full numerical solution. For complex geometry a numerical solution can be developed using a finite differencing method (FDM) or finite element analysis (FEA). In both cases the geometry is subdivided into regular control units and the heat transfer and temperature distribution is calculated for each unit. Most modern simulators, such as Comsol and Ansys, use FEA and can solve for multiple

physics concurrently, hence multi-physics simulations. These software applications are very powerful but also expensive and resource intensive. Furthermore, care must be taken to ensure the boundary conditions for a given problem are defined appropriately. Recent work introduced a light weight, FDM modeling tool optimized for parametric comparison of heat transfer on simple geometries [7, 11].

3.2.1 Foster & Cauer Models

The thermal model most commonly used on datasheets for electronic component temperature rise is a thermal resistor network or "ladder network", of which there are two types: Foster and Cauer [34]. These models represent the total thermal impedance of a composite layer structure as a string of resistor capacitor pairs.

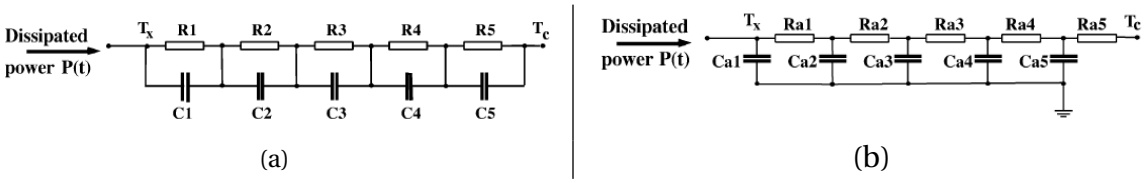


Figure 3.3 (a) Foster Model Network and (b) Cauer Model Network [23]

The Foster network, seen in Fig. 3.3(a), can be derived directly from the general heat transfer equation (A.1) and is commonly used for predicting temperature rise in packaged electronics due to it's mathematical simplicity. The transient thermal impedance can be represented as a sum of exponential terms:

$$Z(t) = \sum_{n=1}^{\infty} R_n(x)(1 - e^{-t/\tau_n}) \tag{3.10}$$

where the time constant, $\tau_n = R_n C_n$. Assuming a constant power, the temperature distribution is described by:

$$T(z,t) = P \sum_{n=1}^{\infty} R_n(x)(1 - e^{-t/\tau_n}) \tag{3.11}$$

For this model, the values of R_n and C_n have no direct physical meaning. It has been shown

that τ_i is identical to the inverse eigenvalues of the heat conduction equation [22, 23], however in practice they are found by fitting a known temperature response curve [34]. A minimum of four terms is required to accurately recreate a known curve [2]. If T_c is set to a constant ambient temperature, then T_x will reflect the temperature evolution at the surface of the composite structure assuming properly adjusted R_n, C_n values. Therefore, the temperature rise of the device can be predicted assuming the backside of the power stage is a constant temperature. It should be noted that if T_c does in fact vary with time the circuit loses its meaning. Per the model, a sudden increase in T_c would result in an equal and immediate increase in T_x when in reality this rise would occur gradually in line with the thermal capacitance of the material [23].

The Cauer Model network, Fig. 3.3(b), represents a rough discretization of the heat conduction equation for 1D heat flow with R_n and C_n representing the actual thermal resistance and capacitance of each layer in the system. Thermal resistance for a given layer can be calculated using (A.5) and thermal capacitance is calculated by:

$$C_{th} = m C_p \tag{3.12}$$

where m is mass and C_p is specific heat. This model is capable of working with a time varying T_c however the temperature evolution at $T_x(t)$ cannot be calculated using a simple expression as with the Foster model. Instead the temperature evolution can be simulated quickly with an equivalent spice model. The direct relationship this model has with the physical geometry enables rapid iterative design, however further refinement is needed to compensate for the accompanying approximation of uni-directional heat transfer.

3.2.2 FEA simulation

When performing FEA simulations care must be taken to properly define the boundary conditions and approximations to best represent the application. The initial conditions

of defining geometry and material properties are ubiquitous, however, careful attention must be taken when defining the mesh. As a rule, higher resolution is desired where the most change is expected. As the SSCB application involves a composite structure of thin layers with a heat source on the top face generating heat flow towards the bottom face, it is essential to have a high resolution along the vertical axis, as demonstrated in Fig. 3.4.

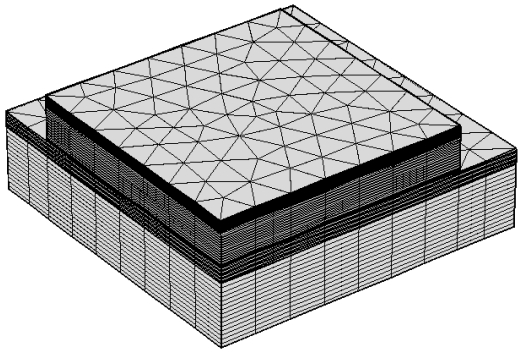


Figure 3.4 Sample mesh on quarter symmetry power stage with increasingly dense vertical resolution towards the top face

Care must also be taken in defining the heat source and sink. Simulators typically allow you to define thermal generation as either a body heat source or a surface heat flux. Most SSCB applications will result in a semi-infinite transient thermal case across the whole power stage for time delays up to millisecond range. In such a case the difference in temperature distribution across the device resulting from the different boundary types may be significant. At the same time if the device is evaluated to behave as a lumped capacitance, this difference may become negligible.

The heat source should approximate the nature of the heat generated by the device being modeled. This is determined by the internal structure of the device itself. For instance, in MOSFETs the majority of conduction losses tend to be generated in the channel region which is a thin region along the top face of the device. JFETs, on the other hand don't have a channel and the majority of their conduction losses are generated over the bulk of the device with a slight bias towards the top half. Therefore, the heat generated in MOSFETs is

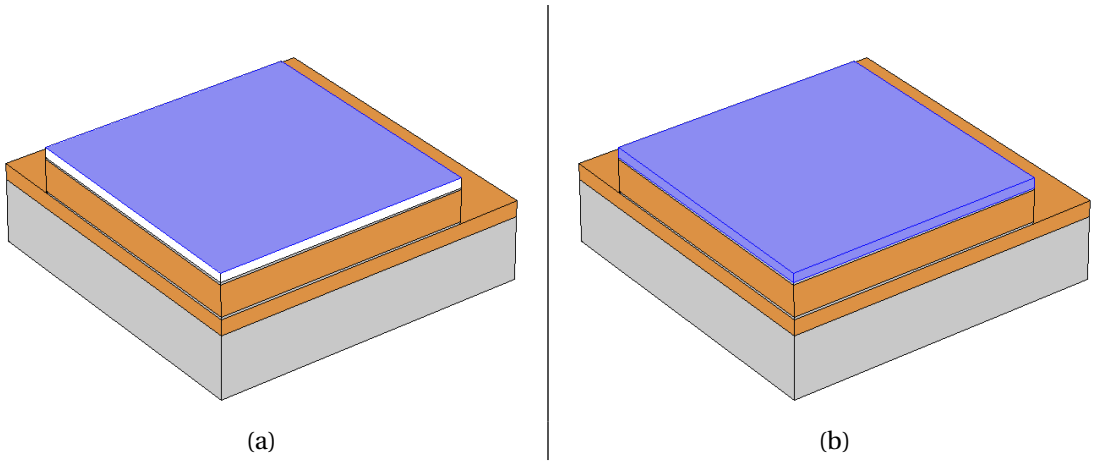


Figure 3.5 Sample quarter symmetry power stage with (a) Surface Heat Flux or (b) Body Heat Source

best approximated with a surface heat flux and a body heat source for JFETs, as illustrated in Fig. 3.5.

The thermal generation can also be simulated by incorporating a joule heating module into the simulator. The joule heating modules simulate heat generated by current moving through a material based on it's bulk resistivity. In the case of the device, the joule heating is based on the temperature dependant on-state resistance, $R_{DS,on}(T)$, as opposed to the bulk resistivity of the material. Therefore, a custom resistivity profile should be used for the device material that models the device resistance temperature dependence to compensate. Some multi-physics simulators allow for incorporating an analytic function which enables a somewhat simpler solution. Most devices will include a plot of $R_{DS,on}\,vs\,T$ which can be curve fit, as shown in Fig. 3.6, and the resulting function can be incorporated into the heat source definition to modulate the simulated heat flux with respect to surface temperature.

For a heat sink the user can define a constant temperature boundary or overall heat transfer coefficient on the back side surface. Here again, in the early regime case the difference is negligible, and defining a small heat transfer coefficient proportional to natural convection can ensure a conservative result.

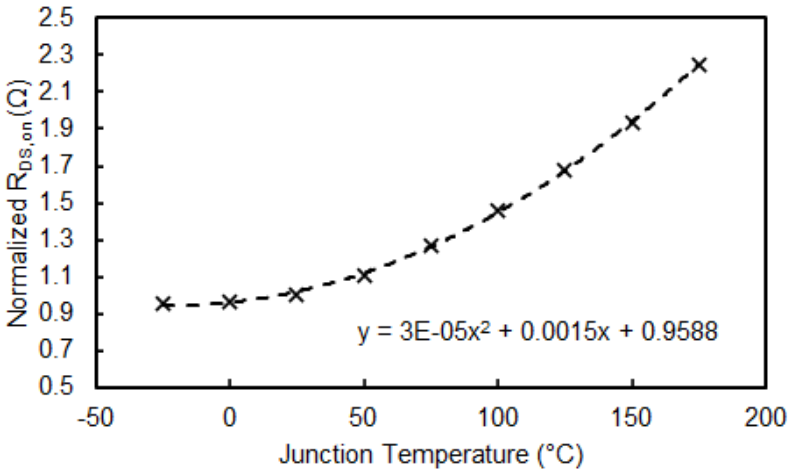


Figure 3.6 Sample normalized $R_{DS,on}(T)$ data points with fit curve and accompanying expression

3.3 Averaging Power Dissipation

Despite the approximation of 1D heat flow, the Cauer model can enable the rapid development of an initial design that can then later be refined through FEA and iterative design. The challenge is that the power dissipation in a SSCB is not constant due to $R_{DS,on}(T)$. Therefore, an approximation for $R_{DS,on}(T)$ is needed to develop an initial design.

This may be possible by leveraging the application boundaries of the problem:

- Only the temperature evolution in response to a current step function of the maximum magnitude is of interest.
- Only the temperature increase between the steady state temperature ($T_{j,ss}$) and the critical junction temperature ($T_{j,c}$) of the device is of interest. Once $T_{j,c}$ is reached the SSCB operates and current is interrupted.
- The $R_{DS,on}(T)$ will follow the same excursion with respect to temperature, and only the temperature evolution will affect the timing of that excursion.
- The temperature evolution is dependant on the composition and geometry of the power stage. Due to engineering limitation, power stages will have similar elements

and geometries, i.e. a dielectric layer thick enough to provide adequate passivation, equally thick top and bottom conductor pads to mitigate thermal stresses, etc, resulting in some degree of similarity in temperature evolution across different structures.

- The temperature evolution will be more strongly dependant on current than $R_{DS,on}(T)$ due to the squared relationship with power dissipation.

Under these conditions, the temperature evolution should fall within a similar family of curves with a slope dependant on the ratio of current relative to device rated current, I_D. The larger the ratio, the faster $R_{DS,on}(T)$ makes its excursion, and the less variation in average dissipation of the power-stage.

Table 3.1 Material thickness and properties of simulated 8mm x 8mm, 10kV power stage comparison

Alumina DBC with Cu Foil

Layer	Thickness (mm)	C_p ($\mathrm{J\,kg^{-1}}$)	ρ ($\mathrm{kg\,m^{-3}}$)	k ($\mathrm{W\,m^{-1}\,K^{-1}}$)
SiC	0.15	1200	3200	450
Ag Sinter	0.035	235	10500	175
Cu pad	0.04	385	8700	400
Alumina	0.508	900	3900	27
Cu pad	0.04	385	8700	400
Ag Sinter	0.035	235	10500	175
AlSiC	2	741	3010	180

ERCD with Cu Foil

Layer	Thickness (mm)	C_p ($\mathrm{J\,kg^{-1}}$)	ρ ($\mathrm{kg\,m^{-3}}$)	k ($\mathrm{W\,m^{-1}\,K^{-1}}$)
SiC	0.15	1200	3200	450
Ag Sinter	0.035	235	10500	175
Cu pad	0.04	385	8700	400
ERCD	0.24	901	3900	8
Cu pad	0.04	385	8700	400
Ag Sinter	0.035	235	10500	175
AlSiC	2	741	3010	180

Alumina DBC with 8mil Cu Pad

Layer	Thickness (mm)	C_p ($\mathrm{J\,kg^{-1}}$)	ρ ($\mathrm{kg\,m^{-3}}$)	k ($\mathrm{W\,m^{-1}\,K^{-1}}$)
SiC	0.15	1200	3200	450
Ag Sinter	0.035	235	10500	175
Cu pad	0.127	385	8700	400
Alumina	0.508	900	3900	27
Cu pad	0.127	385	8700	400
Ag Sinter	0.035	235	10500	175
AlSiC	2	741	3010	180

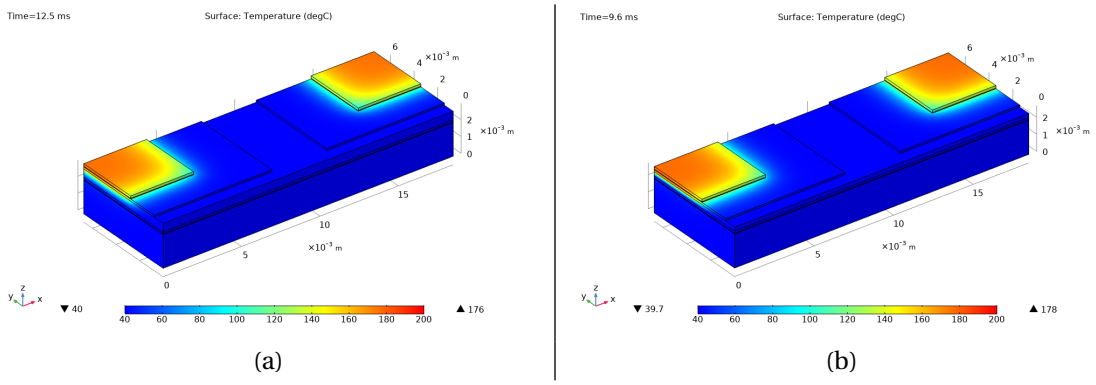
ERCD with 8mil Cu Pad

Layer	Thickness (mm)	C_p ($\mathrm{J\,kg^{-1}}$)	ρ ($\mathrm{kg\,m^{-3}}$)	k ($\mathrm{W\,m^{-1}\,K^{-1}}$)
SiC	0.15	1200	3200	450
Ag Sinter	0.035	235	10500	175
Cu pad	0.127	385	8700	400
ERCD	0.24	901	3900	8
Cu pad	0.127	385	8700	400
Ag Sinter	0.035	235	10500	175
AlSiC	2	741	3010	180

This phenomenon is demonstrated in a suite of FEA simulations that were performed to better understand the evolution of $R_{DS,on}(T)$ during a short circuit pulse on a variety of power stages designed for 10kV passivation. The simulations produce an accurate surface temperature evolution on an 8mm x 8mm, 1.7kV SiC JFET (UJ3N17005) rated for 200 Amps

for current steps of varying magnitudes. Based on the temperature evolution for each step, $R_{DS,on}(T)$ is integrated with respect to time and used to compute an average, $\overline{R_{DS,on}}$.

The power stages that were examined compare a traditional ceramic dielectric, alumina, to an epoxy resin composite dielectric material (ERCD), with two different copper trace thicknesses. The material properties and dimensions for simulation simulated are presented in Table 3.1.



(a) (b)

Figure 3.7 Surface temperature distribution 400A fuse circuit for simulated (a) DBC power stage structure and (b) ERCD power stage structure

These structures were simulated in Comsol Multiphysics, using the approach described in Section 3.2.2, including modulating the heat source based on the extracted $R_{DS,on}(T)$ curve for the selected device. The resulting surface plots for a 400A fuse current are shown in Fig. 3.7 and the evaluated $\overline{R_{DS,on}}$ for each structure at different currents is presented in Table 3.2.

Table 3.2 $\overline{R_{DS,on}}$ Results for 1.7kV SiC JFET power stage structures

	DBC Substrate, 40um Cu			ERCD Substrate, 40um Cu			DBC Substrate, 8mm Cu			ERCD Substrate, 8mm Cu		
Current (A)	Fuse Time (ms)	$\overline{R_{ON}}$ (mΩ)	Energy (J)	Fuse Time (ms)	$\overline{R_{ON}}$ (mΩ)	Energy (J)	Fuse Time (ms)	$\overline{R_{ON}}$ (mΩ)	Energy (J)	Fuse Time (ms)	$\overline{R_{ON}}$ (mΩ)	Energy (J)
175	197.4	9.3	54.97	82.2	9.2	21.91	273.6	9.4	77.51	125.8	9.3	34.58
200	101.6	9.2	36.14	47.8	8.9	15.77	135.5	9.3	49.16	67.1	9	22.91
225	61.3	9	26.68	32.4	8.7	13.02	78.2	9.1	34.78	43.6	8.8	18.17
250	41.5	8.9	21.83	23.9	8.7	11.75	51.4	8.9	27.34	31.4	8.7	15.82
275	30.2	8.8	18.85	18.5	8.6	10.78	36.9	8.8	23.31	24.0	8.6	14.36
300	23.2	8.8	17.12	14.8	8.6	10.21	28.0	8.8	20.93	18.2	8.6	13.61
325	18.3	8.7	15.57	12.2	8.6	9.83	22.1	8.7	19.06	15.7	8.6	13.01

The fuse time is defined as the time it takes for the device to reach $T_{j,c}$. The energy absorbed is an estimation of how much energy the power stage absorbs during the fuse time, calculated as the difference between the average power dissipated and the energy absorbed by the device. The device can be assumed to behave as a lumped capacitance due to its material and thickness per the discussion in Section 3.1. Therefore, the device will absorb energy equal to:

$$E = mC_p\Delta T \tag{3.13}$$

where m is the mass of the device. For an 8mm x 8mm x 150um SiC device heated from an initial temperature of 40 °C to a $T_{j,c}$ of 175 °C, the energy absorbed in the device is 1.25 J.

As can be seen in Table 3.2, the $\overline{R_{DS,on}}$ does converge with increasing current as expected, and varies little across structures for currents near or beyond the rated current. An approximate $\overline{R_{DS,on}}$ scaling function is proposed based on the simulated results by plotting $\overline{R_{DS,on}}$ against the ratio I_{max}/I_D, as seen on Fig. 3.8

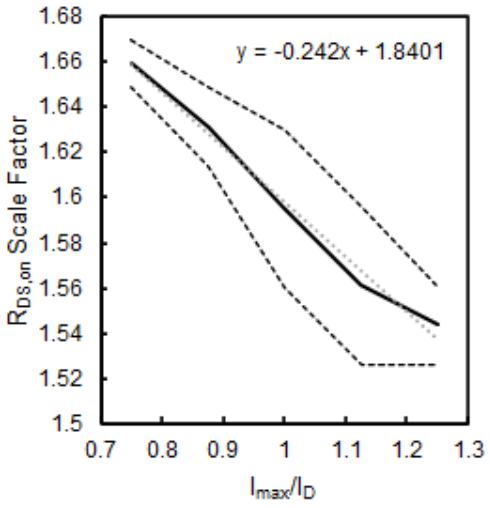


Figure 3.8 $\overline{R_{DS,on}}$ scaling function for 1.7kV SiC JFET

This scaling function can be used to calculate an approximate average power dissipation in an SSCB using 1.7kV SiC JFETs by:

$$\sim \overline{P} = R_{DS,on}(T = 25)(-0.242\frac{I_{max}}{I_D} + 1.84) \tag{3.14}$$

The approximate power dissipation can be input to a preliminary Cauer model representing the layers of the power stage to create an informed starting point for design. The values for R_n and C_n can be modified until the desired temperature evolution is achieved. This preliminary design can then be iterated further using FEA to create a SSCB power stage design that ensures the desired ratings curve.

It should be noted that these simulations assume a constant current regardless of how large when in reality the device would enter current limiting mode for $I >> I_D$. Therefore, deriving this scaling factor is only valid for ratios of I_{max}/I_D where the devices are not in current limiting mode, which is a prerequisite for SSCB design per Section 2.3

This analysis can be extended to derive $\overline{R_{ON}}$ scaling functions for other families of devices. Comparing functions across families of devices may reveal further similarities. This analysis is reserved for future work.

3.4 Trade-offs in Maximizing Thermal Capacity

Increasing the volume of certain layers in the power stage creates more heat storage capacity which can increase the amount of time it takes for the device to reach $T_{j,c}$. However there are some design trade-offs to consider.

The thickness of thermally conductive layers like the copper pads on either side of the dielectric can be varied, or additional copper can even be added beneath the device. Any material added in the heat path adds to the thermal impedance of the power stage once adequate thermal spreading has occurred. With greater thermal impedance, the steady state operating temperature of the breaker will be higher, which in turn shortens the time of excursion possible during a short circuit event and reduces the overall heat storage capacity. Therefore, it is important to include a steady state thermal simulation with each design

iteration to accurately define the initial temperature for each transient thermal simulation.

Material selection can also play a part in increasing heat storage capacity at a trade-off against cost. For instance, the high thermal conductivity and specific heat of SiC makes it an excellent heat reservoir but the material comes at a premium. However, one of the final steps in vertical power device fabrication is to thin the wafer to reduce the bulk resistance of each device. A simple way to add heat storage is to skip this wafer thinning step. while this would increase $R_{DS,on}$ of the SSCB, the active area of the device can be increased to compensate. Note that the wafer yield may be reduced increasing cost per device.

Increasing the area of layers allows for an increase in heat storage capacity without increasing vertical thermal resistance. The device area in particular has a strong positive impact on heat storage capacity as it results in a proportional increase in capacity at every layer in the power stage. The impact can be seen clearly in the simulation results presented in Fig. 3.9.

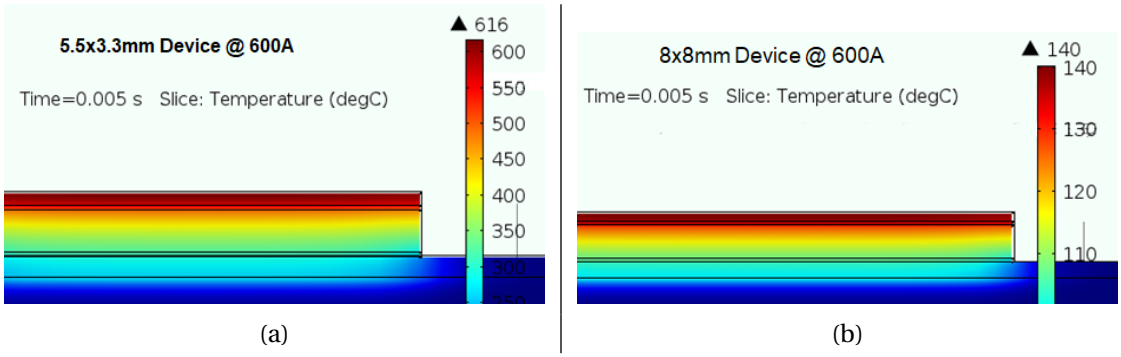


Figure 3.9 Comparison of Temperature Rise for 600A Short Circuit Current in (a) 5.5x3.3mm Device vs (b) 8x8mm Device

The temperature rise after a 600A short circuit sustained for 5 ms is simulated in a 5.5mm x 3.3mm and 8mm square device respectively. The devices were simulated with the same specific on-state resistance, $R_{on,sp}$, and $R_{DS,on}(T)$ behavior. The increased device area of the 8mm square device experienced a temperature rise nearly 500 °C lower than the 5.5mm x 3.3mm device.

CHAPTER

4

SCPM BASED SSCB PROOF OF CONCEPT

4.1 SCPM Topology

In recent literature, a power module topology capable of scaling to medium voltage with ≤50 ns switching rise and fall times has been proposed [18–20]. The topology, seen in Fig. 4.1 is comprised of a series of normally-on JFETs and a low voltage MOSFET forming a switching unit that exhibits normally-off behavior. The fast switching performance is reliant on a dynamic balance network that enforces charge balance across the JFETs [5].

From [18], the SCPM topology turns off by turning off Q7, which raises the source potential of Q6 relative to the gate, driving Q6 to pinch-off. The source potential of Q5 is subsequently raised, driving pinch-off in Q5. This pinch-off process propagates through to Q1, completing the turn off process. The turn on process works similarly. The Q7 is turned

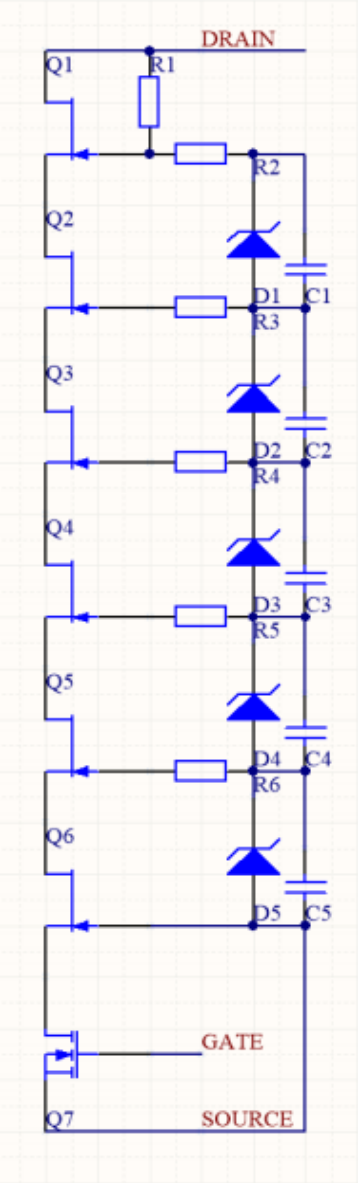


Figure 4.1 Proposed single SCPM Topology [20]

on, reducing the source potential of Q6 to the same as the gate, turning it on and reducing the source potential of Q5. This process continues until all JFETs are turned on. The balance circuit has two parts: (1) the static voltage balance is set by D1-D5 with R1 providing the bias current, and (2) the dynamic voltage balance is set by C1-C5 and R2-R6, which sets the rise/fall times of the SCPM. The capacitance of C1-C5 is based on the difference of the gate charge of Q1-Q5 and the body charge of D1-D5. An extension of the topology includes resistors in series with D1-D6 to divert avalanche current to the JFETs and improve the overall avalanche ruggedness of the module [19].

The SCPM topology is an attractive choice for the breaking element of an SSCB for a number of reasons. The topology enables the fabrication of medium voltage switching modules built from commercially available lower voltage (1.2kV-3.3kV) power devices, reducing cost. The short rise and fall times promises sub microsecond switching action between sensing and actuation. Distributed power dissipation over multiple devices facilitates heat extraction via thermal spreading. A single JFET device failure does not compromise the entire module as JFETs typically fail short, improving reliability. Lastly, [20] indicates the possibility of building a cascode out of SCPM modules to scale up to the tens of kVs, which would make SSCBs competitive with Hybrid CBs. The topology has drawbacks to consider. The SCPM module tends to heat unevenly during switching due to charge flowing from the highest JFET through the rest of the string and dissipating more heat through the lower JFETs. Additionally, the balance network creates an additional leakage path in the off state. However, since a SSCB spends the majority of time operating in the on state, these factors are less of a concern compared to other power electronic applications.

4.2 SCPM Short Circuit Actuation Demonstration

A prototype SCPM module was fabricated from commercially available packaged JFETs to validate the feasibility of the SCPM topology as the breaking element for SSCBs. The

Table 4.1 Prototype SCPM Component Values

Component	Value
C1	68 pF
C2	136 pF
C3	214 pF (68x3)
C4	282 pF (100+180)
C5	340 pF (180x2)
R1	4 MΩ high voltage
RG1-5	10 Ω High Surge Capacity
RA1-5	10 kΩ
D1-D5	AU1PK Avalanche Diode

prototype is composed of six 1.2 kV/80 mΩ normally-on SiC JFETs (UJN1208K) controlled by a 25 V Si MOSFET (BSZ018NE2LSIATMA1) following the avalanche-rugged topology shown in Fig. 4.2. 6 kV/10A prototype modules were construed using the component values shown in Table 4.1; the physical prototype is shown in Fig. 4.3.

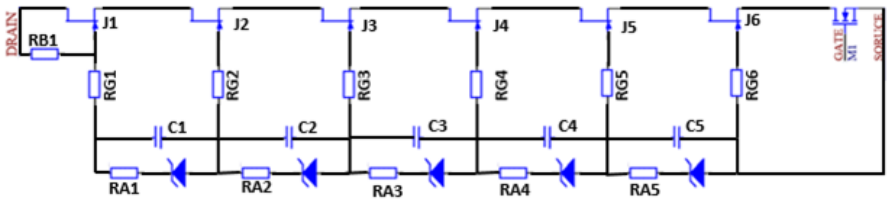


Figure 4.2 Avalanche Rugged SCPM Topology [19]

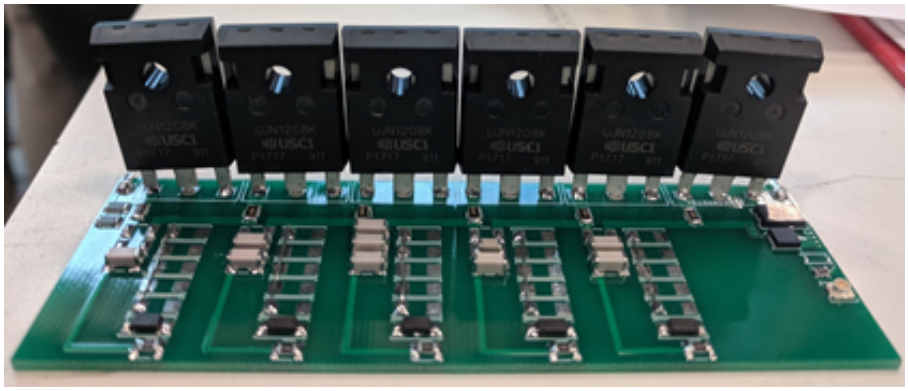


Figure 4.3 SCPM Prototype

Over-current tests were performed for 1 µs short circuit duration across a DC bus up to 3.5 kV with a 50 Ω load resulting in a 70 A fault current (7X rated current) using the test

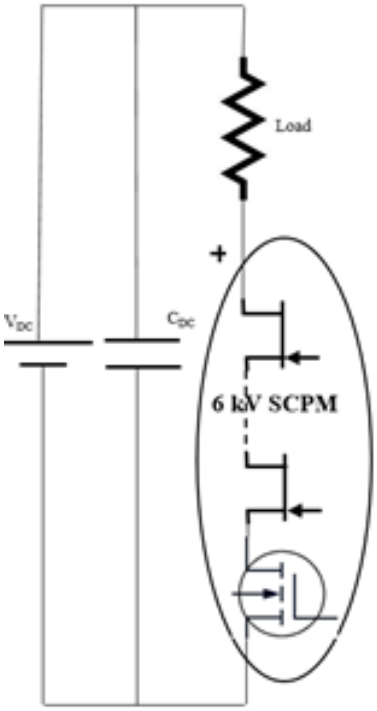


Figure 4.4 Test circuit for over-current test

circuit shown in Fig. 4.4.

Short circuit tests were performed for the same duration as a dead fault across a DC bus up to 2 kV. An optically isolated gate driver operating between 0-10 V was used to provide sufficient voltage isolation to the power devices. The results of the over-current test, Fig. 4.5, demonstrate that the SCPM topology is capable of 7X over-current interruption in approximately 100 ns. There is no indication of current saturation during the 1 µs over-current and, as a result of actuation, there is a 5.7 kV overshoot that would normally be mitigated by snubber and MOV components. Current interruption was also successful in the dead fault short-circuit test. However, at 1 kV there was indication of current saturation and at 2 kV oscillations began to occur from the gate drive despite the optical isolation, seen in Fig. 4.6 and Fig. 4.7 respectively. Despite the oscillation, the SSCB was still controllable as the current is eventually brought back to zero.

The results demonstrate that the SCPM topology using commercially available SiC JFETs

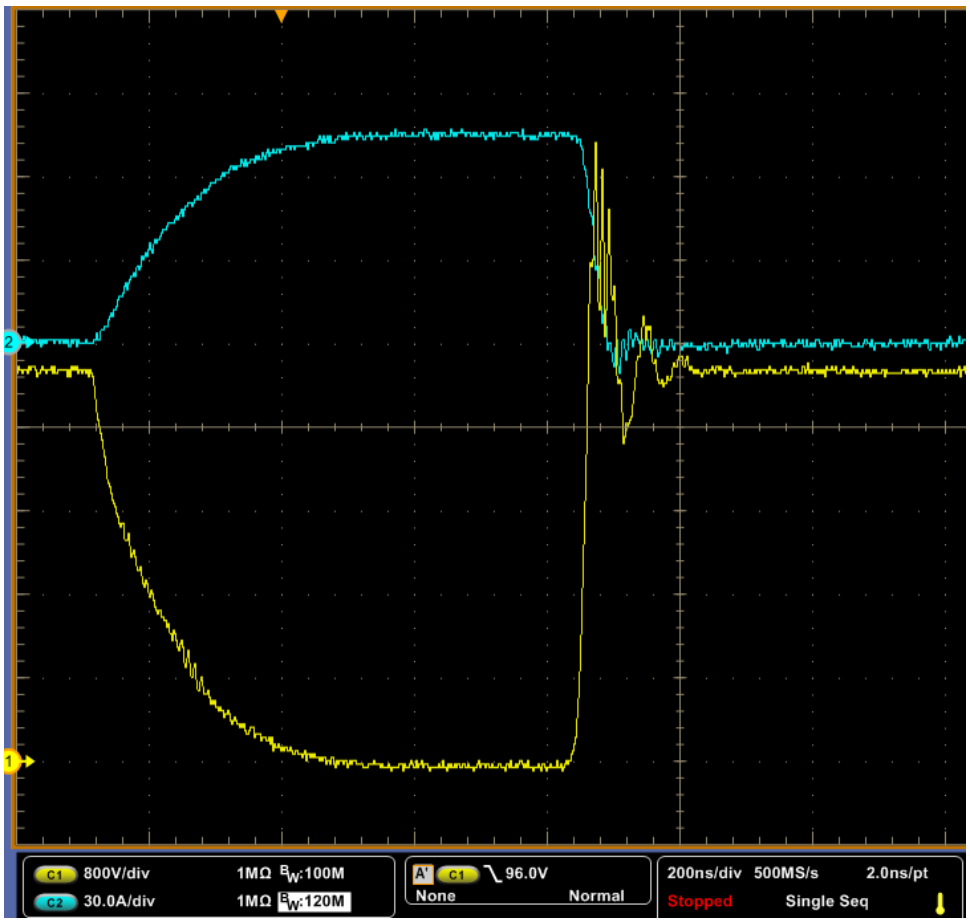


Figure 4.5 3.5 kV Over-current Test with Voltage in yellow (800V/div) Current in blue (30A/div)

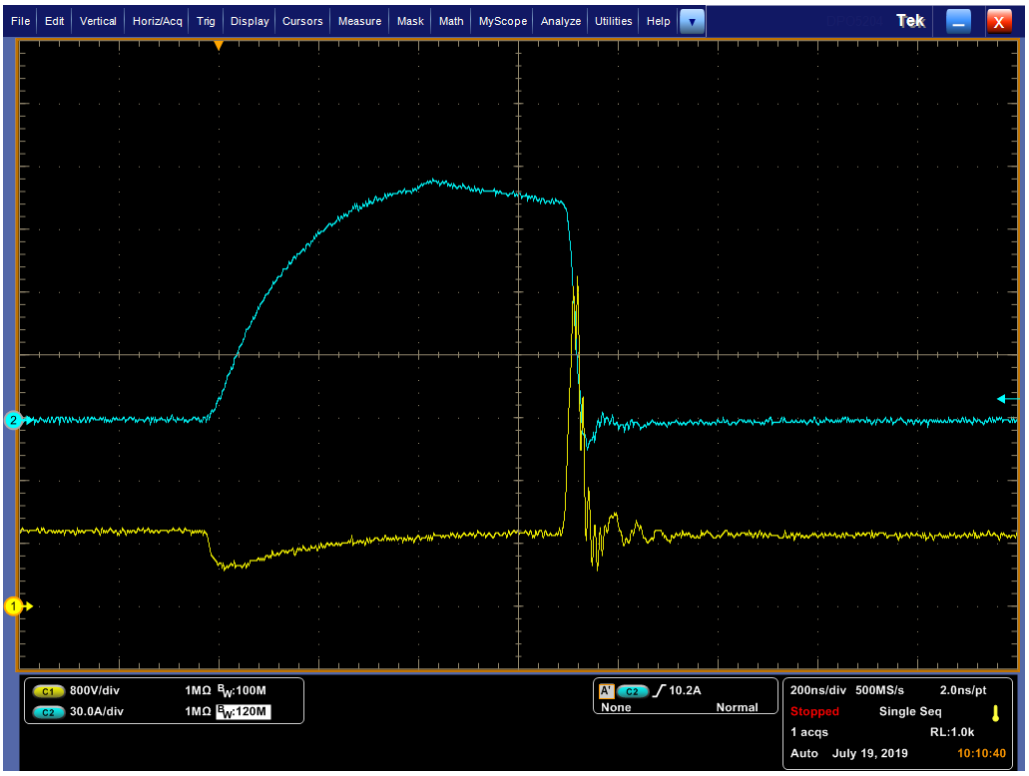


Figure 4.6 1 kV Short-circuit Test with Voltage in yellow (800V/div) Current in blue (30A/div)

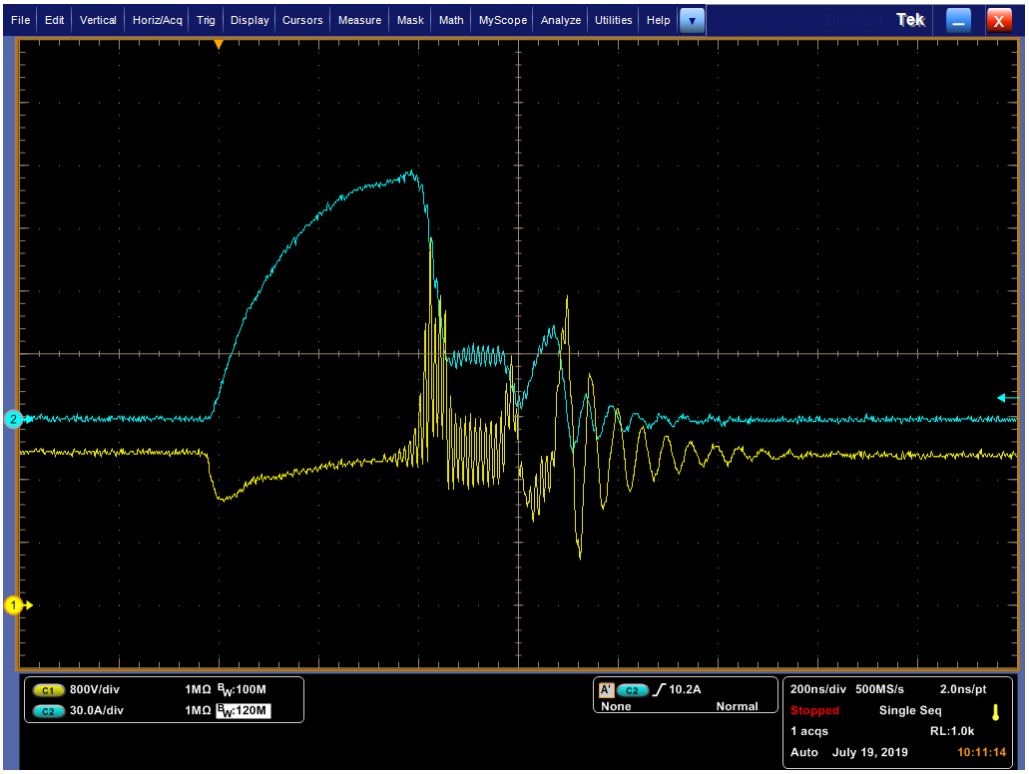


Figure 4.7 2 kV Short-circuit Test with Voltage in yellow (800V/div) Current in blue (30A/div)

is capable of withstanding a 7X over-current for 1 µs and then successfully interrupting the current in 60 ns. In particular, the avalanche balancing network is capable of maintaining sequential switching despite the high di/dt and dv/dt. The results also underscore the challenge of gate drive isolation in the medium voltage range.

4.3 Module Design

The design for a 10 kV/100 A SSCB design using SCPM breaking elements is presented targeting the specifications presented in Table 4.2 for comparison to EasyPact EXE, MV-AC 3Ø vacuum circuit breaker rated for 12 kV/ 630 A.

Table 4.2 Design Specifications for Example SCPM SSCB

Category	Design Target
Rated Voltage	10 kV/100 A/10X
Power	10 MW Steady State
Efficiency	>99.96%
Response Time	10X Dwell >5 ms Instant Trip <250 ns
Power Density	10 kV/10X: 2.76 GW m^{-3}
Cooling	70 °C Ambient
Lifetime	≤ 30000 cycles & 30 Yrs
Nuisance Trip	<0.1% , Digitally Adjustable

The JFET selected for the SCPM based SSCB is the USCi - UJ3N17005 which is rated for $V_{DS} = 1.7kV$, $I_D = 204$A, with an $R_{DS,on}$=6 mΩ at 70 °C. Applying a 70% voltage safety margin to account for overshoot during turn off, the number of devices needed in series, N_S, is calculated from equation 2.2 to be 10. Entering this value along with the system efficiency value from Table 4.2 into equation 2.9 (for the back to back bidirectional approach), N_P is calculated to be 3.

The snubber layer is designed assuming the SSCB is intended for a Data Center application with average cabling of 50 ft from source and 50 ft from load, representing a total system inductance of 24 µH. Factoring this into equations 2.10 and 2.11, $R_s = 10\Omega$ and $C_S > 125$nF. A Kanthal Globar 5 Series 503As resistor is selected, rated for 50 Ω, peak impulse of 50 A,

and 16 kV. Connecting 5 resistors in parallel ensures capacity for trip currents up to 1000 A. Two capacitor solutions were explored; 4x2 KEMET film C4BSYBX3820Z for 12 kV and 1742 A vs. 20x40 KEMET ceramic C3640C884MCGLC for 10 kV and 1130 A. The two solutions trade volume against cost, the analysis is presented in Table 4.3.

Table 4.3 Prototype SCPM Snubber Capacitor Comparison

Capacitor	Film	Ceramic
Cost per Capacitor	$10.08	$1.08
Number of Capacitors	8	1488
Cost (per SSCB)	$80.64	$1607.04
Volume	805 000 mm^3	349 048 mm^3

To meet design specifications the MOV layer, with $V_N > 10kV$ and $V_c > 16.5kV$, is required. The Stackpole Electronics ZOV680K23 high energy varistor is selected and volumetrically scaled to estimate total size. The final SSCB design is presented in Fig. 4.8 and size comparison to the EasyPact EXE is presented in Fig. 4.9.

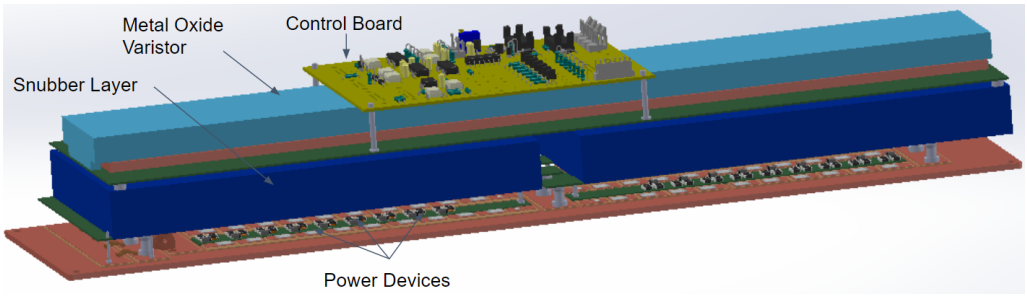


Figure 4.8 SCPM based SSCB Conceptual Drawing

The proposed design provides comparable voltage and current ratings to the Easypact EXE with the fast current interruption of the SCPM topology at a smaller volume and greater power density.

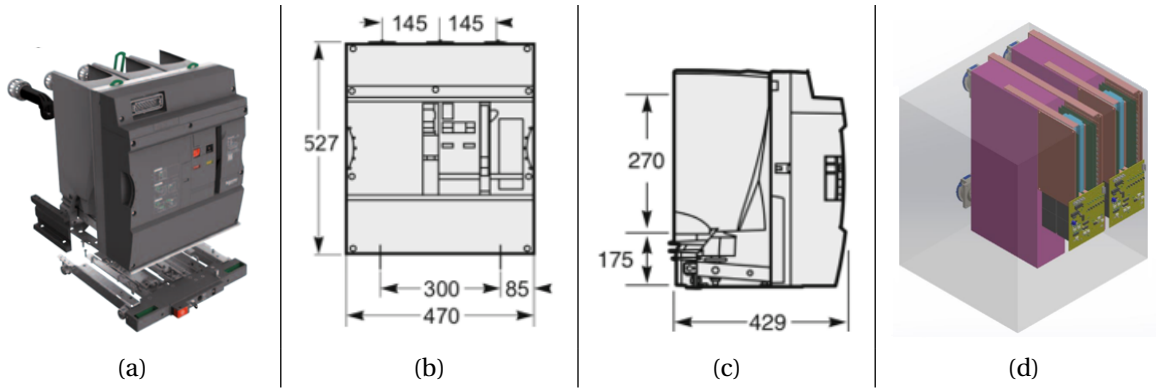


Figure 4.9 Size Comparison of EasyPact EXE to proposed SSCB (mm): (a) EasyPact EXE (b) EasyPact Dimensioned Drawing Front View (c) EasyPact Dimensioned Drawing Side View (d) Three proposed SSCBs can fit within the EasyPact EXE footprint. Two shown with film snubber caps

4.4 SSCB Package Fuse Curve

A thermal analysis was performed to evaluate the trip curve of the prospective power stage for the SCPM SSCB design. As the design uses three SCPMs in parallel, the nominal current for an individual JFET will be 33 A. To extract the fuse curve, time dependant heat transfer simulations were performed using FEA, evaluating the temperature rise in the device for each multiple of nominal current through 10X. The fuse time is defined as the time before the device reaches a critical junction temperature, $T_{j,c} = 175\,°C$. Two power stage designs were considered. The first is a standard Alumina based ceramic substrate and the second is a new Epoxy Rosin Composite Dielectric (ERCD) substrate, both rated for 10 kV. Simulations were performed in keeping with the guidelines outlined in 3.2.2. Care was taken to ensure the resolution of the mesh is independent of the simulation results. The boundary conditions of the simulations are as follows: (1) all surfaces aside from the bottom side of the baseplate are insulated, (2) a volumetric heat source is defined over the body of the device equal to the power dissipation due to the current, and (3) a surface heat flux is defined on the bottom of the baseplate to reflect heat sinking. This heat flux is defined by a user defined heat transfer coefficient of $h = 15\,W\,m^{-2}\,K^{-1}$ to reflect minimal convective cooling and provide a conservative estimate. The power dissipation was calculated dynamically

using an analytical function describing the temperature dependence of $R_{DS}(on)$ extracted from the device data sheet. The material thicknesses and properties used in the simulations are shown in Table 4.4 and the resulting surface temperature distributions for 250A and 300A fuse currents are shown in Fig. 4.10.

Table 4.4 Material thickness and properties of simulated 8mm x 8mm, 10kV power Stage Designs

Alumina DBC Substrate

Layer	Thickness (mm)	C_p ($J\,kg^{-1}$)	ρ ($kg\,m^{-3}$)	k ($W\,m^{-1}\,K^{-1}$)
SiC	0.15	1200	3200	450
Ag Sinter	0.035	235	10500	175
Cu pad	0.127	385	8700	400
Alumina	0.508	900	3900	27
Cu pad	0.127	385	8700	400
Ag Sinter	0.035	235	10500	175
AlSiC	2	741	3010	180

ERCD Substrate

Layer	Thickness (mm)	C_p ($J\,kg^{-1}$)	ρ ($kg\,m^{-3}$)	k ($W\,m^{-1}\,K^{-1}$)
SiC	0.15	1200	3200	450
Ag Sinter	0.035	235	10500	175
Cu pad	0.127	385	8700	400
ERCD	0.24	901	3900	8
Cu pad	0.127	385	8700	400
Ag Sinter	0.035	235	10500	175
AlSiC	2	741	3010	180

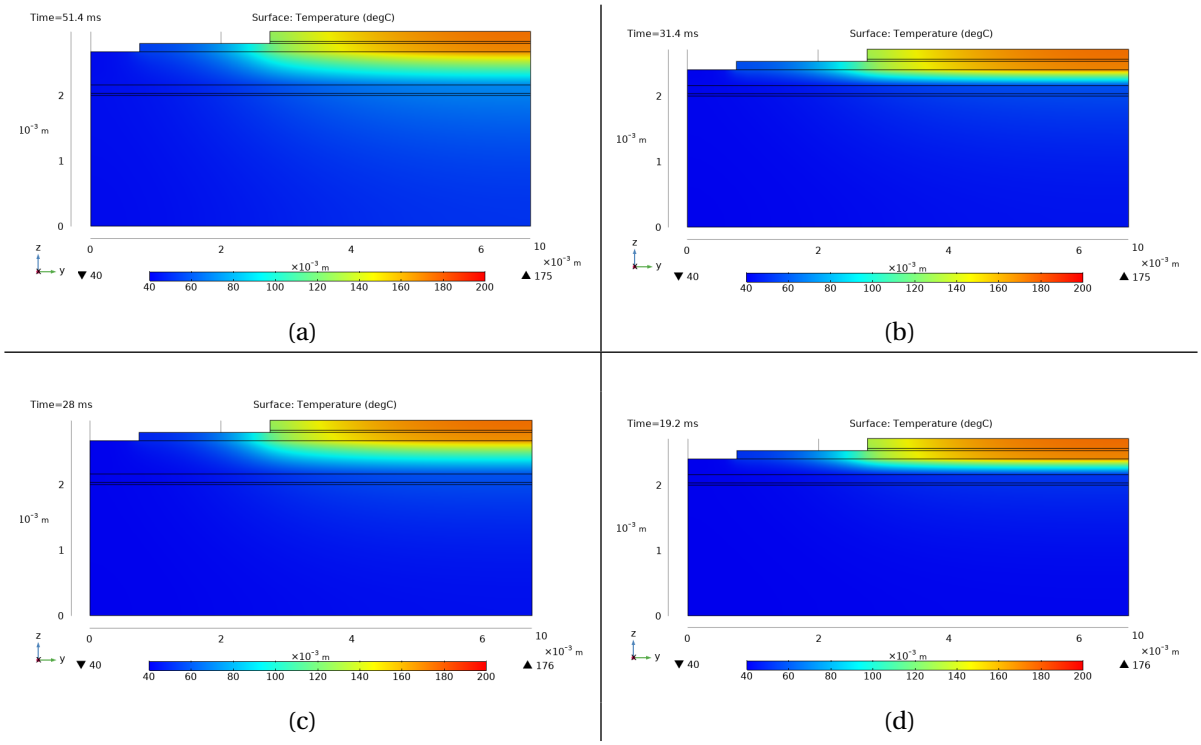


Figure 4.10 Surface temperature distribution 250A fuse circuit on (a) DBC power stage structure and (b) ERCD power stage structure and 300A fuse current on (c) DBC power stage structure and (d) ERCD power stage structure

The fuse time for each current case is extracted to plot the overall package fuse curve for each powerstage design. The results are plotted in Fig. 4.11 for comparison. These curves define the maximum operating limits of the SSCB using the concomitant power stage solution without additional thermal capacity and optimization. This also shows the practicality and success of using a SCPM for a SSCB application.

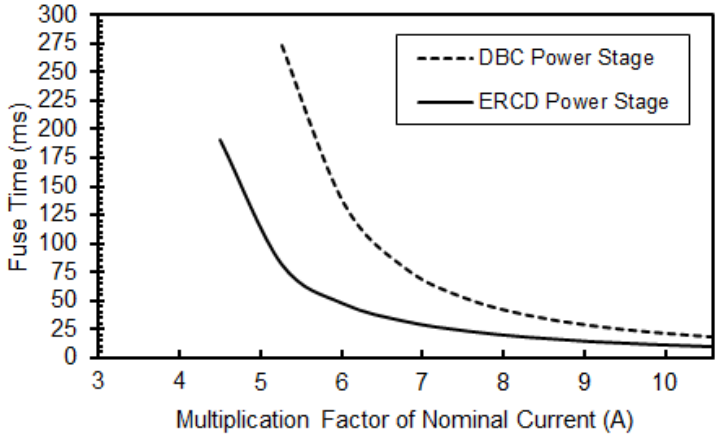


Figure 4.11 SCPM based SSCB simulated fuse curve for DBC and ERCD Power Stage Designs

CHAPTER

5

SUMMARY AND FUTURE WORK

5.1 Summary

This thesis explores and presents the design considerations and approach for scalable Solid State Circuit Breakers ranging into medium voltage. The range of operating behavior for an SSCB at high power is limited by the thermal performance of the power stage and temperature rise in the semiconductor devices. This thermal problem is explored in depth and multiple thermal modeling approaches are presented. Additional, a novel approach for approximating the average power dissipation of a device in a SSCB is proposed, which can be used to expedite the iterative design process. Finally, a 10 kV/100 A SSCB design leveraging a Super Cascode Power Module switching unit is presented alongside a scaled down prototype short circuit interruption demonstration.

The SCPM shows promise for enabling medium voltage SSCBs with fast short circuit interruption using lower cost semiconductor devices. The distributed topology of the SCPM also improves thermal performance by providing more area for thermal spreading and heat storage in the power stage.

5.2 Future Work

This work can be improved and extended in a number of ways including:

1. Optimize the relationship between the snubber and MOV layer to minimize size and cost.

2. Optimize the snubber layer further using staged MOV-Capacitor snubbers.

3. Explore the efficacy of the short circuit power dissipation average method by experimental verification across a variety of semiconductor devices and power stage configurations.

4. Expanding the trip curve by exploring novel methods of improving the thermal performance of the power stage such as double sided cooling, substrate-less packaging, and forced convection cooling with dielectric fluids.

5. Develop a full power prototype of the proposed SCPM based SSCB to validate short circuit interruption time and trip curve.

6. Explore SSCB designs leveraging series interconnections of SCPMs based on recent literature to achieve even greater voltage blocking.

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APPENDIX

APPENDIX

A

STEADY-STATE HEAT TRANSFER THROUGH A COMPOSITE WALL STRUCTURE

The general heat transfer equation through some mass is:

$$\frac{\partial}{\partial x}(k\frac{\partial T}{\partial x})+\frac{\partial}{\partial y}(k\frac{\partial T}{\partial y})+\frac{\partial}{\partial z}(k\frac{\partial T}{\partial z})+\dot{q}=\rho c_p\frac{\partial T}{\partial t} \tag{A.1}$$

where $\dot{q}$ is the thermal generation rate per unit volume ($\mathrm{W\,m^{-3}}$), ρ is the density ($\mathrm{kg\,m^3}$), and C_p is the specific heat capacity ($\mathrm{J\,kg^{-1}\,K^{-1}}$). As can be seen, the thermal conductivity can be different along each axis allowing the heat to propagate differently in each direction, which

in turn is also affected by the geometry in each direction, and each thermal conductivity itself is temperature dependant. In addition, the thermal generation rate can be driven by a variety of external forces. For instance, an electrical current flowing through some material, or joule heating, generates heat at a rate dependant on the current, which is system dependant, and on the electrical resistance, which is temperature dependant.

The complexity can be simplified by making some assumptions. For instance, in calculating the heat transfer through a thin wall it is typically assumed that K is constant, there is no thermal generation, heat is moving uniformly in one dimension, and the system is in steady state. These assumptions reduce equation A.1 to:

$$\frac{\partial^2 T}{\partial x^2} = 0 \tag{A.2}$$

This can be integrated twice and solved for a temperature distribution using the boundary conditions defined assuming some uniform temperature on each side of the wall, T_1 and T_2 respectively:

$$T = T_1 + (T_1 - T_2)\frac{x}{L} \tag{A.3}$$

Where L is the thickness of the wall. This equation can be differentiated with respect to x and substituted into the Fourier law of thermal diffusion:

$$q = -kA\frac{\partial T}{\partial x} = -kA(\frac{T_2 - T_1}{L}) \tag{A.4}$$

The collection of terms defining the coefficient to the temperature difference is seen as the *thermal conductance*, and it's inverse defines the *thermal resistance*:

$$R_{th} = \frac{L}{kA} \tag{A.5}$$

And combining equations A.4 and A.5 completes the relationship forming the electro-

thermal analogy discussed previously:

$$q = \frac{\Delta T}{R_{th}} \qquad \sim \qquad I = \frac{\Delta V}{R} \tag{A.6}$$

This solution can be extended for a composite wall of dissimilar material layers seen in Fig. A.1. R_{th} becomes the sum of the thermal resistance of each layer and the overall heat transfer through the composite wall is evaluated by:

$$q = \frac{T_L - T_o}{R_{th,1} + R_{th,2} + R_{th,n}} \tag{A.7}$$

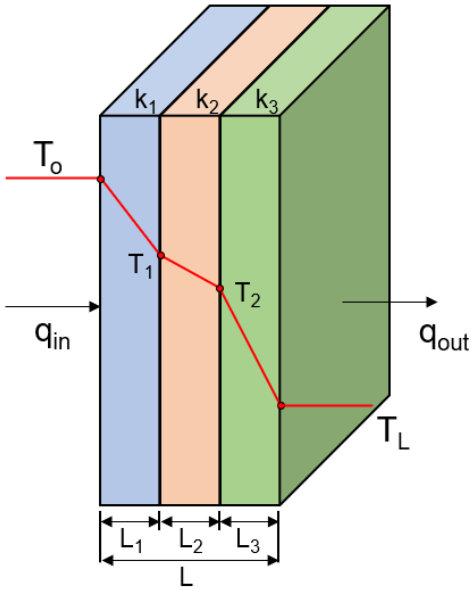

Figure A.1 Heat transfer through a composite wall of dissimilar materials

This case is enticingly similar to the case of the power stage in a power module. The majority of the thermal generation is provided by joule heating in the semiconductor devices, and this heat must travel through the material layers of the power stage and into the heat sink where it is transferred into either the air or a liquid coolant by convection. The layers of the power stage are typically all thin relative to their area however they are

not equal in lateral dimensions, as a result there will be thermal spreading and the one-dimensional heat flux assumption does not hold. The affect of the thermal spreading can be approximately accounted for by replacing A for each material layer with an effective cross sectional area, A_{eff}. By assuming an approximate spreading angle of 45, A_{eff} can be evaluated by:

$$A_{eff} = (l + \frac{t}{2})(w + \frac{t}{2}) \tag{A.8}$$

where l is the length of the material layer, w is the width of the material layer, and t is the thickness of the layer. A more accurate spreading angle through each layer can be evaluated by accounting for the thickness and thermal conductivity of each pair of interfacing layers. A method for evaluating this improved thermal spreading approximation is outlined in [64].