



US007351626B2

(12) **United States Patent**
Colombo et al.

(10) **Patent No.:** **US 7,351,626 B2**

(45) **Date of Patent:** **Apr. 1, 2008**

(54) **METHOD FOR CONTROLLING DEFECTS IN GATE DIELECTRICS**

(75) Inventors: **Luigi Colombo**, Dallas, TX (US);
James J. Chambers, Dallas, TX (US);
Mark R. Visokay, Richardson, TX (US);
Antonio L. P. Rotondaro, Dallas, TX (US)

(73) Assignee: **Texas Instruments Incorporated**,
Dallas, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 167 days.

(21) Appl. No.: **10/739,617**

(22) Filed: **Dec. 18, 2003**

(65) **Prior Publication Data**

US 2005/0136690 A1 Jun. 23, 2005

(51) **Int. Cl.**
H01L 21/336 (2006.01)
H01L 21/8234 (2006.01)

(52) **U.S. Cl.** **438/197**; 438/216; 438/287;
438/591

(58) **Field of Classification Search** 438/216,
438/240, 287, 591, 769, 775, 785, 786, 197,
438/585

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,786,277 A *	7/1998	Yamamoto	438/770
6,013,553 A *	1/2000	Wallace et al.	438/287
6,060,755 A *	5/2000	Ma et al.	257/410
6,162,744 A *	12/2000	Al-Shareef et al.	438/785
6,544,906 B2 *	4/2003	Rotondaro et al.	438/785
6,689,675 B1 *	2/2004	Parker et al.	438/585

* cited by examiner

Primary Examiner—Zandra V. Smith

Assistant Examiner—Khanh Duong

(74) *Attorney, Agent, or Firm*—Jacqueline J. Garner; W. James Brady, III; Frederick J. Telecky, Jr.

(57) **ABSTRACT**

A method for improving high-κ gate dielectric film (104) properties. The high-κ film (104) is subjected to a two step anneal sequence. The first anneal is performed in a reducing ambient (106) with low partial pressure of oxidizer to promote film relaxation and increase by-product diffusion and desorption. The second anneal is performed in an oxidizing ambient (108) with a low partial pressure of reducer to remove defects and impurities.

9 Claims, 1 Drawing Sheet

