## ABSTRACT

SATVIK. High Power Bidirectional Resonant DC-DC Converter With Improved Efficiency. (Under the direction of Dr. Wensong Yu.)

This paper presents a novel bi-directional resonant converter which aims at obtaining high efficiency at desired voltage range of operations through selection of transformer turns ratio. A prototype converter design is performed against a target application of a bidirectional power transfer between a DC Microgrid and a battery based Energy Storage System. Experimental verification of the converter design is performed for a low voltage design to obtain experimental proof of concept for the proposed design along with a simulation level design of the prototype implemented on PLECS.

The converter design targets high efficiency through soft switched Zero Voltage turn on which helps ensure minimal switching losses since a major component for any switching transition loss is the turn on energy dissipation. The design process for the prototype design is discussed in the thesis along with a discussion regarding opportunities for improvement of soft switched load range. A phase shift modulator is designed for the converter to obtain bidirectional power transfer. The modulation scheme used for the reduces the effect component variations on the converter operation with a higher degree of control on the type of soft switched operation simplifying the control design.

The converter design utilises the benefit of it being a non-isolated design by utilising an auto-transformer for voltage gain selection to further improve design in terms of overall cost and volume of the design. A detailed converter design is presented in the thesis along with design equations for selection of the component values. Analytical models for the converter design are developed to model the relation between the average value of the low side bus current and phase shift angle. The design equations and converter operation are verified through simulation level verification.

# High Power Bidirectional Resonant DC-DC Converter With Improved Efficiency

by
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## BIOGRAPHY

Satvik was born in Lucknow, Uttar Pradesh, India in 1994. He received his bachelors degree in Electrical and Electronics Engineering from Manipal Institute of Technology, Karnataka, India in 2016 after which he worked at Philips India,Pune as a Sr. Electrical Engineer for two year. He moved to Raleigh, North Carolina, USA in 2018 looking to pursue his masters in Power Electronics at NCSU. His focus areas for research are DC-DC Power Converters and EV power conversion.

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# 1

# INTRODUCTION

## 1.1 Thesis Objectives and Overview Discussion

The thesis discusses the design and analysis of a high efficiency bidirectional non-isolated DC-DC resonant converter designed for power transfer between a DC Microgrid and a battery-based energy storage system. The main focus of the discussion in this thesis is the operating principle of the converter bidirectional power flow, the soft switched operation of the converter, and a design approach for the selection of the component values. This is followed by a discussion of the control structure for the target application of the proposed design and a simulation level design of the converter against specifications set for the desired application. A low voltage experimental verification for the converter operation performed to verify the soft switching phenomenon is presented.

The proposed converter design aims at utilizing a bi-directional power transfer and to obtain high efficiency through soft switching by current reversal for the switches. The innovation introduced in the design is the introduction of a non-isolated auto-transformer which allows for the design of the converter for any voltage level around which very high efficiency can be obtained. The converter design approach is performed similarly as that of a resonant dual active bridge along with a detailed derivation of the proposed converter topology starting from the dual active bridge converter. A comparison that shows the benefits of the topology is presented to compare the benefits of the design against a similar isolated and non-isolated topology.

The simulation designed allows for verification of the converter operation and also for an estimation of the overall efficiency of the design using a loss model used to determine the transformer and switch losses. The loss models are further verified with the use of analytical equations using which the final efficiency model is presented. Finally, analytical equations are developed to obtain

the values of the current peaks which are used to determine the relationship between the phase shift and the output current used to obtain the controller design.

## 1.2 Thesis Outline

The thesis report is divided into 8 chapters with additional derivations provided in the A and B where the design equations and current derivations are presented.

- **Chapter 2** provides an introduction to the converter application and the derivation of the converter topology. A study of the literature available is performed and the converter topology derivation is provided in detail. The converter design is then compared against state-of-the-art designs with a focus on the benefits offered against each of them.
- **Chapter 3** deals with the conditions required for obtaining bidirectionality for a converter design. The design process is explained in detail with the base equations used for obtaining an initial value for the components. The principle of operation along with the modulator design is described in detail with emphasis on ensuring bidirectional power transfer.
- **Chapter 4** discusses the soft-switching conditions and the benefits of the soft switched operation. The phenomenon of soft switching is explained along with the process by which Zero Voltage Switched (ZVS) transitions are obtained for the given converter design. The major requirements which are essential for ensuring the converter can be soft switched for the operation are discussed along with an analysis of the effects of variations in the optimization properties.
- **Chapter 5** outlines the control structure for the converter for the given application and describes in detail the controller design to obtain an average current control over the controller. It also discusses the modeling of the uncompensated control loop and the design of the controller along with verification on a simulation level.
- **Chapter 6** provides details of the prototype design for the converter application. The chapter details the design specifications used for the selection of the components followed by the actual component values obtained based on commercially available parts.
- **Chapter 7** explains the simulation level design of the converter which describes in detail the modeling approach used for designing the simulation and an experimental setup for verification of the soft switching behavior. The transformer switch loss models used for efficiency verification are presented in order to demonstrate the procedure used to calculated efficiency values.
- **Chapter 8** concludes the thesis and provides a description of the objectives targeted by the thesis and the results of the study. A discussion of the possible areas for further research is provided in this chapter.

CHAPTER

# 2

# LITERATURE REVIEW AND CONVERTER DERIVATION

## 2.1 Introduction

This chapter discusses the literature review and analysis of the current state of the art converter topologies. A detailed discussion regarding the converter application and the targets set for current research in the area is discussed with a discussion of the research performed in this regard. A topological derivation is provided in this section to describe the design process and the objectives set to obtain the proposed converter topology. A comparison between the proposed converter design and the state of the art topologies having a similar region of operation is also presented for a better understanding of the benefits and drawbacks of the proposed design against the target application.

## 2.2 DC Microgrid

A DC Microgrid [1] is an interconnected DC power supply which is used to charge a common voltage line to which several loads can be connected. This type of distribution finds it's application areas such as data centers, electric vehicle charging stations and telecom stations [2], [3], [4], [5]. The main operating modes for the microgrid [6] can be classified as,

- Normal Interconnected Mode- During the mode the microgrid either supplies or draws power from a voltage network.

- Emergency Mode— In this mode of operation, due to either a fault or intentional disconenction, the microgrid can go into "islanding" mode where it disconnects from the main voltage network and can supply power to the loads autonomously.

The "islanding" feature is essential for the microgrid for which satisfactory performance and high efficiency values are expected for the power transfer between the microgrid and the energy storage systems connected to the microgrid. There has been significant research on the topic of microgrid control[7] and stabilisation of the microgrid can be seen in the work of [8].

## 2.3 Energy Storage System

The Energy storage systems(ESS) can be comprised of capacitors or even Lithium Batteries arranged used to power the DC grid to which it is connected[9], [10], [11], [12]. The energy storage system can store energy during off peak operation and discharge the load during peak load conditions. This energy storage bank can also be switched on or off as required by controlling the DC-DC converter. The control for the energy storage system has been investigated and several approaches for high efficiency control have been suggested [6], [13]. The command value for the control of the power flow between the grid and ESS can be obtained from such a control.

## 2.4 Power Electronics Interface

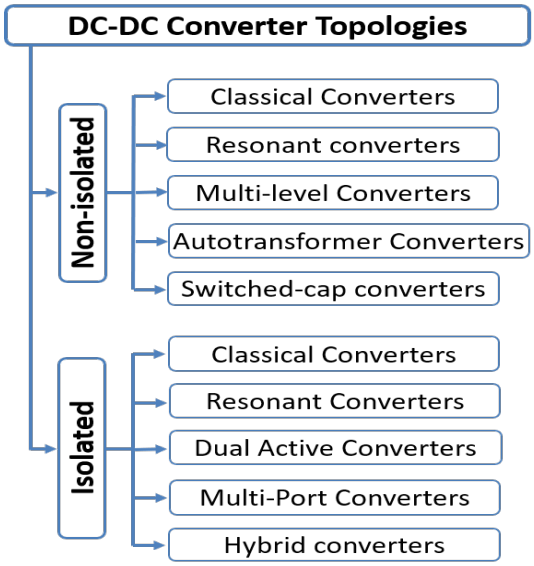


**Figure 2.1** State of the art topologies

Based on the study of the interaction between the ESS and the microgrid, it is evident that there

is a requirement for a near ideal bidirectional power transfer where a reduction in cost and volume would be immensely beneficial. There are several power converter topologies which can be used and have been suggested for for this target including several non-isolated and isolated versions of conventional converter designs[14], [8]. These designs are targeted at obtaining designs for bidirectional transfer while ensuring as high efficiencies as possible and to have minimal environmental impact on the environment. As seen in the work done by [14], phase shift modulated converter designs have several advantages compared to conventional power transfer due to the benefits such as bidirectionality and high efficiency. Non-isolated converter designs for bidirectional power transfer were also compared in order to obtain an improvement in cost and also in terms of power density [15] where bi-directional three level converters were used with the target of optimising the design for improvements in efficiency. However, the existing topologies suffer due to the high cost of the converter due to the high switch ratings and size of the magnetics required to meet the requirements of the design.

With the introduction of Silicon Carbide(SiC) MOSFETs the overall efficiency for high power converter designs can be further improved upon due to benefits such as reduced conduction losses and lower device capacitance in comparison to their silicon counterparts. The use of SiC MOSFETs for bidirectional power converters has been utilised before as done in [16] where the authors compared the performance of the SiC devices in a multi stage bidirectional converter. The efficiency values obtained were upto 98% as noted by the authors. Further research done on designing converters based on SiC note their benefits in terms of power loss which in turn reflects a lower volume of the devices used. The work done by [17] demonstrates an analysis for the SiC MOSFET losses for low frequency high power switching. It can be observed that even for low frequency operations, the device losses due to switching are significant for a dual active bridge design. These losses have a significant contribution in terms of the percentage of total losses in the converter operation. A comparison between the Silicon and Silicon carbide devices has been done by [18] which demonstrates the superiority of the SiC devices over their Si Counterparts which make the the use of SiC devices a viable option for a high efficiency design. The high switching speeds for the power switches also further has additional benefits in terms of reduction in overall size of the magnetics which improves the power density of the overall design.

## 2.5 Target Application

The thesis focuses on the improving the power transfer efficiency between the low voltage gird while ensuring bidirectional power transfer between a DC Microgrid and a battery based energy storage system[19]. The main benefits that the topology seeks to achieve is a reduction in the overall device ratings and subsequent device stresses allowing for reduction in the cost and size of the devices. In addition to this, there has been a focus on reducing the cost of the magnetics for the design by utilising an autotransformer based power transfer. This allows for a focus on the target application as shown in Fig. 2.2.

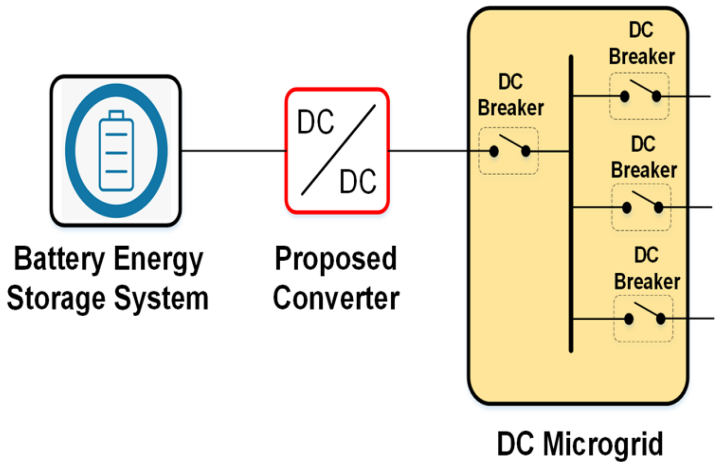


**Figure 2.2** HPBRC application

In order to further improve the soft switching advantage offered by the topology, the converter operation is targeted for a high switching frequency which allows for reduced size of the magentics while the switching losses are kept low due to ZVS turn on. The conduction losses are significantly reduced with the use of SiC MOSFETs which have a significantly lower device rating as compared to the isolated DAB design which allows for reduction in overall cost and volume of the converter.

The benefits as obtained by the proposed design will be discussed in detail in the next sections by comparison with state-of-the-art converter designs which have a similar operation.

## 2.6 State of the art Converter Topologies

### 2.6.1 Dual Active Bridge

The dual active bridge proposed initally by [20][21],[22], is a converter which obtains high efficiency by varying the polarity of the voltage across the power transfer element which for this converter is either an inductor or the leakage inductance of a transformer. Zero Voltage Switched transitions are obtained for the converter design by polarity reversal of the current at the time they are switched which allows the output capacitors of the power switches to discharge. The conventional modulation scheme used for control of the dual active bridge involves the use of a phase shift control to allow for control over the power transfer between the the two ports of the converter.

A schematic for a typical Dual Active Bridge design is presented in Fig. 2.3.In order to obtain bidirectionality, the converter modulation is performed by using a phase shift modulation scheme between the two sides of the switches in order to ensure the average inductor current is close to zero. The phase shift time interval is directly proportional to the total power transfer of the converter.

The base arrangement for the converter design was further modified in order to add capacitors for obtaining a wider soft switching range as seen in the addition of resonant capacitors [23] which

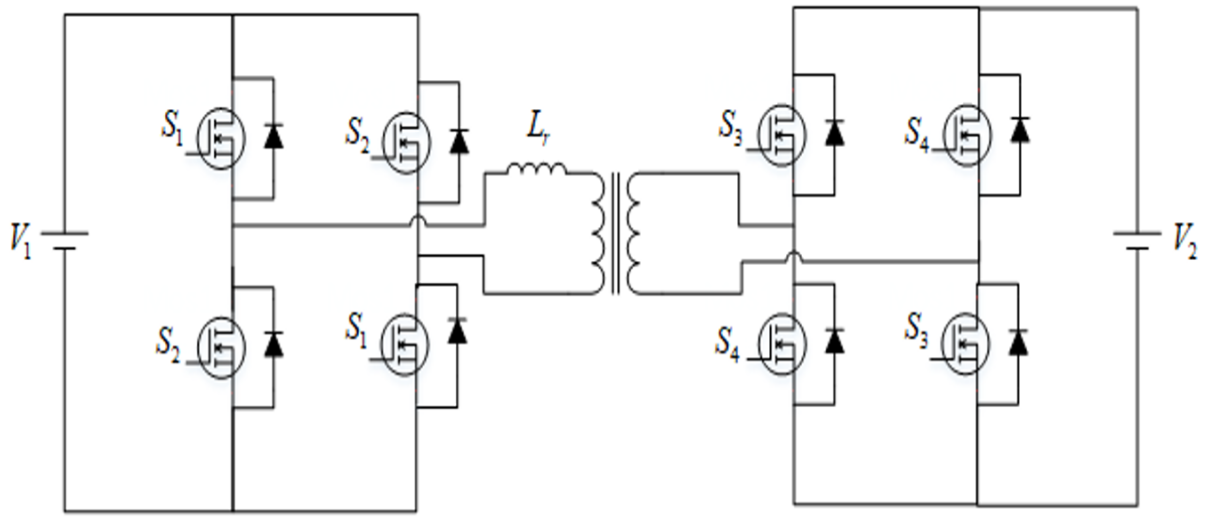


**Figure 2.3** Dual Active Bridge Converter

allow for an increase in the soft switching range by allowing for resonance between the inductive and capacitive elements of the circuit.

### 2.6.2 Switched Capacitor Converters

A switched capacitor converter is an algebraic voltage solver converter which is controlled by digital control to allow for different voltages outputs which are a multiple of the converter input voltage[24],[25],[26],[27] as shown in Fig. 2.4.

As the voltage is switched across the individual capacitors, there is a spike of current due to a change in instantaneous voltage which results in increased losses during switching as the current stress is handled by the power switch. This current spike can be addressed with the use of a inductor which allows for a design which is a series resonant tank. This converter is termed to be a switched capacitor resonant converter design. A schematic for the design can be seen in Fig. 2.4 with a target buck operation for half the input voltage.

The main benefits of using a switched capacitor topology is the high values of efficiency which is obtained as a results of no magnetic components however, there are several modifications in the circuit configuration that allow for improved efficiency through switching loss reduction by ZVS or ZCS. Some of the converters utilised the addition of leakage inductances in order to obtain soft switching through either ZVS/ZCS utilising a frequency modulator for control of the switches,[28][29] however these designs are still limited in output range and are dependent on combinations of a large number of switches and capacitors to obtain variation in voltage gain.

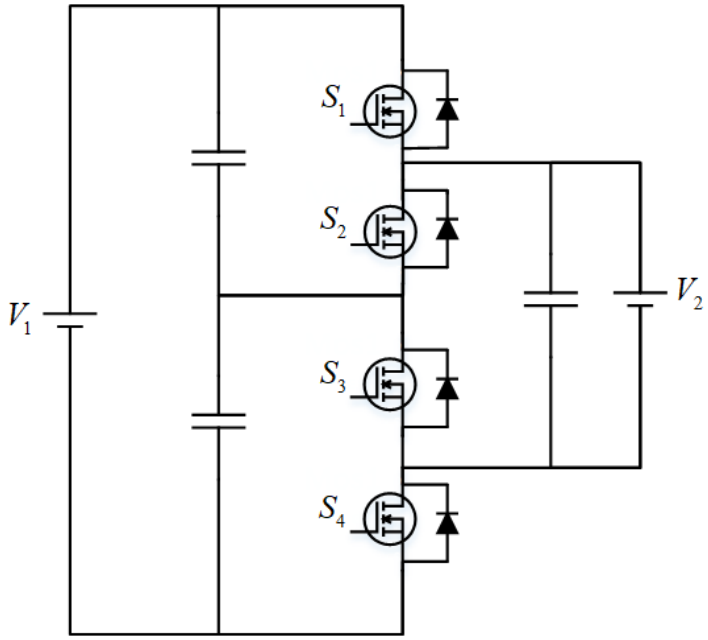


**Figure 2.4** Switched Capacitor Converter

## 2.7 Topology derivation

This section details the converter topology derivation where in the proposed design is obtained starting from a full bridge dual active bridge.

- Step 1:

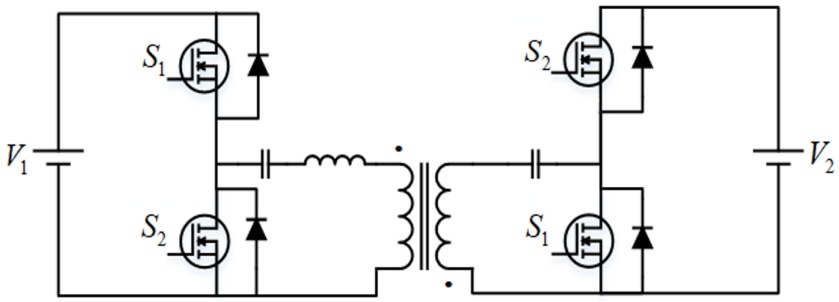


**Figure 2.5** Modification for Step 1

Starting from a Full bridge DAB Design, the number of switches are reduced in order to reduce the gate drive complexity. Additional voltage balancing capacitors are added to both sides of the transformer in order to allow for a voltage balancing across the leakage inductance of

transformer. The capacitors also have another benefit in terms of the addition of an intermediary voltage around which phase shift modulation can be obtained. Since the voltage would be naturally balanced at half the voltage across the the input for the primary side capacitors and half the voltage across the secondary side of the capacitors. Due to this, there is no longer a need to maintain the positive and negative voltage previously required since the positive and negative voltages are obtained across the transformer leakage with just one set of switches. The polarity of the transformer is reversed in order to allow for an average voltage across the capacitors to be maintained at half the input side voltage for the primary and half the output side voltage for the secondary and is essential in ensuring power transfer using phase shift modulation. Hence with this step, with the addition of two capacitors, the number of switches required is reduced.

- Step 2:

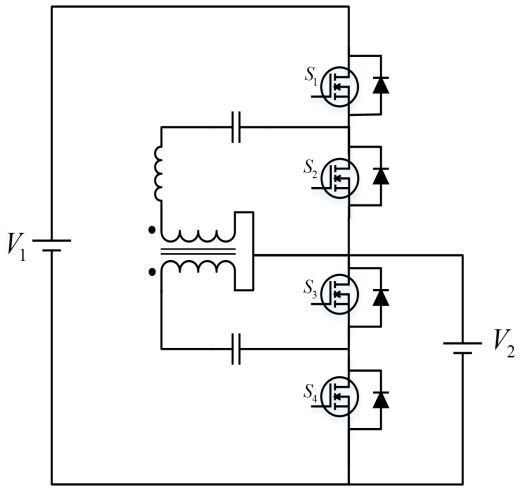


**Figure 2.6** Modification for Step 2

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The next step involves linking the primary side of the circuit with the secondary in order to reduce the total component stress. This step allows for a reduction in the total current that has to be handled by the secondary side switches since a part of the load is now being supplied by the primary side switches. Another benefit of this step is the significant reduction in the voltage stress across the primary side switches as a results of the reduction in the bus voltage as now the switches only need to support the difference between the primary and secondary side voltages. The transformer now sees a reduced voltage stress on the primary which would be the difference between the primary and secondary side bus voltages as in the case of the switches. However, it has to be noted that though there are significant improvements there is a loss of isolation. For the given target application, since there is no requirement for isolation, this change is acceptable.

- Step 3: The next step in the derivation of the final converter topology is the modification of

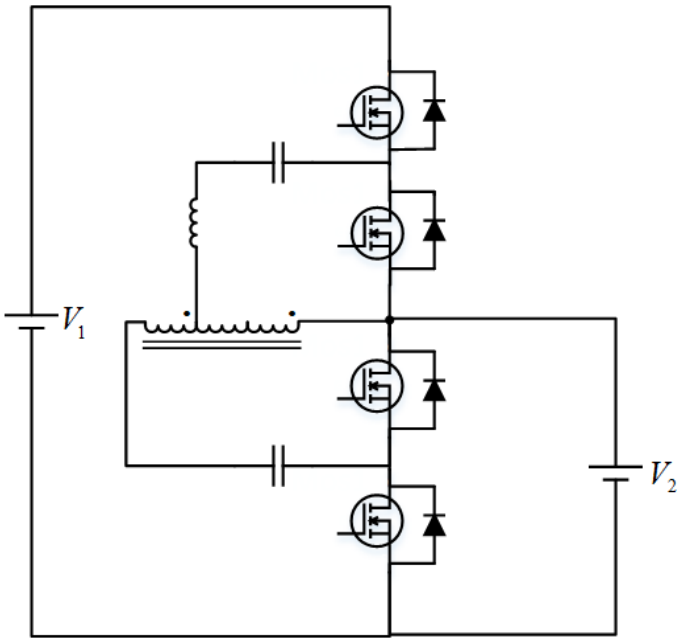



**Figure 2.7** Modifications for step 3

the common connected isolation transformer to a non-isolated auto-transformer as shown in Fig. 2.7. This allows for benefits in cost and volume of the design. This effectively improves the efficiency of the converter due to current sharing in the windings. The total current across the winding can be reduced leading to lower copper losses in the converter.

The proposed converter thus can maintain control over power transfer based on the phase shift control as utilised for a dual active bridge and has several benefits due to its non-isolated design which involve a reduction in the overall component stresses. It can be proved that the overall efficiency targeted by such a design can be significantly high since the device no longer suffers from turn on losses. Another significant feature of such a design is the reduction in switching losses during hard switched turn on transitions due to lower voltage stress on the high side switches and lower turn off current in the case of the low side switches. Since the switching losses are reduced, it is possible to operate at much higher switching frequencies which can further reduce the size of the magnetics and capacitors to be used with the converter. Thus, the overall power density can be improved significantly. Moreover, the use of the autotransformer further aids in overall power loss reduction due to a reduction in the copper losses associated with the transformer. This thesis explains in detail the design and modulation of the proposed design along with a simulation level analysis of the converter against desired application voltages. Optimisation opportunites are presented in order to understand the possibilites of improvement in the soft switching range for the converter along with equations derived to model the magnitude of the resonant current magnitudes

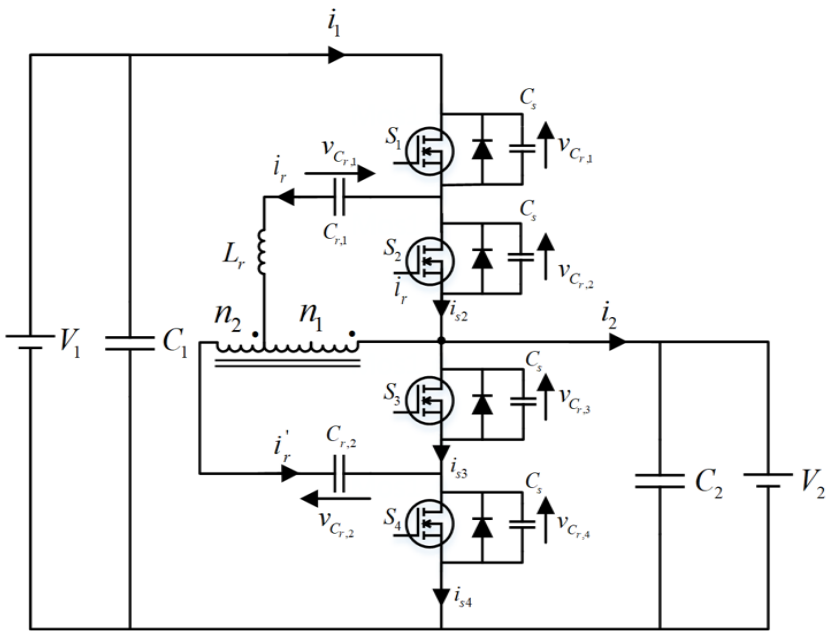



**Figure 2.8** High Power Switched Capacitor Resonant Converter

at the end of each mode. A theoretical model is also derived to obtain a relation between the output current and the phase shift control value.

The final obtained topology is presented in Fig. 2.8 with the features of this topology having been mentioned as:

- Non-isolated design
- Variable output range
- Bidirectional power transfer
- High efficiency due to ZVS soft-switched turn on
- Significantly reduced voltage stresses over all the primary side components
- Significant current stress reduction due to the addition of a current path through the high side switches.

In order to obtain a comparison of the converter topology and the benefits obtained from the improvements in the converter design, two topologies are compared with the proposed converter. The switched capacitor converter is used as a state of the art for comparison due to the fact that the proposed converter is similar to it since the peak operational efficiency values can be obtained around a fixed output to input ratio. Moreover, the efficiency values obtained for such a topology are significantly high around the designed operating voltage gain due to the use of only capacitive elements. All these features make it a good topology which can be used for a comparison between the proposed converter design in terms of operational range similarity.

**Table 2.1** Non-Isolated Converter comparison

| Switched Capacitor Converter | Proposed Converter |
|---|---|
| Voltage gain limited to around half the voltage on V1 side for high to low power transfer. | Voltage gain between input and output side can be varied by controlling the turns ratio of the auto-transformer. |
| Complex digital control required | Phase shift modulation with a PI compensator used for control. |
| High efficiency obtained due to only capacitive elements, ZVS/ZCS operation possible with the use of resonant circuits for improved efficiency | High efficiency ensured by ZVS. |
| High current spikes during transitions due to flying capacitor | Spiking controlled by resonance. |

**Table 2.2** Isolated Converter comparison

| Dual Active Bridge | Proposed Converter |
|---|---|
| Voltage gain between input and output side can be controlled by transformer turns ratio, however losses are higher due to higher current through the windings | Voltage gain control is similar through autotransformer design with total copper loss lowered due to reduction in current |
| Isolation possible | Non-isolated design |
| Higher Device stress due to isolated primary and secondary | Lower device stresses due to reduced current circulation between primary and secondary sides |
| Voltage maintained across leakage inductance by voltage sources | Voltages maintained across leakage inductance as a difference between voltage applied and capacitor voltages |
| Larger converter volume due to transformer size | Reduced converter volume due to autotransformer size |

The isolated Dual Active Bridge converter is used to obtain a comparison for an isolated design again due to similar power transfer stage. Both the converter designs rely on bidirectional current transfer to obtain a soft switched power transfer in order to obtain high efficiency. However, the converter offers improvements in terms of reduced device stresses which allow for improvements in terms of the switching loss reductions during hard switched operations and further reduction in terms of peak efficiency values.

A comparison between the converter designs can be summarised as listed for the non-isolated converter design as given in 2.2 and for isolated converter design as listed in 2.1. These are performed in order to obtain a better understanding of the benefits offered by this converter design.

The differences between the converter topologies demonstrate the benefits the proposed topology has in comparison to the state of the art non-isolated and isolated topologies. The thesis

currently focuses completely on high efficiency values, however, it has to be noted that there are several optimisation opportunities possible in terms of improvements in the soft switching range with improvements in converter control design, power density improvements through optimisations in the transformer size. These possibilities offer a lot of scope in terms of future research possible.

The converter suffers from a limited voltage gain range as the high efficiency values are possible only around the voltage for which the converter is designed for. The minimum power transfer for which the converter loses out on soft switching steadily decreases as the operating voltage moves away from the design target voltage. However, for the proposed application, the converter completely meets the requirements as the voltage variation seen by the converter is limited. Moreover, since the voltage does not have to be maintained the voltage ratings selected for the design is also limited to the difference between the $V_1$ and $V_2$ voltage magnitudes.

## 2.8 Summary

The chapter provides a detailed introduction to the target application and the benefits that the proposed topology has which makes it an ideal choice for the target application. The converter topology derivation and a detailed comparison between an isolated and a non-isolated converter is presented to demonstrate the benefits of the topology.

CHAPTER

# 3

# BIDIRECTIONAL POWER TRANSFER

## 3.1 Introduction

This chapter introduces the converter operating modes required to maintain bidirectional power transfer for the proposed converter design. A detailed analysis of the bidirectional power transfer obtained for the converter and the modulation scheme used to ensure desired operating modes is presented in this chapter along with the detailed derivation of the values of the current magnitudes and observed waveforms for the converter as obtained by simulation of the design on PLECS. The chapter discusses the design equations used for deriving the starting point around which the converter can be designed.

## 3.2 Principle of Operation

In recent years, bidirectional power transfer in a DC-DC converter design has gained traction due to the associated benefits of current polarity reversal which allows for natural Zero Voltage Switched transition [30], [20], [22]. This in turn increases the efficiency of the converter design due to soft switched transition since the current polarity can be reversed in order to have complete device discharge before turn on.

In addition, the power transfer bidirectional power transfer has an additional benefit in terms of significant reduction in the energy stored in the magnetic components since the total energy is transferred by the area under the positive and negative halves. For the proposed converter design, the bidirectionality of the converter power transfer is maintained by controlling the magnitude of voltage across the leakage as shown in Fig. 3.1.

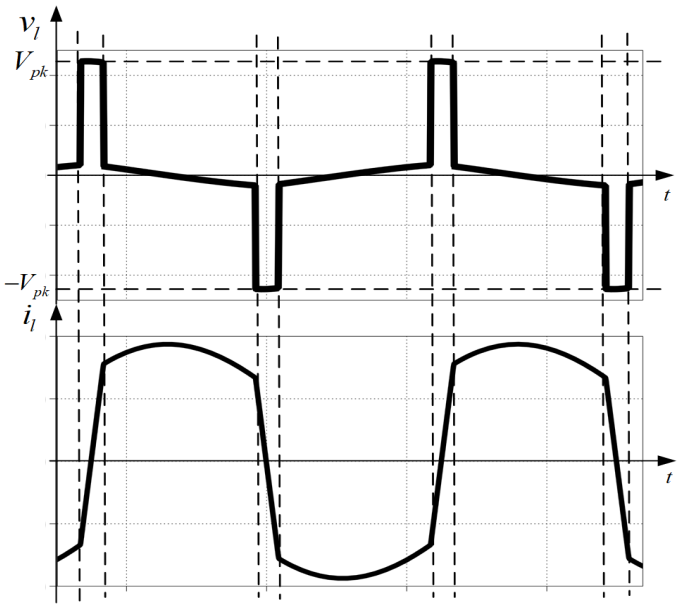



**Figure 3.1** Inductor Waveform

This can be further analyzed for this converter by comparing the energy stored in a buck converter designed for the same power level. The waveform can be analyzed for the operation as shown in Fig. 3.1 by considering each case and analysing the inductor current values using first principles as given in equation

$$v_l = L\frac{di_l}{dt} \tag{3.1}$$

Since Regions 3 and 4 are symmetrical to regions 1 and 2, an analysis is performed only for regions 1 and 2 and extrapolated for regions 3 and 4.

- Region 1:

  During this period, the voltage across the inductor is maintained as a value $v_l$=$V_{pk}$ Hence the inductor current can be obtained by integrating equation 3.1 as:

$$i(T_s) = v_l.T_s - i(0) \tag{3.2}$$

- Region 2: During this period, the voltage across the inductor is maintained as a value $v_l \approx 0$. Hence the inductor current can be obtained by integrating equation 3.1 as:

$$i(T_{sw}/2) \approx i(T_s) \tag{3.3}$$

Hence if the voltage peaks are equal, the current peaks have a linear relationship with the time duration for region 1 and 3 which will be the case during steady state of operation. This inductor

waveform can then be rectified to generate an average current with a value given by the averaging the current across each switching period. Bidirectional power transfer can thus be obtained by reversing the polarity of the voltage seen by the inductor changing the polarity of the inductor current which is achievable by hardware simply by changing the gate pulse sequence.

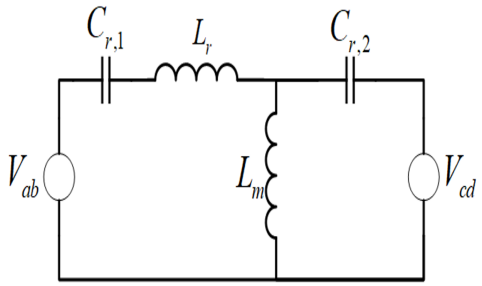



**Figure 3.2** Simplified Resonant Tank Circuit

Since the current can be of either polarity, there is a requirement of semiconductor devices which can conduct current in both directions making MOSFETs the ideal device of choice due to their bidirectional current carrying capacity and unidirectional voltage blocking. In order to obtain control over the inductor voltage, it can be observed from the circuit schematic that a phase shift control between the gate pulses for switches $S_1$ and $S_3$ can provide control over the inductor voltage. The switches $S_2$ and $S_4$ are driven by gate signals complementary to switches $S_1$ and $S_3$ respectively. The converter operator can now be analyzed to obtain the required inductor waveform across the leakage inductance.

## 3.3 Operating Modes

The converter operating modes are identified to obtain a waveform across the leakage inductance of the converter as shown in Fig. 3.1. The individual operating modes are identified and analyzed in order to describe the power flow and the method used for obtaining a bidirectional power flow. It has to be noted that the resonant tank is in fact a series resonant converter [31] [32] hence a model for the tank elements can be generated to obtain an understanding of the frequency response of the tank as shown in Fig. 3.2.

The response of a series resonant tank is inductive for an operating frequency higher than the resonant frequency, $f_r$ given by $f_r = \frac{1}{\sqrt{L_r C_r}}$. For an inductive region of operation, the resonant current lags the voltage and thus it is possible to have some residual current even when the voltage is close to zero which is used to discharge the output capacitors of the power switches. This can be further explained in 4 where the soft switching operation of the converter is discussed in detail.

Since the converter operates in an inductive region of operation the capacitor size is large enough to maintain the voltage during the short intervals when the phase shift is introduced between the

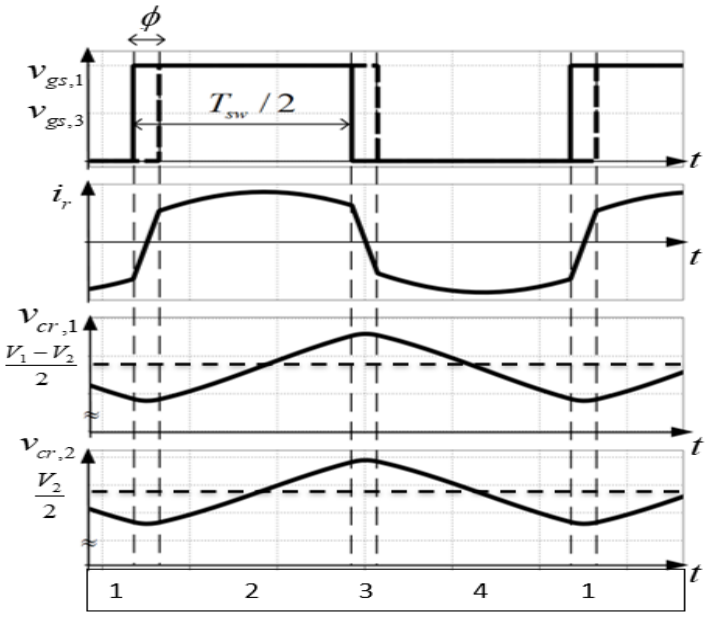



**Figure 3.3** Converter Operation Waveforms

switches allowing for a large voltage across the inductor which is explained in detail below. The relevant waveforms required to explain the operation of the converter are presented in Fig. 3.3. The resonant capacitors are lumped on the primary side represented by $C_r$ in order to simplify analysis. The inductance $L_r$ is the effective leakage inductance of the transformer with the inductance $L_m$ representing the magnetising inductance. The core and copper losses for the transformer are assumed negligible for this analysis and will be accounted for during the loss distribution modelling.

- **Mode 1**:

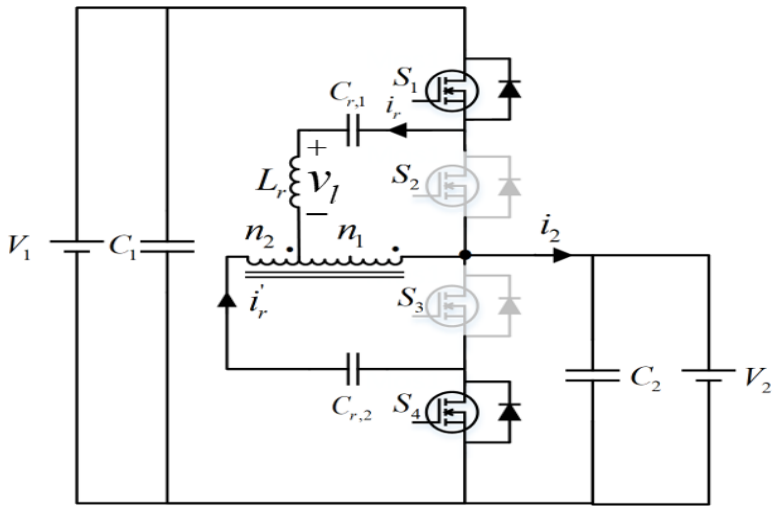



**Figure 3.4** Operating Mode 1

This mode is identified as region when the leakage inductance sees a positive voltage across it in the polarity as marked in Fig. 3.4. The inductor current rises linearly as shown in Fig. 3.3. The relation between the peak current and the phase shift can be proved to be almost linear in this region since the voltage across the resonant capacitor has negligible change from the average value if the capacitors are large. The peak value of the inductor current is thus determined by the phase shift interval.

The current path is through switches $S_1$ and $S_4$. The capacitor voltage for the primary side resonant capacitor is given by $V_{c,r1}$=$V_{cr1,avg}$-$\Delta v_{c,r1}$ and $V_{c,r2}$=$V_{cr2,avg}$-$\Delta v_{c,r2}$. Thus the voltage seen across the resonant tank denoted by $V_{ab}$= $V_1$-$V_2$ and $V_{cd}$=$V_2$.

- **Mode 2**:

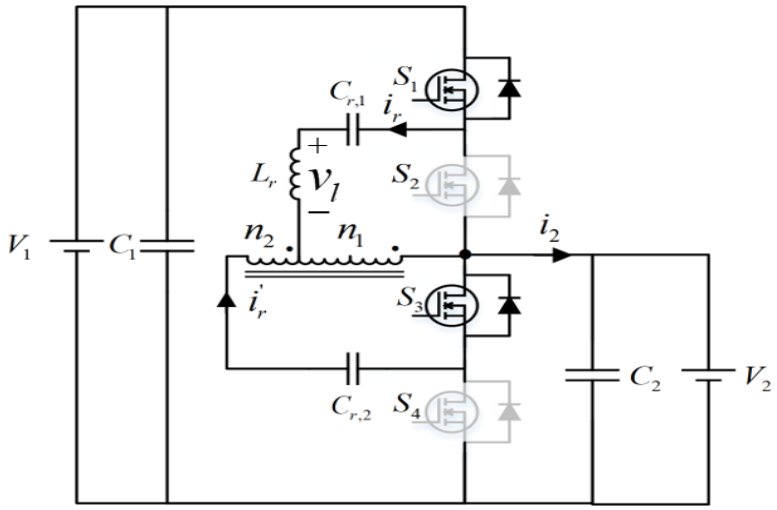



**Figure 3.5** Operating Mode 2

This mode is identified as region when the leakage inductance sees a positive resonant voltage across it in the polarity as marked in Fig. 3.5. The inductor current magnitude either falls or rises with a small variation or maintains its value depending on the voltage difference seen across the leakage inductance. This value is dependent on the magnitude of $V_1$ and $V_2$. The capacitor voltages invert polarity during this mode. The current path is through switches $S_1$ and $S_3$. With reference to the resonant tank, $V_{ab}$= $V_1$ and $V_{cd}$=$V_2$. The average voltage across the resonant tank can be obtained as $v_r$=$V_1$-$V_2$ when $V_1$=$V_2(1+\frac{1}{n})$. During this mode The value of the current $i_2$=$i_r$ due to the conduction of switch $S_3$.

- **Mode 3**:

This mode is identified as region when the leakage inductance sees a negative voltage across it in the polarity as marked in Fig. 3.6. The inductor current falls linearly as shown in Fig. 3.3. This mode is complementary to the operation of the converter in mode 1. The duration of

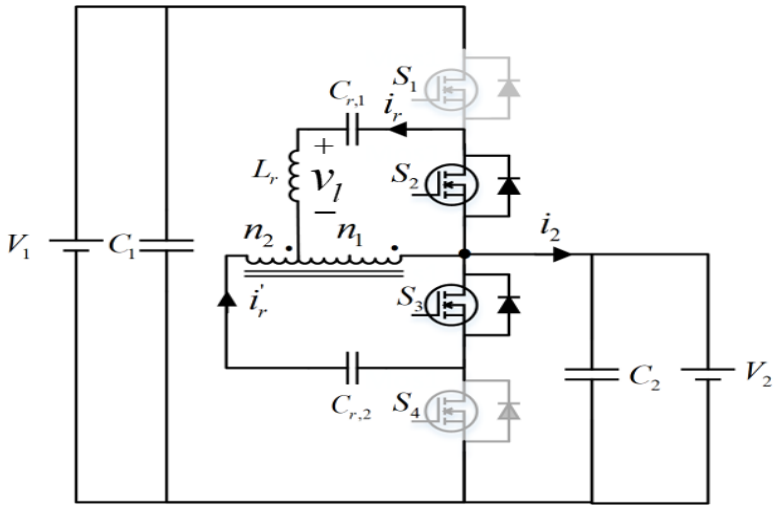



**Figure 3.6** Operating Mode 3

the interval is equal to the duration of mode 1. This is essential for maintaining symmetry of operation. The peak value of the inductor current is equal to the peak current obtained during mode 1 with the operation similar to mode 1.

The current path is through switches $S_2$ and $S_3$. The capacitor voltage for the primary side resonant capacitor is given by $V_{c,r1}=V_{cr1,avg}+\Delta v_{c,r1}$ and $V_{c,r2}=V_{cr2,avg}+\Delta v_{c,r2}$.

The average voltage across the resonant tank as shown in Fig. 3.2 can be obtained as $V_{ab}=0$ and $V_{cd}=0$.

Thus the voltage seen across the resonant tank denoted by $v_r=V_a-V_b$. Since the difference is negligible, the capacitors discharge across the inductor allowing for a linear fall in the current.

- **Mode 4**:

  This mode is identified as region when the leakage inductance sees a negative resonant voltage across it in the polarity as marked in Fig. 3.7. The inductor current magnitude either falls or rises with a small variation or maintains its value depending on the voltage difference seen across the leakage inductance. This value is dependent on the magnitude of $V_1$ and $V_2$. The capacitor voltages invert polarity during this mode. The current path is through switches $S_2$ and $S_4$.

  The average voltage across the resonant tank as shown in Fig. 3.2 can be obtained as $V_{ab}=0$ and $V_{cd}=-V_2$. During this mode The value of current $i_2=i_r'$ due to the conduction of switch $S_2$.

  Thus the voltage seen across the resonant tank denoted by $v_r$ is close to negligible during the condition when $V_1=V_2(1+\frac{1}{n})$ as seen during the analysis for mode 2.

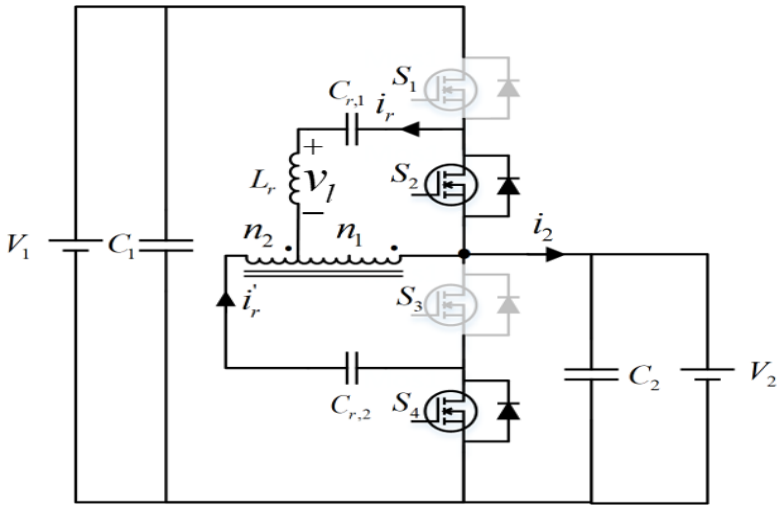



**Figure 3.7** Operating Mode 4

## 3.4 Modulator Design

The modulator for the converter is designed to obtain the required targets of bidirectionality and phase shift control. This is done by controlling the phase angle between two Switches $S_1$ and switch $S_3$. Switches $S_2$ and $S_4$ are driven complementary to the switches $S_1$ and $S_3$ respectively.

The main control element is thus noted to be the phase angle,$\phi$ which can be varied across an output range of [0,2$\pi$] [33]. However, due to converter operation, the total output power is dependent on the area of the current curves during the rectification stages during mode 2 and mode 4. Hence a larger phase angle value results in higher peak current, but there is a reduction in the maximum output power beyond a phase angle of $\pi$. Hence, in order to obtain lower switch losses while maximum power, a peak phase shift value of $\pi$ where the maximum power output for both directions is when the phase difference between the two switches is $\pi$. Based on this, requirement the range of variation for the modulation index, $\phi$ can be obtained as 3.4,

$$\phi \in [-\pi, \pi] \tag{3.4}$$

## 3.5 Converter Design

The converter design involves the design of the resonant tank of the converter[31], [32]. The design is performed starting with design of the transformer including the required leakage inductance values for the transformer. This is followed by the selection of the resonant capacitors based on the required resonant frequency. The resonant frequency is selected to ensure that the converter operates in a current control mode of operation which is only possible if the converter is operating in the inductive mode of operation. Since the resonant tank is in fact a series resonant circuit, the inductive region of operation is ensured by keeping the resonant frequency much lower than the operating frequency.

This section describes in detail the design equations developed in order to obtain the component values for the converter. It has to be noted that a final converter design can be obtained only after a through optimisation process using numerical method based simulation software in order to optimise the design for obtaining the soft switching range and thermal performance. The targets for the optimisation for this design were high efficiency and a soft switching range wide enough to obtain the prior requirement. The primary components which have a significant impact on the soft switching range were identified and then optimised to obtain the high values of efficiency.

### 3.5.1 Transformer Turns ratio selection

The transformer turns ratio is determined by the average voltage stress seen across the primary and the secondary. Assuming phase shift control, the duty period for the switches is maintained to be half the bus voltage values. Thus, a relation between the high and low voltage side voltages denoted by $V_1$ and $V_2$ can be obtained as,

$$\frac{n_p}{n_s} = \frac{V_1 - V_2}{V_2} \tag{3.5}$$

$$\frac{n_p}{n_s} = \frac{n_1}{n_1 + n_2} \tag{3.6}$$

With the required value for the turns ratio between the primary and the secondary sides of the transformer defined, the values for turns ratio for the auto-transformer can be obtained as given by 3.6. The autotransformer allows for current sharing which helps ensure that the total current supplied to the primary side of the winding denoted by $n_1$ is now reduced.

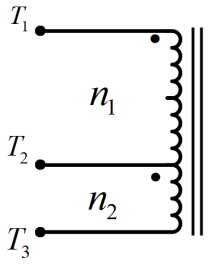



**Figure 3.8** Autotransformer Labelling

The auto-transformer turns are identified as given in Fig. 3.8.

### 3.5.2 Resonant Tank Design

The resonant Tank is designed with an initial starting point being the values of the leakage inductance followed by the selection of a total resonant capacitor value. The value of the capacitors is then obtained from the value selected.

The total power transfer is determined by the leakage inductance of the transformer. Ideally a

smaller inductance leads to large power transfer since a small voltage across the inductor would lead to a large current as given by first principle equations for an inductor. However, the inductor size has to be large enough to be able to store the energy of the output capacitors of the switching power devices which is essential for ensuring soft switching. Based on these requirements the leakage inductance of the transformer can be designed with a detailed derivation of the design equations provided in this section. The magnetising inductance is selected by iterating over values of the inductance to meet the soft switching required in the desired region of operation.

Due to the presence of two inductor values in the converter, the smallest value of inductance i.e. the leakage inductance is used for selection of resonant capacitors. The equations for the selection are presented later in this chapter. The resonant capacitors obtained from the equation serve as the minimal value to be used and can be increased to obtain a the maximum value of leakage inductance which is a requirement for improved soft switching load range.

The transformer magnetizing inductance sizing allows for an extension of the soft switched load.A wider range of soft switching around the operating nominal voltage is possible in this case rather than with just modifications in the leakage inductance. However the value does significantly increase the conduction losses due to increased current. The soft switching range however gradually decreases as the output voltage moves away from the target voltage however and thus there is careful consideration required and an analysis of the profile in order to determine the targeted nominal voltage for design. For the purpose of this design, the value of magnetising inductance is assumed to be large.

#### 3.5.2.1 Leakage inductance selection

The series leakage inductance of the transformer is used to obtain the required power requirements of the converter with the range of soft switching extended by selection of the leakage inductance of the transformer.[34] The converter control is maintained by the use of a simple output voltage to phase shift PI control loop which regulated the converter current to maintain the required voltage levels across the output. However in order to ensure such a control is possible, the resonant circuit must be designed for a frequency which is lower than the switching frequency in order to keep the converter is operated in the inductive zone. The SCRC also suffers from low inductor current during low power output, which is solved by placing the inductor on the side of the transformer with a higher current. With such a design approach, the range where the soft switching can be achieved is increased allowing for better efficiency over a larger range of power for a fixed voltage range.

In order to obtain the value of the leakage inductance[35], two operating modes are identified around the nominal design voltages. Hence, the equations for the two cases can be identified by 3.7 and 3.8 where N=1+1/n.

- ($V_{in}$>$V_{out}N$)

$$L_r = \frac{N((V_1 - V_2)^2 - (V_2/n)^2)^2}{64 I_2 f_{sw} (V_1 - V_2 N)(V_1 - V_2)^2} \tag{3.7}$$

- ($V_{in}$<$V_{out}N$)

$$L_r = \frac{N((V_2/n)^2 - (V_1 - V_2)^2)^2}{64 I_2 f_{sw}(V_2 N - V_1)(V_2/n)^2} \tag{3.8}$$

The maximum value obtained from 3.7 and 3.8 is used to determine the value of leakage inductance to be used for the design. However the value of the leakage inductance is not enough to meet the soft switching requirement as derived in the section below, hence the value of the desired leakage inductance is selected to be at least double the value obtained here. The value obtained serves as an initial point for design and can be increased by optimising the value for increased soft switching range.

#### 3.5.2.2 Resonant Capacitors

In this design there are two inductances that can influence the resonant frequency, the leakage inductance $L_r$ and the magnetizing inductance $L_m$[36]. This results in two resonant frequencies for a fixed value of capacitance $C_r$ denoted by $f_{r,1}$ and $f_{r,2}$ respectively. The value of the lumped resonant capacitance can thus be obtained by,

$$f_{r,1} = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{3.9}$$

With the lumped value for the capacitors obtained, the individual resonant capacitor values, $C_{r,1}$ and $C_{r,2}$ can be obtained by the equations 3.10,

$$C_r = \frac{C_{r,1} C_{r,2} n^2}{C_{r,1} + C_{r,2} n^2} \tag{3.10}$$

### 3.5.3 Power Switch Ratings

The switch selection is performed to meet the high efficiency requirements. The voltage ratings for the switches is selected through the voltage seen across the bus. The high side switches see a voltage given by $V_{top}$=$V_1$-$V_2$ while the low side switches have a voltage given by $V_{bot}$=$V_2$. The RMS current requirements for the devices are similarly obtained based on simulation results for the converter. The second requirement for the switch selection is bidirectional current with unidirectional voltage blocking since the device has to conduct current in both directions in order to ensure bidirectional operation.

The selection of power switches based on the given requirement is however specific to this operation. If the low side voltage has to be maintained by the converter, the high side switches should be rated at the high side voltage $V_1$. It has to be noted that only the body diode is used in this design to obtain soft switching. In order to reduce conduction losses, it is recommended to utilise a parallel connection of MOSFETs since that ensures reduced current due to current division. The paralleled devices are driven by the same drive signal. It is easier to parallel MOSFETs. Essentially, when the gate signals are applied, each device is has minor vairations in the on state resitance

due to which the current values will be different. However as the converter operates, the device carrying higher current heats up as a result of which the on state resistance increases. This change in resistance allows for redistribution as the converter keeps operating allow for a natural balancing of the device currents.

### 3.5.4 Input and Output filters

The input and output filter design is done using capacitor only filters to ensure bidirectionality, the use of additional inductive elements for a second or higher order filter would be ideal but would add additional complexity to the filter design. Hence a simple capacitor based filter is selected with the design goal of minimal voltage variation[37]. Since the resonant network is in fact a series resonant circuit an output capacitor which can be charged by the rectified resonant current makes sense for this design.

The criteria for design is derived from first principles for a capacitor, the voltage variation for a fixed output variation of is used against a calculated average current which is assumed to be supplied completely by the capacitors. Hence, the capacitors can be selected by the equations below:

$$C_{in}\delta V_{in} = I_{in} D T_{sw} \tag{3.11}$$

$$C_{out}\delta V_{out} = I_{out} D T_{sw} \tag{3.12}$$

where D is the duty period of the square wave current and $T_{sw}$ is the switching period. With the values for the resonant capacitors selected, the capacitor is modelled in PLECS and the value of the RMS current through the capacitors is used to obtain the RMS current requirement of the capacitors. The electrolytic capacitors are used to maintain the voltage requirements with ceramic capacitors required to meet the current and filtering requirements. Film capacitors are also connected in parallel to meet the sudden turn on high current requirement and also another filtering for high frequency noise, the filtering is obtained as a results of the lower ESRs of the capacitors.

#### 3.5.4.1 Transformer Design

The transformer design for this circuit serves two purposes, the first one being the conversion of voltage range from the rated half of the input dc value to the required output voltage level and also to provide the required leakage inductance. The second requirement is the leakage inductance offered by the winding air gaps. The value of leakage is essential as it is related to the maximum power transfer possible along with the soft switching range. Designing such a transformer for a high efficiency circuit poses an additional challenge as the total power losses for the transformer have to kept as low as possible in order to obtain the targeted efficiency values. Hence a high efficiency transformer design [38] is used with a special core material selected for the operating range. Such a design approach is targeted to fully utilise the benefits of negligible switching losses the resonant converter design offers.

The design of the transformer uses the core N87 ferrite with winding around the core using Litz wire for obtaining the maximum values of efficiency. The parameters defined by the manufacturer used for the design of the transformer core is set as given in the table (table). The various parameters used for the design calculation are dependent on the core design and the material selected for the core.

The design of the transformer is done with the kgfe method of transformer design [39], where in the design of the transformer is performed keeping in mind the overall power losses. The selection of the core material and core type is done over several iterations where different core types which meet the required minimum kgfe value are tested following which the the number of turns are iterated until the power loss requirements are met.A detailed design process for different core types and changes made over each iteration is described below.

$$n = \frac{\lambda}{2\Delta B A_c} 10^4 \tag{3.13}$$

The number of turns are calculated based on the value of the total volt-sec,$\lambda$ calaculated against the flux density and crossectional area for the core as given in equation 3.13.

Once the turns ratio is obtained, for the primary side, the secondary side turns ratio can be estimated by multiplying the value obtained for the primary with the value required for the secondary winding. The optimisation objectives for this case is to have minimum number of turns across core so as to reduce the total copper losses while ensuring the core losses are maintained low by ensuring a low total flux variation. A detailed design is provided later in this thesis.

## 3.6 Summary

The chapter discussed the operating modes utilised for bidirectional power transfer along with the modulation required to maintain the dersired operating condition. The principle of opeartion that was used as the basis for the design is also considered here which is the main methodology used to maintain phase shift modulation with reduced switches. In addition, the design process and design targets for which the component values are selection is also detailed in this section in order to describe the overall design process and the optimisation targets.

CHAPTER

# 4

# SOFT SWITCHING BEHAVIOR

## 4.1 Introduction

This chapter discusses the soft switching behavior of the converter during the transitions between each mode. A detailed analysis of the conditions required to obtain soft switching will be discussed along with identification of the ZVS range of the design as well as the range of ZVS for a converter design.

With an explanation of the bidirectional power flow and how the same is introduced in the proposed converter design, an emphasis is laid on the benefits of such a power flow which is mainly related to the soft switched transitions observed in the converter. An analysis of the benefits of soft switching along with the idea of how soft switching can be approached for a design will be discussed in this chapter.

## 4.2 Soft Switching fundamentals

Soft switched transitions for power switches allow for reduced losses and heating. This has benefits in terms of reduced size of the heat sink used for heat dissipation of the power devices and better thermal management. This allows for smaller converter designs allowing for higher power density [39]. As a result there has been a lot of focus on designing converters which can obtain higher efficiency through soft switching. For brevity sake, the discussion for this is limited to switching losses in the case of power MOSFETs. In hard switching transitions, total losses in the power switches can be classified as:

- **Conduction losses**: The total conduction losses are obtained as a results of the heating generated when the device is conducting. This loss is directly proportional to the square of the RMS current through the switch can be obtained as a sum of the total current squared multiplied by the on state resistance of the device.

$$P_{sw,cond} = I_{sw,rms}^2 R_{ds,on} \tag{4.1}$$

  In order to have a better estimate of the total conduction losses, the losses are estimated using the thermal resistance at the maximum operating temperature since during normal operation, the heating across the device would lead to an additional increase in the temperature.

- **Switching losses**: The total switching losses in a transition can be further subdivided as turn on losses and turn off losses. These are a significant portion of the total switch loss and increase significantly with an increase in operating switching frequency. The turn on loss can be estimated based on the area obtained under a turn on transition. An estimate for the turn on and turn off losses can be obtained however based on the datasheet details for a given operating condition,

$$P_{sw,turn-on} = \frac{E_{on} V_{bus} I_{sw,on} f_{sw}}{I_{test} V_{test}} \tag{4.2}$$

  Similarly, the turn off losses are the area of the obtained for the turn off transition and are affected by the frequency as well. The estimation of turn off losses can be done from values obtained in the datasheet as given below,

$$P_{sw,turn-off} = \frac{E_{off} V_{bus} I_{sw,off} f_{sw}}{I_{test} V_{test}} \tag{4.3}$$

  The details for the terms used in equation 4.2 is listed as follows:

  - $E_{on}$ : Turn on energy loss for test voltage.
  - $E_{off}$ : Turn off energy loss for test voltage.
  - $V_{bus}$ : Nominal operation bus voltage across switch.
  - $I_{on}$ : Device current at the time of turn on.
  - $I_{off}$ : Device current at the time of turn off.
  - $f_{sw}$ : Operating frequency of the device

Hence based on the estimates shown it is evident that the switching losses are an optimisation target if the switching frequency has to be increased since higher switching frequencies offer benefits such as reduction in volume of the overall converter due to reduction in the size of magnetic and capacitive elements.

If the bus voltage across the device at the time of turn or the switch current can be maintained close to zero, a zero voltage or zero current switched transition can be obtained for the device.

## 4.3 Soft Switching Transition Analysis

The current polarity inversion across each switching period allows for reduced switching losses by allowing for Zero Voltage Switched(ZVS) Transitions. This section details the soft switched transition between each mode of operation.

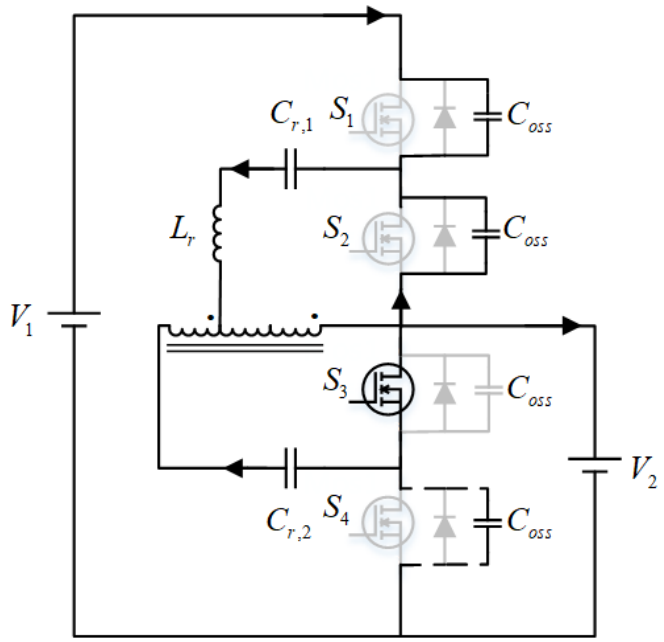



**Figure 4.1** Transition from Mode 4 to Mode 1 (a)

- **Transition from Mode 4 to Mode 1 -a** During this mode the converter transitions from the negative resonant mode marked by switches $s_2$ and $S_4$ turned on to the charging mode where the switch $S_2$ turns off and $S_1$ turns on. The current is in the direction as shown in Fig. 4.1. The figure shows the point where the gate signal has just been turned off for $S_2$ and the gate signal for $S_1$ is still low. This interaction takes place during the dead time between the two switches. Since $S_1$ was previously on, the device voltage across the output capacitance is close to 0 whereas the device voltage across $S_2$ is a value which is the difference between the high and low side bus voltages. Since the MOSFETs are not in conduction mode, the current needs a path to conduct and thus charges the output device capacitance for $S_1$ whereas it discharges the output capacitance for device $S_2$.

- **Transition from Mode 4 to Mode 1 -b**

  This transition occurs when the device output capacitance for $S_2$ has been completely discharged and the blocking voltage is now supported by the output capacitance for $S_1$. The output capacitance across $S_2$ is not completely discharged and thus the current needs a path

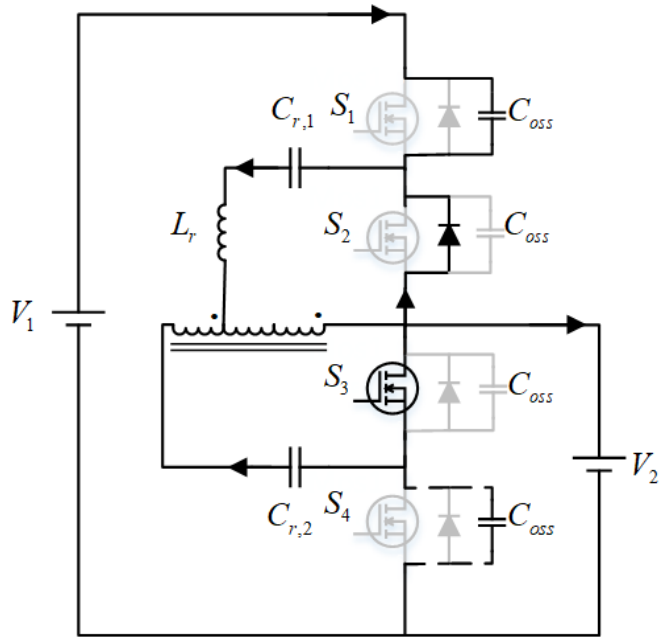



**Figure 4.2** Transition from Mode 4 to Mode 1 (b)

to conduct. Similarly the output capacitance for $S_1$ is completely charged and the device $S_1$ stops conducting and the device completely turns off. Now if the current magnitude is still in the same direction and the dead time is enough, the body diode starts conducting as the current needs a path to conduct. This requires the current flowing through the body diode which clamps the voltage to a value close to zero before the gate signal for $S_2$ has arrived. Since the voltage is almost zero, the device can turn on with Zero Voltage reducing the turn on losses which are directly proportional to the bus voltage to almost a negligible quantity.

- **Transition from Mode 4 to Mode 1 - c**

  This transition is marked by the gate signal crossing the minimum threshold required to turn on the MOSFET. Since the voltage across $S_2$ has already been clamped to a zero, the device turn on can take place with minimal transition losses since there is no stored charge in the MOSFET. This allows for the device turn on at significantly lower turn on energy dissipation and can thus have significantly reduced heating across the device. This turn on has been shown in Fig. 4.3 which shows the device turn and the associated current directions during this transition.

## 4.4 Soft Switching Requirements

Soft Switched ZVS turn on is possible if the current magnitude before turn on is large enough to ensure completed discharge of the stored energy in the devices. The second factor that is essential to ensure ZVS is the dead time duration. If the current magnitude is small, a longer dead time results

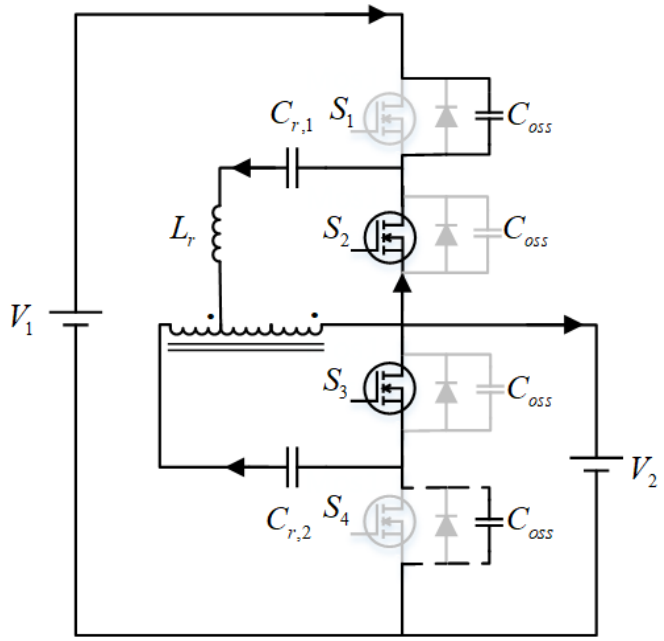



**Figure 4.3** Transition from Mode 4 to Mode 1 (c)

in current reversal which forces the current direction to change returning the previously conduction body diode to a non-conducting mode. Furthermore, the reverse current can now charge the device capacitance causing energy to be stored in the device similar to when the device is in blocking mode. This requires careful attention to the value of the dead time especially for lighter loads. Based on these factors[40][41][42], the minimum requirements for ensuring complete zero voltage turn on which can be determined. The minimum current at the time of device turn on is identified in order to estimate the major components involved in the current transition, followed by an estimation of the minimum dead time required to obtain completely soft switched transitions.

- Minimum Turn on current: The minimum requirement for a soft switched turn on can be understood by estimating the maximum energy that can be stored in a device when in blocking mode. This data is typically available in terms of the output capacitance in the device datasheet and is used for analysis. The device can be modelled as a capacitor when no gate signal is applied which charges to the blocking voltage. Thus, assuming the resonant capacitors to be large enough to act as voltage sources during the dead time transitions, the minimum current required for complete ZVS can be identified by analysing the energy balance between the output capacitances of the complementary devices and the leakage inductance. This can be analysed analytically as shown below,

$$E_L \geq 2E_{sw,turnon} \tag{4.4}$$

$$\frac{1}{2}Li^2_{turnoff} \geq C_{oss}V^2_{bus} \tag{4.5}$$

$$I_{min} \geq V_{bus}\sqrt{\frac{2C_{oss}}{L_r}} \tag{4.6}$$

Solving 4.6 the minimum turn off current equation can be derived to ensure the devices are soft switched. This value is different for both the top and the bottom side switches with the equations for both the sides identified as

$$I_{min,top} \geq V_1 - V_2\sqrt{\frac{2C_{oss}}{L_r}} \tag{4.7}$$

$$I_{min,bot} \geq V_2\sqrt{\frac{2C_{oss}}{L_r}} \tag{4.8}$$

It can be observed from the analysis that the value of inductance significantly determines the minimum current required for complete turn off. Hence a larger value of leakage would help improve the soft switching range. However, the leakage inductance size is also essential for power transfer and thus a larger leakage would result in larger values of phase shift required for the same amount of power transfer limiting the maximum output power. Thus, the first optimisation opportunity can be identified here as the value of the leakage inductance that is required to obtain the minimum turn on losses.

- Dead Time:

  Another important factor which determines the soft switching behaviour is the dead time applied between turn off of a device and turn on of the complementary device. This can be analysed by understanding the converter operation during the transition. The circuit can be assumed to be completely inductive during this period since the capacitors are large enough to act as voltage sources during short intervals. Thus the current during a transition can be obtained as,

$$i_r(t) = I_D\, cos(\omega_s t_d) \tag{4.9}$$

  where, $\omega_s = \frac{1}{2L_rC_r}$ and $I_D$ is the current magnitude at the time of turn off. The minimum time required to completely discharge the output capacitance can thus be obtained as,

$$v_{cr}(t) = \frac{1}{2C_{oss}}\int i_r(t)dt \tag{4.10}$$

  Solving 4.10 for $v_{cr} \geq 0$ can be obtained for when the value of $t_{d,} = \pi/2\omega_s$.

  Hence the minimum values of dead time for the top and the bottom switches can be obtained as

$$\omega_{s,top} = \frac{1}{\sqrt{2L_rC_{oss}}} \tag{4.11}$$

$$\omega_{s,bot} = \frac{1}{\sqrt{2n^2L_rC_{oss}}} \tag{4.12}$$

The values for the top and bottom side dead times can be substituted into the dead time equations to obtain the dead time values required to obtain soft switched transitions for top and bottom side switches.

## 4.5 Summary

The chapter discussed the soft switching transitions that allow for ZVS turn on of the devices. This chapter also discusses the minimum conditions required to obtain a soft switched transition with the main factors for the requirement having been obtained as the leakage inductance of the transformer and the dead time between complementary switches. The requirements obtained from the converter soft switching requirements can be used to identify the minimum current required for each voltage level to determine the soft switching behaviour for a particular power output.

CHAPTER

# 5

# CONTROL DESIGN

## 5.1 Introduction

This chapter discusses the controller design process used to obtain a bidirectional average current control for the design. An average current control is used to simplify the control design process as for an average current the modulator control is directly proportional to the magnitude with the frequency response of any change dominated by the frequency response of the LPF.

The equations derived in B are used to obtain a gain term for the modulator control term to the output current magnitude followed by the gain term of the controller. The control loop is designed using a PI compensator which is used to a high bandwidth while still maintaining high phase margin.

## 5.2 Control Design Objective

The converter operation is bidirectional with the modulator design being linear for both positive and negative value. Thus, the main objective of a controller for such a bidirectional power transfer is to ensure that the response is stable and doesn't have any major variations as the power transfer command changes from a positive to a negative value. The small signal model for the converter can be derived utilising an approach that is performed for a hybrid dual active bridge converter since conventional averaging approaches with a small signal approximation of perturbations will not be accurate. The reason for this is that the current average during each period is negligible making the perturbations much larger than the averaged bias point. Hence, the small signal modulation should account for this in order to obtain a model which account for the effect of small signal variations in the control command which in this case will be the modulator phase angle.

Due to this limitation a simpler control scheme is utilised to obtain control over the reference value and the ensure operation is stable. This is done by utilising a current control scheme which is known to reduce the order of the plant function hence making controller design possible with a simple PI compensator. Inherent current limiting is possible in this case to ensure the converter design

## 5.3 Control Loop Design

The control loop is designed in order to ensure the converter control is bidirectional and stable in both directions of power transfer. In order to obtain this control and to reduce the complexity of the control loop, an averaged current control is established where the low side current,$I_2$ is monitored. This quantity is then averaged and compared to a reference command. The compensator then operates on the error between the command and the measured value in order to generate the phase shift command which is then used by the phase shift modulator which drives the gate signals for the MOSFETs.

For the purpose of this thesis, the reference command for the current loop is a constant quantity generated as the required power command divided by the output voltage of the low side bus voltage. However, depending on the requirement, this quantity can either be generated by a lower bandwidth voltage loop or an external command generator.

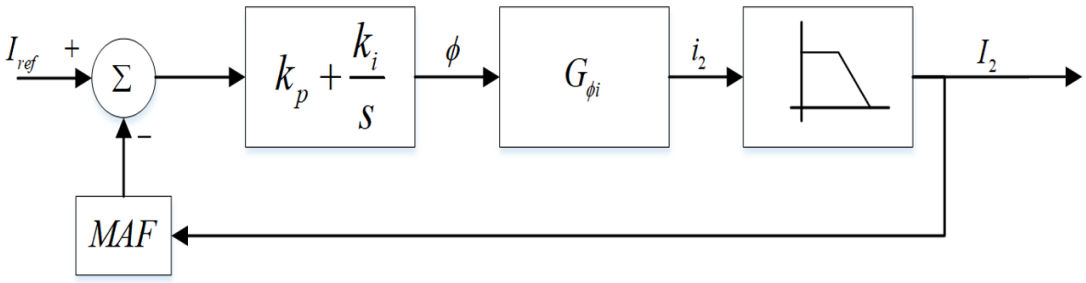



**Figure 5.1** Control Blocks

### 5.3.1 Current measurement

The current measurement is performed near the ESS denoted by voltage source $V_2$ since the power delivered to and from the battery energy storage system is the main focus of the control. The current $i_2$ thus obtained is then averaged using a LPF filter with a cutoff frequency as low as can be obtained on hardware. Thus,a cutoff frequency of 10kHz is used for the design of the LPF. The average current is further filtered using a Moving average filter with a sampling frequency of more than double the LPF selected to be 50 kHz for the given design. The output of the moving average filter is the final

sensed quantity.

### 5.3.2 Control to average current magnitude relation

Based on the current equations as derived in Appendix B, the average current across the low side bus voltage can be obtained by solving the set of equations as given in Appendix B.

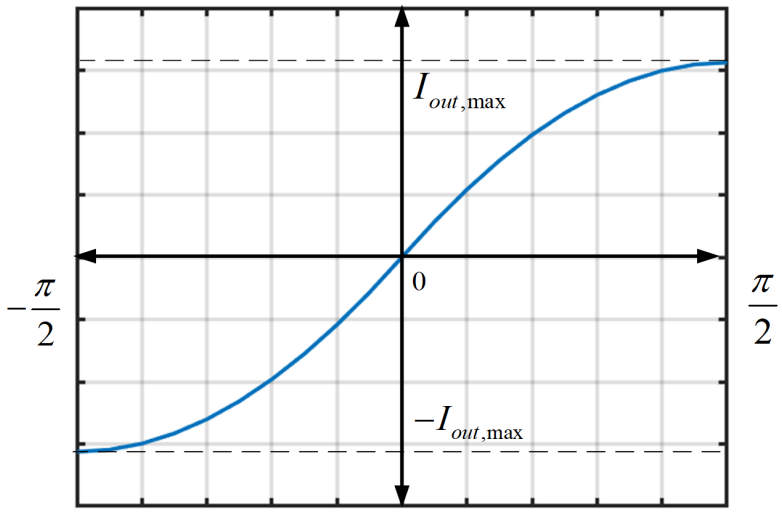



**Figure 5.2** Phase angle to Average Current Relationship

Upon substituting the values for the component values for given prototype a normalised waveform for the phase shift to average current output can be obtained which is used to determine the average slope for the converter phase angle to average current can be obtained. It can be observed that the phase angle does vary as the voltage gain changes from 1 as shown in 5.2. It has to be noted that the value of M=$\frac{V_2 N}{V_1}$ where N=1+1/n with n being the turns ratio such that $n_p$:$n_s$=1:n.

It can be observed that the control is symmetrical around the design voltage for which the gain of the slope is calculated and used to obtain the gain for the block between the phase shift and the instantaneous value of current.

### 5.3.3 Compensator design

The converter loop gain is modelled as a constant value set by the gain between the phase shift modulation command $\phi$ and the average peak value of the converter. The average gain however is an approximation and thus there are minor variations in the control to command magnitude. The uncompensated loop gain frequency response for a loop gain shown in Fig. 5.1. The uncompensated loop gain of the converter is obtained with the loop gain between the phase command $\phi$ and the

peak output current modelled as constant gain with the values for the gain obtained by plotting the curves for phase shift versus the output current magnitudes.

The transfer function for the low pass filter is modelled as,

$$T_{s,lpf} = \frac{1}{\frac{s}{\omega_l} + 1} \tag{5.1}$$

The uncompensated loop gain frequency response for the control can be obtained as Fig. 5.3. This is used to estimate the gain and low frequency poles for the compensator.

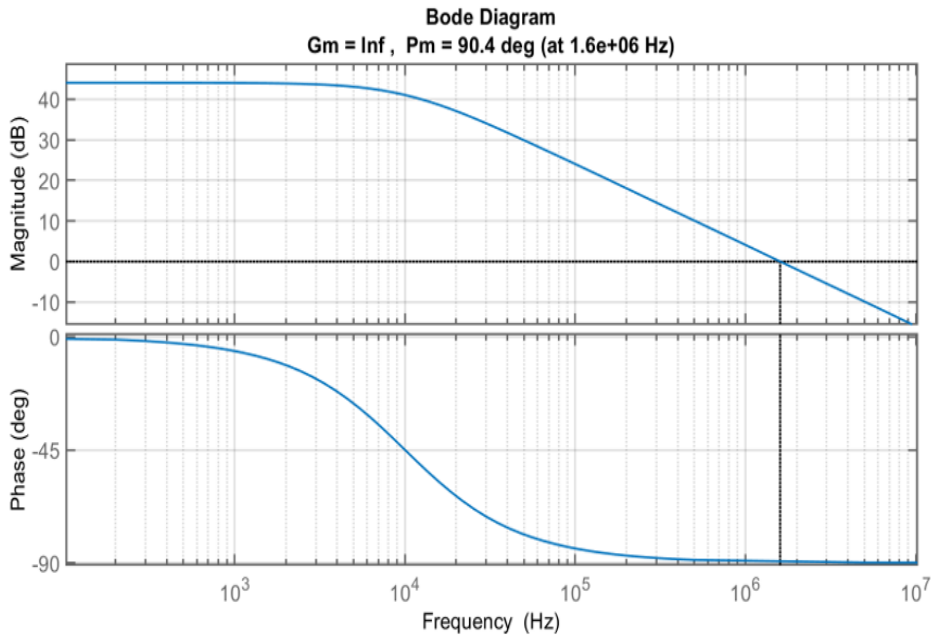



**Figure 5.3** Uncompensated Loop frequency response

A PI compensator can be designed around this point by selecting the PI compensator zero located at a frequency $f_l$=2kHz and gain, $K_p$=0.03. Thus the compensated loop can be obtained as Fig. 5.4. The final compensator response is verified in the final simulation level verification.

## 5.4 Simulation verification

The control loop designed as defined in Chapter 5 is verified against simulation results in order to verify the bandwidth of the control loop. The control design verification is performed for a variation of command reference from a positive reference command to a negative reference command. The low side bus voltage is maintained around the design value of $V_2$=555 V. The main targets for the verification are the bandwidth around the design point, the bidirectionality of the converter control design and the stability of operation across the entire operating range.

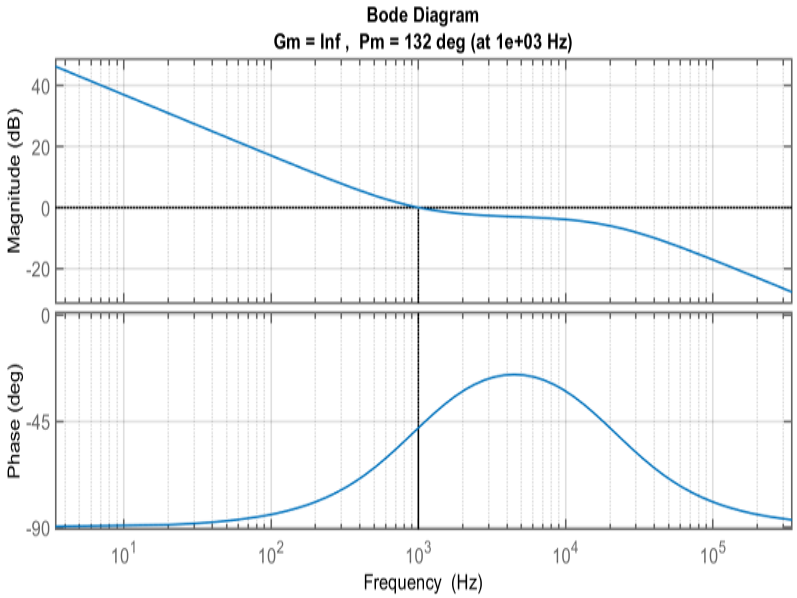



**Figure 5.4** Compensated Loop frequency response

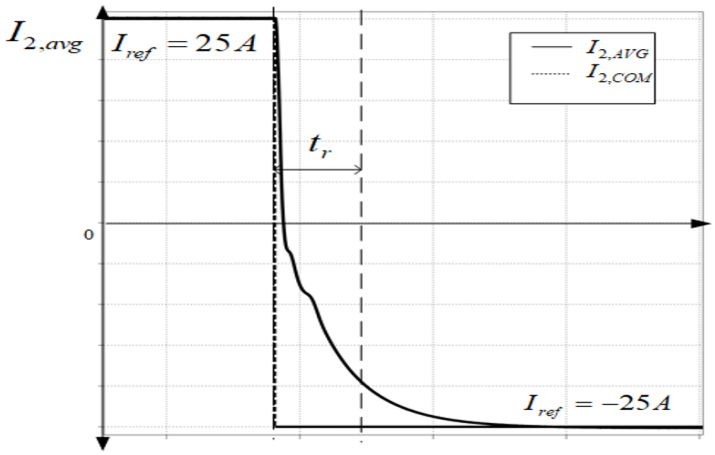



**Figure 5.5** Controller Response

## 5.5 Summary

The chapter discusses in detail the converter control design and the objectives that are set for the converter design. There are several opportunities possible in the control design for a more robust control loop however the thesis focuses on just a current loop control to ensure that the requirements for bidirectional power transfer is met while ensuring converter stability across the entire operating range. The control design here is still an approximation based approach where the gain term between the phase angle and the average current magnitude is approximated since the deviation for different gains is not too large.

CHAPTER

# 6

# PROTOTYPE DESIGN

## 6.1 Introduction

This chapter discusses the component selection performed for the prototype converter design against the equations defined in Chapter 3 followed by optimisation of the values to obtain a larger soft switching range as described in Chapter 4. The final values and part numbers of the components used are provided in this section. The values of the converter components are estimated analytically along with equations provided for the verification to be used for ensuring the simulation results meet the expected performance values.

Commercially available components are selected and modelled in the simulation to estimate the performance of the converter hardware response which . Thermal models parameters are obtained against device datasheet however for an analytical verification of obtained simulation results, equations are described in this chapter used to evaluate the accuracy of the thermal modelling. Transformer losses are estimated based on the RMS currents across the windings and core losses obtained against expected core losses for N87 material datasheet. These are used to estimate the total losses in the converter design to obtain an estimate of the targeted efficiency of the converter.

## 6.2 Converter Component Selection

: The converter components are selected based on a combination of theoretical design equations as obtained in Chapter 3 and values obtained from simulation results which are used to design the converter. The converter design specifications used for the design are selected around the targeted application as given in Chapter 1. The converter specifications used for a prototype design for this

**Table 6.1** Converter Design Specifications

| Specifications | Value |
|---|---|
| DC Microgrid Bus Voltage, $V_1$ | 1000 ± 10 V |
| ESS Bus Voltage, $V_2$ | 480-600 V |
| Max Output Power, $P_{out}$ | 30 kW |
| Switching Frequency, $f_{sw}$ | 200 kHz |

thesis are presented in 6.1.

Based on the design specifications, the converter design can be performed. As defined in Chapter 3, the converter design is performed by first selecting the transformer turns ratio followed by the resonant tank design. This is followed by the selection of resonant capacitors, power switches and the transformer. The input and output filters are designed using capacitive filters to ensure minimal bus voltage variation.

### 6.2.1 Transformer Design

The turns ratio selection is the first starting point which determines the voltage around which the maximum load range can be soft switched. The turns ratio can be selected using 3.5. Selecting a voltage in the around the middle of the ESS Side voltage variation as a nominal voltage for design, the turns ratio can be calculated as,

$$\frac{n_p}{n_s} = \frac{1}{n} = \frac{1}{1.25} \tag{6.1}$$

The values for the turns ratio of the auto-transformer can now be obtained using 3.6 as, $n_1$:$n_2$=1:0.25. This is used as a starting point for the transformer design. A core material of N87 is selected since the operating frequency is 200kHz.

Leakage inductance of the transformer is selected by selecting the maximum value of the values obtained by substituting the value of the turns ratio obtained in 6.1 in 3.7 and 3.8. The value obtained is the minimum value required to meet the output power requirement. The soft switching requirement requires a larger value of leakage inductance. Upon optimising the value of the leakage inductance, a value is selected in order to meet the soft switching requirement and the output power requirements.

Core selection for the auto-transformer is performed by assuming the transformer to be two windings shorted at a common point. The transformer specifications can thus be listed for the peak variations in the component values as given in 6.2 and 6.3. This allows for two operating points around which the worst case current and voltage stress will be obtained across the transformer. The second condition that is essential for core selection is the maxum flux density variation across the transformer core. Since the peak flux density variation directly impacts the total core losses in the transformer, the core selection and the turns selection is performed by iterating against these requirements. The third condition that is considered for the selection of the core is the overall

**Table 6.2** Transformer Design Specifications at $V_2$=600V

| Specifications | Value |
|---|---|
| Primary Side Peak Average Voltage, $V_{1,avg}$ | 260 V |
| Secondary Side Peak Average Voltage, $V_{2,avg}$ | 65 V |
| Primary Side RMS Current, $V_{1,avg}$ | 16 A |
| Secondary Side RMS Current, $V_{2,avg}$ | 60 A |
| Switching Frequency, $f_{sw}$ | 200kHz |

**Table 6.3** Transformer Design Specifications at $V_2$=480V

| Specifications | Value |
|---|---|
| Primary Side Peak Average Voltage, $V_{1,avg}$ | 200 V |
| Secondary Side Peak Average Voltage, $V_{2,avg}$ | 50 V |
| Primary Side RMS Current, $V_{1,avg}$ | 25 A |
| Secondary Side RMS Current, $V_{2,avg}$ | 90 A |
| Switching Frequency, $f_{sw}$ | 200kHz |

volume and total losses that can be obtained for the transformer. Since the main target for the design is high efficiency, a slightly lower flux density variation is considered to allow for lower losses across the transformer.

The wire size is then calculated by ensuring the total winding area is well within the maximum limit set by the coil former area available. The magnetising inductance is calculated for the primary side of the transformer by,

$$L_m = \frac{\mu n_1^2 A_c}{l_m} \tag{6.2}$$

The transformer core selected along with the details of the core parameters and winding details is presented in 6.4. Based on the core dimensions, a coil former is selected around which the wire has to be wound. The value of cross-sectional area is obtained from the datasheet and drawings of the coil former. The total winding area for CP-E65/32/27-1S can be obtained as 435 $mm^2$. Since the maximum value of winding area is now defined, the maximum wire gauge can be selected for the design in order to reduce the total losses across the winding. The total width of the coil is then verified by ensuring that the total height of the completely wound core can be wound around the core with enough margin. Since the operation of the transformer is around 200kHz, litz wire is used to ensure the copper losses in the transformer are reduced. The leakage inductance of the transformer would require experimental verification and is thus not calculated here.

$$P_{tf,copper} = I_{rms}^2 R_s \tag{6.3}$$

The losses for the transformer can be identified as the sum of the core loss and the copper loss.

**Table 6.4** Transformer Design Details

| Specifications | Value |
|---|---|
| Core Part Number | B66387G0000X187 |
| Coil Former Part Number | CP-E65/32/27-1S |
| Core Type | EE 65/32/27 |
| Core Material | N87 |
| Mean Length per Turn,MLT | 130 mm |
| Primary Side Wire Gauge | AWG 14 |
| Secondary Side Wire Gauge | AWG 14 |
| Bobbin Winding Area,$W_A$ | 675 $mm^2$ |
| Cross-sectional Area,$A_c$ | 529 $mm^2$ |
| Window Area,$A_c$ | 430 $mm^2$ |
| Number of primary windings,$n_1$ | 12 |
| Number of secondary windings,$n_2$ | 3 |
| Magnetising Inductance,$L_m$ | 5.7 µF |
| Primary Side resistance,$R_1$ | 9.3 mΩ |
| Primary Side resistance,$R_2$ | 2.3 mΩ |
| Magnetising Path Length, $l_m$ | 147 mm |
| Magentising Inductance, $L_m$ | 1.2 mH |

**Table 6.5** Resonant Capacitor Specifications

| Specifications | Value |
|---|---|
| Primary Side Max working Voltage, $V_{cr,1}$ | 600 V |
| Primary Side Max RMS Current, $I_{cr,1}$ | 120 A |
| Secondary Side Max working Voltage, $V_{cr,2}$ | 600 V |
| Secondary Side Max RMS Current, $I_{cr,2}$ | 90 A |

The transformer core loss value is determined based on the losses that would be obtained for the peak flux density that would be obtained for the transformer operation. This value is then add to the copper losses estimated for the transformer operating at a temperature of 100°. The winding resistances are estimated from the wire.

### 6.2.2 Resonant Capacitor

The resonant capacitor for the primary and secondary size are selected to meet the high current requirement of the resonant capacitors. Since, the current requirement is high, film capacitors are selected since the ESR for these type of capacitors is low. Another reason for the selection is the high current handling capability of the selected part numbers. The value for the resonant capacitors is selected based on 3.9 and 3.10. The selection criteria for the capacitors is obtained based on the simulation results. The specifications for the capacitors is listed in 6.5.

**Table 6.6** Resonant Capacitor Value

| Designation | Part Number | Value | Connection(Series-Parallel) |
|---|---|---|---|
| $C_{r,1}$ | 474PMB302KA | 0.47 µF,3000 V | 2-7 |
| $C_{r,2}$ | 474PMB302KA | 0.47 µF,3000 V | 2-6 |

**Table 6.7** Power Switch Specifcations

| Specifications | Value |
|---|---|
| High Side maximum bus voltage, $V_{sw,1}$,$V_{sw,2}$ | 520 V |
| Low Side maximum bus voltage, $V_{sw,3}$,$V_{sw,4}$ | 600 V |
| High Side Max RMS Current, $I_{sw,1}$,$I_{sw,2}$ | 80 A |
| Low Side Max RMS Current, $I_{sw,3}$,$I_{sw,4}$ | 65 A |

The resonant capacitor is selected to be 0.5 times the switching frequency, $f_{sw}$=200 kHz which can be obtained as $f_r$=100kHz. The value can be increased further however a higher value limits the maximum power that can be delivered by the converter since a large portion of the current is used to charge the resonant capacitors.

In order to meet the current requirement film capacitors are selected and arranged in series and parallel combination in order to meet the peak current requirements due to their low ESR and high current handling capacity. The combinations are presented in 6.6.

## 6.3 Power Switches

The power switches are selected to meet the working voltage requirement and the maximum RMS current that has to be handled by the MOSFETs. In addition to this, in order to keep the losses minimum, switches with the least value of on state resistance is selected to ensure minimal conduction losses. This is done not only to ensure minimal losses but also reduced heating across the devices.

**Table 6.8** Switch Parameters

| Specifications | Value |
|---|---|
| High Side maximum Working voltage, $V_{sw,1}$,$V_{sw,2}$ | 700 V |
| Max RMS Current(25°C), $I_{sw,1}$,$I_{sw,2}$ | 140 A |
| Max RMS Current(100°C), $I_{sw,1}$,$I_{sw,2}$ | 140 A |
| Max On state resistance, $R_{ds,on}$ | 19 mΩ |
| Max Junction Temperature, $T_j$ | 175°C |
| Max thermal resistance, $R_{\theta_{j,case}}$ | 0.22 W/°C |

**Table 6.9** Capacitive Filter Specifications

| Specifications | Value |
|---|---|
| Max High Side Working Voltage, $V_1$ | 1000 V |
| Max Low Side Working Voltage, $V_2$ | 600 V |
| High Side maximum RMS Current, $i_{c,1}$ | 17 A |
| Low Side maximum RMS Current, $i_{c,2}$ | 30 A |

**Table 6.10** High Voltage Side Filter

| Capacitor Type | Part Number | Value | Connection |
|---|---|---|---|
| Electrolytic | B43541B8476M000 | 47 µF,600 V | 4 Series |
| Film | R76TN2820(1)H4(2) | 0.082 µF,1600 V | 6 Parallel |
| Ceramic | C2225C104KFRACTU | 0.1 µF, 1600 V | 5 Parallel |

Based on the specifications as listed in 6.7, the switch selected is a MicroSemi MSC015SMA070B. The MOSFET specifications are listed in 6.8. In order to improve total efficiency of the converter, two switches are used in parallel in order to minimise the conduction losses across the switches.

### 6.3.1 Input and Output Filters

The input and output filters are designed based on combinations of electrolytic, film and ceramic capacitors. The electrolytic capacitors with high ESR are used for energy storage whereas the filtering is provided by the combination of film and ceramic capacitors which have much lower ESR values. The capacitors are connected in parallel and series combinations in order to meet the required capacitance values and also to ensure the required RMS rating for the current that has to be supplied by the capacitors is met. The values for the capacitances and RMS current are as described in 6.9.

The input filter is designed based on the combination as presented in 6.10 whereas the output filter is designed by a combination as presented in 6.11.

The effective fiter capacitance as obtained from the combinations is presented in 6.12.

**Table 6.11** Low Voltage Side Filter

| Capacitor Type | Part Number | Value | Connection |
|---|---|---|---|
| Electrolytic | LGN2X101MELC30 | 100 µF,600 V | 2 Series |
| Film | R76QR3470(1)H3(2) | 0.47 µF,1000 V | 5 Parallel |
| Ceramic | C2220X104KDRACAUTO | 0.1 µF, 1000 V | 5 Parallel |

**Table 6.12** Capacitor Parameters

| Specifications | Value |
|---|---|
| High Bus Side Effective Capacitance, $C_1$ | 15 µF |
| Low Bus Side Effective Capacitance, $C_2$ | 53 µF |
| Max High Side capacitor RMS Current, $I_{c,1,rms}$ | 34 A |
| Max Low Side capacitor RMS Current, $I_{c,2,rms}$ | 42 A |
| Max High Side DC Working Voltage, $C_{c,1,max}$ | 1600 V |
| Max High Side DC Working Voltage, $C_{c,1,max}$ | 1200 V |

**Table 6.13** Estimated Switch Losses

| Specifications | Value |
|---|---|
| Total Worst Case Conduction Loss for $S_1$ and $S_2$ , $P_{cond}$ | 105 W |
| Total Worst Case Conduction Loss for $S_3$ and $S_3$ , $P_{cond}$ | 63 W |
| Total Worst Case Switching Loss for $S_1$ and $S_2$ , $P_{sw}$ | 190 W |
| Total Worst Case Switching Loss for $S_3$ and $S_4$ , $P_{sw}$ | 103 W |

### 6.3.2 Heat Sink Selection

The heat sink selection is performed post estimation of the worst case thermal losses. The estimation of losses is performed using an estimation of maximum heat dissipation from the switches as a result of the combination of the conduction and switching losses. The selection of the heat sink is performed to ensure the maximum temperature across the junction of the device does not exceed the maximum value as stated by the device datasheet. Two air cooled heat sinks are used to ensure the device temperature is limited to a value below the maximum junction temperature. The total loss across the MOSFETs can be obtained as the sum of the switching and the conduction losses. The conduction losses are obtained as the average losses due to the RMS current across the on state resistance of the device and the switching losses are due to on and off state current and voltage across the device. Due to the soft switched zero voltage turn on of the devices, the turn on losses are negligible. The only losses that have to be covered thus are the turn off losses. The datasheet for the MOSFET selected provides this value for a fixed point which can be extrapolated to obtain the

**Table 6.14** Max Device Temperature

| Switch | $P_{sw,tot}$ | $\delta T$ |
|---|---|---|
| $S_1$-$S_4$ | 295 W | 90° |
| $S_5$-$S_8$ | 166 W | 50° |

losses for the operating voltage against which the losses can be verified. For the air cooled heat sink, LAM 15 K, the total thermal resistance using a 24 V cooling fan (Kugelgelagert,24 V DC), the total cummulative thermal loss across the switch can be estimated as $R_\theta$=0.25 $^{\circ C}$. The total temperature rise is then estimated by,

$$\Delta T = P_{sw,tot} R_{\theta_{tot}} \tag{6.4}$$

The total thermal increase for the converter design is obtained as given in 6.14. Thus, the maximum junction temperatures for the devices can be estimated for $T_{amb}$=50° as 140 ° and 100 ° for top side and bottom side switches respectively.

$$E_{off} = \frac{V_{bus} I_{sw,turnoff}}{V_{test} I_{test}} E_{off,test} f_{sw} \tag{6.5}$$

$$E_{on} = \frac{V_{bus} I_{sw,turnon}}{V_{test} I_{test}} E_{on,test} f_{sw} \tag{6.6}$$

Based on the equations 6.6 and 6.5, the turn on and turn off losses can be estimated. However since the losses at the time of turn are negligible since the $V_{bus} \approx 0$ V, only the turn off losses are considered.

$$P_{cond} = I^2_{sw,rms} R_{ds,on} \tag{6.7}$$

The conduction losses for the switch can be obtained by calculating the worst case RMS current across the switch using 6.7 for each switch. The total loss across the switch can thus be obtained to be $P_{sw,loss}$=$P_{cond}$+$E_{on}$+$E_{off}$. Based on the equations and utilising the worst case current and turn off current values for each switch the losses for the switches can be used to determine the total loss across the switches for the worst case operating conditions when ESS Bus voltage,$V_2$=480 V as given in 6.13.

### 6.3.3 Power Density Calculation

Based on the cummulative volume of all the components obtained from 6.15, the power density of the converter can be obtained as,

$$\rho = \frac{P_{conv}}{V_{conv}} = \frac{30kW}{3.7L} \tag{6.8}$$

$$\rho = 8.11 kW/L \tag{6.9}$$

## 6.4 Summary

The chapter describes in detail the converter design and the factors used for selecting the final values of the component. The component values obtained in this chapter are then used in Chapter 7 in order to estimate the performance of the converter. In addition to a verification of the converter

**Table 6.15** Component Volume

| Designation | Part Number | Quantity | Volume (in $cm^3$) |
|---|---|---|---|
| Input Capacitor,$C_1$ | B43541B8476M000 | 4 | 6.75 |
| | R76TN2820(1)H4(2) | 6 | 4.77 |
| | C2225C104KFRACTU | 5 | 0.14 |
| Output Capacitor,$C_2$ | LGN2X101MELC30 | 2 | 11.2 |
| | R76QR3470(1)H3(2) | 5 | 19 |
| | C2220X104KDRACAUTO | 5 | 0.07 |
| Transformer | B66387G0000X187with CP-E65/32/27-1S | 1 | 78.65 |
| Winding | AWG 14 | - | 2.23 |
| Heat Sink | LAM 15 K | 2 | 375 |
| Cooling Fan | Kugelgelagert,24 V DC | 2 | 37.5 |
| Resonant Capacitor ,$C_{r,1}$ | 474PMB302KA | 14 | 100 |
| Resonant Capacitor ,$C_{r,2}$ | 474PMB302KA | 12 | 100 |
| MOSFET ,$S_1$-$S_8$ | MSC015SMA070B | 8 | 1.85 |

operating waveforms, additional information is also provided for evaluation of the thermal model for the converter.

CHAPTER

# 7

# SIMULATION AND EXPERIMENTAL LEVEL VERIFICATION

## 7.1 Introduction

This chapter discusses the hardware experimental setup and the tests performed for verification of the converter operation. The overall setup and the waveforms obtained from hardware tests is presented in this section along with a discussion of the results of the waveforms.

A simulation level design of the prototype for the desired application is presented here which describes in detail the converter efficiency model. The simulation is used to obtain a verification of the converter operation, obtain information about the thermal performance of the converter.

The chapter ends with a detailed loss distribution model, and efficiency graphs for the best case and extreme case operating conditions. An optimistic model of converter power density is also derived for the current prototype design.

## 7.2 Simulation Level Verification

In order to determine performance of the converter design before hardware implementation, a simulation level analysis of the converter is required in order to verify derived equations and hardware model. A simulation level implementation also allows for opportunities for optimisation verification by evaluating the effect of variations on the converter design and the related benefits of these changes on the design. An initial design point is obtained using the values and equations derived in the previous sections followed by optimisation in order to increase the soft switching range. Since

the focus is on ensuring high efficiency is maintained, an infinite value of mutual inductance is assumed for the transformer. After the design the value of the mutual inductance can be verified to be in the order of mH and thus can be approximated to be large enough to be ignored in terms of the simulation level design. The next target that is to be targeted is an estimation of the total losses obtained by calculating the thermal losses for the switches and the flux density related core and current related copper losses for the transformer. Since the losses due to the trace and component parasitics are small they have been ignored in this analysis.

### 7.2.1 Converter Design

The simualtion verification is done using two models for obtaining the operational performance of the converter and the thermal model separately. The major distinction between the two is the difference in the switch modelling which for the case of the operational verification is done by modelling the device capacitance as a parallel capacitor across the MOSFET and for the thermal model is the use of the thermal models as avilable in the switch datasheet in order to simulate the thermal behaviour of the device during varying operating conditions.

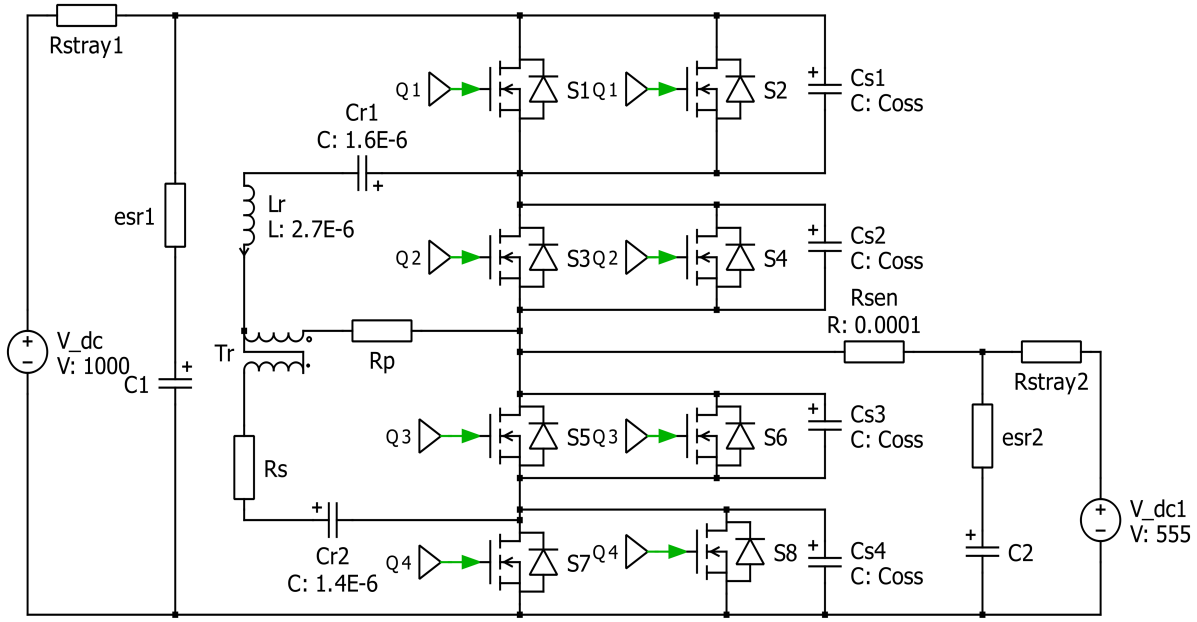



**Figure 7.1** Converter Modelling for simulation verification

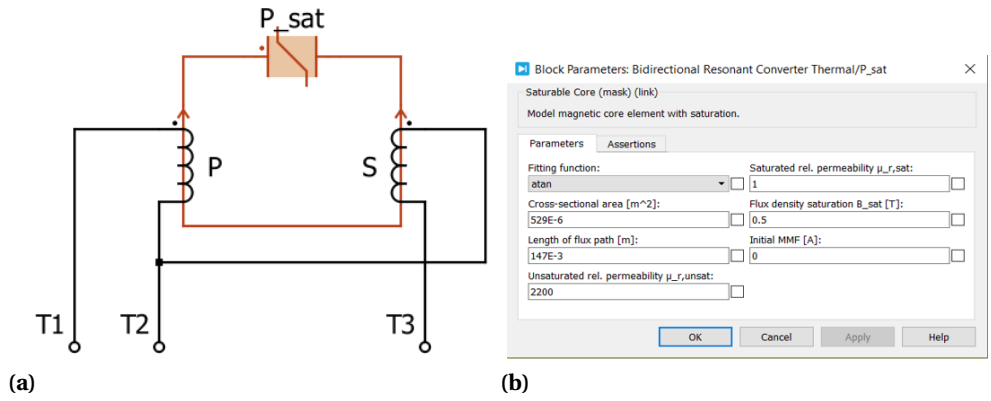
The parameters as listed in 7.1 are used as component parameters for the converter design. With this modelling, the converter optimisation and equation verification is performed in order to obtain a simulation level verification of the converter operational equations. The next step which would be the thermal modelling of the converter components.

The transformer is modelled using only a primary side leakage inductance with series resistances

**Table 7.1** Simulation Design

| Component Designation | Value |
|---|---|
| DC Microgrid Bus Voltage $V_1$ | 1000 V |
| ESS Bus Voltage $V_2$ | 480-600 V |
| Primary Side Resonant Capacitor, $C_{r,1}$ | 1.6 µF |
| Secondary Side Resonant Capacitor, $C_{r,2}$ | 1.4 µF |
| Primary Side winding AC resistance, $R_{ac,1}$ | 10.1 mΩ |
| Secondary Side winding AC resistance, $R_{ac,2}$ | 2.5 mΩ |
| Leakage inductance, $L_r$ | 2.7 µH |
| Input Capacitor, $C_1$ | 15 µF |
| Output Capacitor, $C_2$ | 53 µF |
| MOSFET output capacitance, $C_{oss,1}$-$C_{oss,4}$ | 512 pF |

of the windings presented for both the primary and the secondary sides of the transformer. In order to estimate the core losses, a saturable core is used in order to obtain an estimate of the total variation in the flux density , ΔB. This is then compared with the estimated copper losses for the given operating frequency and maximum flux variation as provided by the manufacturer for the core. This procedure allows for a better thermal loss estimation as compared to an approach utilising the steinmetz equations for loss verification. Core losses can be estimated by obtaining the ac resistance of the wire for the given operating frequency. Since litz wire is used, the variation in the actual resistance obtained for the given operating frequency is limited to around 1.003 times the dc value of the wire resistance. For the purposes of loss estimation, the effective value of resistance at a temperature of 100 °C which is then used for calculation of the copper losses.




**(a)** **(b)**

**Figure 7.2** (a) Transformer Modelling (b) Saturable core value

### 7.2.2 Modulator Design

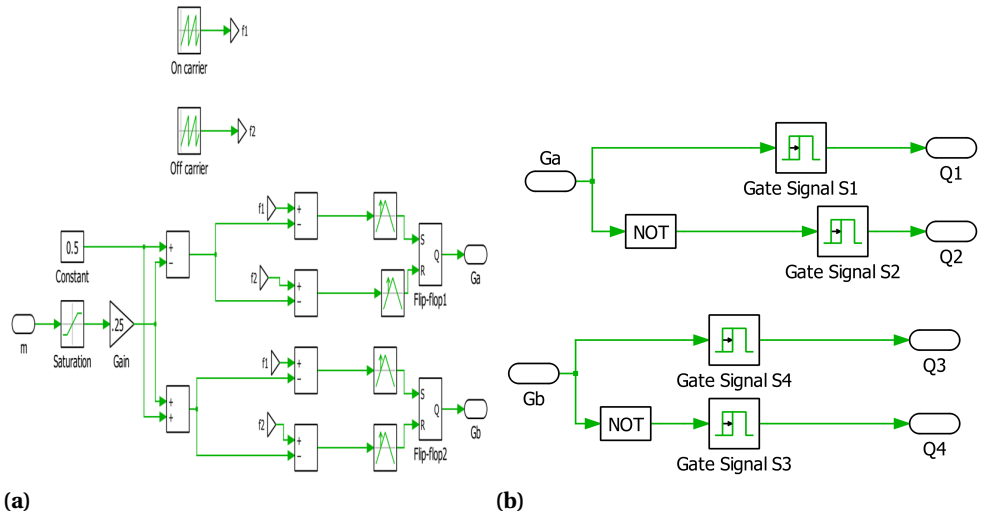



**Figure 7.3** (a) PSM Modulator (b) Gate drive

The phase shift modulation for the converter is designed as given in 7.3 for a fixed value of duty ratio set at 50%. There are two control pulses generated by the modulator which are used to drive Switch $S_1$,$S_2$ and the second signal which drives switches $S_5$,$S_6$. The phase shift angle is controlled by the modulation control signal m. The control signals for the switches $S_3$ and $S_4$ is driven by inverting the signals for $S_1$,$S_2$ whereas the drive signal for $S_7$ and $S_8$ is driven by inverting the signals for $S_5$,$S_6$. The dead time between the blocks is modelled using turn on delays for the switches with values set as 110 ns for the high side switches and 150 ns for the low side switches.

### 7.2.3 Control Loop Implementation

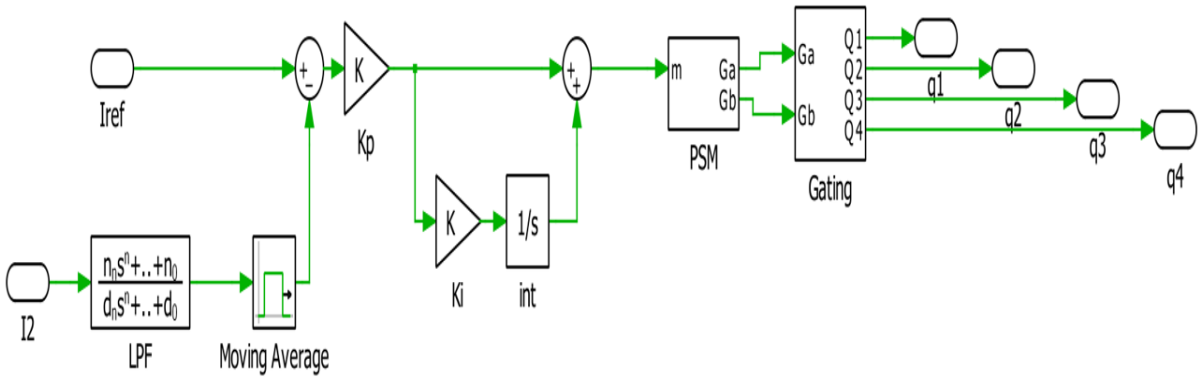



**Figure 7.4** Converter Control Block

**Table 7.2** Control block parameters

| Component Designation | Value |
|---|---|
| Low Pass Filter cutoff frequency, $f_{c,lpf}$ | 10 kHz |
| Moving average filter sampling frequency,$f_{c,maf}$ | 50 kHz |
| PI Compensator gain, $k_p$ | 0.003 |
| PI Compensator pole frequency, $f_{l,pi}$ | 2 kHz |

The control loop is implemented using a low pass filter along with a moving average filter for measurement of the ESS Side current $i_2$ as shown in 7.4. This value is then compared against the command value for the average current. The difference is used by the PI Compensator to generate the command signal m which then is used to drive the Phase shift modulator.

### 7.2.4 Switch Thermal Model

Switch losses as determined from the manufacturer datasheet is used to develop the thermal loss model. The main decomposition is performed in terms of identification of the turn-on and the total turn-off losses. Since the converter operates with a ZVS turn on, the overall losses during turn on is assumed to be close to zero which implies that any switching losses obtained during high current operation would be due to turn off losses.

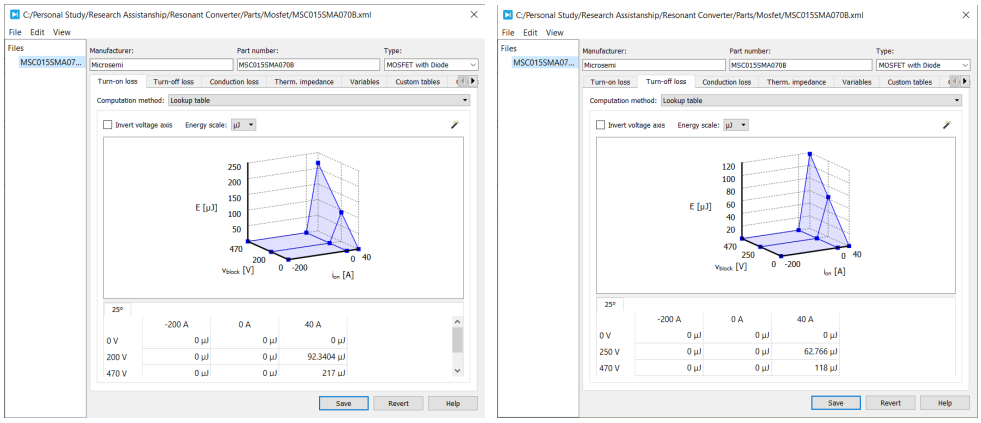



**Figure 7.5** (a) Turn on loss estimation model (b) Turn off loss estimation model

## 7.3 Simulation Results

The verification required from the simulation is in terms of the overall loss model and estimation of the efficiency for the design. The method as described above is used to obtain an estimate with the loss distribution based on the models generated as per the previous section. The values are verified against theoretical values obtained for the overall switch loss and transformer losses. These values are then used to calculate the thermal loss distibution and efficiency curves.

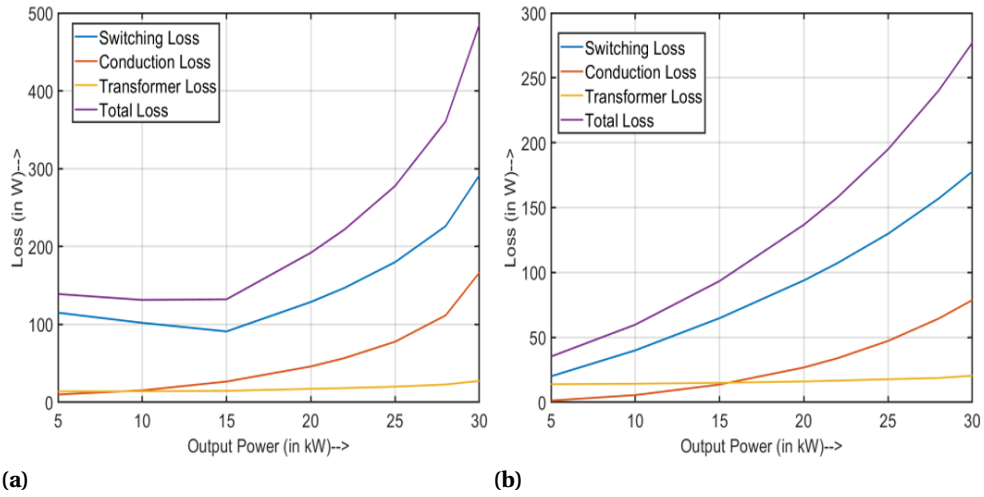



**Figure 7.6** (a) Loss Distribution at $V_2$=480 V (b) Loss Distribution at $V_2$=555 V

The loss distribution in the transformers based on the variations in the actual values of the converter are presented in 7.6. These values are presented for the best case variation where in the ESS Bus Voltage is maintained at $V_2$=555 V for which the converter turns ratio has been selected. Soft switching at this voltage is possible for lower power ratings and thus the value of efficiency calculated are high. Thus, this has been considered as the best case loss distribution and presented in 7.6(b). For the worst case, the loss distribution for the ESS Bus Voltage set at $V_2$=480 V is used. The minimum soft switched power required at the ESS Side is higher than for the best case and thus efficiency values are much lower. Moreover, the current is also significantly high causing increased conduction losses and also higher turn off losses which increase the overall loss values for the transformer and the switches as shown in 7.6(b).

It has to be noted that for this loss distribution estimate, the losses in the transformer and switches are considered since the losses in the parasitics would be negligible. An efficiency curve against the simulation results is obtained for the converter and presented in 7.7. It can be observed that the overall efficiency values are signifcantly high for a majorit of the load range with upto 98% efficiency obtained for the entire operation bus voltage range. The highest efficiency can be obtained for an operation where the power transfer to the ESS is upto 10 kW when the ESS Side Bus voltage is

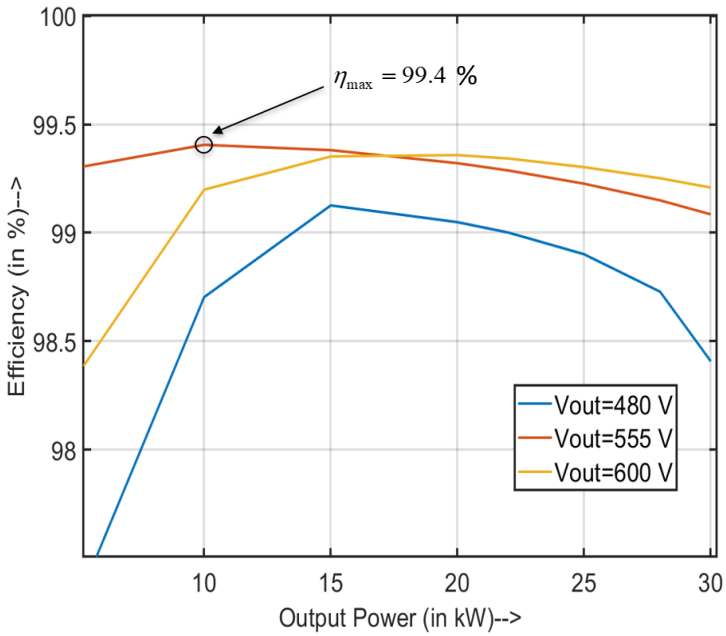



**Figure 7.7** Efficiency curves

maintained at $V_2$=555 V and is upto 99.4 %.

## 7.4 Experimental setup

A low voltage experimental setup was designed to verify converter operational theory and compare the simulation results against the actual hardware results. The setup specifications are listed in 7.3.

The setup comprises of discrete components connected as shown in Fig. 7.8. The main objective of the test setup was to verify soft switched ZVS turn on operation of the switches. This is performed by obtaining the waveforms across the device voltages for the high and low side switches. Since $S_1$ is complementary to $S_2$ and $S_3$ is complementary to $S_4$, waveforms for only one device for each leg was

**Table 7.3** Experimental converter design specifications

| Specification | Expected Value |
|---|---|
| Input Voltage | 500 V |
| Output Voltage | 400 V |
| Output Power | 3.2 kW |
| Transformer leakage inductance, $L_r$ | 2.2 $\mu$H |
| LV Side Resonant Capacitor, $C_{r,1}$ | 3 $\mu$F |
| HV Side Resonant Capacitor, $C_{r,2}$ | 1 $\mu$F |
| Transformer Turns Ratio, $n_p$:$n_s$ | 3:12 |
| Operating Frequency, $f_{sw}$ | 200kHz |
| Dead Time, $t_d$ | 200 ns |

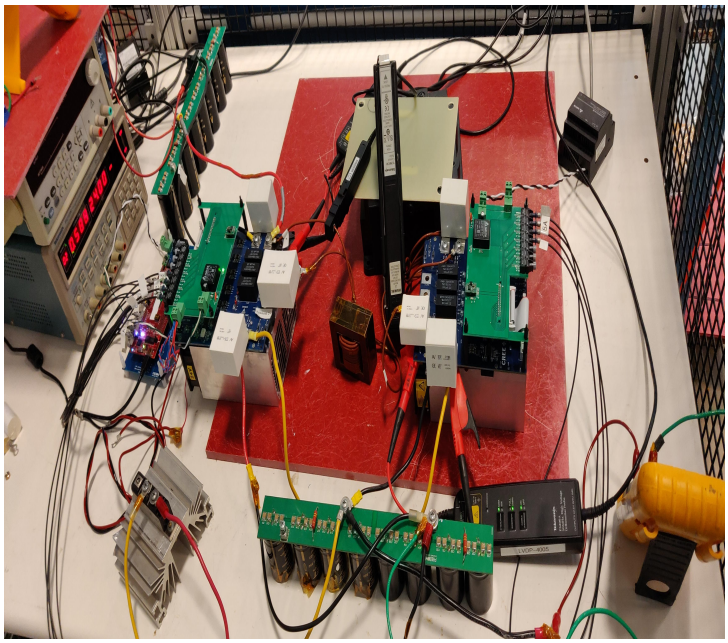


**Figure 7.8** Converter Prototype Hardware Setup

observed along with the current across the transformer. The measurements are made using current probes set up to measure currents across the primary and the secondary side of the transformer. The voltage measurements are made using using high voltage differential probes set to measure the voltage across switch $S_2$ and $S_3$. For the hardware setup designed, no control loop was designed, instead the converter is run in open loop with constant phase angle between the devices $S_1$ and $S_3$ denoted by $\phi$. A texas TI F28379D DSP is used to drive a SiC gate drive circuit driving Cree CCS050M12CM2 SiC MOSFET Module.

## 7.5 Experimental Results

The converter was operated at voltage ratings as defined in 7.3 with a phase angle of $\phi=\frac{2\pi}{5}$ ,i.e. $T_s$=1 µs. The current and voltage waveforms obtained for the converter are presented in 7.9. It can be observed from the waveforms that the switches $S_2$ and $S_3$ have completely soft switched turn on as the voltage waveforms recorded across the devices have minimal oscillations as would normally be observed during a hard-switched transition.

## 7.6 Comparison of magnetics

In order to evaluate the converter stress on magnetics, the stress on the inductor is evaluated in order to obtain a performance metric against a conventional buck converter. The reason for this comparison is since the operational range of the proposed converter is limited as compared to the operational range of the buck converter, the stress on the magnetic components which would be

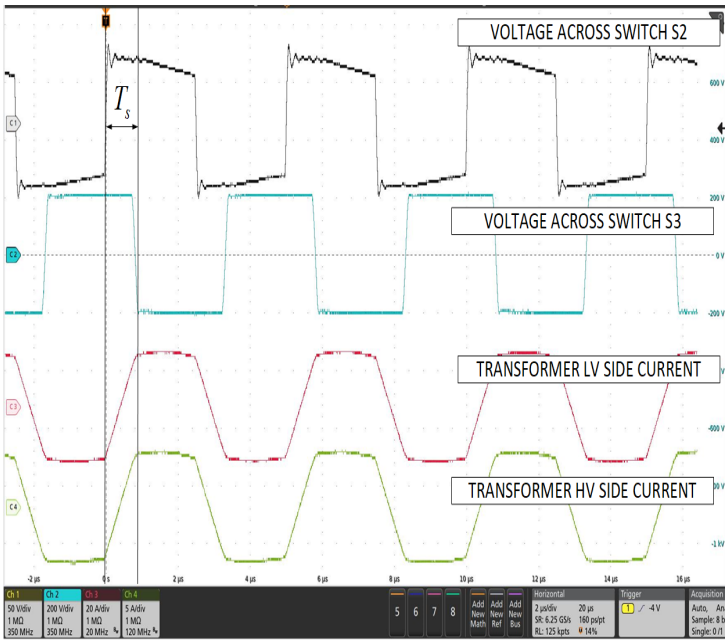



**Figure 7.9** Switching Waveforms

the inductor in the case of a buck converter would be compared to the stress across the leakage inductance of the transformer. The metric used for comparison is the minimum energy stored in the inductance for the buck converter and the minimum energy stored in the leakage inductance of the proposed converter.

The equation for the minimum energy stored in the leakage inductance can be obtained for converter for two modes of operation as derived in A.25,

$$E_l = \left| \frac{(V_1 - V_2 N) I_2}{2N f_{sw}} \right| \tag{7.1}$$

where N=1+1/n and $V_k$ is obtained as

- Case 1 ($V_1 > V_2N$): $V_k = V_1 - V_2N$
- Case 2 ($V_1 < V_2N$): $V_k = V_1 - V_2N$

Upon solving the above equation for a given converter design, a comparison can be made for the average inductor energy for the proposed design and a conventional buck converter.

Based on 7.1, the values for the converter specifications can be substituted into the equation to obtain the minimum energy stored in the leakage inductance. It has to be noted that the energy in this case is obtained to be not dependent on the value of the leakage inductance $L_r$ and instead depends on the primary side voltage stress and $I_2$current.

Similarly for a buck converter it is known that the inductor energy is minimum for the case when the average inductor current is half the value of the peak current across the inductor[43]. Hence the

minimum value of inductor energy can be obtained as,

$$E_{L,buck} = M(1-M)\frac{V_1 I_2}{f_{sw}} \tag{7.2}$$

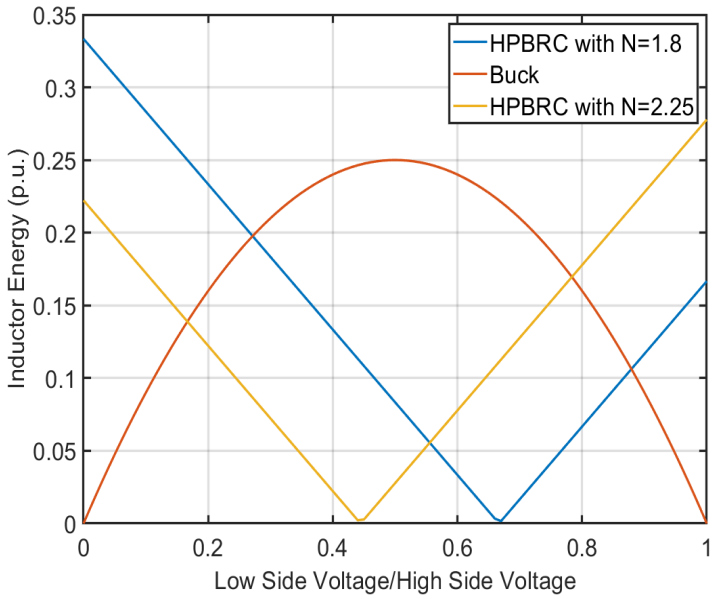



**Figure 7.10** Comparison of inductor energy curves

The energy curves are normalised with a base value of $V_1 I_2 / f_{sw}$ since these parameters are dependent on the converter design and the application for which it is designed. Utilising 7.2 and 7.1 with a value of N=1.8 (for transformer turns ratio set as 1:1.25) and N=2.25 (for transformer turns ratio set as 1:0.8) , the total energy stored across the inductor can be compared as shown in Fig. 7.10.

## 7.7 Summary

The hardware experiment provided more insight to the converter implementation related challenges. An efficiency test was not performed for the current setup due to the lack of a well designed PCB where in the actual values for the converter volume and efficiency could be obtained while ensuring minimal stray losses. Since the components were discrete units connected by lengthy wires there was a significant chance of the losses being high for such a design along with results with higher values than the expectation. However, since the majority of the switching losses are due to turn on energy dissipation, the efficiency is expected to be high.

The simulation results obtained for the prototype however demonstrate an analytical solution for efficiency values. The high values and the low thermal losses for the devices further provide evidence which suggest the use of the converter design for the application.

CHAPTER

# 8

# CONCLUSION AND FUTURE WORK

## 8.1 Conclusion and future work

The thesis focuses on a new converter design targeting an application where there is a bidirectional power transfer between a DC Microgrid and a battery based energy storage system. A prototype was designed and simulated on PLECS in order to study the converter operation using which design equations were developed and verified to model the resonant circuit operation. An average current control loop was designed with the low bus current used as a reference in order to control the converter operation.

A detailed transformer design and thermal model was developed in order to estimate values of efficiency that could be obtained through the converter design. The soft switching requirements and conditions required to maintain soft switch were also analysed in order to determine opportunities for optimisation of component values.

The proposed converter design offers several benefits in terms of high efficiency, reduced volume of overall converter and bidirectional power flow with converter benefits such as reduced component stress which have been studied in this thesis. The comparison with a buck converter design in terms of the stress on the magnetic components demonstrates the benefits in terms of magnetic stress on the components. There are several opportunities available in terms of optimisation along with improvements in converter control design and soft switching operation. Better control design and stability analysis would be possible with the development of a small signal model which can greatly improve control loop design accuracy and is another avenue for exploration and future research.

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## PUBLICATIONS

Some of the research leading to this thesis has appeared previously in an conference paper digest submission which has been accepted for submission,

### Conference Papers

- FNU Satvik, Siyuan Chen, Dakai Wang, Wensong Yu: *Switched Capacitor Resonant Converter with Variable Output Voltage.* – *IEEE Energy Conversion Congress and Exposition*, October 2020, Detroit, Michigan

# APPENDICES

APPENDIX

# A

# DERIVATION FOR TRANSFORMER LEAKAGE VALUE CALCULATION

## A.1 Component Equation Derivation

Component values for the converter are obtained after operational verification of the converter design in order to verify the converter operation. This is performed assuming the input and output capacitances are large enough to be ignored and are represented by the voltage sources $V_1$ and $V_2$ respectively. The input and output capacitances are modelled as the cumulative value of the capacitances and represented as $C_1$ and $C_2$. The resonant capacitors are split and modelled as $C_{r,1}$ and $C_{r,2}$. The capacitances placed parallel to the MOSFETs are for the energy stored in the device when in blocking mode. The converter design is analysed in order to obtain an initial value for the design and selection of the components. This analysis involves the derivation of base equations for component value calculation followed by optimisation of these values based on a knowledge of improvements possible against limits that can be identified in order to estimate maximum design limitation. In this section, the design equations are derived for estimation of the leakage inductance as used in 3.7 and 3.8. The analysis for the converter is based on the approach as given in [44]. The derivation is performed based on the following assumptions:

- The input and output filter capacitors and resonant capacitors are large i.e. the voltage ripple in the capacitors is assumed to be small.
- The converter is assumed to be operating in steady state.

- Dead Time between switches is assumed to be negligible.
- Resonant capacitors are lumped together with a value as given by 3.10.
- Magnetising inductance assumed to be large so that the circulating current is minimal.

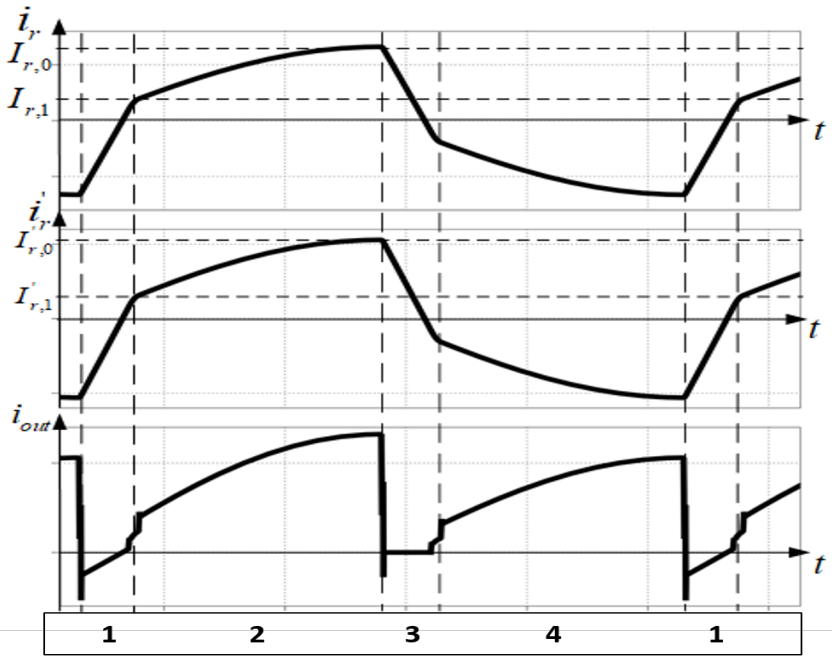



**Figure A.1** Current Waveforms for $V_1$<$V_2$N

The converter waveforms differ when operated at different voltages between the high and low side bus voltages as presented in A.1 and A.2. This leads to two cases which can be identified for derivation of the current due to the difference in the current slopes. The two different operating modes can be identified around the voltage gain across the transformer. The voltage across the transformer is balanced when $V_1$=$V_2$N, where N=1+1/n, with n being the turns ratio as defined in 3. Thus, there are two cases which can be identified where the high side voltage, $V_1$ is either $V_1$>$V_2$N as shown in Fig. A.2 or $V_1$<$V_2$N as shown in Fig. A.1.

The average voltage across the lumped capacitance $C_r$ denoted by $V_{cr}$=$V_1$-$V_2$+$V_2$/n. The phase shift terms can be identified for the two modes as starting from 3.1,

- $V_1$>$V_2$N: For this mode, the value of phase shift can be calculated as,

$$\frac{di_r}{dt} = V_l = \frac{I_{r,0} + I_{r,1}}{T_s} \tag{A.1}$$

During Mode 1, the total voltage across the resonant circuit can be obtained as the difference

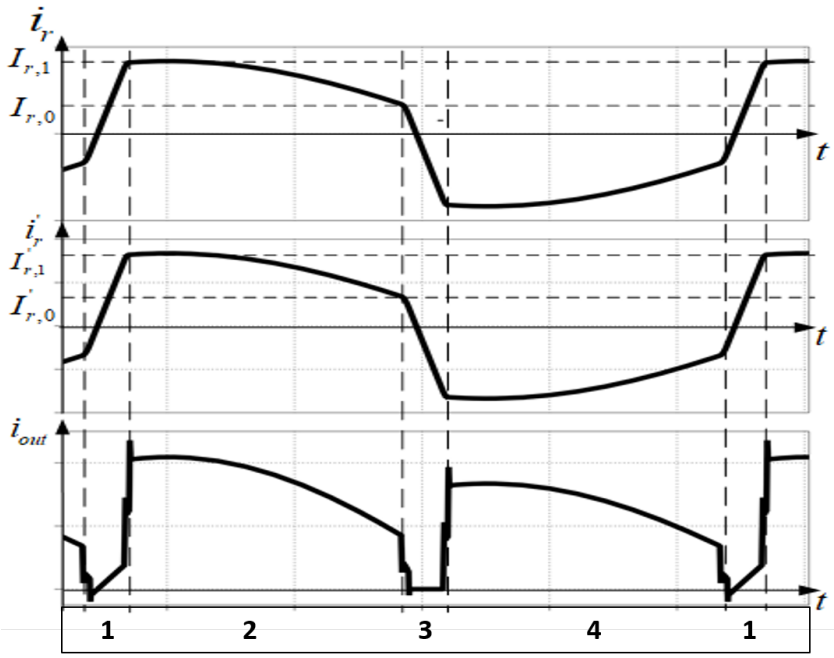



**Figure A.2** Current Waveforms for $V_1$>$V_2$N

between the high and low bus voltages and the leakage inductance.

$$V_l = \frac{V_1 - V_2 + V_2/n}{2} \tag{A.2}$$

Solving A.1 and substituting A.2 and $V_a$= $V_1$-$V_2$+$V_2$/n, the phase shift value can be calculated for this mode as,

$$T_s = \frac{2(I_{r,0} + I_{r,1})L_r}{V_a} \tag{A.3}$$

Similarly, an equation can be derived for mode 2 where the average voltage stress across the inductor can be defined as

$$V_l = \frac{V_1 - V_2 - V_2/n}{2} \tag{A.4}$$

The equation for the current across the inductor for mode 2 can be obtained as,

$$\frac{d\,i_r}{d\,t} = \frac{V_1 - V_2 + V_2/n}{2L_r} = \frac{I_{r,1} - I_{r,0}}{T_s'} \tag{A.5}$$

where $T_s'$=$T_{sw}$/2-$T_s$, Solving A.5, and substituting $V_b$= $V_1$-$V_2$-$V_2$/n, the phase shift value can be calculated for this mode as,

$$T_s' = \frac{2(I_{r,0} - I_{r,1})L_r}{V_b} \tag{A.6}$$

- $V_1$<$V_2$N: Similar to the analysis as performed for the previous mode, the value of phase shift

can be calculated as,

$$\frac{d\,i_r}{d\,t} = V_l = \frac{I_{r,0} + I_{r,1}}{T_s} \tag{A.7}$$

During Mode 1, the total voltage across the resonant circuit can be obtained as the difference between the high and low bus voltages and the leakage inductance.

$$V_l = \frac{V_1 - V_2 + V_2/n}{2} \tag{A.8}$$

Solving A.7 and substituting A.8 and $V_c = V_2 + V_2/n - V_1$, the phase shift value can be calculated for this mode as,

$$T_s = \frac{2(I_{r,0} + I_{r,1})L_r}{V_c} \tag{A.9}$$

Similarly, an equation can be derived for mode 2 where the average voltage stress across the inductor can be defined as

$$V_l = \frac{V_2 + V_2/n - V_1}{2} \tag{A.10}$$

The equation for the current across the inductor for mode 2 can be obtained as,

$$\frac{d\,i_r}{d\,t} = \frac{V_2 + V_2/n - V_1}{2L_r} = \frac{I_{r,1} - I_{r,0}}{T_s^{'}} \tag{A.11}$$

where $T_s^{'} = T_{sw}/2 - T_s$, Solving A.11, and substituting $V_c = V_1 - V_2 + V_2/n$, the phase shift value can be calculated for this mode as,

$$T_s^{'} = \frac{2(I_{r,0} - I_{r,1})L_r}{V_b} \tag{A.12}$$

The analysis also requires an average value to be calculated for the output current, which can be obtained as follows:

- Mode 1: During this mode, the average current is obtained as,

$$i_2 = i_r - i_r^{'} \tag{A.13}$$

The value of the output current is symmetrical and even if the dead time is included is a very small value that can be approximated to a value close to 0.

- Mode 2: During this mode, the output current is equal to the primary side current of the transformer. This value is obtained as,

$$i_2 = i_r \tag{A.14}$$

The area under the trapezoid for this mode can be calculated as,

$$I_{2,1} = \frac{(I_{r,0} + I_{r,1})T_{s'}}{2} \tag{A.15}$$

Since the capacitors are assumed to be large enough, the current in this mode can be approximated to have a linear increase. The value of the average current can be obtained as the area under the trapezoid with the height to be obtained as the magnitude of the $I_{r,0}$ and $I_{r,1}$.

- Mode 3: During this mode, there is no flow to output hence the output current,

$$i_2 = 0 \tag{A.16}$$

The area under the trapezoid for this mode can be calculated as,

$$I_{2,2} = \frac{(I_{r,0} + I_{r,1})T_{s'}}{2n} \tag{A.17}$$

- Mode 4: During this mode, the output current is equal to the secondary side current of the transformer. This value is obtained as,

$$i_2 = i_r^{'} = \frac{i_r}{n} \tag{A.18}$$

Similar to mode 2, the average output current can be calculated by approximating the current curve to be trapezoid and calculating the area under the curve. Since the magnitude of the current is related to the average current calculated under mode 2 by the transformers turns ratio, the average area under the triangle is also found to be the same value.

The final average current for the converter can be averaged for the total duration of the switching period, $T_{sw}$. Hence the average current across the low side bus voltage can be calculated to be,

$$I_2 = \frac{N(I_{r,0} + I_{r,1})T_{s'}}{2T_{sw}} \tag{A.19}$$

It can be noted that $T_{sw}$=2($T_s$+$T_s^{'}$). Substituting the value for $T_s^{'}$ in A.19 from A.6 ,

$$I_2 = \frac{NL_r(I_{r,0}^2 - I_{r,1}^2)}{T_{sw}(V_1 - V_2N)} \tag{A.20}$$

Rearranging A.20, the value for the leakage inductance can be obtained as,

$$L_r = \frac{(V_1 - V_2N)}{Nf_{sw}I_2(I_{r,0}^2 - I_{r,1}^2)} \tag{A.21}$$

The converter design is performed to obtain a minimal volume for the transformer which is possible if the energy stored in the leakage inductance,

$$E_l = \frac{1}{2}L_r i_{pk}^2 \tag{A.22}$$

Substituting $i_{pk}$=$I_{r,0}$ and solving it can be noted that,

$$E_l = \frac{1}{2}\frac{(V_1 - V_2N)}{Nf_{sw}I_2}\frac{i_{r,0}^2}{(I_{r,0}^2 - I_{r,1}^2)} \tag{A.23}$$

A.23 can be compared to solved as,

$$E_l = \frac{(V_1 - V_2N)}{8Nf_{sw}I_2}\left(\sqrt{\frac{I_{r,0}+I_{r,1}}{I_{r,0}-I_{r,1}}} + \sqrt{\frac{I_{r,0}-I_{r,1}}{I_{r,0}+I_{r,1}}}\right)^2 \tag{A.24}$$

It can be proved as done by [44] that the minimum energy across the leakage inductance is possible if $I_{r,1}$=0

Hence, the minimum energy condition can be obtained as,

$$E_{l,min} = \frac{(V_1 - V_2N)}{2Nf_{sw}I_2} \tag{A.25}$$

Since, the target of the intial design process is to ensure a minimal volume of the transformer leakage inductance, the derivation is obtained for a condition when the value of $I_{r,1}$=0. The objective is to obtain the minimum value of leakage inductance in order to meet the required $I_2$ current requirement.

It is known that,

$$f_{sw} = \frac{1}{2(T_s + T_s^{'})}) \tag{A.26}$$

Substituting A.3, A.6 and A.20 in A.26 and solving,

$$I_2 = \frac{N((V_1 - V_2)^2 - (V_2/n)^2)^2}{64L_r f_{sw}(V_1 - V_2N)(V_1 - V_2)^2} \tag{A.27}$$

Rearranging A.27, the value of leakage inductance for given operating condition can be obtained as,

$$L_r = \frac{N((V_1 - V_2)^2 - (V_2/n)^2)^2}{64I_2 f_{sw}(V_1 - V_2N)(V_1 - V_2)^2} \tag{A.28}$$

Similarly solving for the case $V_1$>$V_2$N, the minimum value for the leakage inductance can be obtained as,

$$L_r = \frac{N((V_2/n)^2 - (V_1 - V_2)^2)^2}{64I_2 f_{sw}(V_2N - V_1)(V_2/n)^2} \tag{A.29}$$

With the value for the leakage inductance obtained the minimum value needed to transfer the output power is met, however the soft switching requirement is not met since the inductor will not be large enough to completely discharge the output capacitance. Hence, a value of atleast twice the value calculated should be used for the leakage inductance of the transformer.

For case $V_1$>$V_2$N, the minimum value for the leakage inductance can be obtained as,

$$E_{l,min} = \frac{(V_2 N - V_1)}{2N f_{sw} I_2} \tag{A.30}$$

APPENDIX

# B

# DERIVATION AND VERIFICATION OF OUTPUT CURRENT TO PHASE SHIFT RELATION

## B.1 Converter Operation Analysis

The converter is then analyzed analytically against the model as shown in Fig. 3.2[32],[33]. In order to analyze the circuit the resonant current and voltage equations for a series resonant converter are utilised [45]. As mentioned previously, the analysis is performed with all elements referred to the primary for simplification of the analysis. The equations used are shown below:

$$i_r(t) = \frac{v_r - V_{cr0}}{\omega_r L_r} sin(\omega_r(t - T_M)) + I_{r0} cos(\omega(t - T_M)) \tag{B.1}$$

$$v_{cr}(t) = V_{cr0} + \omega_r^2 L_r \int_{T_M}^{t} i_r(t) dt \tag{B.2}$$

The analysis for the converter is performed using state space analysis in order to simplify analysis [44]. The analysis involves utilising the time domain resonant equations to obtain current peak values for different values of phase shift at the end of each cycle. These values for the minimum and maximum current peak magnitudes can be used to obtain the value of the output current for different values of phase shift. A final verification of the equations is performed against values obtained from simulation results. The following assumptions have been made for the analysis:

- No voltage drop on switching devices.
- Constant output and input voltage
- Steady State operation
- Infinite Magnetising Inductance

The resonant voltage can be obtained for each mode of operation as described in the above section with the value for $v_r$ given by

$$v_r = \begin{cases} V_1 - V_2 + V_2/n & \text{Mode 1} \\ V_1 - V_2 & \text{Mode 2} \\ 0 & \text{Mode 3} \\ V_2/n & \text{Mode 4} \end{cases} \tag{B.3}$$

It is defined that $T_s^{'}$=$T_{SW}$/2-|$T_s$| and $V_k$=$V_1$-$V_2$+$V_2$/n. Hence, definining state space variables as:

$$\hat{i_r}(t) = |i_r(t)| \tag{B.4}$$

$$\hat{v_{cr}}(t) = V_k/2 + |v_{cr}(t) - V_k/2| \tag{B.5}$$

Based on the state space variables assigned the value for each mode can be analyzed. Since modes 3 and 4 are symmetrical, only modes 1 and 2 are analyzed. Similar values can be obtained for modes 3 and 4 due to symmetry.

1. Mode 1 ($0 \leq t \leq T_s$) :

   For this mode, the initial conditions are defined as:

$$v_{Cr0} = V_k/2 - (v_{cr}(0) - V_k/2) = V_k - v_{cr}(0) \tag{B.6}$$

$$I_{r0} = |i_r(0)| = -i_r(0) \tag{B.7}$$

   Upon solving for equation B.1 and B.2 using the inital conditions B.6, B.7 and $v_r$ as given in B.3 for $T_M$=0 B.1 becomes

$$\hat{i_r}(T_s) = \frac{\hat{v_{cr}}(0)}{\omega_r L_r} sin(\omega_r T_s) - \hat{i_r}(0) cos(\omega_r T_s) \tag{B.8}$$

   Substituting t=$T_s$ in B.8, we get

$$\hat{i_r}(T_s) = \frac{\hat{v_{cr}}(0)}{\omega_r L_r} sin(\omega_r T_s) - \hat{i_r}(0) cos(\omega_r T_s) \tag{B.9}$$

$$\hat{v_{Cr}}(T_s) = V_k - \hat{v_{cr}}(0)cos(\omega_r T_s) - \omega_r L_r \hat{i_r}(0)sin(\omega_r T_s) \tag{B.10}$$

The above equation can re-written in a matrix form as:

$$\begin{bmatrix} \hat{i_r}(T_s) \\ \hat{v_{cr}}(T_s) \end{bmatrix} \begin{bmatrix} -cos(\omega_r T_s) & \frac{1}{\omega_r L_r} sin(\omega_r T_s) \\ -\omega_r L_r sin(\omega_r T_s) & -cos(\omega_r T_s) \end{bmatrix} \begin{bmatrix} \hat{i_r}(0) \\ \hat{v_{cr}}(0) \end{bmatrix} + \begin{bmatrix} 0 \\ V_1 - V_2 + V_2/n \end{bmatrix} \tag{B.11}$$

2. Mode 2 ($T_s \leq t \leq T_{SW}/2$) :

For this mode, the initial conditions are defined as:

$$v_{Cr0} = \hat{v_{cr}}(T_s) \tag{B.12}$$

$$I_{r0} = \hat{i_r}(T_s) \tag{B.13}$$

Upon solving for equation B.1 and 3.10 using the inital conditions B.12, B.13 and $v_r$ as given in B.3 for $T_M$=0 and t=$T_s$, the equation for $i_r$(t) for this mode can be obtained as,

$$\hat{i_r}(t) = \frac{-V_2}{n\omega_r L_r} sin(\omega_r(t - T_s)) - \hat{i_r}(0)cos(\omega_r t) + \frac{\hat{v_{cr}}(0)}{\omega_r L_r} sin(\omega_r t) \tag{B.14}$$

Substituting the boundary condition t=$T_s$ in B.14, we obtain,

$$\hat{i_r}(T_{SW}/2) = \frac{-V_2}{n\omega_r L_r} sin(\omega_r T_s^{'}) - \hat{i_r}(0)cos(\frac{\omega_r T_{SW}}{2}) + \frac{\hat{v_{cr}}(0)}{\omega_r L_r} sin(\frac{\omega_r T_{SW}}{2}) \tag{B.15}$$

$$\hat{v_{Cr}}(T_{sw}/2) = V_1 - V_2 + \frac{V_2}{n} cos(\omega_r T_s^{'}) - \hat{v_{cr}}(0)cos(\frac{\omega_r T_{SW}}{2}) - \omega_r L_r \hat{i_r}(0)sin(\frac{\omega_r T_{SW}}{2}) \tag{B.16}$$

During this mode the secondary side of the transformer is connected to $V_2$. Hence the average magnitude of current $I_2$ can be obtained for this case as

$$I_{2,1} = \frac{2}{T_{SW}} \int_{T_s}^{T_{SW}/2} i_r(t) dt \tag{B.17}$$

B.15 and B.16 obtained at the end of mode 2 can be solved as simultaneous equations in order to obtain

$$\begin{bmatrix} \hat{i_r}(t + \frac{T_{SW}}{2}) \\ \hat{v_{cr}}(t + \frac{T_{SW}}{2}) \end{bmatrix} \begin{bmatrix} -cos(\frac{\omega_r T_{SW}}{2}) & \frac{1}{\omega_r L_r} sin(\frac{\omega_r T_{SW}}{2}) \\ -\omega_r L_r sin(\frac{\omega_r T_{SW}}{2}) & -cos(\frac{\omega_r T_{SW}}{2}) \end{bmatrix} \begin{bmatrix} \hat{i_r}(t) \\ \hat{v_{cr}}(t) \end{bmatrix} + \begin{bmatrix} -\frac{V_2}{n\omega_r L_r} sin(\omega_r T_s^{'}) \\ V_1 - V_2 + \frac{V_2}{n} cos(\omega_r T_s^{'}) \end{bmatrix} \tag{B.18}$$

By symmetry it is evident that the state space variables are symmetric over half period such that, $v_{cr}(t+\frac{T_{SW}}{2})$=$v_{cr}(t)$=$\hat{v_{cr}}$ and $i_r(t+\frac{T_{SW}}{2})$=$i_r(t)$=$\hat{i_r}$.Substituting $Z_r$=$\omega_r L_r$, $V_2^{'}$=$V_2$/n and $V_k$=$V_1$-$V_2$+$V_2$cos($\omega_r T_s$), B.18 can be solved to obtain,

$$\hat{i_r} = \frac{-V_2^{'}}{2Z_r} sin(\omega_r T_s^{'}) + \frac{V_k}{2Z_r} tan(\omega_r T_{sw}/4) \tag{B.19}$$

$$\hat{v_{cr}} = \frac{V_2^{'}}{2} sin(\omega_r T_s^{'}) tan(\omega_r T_{sw}/4) + \frac{V_k}{2} cos(\omega_r T_s^{'}) \tag{B.20}$$

The initial values obtained from B.19 and B.20 obtained is used in B.18 in order to solve B.17. Thus, the average value of current $I_2$ can be obtained as,

$$I_{2,1} = \begin{bmatrix} \frac{2}{\omega_r T_{SW}}(sin(\omega_r T_s) - sin(\frac{\omega_r T_{SW}}{2}) \\ \frac{2}{\omega_r Z_r T_{SW}}(cos(\omega_r T_s) - cos(\frac{\omega_r T_{SW}}{2}) \end{bmatrix}^T \begin{bmatrix} \hat{ir} \\ \hat{v_{cr}} \end{bmatrix} - \frac{2V_2^{'}}{\omega_r Z_r T_{SW}}(1 - cos(\omega_r T_s^{'})) \tag{B.21}$$

The value of $I_{2,1}$ obtained is equivalent to the first half period, however for modes 3 and 4,, the average value of $I_2$ denoted by $I_{2,2}$ can be calculated assuming magnetising inductance of the transfer to be large enough to be negligible by,

$$I_{2,2} = \frac{2}{T_{SW}} \int_{T_s+T_{SW}/2}^{T_{SW}} i_r^{'}(t) dt \tag{B.22}$$

Since $i_r^{'}$= $i_r$/n and the current is symmetric during steady state operation, the average value of the output current can be obtained for modes 3 and 4 similarly as,

$$I_{2,2} = I_{2,1}/n \tag{B.23}$$

Hence the total value of the average current in during the entire switching period can be obtained as

$$I_2 = I_{2,1}(1 + 1/n) \tag{B.24}$$

Considering a gain of the transformer around the transformer turns ratio selection by the relation,

$$M = \frac{V_2(1+\frac{1}{n})}{V_1} \tag{B.25}$$

The analysis performed above is used to obtain the values for the current peaks at the time of switching. Additional information such as the phase shift value in relation to the average output current magnitude can be obtained by this analysis. The current peak values can be used to determine the ZVS turn on soft switched region of operation since the current magnitude at the end of each switching cycle is the current that is used to discharge the SiC MOSFETs. The current peak magnitudes required to achieve complete soft switching have been derived in the next chapter.

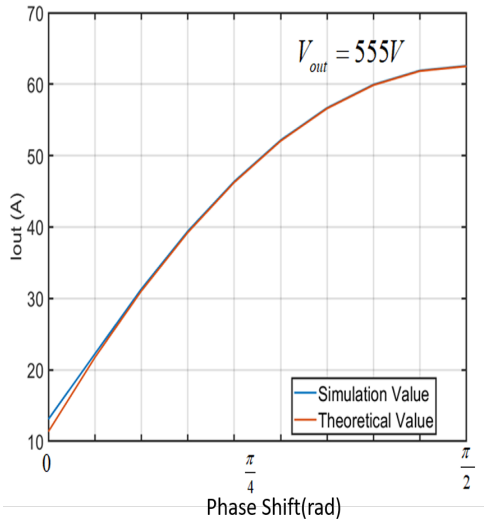
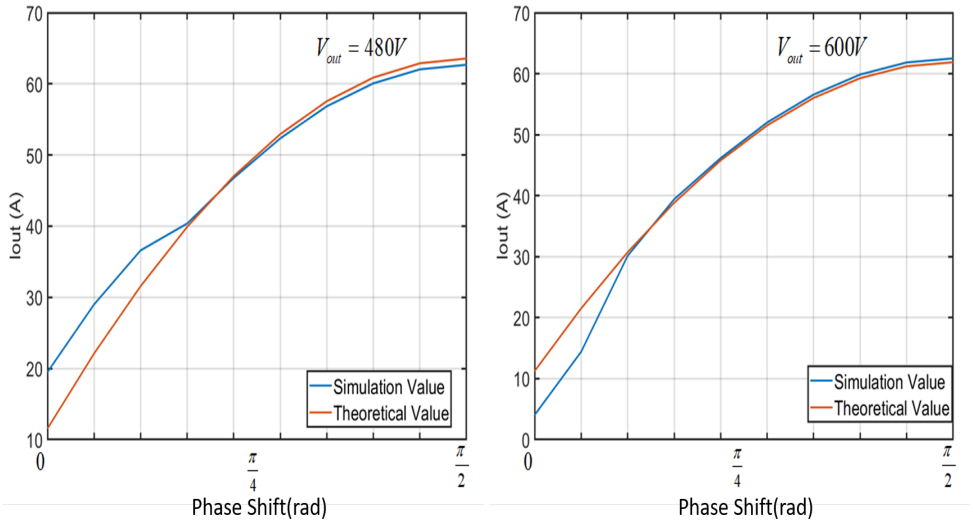



**Figure B.1** Equation Verification for $V_2$=555 V




**(a)** **(b)**

**Figure B.2** (a) Equation Verification for $V_2$=480 V (b) Equation Verification for $V_2$=600 V

## B.2 Verification for derived current equation

The verification of the average low side bus current equations is performed by comparing the values obtained from the theoretical equations against simulation results. This step is necessary to validate the equations. A verification of the simulation model was performed against hardware results however a final detailed verification against a hardware setup in open loop is required to verify the low side bus voltage current to the phase shift equations.

The equations derived by solving B.18 to obtain the value for B.24 is verified against values obtained from simulation results and compared in order to verify values obtained. The worst case operating conditions are presented in Fig. B.2.

The equations can be seen to be a good fit in the case of best case operating condition which is the voltage around which the converter is designed as shown in Fig. B.1.

The comparisons are only provided against simulation results however experimental verification for the converter have to be obtained in order to completely verify the final results.