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Kermani

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[54] INTEGRATED CIRCUIT HAVING REDUCED PROBABILITY OF WIRE-BOND FAILURE

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[52] **U.S. Cl.** **438/617**; 438/123; 438/612; 438/666; 257/784; 257/786

[58] **Field of Search** 438/612, 666, 438/110, 123, 617; 257/784, 786, 666

[56] **References Cited**

U.S. PATENT DOCUMENTS

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[57] **ABSTRACT**

The present invention provides an improved integrated circuit technique for increasing the reliability of wire-bonds in an integrated circuit by increasing the contact angle between certain pins and their respective wire-bonds, particularly those pins otherwise most susceptible to wire-bond failure, i.e., those pins conventionally located toward the corners of a conventional integrated circuit. By doing so, the overall length of the wire-bonds in a chip will be reduced, which in turn can result in further reduction of the probability of wire-bond failures. In a disclosed embodiment, a five or more sided integrated circuit shape is introduced wherein pads on up to four sides of an integrated circuit wafer chip are bonded to pins supported on eight edges of an integrated circuit package. An integrated circuit having at least five pin-supporting edges renders more robust wire-bond angles for any given integrated circuit package size.

10 Claims, 5 Drawing Sheets

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