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(54) **OPTOELECTRONIC DEVICES HAVING ARRAYS OF QUANTUM-DOT COMPOUND SEMICONDUCTOR SUPERLATTICES THEREIN**

FOREIGN PATENT DOCUMENTS

EP 0 178 831 B1 8/1991

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(57) **ABSTRACT**

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Related U.S. Application Data

(62) Division of application No. 10/760,966, filed on Jan. 20, 2004, now Pat. No. 6,914,256, which is a division of application No. 10/178,941, filed on Jun. 24, 2002, now Pat. No. 6,709,929.

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(51) **Int. Cl.**
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(52) **U.S. Cl.** **257/15**; 257/E29.071; 977/762

(58) **Field of Classification Search** 257/15, 257/22, E29.07, E29.071, E21.404; 977/762, 977/763, 814, 815, 819

See application file for complete search history.

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Methods of forming a nano-scale electronic and optoelectronic devices include forming a substrate having a semiconductor layer therein and a substrate insulating layer on the semiconductor layer. An etching template having a first array of non-photolithographically defined nano-channels extending therethrough, is formed on the substrate insulating layer. This etching template may comprise an anodized metal oxide, such as an anodized aluminum oxide (AAO) thin film. The substrate insulating layer is then selectively etched to define a second array of nano-channels therein. This selective etching step preferably uses the etching template as an etching mask to transfer the first array of nano-channels to the underlying substrate insulating layer, which may be thinner than the etching template. An array of semiconductor nano-pillars is then formed in the second array of nano-channels. The semiconductor nano-pillars in the array may have an average diameter in a range between about 8 nm and about 50 nm. The semiconductor nano-pillars are also preferably homoepitaxial or heteroepitaxial with the semiconductor layer.

5 Claims, 8 Drawing Sheets

