ABSTRACT

DUAN, XIAOMING. High Performance Integrated Controller with Variable Frequency Control for Switching DC-DC Converters. (Under direction of Dr. Alex Q. Huang.)

Development of digital core chips poses serious challenges to the power supply design. High performance switching DC-DC converter must meet requirements of high current, low voltage tolerance, fast transient response, high power efficiency, small profile and low cost. The conventional PWM control with constant switching frequency has limitation to improve both transient response and power efficiency because there is a conflicting requirement on switching frequency. The control scheme with variable frequency has promising features to achieve better overall performance, but the issues in the reported design approaches limit their usefulness in the practical applications. This dissertation reviews and summarizes the issues and the design considerations in the high current switching DC-DC converters. To improve the system performance, novel control architecture with variable switching frequency and novel implementation of the integrated controller are proposed in this dissertation. The proposed control architecture is modeled and analyzed. Fully differential circuits are designed to implement the control core functions. The design methodology and the design considerations are discussed. The control concept and the proposed circuits are verified by the prototype controller chip.

High Performance Integrated Controller with Variable Frequency Control for Switching DC-DC Converters

by

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Approved by:

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To my wife,
Manjing Xie

and my parents,
Qiquan Duan and Yun Yu

BIOGRAPHY

The author, Xiaoming Duan, was born in Anhui, China, on October 09, 1976. He received B.S. degree in Physics from Tsinghua University, Beijing, China, in 1998, and M.S. degree in Electrical Engineering from Virginia Polytechnic Institute and State University, Blacksburg, VA, in 2004. He transferred to Raleigh, NC, with his advisor and started to pursue Ph.D degree in North Carolina State University in 2004.

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My academic path in US extended from Virginia Tech (2001-2004) to North Carolina State University (2004-2006). I am indebted to the past friends and colleagues in Virginia Tech, especially, Mr. Nick Sun, Dr. Xin Zhang, Dr. Yunfeng Liu, Mr. Meng Yu, Dr. Bin Zhang, Mr. Hongfang Wang, for their stimulating conversations and friendship.

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My heartfelt thanks belong to my wife, Manjing Xie. She supports me with her brilliant ideas and soothing cares. Her love accompanies me going through ups and downs.

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Chapter 1 Introduction

1.1 Power consumption in high performance computer systems

In modern computer systems, great amount of power is consumed by the digital core chips for intensive data computation. A good example of such chips is the high performance microprocessor (CPU). When transistor technology moves into the nanometer scale, power demand of microprocessors could be even higher because more transistors are integrated and the leakage current of the transistor increases [Agerwala'05]. Another driving force of increasing power consumption in digital core chips is demand of high throughput in the computing devices. For example, the clock frequency in Intel's CPUs has been continuously increased for three decades to improve the system performance.

Power consumption in computer systems emerges as a serious concern for several reasons. First, huge power dissipation causes severe thermal burden to the system. Adding or enlarging heat sinks and cooling fans are undesirable for increasing size and weight of the system. Secondly, since portable devices have gained significant share of market, power-efficient design becomes critical in business competition. Battery lifetime is now a key metric of performance for most portable devices. Thirdly, supplying required power into the core chips is getting more difficult than before. As shown in Fig. 1.1, the current in Intel's CPUs was rapidly increasing in the past decades while the supply voltage kept scaling down [Aygun'05]. The tolerance window of the voltage shrinks to less than 100 mV, at the same time, the current slew rate reaches more than hundreds Amperes per micro second during CPU transitions [Stanford'04]. For the power

supply designers, it is a nightmare to supply such huge dynamic current with the voltage tightly regulated [Lee'99]. Besides, due to the parasitic components inside the package and the chip, stabilizing voltage inside the chip is also troublesome even though the voltage outside the chip is constant. As we know, the supply voltage is crucial for maintaining chip functionality. The voltage higher than the top limit may physically damage the chip, and the voltage under the bottom limit may violate the delay requirement of the digital circuits [Saint-Laurent'04].

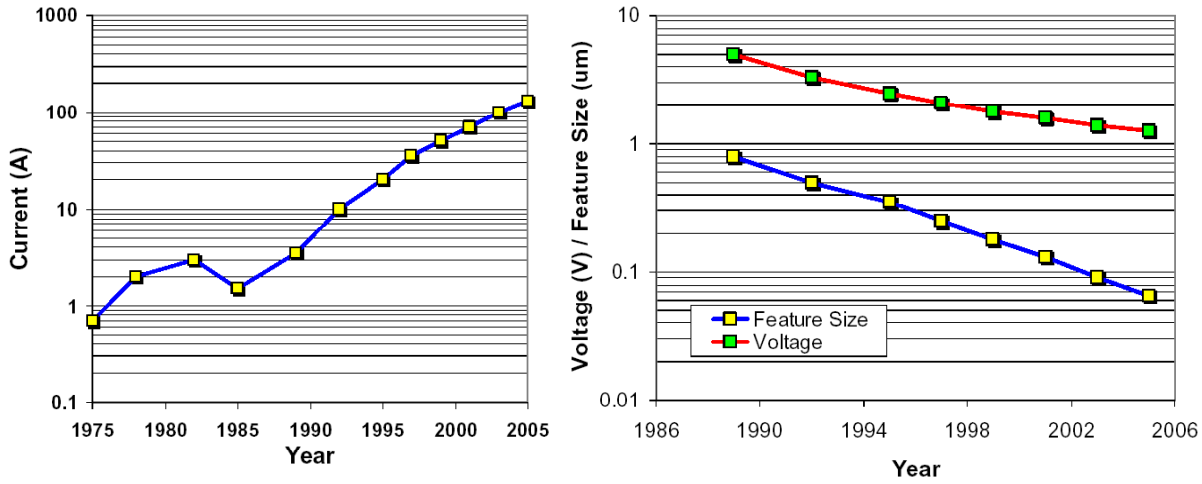
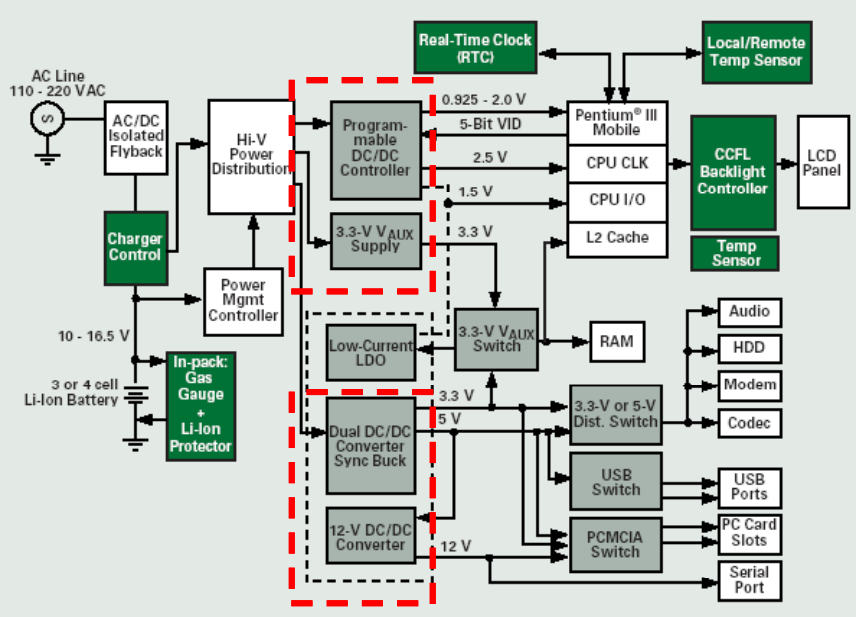


Figure 1.1 Trends of current, voltage and technology feature size of Intel's microprocessor

1.2 Power distribution and voltage regulators in computer systems

In most computer systems, electrical energy comes from the centralized power source, such as the silver box, the power adaptor or the battery. Requirements of power in various chips are quite different. For example, LED drivers for the display usually require higher voltage and less current, but the digital core chips require lower voltage and much more current. To meet requirements of the whole system, a large number of voltage regulators are used to process the power to accommodate different loads [Mammano'93]. Fig. 1.2 shows a typical power management system in a mobile computer [TI].

Among the voltage regulators, the switching voltage regulators (or the switching DC-DC converters) are mostly used for supplying high current to the loads for high efficiency. The Voltage Regulator Module (VRM) for supplying power to CPUs on the motherboard is one of such applications. In today's industry, most high current converters are designed based on the multi-channel synchronous Buck converter shown in Fig. 1.3 [Zhou'00]. In the circuit, each channel that comprises a main switch (or a high side switch), a synchronous rectifier (or a low side switch) and a power inductor, manipulates current flows by turning on and off the switches. By connecting all channels in parallel, the currents in all channels are added up to supply the load current. The output voltage is maintained at required level by using a controller that generates the switching driver signals or the duty cycle signals. Large amount of output capacitors are used to reduce the voltage ripples and maintain voltage regulation during load current transient. In desktop and laptop computers, the DC-DC converter is built around the CPU on the motherboard. The CPU power management system is made up of the power source, the DC-DC converters, the motherboard and power management circuits inside the CPU itself.



Switching DC-DC converters

Figure 1.2 Power management system in a mobile computer

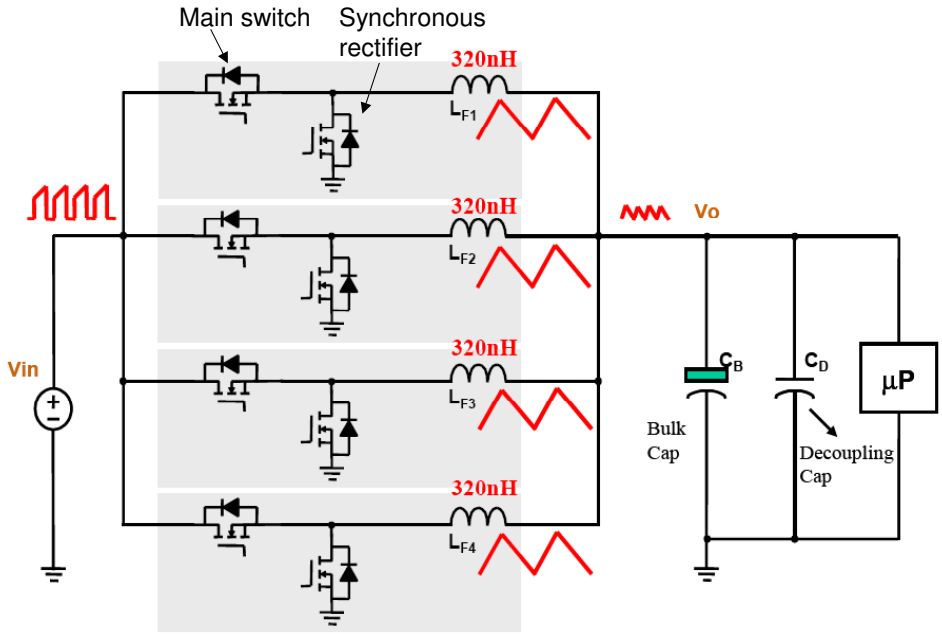


Figure 1.3 A multi-channel DC-DC converter for powering microprocessors

1.3 Tradeoff between high efficiency and fast load transient response

High efficiency and fast load transient response are two major requirements in high current DC-DC converters design [Panov'01].

Although power efficiency of the switching converters is considered high compared with other voltage regulators such as the linear regulator and the switching capacitor regulator, power loss in the power supply circuits adds up to be a significant portion of total power consumption in the computer system. From experimental results shown in Fig. 1.4, 10 percent of power is consumed by the power supply in a mobile computer running a test bench program [Chinn'03]. In contrast, only 6 percent of power is consumed by the CPU itself. In fact, power consumption of CPUs has been significantly reduced in mobile computer systems by adopting power management techniques and new computer architecture design [Intel-1'04]. There is strong motivation to improve power efficiency of power supply circuits in mobile systems.

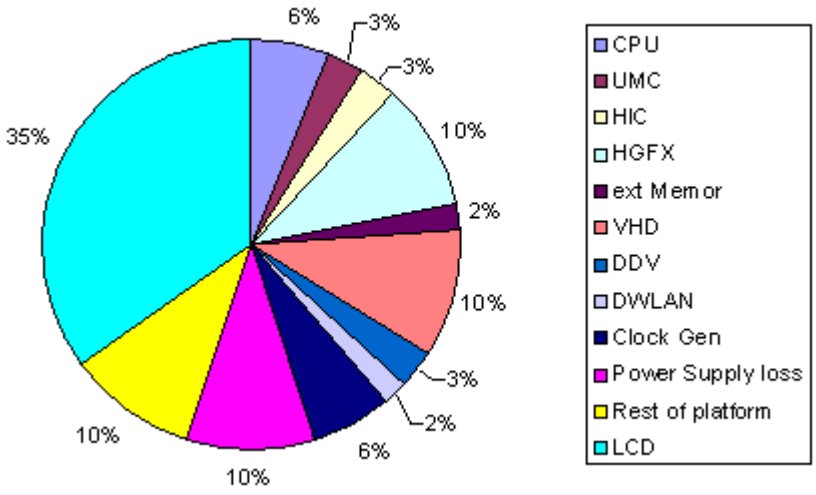


Figure 1.4 Average power distribution in a mobile computer

Power efficiency of the typical multi-channel Buck converter is determined by many factors including design parameters, operation conditions and component characteristics.

For instance, power efficiency is affected by the switching frequency, the load current, the input voltage, the output voltage, the on-resistance and the gate capacitance of power switches and the parasitic resistance of inductors. Although most of them are related to the power stage design that is not focus of this dissertation, the control strategy and the controller implementation also have significant impact to power efficiency. One of the most important design parameters is the switching frequency. In general, relatively low switching frequency is preferred for power efficiency because many power losses in the switching converters, such as switch turn-on loss, switch turn-off loss and deadtime loss, increase with the switching frequency [Bai'03]. Fig. 1.5 shows a typical power loss breakdown of a synchronous Buck converter with switching frequency at both 300 KHz and 1 MHz [Ren'05-1]. Significant degradation of power efficiency from 300 KHz to 1 MHz was measured as shown in Fig. 1.6.

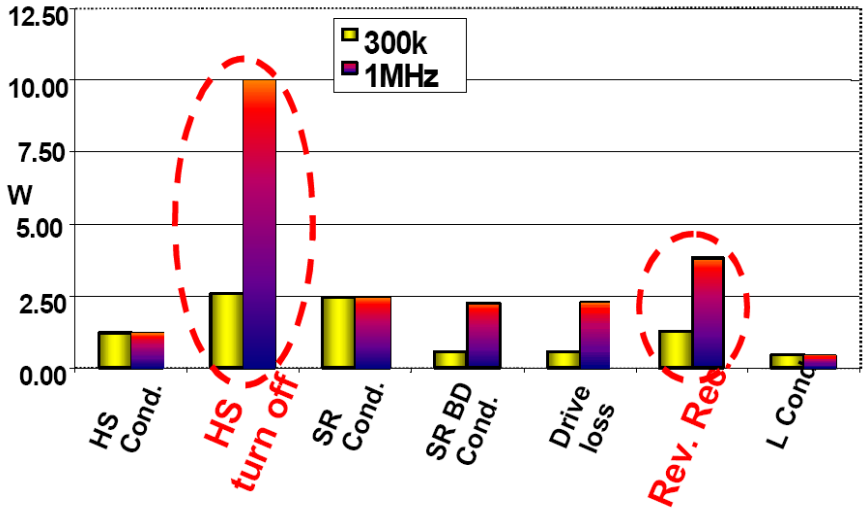


Figure 1.5 Power loss breakdown in a VRM with input voltage 12 V, output voltage 0.8 V and load current 80 A

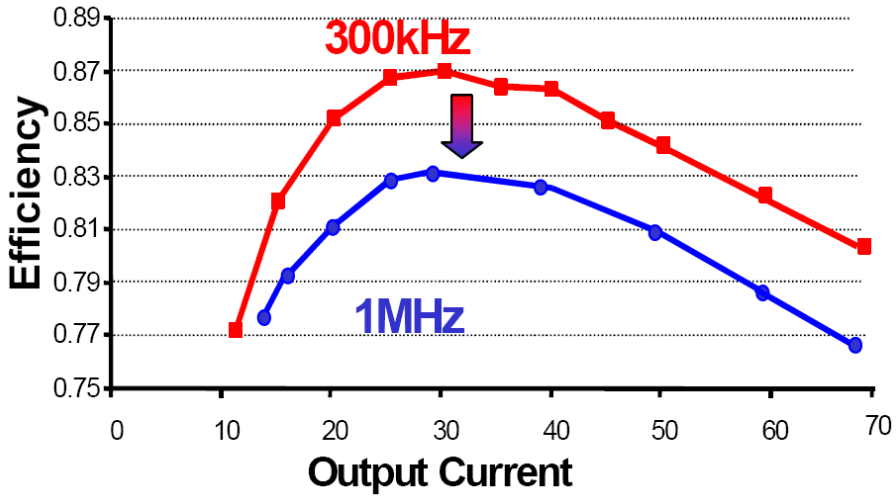


Figure 1.6 Measure efficiency vs. output current of a VRM [Ren'05-1]

However, lowering switching frequency is not a perfect solution since it might compromise another important target of design, i.e. load transient response. As we know, the DC-DC converters are controlled by closed-loop feedback so that the output voltage can be accurately regulated. The converter's response to dynamic load current is governed by both the closed-loop feedback and the open-loop output characteristics, especially, the impedance of output capacitors. For the conventional control scheme with constant switching frequency, feedback loop design needs deal with the sampling effect and switching noises. The closed-loop bandwidth is usually designed below one fifth of the switching frequency in order to guarantee stability at steady state [Mitchell'01]. If the control bandwidth is not high enough, large amount of output capacitors is needed to reduce output impedance beyond the control bandwidth and to keep voltage spikes within the tolerance window. For the VRMs, large amount of output capacitors are not cost effective in the design. More importantly, the output capacitors occupy large real estate on the motherboard as shown in Fig. 1.7, which is precious in mobile computer systems.

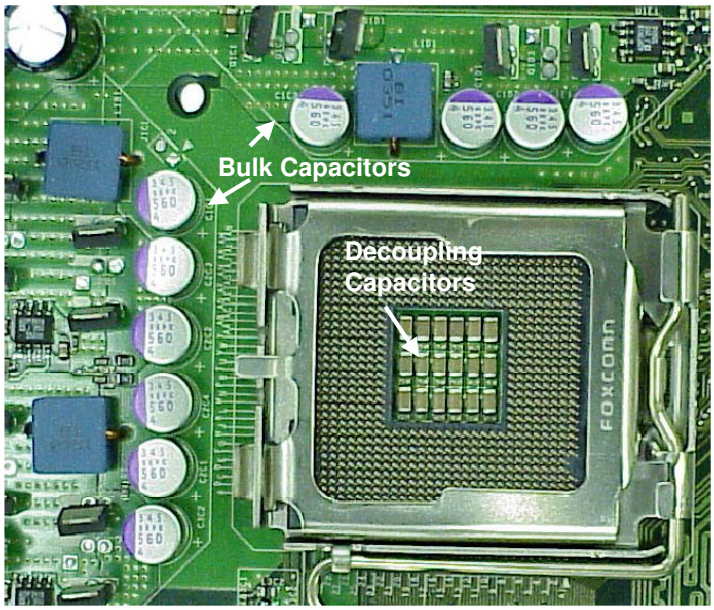


Figure 1.7 VRM components and CPU socket on the motherboard

1.4 Research motivations

Improving dynamic response without sacrificing power efficiency is one of the most popular topics in the filed of switching power supply design. Different approaches were proposed based on either the circuit topology or the control strategy.

For the topology approaches, the basic topology shown in Fig 1.2 is modified with additional circuits added to realize better overall performance. For example, the approach proposed in [Ren'05-1] introduced two stages in which the first stage converts the input voltage to an intermediate bus voltage and the second stage converts the intermediate bus voltage to the output voltage. By the two-step conversion, the design requirements on both stages are somehow relaxed. Since the ratio of the input voltage to the output voltage is reduced in both stages, some losses related to switching transitions is significantly reduced, which makes it possible to use much higher switching frequency without sacrificing too much of power efficiency. Another example of the topology

approaches is using the circuits that only work during the transient, such as the active clamp [Li'06]. With these approaches, the switching DC-DC converter is designed only to supply the static current while the dynamic current is handled by the clamping circuits. Since the requirement of transient response on the switching DC-DC converter is reduced, it is possible to use relatively low switching frequency to achieve higher efficiency. In practical design, the power loss in the clamping circuits should be well limited so that the overall efficiency is not degraded too much by the clamping circuits. Compared with the control approaches, the topology approaches have more flexibility in design, but adding the extra circuits may increase design complexity, the cost and the size of the system.

For the control approaches, a key idea is to separate load transient response with steady state performance in the switching DC-DC converters. One of the methods is introducing non-linear control functions in addition to the linear control function. For example, the transient response can be simply improved by saturating the duty cycle when the load transient is detected. However, because of its non-linear nature, it is difficult to build the proper model for the system, and system operation may vary significantly under different situations. Another approach to solve the dilemma of the switching frequency is to implement the control with variable switching frequency. As shown in Fig. 1.8 and Fig. 1.9, the switching frequency changes dynamically during load transients. If the system operates in steady state for most of the time, the average switching frequency is mainly determined by the steady state switching frequency. Therefore, lower switching frequency can be designed to improve power efficiency. The transient response of the system is no longer constrained by the steady state switching frequency. It is possible to

achieve good dynamic response without sacrificing power efficiency. If the control of the variable frequency is implemented with linear circuits, the system can be well modeled and analyzed with simple linear models. Robustness of design can be achieved in the design. Besides, power efficiency in the light load condition can be dramatically improved by reducing the switching frequency. The control technique with variable frequency can cover both the light load condition and the heavy load condition and give smooth transition between them. On the contrary, in the typical constant frequency controls, a dedicated control for light load condition, such as burst mode control, pulse-skipping control, is designed in addition to the normal control mode for heavy load. The transition between the two controls is always headache in the design.

Although control architecture with variable frequency has shown promising features, it is challenging to implement the variable frequency control with circuit techniques. For example, because of the wider range of the switching frequency, the signal dynamic range is extended and higher bandwidth up to tens of MHz is sometimes required in the control circuits. Because switching is no longer periodically controlled, the noise spectrum is expanded. The control circuits need to live with the wideband noise. Furthermore, there is no clock signal available in the design; the synchronization of the multiple channels is no longer straightforward. It is the motivation of this dissertation to propose and analyze a control scheme with variable switching frequency and present novel design approaches to deal with the practical issues and achieve better performance.

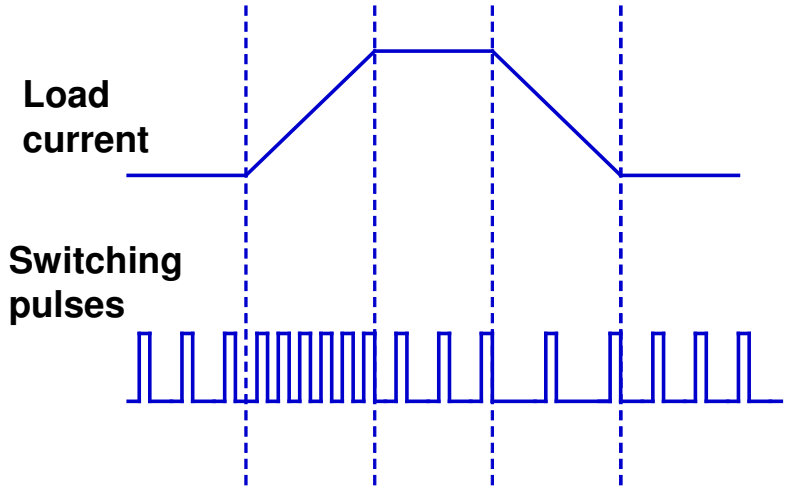


Figure 1.8 Variable switching frequency changing with load current

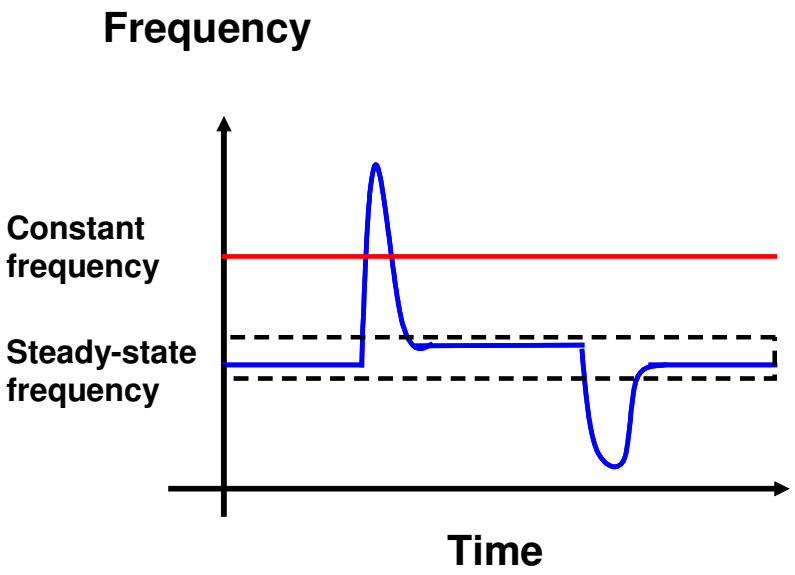


Figure 1.9 Plot of frequency versus time in variable frequency control

1.5 Outline of dissertation

In Chapter 2, the conventional PWM control with constant switching frequency is reviewed. The limitation and design tradeoffs of conventional control design are identified. A new control scheme based on current mode control with variable switching frequency is proposed. The control system is analyzed with small signal models. The

design guidelines are derived to meet the system specifications. In Chapter 3, the integrated controller for switching DC-DC converters is introduced. Design methodologies to implement the integrated circuits, the issues with noise in the DC-DC converters and current sensing techniques are discussed. In Chapter 4, the core control circuits for the proposed control scheme are presented. Fully differential architecture is proposed. Some practical issues related to current sensing, noise immunity and regulation accuracy are addressed in the circuit design. In Chapter 5, the required design tasks in the multi-channel controller, interleaving and current sharing, are discussed. The traditional design techniques are reviewed. The design approaches for the proposed controller are proposed. In Chapter 6, design of the prototype two-channel controller is briefly introduced. Some of the simulation and test results are summarized. Finally, Chapter 7 concludes the dissertation and provokes a discussion on future work.

Chapter 2 Current Mode Variable Frequency Control

2.1 Background and review of conventional PWM control

A DC-DC converter can be partitioned into two parts: the power stage and the controller. A single channel Buck converter is shown in Fig. 2.1 as an example. The power stage is a multiple-input single-output system. The system inputs are the driver signal $d(t)$ and the input voltage $v_{in}(t)$, and the system output is the output voltage $v_{out}(t)$. The state of system can be represented by two state variables, the output voltage $v_{out}(t)$ and the inductor current $i_L(t)$. The purpose of the control is to maintain the output voltage constant and equal to the reference voltage V_{ref}.

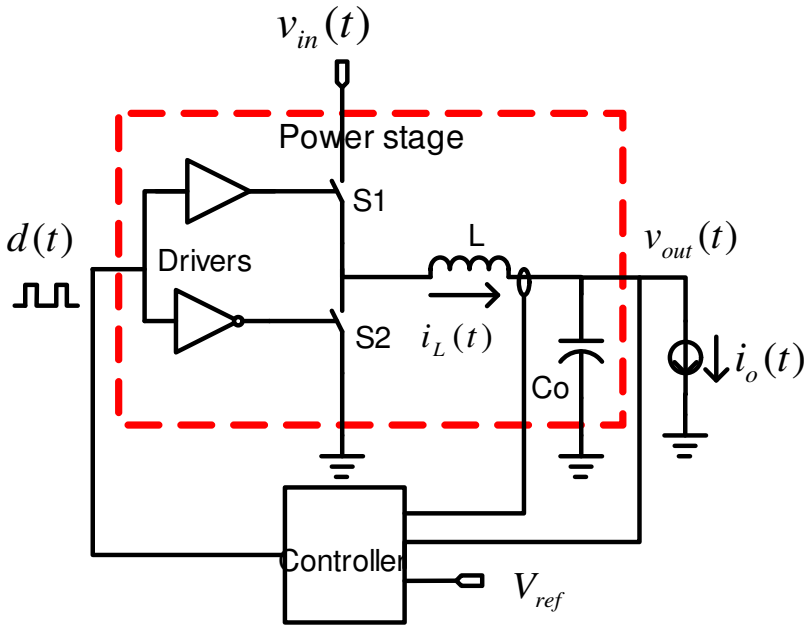


Figure 2.1 Block diagram of a DC-DC converter

Since the DC-DC converter is connected to the pre-regulated power supply or the battery, the input voltage $v_{in}(t)$ can be modeled as a voltage source with certain output impedance. The driver signal $d(t)$ is a series of pulses. In each pulse cycle, during on time the main

switch S1 is conducting the current from the input source to the load; during off time the synchronous rectifier S2 is conducting the free wheeling current in the inductor. If the period of the pulse cycle, T_s, is constant, $d(t)$ can be represented by the duty cycle or the pulse width (or the on time t_{on}):

$$dutycycle = \frac{t_{on}}{t_{on} + t_{off}} = \frac{t_{on}}{T_s} = t_{on} f_s \qquad (2.1)$$

If switching frequency is constant, the pulse width is modulated in the control. In this dissertation, control with constant switching frequency is referred as the Pulse Width Modulation (PWM) control. In fact, most of commercial switching DC-DC converters are designed with the PWM control. Varieties of PWM control methods have been developed. The implementation of the PWM control has standard design procedures [Patel'85].

Existing PWM control methods can be categorized by signals used in the feedback: voltage mode controls only use output voltage feedback; current mode controls use feedback of both the output voltage and the current [Dixon'85]. Fig. 2.2 shows a simple implementation of the voltage mode control, where the circuit that transfers the error signal $v_e(t)$ into the driver signal is the PWM modulator. For current mode controls, many implementation methods have been developed. The current mode control methods can be roughly categorized by implementations of current sensing: the Instantaneous Current Mode control (ICM control), the Average Current Mode control (ACM control) and the indirect current mode control. Specifically, the ICM control senses instantaneous current waveforms in either the inductors or the switches. The examples of the ICM control include Standard Control Module (SCM) implementation, the peak current

control (or the current injection control), the valley current control, etc [Dixon'85]. An implementation of the peak current control is shown in Fig. 2.3. The ACM control senses averaged current information, which means AC ripples in the inductor current are reduced by filtering and only low frequency components of the current signals are used for control [Tang'93-2]. An example of ACM is the active droop control [Yao'03-2] shown in Fig. 2.4. The indirect current mode control uses the current information in alternative forms. For example, integration of the current is used in the charge control [Tang'93-1]. Sometimes, sensing the current indirectly saves much effort in circuit implementation. Each implementation approach of the current mode control has its own advantages and limitations. Proper choice of the control depends on the specific application. The control discussed in this dissertation falls into the first category, the instantaneous current mode control.

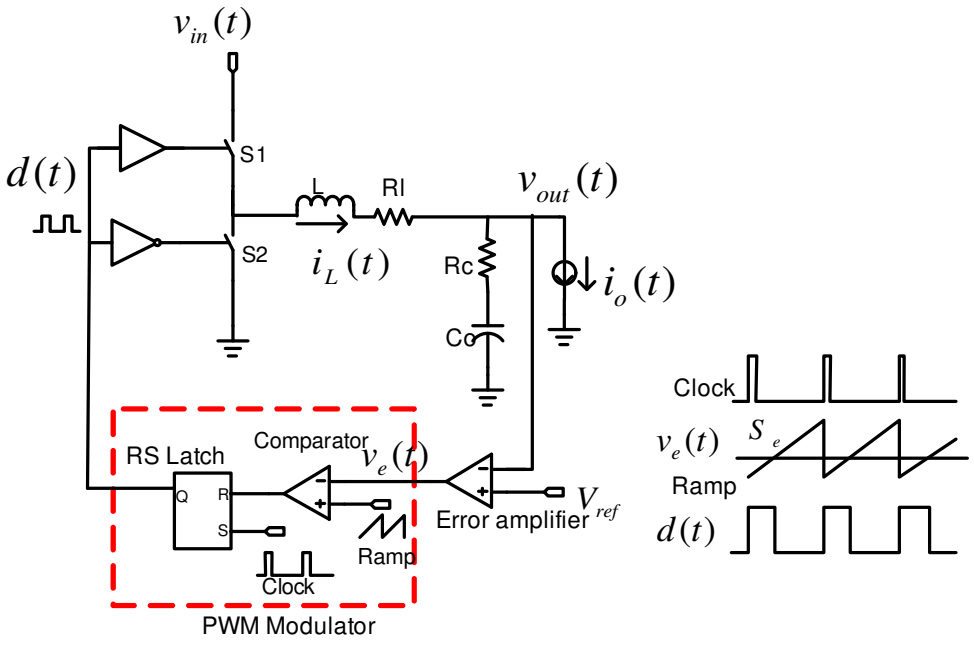


Figure 2.2 An implementation of voltage mode PWM control

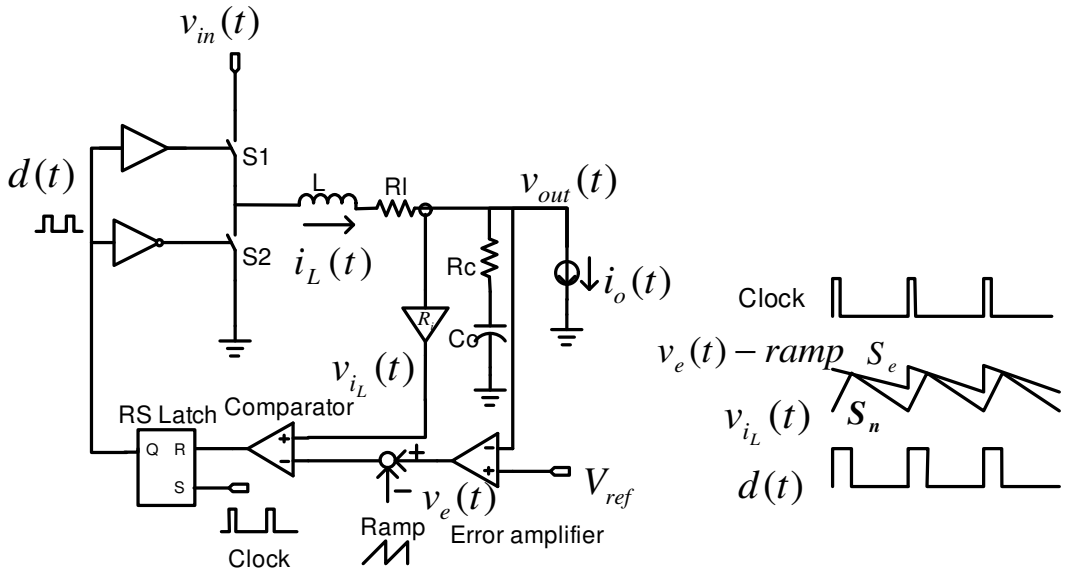


Figure 2.3 An implementation of peak current control

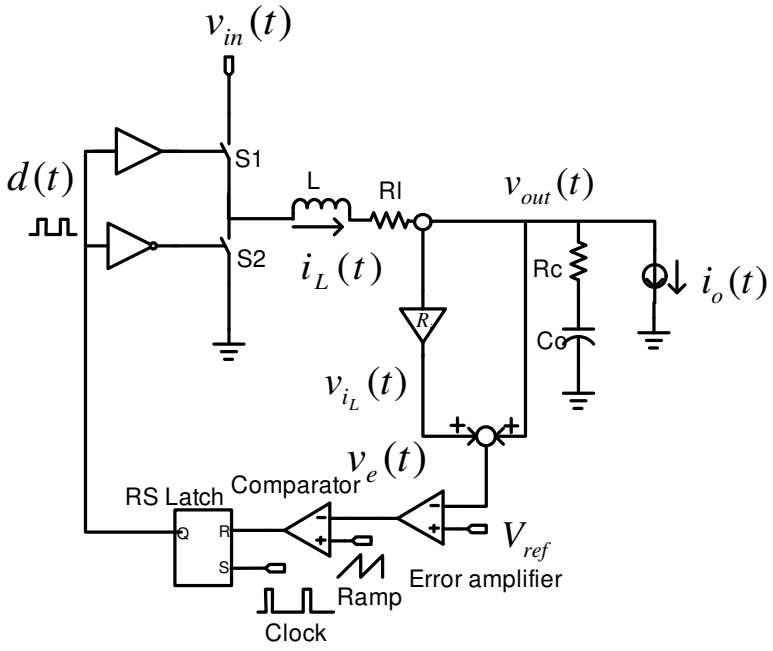


Figure 2.4 An implementation of active droop control

Modeling and analysis of the control system in switching DC-DC converters is usually done by small signal analysis in frequency domain [Ridley'88]. Since the system in nature is a mixed-signal system with both discrete signals and continuous signals,

approximation is needed before the system can be simply modeled as a continuous linear system. A useful method of approximation is averaging in which switching ripples are omitted and only averaged signals are considered in the model. It should be noted that the averaged model is accurate only if the interested frequency is much lower than the switching frequency [Ridley'88]. With this assumption, the system is linearized and characterized by the transfer functions. The system block diagram can be used to analyze the feedback loops. Fig. 2.5 and Fig. 2.6 show the system block diagrams of the voltage mode control and the peak current control system, respectively.

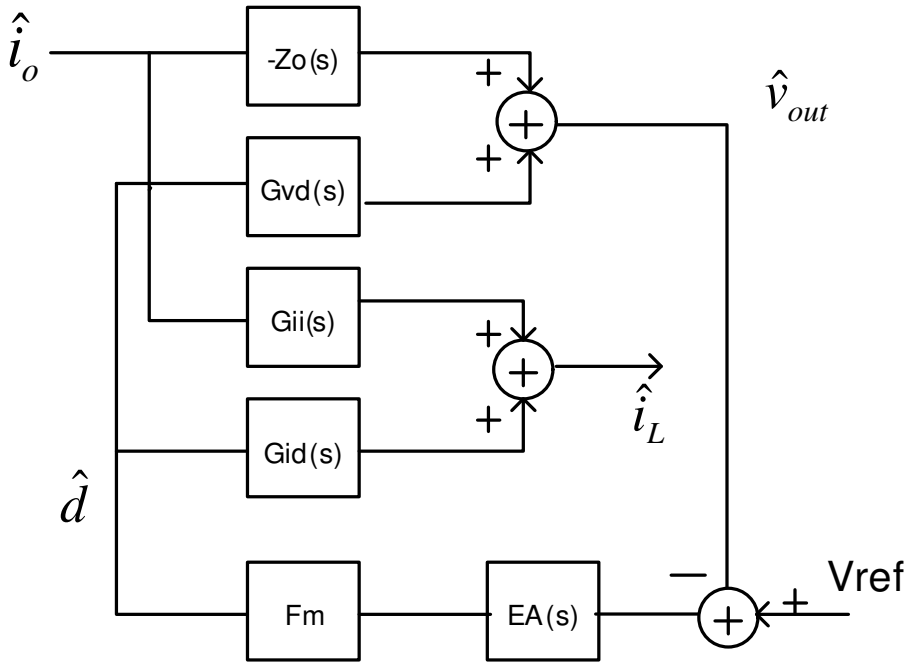


Figure 2.5 System block diagram of a DC-DC converter with voltage mode control

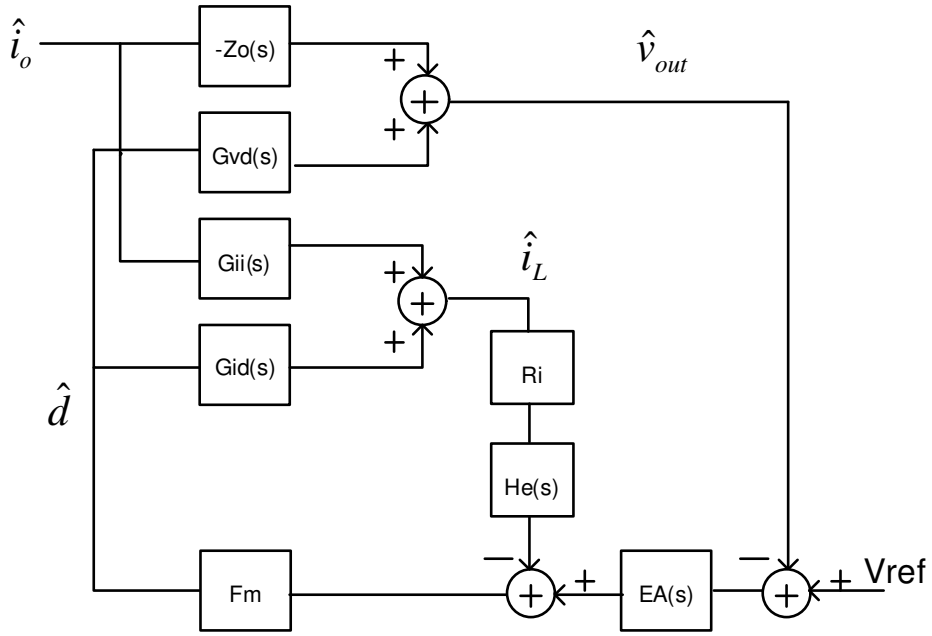


Figure 2.6 System block diagram of a DC-DC converter with peak current control

Here, $G_{vd}(s)$, $G_{id}(s)$, $G_{ii}(s)$ and $Z_o(s)$ are transfer functions of the power stage. The definitions and equations of these transfer functions in the Buck converter under Continuous Conduction Mode (CCM) are listed as in Table 2.1. $EA(s)$ is the transfer function of the error amplifier. F_m and R_i are small signal gains of the PWM modulator and the current sensing gain, respectively. In Fig. 2.6, $He(s)$ models the sampling effect in the instantaneous current mode control [Ridley'90].

Table 2.1 Transfer function gains in small signal models

<table>
<tr><td colspan="2">$$G_{vd}=\left.\frac{\hat{v}_{out}}{\hat{d}}\right|_{I_o}=V_{in}\frac{1+sR_cC_o}{1+\frac{s}{\omega_0 Q}+\left(\frac{s}{\omega_0}\right)^2},\omega_0=\frac{1}{\sqrt{LC_o}},Q=\frac{1}{\omega_0(R_l+R_c)C_o}$$</td></tr>
<tr><td colspan="2">$$G_{id}=\left.\frac{\hat{i}_L}{\hat{d}}\right|_{I_o}=V_{in}\frac{sC_o}{1+\frac{s}{\omega_0 Q}+\left(\frac{s}{\omega_0}\right)^2}$$</td></tr>
<tr><td colspan="2">$$Z_o=-\left.\frac{\hat{v}_{out}}{\hat{i}_o}\right|_{D}=R_l\frac{1+\frac{s}{\omega_1 Q_1}+\left(\frac{s}{\omega_1}\right)^2}{1+\frac{s}{\omega_0 Q}+\left(\frac{s}{\omega_0}\right)^2},\omega_1=\frac{1}{\sqrt{LC_o}}\sqrt{\frac{R_l}{R_c}},Q_1=\frac{1}{\omega_1(\frac{L}{R_c}+R_lC_o)}$$</td></tr>
<tr><td colspan="2">$$G_{ii}=\left.\frac{\hat{i}_L}{\hat{i}_o}\right|_{D}=\frac{1+sR_cC_o}{1+\frac{s}{\omega_0 Q}+\left(\frac{s}{\omega_0}\right)^2}$$</td></tr>
<tr><td>Voltage mode control</td><td>Peak current control</td></tr>
<tr><td rowspan="2">$$F_m=\frac{1}{S_eT_s}$$
S_e: Slope of the ramp</td><td>$$F_m=\frac{1}{(S_e+S_n)T_s},S_n=\frac{R_i(V_{in}-V_{out})}{L}$$</td></tr>
<tr><td>$$H_e(s)\approx 1+\frac{s}{\omega_n Q_z}+\left(\frac{s}{\omega_n}\right)^2,\omega_n=\frac{\pi}{T_s},Q_z=\frac{-2}{\pi}$$</td></tr>
</table>

With the small signal model, important characteristics of the control system, such as open loop gains and output impedance, can be calculated.

$$T_v(s)=G_{vd}(s)EA(s)F_m \qquad (2.2)$$

$$T_i(s)=G_{id}(s)R_iF_mH_e(s) \qquad (2.3)$$

$$T(s)=\frac{T_v}{1+T_i}=\frac{G_{vd}(s)EA(s)F_m}{1+G_{id}(s)R_iF_mH_e(s)} \qquad (2.4)$$

$$Z_{oc}(s)=\frac{(R_c+\frac{1}{sC_o})(\frac{Ls}{Ls+R_c+\frac{1}{sC_o}}+T_i)}{(1+T_2)(1+T_i)}\approx\frac{R_c+\frac{1}{sC_o}}{1+T_2},(T_i=0,orT_i>>1) \qquad (2.5)$$

Here, $T_v(s)$ and $T_i(s)$ are the voltage loop gain and the current loop gain, respectively. $T(s)$ is the overall voltage loop gain with current loop closed. $Z_{oc}(s)$ is the closed-loop output impedance. In Equ. 2.5, the approximation is valid in voltage mode control ($T_i=0$) and at frequency range where $T_i>>1$ in the current mode control. In the typical design approaches, system stability and dynamic response is designed by choosing proper gains, including $EA(s)$, R_i and F_m. Bode plots can be used to evaluate system characteristics [Erickson'01].

2.2 Design considerations of load transient response

In high current DC-DC converters, such as VRMs, transient response is extremely important. The voltage spikes during load current transient must be limited within the tolerance window. To understand the constraints of the transient response in the converters, three major limiting factors are analyzed.

1. Switching frequency

Switching frequency determines the sampling rate in the PWM modulation. As illustrated in Fig. 2.7, $v_e(t)$ is sampled every clock cycle. To avoid aliasing effects, the system bandwidth must be less than half of the switching frequency. In real implementation, large amount of noise exists at the frequency band close to the switching frequency. Because of non-linearities in the circuit, the noise could be transferred to low frequency through inter-frequency modulation. The control bandwidth must be further reduced to

improve system robustness under influence of the noise. It is common practice to design the loop gain bandwidth less than one fifth of the switching frequency [Mitchell'01]. Furthermore, the switching frequency also affects system transient response by the action delay effect that is not reflected in the small signal model [Wong'02-1]. If the transient event occurs after the switch is turned off, the converter needs to wait until next switching cycle to take any action. If the switching frequency is low, this delay could be long enough to cause significant voltage drop during step-up transient of the load current. Some design modifications were reported to improve transient response by introducing duty cycle saturation in PWM modulation [Panov'01]. For example, by modifying the PWM modulator, the duty cycle is changed to zero or maximum duty cycle immediately after $v_{out}(t)$ or $v_e(t)$ is out of the preset boundaries. Because of nonlinear nature of this design, system stability cannot be predicted by the developed linear models. Tuning of the circuit parameters is necessary to guarantee system stability in all conditions.

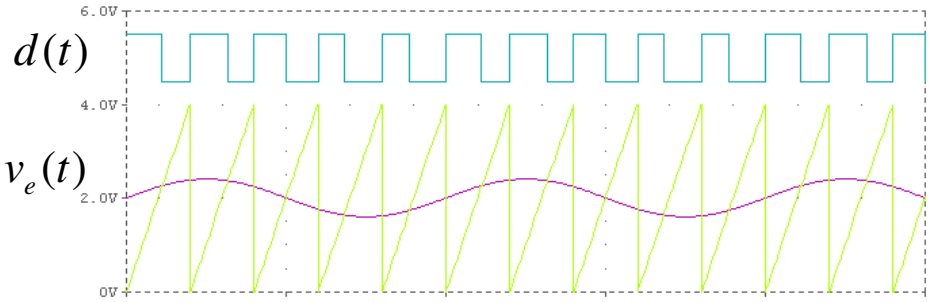


Figure 2.7 Sampling control signal with constant ramp signal

2. Output inductor

If all parasitic elements are ignored, the output filter is simplified as in Fig. 2.8. Voltage variation during the load transient is determined by the charge unbalance in the output capacitor [Wong'98]. From simplified current waveforms in Fig. 2.8, the voltage spike is estimated as:

$$\Delta v_{out} = \frac{\int [i_L(t) - i_o(t)]dt}{C_o} = \frac{I_o^2}{2C_o \left.\frac{di_L}{dt}\right|_{\max}} \qquad (2.6)$$

The maximum slew rates of the inductor current for step up and step down are determined by the input voltage, the output voltage and the inductance value:

$$\left.\frac{di_L}{dt}\right|_{up,\max} = \frac{V_{in} - V_{out}}{L}, \quad \left.\frac{di_L}{dt}\right|_{down,\max} = \frac{V_{out} + V_{diode}}{L} \qquad (2.7)$$

Here, $V_{diode} \approx 0.7V$ is the voltage drop on the body diode of the synchronous rectifier.

Since the slew rate of the inductor current is limited by the inductance value, reducing inductance helps improving system response to the load transient. The relation of the inductance and the control bandwidth was analyzed in [Wong'02-2]. In practice, there are more considerations on the inductor design. For instance, relatively large inductance is sometimes needed to improve the power efficiency or to reduce the voltage ripple. For the control design, letting the inductor currents slew with maximum slew rates during the transient gives the best performance of transient response. In another words, faster transient response can be obtained by saturating duty cycle during large load transient. However, saturated control circuits may cause trouble in stabilizing the system.

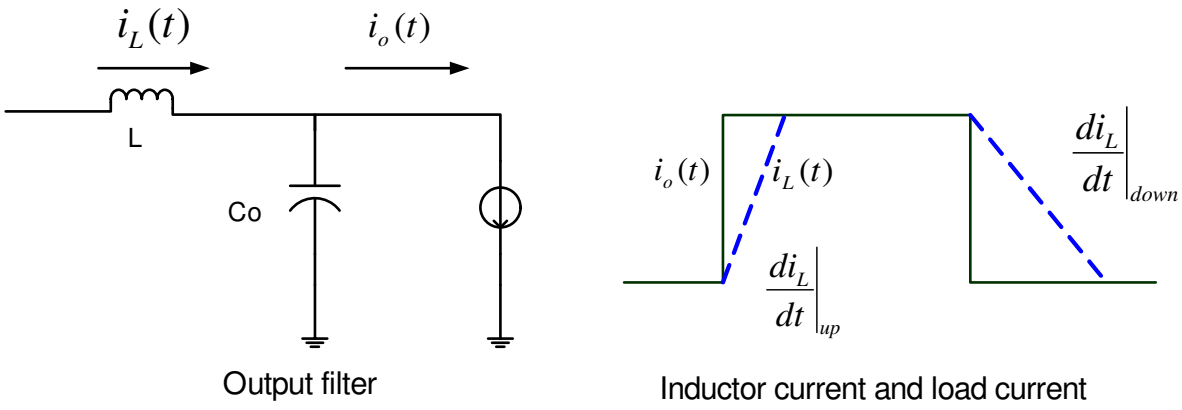


Figure 2.8 Output filter and current waveforms during transient

3. Power delivery network

Power delivery network (PDN) is the physical network from the power stage of the switching converter to the internal power bus of the load circuit [Ren'05-2]. Physical connection between the VRM and the microprocessor is shown in Fig. 2.9. A circuit model of PDN is shown in Fig.2.10. Because high current goes through PDN, the parasitic inductance and resistance in PDN play important role during the current transient. High frequency impedance made by the PDN between the power supply and the load circuits could cause excessive voltage variations or even resonance on the internal voltage bus excited by high frequency current transients [Muhtaroglu'04]. Comprehensive design efforts are needed to maintain low impedance over required frequency range, including power supply design, motherboard design, chip package design and on-chip power bus design [Ji'05] [Arabi'04]. For power supply design, the issue is usually reduced to designing the control system with proper output capacitors and optimizing layout of the power path on the motherboard. To simplify the power supply design, the load is usually modeled as a dynamic current source instead of the complex PDN. The effect of PDN is represented by the slew rate of the current source. For example, a current source with slew rate of 100 A/μs connected to the decoupling capacitors is used to model the CPU load with typical motherboard layout.

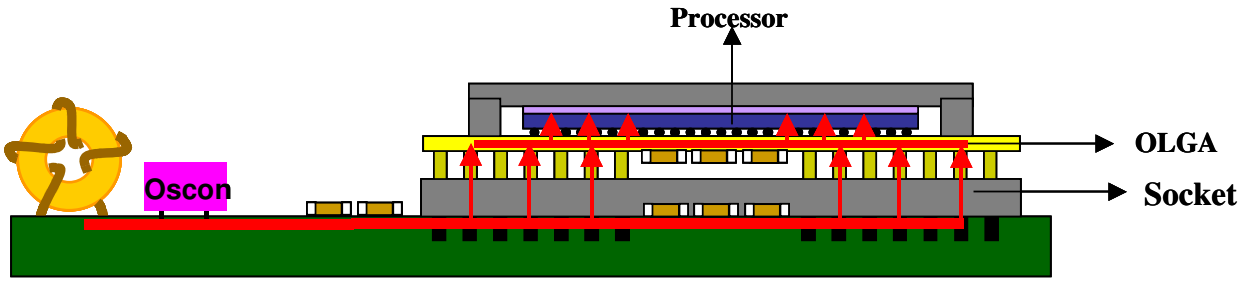


Figure 2.9 Simplified connection between VRM and CPU on motherboard

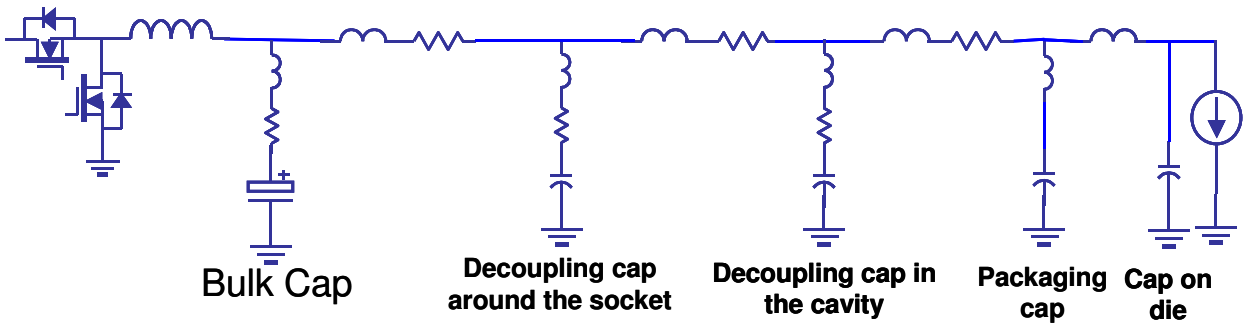


Figure 2.10 A circuit model of power delivery network between VRM and CPU

2.3 Design with adaptive voltage positioning

Adaptive Voltage Positioning (AVP) is a design approach that helps to improve load transient response of the switching DC-DC converters and reduce the amount of output capacitors required to meet the specifications [Waizman'01]. With AVP design, the output voltage varies with the load current as shown in Fig. 2.11. Compared with non-AVP design, the allowed voltage variation for full swing load transient is doubled with AVP design. The effective output impedance in ideal AVP design behaves like a constant resistance over certain frequency range. Fig. 2.12 is the load line at steady state. The slope of the load line is referred as the load line resistance or the droop resistance R_{droop}. The typical value of the droop resistance is in range of 0.5 mΩ to 3 mΩ. As the CPU

voltage gets lower, the trend of the droop resistance is getting smaller. The output voltage at steady state can be expressed as:

$$V_{out} = V_{ref} - I_o R_{droop} \qquad (2.8)$$

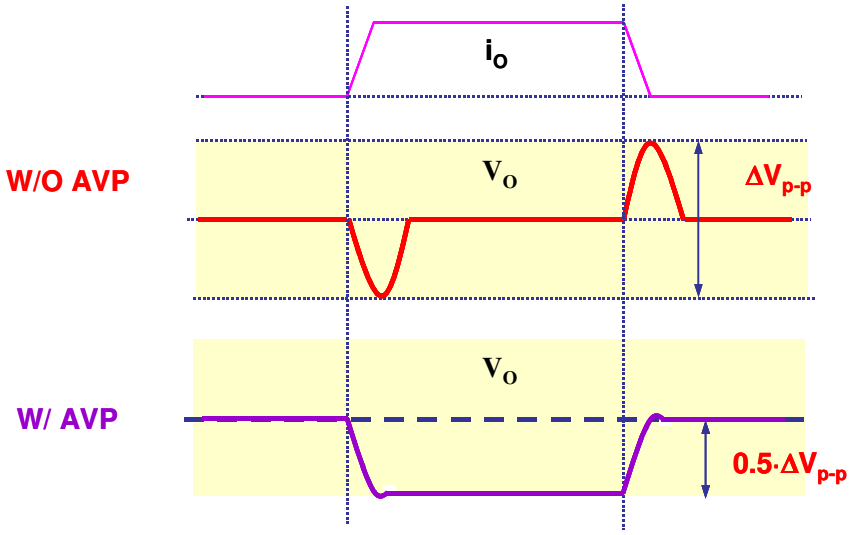


Figure 2.11 Transient voltage waveforms w/ and w/o AVP design

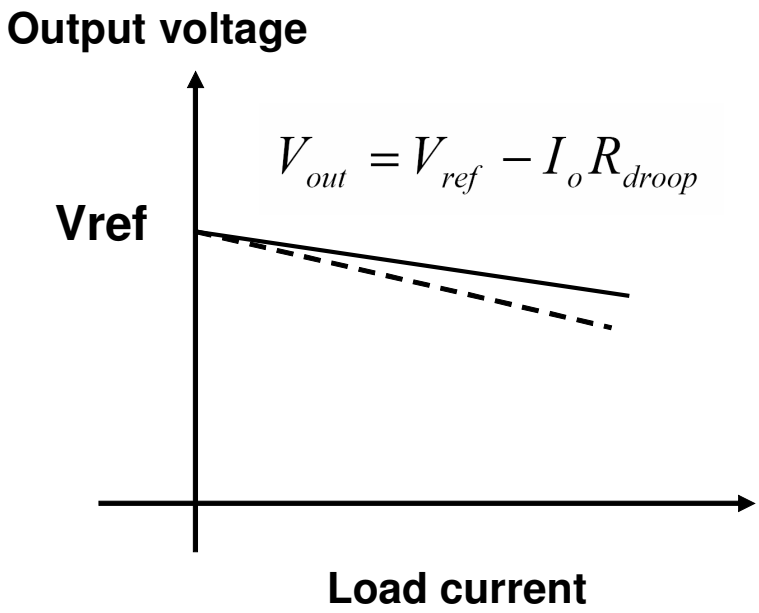


Figure 2.12 The load line of the output voltage

Implementation of AVP design is studied in [Yao'04]. The principle of AVP design is to make closed-loop output impedance flat over certain frequency range. The partial model

of the PDN is shown in Fig. 2.13. Usually, large volume electrolytic capacitors are used as the bulk capacitors, and small volume Multi-Layer Ceramic Capacitors (MLCC) are used for the high frequency decoupling capacitors. The impedance of the bulk capacitors $\boldsymbol{Z_{Cb}}$ and the impedance of the decoupling capacitors $\boldsymbol{Z_{Ce}}$ are plotted in Fig. 2.14. Because of $C_o >> C_e$, the PDN impedance is dominated by Z_{Cb} at low frequency. The PDN impedance at high frequency is determined by both Z_{Ce} and other components in PDN. With feedback control, the closed loop output impedance Z_{oc} is regulated at frequency below the bandwidth. As shown in Fig. 2.14, a good approach to achieve flat Z_{oc} is to design the control bandwidth of T_2 at $\omega_{ESR} = \frac{1}{R_c C_o}$ and $R_c = R_{droop}$. According to (2.5), the transfer function of T_2 should be designed as:

$$T_2 = \frac{\omega_{ESR}}{s} = \frac{1}{sR_C C_o} \qquad (2.9)$$

It should be noted that, in current mode control, $T_i >> 1$ is required within bandwidth of T_2 to satisfy approximation in (2.5).

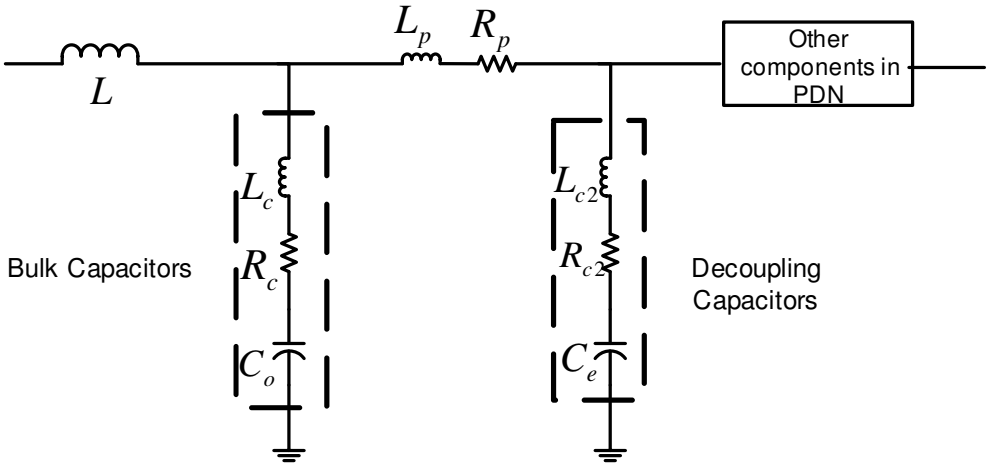


Figure 2.13 Partial model of the power delivery network

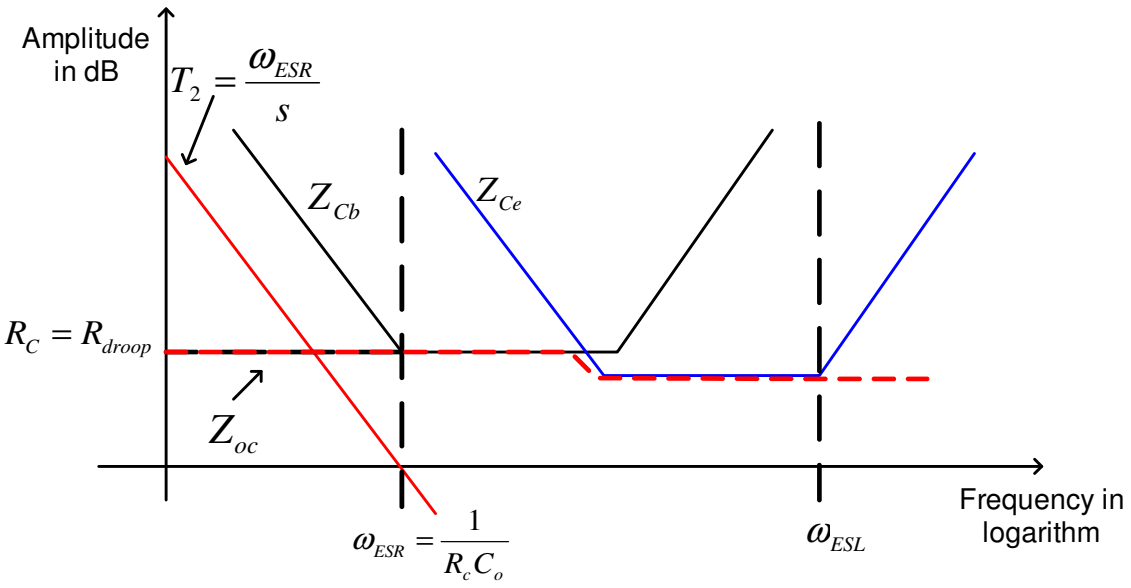


Figure 2.14 Plots of impedance for AVP design

2.4 Control with variable switching frequency

If the switching frequency is no longer constant in control, one more variable is controllable than in the constant frequency control, which gives more flexibility to the control design. The control method with variable switching frequency is sometimes referred as Pulse Frequency Modulation (PFM) control. The implementation of variable frequency control can be either single-edge or double-edge. In the single-edge control, either on time or off time is modulated while the other is kept unchanged. The examples of the single-edge variable frequency control are constant-on-time control and constant-off-time control [Ridley'90]. In the double-edge control, both on time and off time are modulated in control. The examples of double-edge variable frequency control include hysteretic voltage control [Abu-Qahouq'04], sliding mode control [Giral'00] and Delta-Sigma control [Rao'02].

2.4.1 Constant on time control

Choosing single-edge control or double-edge control is tradeoff between control flexibility and control complexity. For VRM applications, constant on time control has several advantages in practical design.

First, the input voltage of VRMs is in the range of 12 V to 20 V, and output voltage in the range of 0.5 V to 2 V. High input-voltage-to-output-voltage ratio indicates that the duty cycle is small and the on time is short at steady state. The on time of some applications could be as low as 50 ns. In circuits design, the minimum controllable time is limited by delays in the drivers and other control circuits. It is not practical to modulate the on time when the on time is close to the minimum controllable time. Besides, the current sensing circuits have limited bandwidth, usually below 10 MHz. It is difficult to sense the instantaneous current waveforms within such short on time. However, the off time is ten times longer than the on time. If the off time is modulated, it is much easier to implement the control circuits and current sensing circuits. Since high frequency switching noise has been well damped during off period, the control robustness to noise can be significantly improved with off time modulation. Secondly, the system reliability is enhanced with fixed on time. The duration of the on time determines the amount of energy transferred from the input voltage source to the load in each cycle. By fixing the on time, limited energy flows into the converter in each cycle, which helps protecting the load and the power switches when system malfunction or overloading happens.

2.4.2 Frequency regulation at steady state

In DC-DC converter design, it is beneficial to keep the steady-state switching frequency constant for simplifying power stage design and controlling noise spectrum in the

converter. For constant-on-time control under CCM, the switching frequency at steady state varies with the input voltage and the output voltage. Since the input voltage and the output voltage are varying slowly, it is possible to regulate the steady-state switching frequency by adjusting on time accordingly. If all power loss is ignored, the steady-state switching frequency of the Buck converter under CCM is:

$$f_s \approx \frac{V_{out}}{V_{in}} \frac{1}{t_{on}} = \frac{V_{ref}}{V_{in}} \frac{1}{t_{on}} \qquad (2.10)$$

If t_{on} is designed linearly proportional to $\frac{V_{ref}}{V_{in}}$, the dependency of f_s on the input voltage and output voltage can be removed. The value of f_s can be adjusted by changing the coefficient in Equ. 2.10. Circuit implementation will be discussed in Section 4.4.

2.5 Proposed control scheme with variable switching frequency

2.5.1 System architecture

The proposed control scheme employs constant-on-time current-mode control with novel system architecture illustrated in Fig. 2.15. Here R_s is the current sensing gain; $LPF(s)$ is the transfer function of the low pass filter. The current sensing amplifier and the voltage error amplifier have constant gain up to their bandwidths. Because of the 3-dB bandwidths of the amplifiers are designed much higher than the system bandwidth, the gains of the current sensing amplifier and the voltage error amplifier are simplified as the constants: A_i and A_v, respectively.

To understand the control system, the system is divided into a main control loop and an error correction loop as shown in Fig. 2.16. In the main feedback loop, the driver signal $d(t)$ is generated by comparing the outputs of the current sensing amplifier and the voltage error amplifier. Because of high bandwidth in this loop, fast transient response could be achieved. Besides, the switching frequency can instantaneously change during the transient. The transient response is no longer limited by the steady-state switching frequency. Lower steady-state switching frequency could be designed to improve the efficiency. However, the output voltage accuracy is affected by the current ripple, offset of the comparator, and delays in the loop. The additional error correction loop is added to remove the static error. With the integrator in the error correction loop, the error is amplified and injected back into the main feedback loop. A small offset added to the comparator compensates the static error introduced in the main feedback loop. Since the high frequency load transient is mainly related to the main feedback loop, the frequency response of the error correction loop can be designed much slower to guarantee the

system stability. The frequency characteristics of the two loops are illustrated in Fig. 2.17.

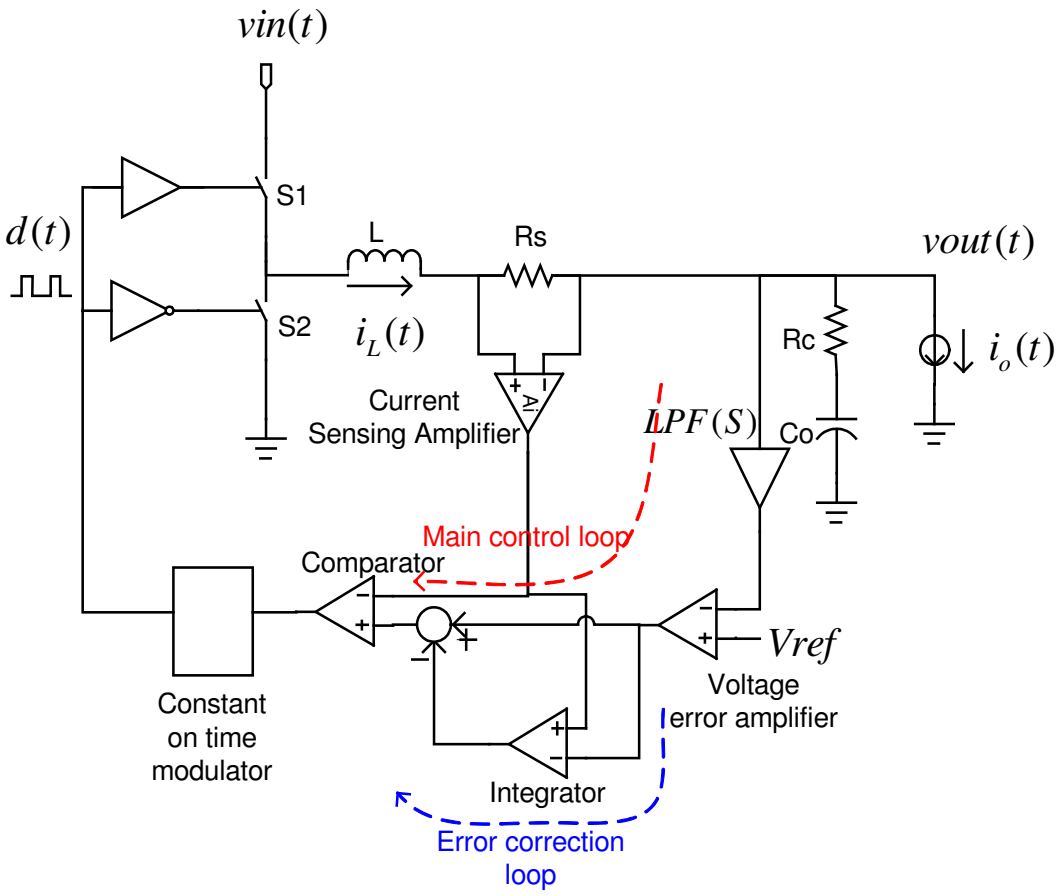


Figure 2.15 System schematics with proposed control scheme

Therefore, the proposed control scheme combines the advantages from traditional current mode control and constant-on-time variable frequency control to provide good tradeoff between transient response and steady state performance. In the proposed control architecture, the traditional compensator is replaced by several simple blocks, such as the low pass filter and the integrator, which simplifies the system design. Furthermore, the proposed control scheme provides a good approach to implement AVP design, as discussed in Section 2.5.

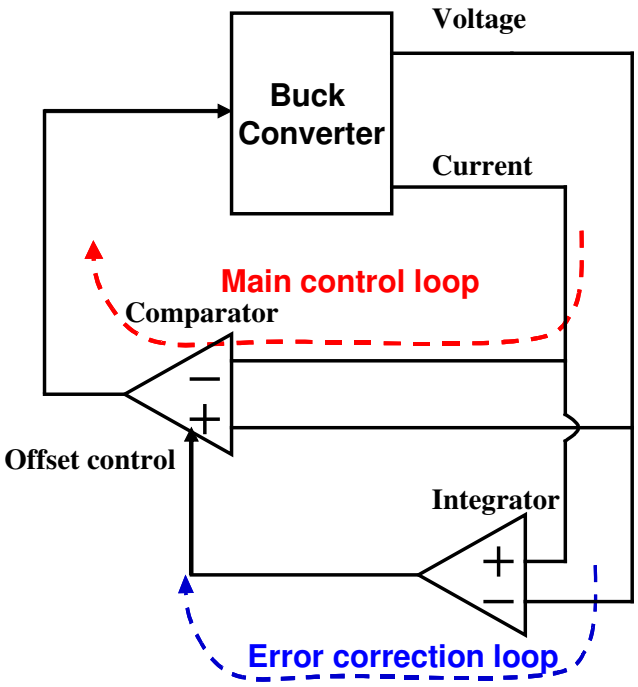


Figure 2.16 Simplified diagram showing two control loops

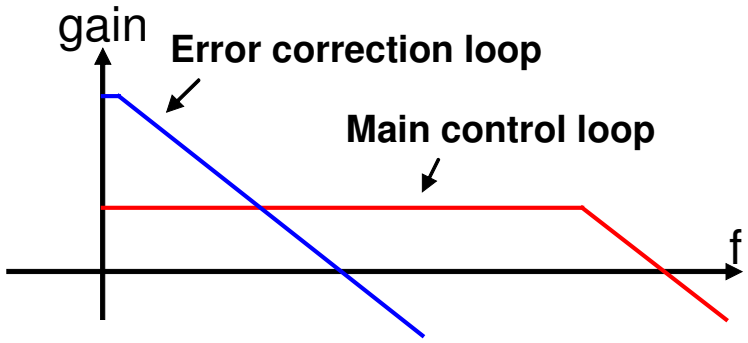


Figure 2.17 Frequency characteristics of the two control loops

2.5.2 AVP design

In Fig. 2.18, the simplified control system is drawn resembling a fully differential amplifier in a closed-loop configuration. The voltage error amplifier and the current sensing amplifier are equivalent to two input stages with finite gains. Combination of the comparator, the modulator and the power stage behaves like an output stage with high gain. The error correction loop built inside the comparator effectively removes the

systematic offset. Therefore, the differential error between the two inputs of the output stage is reduced to zero in average by the high gain. Since the outputs of the two input stages are equal in the average, the following equation is obtained:

$$< V_{ref} - v_{out} > A_v = < i_L > R_s A_i \qquad (2.11)$$

Hence: $< v_{out} > = V_{ref} - < i_L > R_s \frac{A_i}{A_v}$ (2.12)

Compared with (2.8),

$$R_{droop} = R_s \frac{A_i}{A_v} \qquad (2.13)$$

It is noticed that the droop resistance is determined by R_s and a ratio of two gains, $\frac{A_i}{A_v}$.

This arrangement has advantages to implement accurate R_{droop} with integrated circuits. As discussed in Chapter 4, the gain is determined by the on-chip components, such as the resistors. The ratio of the gains is determined by the size ratio of these components. If circuit structures of the two amplifiers are symmetric and good layout matching is achieved, it is possible to cancel the gain variations from process variations and temperature drifting. Although the droop resistance is influenced by tolerance of the sensing gain R_s, (2.13) implies that the tolerance of R_s can be simply compensated by tuning the gain of one of the amplifiers. By designing variable gain circuits, the droop resistance can be adjusted with high precision. Moreover, it is possible to reduce the value of R_s to save power loss in the current sensing circuits by designing higher gain ratio.

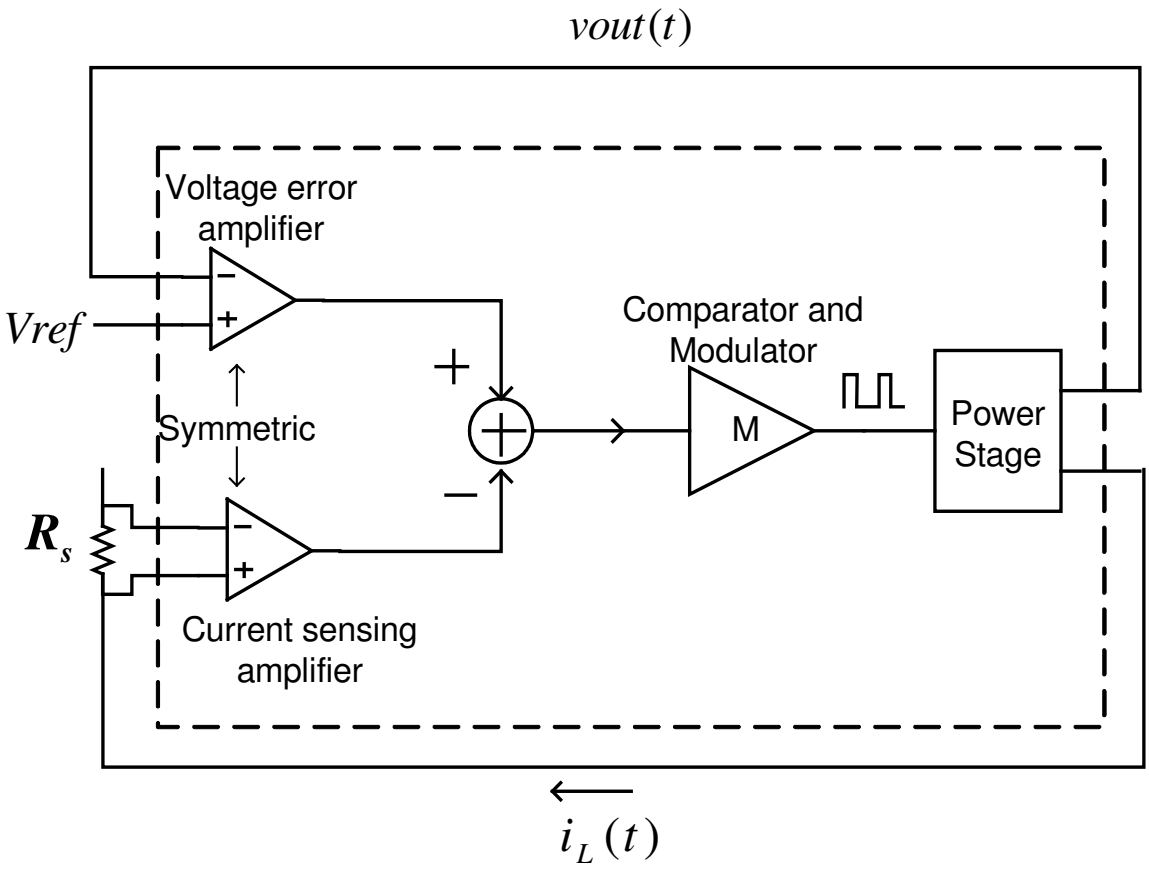


Figure 2.18 Simplified system block diagram for AVP design

2.5.3 Small signal analysis

The small signal model for the proposed control architecture is shown in Fig. 2.19. Here, $F_c(s)$ is added to model the phase lead effect in the constant-on-time control [Ridley'90], and $INT(s)$ is the gain of the integrator in the error correction loop.

$$F_c(s) = e^{sD'T_s/2} \qquad (2.14)$$

$$INT(s) = \frac{\omega_i}{s} \qquad (2.15)$$

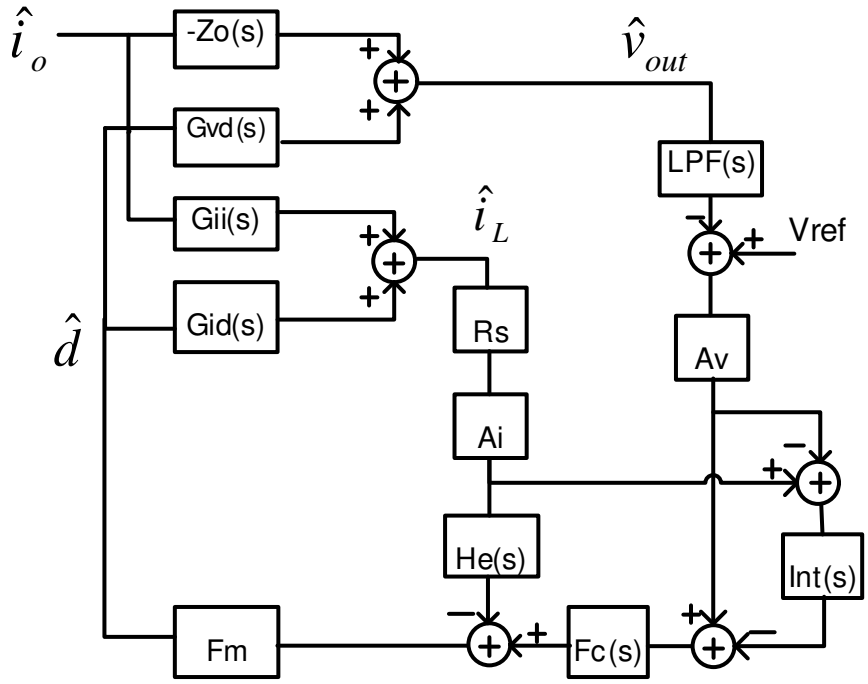


Figure 2.19 Small signal model of proposed control scheme

From the developed model, the overall voltage loop gain T can be derived:

$$T(s) = \frac{T_v}{1 + T_{i1} + T_{i2}} = \frac{LPF(s)(1 + INT(s))G_{vd}F_cF_mA_v}{1 + G_{id}F_mR_sA_iH_e(s) + G_{id}F_mR_sA_iF_cINT(s)} \qquad (2.16)$$

The voltage loop gain, T_v, and the two current loop gains, T_{i1} and T_{i2} are defined as followings:

$$T_v = LPF(s)(1 + INT(s))G_{vd}F_cF_mA_v \qquad (2.17)$$

$$T_{i1} = G_{id}F_mR_sA_iH_e(s) \qquad (2.18)$$

$$T_{i2} = G_{id}F_mR_sA_iF_cINT(s) \qquad (2.19)$$

With typical design parameters, the magnitudes of two current loop gains are relatively small at low frequency, as shown in Fig. 2.20.

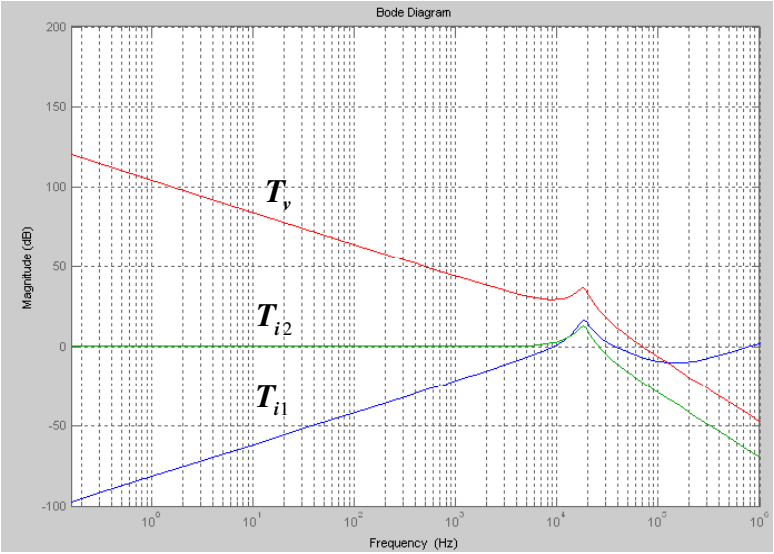


Figure 2.20 Plot of the voltage loop gain and the current loop gains

At low frequency, the overall loop gain T can be approximated as:

$$T(s) \approx LPF(s)(1+INT(s))G_{vd}F_cF_mA_v \approx LPF(s)INT(s)G_{vd}F_mA_v \quad (2.20)$$

By substituting G_{vd} from Table 2.1 and (2.15), T is further simplified at low frequency where $\omega < \omega_0$:

$$T(s) \approx \frac{LPF(s)\omega_i V_{in}(1+sR_cC_o)F_mA_v}{s(1+\frac{s}{\omega_0 Q}+\frac{s^2}{\omega_0^2})} \approx \frac{LPF(s)\omega_i V_{in}(1+sR_cC_o)F_mA_v}{s} \quad (2.21)$$

From the discussion in Section 2.3, the ideal loop gain in AVP design is $T = \frac{1}{sR_cC_o}$.

In (2.21), the ideal loop gain can be obtained by choosing:

$$LPF(s) = \frac{1}{1+R_cC_os} \quad (2.22)$$

and $\omega_i = \frac{1}{R_cC_oV_{in}F_mA_v}$. (2.23)

Since F_m and A_v are the parameters that are related to the circuits inside the controller chip, it is better to replace them with external parameters.

The modulation gain of the constant-on-time control is approximated as:

$$F_m = \frac{D}{S_f T_s} \approx \frac{D}{\frac{R_s A_i V_{out}}{L} T_s} \qquad (2.24)\ \text{[Ridley'90]}$$

Hence, the value of ω_i can be calculated from all external parameters:

$$\omega_i = \frac{R_{droop} V_{out} T_s}{R_c C_o V_{in} D L} \approx \frac{R_{droop} T_s}{R_c C_o L} \qquad (2.25)$$

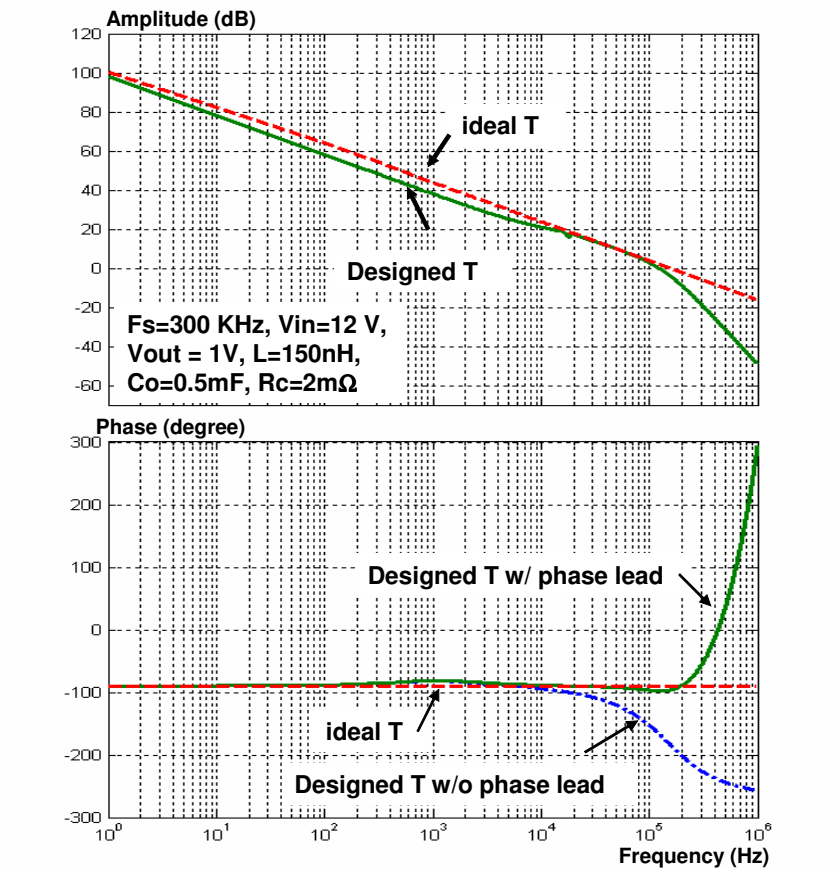


Figure 2.21 Bode plot of open loop gains

With the design guidelines in (2.22) and (2.25), implementation of control loop is simplified to design a first-order low pass filter and an integration capacitor. Once the parameters, such as R_{droop}, T_s, L, are decided in design, output capacitance C_o can be chosen as a variable to determine the system bandwidth and to calculate the rest of design

parameters. Fig. 2.21 shows an example of designed loop gain. It is noticed that the phase margin is significantly boosted by the phase leading effect in the constant-on-time control. The designed loop gain is very close to the ideal loop gain.

At the high frequency range that is close or beyond half of the steady state switching frequency, the assumption of the small signal model is no longer valid. Furthermore, the small signal analysis presented above assumes the switching frequency is constant, which is not accurate to predict large signal transient. As shown in Fig. 2.22, the switching frequency is significantly changed when large perturbation is applied during large load transient.

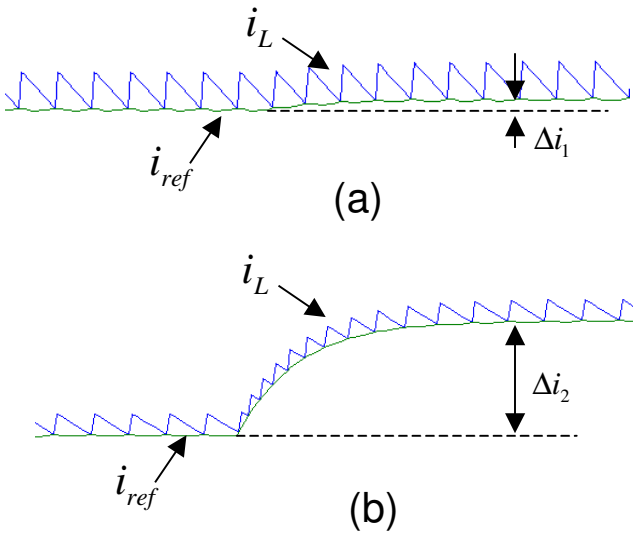


Figure 2.22 Current transient waveforms under small and larger perturbations

Therefore, a new model is used to predict the system response with large signal transient. The assumption of the model is that the inductor current will follow the envelop generated by the voltage error amplifier, and the difference between the average value and bottom envelop value of the inductor current is negligible. This assumption is satisfied only if the duty cycle is not saturated (or the duty cycle does not reach its

maximum or minimum boundaries during the transient), and the perturbation amplitude is much larger than the ripple of the inductor current. Once the assumption is satisfied, the inductor current is simplified as a voltage-controlled current source with the gain of $\frac{-1}{R_{droop}}$, as shown in Fig. 2.23. The output impedance can be derived as:

$$Z_{oc} = -\frac{\hat{v}_o}{\hat{i}_o} = \frac{R_c + \frac{1}{sC_o}}{1 + (R_c + \frac{1}{sC_o})\frac{LPF(s)}{R_{droop}}} \qquad (2.26)$$

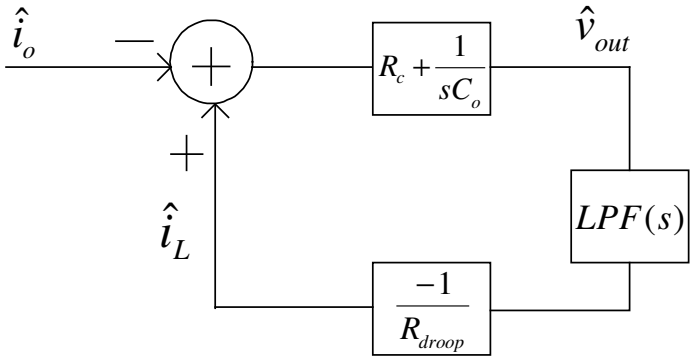


Figure 2.23 Simplified feedback loop to analyze transient response

By substituting (2.22) and assuming $R_{droop} = R_c$, the output impedance in (2.26) is simplified as $Z_{oc} = R_{droop}$. From the new model it is concluded that, given the assumption is satisfied, the system can maintain the output characteristics as required for large load transient. The prediction of transient response by the model is verified by comparing circuit simulation results and model simulation results at the transient, as shown in Fig. 2.24.

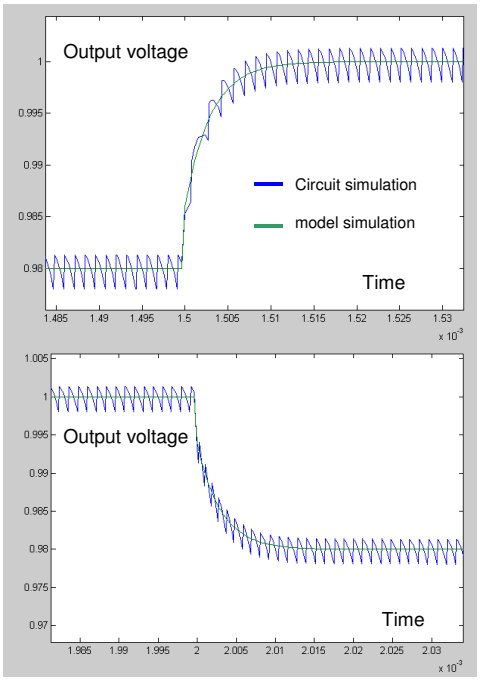


Figure 2.24 Comparison of results of circuit simulation and model simulation at transient

2.5.4 Comparison with peak current control

A case study was performed to compare the performance of the proposed control scheme and the traditional peak current control. Two control systems were designed with the same parameters listed in Table. 2.2:

Table 2.2 Parameters for control system design

Input voltage	12 V
Output voltage	1 V
Steady-state switching frequency	300 KHz
Inductor	150 nH
Maximum load current	20 A
Current sensing gain $\boldsymbol{R_s}$	2 mΩ
Lumped ESR of output capacitors $\boldsymbol{R_c}$	2 mΩ
AVP droop resistance $\boldsymbol{R_{droop}}$	2 mΩ

The simulation models were built with Simulink in Matlab, as shown in Fig. 2.25 and 2.26.

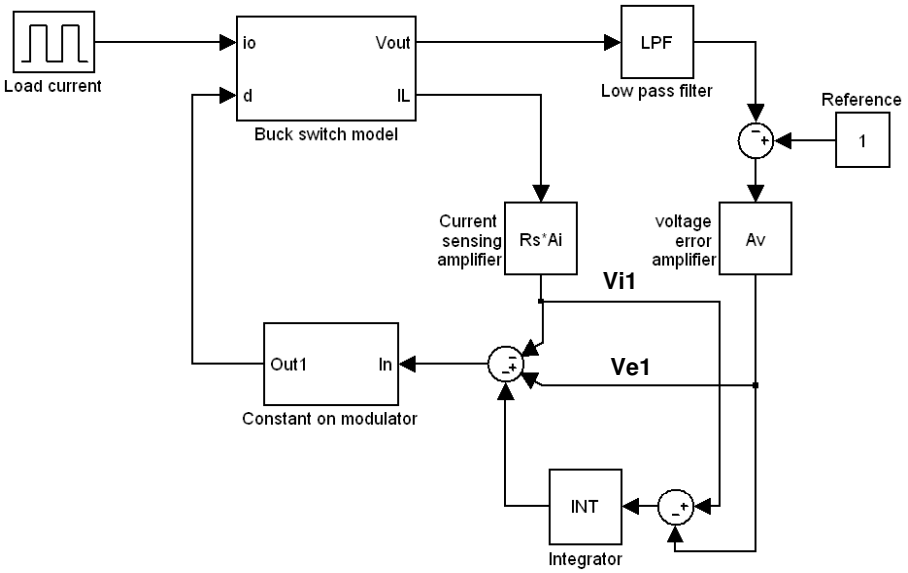


Figure 2.25 Simulation diagram for proposed control

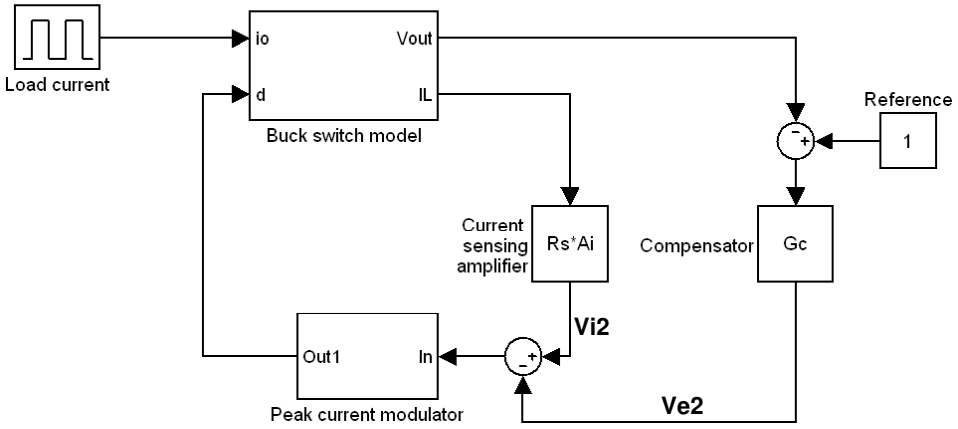


Figure 2.26 Simulation diagram for peak current control

Here, A_i and A_v are modeled as the unit gain amplifiers with 3-dB bandwidth at 1 MHz:

$$A_i(s) = A_v(s) = \frac{1}{1 + s/6.28\times10^6} \qquad (2.27)$$

The low pass filter LPF and the integrator INT in Fig. 2.23 are designed as followings:

$$LPF(s) = \frac{1}{1 + sR_cC_o} = \frac{1}{1 + sC_o \times 0.002} \qquad (2.28)$$

$$INT(s) = \frac{10^3}{s} \qquad (2.29)$$

According to [Yao'04], the compensator for peak current control, G_c, is designed as:

$$G_c(s) = \frac{R_s}{R_c}\frac{1+\frac{s}{\pi f_s}}{1+sR_cC_o} = \frac{1+\frac{s}{9.4\times10^5}}{1+sC_o\times0.002} \qquad (2.30)$$

As non-idealities in the circuits, 10 mV offset voltage and 10 ns delay time were added to the modulators in both systems.

The systems were simulated with the output capacitance C_o as a variable. In Fig. 2.27, the waveforms show that both systems have stable switching with output capacitance equal to 1 mF. However, the system with the peak current control has apparently larger voltage error at steady state than the system with the proposed control. The DC error in the peak current control system is caused by low DC gain in the feedback loop.

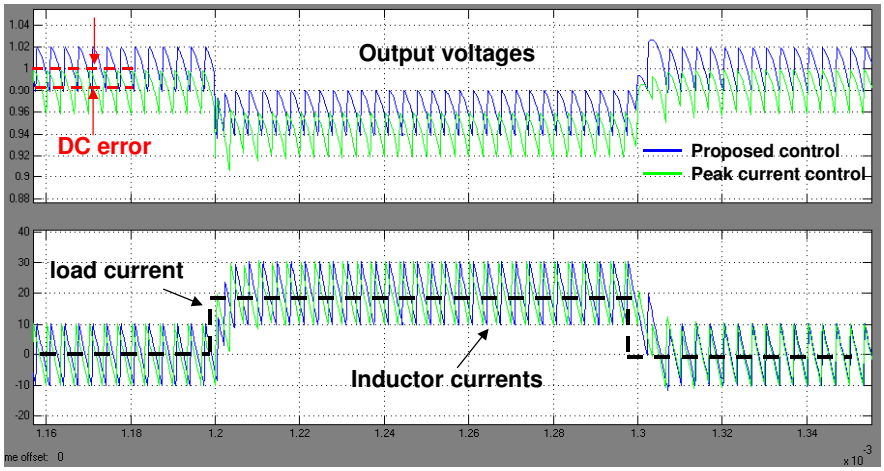


Figure 2.27 Simulation waveforms with output capacitance of 1 mF

The internal control signals, i.e. outputs of current sensing amplifiers and error amplifiers, are plotted in Fig. 2.28. It is noticed that the ripples on Ve2 have larger amplitude than that on Ve1. The larger ripples on the control signal make the system with the peak current control more sensitive to the noise. Because the compensation in the

peak current control (Equ. 2.30) is designed with one zero added at half of the switching frequency, less attenuation is resulted for high frequency noise. Since in this design approach [Yao'04] the zero is intentionally added to help system stability by increasing phase lead in the loop, high bandwidth is not adequate for poor noise immunity.

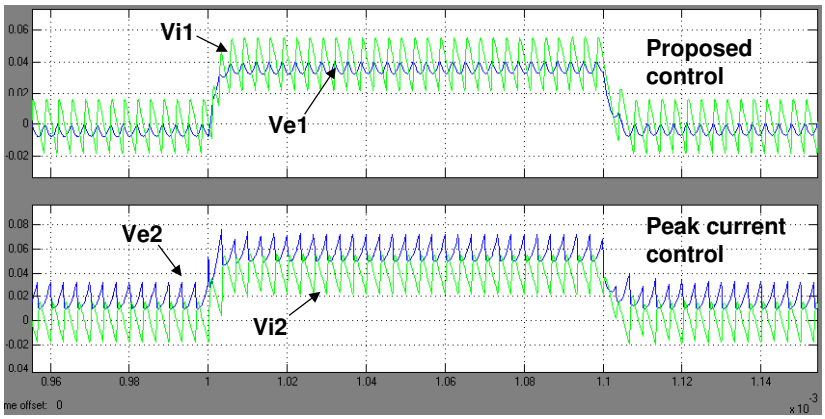


Figure 2.28 Internal control signals in two systems (Co=1mF)

The value of output capacitance was further reduced to test the system performance at higher frequency. With output capacitance equal to 0.4 mF, the results in Fig. 2.29 show that the system with the peak current control was no longer stable. However, the system with the proposed control is still stable and shows good regulation and load transient response.

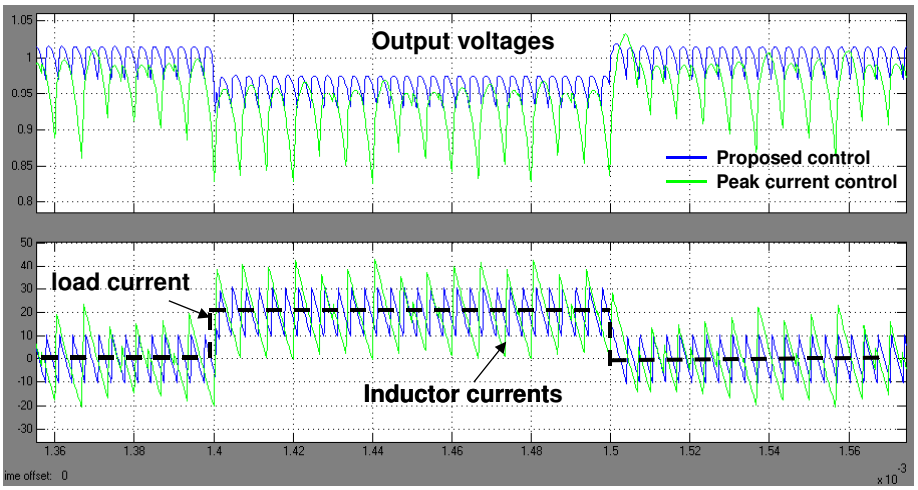


Figure 2.29 Simulation waveforms with output capacitance of 0.4 mF

It is shown by the comparison study that the proposed control scheme has apparent advantages over the peak current control, including static regulation and system dynamics. Most importantly, with the proposed control scheme, it is possible to achieve higher control bandwidth without requiring higher switching frequency.

2.5.5 Power efficiency and control bandwidth

As mentioned in Chapter 1, the tradeoff of the power efficiency and the control bandwidth is a fundamental problem for the switching DC-DC converters. From previous discussion, the ideal bandwidth of control to achieve constant output impedance is $\omega_{ESR} = \frac{1}{R_c C_o}$. Given that R_c, ESR of the output capacitor, is fixed in the design, the less output capacitance is used, the higher control bandwidth is required. The highest control bandwidth that can be achieved in the design is related to the switching frequency and the control scheme. In general, the higher switching frequency is used, the higher control bandwidth can be designed. The ratio of the highest control bandwidth, f_c, and the averaged switching frequency, f_s, is denoted as λ:

$$\lambda = \frac{f_c}{f_s} \qquad (2.31)$$

From the comparison in Section 2.5.4, the proposed control scheme has higher ratio factor λ than the peak current control.

On the other hand, the power efficiency has opposite trend with the switching frequency. The power loss of the DC-DC converter can be expressed as:

$$P_l = P_{sw}(f_s) + P_{con1} + P_{con2}(f_s) \qquad (2.32)$$

Here, P_{sw} is the switching loss caused by the voltage and current overlaps during switching, deadtime between conduction of high side and low side switches, the loss in the driver, etc. These losses are related to switching events, so they are roughly proportional to the switching frequency.

$$P_{sw} = E_{sw} f_s \qquad (2.33)$$

Here, E_{sw} is the total energy loss in one switching cycle.

In (2.32), P_{con1} is the part of the conduction loss that is independent of the switching frequency, and P_{con2} is another part of the conduction loss that is related to the ripple of the current. The conduction loss is the resistive loss when the current flows through the switches and the inductor. Since the RMS value of the current changes with the ripple amplitude, the conduction loss is related to the switching frequency through the changes of the ripple amplitude. To show this dependency clearly, the conduction loss is divided into two portions: P_{con1} is determined only by the DC level of the current, P_{con2} is determined only by the ripple amplitude, I_{ripple}:

$$P_{con1} = R_{total} I_o^2 \qquad (2.34)$$

$$P_{con2} = \frac{1}{3} R_{total} I_{ripple}^2(f_s) = \frac{R_{total} D^2 V_{in}{}^2}{12 L^2 f_s^2} \qquad (2.35)$$

Here, $D = \frac{V_{out}}{V_{in}}$ is the duty cycle; I_o is the load current in the steady state; R_{total} is the total resistance on the current path, including the on resistance of the high side switch, R_{on_hi}, the on resistance of the low side switch, R_{on_low}, and the resistance of the inductor and metal traces, R_L.

$$R_{total} = D \cdot R_{on\_hi} + (1-D) \cdot R_{on\_low} + R_L \quad (2.36)$$

From (2.32) through (2.35), the total power loss is estimated as:

$$P_l = E_{sw} f_s + R_{total} I_o^2 + \frac{R_{total} D^2 V_{in}^{\ 2}}{12 L^2 f_s^2} \quad (2.37)$$

The power efficiency is:

$$\eta = \frac{P_o}{P_l + P_o} = \frac{V_{out} I_o}{P_l + V_{out} I_o} \quad (2.38)$$

A set of typical parameters listed in Table 2.3 is used to calculate the power efficiency under different switching frequency. Note that E_{sw} in Table 2.3 is empirical data measured from the simulation with the device models.

Table 2.3 The list of parameters to calculate the efficiency

Vin	Vout	Io	D	R_{on_hi}	R_{on_low}	R_L	L	E_{sw}
12V	1V	20A	1/12	8mΩ	2mΩ	2 mΩ	400nH	13uJ

Fig.2.30 plots the calculated power efficiency versus the switching frequency. It is shown that power efficiency peaks at the frequency, f_{s_opt}, about 60KHz with the parameters listed in Table 2.3. It is concluded that the switching loss (the first term in Equ. 2.32) is the dominant power loss when the switching frequency is beyond f_{s_opt}, and the ripple-introduced loss (the third term in Equ. 2.32) is the dominant power loss when the switching frequency is below f_{s_opt}.

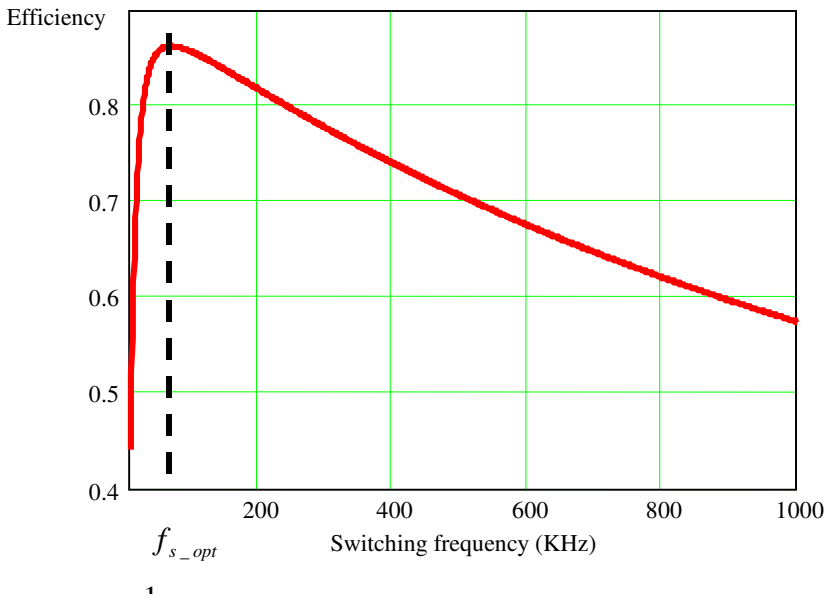


Figure 2.30 Efficiency versus switching frequency

By combining (2.31) and (2.38), the relation of the power efficiency and the control bandwidth can be derived. If the control bandwidth is design as $f_c = \frac{1}{2\pi R_c C_o}$, the relation of the power efficiency and the output capacitance can also be derived. Fig. 2.31 shows the calculated power efficiency versus the output capacitance with the ratio factor λ varying from $\frac{1}{10}$ to $\frac{1}{3}$.

In Fig. 2.31, it is clearly shown that the higher power efficiency can be obtained by increasing the ratio factor λ. It confirms the advantage of the proposed control scheme since the proposed control scheme has higher λ than the conventional control with constant switching frequency. The improvement is more significant when less output capacitor is used or the higher control bandwidth is designed. With the proposed control scheme, the control bandwidth can even been pushed close to half of the steady state

switching frequency without getting into instability. Although the model used in analysis may not be accurate at such high frequency, the qualitative trend is evident.

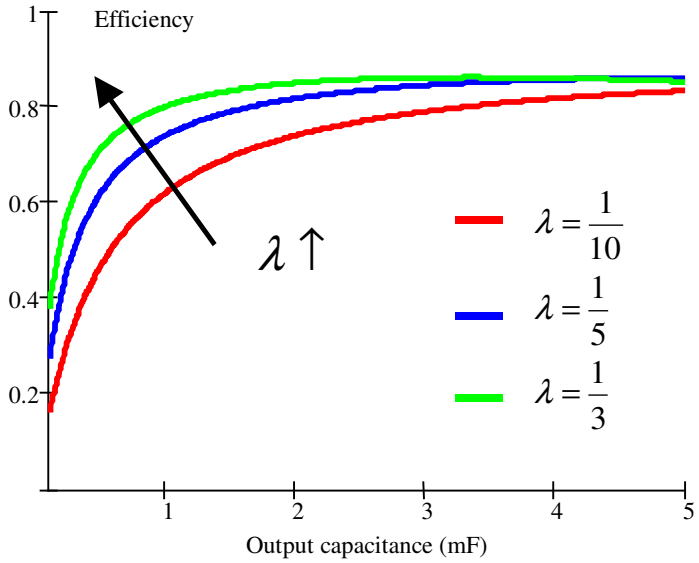


Figure 2.31 Efficiency versus output capacitance

After all, the control bandwidth is not only limited by the switching frequency, but also by some other factors, such as circuit performance, noise immunity and duty cycle saturation. Some of these limitations are discussed in Section 2.5.6.

2.5.6 Bandwidth limitations

1. Noise in the control signals

With higher control bandwidth, more noise could be coupled into the feedback loop. As shown in Fig 2.28, the ripples on the control signal from the error amplifier is considerably large at steady state. Although in the simulations the noise could be damped in the feedback loop, circuit nonlinearity in the real system could mix the noise with low frequency control signal and cause abnormal switching behavior at steady state. To attenuate the noise effectively, it is better to design the control bandwidth less than one

third of the switching frequency or even less. Since system's sensitivity to noise is largely related to the real implementation of control circuits and power stages, the circuits presented in Chapter 4 intend to improve noise immunity so that larger control bandwidth could be achievable in the practical design.

2. Duty cycle saturation

The system transient response not only depends on the control bandwidth, but also the output inductor. When the duty cycle is saturated during the transient, the inductor current slews with its maximum rates, as shown in Fig. 2.8. From the critical inductor theory in [Wong'02-2], the control bandwidth that makes duty cycle saturate during large transient is determined as:

$$\omega_{crit} \approx \frac{(\pi/2)V_{in}}{\Delta I_o L}\Delta D_{\max} \qquad (2.31)\ \text{[Wong'02-2]}$$

Here, $\Delta D_{\max}$ is the maximum variation of duty cycle during the transient.

For the step-down transient in which the load current steps from maximum level to zero, the critical bandwidth is much less because $\Delta D_{\max}$ is much smaller than in the step-up transient. With the parameters in the Table 2.2, the critical bandwidth is about 100 KHz. A useful strategy in the design is to choose the control bandwidth equal to the critical bandwidth so that the system utilizes the maximum potential at transient response.

2.6 Summary of Chapter 2

In Chapter 2, the background of the PWM control is reviewed. The conventional control architectures for the PWM control and the small signal model used for analyzing the control system are discussed. Because the load transient response is the most important specification for the control design, the limiting factors of the load transient response are identified and discussed, including the switching frequency, the output inductor and the power delivery network. An important technique to improve transient performance, AVP design, is discussed.

For overcoming the limitation of the constant frequency PWM control, the control architecture based on current mode and variable switching frequency is proposed in this Chapter. This control architecture features a unique method to implement the AVP design. The symmetric structure provides practical way to implement the control with the integrated circuits. A small signal analysis is performed to analyze the system dynamics and provide the design guidelines. Finally, the comparison between the proposed control scheme and the conventional peak current control is studied. The study proves the advantages of the proposed control over the peak control. Some further considerations regarding bandwidth limitation and duty cycle saturation are discussed.

Chapter 3 Integrated Controller for Switching DC-DC Converters

3.1 Introduction

Typical high current multi-channel switching DC-DC converters are implemented with several integrated chips and some discrete power components, as shown in Fig. 3.1 [Intersil-2]. The choice of this configuration results from tradeoff of the cost, technology capability and application requirements. Because the power switches are traditionally manufactured with vertical technology to obtain good device performance, currently they are not compatible with the lateral technology used for driver chips and controller chips. However, packaging level integration of drivers and power switches is feasible and becomes a trend in industry nowadays [Renesas]. Since the controller and the drivers are implemented with similar technology, there is no technical obstacle to integrate both of them on the same dies. The tradeoffs are design flexibility and the cost.

The controller is circuit implementation of the control schemes such as the examples shown in Fig. 2.3 and Fig 2.4. Major blocks of the current mode controller include the error amplifier, the current sensor and the modulator. Specifically, the error amplifier senses the voltage signals from the power stage and amplifies the voltage error. Typical error amplifiers (also called compensators) are low pass filters with high gain at low frequency and phase compensation at certain frequency range. Frequency characteristics of the error amplifier are critical for system performance such as stability and transient response. The current sensing circuit measures the current in the inductors or the switches for control and protection purposes. The current sensing circuit is often challenging in design because the circuit must deal with the issues, such as low signal-to-noise ratio,

variation tolerance, temperature drifting. With sensed current signals and amplified voltage error signals, the modulator is used to generate the pulse signals as the outputs of the controller. To some degree, the modulator is similar to Analog to Digital Converter (ADC) since the modulator also converts signals from continuous-time domain to discrete-time domain under certain rules. The comparator is a basic element to implement both the modulator and ADCs. In the multi-channel controllers, the collaboration between different channels, such as the current sharing and the phase interleaving, are also required.

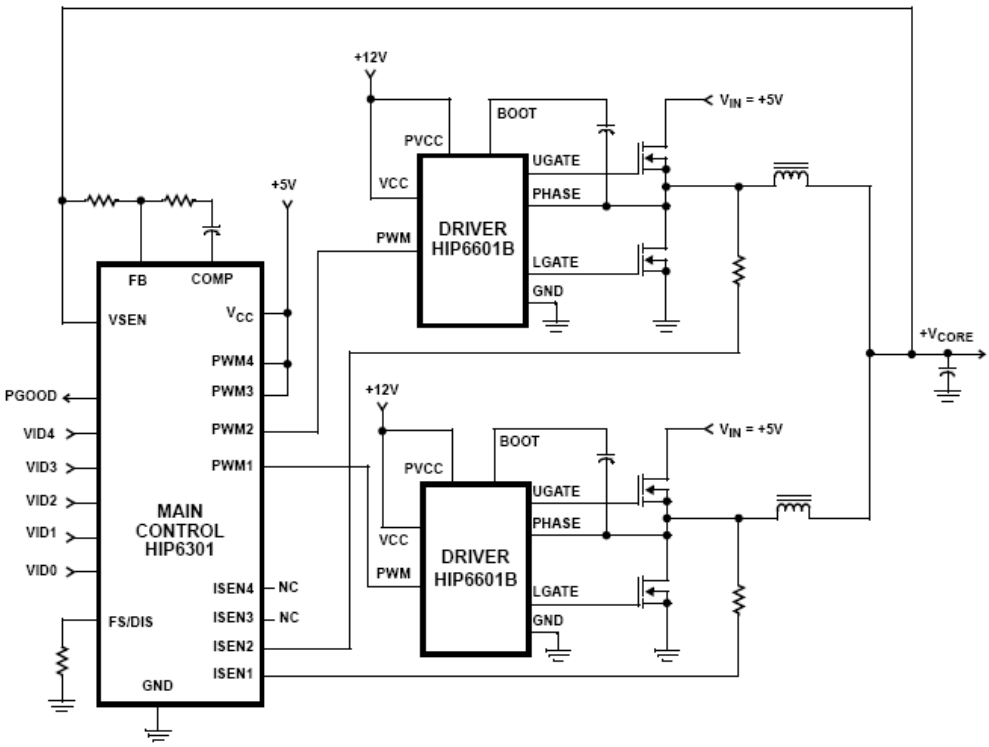


Figure 3.1 Two-channel DC-DC converter designed with commercial chips

Besides the basic functions, the commercial controller usually has to include protection functions for both the load and the power supply itself, for instances, short circuit protection, over voltage protection, input under voltage protection and over temperature protection. To have smooth operation at initial period after the converter is started, soft

startup function is also needed in the controller. The voltage reference and the current reference in the controller are generated with high precision bandgap circuit. Additionally, the Digital to Analog Converter (DAC) that produces dynamic reference voltage controlled by the digital signals from the CPUs is required in the VRM applications. Since the output voltage of the DC-DC converter need be very accurate in VRM applications, the trimming circuits are often necessary to reduce errors from process variation and temperature drifting. Fig. 3.2 shows an example of functional blocks of a commercial 4-channel controller.

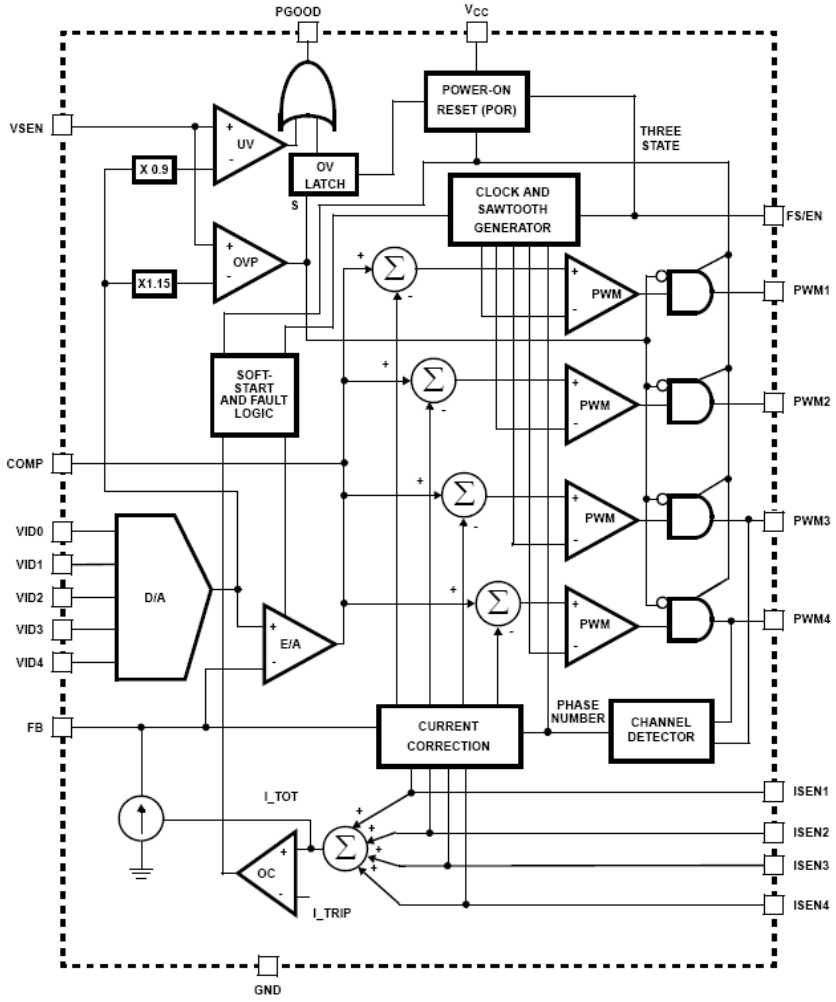


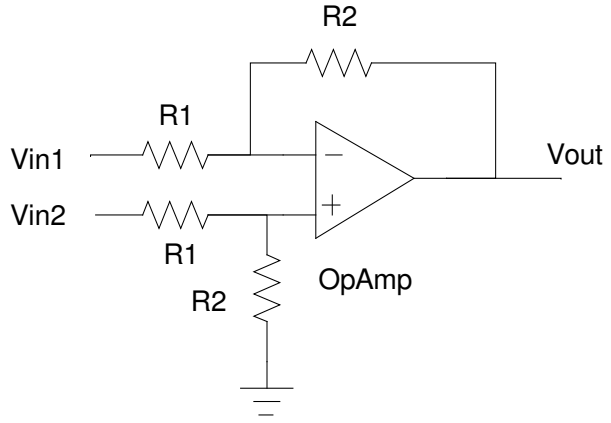
Figure 3.2 Block diagram of a commercial controller chip (HIP6301)

For the controller design, the basic objective is to meet all specifications required by the load of the DC-DC converter, such as Intel's Pentium 4 CPU. The details of these specifications include power efficiency, accuracy of static output voltage, amplitude of the voltage ripples, slew rate of dynamic output voltage, voltage variation under load transient, etc [Intel-2'04]. Besides, other important objectives in the controller design include simplifying the application design and reducing the application cost. To achieve these, the controller design should minimize sensitivity to parasitic effects and noise from external circuits, and also the controller should minimize the number of external components in the applications. In the commercial controllers, most of functions are implemented with analog integrated circuits. The methodology of the analog circuit design for the controller is discussed in Section 3.2. Issues with noise and current sensing are discussed in Section 3.3 and 3.4. Finally, the implemented controller is introduced in Section 3.5.

3.2 Design methodology of control circuits

Analog circuits design for the controller was historically dominated by the voltage approach in which signals are represented by the voltage. The usage of Operational Amplifiers (OpAmp) greatly enhanced the capability of the analog design. Various functions can be synthesized by the OpAmps connected with on-chip or off-chip passive components, such as resistors and capacitors. For example, Fig. 3.3 shows a voltage subtraction circuit designed with the OpAmp. The closed-loop OpAmp-based circuits enjoy good linearity and accuracy partially due to high voltage gain of the OpAmp. However, the circuits' dynamic performance is limited by characteristics of the OpAmps. In a closed-loop amplifier implemented with the OpAmps, the gain-bandwidth product of

the amplifier is limited and determined by the OpAmp. Therefore, the bandwidth is lower when high DC gain is required. With conventional 0.5μm CMOS technology, the gain bandwidth product of the OpAmp is around tens of Mega Hertz with reasonable power consumption of the circuits. Low gain design is more preferable for high bandwidth amplifier. Besides, implementation of complex functions with voltage approach might not be cost effective because much of silicon area is needed to realize on-chip resistors and capacitors. Especially, high value resistors are sometimes necessary to reduce power consumption or to increase input impedance.



$$V_{out} = (V_{in2} - V_{in1})\frac{R2}{R1}$$

Figure 3.3 A voltage subtraction circuit implemented with OpAmp

Alternatively, analog circuits in the controller can be designed with the current approach in which signals are represented by currents. Since the transistor by nature is a voltage-controlled current source or a transconductor, circuit design for processing current signals could be much simpler than its counterpart for processing voltage signals [Lee'04]. As an example, Fig. 3.4 shows a current-mode adder. With the current approach, some complicated non-linear circuits, such as analog multiplier and nonlinear gain amplifiers,

can be implemented with relatively lower cost [Chen'03]. More importantly, the frequency response of current mode circuits is much faster than voltage mode circuits. It has been shown that the transistors can be used approximately up to intrinsic frequency f_T [Toumazou'90]. Because of low voltage swing at internal nodes of the current mode circuits, parasitic capacitance has less influence on circuits' frequency response. The current mode circuits designed with CMOS technology has been used around 100 MHz [Nauta'92]. Besides, with the current approach the requirement on the supply voltage is reduced. Since polarity of the current signal can be simply defined by its direction, dynamic range of the signals is doubled without using bi-directional supply voltage. Because maximum swing of the signals is mainly determined by the bias current instead of the supply voltage, lower supply voltage is possible in the current mode circuits [Pennisi'02].

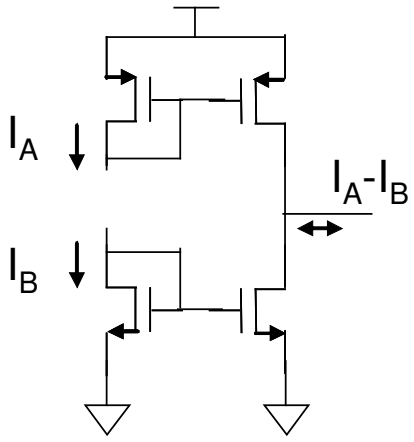


Figure 3.4 A current subtraction circuit

However, there are disadvantages with the current approach [Toumazou'90]. For example, large signal linearity and gain accuracy of the current mode amplifier are usually poor in the design. Tuning circuits are sometimes necessary to achieve good accuracy. Noise immunity could be a problem in high bandwidth current mode circuits.

Sometimes more power consumption is resulted to increase amplitude of the current signals.

The good design practice is to combine the merits of both voltage mode circuits and current mode circuits. As discussed in Chapter 4, the most important circuits in the controller in terms of accuracy and noise sensitivity are the control core circuits that include the current sensing amplifier, the voltage error amplifier and the modulator. These circuits form the feedback loop in the whole converter and fulfill the basic function of the controller. To have optimal performance, the frond-end of the control core circuits can be designed with voltage mode amplifier with low DC gains. Because these voltage amplifiers are interface between power stage and the controller, noise must be shielded by these amplifiers from going inside the controller. After the front-end voltage amplifier, the signals are converted into currents by transconductance amplifiers. By taking advantages of these preconditioned current signals, following circuits in the controller, such as the modulator and the current balancing circuits, are greatly simplified. Because the current signals can be transferred without being affected by the transistor mismatches, the current signals can travel long distance from blocks to blocks on the die. Therefore, complicate functions and internal communication are implemented with current mode circuits. Finally, before the signals go out of the controller, they are converted back to voltage because traditionally most chip-to-chip interface is designed with voltage signals only.

3.3 Noise issue in integrated controllers

Compared with other analog integrated circuits, power management circuits have severe working environment due to noise. In fact, noise is one of major reasons for design

failure of the power management circuits. It is important to understand the mechanism how noise is generated and transferred in switching DC-DC converters. In this Section, three types of the noise coupling from ambient to the controller chip are discussed.

The first type of noise coupling is through signal sensing circuits. Shown in Fig. 3.5, stray resistance R_p and stray inductance L_p in the PCB interconnections are in the order of milli-Ohm and nano-Henry, respectively. With high static current and high current slew rate di/dt going through these elements, voltage spikes and steps are generated at inputs of current and voltage sensing circuits. The noise amplitude is comparable or even higher than the real signals. Fig. 3.6 shows measured waveforms on two input terminals of the current sensor. The amplitude of common mode noise is more than five times larger than the actual signal, the differential voltage between the two inputs. If the noise is not well attenuated, the control signals inside the chip can be significantly distorted and chaotic switching could occur as a result [Tse'03]. Fig.3.7 shows an example of the control signal corrupted by the noise.

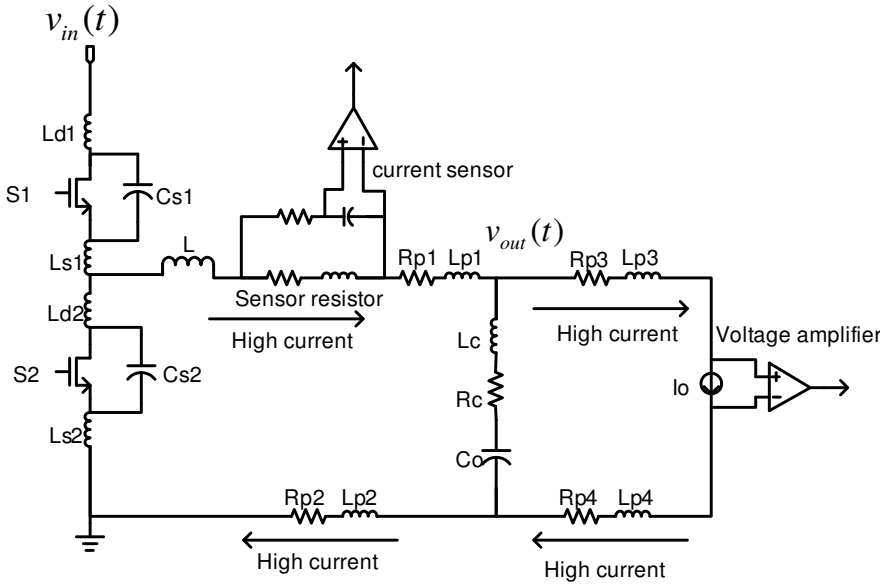


Figure 3.5 The parasitic elements that generate noise in current and voltage sensing

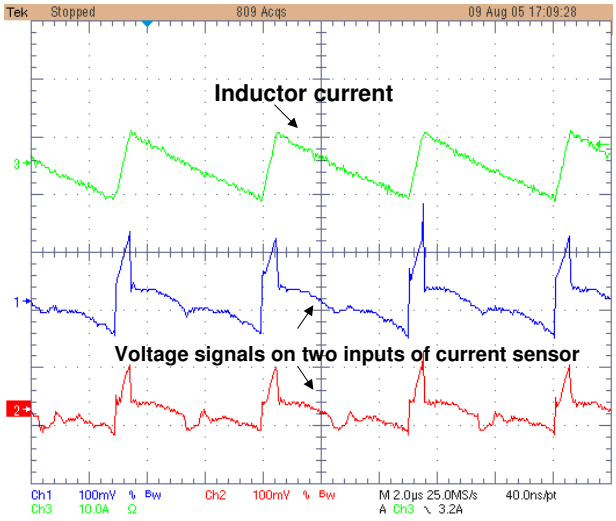


Figure 3.6 Measured signals at inputs of current sensor

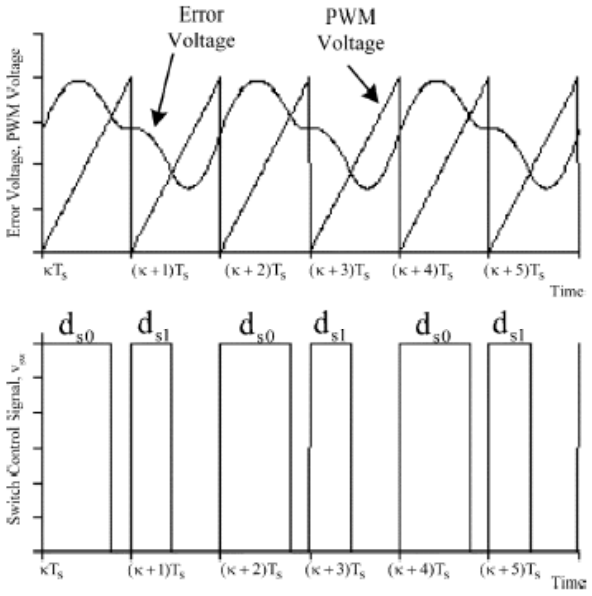


Figure 3.7 Sub-harmonic switching caused by noise in error signal

The second important path for noise coupling is through the power supply of the controller, especially through grounding connections. In practical design, the load, the input power source and the power supply of the controller are electrically connected on the PCB. As shown in Fig. 3.8, the PCB metal trace introduces parasitic resistance and parasitic inductance on the current paths. The signal ground and the power ground are coupled through resistive connection and parasitic capacitance. Although most of noise

in the power supply of the controller is generated as common mode noise, the noise could be converted into differential-mode noise by asymmetric impedance in the internal nodes. It is helpful to add decoupling capacitors between VDD and the ground. Since the decoupling capacitors provide a low impedance path between VDD and ground at high frequency, high frequency noise can be significantly reduced. However, the effectiveness of the decoupling capacitors is limited by the series resistance and the series inductance from the capacitor terminals to the internal power nodes. Usually, it is necessary to separate the ground pins for the power ground and the signal ground. From control circuit design perspective, the controller must have high immunity to the supply noise to survive excessive noise in the supply.

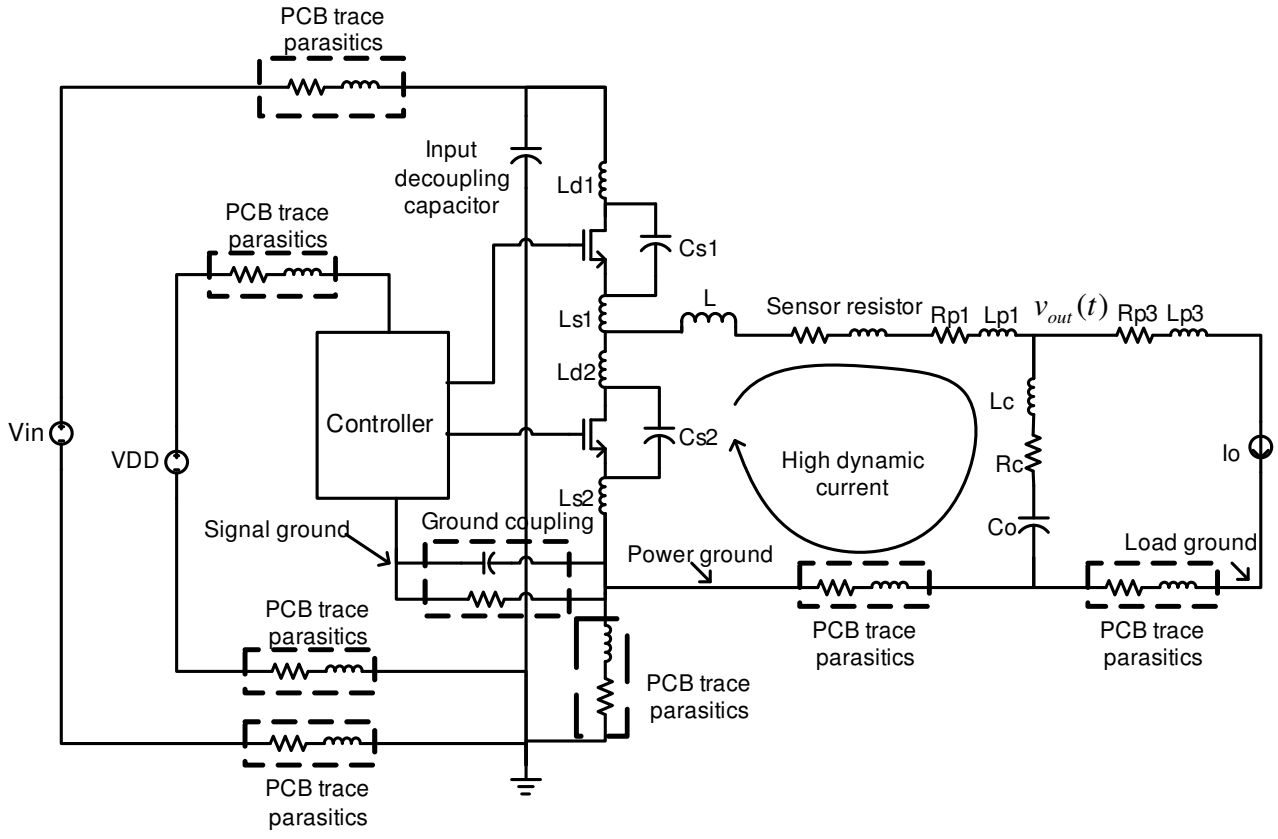


Figure 3.8 The circuit model showing parasitic elements in ground connection

The third important path for noise coupling is Electromagnetic (EM) coupling [Mugur'01]. Because of high current switching in the power stage, considerably high EM energy is radiated into the ambient. The metal objects, such as the metal trace on the PCB and the metal frame in the chip package, collect EM noise by the antenna effect. The collected high frequency noise then mixes with real signals inside the controller. Because it is difficult to model the EM field, this type of noise coupling cannot be well predicted in simulation. The common practice to reduce this type of noise coupling includes reducing the area of noise emitters and noise collectors and adding proper shielding to the sensitive parts in the circuits. For example, the switching nodes between two power switches are major noise emitters. It is better to reduce the area of these nodes on the board. To reduce the noise collection at voltage or current sensors, the trace of two input nodes should be closely located so that the loop area is reduced. By this way, the EM noise is limited to common-mode noise that is much easier to be filtered out than the differential-mode noise. Sometimes a ground plane is added in PCB to isolate the switching nodes from the input traces of sensing circuits.

In order to deal with large amount of noise, the controllers could be designed conservatively with low bandwidth. If the system bandwidth is designed much lower than the switching frequency, much of the noise could be attenuated by the loop. However, the low bandwidth design obviously sacrifices dynamic response of the system. The more effective way to deal with the noise issues is to develop circuit techniques that give better noise immunity without sacrificing the speed. In Chapter 4, fully differential architecture is adopted in the integrated controller. Some circuit techniques will be discussed to optimize the system performance on noise immunity.

3.4 Current sensing design

Sensing current is commonly required in the switching DC-DC converter design. In current-mode control, the current signal is a part of feedback signals. Especially, for the proposed control scheme, feedback control requires instantaneous current waveform to generate the duty cycle signal, and AVP design requires accurate value of average current in the inductor. Even though only voltage is needed to close the feedback loop in the voltage-mode control, the current signal is still needed for protection purposes. Sensing current is one of the critical tasks of the controller. This Section provides a brief review on the current sensing design.

A number of methods were developed to sense the current in the DC-DC converters. These methods can be roughly categorized as three types. As shown in Fig. 3.9, the first type of current sensing methods is using sensing resistors. A precision resistor is added in series with the inductor so that the voltage on the resistor can be measured as the current signal [Ridley'02]. This simple method provides current signal of good quality. However, adding resistance in the current path decreases power efficiency severely. In typical VRM application, adding 1 mΩ sensing resistance will lower the efficiency by 1% to 2%. To maximize the efficiency, minimal sensing resistor must be used. On the other hand, low sensing resistance causes poor Signal-to-Noise Ratio (SNR) in the sensed signals. For instance, the worst SNR of the sensor input signals could be as low as –30 dB to –40 dB when 1 mΩ sensing resistance is used, which poses great challenges to the current sensing amplifier design. Alternative way to sense the current with sensing resistor is to add the resistor in series with one of the switches, as shown in Fig. 3.10. By this means, the power consumption on the sensing resistor could be reduced. Since sensed current

waveform is not continuous, average current need to be extracted from the pulse signals by using techniques like sample-and-hold. An issue with sensing the switch current is that the current in the switch is a narrow pulse signal when on time of the switch is short. Especially, for the top switch S1, the oscillation from the parasitic components in the switches causes much of troubles in current sensing design.

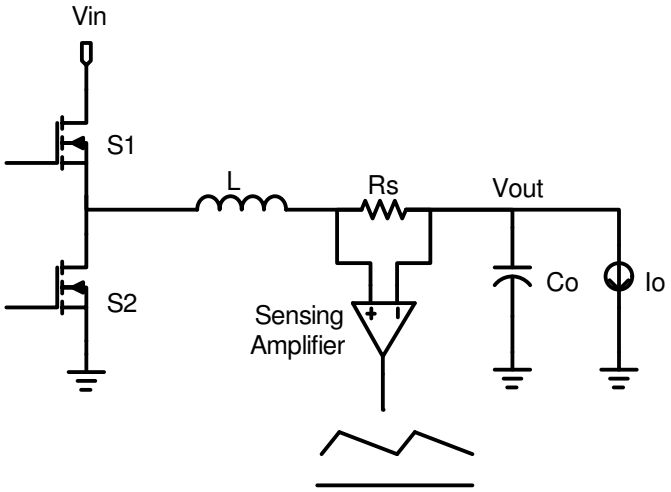


Figure 3.9 Current sensing method – sense inductor current with a resistor

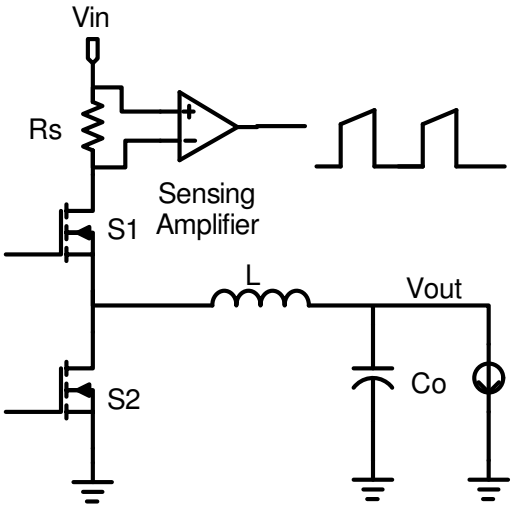


Figure 3.10 Current sensing method – sense switch current with a resistor

The second type of current sensing methods is using signals across the inductor [Lenk'99] [Dallago'00], as shown in Fig. 3.11 to 3.13. The basic idea of this approach is

that the current signal in the inductor can be restored from the voltage signal on the inductor. For example, in Fig. 3.11, the voltage on the capacitor C1 can be calculated as:

$$v_s = \frac{i_L R_p (1 + s\frac{L}{R_p})}{1 + R_1 C_1 s} \qquad (3.1)$$

From (3.1), the DC value of v_s is proportional to the inductor current with the gain equal to R_p that is the series parasitic resistance in the inductor. To get the exact waveform of v_s that is proportional to the inductor current, the condition in (3.1) is:

$$\frac{L}{R_p} = R_1 C_1 \qquad (3.2)$$

Therefore, the inductor current waveform can be restored as the voltage on C1 when the time constants of the L-R and R-C networks match each other.

This current sensing method, or so-call DCR sensing, has shown practical advantages on reducing the power consumption and providing current signal of high quality. In practice, when only average current is needed in the design, large time constant in R-C network can be adopted to reduce the noise in the sensed signal.

Fig. 3.12 is an alternative way to implement DCR sensing where a transconductor amplifier is used to sense the voltage signal across the inductor. In this design, the gain is scaled by the transconductance and the resistor R1 [Zhang-1'05]. It has been shown that the noise sensitivity in the design is better than the design in Fig. 3.11. However, the performance of the transconductor has significant impact on accuracy of the current sensing. The transconductor is required to handle wide range of the input signal. The frequency response of the transconductor needs to be high enough to deal with the high frequency ringing in the input signal.

The limitation of DCR sensing arises from the tolerance of Rp and L. The typical value of Rp is around 1mΩ to 2mΩ. The tolerance of Rp and L can be as high as 20% in the commercial inductors. To improve the accuracy in the current sensing, tuning circuits can be used in the sensing amplifiers. In [Forghani-zadeh'05], the current sensing gain is adaptively adjusted in the initial period when the converter is started up.

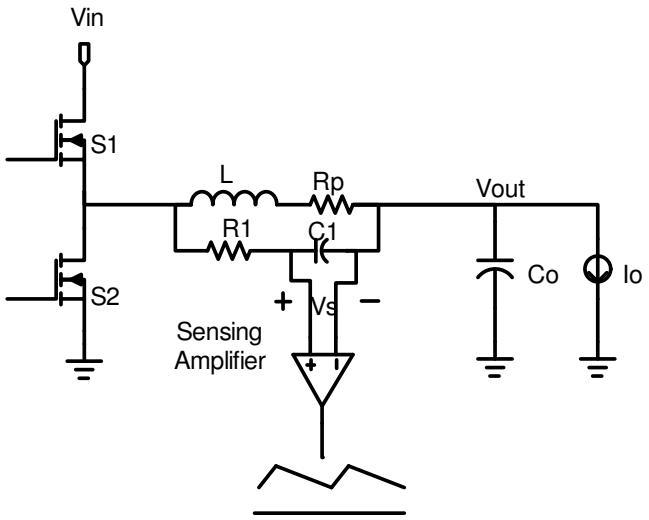


Figure 3.11 Current sensing method –inductor DCR sensing

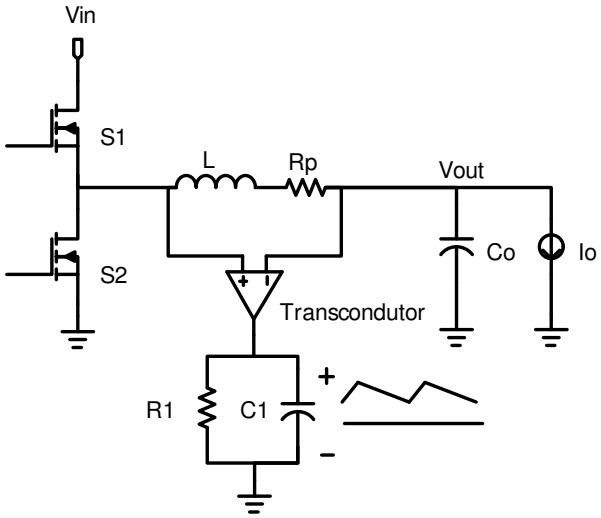


Figure 3.12 Current sensing method - improved DCR sensing

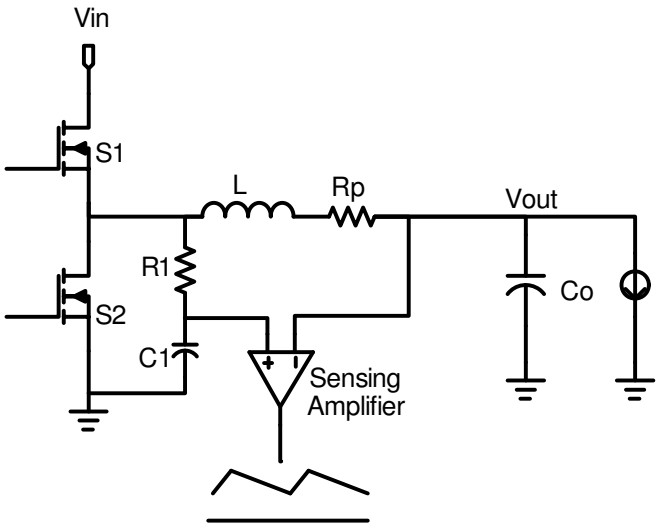


Figure 3.13 Current sensing method – alternative implementation of DCR sensing

The third type of the current sensing methods is using the voltage drop on the switches, as shown in Fig. 3.14 and 3.15. As the drain to source voltage on the switch is proportional to the switch current if the on resistance of the switch is constant, this current method is called Vdson sensing.

As shown in Fig. 3.14, the voltage on the bottom switch is selected by two switches, S3 and S4, at input of the amplifier. By adding S3 and S4, the high voltage on the S2 can be blocked from the input of the amplifier. In Fig. 3.15, S4 is replaced by a resistor, R1 [Yuvarajan'91]. If R1 is much larger than the on resistance of S3, the voltage on R1 is approximately equal to the voltage on S2.

The Vdson sensing methods have advantage of low power consumption. But the sensed signal is contaminated by the switching noise at drain voltage of S2, similarly as in Fig. 3.10. Another issue with this method is that the on resistance of the power switches is varying with temperature and manufacturers. Temperature compensation is necessary to have enough accuracy in the design.

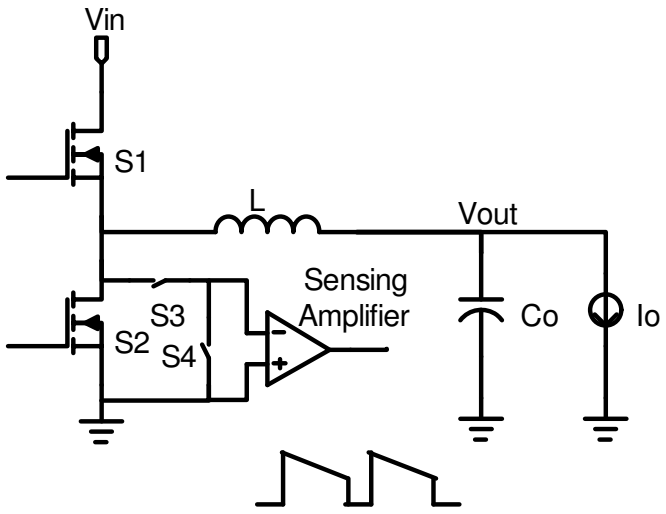


Figure 3.14 Current sensing method – sense switch current by Rdson

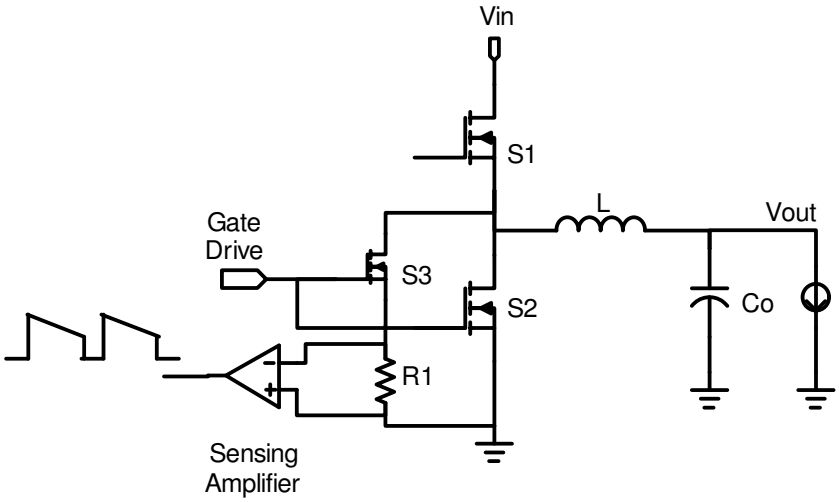


Figure 3.15 Current sensing method – sense switch current with sensor FET

3.5 Overview of the implemented controller

Fig.3.16 shows the circuit block diagram of the controller. According to their functions, the whole chip can be partitioned into four functional units: control core unit, multi-channel control unit, sleep mode control unit and reference generation unit.

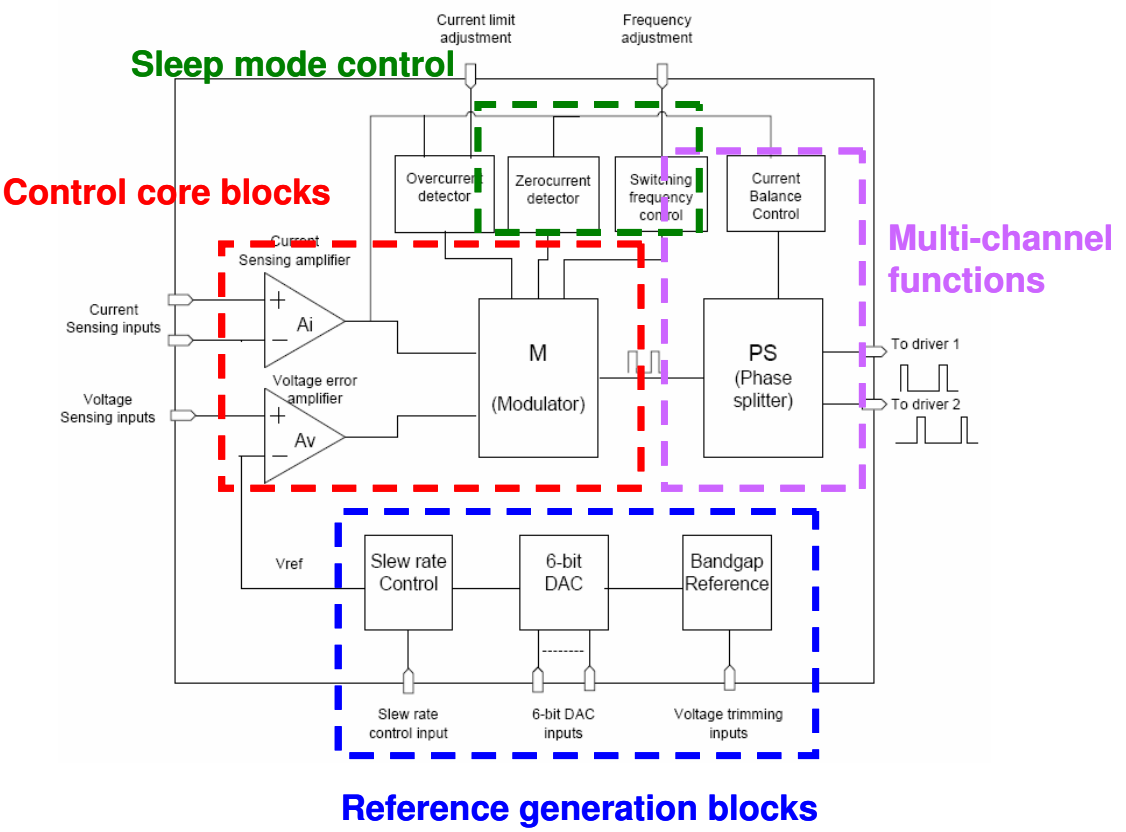


Figure 3.16 Circuit block diagram of implemented controller

The control core unit, including the current sensing amplifier, the voltage error amplifier and the modulator, is the key functional unit that generates the duty cycle signal from the signals sensed in the power stage and form the closed-loop feedback. The circuit characteristics of the control core unit, such as noise rejection and frequency response, have significant impacts on system static and dynamic performance. The details of the control core unit design are discussed in Chapter 4.

The multi-channel control unit is the circuit unit that generates the driver signals for all individual channels. The input signal of the multi-channel control unit is the duty cycle signal from the control core unit. By manipulating the timing and the pulse width of the duty cycle signal for each channel, the different channels have proper interleaving and current balancing. The design of these functions is discussed in Chapter 5.

In portable applications, the system runs in standby mode or low power mode for considerable amount of time. The system power efficiency in these modes is one of the most important concerns in portable system design. Therefore, a dedicated control unit is designed for the sleep mode.

Besides the control functional units, there are some additional functions required by the applications, such as dynamic reference. According to Intel's IMVP specifications, the output voltage of VRM should be controlled by digital signals from the CPU in certain fashion. For example, the output voltage in the active mode and the sleep mode are shifted with a constant voltage; the slew rate of the voltage transition should be tightly limited in certain range. These requirements are fulfilled by the reference generation unit that includes a bandgap reference, 6-bit DAC and slew rate control circuits.

3.6 Summary of Chapter 3

In Chapter 3, the integrated controller for DC-DC converter is introduced. The key functions of the controller are identified. The methodology to design a high performance controller is discussed. Having the advantages and the disadvantages of both the voltage mode and the current mode circuit design, the optimal approach is to take advantage of both of them and avoid their drawbacks. This principle is practiced in the circuit design presented in Chapter 4. The noise and the current sensing are two major challenges in the

controller design. The design considerations on three types of noise coupling, including signal sensing noise, power supply noise and electromagnetic noise, are discussed. In the proposed controller, the full differential circuits are used to overcome the noise problems. The techniques to sense the current are reviewed. The inductor DCR sensing is shown to be the promising way in the practical design. The design considerations of DCR current sensing methods are discussed. Finally, the block diagram of the implemented controller is presented. The major functions of the controller are described.

Chapter 4 Fully Differential Control Core Circuits

4.1 Introduction

The control core circuits are illustrated in Fig. 4.1 that has three major blocks: the voltage error amplifier, the current sensing amplifier and the modulator. The current sensing design is illustrated with the current sensing resistor; however, in the real implementation, it can be implemented with any methods of DCR current sensing. In this case, R_s is the effective current sensing gain.

Both the current sensing amplifier and the voltage error amplifier have finite DC gains. As discussed in Chapter 2, the gain ratio is a critical parameter to control the accuracy of the AVP droop resistance. As mentioned before, the two amplifiers should have good gain matching so that the variation of gain can be well cancelled.

The proposed implementation of control core circuits is based on fully differential architecture. Because both the voltage error amplifier and the current sensing amplifier are at front-end of the controller that receives signals from the noisy power stage, noise must be well attenuated before it is passed to other circuits inside the controller. Fully differential circuits have been proven to have superior performance over their signal-ended counterparts. For example, fully differential circuits provide a larger output voltage swing and less susceptible to common-mode noise. The even-order nonlinearities are not present in the differential output of a balanced circuit. However, fully differential circuits have not been reported in power management circuits design. In this Chapter, the design of control core circuits is systematically gone through. Some of design considerations are discussed. Simulation and test results are presented to verify the circuit performance.

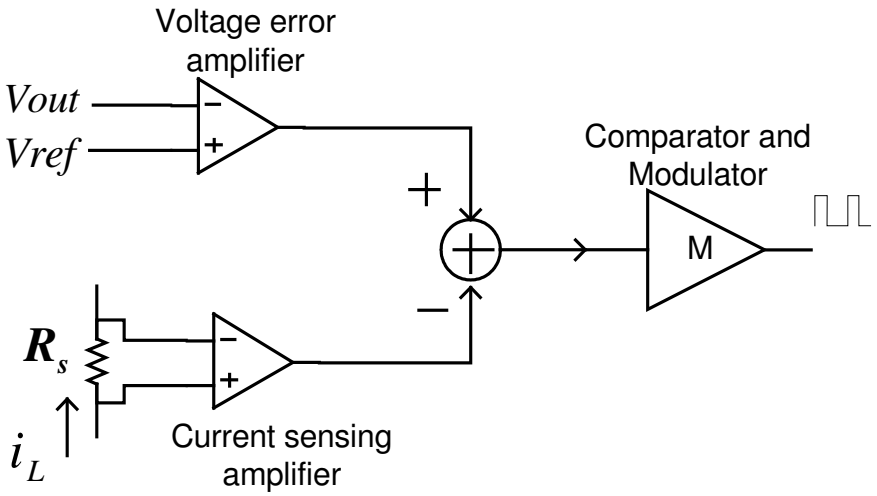


Figure 4.1 Control core circuits in the controller

4.2 Current sensing amplifier

As discussed in Section 3.4, current sensing is one of most challenging circuits in the controller. No matter what method is used to sense the current, the current signal always has small amplitude and poor noise contamination. As a result, the most important requirement of the sensing amplifier is good noise rejection. Besides, input signal range and gain linearity are also important in the design. The target of input signal range is from 1 mV to 100 mV, which covers the sensing resistance from 1 mΩ to 5 mΩ. Although the accuracy of absolute gain value is less important for controlling the AVP droop resistance, the gain matching between two current sensing amplifiers for two channels, and gain matching between current sensing amplifier to the voltage error amplifier are required. With above considerations, the current sensing amplifier is configured with three fully differential stages, shown in Fig. 4.2.

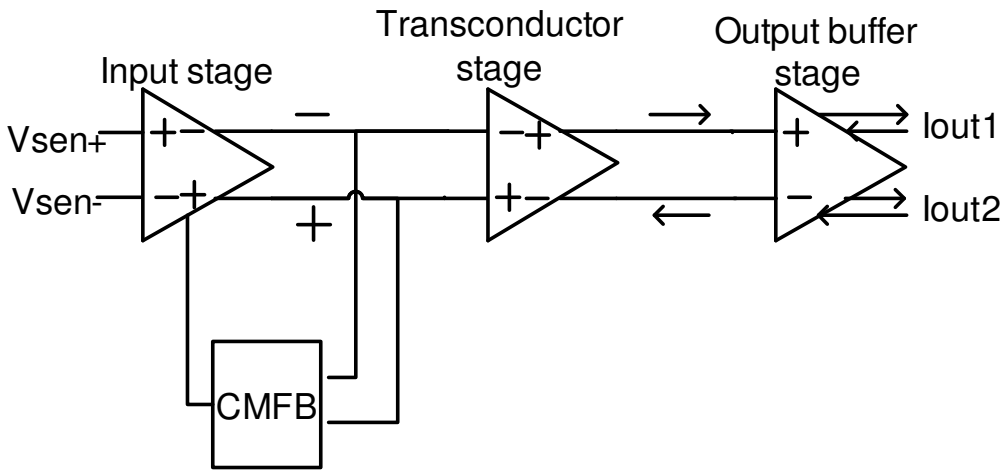


Figure 4.2 Circuit structure of current sensing amplifier

The input stage shown in Fig. 4.3 is a voltage mode amplifier with resistive feedback. The primary design goals of the input stage are noise rejection and signal conditioning. Benefited from low gain design (nearly 18 dB) and voltage feedback, the input stage has wide common-mode input range and high linearity. With common-mode feedback (CMFB), the common-mode voltage is maintained at a constant level, which eases the design of the following stages. The DC gain in the input stage helps boost the total gain of the amplifier, which saves power consumption in the second stage.

Frequency response of the input stage is designed with two considerations. On one hand, the input stage serves as a bandwidth limiter that prevents high frequency noise from passing through into the second stage. By taking advantage of voltage mode design, small amount of compensation capacitance (1 pF) at output nodes controls the bandwidth of the input stage. On the other hand, the bandwidth of the input stage should be high enough to avoid excessive phase delay. Fig. 4.4 shows the sketched waveforms of input and output signals. Although exact shape of the current waveform is not required by control, excessive phase delay of the current signal will cause instability at steady state, especially

when the delay is comparable to the on time. To guarantee the system robustness, the phase delay at the maximum switching frequency (800 KHz) is designed less than 25 degree. The 3-dB bandwidth of the input stage is about 3 MHz. The simulated frequency response of the input stage is shown in Fig. 4.5.

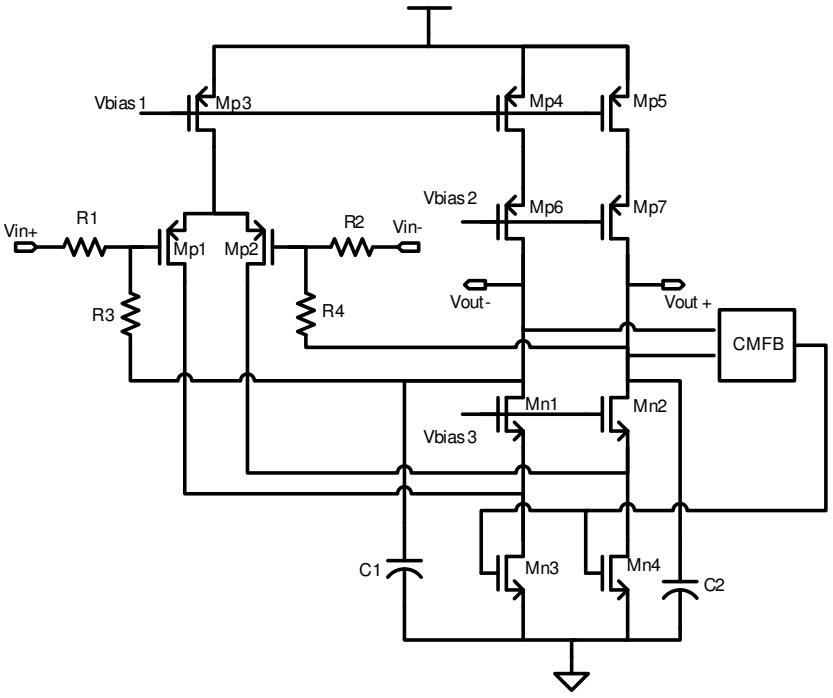


Figure 4.3 Input stage of current sensing amplifier

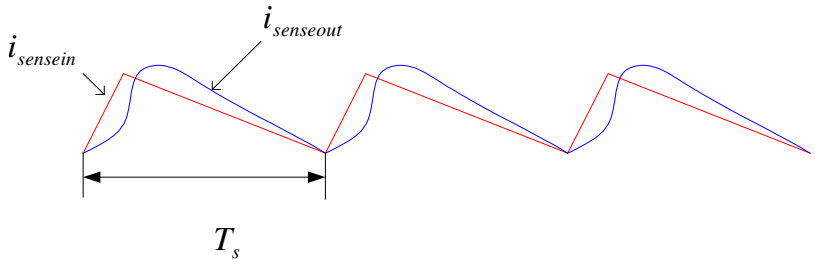


Figure 4.4 Input and output waveforms of the current sensor

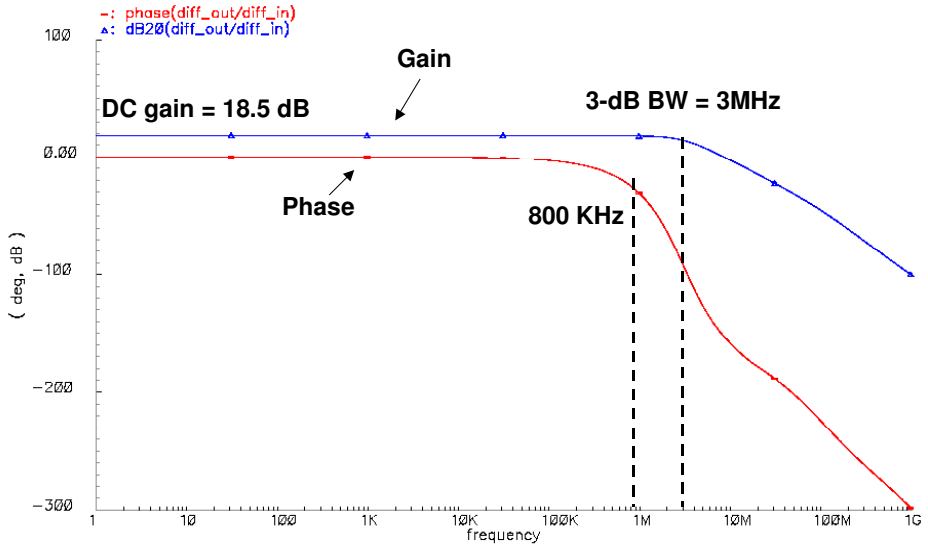


Figure 4.5 Frequency response of input stage in current sensing amplifer

The second stage of the current sensing amplifier shown in Fig. 4.6 is a linear transconductor that converts the differential voltages into the differential currents.

$$I_{out+} - I_{out-} = G_{m1}(V_{in+} - V_{in-}) \qquad (4.1)$$

Since differential input range of the transconductor is as large as ± 1 V, large signal linearity is required in design. In Fig. 4.6, two feedback loops are formed by Mn1~4 and Mn5~8. The high loop gain forces the differential voltage on the resistor to follow the input differential voltage [Johns'97]. Therefore, linear transconductance is obtained:

$$G_{m1} \approx \frac{1}{R} \qquad (4.2)$$

The gain linearity over the input voltage is plotted in Fig. 4.7. From simulation, the gain variation is less than 5%.

To maintain the stability of the two loops, dominant pole compensation is added to nodes A and B. The simulated frequency response is shown in Fig.4.8. The gain bandwidth is about 10 MHz.

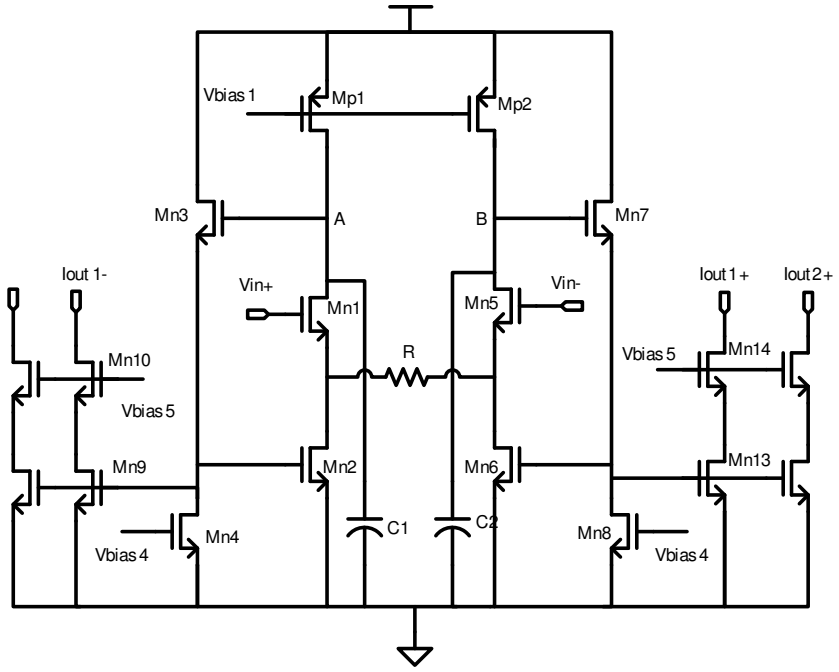


Figure 4.6 Transconductor stage of current sensing amplifier

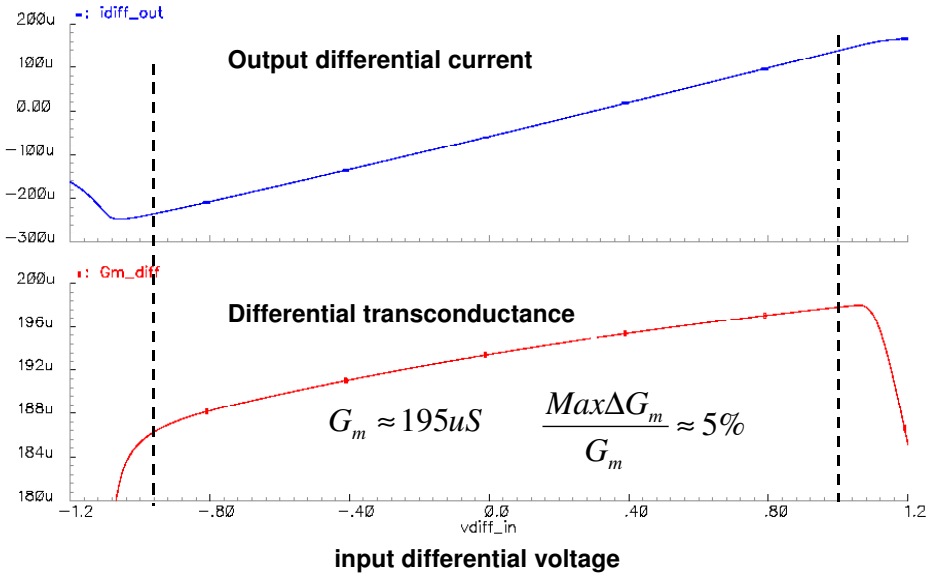


Figure 4.7 Gain linearity of the transconductor stage

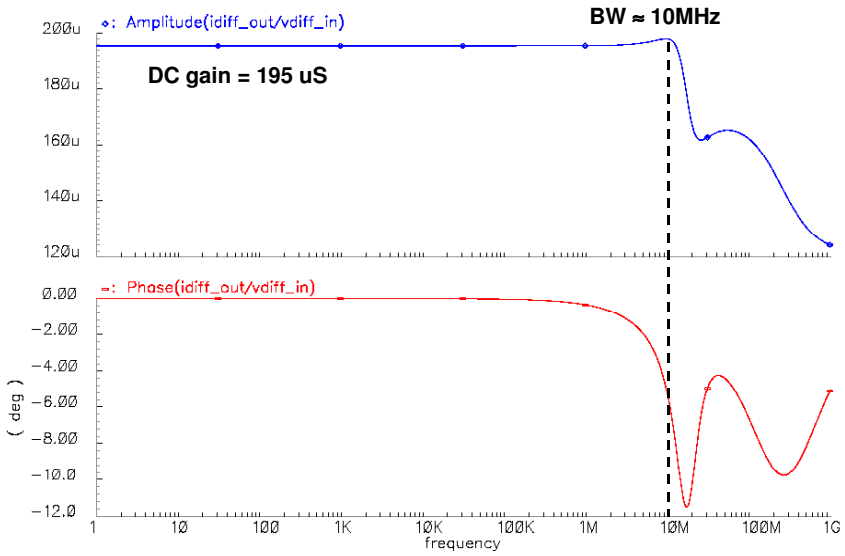


Figure 4.8 Frequency response of transconductor stage

The output stage of the current sensing amplifier is the current buffers formed by Mn9~12 and Mn13~16 in Fig. 4.6. The output impedance is boosted by the common gate configuration. Multiple outputs are simply obtained with current mirrors. Additional gain can be produced by increasing the ratios of the current mirrors.

Since the whole circuit is completely symmetric, the ideal gain from the common mode input to the differential output and the ideal gain from the power supply noise to the differential output are both zero. Variation of the common mode output is reduced by the common mode feedback circuits. After all, the output common mode signals have little effect on the system control because the circuits following the amplifier are also fully differential circuits. Practically mismatches in the layout and device properties cause differential noise at the output, but the mismatches can be minimized by drawing the layout with good symmetry. The simulation and test results shows that the designed circuits have high immunity to the common mode input noise and the power supply noise.

The overall transconductance of the current sensing amplifier is about 1.6 mS with bandwidth about 3 MHz. The simulation waveforms with current sensing inputs are shown in Fig. 4.9.

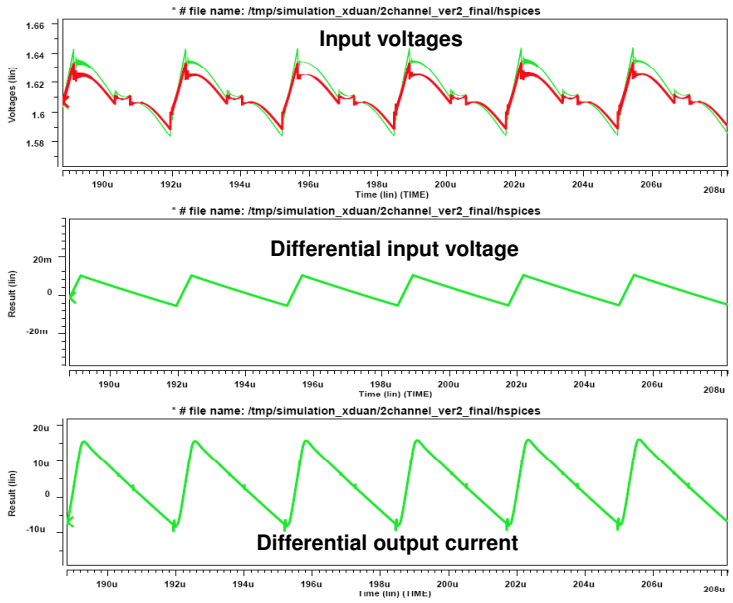


Figure 4.9 Simulation waveforms of current sensing amplifier

4.3 Voltage error amplifier

The structure of the voltage error amplifier is shown in Fig. 4.10. For good gain matching, most of circuits in the voltage error amplifier are implemented with the same circuits in the current sensing amplifier except that the voltage error amplifier has four input signals instead of two input signals, and the additional variable gain cell.

As discussed in Section 3.3, parasitic resistance and inductance in the interconnection cause significant voltage variations on the ground. To sense the exact voltage on the CPU, differential voltage is sensed between the CPU supply voltage and the CPU ground. Inside the controller, the reference voltage can be generated differentially to further improve noise rejection to power supply noise. With two sets of differential inputs, the

voltage error amplifier is actually a Differential Difference Amplifier (DDA) with a linear gain G_m:

$$i_{o+} - i_{o-} = G_m[(V_{ref+} - V_{ref-}) - (V_{out+} - V_{out-})] \qquad (4.3)$$

The schematic of the input stage is shown in Fig. 4.11.

If let $R_1 = R_4$, $R_2 = R_5$ and $R_3 = R_6$, the linear gain is obtained:

$$v_{o+} - v_{o-} = \frac{R_3}{R_1}(V_{ref+} - V_{ref-}) - \frac{R_3}{R_2}(V_{out+} - V_{out-}) = \frac{R_3}{R_1}[(V_{ref+} - V_{ref-}) - \frac{R_1}{R_2}(V_{out+} - V_{out-})] \quad (4.4)$$

The ratio of the output voltage and the reference voltage can be adjusted by changing $\frac{R_1}{R_2}$. In this design, $\frac{R_1}{R_2} = 1$ is chosen to keep the output voltage equal to the reference voltage.

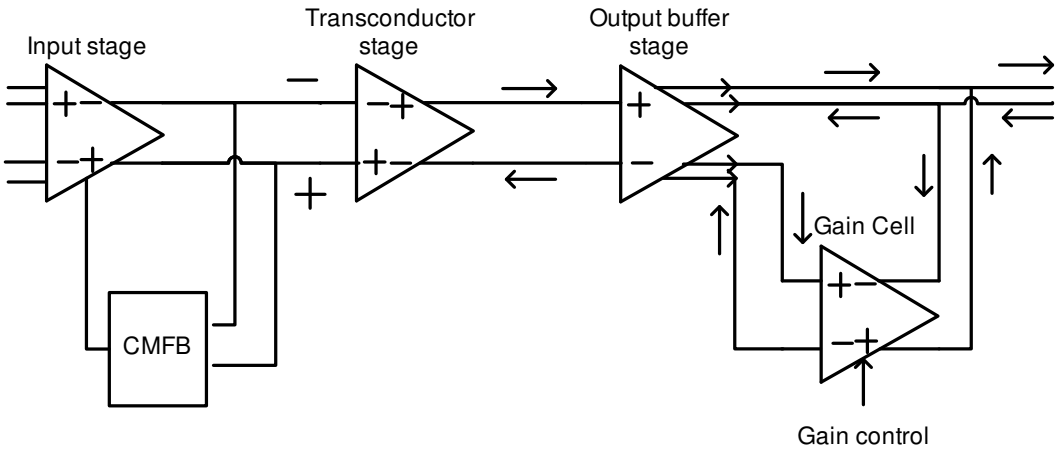


Figure 4.10 Circuit structure of voltage error amplifier

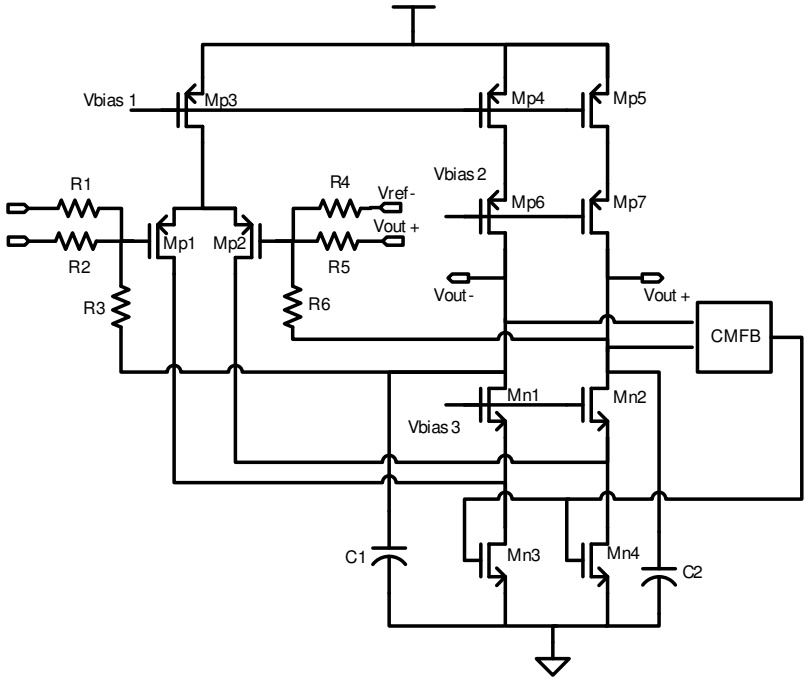


Figure 4.11 Input stage of voltage error amplifier

The gain cell in Fig. 4.10 is added to tune the gain of the voltage error amplifier. The schematic of the gain cell is shown in Fig. 4.12, where the output of the gain cell is summed with the input currents to increase total transconductance. The output of the gain cell is calculated as:

$$i_{o+} - i_{o-} = (i_{in+} - i_{in-})(1 + \frac{I_1}{I_2}) \qquad (4.5)$$

Here, I_1 is the bias current in Q_1 and Q_2, and I_2 is the bias current in Q_3 and Q_4. The gain is adjusted by adjust the current in Mn1.

For tuning the droop resistance, the transconductance of the voltage error amplifier is designed variable from 1.1 mS to 2.0 mS. As shown in Fig. 4.13, the transconductance has linear relation with the bias current. The frequency response of the voltage error amplifier is similar to that of current sensing amplifier, as shown in Fig. 4.14.

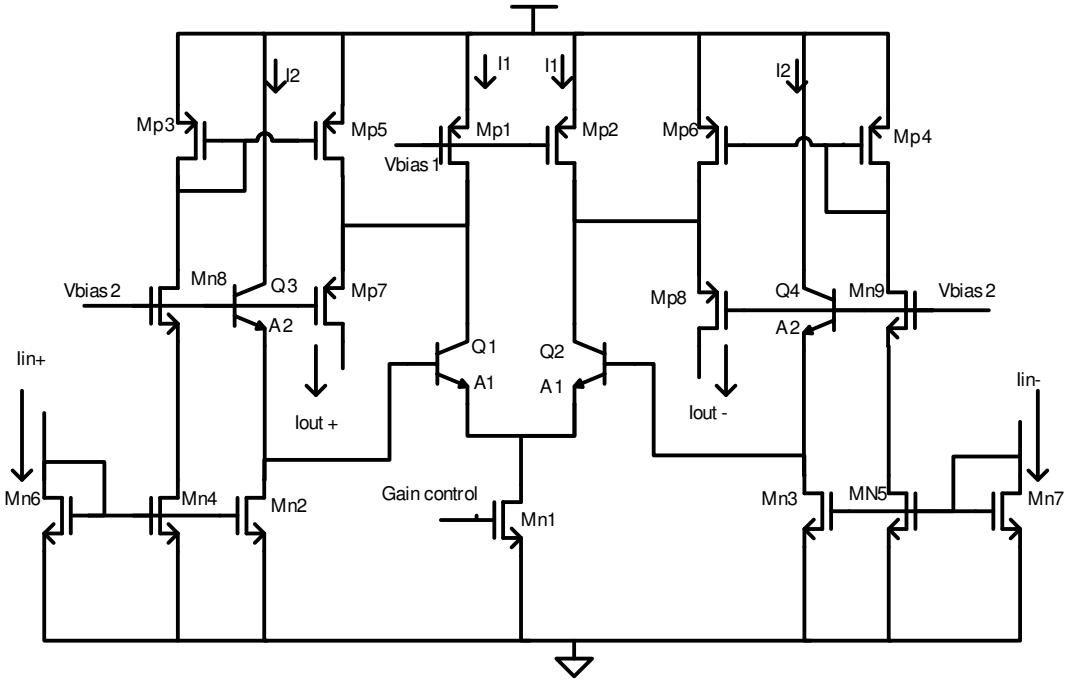


Figure 4.12 Gain cell in voltage error amplifier

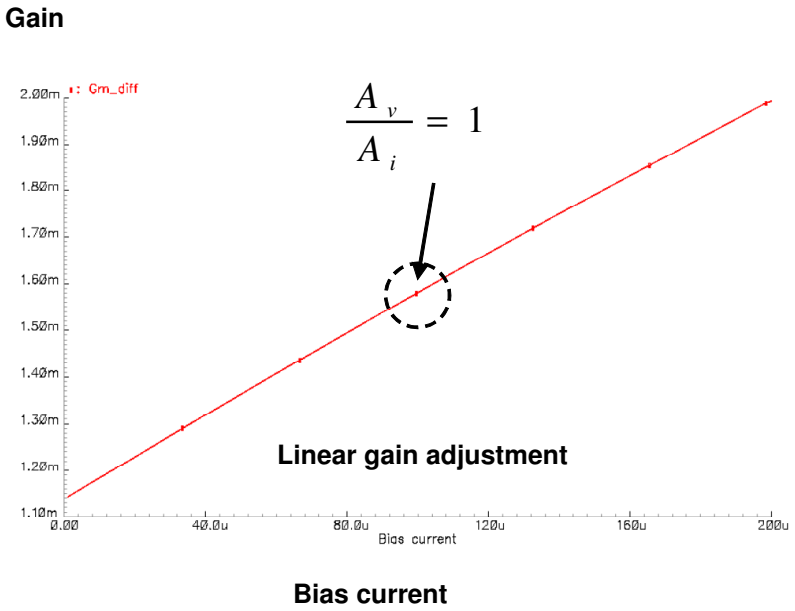


Figure 4.13 Transconductance vs. bias current in voltage error amplifier

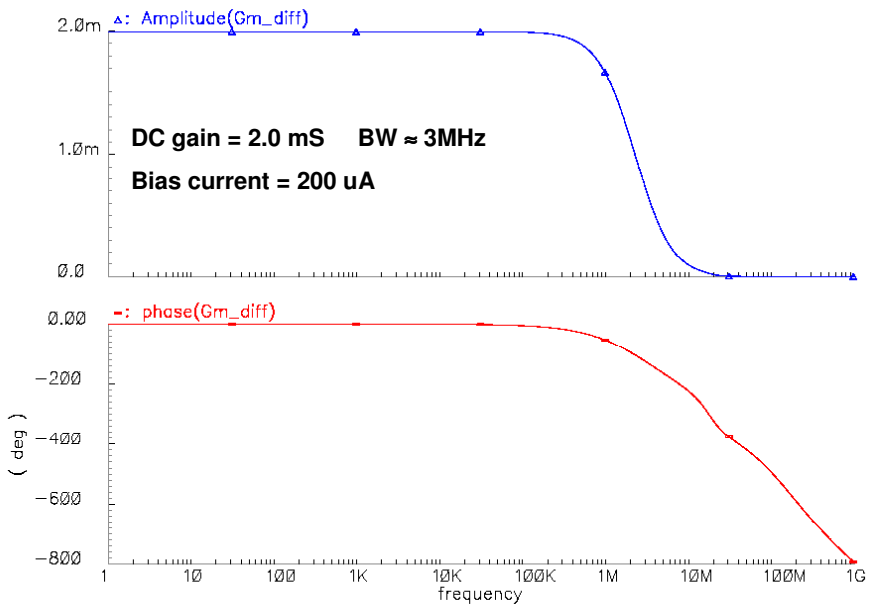


Figure 4.14 Frequency response of voltage error amplifier

4.4 Constant on time modulator

The modulator is the circuit that converts the continuous control signal to the duty cycle signal. Depending on the control scheme, the implementation of the modulator is different. In the traditional PWM modulator, the duty cycle signal $d(t)$ is modulated by comparing the control signal $v_e(t)$ with the ramp signal [Erickson'01], as shown in Fig.4.15. For the variable frequency control, constant ramp signal is not available for modulation. The modulator for the proposed control scheme is designed as in Fig. 4.16, where the rising edge of $d(t)$ is triggered by the output of the comparator, and the on time of $d(t)$ is controlled by a delay block.

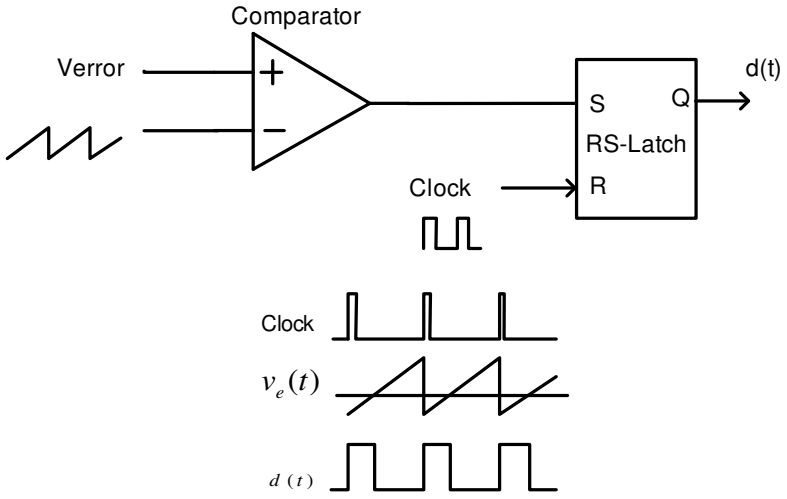


Figure 4.15 Conventional implementation of PWM modulator

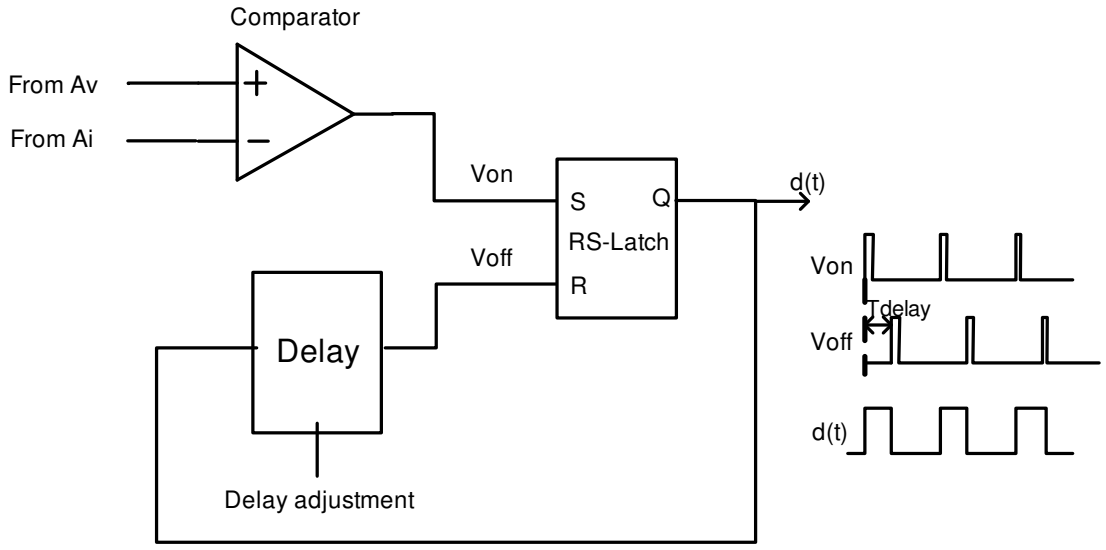


Figure 4.16 Modulator designed for proposed control scheme

As discussed in Section 2.4, the static error in the main feedback loop is corrected by the error correction loop. In circuit design, the error correction loop is realized by making two inputs of the comparator in Fig. 4.16 have equal average levels. Let $i_{Ai+} - i_{Ai-}$ be the differential signals from the current sensing amplifier, and let $i_{Av+} - i_{Av-}$ be the differential signal from the voltage error amplifier. The comparator compares the two differential signals, and the average values of the two differential signals are assumed equal:

$$\left\langle i_{Av+} - i_{Av-} \right\rangle = \left\langle i_{Ai+} - i_{Ai-} \right\rangle \qquad (4.6)$$

The equation can rearranged as:

$$\left\langle i_{Av+} + i_{Ai-} \right\rangle = \left\langle i_{Av-} + i_{Ai+} \right\rangle \qquad (4.7)$$

Let $i_{in+} = i_{Av+} + i_{Ai-}$, $i_{in-} = i_{Av-} + i_{Ai+}$

It is equivalent to compare i_{in+} and i_{in-}, and make $\left\langle i_{in+} \right\rangle = \left\langle i_{in-} \right\rangle$.

The schematic of the comparator is shown in Fig. 4.17. Low impedance input stage is formed by Mn3~6. The cross-coupled active load Mp1~2 and the diode connection active load Mp3~4 help to reduce comparison delay to less than 10 ns. The integrator amplifies the difference between i_{in+} and i_{in-}, and the error signal is injected back by an offset current i_{offset}.

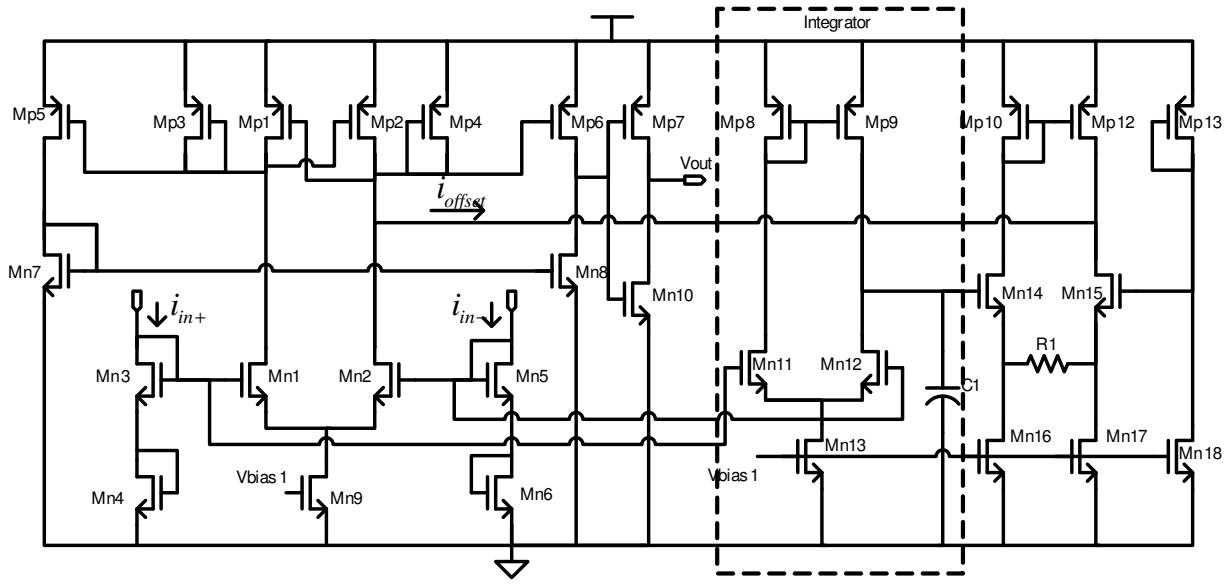


Figure 4.17 Current comparator with injected offset for error correction

The feedback gain of the error correction loop can be adjusted by the external capacitor C_1 and the internal resistor R_1. With $C_1 = 50pF$ and $R_1 = 50K\Omega$, the simulation

waveforms are shown in Fig. 4.18. With the error correction loop, the DC error of the output voltage is reduced to less than 1 mV in simulation.

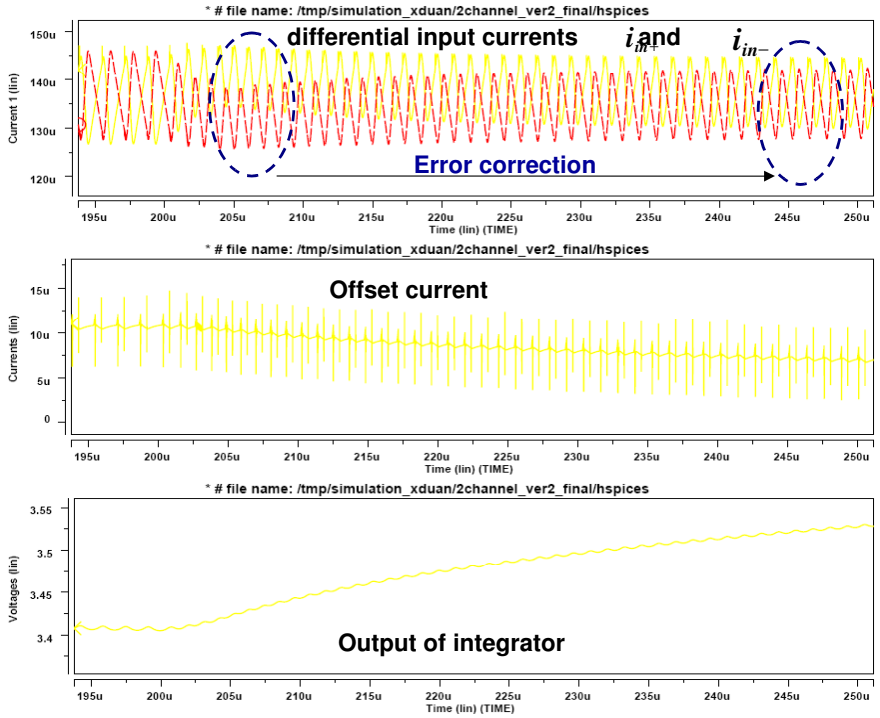


Figure 4.18 Simulation waveforms showing error correction by injecting offset current

The delay block in Fig. 4.16 generates the on time, as discussed in Section 2.3.2, delay time should be proportional to $\frac{V_{ref}}{V_{in}}$ to maintain the steady state switching frequency constant in CCM. The circuit of the delay block is shown in Fig. 4.19, where G_{m1} and G_{m2} are two transconductors. The delay time is:

$$t_{delay} = \frac{G_{m1}}{G_{m2}} RC \cdot \frac{V_{ref}}{V_{in}} \qquad (4.8)$$

G_{m1} is designed adjustable with an external resistor R_1 ,as shown in Fig.4.20.

$$G_{m1} \approx \frac{1}{R_1} \qquad (3.9)$$

Therefore, the steady state switching frequency in CCM has no dependency on the input voltage and the output voltage, and it can be linearly adjusted by R_1.

$$f_s \approx R_1 \frac{G_{m2}}{RC} \propto R_1 \qquad (3.10)$$

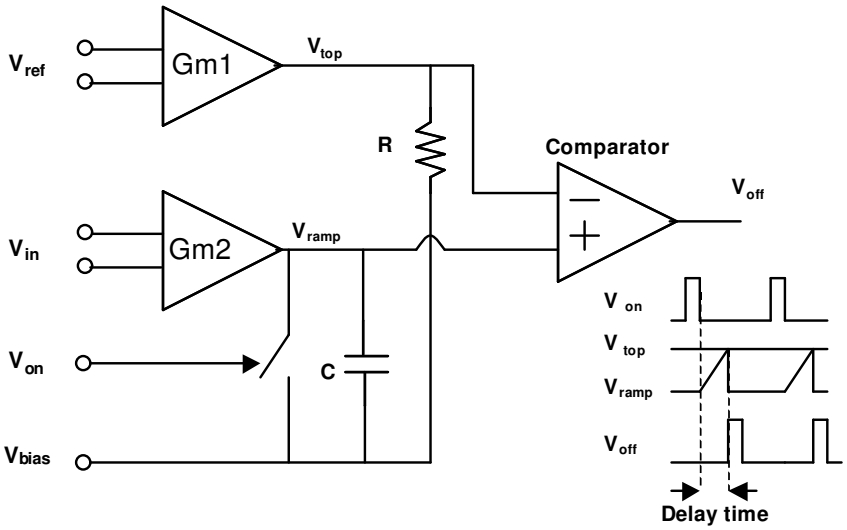


Figure 4.19 Voltage-controlled delay block

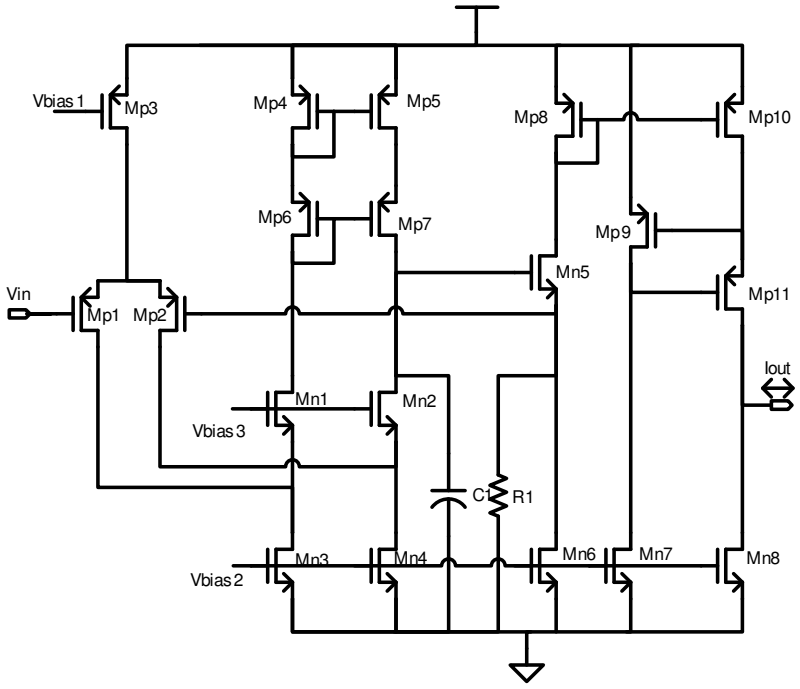


Figure 4.20 A transconductor with linear gain determined by R1

4.5 Summary of Chapter 4

In Chapter 4, the circuits to implement the core function of the controller are presented, including the current sensing amplifier, the voltage error amplifier and the constant on time modulator. These circuits form a closed feedback loop to regulate the output voltage. The performance of these circuits directly determines the system speed, accuracy and stability. The two amplifiers are designed with fully differential structure. The current sensing amplifier has three stages. The design considerations and circuit performance are presented. The voltage error amplifier has similar structure as the current sensing amplifier to have good gain matching. In addition, the voltage error amplifier has the gain control function to adjust the AVP droop resistance. Fully differential or remote voltage sensing is incorporated in the voltage error amplifier without adding complexity. The constant on time modulator consists of a current comparator and a voltage controlled delay block. The current comparator provides automatic error correction by using the offset control. The voltage controlled delay block adjusts the on time according to the input voltage and the reference voltage so that the steady state switching frequency will not vary with the input voltage or the reference voltage.

Chapter 5 Design of Interleaving and Current Sharing

5.1 Multi-channel DC-DC converters

Multi-channel DC-DC converters have been proved to be a practical way to supply high current with today's design capability. As an example, a two-channel Buck converter is shown in Fig. 5.1, where each channel consists of a pair of power switches, an inductor and some input capacitors. The output capacitor is usually located close to the load in order to minimize the parasitic elements between the power supply and the load. Because current capabilities of the power devices are limited by thermal and reliability issues, the maximum current for each channel is typically 20A to 30A. By paralleling more channels, high current can be achieved up to hundreds of Amperes [Bindra'02].

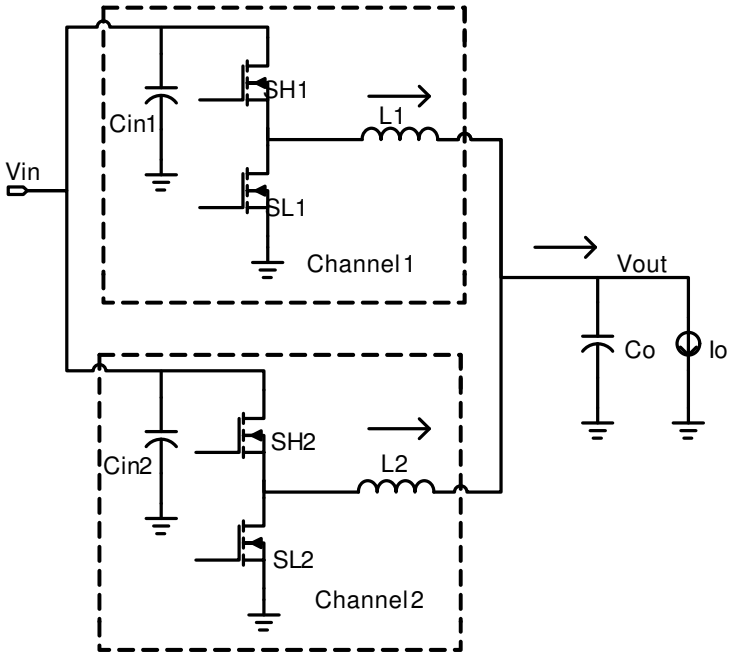


Figure 5.1 Simplified diagram of a two-channel DC-DC converter

If the output capacitor Co is divided and moved into each channel as shown in Fig. 5.2, the whole converter can be considered as two separated voltage sources connected in

parallel, as shown in Fig. 5.3. R_{s1} and R_{s2} represent the source resistance of the two voltage sources. The overall impedance seen from the load is the parallel resistance of R_{s1} and R_{s2}. Therefore, the whole converter has lower output impedance and better voltage regulation is achieved when delivering high current. In this sense, multi-channel architecture is a useful way to obtain ultra-low output impedance without increasing design difficulties in each channel.

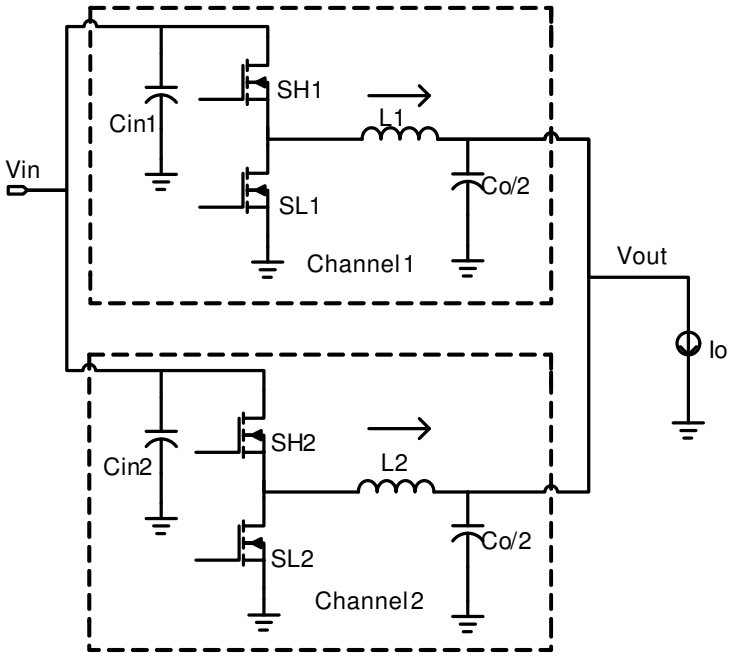


Figure 5.2 Two DC-DC converters in parallel with divided output capacitors

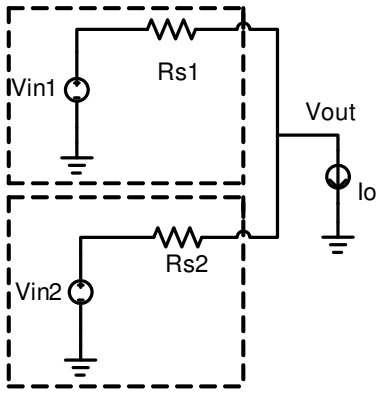


Figure 5.3 Simplified model of two-channel DC-DC converter

One of difference between the DC-DC converter and the ideal voltage sources in Fig. 5.3 is that the currents in the DC-DC converter are not constant. In certain applications, the inductor current may have ripples as high as 50% of the average current. These large current ripples could cause intolerable voltage fluctuations at the input and the output of the DC-DC converter unless huge capacitors are used at the input and the output of the converter. One important technique to minimize the effects of these current ripples is referred as the multi-channel interleaving design that is widely adopted in most industrial products [Chin'95].

Another issue with multi-channel architecture is about the current distribution among channels. From Fig. 5.3, the current in each channel is determined by the effective output resistance of the channel, e.g. R_{s1} and R_{s2}. For ideal performance, the currents should be evenly distributed among all channels. Otherwise, excessive current flowing in any channel could introduce thermal and electrical stress on the devices. Reliability issues occur when the current exceeds the thermal limitation or the devices are exposed to the stress for an extended period. To guarantee current sharing under all operation conditions, current sharing control should be implemented in the controller. The simulation waveforms in Fig. 5.4 show the effectiveness of the current sharing control.

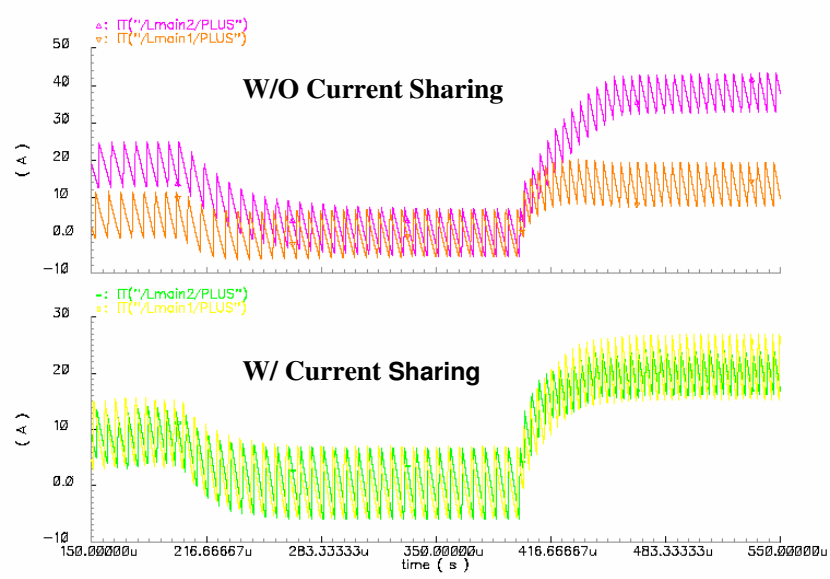


Figure 5.4 Simulation waveforms with and without current sharing

5.2 Multi-channel interleaving

5.2.1 Review of interleaving design

Interleaving is one of the important advantages of the multi-channel configuration compared with the high current single-channel configuration in which high current capability is achieved by using multiple devices in parallel. With interleaving design, the switching phases of different channels are shifted from each other, as illustrated in Fig. 5.5. Since all inductors are shorted at the output, the output current of the converter is the sum of each individual inductor currents. The ripple of the output current is reduced by the cancellation effect of interleaved currents, as shown in Fig. 5.6. The ripple frequency of the output current is effectively increased without increasing the actual switching frequency in each channel. This ripple cancellation effect is related to the duty cycle and the number of the channels. Fig. 5.7 shows calculated ripple reduction under different duty cycles and channel numbers assuming that the phases of all channels are evenly distributed [Wong'01]. For applications like the VRM, the duty cycle is usually small,

around 0.1. Therefore, better cancellation can be achieved by increasing the channel number. However, the optimal number of channels is determined by design specifications, design cost, design difficulties, etc. For the typical VRM applications in desktop and notebook computers, the channel number is from 2 to 4.

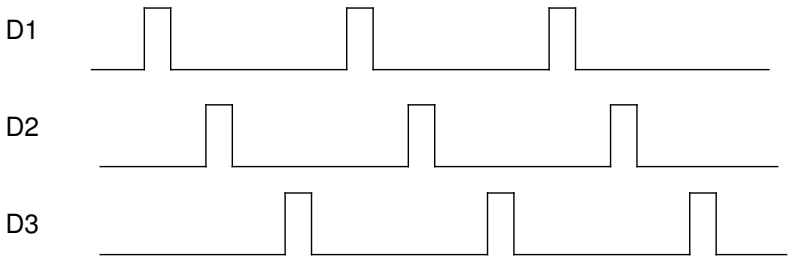


Figure 5.5 Clock signals with phase shifts

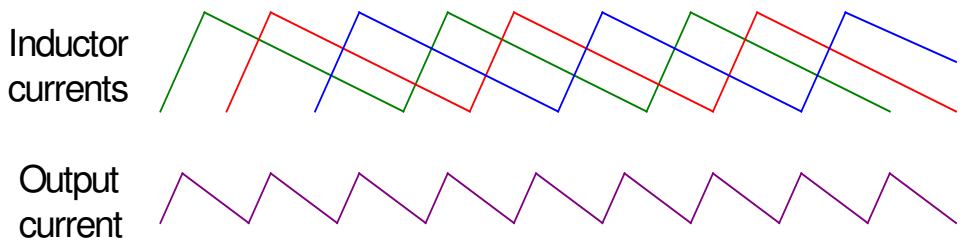


Figure 5.6 Ripple reduction from interleaving

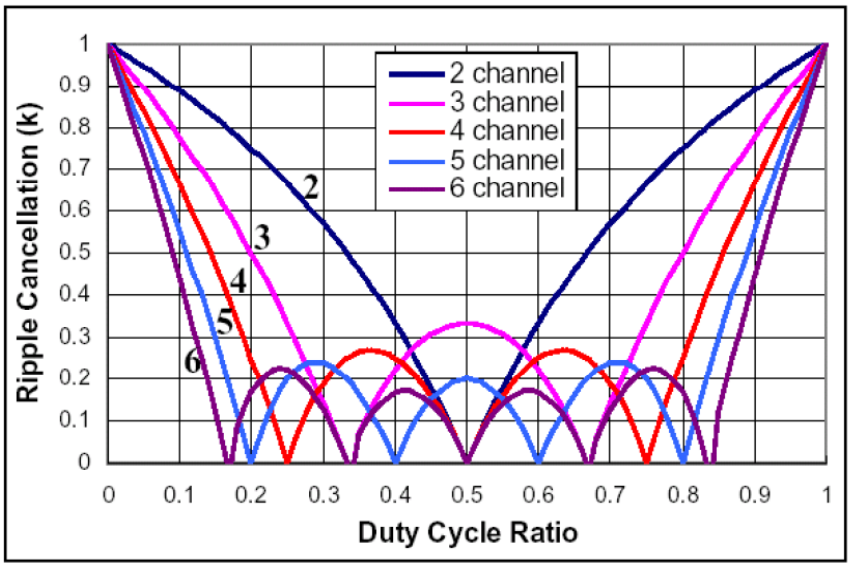


Figure 5.7 Calculated ripple cancellation v.s. duty cycle

To implement the interleaving design, duty cycle signals for individual channels need be synchronized with certain phase shift. For the control scheme that has clock signal available for synchronization, the interleaving design could be straightforward. A simple method is to use shifted ramp signals to generate the shifted duty cycle signals as shown in Fig. 5.8. Since the control signal is shared by all channels, only one feedback control is needed for the whole converter. Fig. 5.9 shows a circuit to generate interleaved ramp signals from a clock signal [Zhang-1'05]. The phase splitter can be implemented by the circuit in Fig. 5.10. Even phase shifting is guaranteed by periodicity of the input clock signal.

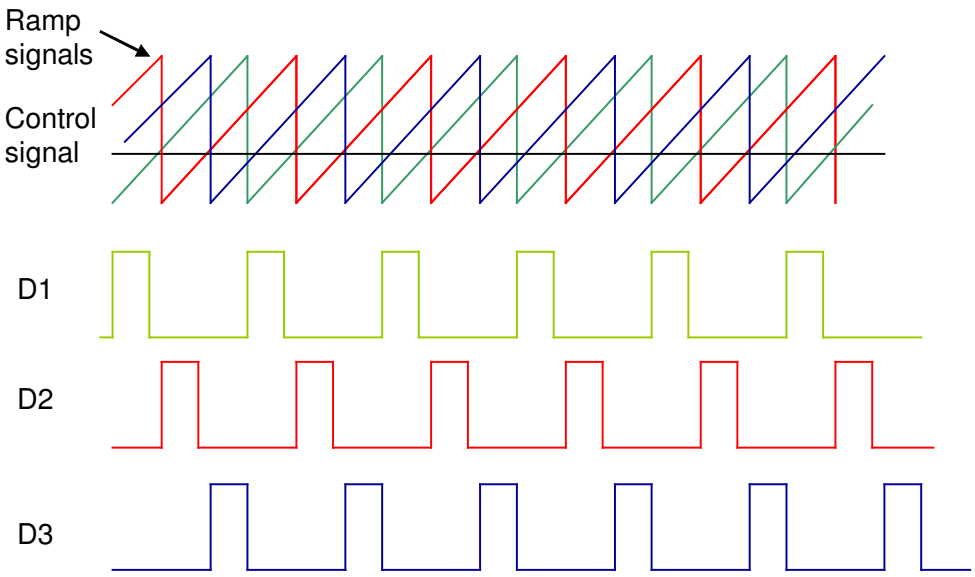


Figure 5.8 Duty cycle generated from shifted ramp signals

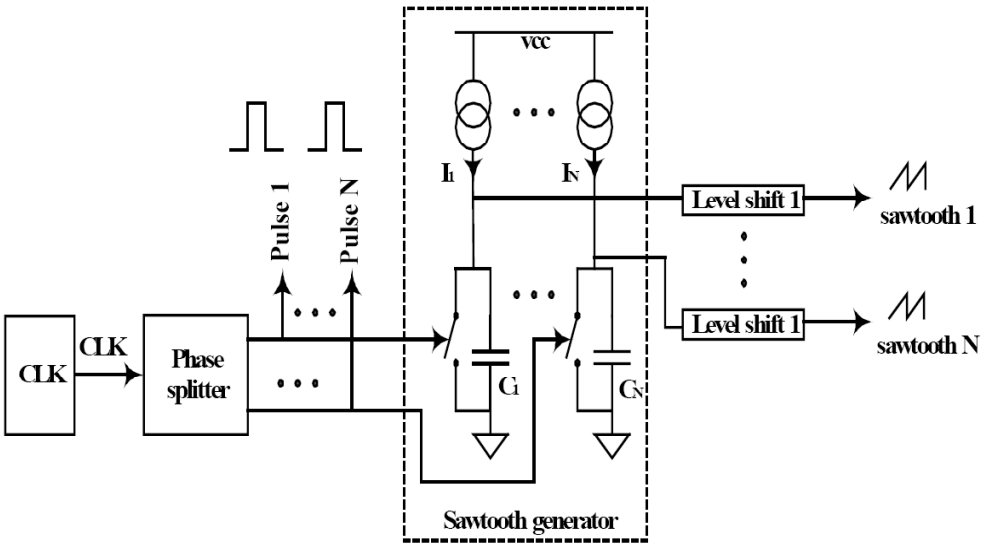


Figure 5.9 A circuit to generate interleaved ramp signals from a clock signal

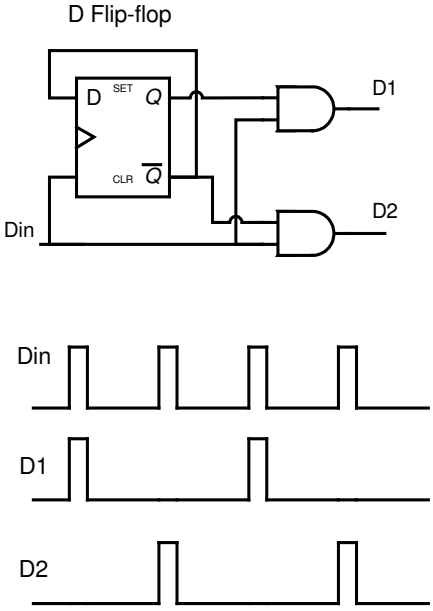


Figure 5.10 A circuit to split the clock signal

However, in the control schemes with variable switching frequency, there is no clock signal available for synchronization. The interleaving design is more challenging in these controls because the switching frequency and the switching phase are dynamically changing during operation. One design approach is to use the Phase Lock Loop (PLL)

circuit to dynamically synchronize the switching phases. A circuit to implement the PLL is shown in Fig. 5.11. The duty cycle signal in one of channels can be used as the reference clock signal. The phases of other duty cycle signals are locked to the reference clock signal. The phase shift can be accurately controlled in the PLL circuit, but there are some disadvantages of this approach. For instances, the phase detector circuit usually requires a low frequency filter. If the switching frequency is very low in some conditions, external passive components are necessary to realize the low cutoff frequency in the filter, which adds cost to the controller chip. Besides, the complexity of PLL circuits demand significant design efforts and silicon area. To overcome the problems with PLL approach, a much simpler design is proposed.

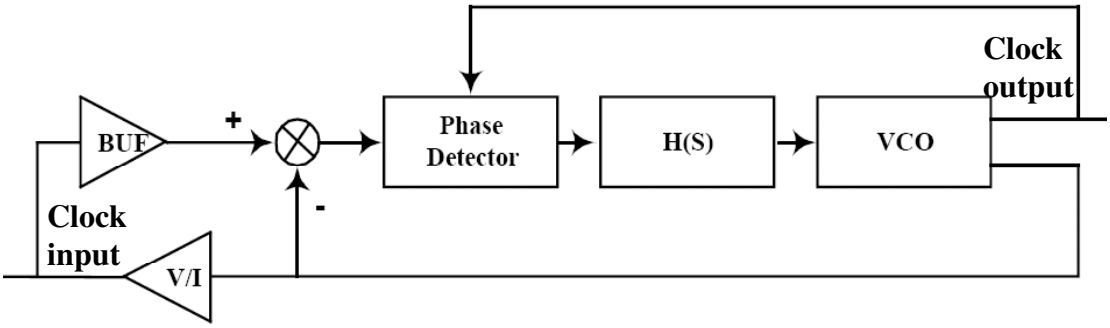


Figure 5.11 A circuit diagram to implement PLL

5.2.3 Proposed interleaving design

Fig 5.12 shows the proposed method to generate the interleaved duty cycle signals with variable switching frequency. The basic idea of the proposed design is to consider the multi-channel converter as a single-channel converter with increased switching frequency. In Fig.5.12, the "ON" pulse is the main switching signal controlled by the closed-loop feedback. The timing of the "ON" pulses is dynamically varying to keep the

output voltage within regulation. The duty cycle signals for each channel are selected from the "ON" signal by toggling the status of the multiplexer. In other words, the "ON" signal is passed to each individual channel one by one. If the pulses in the "ON" signal are periodic in the steady state, the phases of the duty cycle signals are evenly distributed among the channels. Similar design was reported in [Abu-Qahouq'04], however, the proposed design in Fig. 5.12 has advantage of glitch free and less delay from the "ON" signal to the output duty cycle signals. Because the T flip-flop is triggered by negative edges, the multiplexer changes status before the input pulse arrives. The delay from the input pulse "ON" to the output is reduced to one AND gate delay plus one RS-Latch delay.

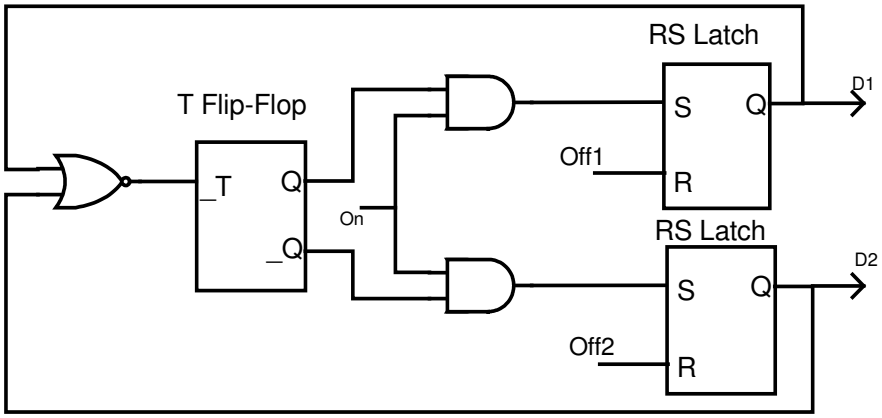


Figure 5.12 A multiplexer to generate interleaved duty cycle signals

In Fig. 5.12, the signals "OFF1" and "OFF2" are individually generated for each channel to determine the falling edges of the duty cycle signals or the duration of the on time, as shown in Fig. 5.13. Therefore, in each duty cycle signal, the turn-on is initiated by the common "clock" signal, i.e. the "ON" signal, and the turn-off is initiated by the timers in each individual channel. As we discussed in Section 4.4, the timers are adjusted by the input voltage, the reference voltage to keep the steady state switching frequency constant.

As we will discuss in Section 5.3.2, the "OFF" signals are also adjusted for the current sharing control. Both the "ON" signal and the "OFF" signals are dynamically varying under control of the feedback loop. The whole system operates like a Voltage Controlled Oscillator (VCO) in which the input signals are static signals, such as the input voltage, the reference voltage, and the output signal is a series of the pulse signals, such as the duty cycle signals. This arrangement provides a simple way to implement the variable frequency control for the multi-channel DC-DC converters.

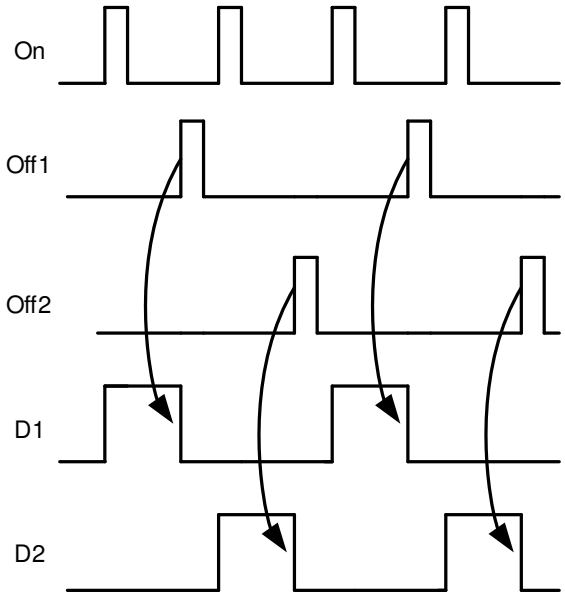


Figure 5.13 Timing diagram of the switching signals

Furthermore, the interleaving design in the proposed control architecture has been greatly enhanced by inductor current feedback. As shown in Fig. 5.14, inductor currents are summed and compared with the control signal from the voltage error amplifier. Since inductor currents have the same phases as the switching signals, the current waveforms serve as the phase detection signals naturally generated to feedback the phase shift among different channels. These current signals work similarly as the ramp signals in Fig. 5.8. If

the delay in the current sensing is neglected, the current signals can maintain the even phase shifting.

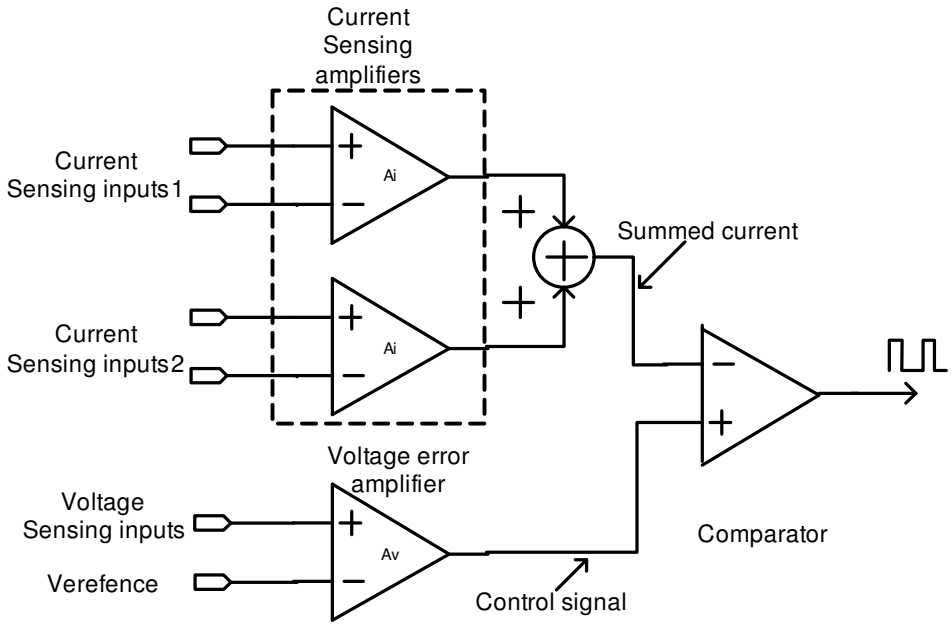


Figure 5.14 The current and the voltage feedback signals used in the control

However, the ripples in the control signal and the delays in current sensing circuits have significant impact to the interleaving performance. As shown in Fig. 5.15 (a), two current waveforms are perfectly interleaved with 180° phase shift when the control signal is stable, but in Fig.5.15 (b) the two current waveforms has uneven phase shifting when large ripples exist in the control signal. For the similar reason, delays in the current sensing amplifiers disturb the phase shifting by distorting the phase information. As rule of the thumb, the total delay in the current sensing circuits should be kept less than the on time of the switching cycle so that the delay has no deteriorating affect on interleaving performance.

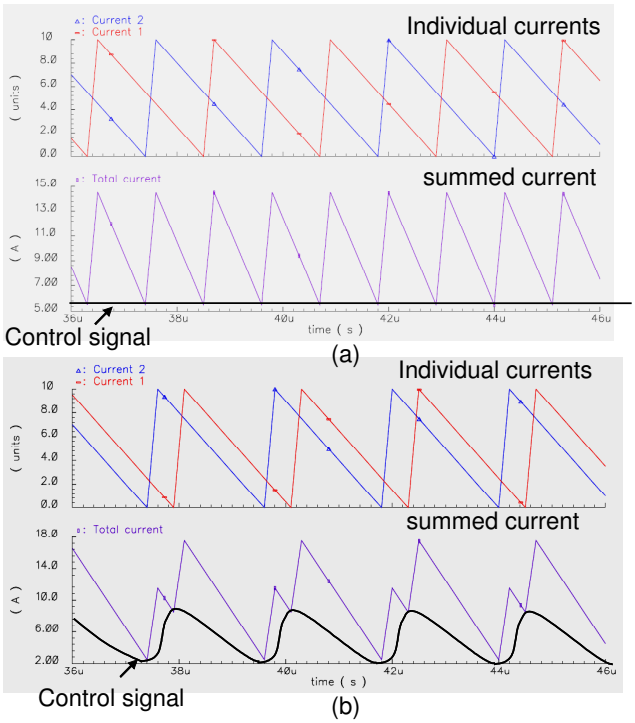


Figure 5.15 Ideal interleaving (a) and imperfect interleaving with unstable control signal (b)

5.3 Multi-channel current sharing

5.3.1 Review of current sharing design

In multi-channel DC-DC converters, mismatches among circuits and components affect the current distribution in different channels. For example, in Fig 5.8, the mismatch of the ramp signals will make duty cycles unequal in different channels. Even though the mismatch of duty cycles from controller circuits is completely compensated or trimmed, the drivers in different channels still introduce mismatches on the duty cycles since they are made by individual chips. Besides, mismatches of power switches, power inductors and PCB layout also affect current sharing among channels. Therefore, current sharing must be actively enforced by the control circuits. Some of techniques to achieve current sharing control are briefly introduced in this Section.

One simple method to maintain current sharing in the current mode control is to directly control the current level in each channel by a common control signal. As shown in Fig. 5.16, the peak current control limits the peak amplitude of the inductor currents by a common control signal, "Verr". If the comparator offsets and the mismatches of the external ramp signals ("Ext_ramp 1" ~ "Ext_ramp n") are ignored, the peak inductor currents in all channels are equally controlled. This current sharing design is widely used since it is simply inherited in the main control architecture. Similarly, the valley current control or some average current controls provide excellent features to achieve current sharing design. However, the mismatches in the ramp signals can cause unacceptable current imbalance. Some techniques are developed to deal with this issue, such as the ramp generator with automatic matching proposed in [Zhang-1'05].

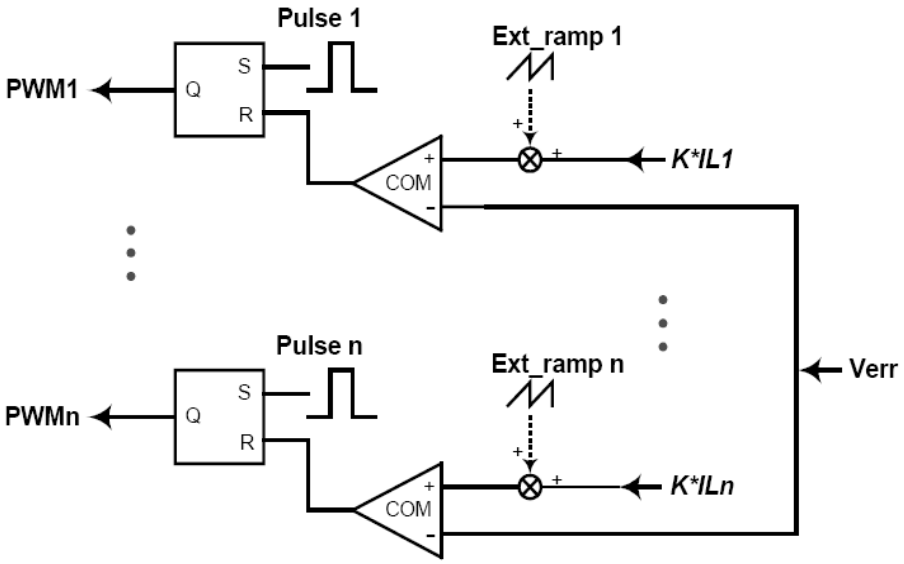


Figure 5.16 Current sharing design with peak current control

Some other techniques to achieve current sharing are using dedicated feedback loops for current sharing. These techniques are usually used together with the voltage mode controls in which no current signal is available in the main feedback loop. One example shown in Fig 5.17 has auxiliary circuits to calculate the average current of all channels and the error between the current in the individual channel and the average current. The error signals are injected back into the main control loop through the control signal, "Verr". Because of high loop gain in the current sharing loops, the inductor current in each channel is regulated around the average current of all channels. With the common current bus, it is possible to add or remove some channels without affecting the function of the whole system. Therefore, this architecture is widely used in configurable power systems. The stability and the dynamics of such current sharing systems are studied in [Sun'06].

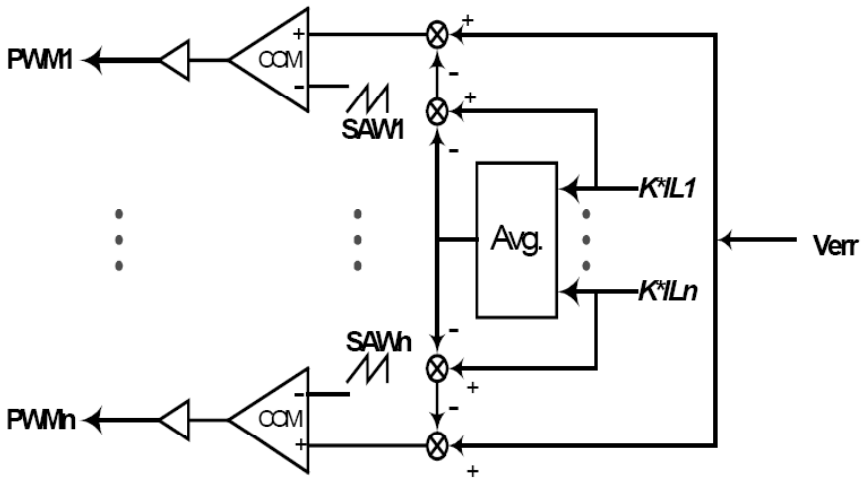


Figure 5.17 Current sharing design with common current bus

Fig 5.18 shows another example to use separated loop for current sharing. In this design, the current sharing control is built in the ramp generator. The current signals from different channels, "Vx1" to "Vxn", are used to change the levels of ramps. Because the duty cycles are adjusted by the level of ramp signals, the unbalancing current is reduced by the negative feedback.

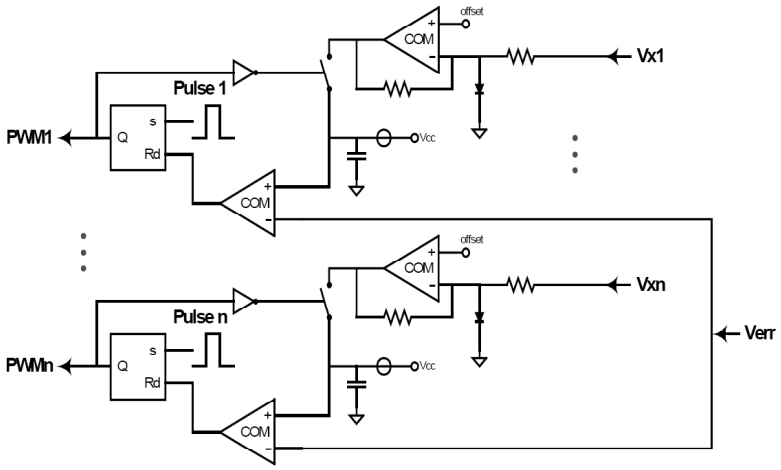


Figure 5.18 Current sharing design by adjusting the level of ramp signals

5.3.2 Proposed current sharing design

The techniques reviewed in the early section are mostly useful in the constant frequency PWM control. In the proposed control architecture, the main control loop uses the

summed current and the output voltage to generate the "ON" signal. The balance of the individual current needs be enforced by additional control loop. As we know, duty cycle can be changed by modifying either the on time or the off time. In the proposed control architecture, the main control loop modulates the off time to regulate the output voltage while the on time is left constant. If current sharing control is made by modulating the on time, the current sharing control can be separated from the main control. In such way, the control design can be greatly simplified, and interference between the two control loops is minimized. Therefore, the proposed current sharing control is designed to control the on time for each duty cycle signals. The design concepts and the circuit implementation are discussed in this section.

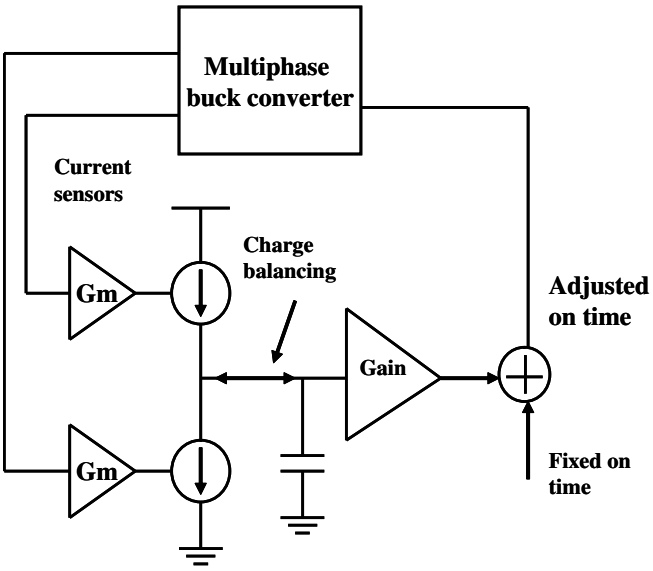


Figure 5.19 Current sharing design with on time modulation

The basic idea to implement current sharing control with on time modulation is illustrated in Fig. 5.19. As discussed in Chapter 4, the inductor currents are sensed by the transconductance amplifiers. In Fig. 5.19, the outputs of the transconductance amplifiers are summed together with a capacitor. Any unbalanced current will accumulate charge in the capacitor. In other words, if the charge in the capacitor is balanced at a constant level,

the inductor currents are also balanced. By this means, the current balancing is transformed into the charge balancing. The objective of the feedback control is to maintain the constant charge in the capacitor.

In Fig. 5.19, a gain stage is added within the current sharing loop to have high DC gain. The on time modulator is designed to add small variation to the fixed on time calculated from the voltage-controlled delay block in Fig 4.19. The adjusted on time varies when the voltage on the charging capacitor varies. With negative feedback, the current sharing is maintained between the two channels when the voltage on the charging capacitor is stable at a constant level. When there are more than two channels, one channel can be chosen as the reference channel. Each of the rest channels has its own current sharing loop to maintain its current equal to the reference channel.

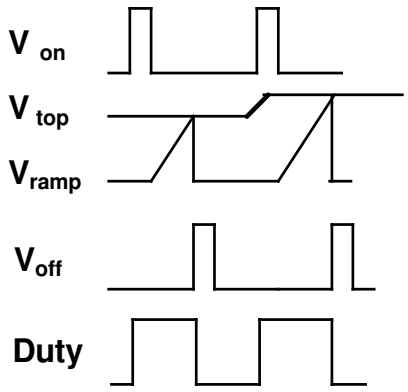


Figure 5.20 Adjusting on time for current sharing

The on time modulator is designed by adding small variation to the signal V_{top} as shown in Fig. 5.20. The V_{top} signal is used to control the delay time in Fig. 4.19. As discussed in Section 4.4, the V_{top} signal is designed proportional to the reference voltage. When the reference voltage changes, the V_{top} signal changes to adjust on time and maintain the steady state switching frequency almost constant. With the current sharing control, the

V_{top} signal has additional function to adjust on time to remove current imbalance. Since the V_{top} signal has much smaller adjustment for the current sharing control, it does not affect the function to maintain the switching frequency constant. The schematic of the gain stage and the on time modulator is shown in Fig. 5.21.

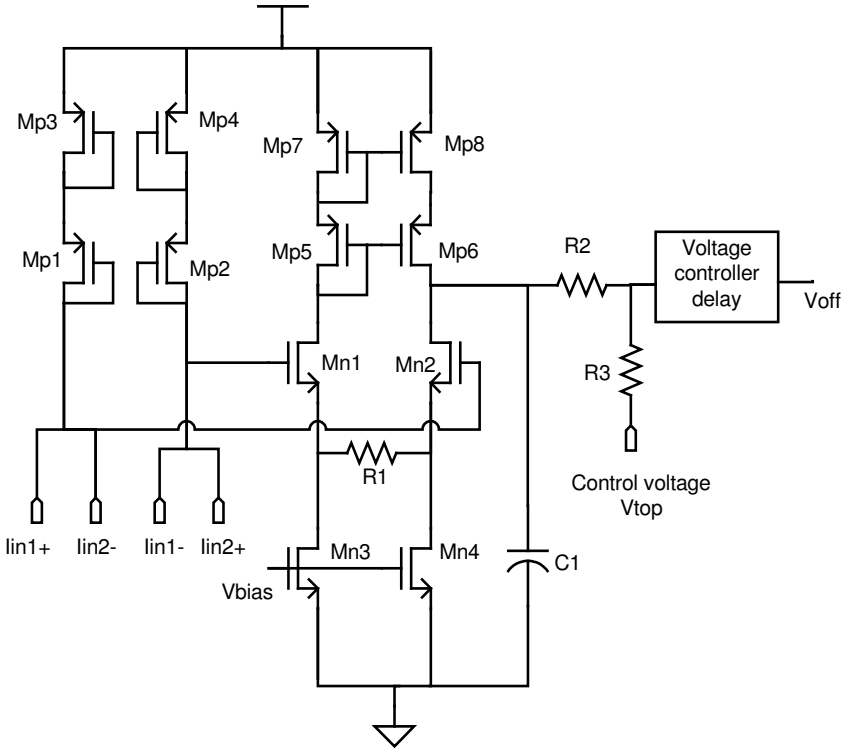


Figure 5.21 Schematic of gain stage and on time modulator for current sharing

The circuit has inputs of two differential current signals from the current sensing amplifiers. By crossing the polarity of the input currents, the difference between the two currents is extracted. The differential signal is amplified by a transconductance amplifier. To remove the ripples in the signals, C_1 is implemented with an external capacitor. The output of the gain stage adjusts the signal V_{top} through two resistors, R_2 and R_3.

5.3.3 Analysis of the current sharing loop

Because there are multiple poles and high DC gain in the current sharing loop, the stability of the current sharing loop is an important concern in the design. Besides, the dynamic performance of the current sharing function sometimes is also important. For example, with slow response of the current sharing design, some channels may have higher current at beginning of the transient events. In the applications with frequent transients events, the channels frequently exposed to the high stress could have reliability problem.

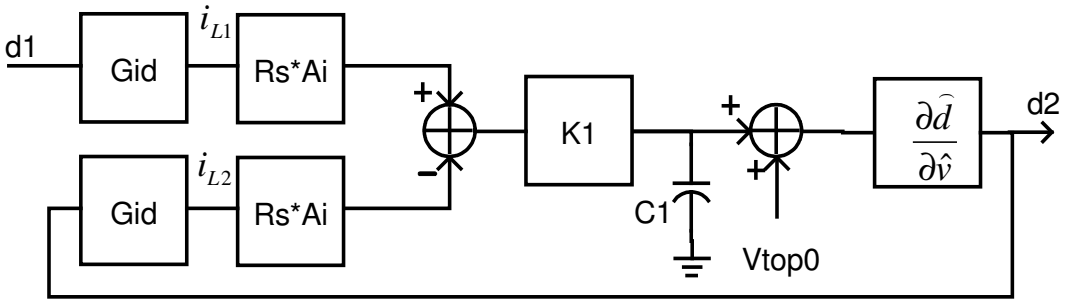


Figure 5.22 Small signal model to analyze system dynamics of current sharing control

To analyze the current sharing control loop, a small signal model is built as shown in Fig. 5.22. In this model, one of the two channels is used as the reference for the other channel. The terms in the model are described as follows:

$d1, d2$: duty cycles for two channels;

G_{id} : transfer function from the duty cycle to the inductor current;

$R_s * A_i$: current sensing gain;

G_m : transconductance of the gain stage;

$\frac{\partial \hat{d}}{\partial \hat{v}_{top}}$: modulation gain from V_{top} to the duty cycle.

The loop gain for the current sharing is

$$T_{csh} = \frac{G_{id} R_s A_i G_m}{sC_1} \frac{\partial \hat{d}}{\partial \hat{v}_{top}} \qquad (5.1)$$

To simplify the estimation of the modulation gain $\frac{\partial \hat{d}}{\partial \hat{v}_{top}}$, frequency variation is ignored. With this assumption, the modulation gain is simply determined by the slope of the ramp in Fig. 5.20 and the steady state switching frequency:

$$\frac{\partial \hat{d}}{\partial \hat{v}_{top}} \approx \frac{f_s}{S_{ramp}} \qquad (5.2)$$

Therefore, the loop gain of the current sharing loop is estimated as:

$$T_{csh} \approx \frac{G_{id} R_s A_i G_m f_s}{sC_1 S_{ramp}} \qquad (5.3)$$

In the design, most of the parameter in (5.3) is predetermined by other factors. The parameters used to design stable current sharing loop are transconductance of the gain stage, G_m, and the charging capacitor, C_1. In practical applications, some of parameters are fixed by the internal circuits. The system stability can be maintained by choosing proper value of C_1.

5.4 Summary of Chapter 5

Interleaving and current sharing are two important design requirements in the high current multi-channel DC-DC converter design. The techniques to implement interleaving and current sharing are reviewed in this Chapter. Most techniques are based on conventional constant frequency PWM control in which the switching can be synchronized by the clock signal. For the proposed control with variable frequency, the interleaving and current sharing design must base on the structure of the main control without adding too much of complexity.

The proposed design for interleaving uses an internal signal generated in the main control loop, the “ON” signal, as the clock signal. The phases of each channel is controlled by a glitch-free multiplexer. The even distribution of phases is enhanced by using the current sensing circuits as the phase detector for each channel. This design is much simpler than the design with PLL.

The proposed current sharing design uses the current in one of the channels as the reference for the other channels. The current sharing loop is added to the main control loop by modulating the on time. The balance of the currents is detected by the charge balance in a capacitor. The circuit for the current sharing is described and a small signal model is presented to analyze the stability and dynamics of the current sharing loop.

Chapter 6 Simulation and Experimental Verification

6.1 Prototype design

A prototype controller was designed for the Voltage Regulator Modules (VRM) used in notebook computers. Compared with the VRM used in desktop computers, the mobile VRM is required to work with wider range of the input voltage and the output voltage, and there are more sophisticate mode transitions. For example, Intel introduced the Intel Mobile Voltage Position (IMVP) technology on Pentium mobile microprocessors. With IMVP technology, the supply voltage of the CPU dynamically changes with its operation modes, such as the active mode, the deep sleep mode, the deeper sleep mode and the shutdown mode. The output voltage of the VRM in each mode and the slew rate during mode transition are specified by CPU's manufacturers. The challenge of the controller design is to meet all these requirements while keeping high reliability, small profile, low cost, etc. The prototype controller was designed according to the IMVP-IV specifications. Some of the design targets are summarized in Table 6.1:

Table 6.1 Specification parameters of the designed VRM controller

Input Voltage	5 V ~ 20 V
Output voltage	0.7 V ~ 1.7 V
Load current	0 ~ 40 A
Switching frequency at steady state	200 KHz ~ 600 KHz
Channels	2
Modes	Active/ Sleep/Shutdown
VID bits	6
Supply voltage	5 V

The controller chip was implemented with 5V CMOS 0.5µm technology with bipolar options. The chip microphotograph is shown in Fig. 6.1. The chip package is TQFN-40. The pin arrangement of the controller chip is shown in Fig. 6.2. The description of the pins is listed in Table 6.2.

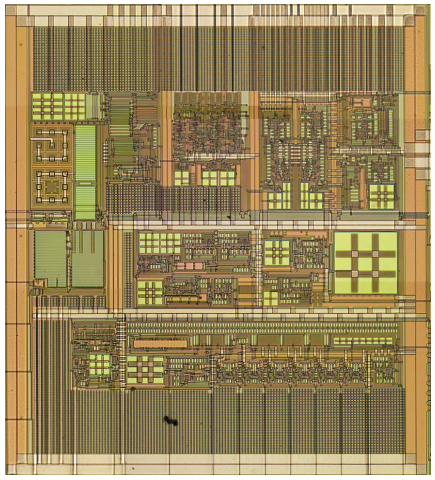


Figure 6.1 Microphotograph of the controller chip

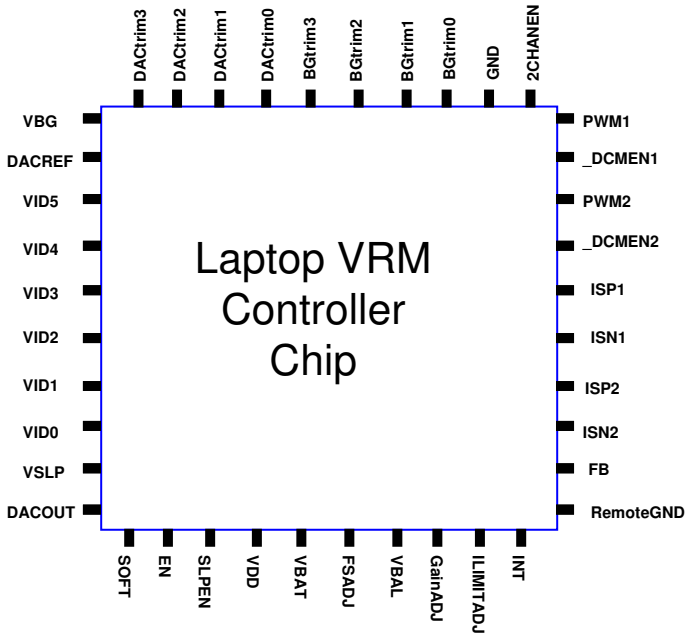


Figure 6.2 Pin-out of the prototype controller

Table 6.2 Pin descriptions of the controller chip

Pin name	Pin description
VDD	5V power supply
GND	Ground of the controller chip
PWM1, PWM2	Output of the duty cycle signal for each channel
_DCMEN1, _DCMEN2	Output of DCM enable signals for sleep mode
ISP1, ISN1, ISP2, ISN2	Input of current sensing signals
FB	Input of the feedback signal
RemoteGND	Input of the remote ground sensing
EN	Input of Chip enable signal
SLPEN	Input of sleep mode enable signal
2CHANEN	Input of channel 2 enable signal
VBG	Output of bandgap reference signal
DACREF	Output of DAC reference signal
FSADJ	Input to adjust switching frequency
GAINADJ	Input to adjust gain of voltage error amp.
ILIMITADJ	Input to adjust current limit
VBAL	Connection to current sharing capacitor
INT	Connection to integrator capacitor for error correction
SOFT	Connection to capacitor for soft reference transition
VBAT	Input of battery voltage sensor
DACOUT	Output of DAC
VSLP	Input of reference for sleep mode
VID [0:5]	Input of VID signals
BGTRIM[0:3], DACTRIM[0:3]	Trim inputs for bandgap and DAC

6.2 System simulation

The designed blocks and the DC-DC converter system were simulated with HSPICE. The parasitic components, mismatches of external components and noise in the power stage were included in the top-level simulation to test the robustness of the circuits. Some of the simulation results are included in Fig. 6.3 to 6.7.

Fig 6.3 shows the load transient response with load current from 0A to 40A. The simulation was performed with 1mF output capacitor and 300nH output inductor. The simulation results show desired AVP waveform with about 50 mV voltage drop. The performance of current sharing control is also verified by this simulation.

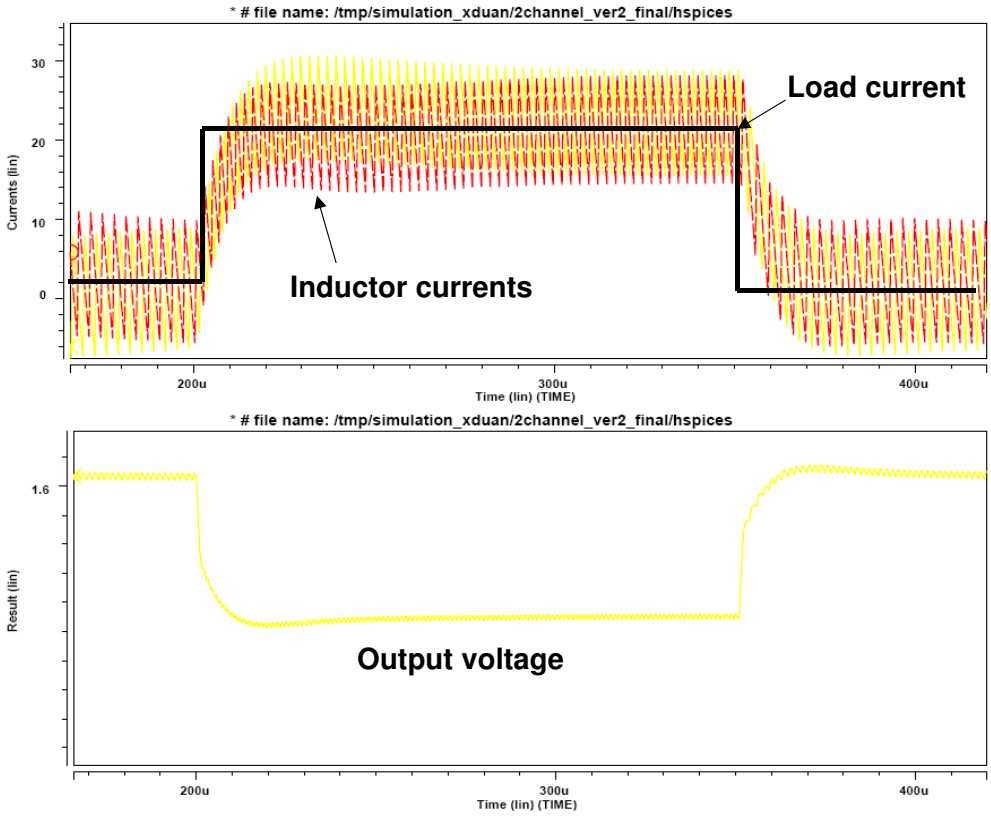


Figure 6.3 Transient simulation results

Fig. 6.4 shows the simulation waveforms of initial startup and mode transition between the active mode and the sleep mode. After the chip is enabled, the converter starts up with

the controlled slew rate so that the initial current does not beyond the safety limits. In the active mode, the inductor current is in CCM (Continuous Conduction Mode). After the sleep mode is enabled, the converter goes into DCM (Discontinuous Conduction Mode). The switching frequency in the sleep mode is much less than in the active mode. The output voltage in the sleep mode is lower than in the active mode to further save the power consumption of the CPU.

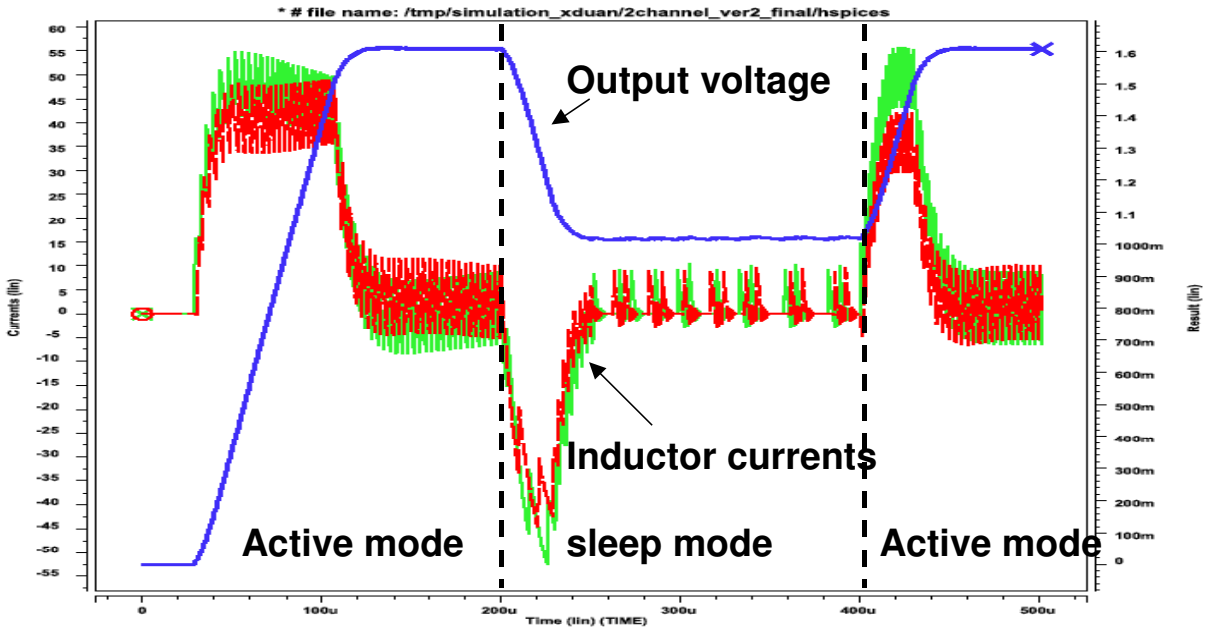


Figure 6.4 Simulation of mode transition between active mode and sleep mode

Fig. 6.5 shows the simulation waveforms when the input voltage sweeps from 20 V to 5 V. The converter works stably with the whole range of the input voltage. Since the switching frequency is regulated around 400 KHz by the on time control, the ripple of the inductor current decreases with the falling input voltage.

Fig. 6.6 shows the simulation results of dynamic VID control. Since the reference of the converter is generated by the DAC with VID inputs, the output voltage of the converter is controlled by the VID inputs. In this simulation, the VID is transited between the

minimum (000000) to the maximum (111111), the output voltage sweeps between 1.7V and 0.7V with the controlled slew rate. The slew rate control is adjusted by an external capacitor. The maximum slew rate is limited by the maximum current allowed during the transition.

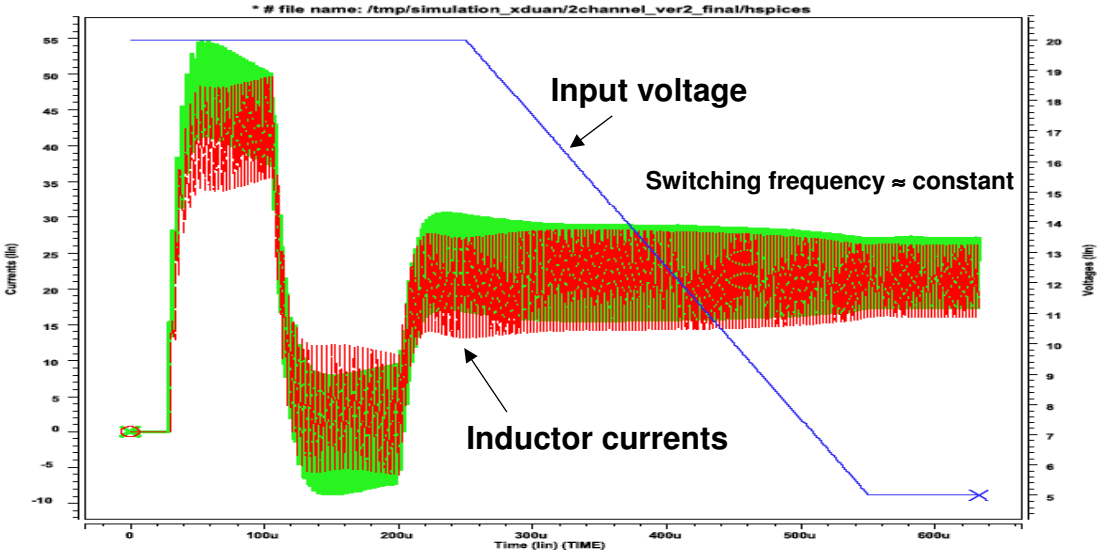


Figure 6.5 Simulation with input voltage varying from 20 V to 5 V

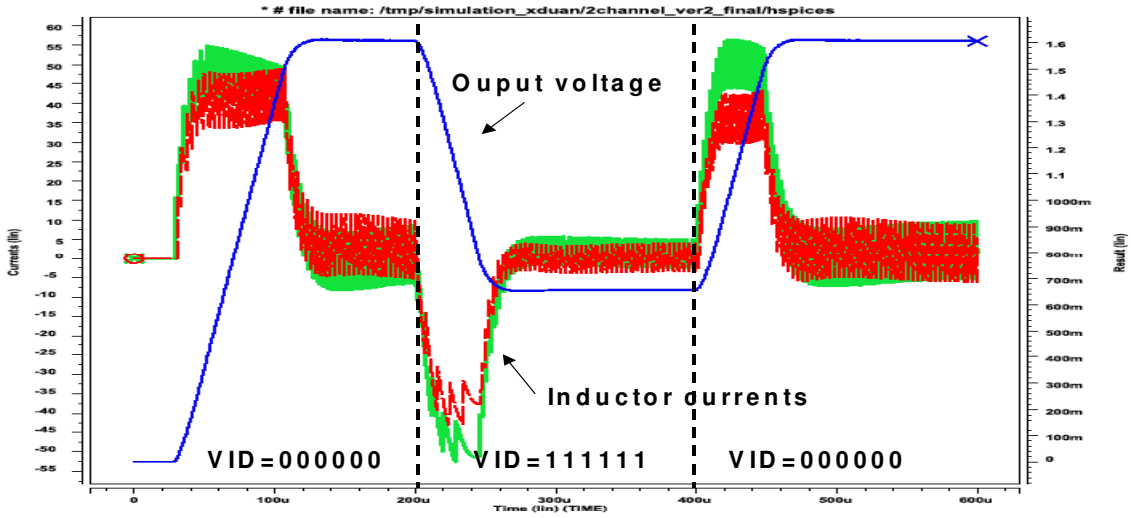


Figure 6.6 Simulation of dynamic reference voltage

6.3 Experimental results

The VRM test board shown in Fig. 6.7 is designed to test the controller chip. The components used in the test are listed in Table 6.3.

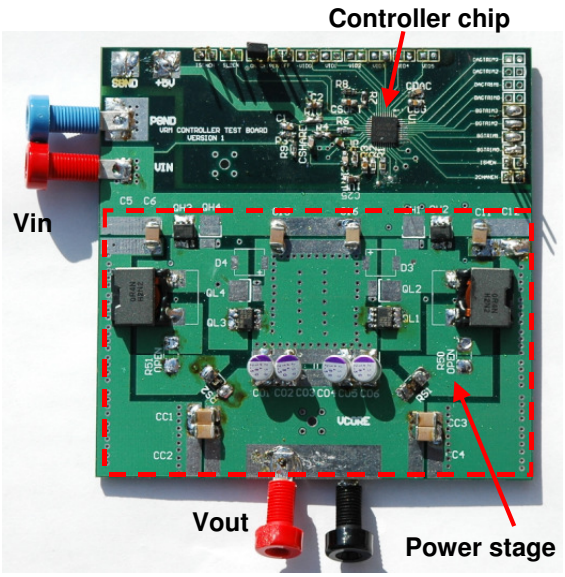


Figure 6.7 Test board for the controller

Table 6.3 List of components used in the test

Component	Part name
High side power MOSFET	IRF7811
Low side power MOSFET	IRF7822
Driver chip	LM2722
Output inductor	400nH/1.5mΩ
Output bulk capacitor	OSCON cap 270uF*4
Decoupling capacitor	Ceramic cap 47uF*4

The steady state waveforms in the active mode and the sleep mode are shown in Fig. 6.8 and Fig. 6.9, respectively. The system works stably with constant switching frequency at steady state. The test results show good current balancing and interleaving between the

two channels. Small output voltage ripples are achieved by ripple cancellation, as shown in Fig. 6.10.

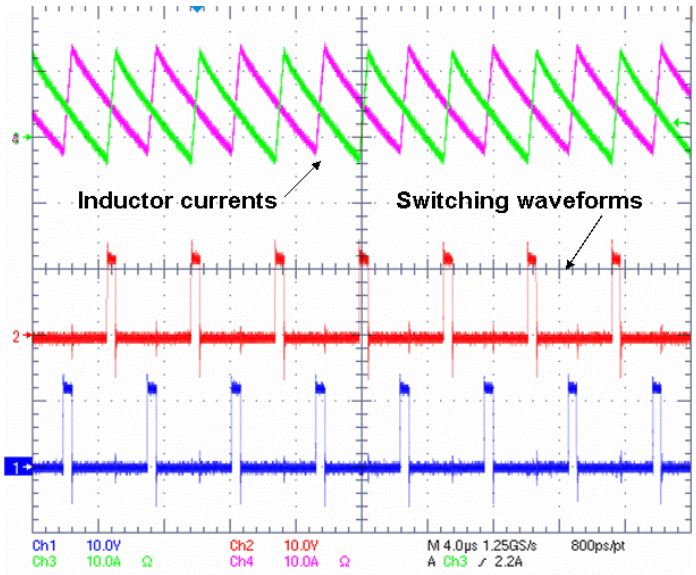


Figure 6.8 Active mode Vin=12V, Vout=1.2V, Io=10A

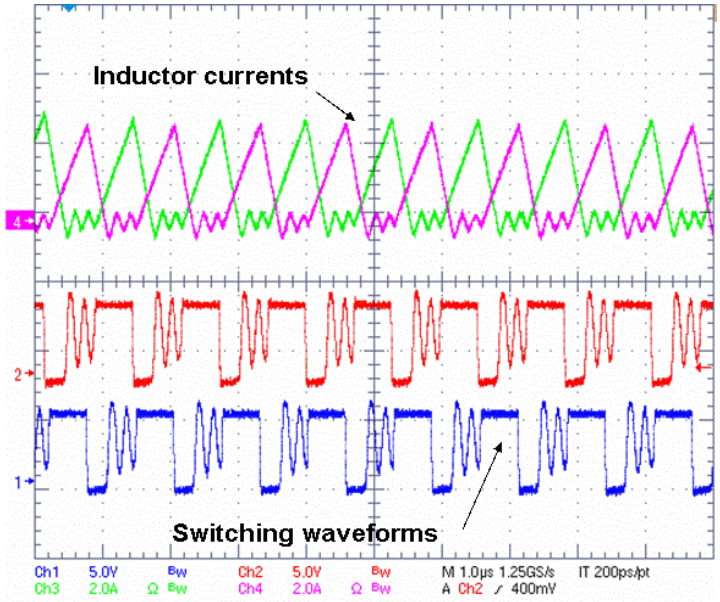


Figure 6.9 Sleep mode, Vin=5V, Vout=1.2V, Io=5A

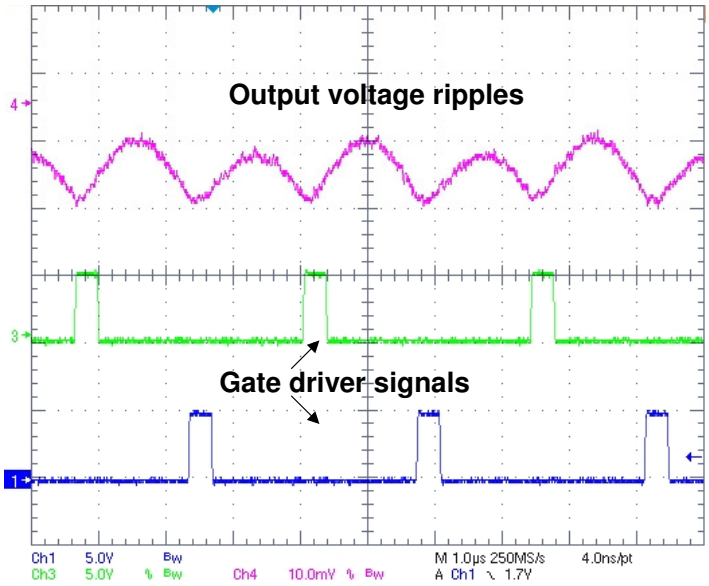


Figure 6.10 The output voltage ripple: Vin=12V, Vo=1V

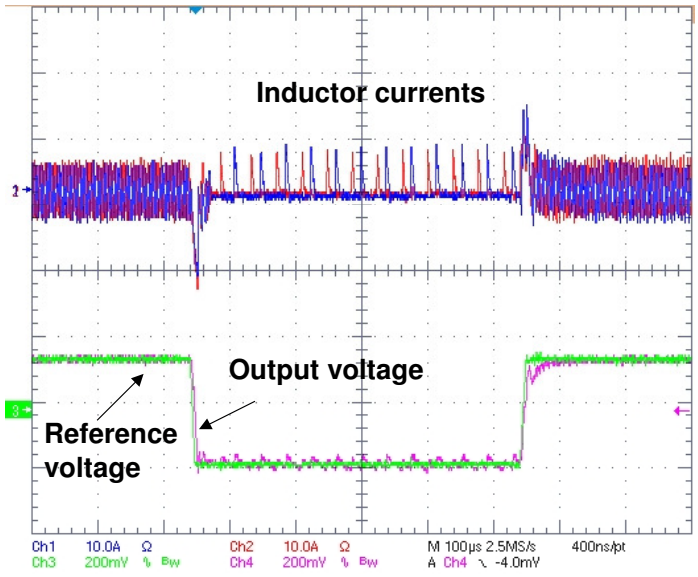


Figure 6.11 Transition between active mode and sleep mode

The voltage transition during mode transition and VID transition were tested, as shown in Fig. 6.12 ~ 6.13. The output voltage follows the reference voltage that transits with constant slew rate controlled by an external capacitor.

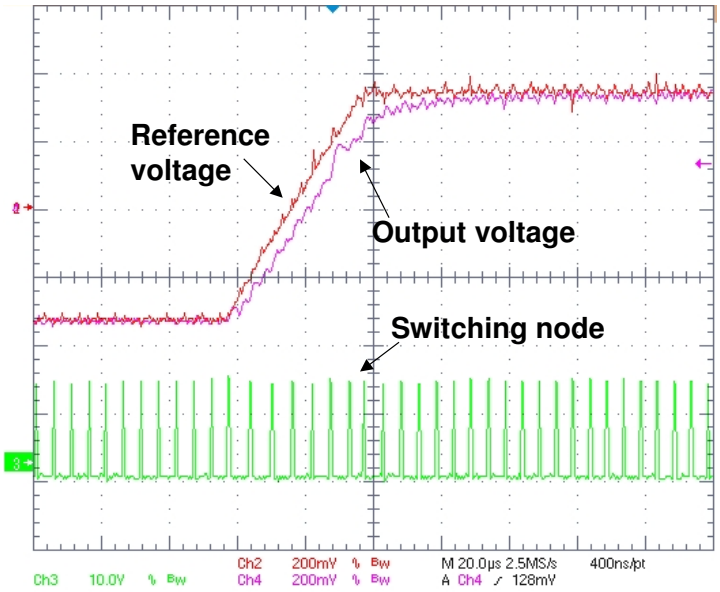


Figure 6.12 VID step-up transition

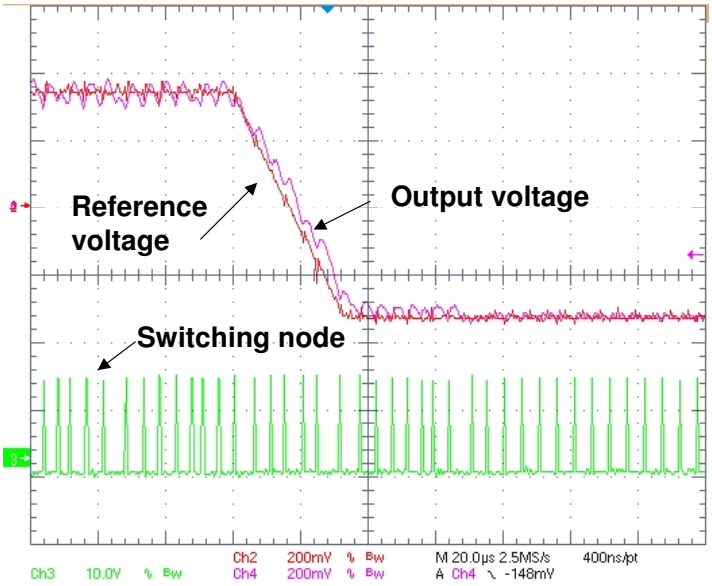


Figure 6.13 VID step-down transition

The load transient were tested with maximum current slew rate of 50A/µs. As shown in Fig. 6.14, the controller has good response to load transient with output capacitance as low as 1 mF. Voltage spikes are well below the AVP window. The droop resistance of the AVP is adjustable from 1.5 mΩ to 3 mΩ. The trajectory of the output voltage and the load current is plotted in Fig. 6.15.

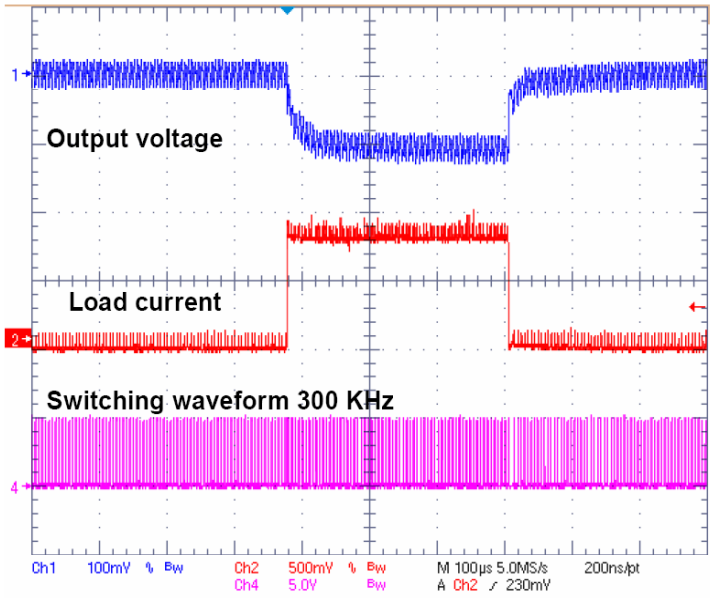


Figure 6.14 Load transient: Vin=12V, Vout=1.2V, Io=0~40A

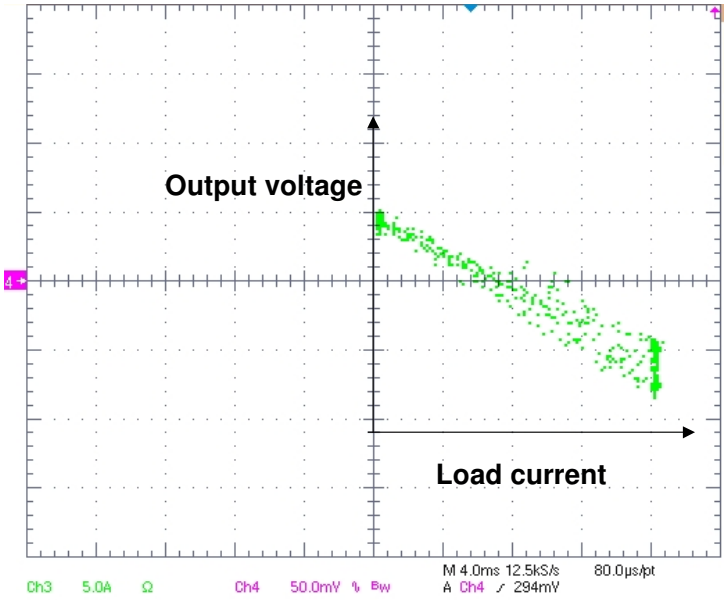


Figure 6.15 The trajectory of output voltage and load current

The steady-state switching frequency was measured with input voltages varying from 5 V to 18 V. From the test results plotted in Fig. 6.16, the variation of switching frequency is less than 5%.

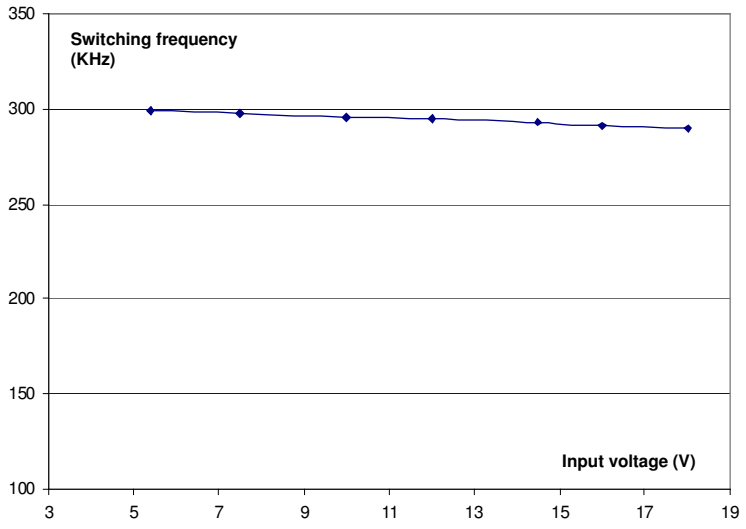


Figure 6.16 Steady-state switching frequency v.s. input voltage

The output voltage error is measured as difference between the output voltage and the reference voltage. Fig. 6.17 shows test results with the reference voltage from 0.9 V to 2.3 V. The output voltage error is limited less than ± 4 mV in the experiments.

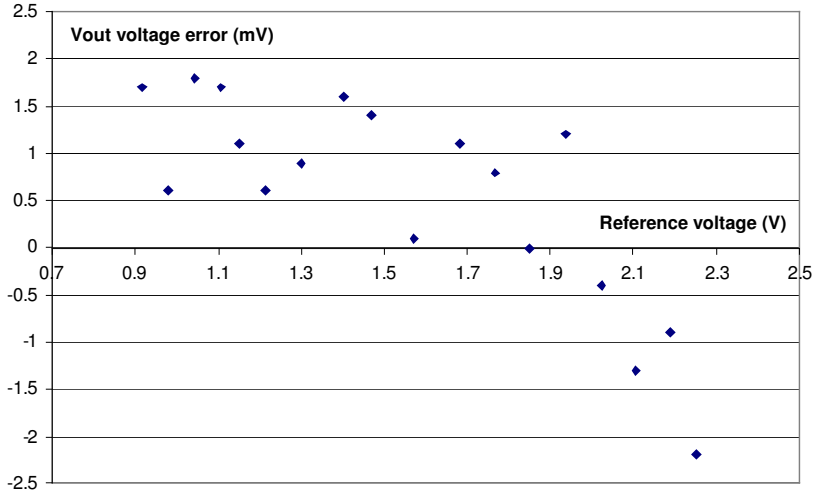


Figure 6.17 Output voltage error v.s. reference voltage

6.4 Summary of Chapter 6

In Chapter 6, the system level simulation, the prototype design and some of the test results are presented. The prototype controller is designed for two-channel 40A DC-DC converter for Intel Pentium mobile CPUs. The chip is tested with the input voltage from 5V to 20V and the load current from 0A to 40A. The test results verified the major functions implemented in the controller, including two channel interleaving, current sharing, sleep and active mode, dynamic reference transition, frequency regulation. The measurements show the designed two-channel DC-DC converter has good load transient response, smooth mode transition, and accurate voltage regulation. Some of the test results are summarized in Table 6.4:

Table 6.4 Summary of test results

Maximum input voltage range	3 V ~ 20 V
Output voltage	0.7 V ~ 2.3 V
Maximum load current	40 A
AVP droop resistance	1.5 mΩ ~ 3 mΩ
Output voltage error	$< \pm 4$ mV
Switching frequency at steady state	200 KHz ~ 600 KHz
Maximum slew rate of output voltage	≈ 50 mV/μs
Switching frequency variation (Vin = 5 V ~ 18 V)	< 5%
Efficiency at 30 A (active mode, 300KHz)	≈ 85%
Efficiency at 1 A (sleep mode)	≈ 87%

Chapter 7 Conclusion and Future Work

7.1 Conclusion

Development of digital core chips poses serious challenges to the power supply design. High performance switching DC-DC converter must meet requirements of high current, low voltage tolerance, fast transient response, high power efficiency, small profile and low cost. The conventional PWM control with constant switching frequency has limitation to improve both transient response and power efficiency because there is a conflicting requirement on switching frequency. The control scheme with variable frequency has promising features to achieve better overall performance, but the issues in the reported design approaches limit their usefulness in the practical applications. This dissertation presents novel control architecture with variable switching frequency and novel implementation of the integrated controller. The control concept and the proposed circuits are verified by the prototype chip designed for mobile VRM applications. The contributions of this work are summarized as followings:

1. A novel implementation of current-mode variable-frequency control is proposed. The system architecture features a dual-loop feedback and a unique structure with symmetric signal paths for voltage and current signals. The symmetric structure provides practical advantages for integrated controller design to achieve accurate control on the AVP droop resistance. Compared with reported control techniques, the proposed control architecture has advantages of improved transient response without increasing steady-state switching frequency, simple compensation design and high feasibility for practical implementation.

2. The proposed control architecture is analyzed with a small-signal model. With the small-signal model, design guidelines are derived to achieve constant output impedance. The implementation of compensation is simplified to design a first-order low pass filter and an integration capacitor. The model was verified by both circuit simulation and model simulation.
3. Novel circuits based on fully differential structure are proposed to implement the control core function. The current sensing amplifier and the voltage error amplifier have features of high noise immunity, good gain matching and programmable gain ratio. The comparator in the constant on time modulator has a feature of automatic error correction through offset control. These circuits are verified in the prototype controller. The techniques in these circuits can be used for other applications.
4. The implementations of interleaving and current sharing for the proposed variable control are proposed. With the proposed interleaving design, even phase distribution among the interleaved channels is achieved without using PLL. In the proposed current sharing design, the current balance is maintained by the charge balance on the capacitor. The current sharing control is designed with simple circuit compatible with the main control structure. A small signal model is built to analyze the current sharing loop.

7.2 Future work

Along with the development of semiconductor technologies, the requirement on the power supply is becoming more diverse and strict. In the whole system, the power management block becomes an important part that affects the reliability, the portability and the cost of the system. This dissertation tries to address the issues in the specific application, such as the VRM for the CPU, however, the design concepts have potential to be extended to other applications. There are some interesting research directions:

1. The proposed control architecture and the circuit implementation have succeed to work with switching frequency up to 600 KHz at steady state. When the switching frequency is pushed even higher, the system stability becomes a severe issue because the delay and the noise in the circuits begin to interfere with the control signals. It is important to understand how the delay and the noise affect the system. With this knowledge, it is possible to design the control circuits more robust to the delay and the noise.
2. In variable frequency control, switching frequency varies when there is load transient or input voltage variation. The noise associated with the switching frequency may affect some circuits that are sensitive to noise. To solve this problem, more sophisticate control on the switching frequency may be needed. One possible approach is to control the switching frequency according to the operation of the load system. The switching frequency itself can be a control variable to obtain optimal performance for the system.
3. For the portable applications, the power consumption in the standby mode is an important concern to extend the battery lifetime. In the designed controller, sleep mode control reduces the switching frequency to improve the efficiency. To

further improve the efficiency, optimal control may be designed in the sleep mode. For example, the peak amplitude of the inductor current can be adjusted according to load current, input voltage to achieve higher power efficiency.

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