

Abstract

OH, JAEHWAN. Electrical Characterization of TiSi_2 Nanoscale Islands by Scanning Probe Microscopy. (Under the direction of Robert J. Nemanich)

Using conducting tip atomic force microscopy (c-AFM), we have measured the current voltage characteristics of individual sub-micron islands of TiSi_2 on Si(100) surfaces and we have developed an imaging approach that distinguishes the electrical properties of the islands. The Schottky barrier height (SBH) of the sub-micron TiSi_2 islands was deduced from the I-V measurements. The results indicate that there is a significant variation of SBH among the islands on the same surface. The measurements employ a conventional AFM with a heavily B-doped diamond tip to obtain the current-voltage relations. In contact mode AFM, electrical signals are extracted independently from the topographic image. In addition, we have developed a new imaging method to probe the local electrical properties of a surface with regions of different conductivity. Using a lock-in technique both phase and amplitude images were obtained, and the resultant image is essentially a map of the differential surface conductivity. Using this method, TiSi_2 islands on a Si(100) surface were imaged. This approach can be readily extended to other materials systems.

Nanoscale TiSi_2 islands of lateral diameter of ~ 5 nm are formed by electron beam deposition of a few monolayers of titanium on atomically clean Si(111) 7×7 surface followed by *in situ* annealing at high temperatures (800-1000°C). Direct probing of the electrical characteristics of these islands was performed using ultra high vacuum scanning tunneling microscope (UHV-STM) and scanning tunneling spectroscopy (STS).

We form a double-junction system for observation of single electron tunneling effects such as Coulomb blockade and Coulomb staircase. Moreover the small dimensions of the system allow room temperature observation. The experimental results are compared with the numerical fitting values and they are in good agreement. Utilizing the prediction by the orthodox theory, we can explain our observation within the framework of single electron tunneling. We have observed the dependence of single electron tunneling on the doping type of the substrate. This result suggests that the nanoscale Schottky barrier in island-substrate interface can play a role as a tunnel barrier in this structure.

Electrical Characterization of TiSi_2 Nanoscale Islands by Scanning Probe Microscopy

By

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To my family

Biography

Jaehwan Oh was born on April 24th, 1967 in Namwon, Korea to Jung-Ja Kang and Hae-Sun Oh. The family moved to Seoul when he was 2 years old. He is the eldest son of four brothers. He was interested in science and engineering as a teenager and enrolled at the Seoul National University to major physics education. He earned the Bachelor of Science in Physics Education in 1989.

For his graduate studies, Jaehwan moved to the United States and earned the Master of Science in Physics at the College of William and Mary in Williamsburg, Virginia in 1992. While studying there, he developed the interest in the area of surface and interfaces. After fulfilling the mandatory military service as a civil service agent in Korea, he returned to the U.S. to resume his Ph.D. work at North Carolina State University in Raleigh in the fall of 1996.

Jaehwan married Kristen Hyun Kim in May 1997. At the same time, he decided to work for Professor R. J. Nemanich in the surface science laboratory, after passing the qualifier. For the next four years he studied surface and interface of metals and semiconductors with scanning probe microscopes as main characterization tools. He completed his Ph.D. on July 20, 2001.

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List of Abbreviations

AES	Auger Electron Spectroscopy
AFM	Atomic Force Microscopy (Microscope)
BPF	Band Pass Filter
c-AFM	conducting AFM
CITS	Current Image Tunneling Spectroscopy
CNL	Charge Neutrality Level
CVD	Chemical Vapor Deposition
DAC	Digital-to-Analog Converter
DOS	Density of states
EFM	Electrostatic Force Microscopy (Microscope)
FET	Field Effect Transistor
FL	Fermi Level
HOPG	Highly Oriented Pyrolytic Graphite
IR	Infrared
LDOS	Local Density of States
LEED	Low energy Electron Diffraction
lps	line per second
MFM	Magnetic Force Microscopy
MIGS	Metal-Induced Gap States
MOS	Metal-Oxide-Semiconductor
PSPD	Position Sensitive Photodetector
PZT	Lead Zinc Titanate
SBH	Schottky Barrier Height
SCM	Scanning Capacitance Microscopy (Microscope)
SEM	Scanning Electron Microscopy
SET	Single Electron Tunneling
SMU	Source Measure Unit
SPM	Scanning Probe Microscopy (Microscope)
SSL	Surface Science Laboratory
STM	Scanning Tunneling Microscopy (Microscope)
STS	Scanning Tunneling Spectroscopy
TEM	Transmission Electron Microscopy
UHV	Ultra High Vacuum
UPS	Ultraviolet Photoelectron Spectroscopy
XPS	X-ray Photoelectron Spectroscopy

Chapter 1. Introduction

1.1 Motivation

As device structures approach the nanometer scale it is necessary to characterize electrical properties on the same scale. In this size regime conventional electrical characterization approaches are limited by lithographic dimensions and probe positioning. Surface spectroscopic tools such as x-ray or ultra violet photoelectron spectroscopy (XPS or UPS) give area-averaged information even though they provide important information about the surface and interface electronic properties. Therefore, more approaches based on scanning probe techniques are being considered.

Since the inception of scanning tunneling microscope (STM) in 1981 by Binnig and Rohrer, many variations of STM have been introduced [1]. These scanning probe microscopies (SPM) can provide location specific information. STM is a powerful tool for imaging the clean surface with atomic resolution. Spectroscopic analysis can be obtained by sweeping the tip (or sample) voltage. However STM is limited to the surface of metals or semiconductors due to its imaging mechanism, which involves the tunneling of electrons. The morphological and electrical properties can be separated more distinctly in conducting atomic force microscopy (c-AFM), and the technique can provide electrical properties of the surface that are not accessible from STM. The most direct approach is to use c-AFM and to record local I-V measurements at the regions of interest.

Previous studies have shown that a thin layer of titanium reacts with the silicon substrate to form nanometer scale silicide island structures [2-5]. The silicide island formation process depends on the surface and interface energies. These results

demonstrated that it may be possible to control the surface dynamics to achieve the desired silicide nanostructures. In addition to the morphological study of these TiSi_2 islands, understanding their electrical characteristics is necessary in order to make any assessment for future electronic application. But direct electrical probing has not been reported to date.

As the dimensions of the semiconductor structures approach nanometer scale single electron transport effects are observed. A nanoscale island ($d < 5\text{nm}$) between two electrodes with tunnel barriers forms a double-barrier structure, which will exhibit these effects. When the energy required to add a single electron to the island becomes much larger than the thermal fluctuation energy and the electron transport is inhibited for a range of voltage. This phenomenon is known as Coulomb blockade and Coulomb staircase [6].

It is our intention to enable local electrical measurements utilizing a c-AFM and STM on these nanostructures. In this work we have measured the local I-V characteristics of TiSi_2 nanoscale islands using the both techniques. We also have developed a new imaging method that enables one to identify the areas of different conductivities using a lock-in detection technique. The resulting map of differential conductivities of the surface is combined with the results from the I-V measurement to give a more detailed picture of sub-micron Schottky barriers.

1.2 Scope of the thesis

In chapter 2, we review some of the most basic ideas that will be necessary in understanding the results that are presented in the following chapters. In the first section

we review the interface of a metal and a semiconductor and their electrical properties. In the following section, we review the physics of single electron tunneling (SET) and previous results of SET effects involving a metal-semiconductor system in particular.

In chapter 3, we will review STM in terms of electrical characterization. First, the scanning tunneling microscope is reviewed. Its operational principle, instrumentation, and scanning tunneling spectroscopy (STS) will be briefly described. In STS, it is possible to identify local electrical properties with nanometer precision. The qualification of our STM as a tool is evidenced by atomic scale resolution and spectroscopic data.

In chapter 4, we discuss AFM techniques in general. Conducting AFM is also reviewed for its role in electrical characterization of local surface structures.

In chapter 5, we give the description of the experimental facilities that are not mentioned in the earlier chapters such as ultra high vacuum (UHV), auger electron spectroscopy (AES), and low energy electron diffraction (LEED).

In chapter 6, local electrical measurements of the TiSi_2 Schottky barrier utilizing a c-AFM are given. In this work we have measured the local I-V characteristics of TiSi_2 nanoscale islands. We also have developed the new imaging method that enables one to identify the areas of different conductivities using a lock-in detection technique.

In chapter 7, we explore electrical properties of TiSi_2 islands are less than 5 nm in diameter, which is small enough to anticipate that the single electron charging effects will occur at room temperature. Our experiments were performed after forming TiSi_2 *in situ* on a $\text{Si}(111)7\times 7$ surface. The room temperature I-V results indicate Coulomb blockade and Coulomb staircases on these islands.

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Chapter 2. Theoretical Background

In this chapter we review some of the most basic ideas that will be necessary in understanding the results that are presented in the following chapters. In the first section we review the interface of a metal and a semiconductor and their electrical properties. In the following section, we review the physics of single electron tunneling (SET) and previous results of SET effects involving a metal-semiconductor system in particular.

2.1 Metal-Semiconductor Interface

In this study we are most interested in the metal-semiconductor interface and its electrical characteristics when their size is decreased to sub-micron or nanoscale. The metal semiconductor interface is one of two interfaces employed to obtain SET effects. The other interface is vacuum or ambient depending on the characterization tool that was used. Therefore it is necessary to have a firm understanding of this interface. We will review the formation of the metal-semiconductor interface (equilibrium), its behavior under bias (non-equilibrium or quasi-equilibrium) and deviations from standard theory when the size of the interface is decreased.

2.1.1 Formation of Schottky Barrier

It was more than a century ago when Braun first observed the asymmetric nature of electrical conduction that exists between a metal-contact to a semiconductor [1]. Then in 1931, the first step towards the understanding of the metal-semiconductor interface was taken by Schottky and his co-workers who showed there is a kind of potential barrier

at the contact. However, the exact nature of this interface is still not completely understood to this date.

When describing the formation of the Schottky barrier at a metal-semiconductor interface there are two extreme cases to be considered: the Schottky-Mott limit and the Bardeen limit. The main difference in these cases is the role of the surface states or the interface states.

2.1.1.a Schottky-Mott limit

The Schottky-Mott process is depicted in Fig. 2.1. We begin with a metal and a semiconductor, each neutral and separated from each other. The work function of the metal is assumed to be larger than that of the n-type semiconductor. It is also assumed that the surface of the semiconductor is free of any surface states, thus the bands are flat up to the surface. The nature of surface states will be discussed in the next section in more detail.

When a metal film forms an intimate contact with a semiconductor surface, the charge neutrality requires electrons transfer from the semiconductor to the metal in order to align the Fermi levels of the metal and semiconductor. As a result, the metal is charged negatively and the semiconductor obtains a positive charge. The negative charge on the metal is accumulated within the Thomas-Fermi screen length ($\sim 0.5\text{\AA}$) from the interface. Since the dopant density of the semiconductor is much less than the concentration of electrons in the metal, the uncompensated donors extends deeper into the semiconductor to compensate for the negative charges from the metal, thus forming a depletion region.

Therefore, the conduction and valence bands of the semiconductor bend upward and develop a barrier for electrons given by

$$\Phi_B = \Phi_M - \chi_S.$$

For a metal contact to a p-type semiconductor, we can apply similar analysis to obtain the barrier for hole conduction which is given by

$$\Phi_B = (E_g + \chi_S) - \Phi_M.$$

2.1.1.b Bardeen limit

Experimentally measured Schottky barriers do not typically follow the simple Schottky-Mott theory. In some instances, the SBH is essentially independent of the metal work function. In Bardeen's approach to Schottky barrier formation, the semiconductor is assumed to have surface states as shown in Fig. 2.2 (a). These surface states can be located either within the band gap or outside the band gap depending on the materials. Surface states that are located outside the bandgap do not affect band bending. Surface states within the bandgap are divided into two categories. A definition of the charge neutrality level (CNL) is necessary before this categorization can be done.

The CNL, Φ_o , is defined as the level in which the surface state band will have no charge when filled up to that level. In other words, if $\Phi_o > E_f$, then surface states charges are positive and vice versa. Hence, surface states below Φ_o are referred as donor-like states and those above Φ_o acceptor-like states. If the surface states have large density of states, $\Phi_o \sim E_f$ and the surface Fermi level (FL) is called 'pinned'. When FL pinning occurs, the SBH is essentially independent of the metal work function as shown in Fig. 2.2 (b).

2.1.1.c Intimate contact- MIGS and Defects states

Bardeen's model of the Schottky barrier as presented in the previous section utilizes interface states to explain SB formation. However, in many cases, UHV prepared metal-semiconductor interfaces are 'intimate' and have no insulating layer between metal and semiconductor. When intimate contact is formed, the metal and semiconductor are no longer isolated from each other as in the case with an insulating layer. Several factors should be considered in this case as follows:

- 1) change of the bonding structures of the metal and semiconductor.
- 2) abruptness of the interface.
- 3) reaction of the metal and semiconductor at the interface.
- 4) extension of the electron wavefunctions into the semiconductor: MIGS.

Thus, it is necessary to consider all of these effects in describing the electronic states of a metal-semiconductor interface. Today a detailed explanation of many interfaces has not been obtained. Jellium based model calculation [2] showed the existence of metal induced gap states (MIGS) in the band gap of the semiconductor. The SBH for materials systems considering MIGS were evaluated [3]. It was found that the SBH were less dependent on Φ_m for covalent semiconductors like Si and GaAs. The calculation showed that the density of MIGS was sufficiently high to cause FL pinning.

Spicer [4] proposed the 'Unified defect model' noting that imperfections such as steps and vacancies may act the same way as the MIGS to cause FL pinning. But the defect model may not have a significant influence when the metal contact size approaches the nanometer scale.

2.1.2 Current Transport Mechanism

As one method to investigate the Schottky barrier we consider current-voltage (I-V) measurements experiment. Regardless of the formation process of the Schottky barrier, we may be able to extract the information about the SBH from this measurement.

There are many carrier mechanisms involved in current transport at a metal-semiconductor interface. Some of the mechanisms are shown in Fig. 2. 3. The most probable process in practical macroscopic Schottky diodes is (a) transmission over the barrier, which is referred to as the thermionic emission. This is the standard model used widely in obtaining the SBH, and we also used this model for determination of the SBH of our TiSi_2 structures in this study. Other mechanisms such as tunneling through the barrier, recombination at the depletion region, and recombination at the neutral region are also shown.

2.1.2.a. Thermionic emission

We consider first thermionic emission. For a moderately doped semiconductor, this process contributes most significantly to the charge transportation. Upon biasing the interface, the Fermi levels in the metal and semiconductor will no longer be aligned and thermally excited electrons will go over the barrier from either side. The barrier height for electrons in the semiconductor varies according to the bias. For forward bias, the barrier for electrons is reduced thereby increasing the current from the semiconductor to the metal. In reverse bias, the barrier is increased and the current from the semiconductor to the metal decreases. For electrons in the metal, however, the barrier is not changed

significantly in either bias. The current flow from the metal to the semiconductor remains the same regardless of the polarity of the bias voltage.

The current flow mechanisms noted above were first suggested by Bethe [5] and further refined by Crowell and Sze [6]. This current is written as follows

$$I(V) = I_s e^{\frac{qV}{nkT}} \left[1 - e^{-\frac{qV}{kT}} \right], \quad (2.1)$$

where q is the electronic charge, k is the Boltzmann constant, T is the absolute temperature, V is the applied bias, and n is the ideality factor. In above equation, I_s is the saturation current, given by

$$I_s = A^* A T^2 \exp\left(-\frac{q\Phi_B}{kT}\right), \quad (2.2)$$

where A^* is the Richardson constant, A is the area of the diode, and Φ_B is the Schottky barrier height (SBH) of the junction. For $V > 3kT/q$, Eq. 2.1 can be rewritten as

$$I = I_s \left[e^{\frac{qV}{nkT}} - 1 \right] \quad (2.3)$$

and we will use this expression to determine the SBH and ideality factor for the structures studied here. The measured forward I-V curve is plotted on semi-logarithmic plot. The linear region is fit to obtain the slope and the y-intercept. The ideality factor and SBH are found from the slope of the linear region and the saturation current, respectively, i.e.

$$\frac{1}{n} = \frac{kT}{q} \frac{d(\ln I)}{dV}, \quad (2.4)$$

$$\Phi_B = \frac{kT}{q} \ln\left(\frac{A^* A T^2}{I_s}\right) \quad (2.5)$$

However, the validity of the above equation is based upon the assumption of a homogeneous interface with a uniform SBH.

2.1.2.b Tunneling (Field emission & Thermionic field emission)

The other important process in metal-semiconductor current transport is tunneling. Just like metal-vacuum tunneling, in a metal-semiconductor interface, electrons may tunnel through the Schottky barrier without reaching the top of the barrier when the barrier width is not thick. This problem can be solved using the WKB approximation [7]. A triangular barrier is most often considered to describe the potential barrier.

Tunneling of electrons through the Schottky barrier has been reviewed in detail by Padovani [8]. According to their findings, tunneling of electrons through the barrier can contribute to the current either by direct tunneling of electrons from the Fermi level of the semiconductor to the metal (field emission) or with the assistance of thermal energy such that electrons will be excited to higher energy and tunnel through less the triangular barrier (thermionic field emission). Field emission or direct tunneling is more likely to be observed when the semiconductor is heavily doped such that the Fermi level is above the conduction band minimum. Therefore, we will mainly concentrate on thermionic field emission here.

For field emission and thermionic field emission, the current is given by [9]

$$I = I_s e^{(V/E_0)} \left[1 - e^{-\frac{qV}{kT}} \right] \quad (2.6)$$

where $E_0 = E_{00} \coth(qE_{00}/kT)$ and E_{00} is given by

$$E_{00} = \frac{\hbar}{2} \left[\frac{N_D}{m^* \epsilon_S} \right]^{1/2} \quad (2.7)$$

where m^* is the effective mass of electrons in the semiconductor, ϵ_S is the permittivity, and N_D is the donor concentration. The ratio kT/qE_{00} is a measure of the relative importance of thermionic emission and tunneling. E_{00} is the diffusion potential of a Schottky barrier such that the transmission probability for an electron whose energy coincides with the bottom of the conduction band at the edge of the depletion region is equal to e^{-1} . We can expect field emission if $kT \ll qE_{00}$, thermionic-field emission if $kT \sim qE_{00}$, and thermionic emission if $kT \gg qE_{00}$, respectively. For silicon, the criterion of $kT \sim qE_{00}$, i.e. thermionic-field emission, corresponds $N_D \sim 10^{19} \text{ cm}^{-3}$. Therefore in our experiments with a moderate doping ($N_D \sim 10^{16} \text{ cm}^{-3}$), neither field emission nor thermionic field emission should make a significant contribution to the total current.

2.1.2.c Minority carriers (recombination & injection)

Electron-hole recombination normally takes place via localized states, and the most effective recombination centers are those with energies lying near the center of the forbidden gap. The theory of current due to such recombination centers in Schottky diodes is similar to that for p-n junctions, and the current is given as

$$I_r = I_{r0} \exp(qV/2kT)[1 - \exp(-qV/kT)] \quad (2.8)$$

where $J_{r0} = qn_i w / 2\tau_r$. Here n_i is the intrinsic electron concentration, proportional to $\exp(-qE_g/2kT)$, w is the thickness of the depletion region, and τ_r is the lifetime within the depletion region. Then the total current is sum of thermionic current and recombination current. The ratio of these two is proportional to

$$T^2\tau_r \exp[q(E_g + V - 2\Phi_B)/2kT]. \quad (2.9)$$

Thus, the recombination component is likely to be more important in high barriers, in materials with low lifetime, at low temperatures, and at low forward bias voltage.

In some cases holes are diffused into the neutral region and this effect is termed hole injection. This is likely to happen when the SBH is greater than half of the band gap causing the region of the semiconductor near metal to have a high density of holes. The hole current can be written as

$$J_h = \frac{qD_p p_0}{L} [\exp(qV/kT) - 1] \quad (2.10)$$

where $p_0 (=n_i^2/N_D)$ is the equilibrium concentration of holes at the edge of the depletion region, and D_p and L are the diffusion constant of holes in the bulk semiconductor and the thickness of the neutral region, respectively. The hole injection ratio is defined as

$$\gamma_h = \frac{J_h}{J_e + J_h} \sim \frac{J_h}{J_e} = \frac{qD_p n_i^2}{N_D L A^* T^2 \exp(-q\Phi_B/kT)}. \quad (2.11)$$

In the above expression, thermionic emission theory is assumed for the electron current. The injection ratio increases with Φ_B since J_e is reduced, and decreases with increasing N_D because of a decrease in p_0 and a consequent reduction of J_h . For a typical silicon diode ($\Phi_B = 0.8\text{eV}$, $N_D = 10^{16}\text{cm}^{-3}$, and $L \sim 5\mu\text{m}$), the ratio γ is $\sim 10^{-4}$, so that hole injection is negligible in practice.

However, for point-contact diodes an increased injection ratio was observed experimentally and theoretically [10, 11]. Clarke et al.[12] suggested that in the point contact diode the hole concentration decays as $1/r$, where r is the contact radius. The

smaller the contact, the more rapid is the decay of injected minority carriers. This corresponds to enhanced minority-carrier diffusion current density. For a diode with contact radius $r=0.2 \mu\text{m}$, a hole injection ratio as high as 0.95 was obtained through the calculation. This process may become more dominant as the size of the diode becomes smaller in our study.

2.1.3 Non-uniform SBH and ideality factor

Even in the same sample with the same processing, the measured SBH is not typically uniform from diode to diode. In fact, it has been suggested that it is more natural to imagine the SBH to be non-uniform over the interface and to consider the uniform SBH as a special case. Thus, the current-voltage relationship discussed in the earlier sections needs to be modified accordingly. Tung compiled several experimental and numerical results to support this argument [13]. A combination of patches of different SBH was employed to explain the I-V's that show a deviation from the standard thermionic emission theory.

Some of the mechanisms suggested that make the SBH deviate from the uniform value include defects [4], MIGS [14], and effective work function [15]. Another possible mechanism for non-uniform SBH's is due to local specifics of the interface structure [16]. For instance, the previous TEM studies demonstrated that TiSi_2 islands exhibit different cross-sections in the same sample [17]. These results support the idea of a non-uniform SBH.

2.2 Single Electron Tunneling

2.2.1 Introduction

When the size of the metallic clusters or islands becomes smaller as nanotechnology develops, these structures will be employed in regimes, where the classical theory no longer holds. Thus it is foreseeable that in the near future we will be faced with the challenge of controlling the quantum mechanical behavior of the nanoscale system. The physics of single electron tunneling (SET) is one manifestation of these important phenomena[18], [19].

The current flow through systems of tunnel junctions shows unusual behavior when the capacitance of a junction is small enough that the electrostatic charging energy is greater than the thermal energy of the charge carriers. In this case, the discreteness of the electronic charge will play a role in the conduction properties of the system. These phenomena are referred to as SET effects.

The basic conditions for SET effects to occur in a system of small tunnel junctions are as follows. The first condition requires that the tunnel barriers have tunneling resistances R_T that exceed the resistance quantum R_K , i.e.,

$$R_T \gg R_K, \quad R_K = h/e^2.$$

The tunneling resistance is a phenomenological quantity that is related to the tunneling rate through the barrier and the voltage difference V : $\Gamma = V/eR_T$. The tunneling resistance can be expressed in terms of the microscopic quantity T , which is the barrier transmission coefficient at the Fermi energy:

$$R_T^{-1} = 4\pi NTR_K^{-1}, \quad (2.12)$$

where N is the number of independent electron channels through the barrier. This condition is obtained by requiring that for an excess charge on the island the energy uncertainty associated with the lifetime due to tunneling $\tau_r = R_T C$ is much smaller than the charging energy $E_C = e^2/2C$. This condition ensures that the wave function of an electron on an island is localized there. It is believed that if the tunneling resistances are smaller than R_K , the charging effects will not be observed because of the delocalized states in which electrons flow through an island without charging it.

The second condition requires that the islands must be small enough such that the charging energy, E_C , associated with adding an electron to an island, far exceeds the available energy of thermal fluctuations, i.e.,

$$E_C \gg kT.$$

If the energy required for adding an electron to the island exceeds the available energy of thermal fluctuations, then charge transport will be suppressed. When these two conditions are met, charge transport through the system will be governed by the Coulomb charging energy.

One of the simplest systems to detect SET effects is made up of two tunnel junctions coupled in series, as shown in Fig 2. 4. This system consists of a small metallic island connected to two metallic contacts with tunnel junctions. The metallic island is completely surrounded by an insulating material. If a fixed voltage difference is applied between the two contacts, the only way for current to flow is by electrons tunneling through the island. In the process of tunneling on-to and off-of the island, an electron necessarily makes the charge of the island change by an amount equal to the charge of an

electron. If the requirements listed above are met, current flow through the island will exhibit SET effects.

Depending on the nature of the double barrier junction, SET effects will be manifested in one of several different features in the $I(V)$ characteristic. For symmetric junctions ($R_C=R_C$), there will be a suppression of the tunnel current for some finite voltage about zero bias. This is referred to as the Coulomb blockade. For strongly asymmetric junctions, ($R \gg R$ and $C \gg C$ or vice versa), periodic oscillation of the tunnel current as a function of the bias voltage will also be observed. Each period corresponds to the addition/removal of an electron to/from the middle electrode. This is referred to as the Coulomb staircase. A simplified perspective of the Coulomb blockade and staircase is depicted in Fig. 2.5.

2.2.2 Historical review

The first experimental observations of Coulomb blockade were made in the late 1960's in systems consisting of small ($\sim 10\text{nm}$) metallic particles embedded in an oxide layer between two planar metal electrodes[20, 21], as shown in Fig. 2. 6. These systems could be understood as many double-barrier junctions in parallel, and the experiments thus measured ensemble effects. These experiments were all performed at liquid-He temperatures in order to suppress thermal fluctuations.

Advances in lithographic techniques have made it possible to engineer very small, well-defined double-barrier junctions with capacitances in the 10^{-15} F range [22], [23], [24]. In this size range, SET effects can be observed at millikelvin temperatures. These systems typically consist of 10 to 100 well-defined double-barrier junctions in series.

Effects due to the time correlation of the tunnel events were observed in these structures in addition to the Coulomb blockade and Coulomb staircase. The time correlation of tunnel events was predicted to occur in arrays of double barrier junctions, but not in a single double-barrier junction [19].

With the development of the STM, it has been possible to study SET effects in systems with a single double-barrier junction [25-30]. Most of the systems studied with the STM are actually very similar to those used in the first observations of SET effects. The main difference is that one of the planar electrodes is replaced with an STM tip, as shown in Fig. 2.7. One tunnel junction is between the STM tip and the particle, and the other is between the particle and a conducting substrate. The metallic particles are typically formed by the aggregation of atoms evaporated onto thin oxide or organic layers.

The STM has several advantages in the study of SET effects. Topographic data indicating the size and location of the particles can be obtained simultaneously with the spectroscopic data. This allows the spatial and conduction properties of the system to be characterized at the same time. The junction formed by the tip and the particle is adjustable, which allows the conduction properties to be investigated as the tip-particle junction is varied. Using this configuration, junctions with capacitances on the order of 10^{-18} F to 10^{-19} F can be fabricated. These junctions have capacitances that are much smaller than those produced by lithographic techniques. Because of this, the threshold temperature for observing SET effects is much higher. Most STM experiments on SET can be performed at liquid He temperatures, as opposed to the millikelvin temperatures

needed for microfabricated structures. Recently, it has even been possible to fabricate structures small enough to observe SET effects at room temperature [30-33].

2.2.3 Semiclassical Theory of SET

In this section, a semiclassical theory for SET effects in a double-barrier tunnel junction is presented. In the theoretical model, each junction is represented by a parallel combination of capacitance and resistance, and has a tunneling rate associated with it. These quantities are denoted by C_i , R_i , and Γ_i , respectively [25, 28]. For simplicity, the R_i is assumed to be voltage independent. The tunneling rate across a junction can be calculated from a golden-rule assumption to be

$$\Gamma_i^\pm(V, q) = -\frac{E_i^\pm(V, q)}{e^2 R_i [1 - \exp(E_i^\pm / kT)]} \quad (2.13)$$

Where E_i is the change in electrostatic energy of the entire system when an electron tunnels across the i^{th} junction. The direction of the electron tunneling is given by the + or – sign. Tunneling rates in the opposite direction can be calculated by making use of the fact that

$$\Gamma_i^+(V, q) = \Gamma_i^-(-V, -q). \quad (2.14)$$

The $E_i(V, q)$ are functions of both the bias voltage, and the quantized charge on the island. The E_i can be calculated from electrostatic considerations due to the change in energy as charges move on and off the island.

$$E_1^\pm = \left(\frac{Q^2}{2C_\Sigma} - \frac{(Q \pm e)^2}{2C_\Sigma} \right) \pm \frac{eC_2}{C_\Sigma} V \quad (2.15)$$

$$E_2^\pm = \left(\frac{Q^2}{2C_\Sigma} - \frac{(Q \pm e)^2}{2C_\Sigma} \right) \pm \frac{eC_1}{C_\Sigma} V \quad (2.16)$$

Q is the excess charge on the center electrode before the electron tunnels, C_i is the capacitance of the j^{th} electrode, and $C_\Sigma = (C_1 + C_2)$. The first term is just the change in the charging energy of the island as it gains or loses an electron. The second term is the potential drop across the barrier times the electron charge. If we let $Q = (ne - Q_0)$, these equations can be written as

$$E_1^\pm = \frac{e}{C_\Sigma} \left(\frac{e}{2} \pm (ne - Q_0) \pm C_2 V \right) \quad (2.17)$$

$$E_2^\pm = \frac{e}{C_\Sigma} \left(\frac{e}{2} \pm (ne - Q_0) \mp C_1 V \right) \quad (2.18)$$

Here, n is the integer nearest Q/e and $|Q_0| \leq e/2$. Q_0 is referred to as the fractional charge. Q_0 is a continuous variable, and it accounts for the dependence of the double-barrier junction on external charges Q_{ext} , and on the contact potential of the electrode materials[19, 28, 30]. The fractional charge can be written as

$$Q_0 = \frac{1}{e} [C_1(\Delta\phi_1) - C_2(\Delta\phi_2)] + \gamma Q_{\text{ext}} \quad (2.19)$$

where γ is a constant and $\Delta\phi_1$ and $\Delta\phi_2$ are the contact potentials of the two junctions. If one knows the average charge distribution on the island, $\sigma(V, q)$ then the total current through the array is the net flow through any one junction.

$$I(V) = e \sum_{n=-\infty}^{\infty} \sigma(n) [\Gamma_2^+(n) - \Gamma_2^-(n)] = e \sum_{n=-\infty}^{\infty} \sigma(n) [\Gamma_1^-(n) - \Gamma_1^+(n)] \quad (2.20)$$

In order to use Eq. 2.20 to calculate $I(V)$, the $\sigma(n)$ must be determined. This is accomplished by making use of the fact that in a steady state, the probability of making a

transition between adjacent charge distributions is zero. This requirement can be expressed as

$$\sigma(n)[\Gamma_1^+(n) + \Gamma_2^+(n)] = \sigma(n+1)[\Gamma_1^-(n+1) + \Gamma_2^-(n+1)] \quad (2.21)$$

Subject to the constraint

$$\sum_{n=-\infty}^{\infty} \sigma(n) = 1. \quad (2.22)$$

With these equations, a numerical solution for the I(V) characteristics of an arbitrary tunnel junction was generated [34] and used to fit the experimental results.

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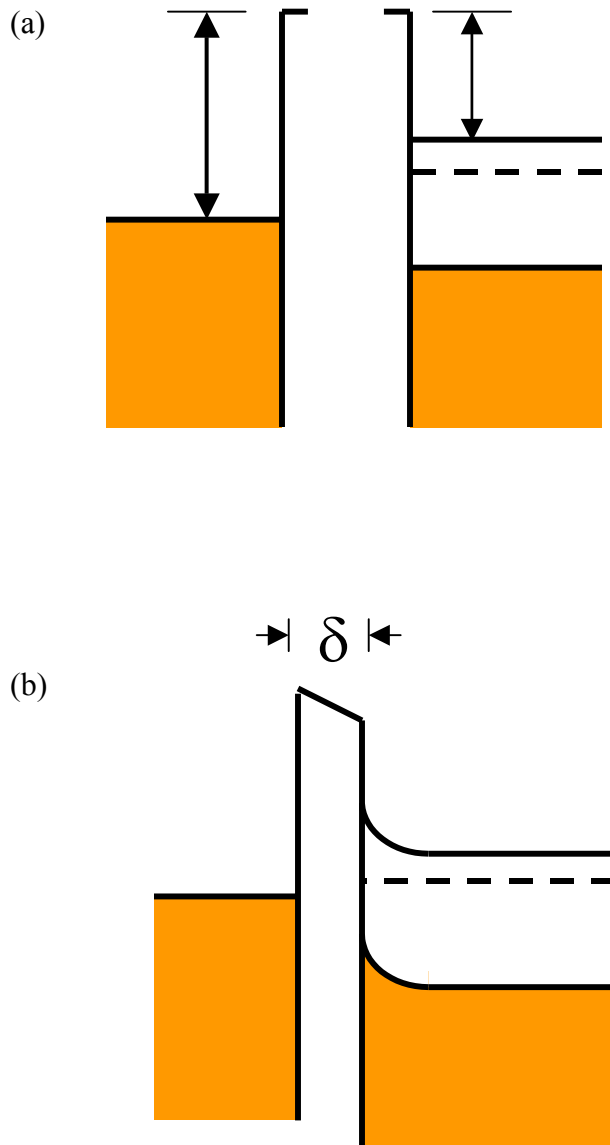


Fig. 2.1 Schottky barrier formation in the Schottky-Mott model (a) the metal and semiconductor are isolated from each other, (b) in equilibrium and approaching, (c) intimate contact.

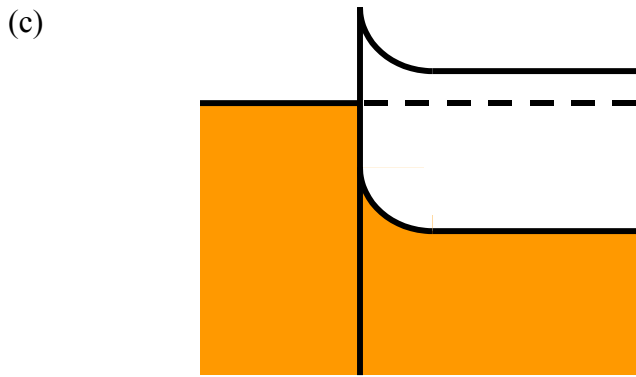


Fig. 2.1 (continued)

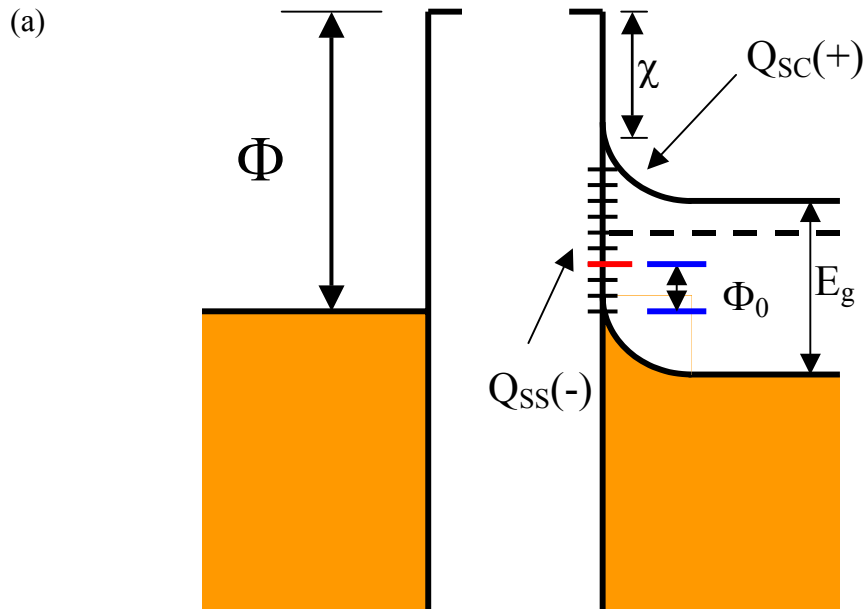


Fig. 2.2 (a) Schottky barrier formation in Bardeen's model; the metal and semiconductor are isolated. Q_{ss} is the charge due to surface states. Conduction and valence bands are bent before contact is made.

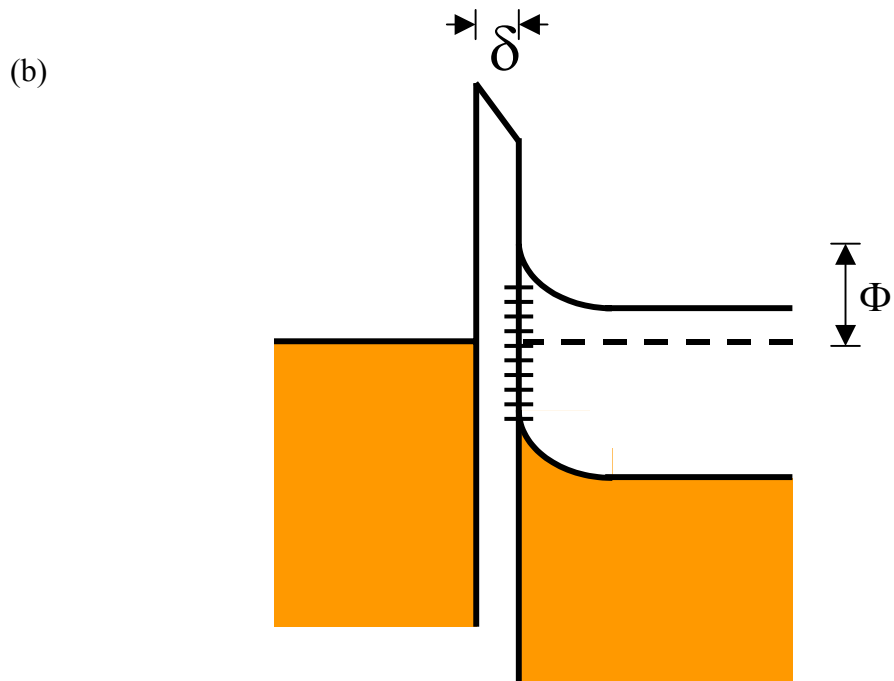


Fig. 2.2 (b) Schottky barrier formation in Bardeen's model; the metal and semiconductor are in equilibrium.

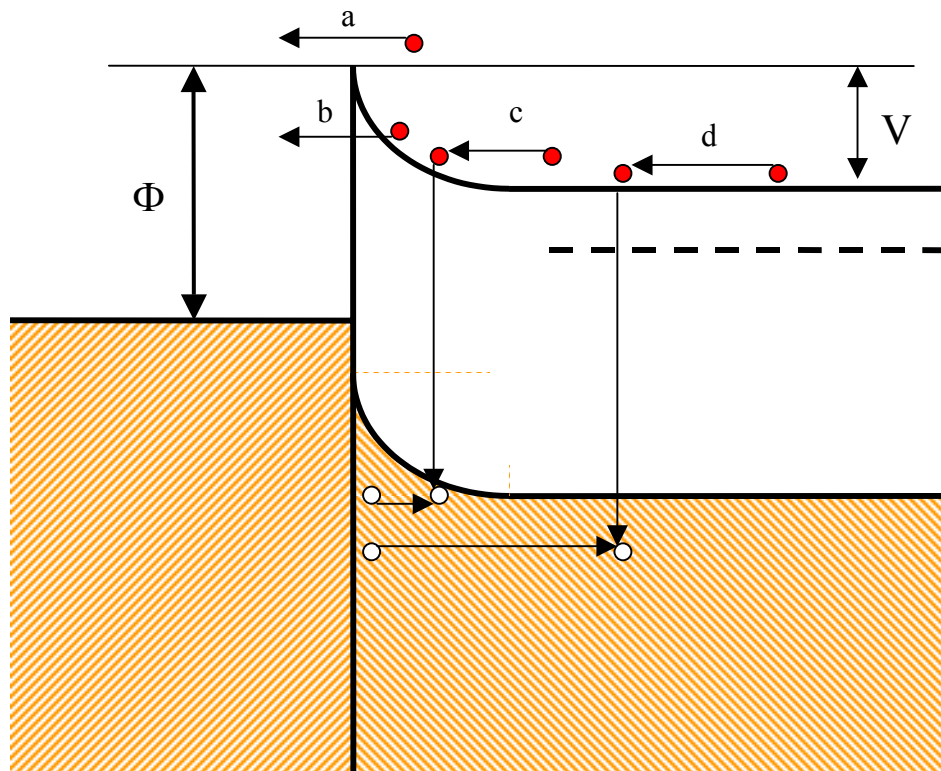


Fig. 2.3 Transport mechanisms across the Schottky barrier; (a) thermionic emission, (b) tunneling, (c) recombination in the depletion region and (d) hole injection into the neutral region.

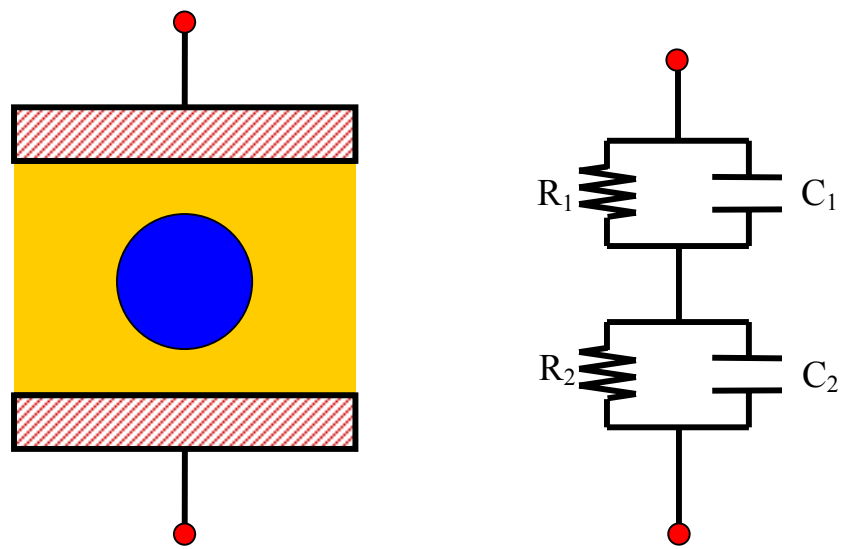


Fig. 2.4 Double tunnel junction and its model. Each tunnel barrier is depicted as a combination of resistance and capacitance.

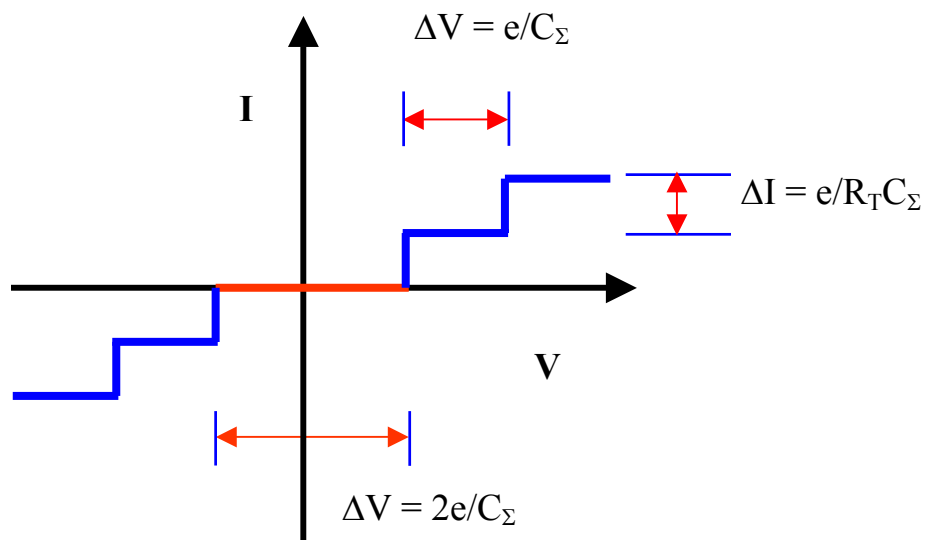


Fig. 2.5 Coulomb blockade and staircase in double tunnel junction system.

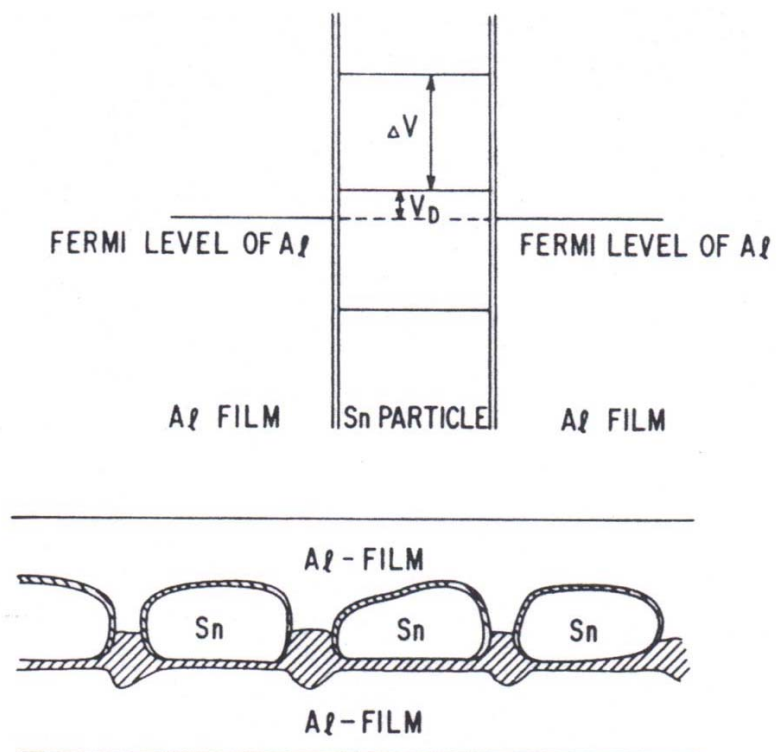


Fig. 2.6 Model and level scheme of Sn particle in a tunnel junction. (from Giaever [20])

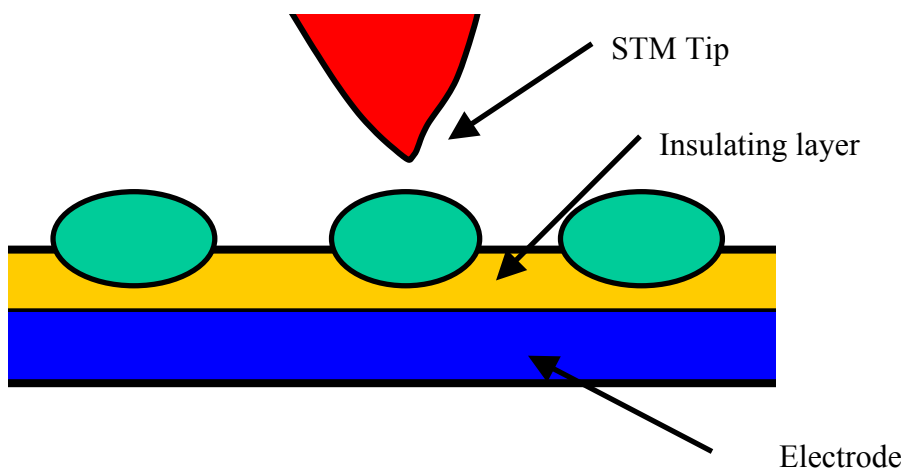


Fig. 2.7 Experimental configuration of a double barrier junction. A STM tip replaces one of the electrodes.

Chapter 3. Scanning Tunneling Microscopy and Spectroscopy

The experimental techniques for nanoscale characterization need both direct imaging and characterization at the nm length scale. For high-resolution imaging at the nanoscale, techniques include scanning electron microscopy (SEM), transmission electron microscopy (TEM), scanning tunneling microscopy (STM) and atomic force microscopy (AFM). In support of these, surface analytical tools such as x-ray photoelectron spectroscopy (XPS), ultraviolet photoelectron spectroscopy (UPS), and Auger electron spectroscopy can provide spatially averaged spectroscopic information. Among these techniques, only STM and STM-based spectroscopic techniques can provide both imaging and spectroscopic characterization capabilities.

STM was invented in early 1980's by Binnig and Rohrer and is a powerful tool to image the real space of surfaces [1, 2]. STM and STM-based techniques are widely used in the areas of physics, chemistry, material science, biology, etc. Since its invention, STM has evolved from a surface imaging tool into a very powerful nanometer scale surface characterization and modification tool [3, 4].

In this chapter, we will review scanning tunneling microscopy in terms of electrical characterization. First, the scanning tunneling microscope is reviewed. Its operational principle, instrumentation, and scanning tunneling spectroscopy (STS) will be briefly described. In STS, it is possible to identify local electrical properties with nanometer precision.

3.1 Operation principles of STM

STM images are obtained by probing a tip over the surface of a sample as shown in Fig. 3.1. When a sharp metal tip is brought very close to a sample, the wave functions of the tip and sample overlap and electrons will tunnel through the potential barrier. A net current can be measured when a bias voltage is applied. The vacuum gap between two conducting electrodes, tip and sample in this case, is considered as the tunnelling barrier. We can model this problem as a one dimensional rectangular barrier, and the solution for the Schrödinger equation has the form

$$\psi \propto e^{-\kappa z}. \quad (3.1)$$

Therefore, for small voltages, the resulting tunneling current I decays exponentially with barrier width as

$$I \propto e^{-2\kappa z}, \quad (3.2)$$

where z is the gap distance between tip and sample and κ is termed the decay constant, which is related to the local work function ϕ of tip and sample as

$$\kappa = \hbar^{-1} \sqrt{2m\phi}, \quad (3.3)$$

where m is the mass of electron.

For two electrodes with an applied voltage V as shown in Fig. 3.2(c), only the states within eV of the Fermi energy can contribute to the tunneling current. According to the exclusion principle, the process involves electrons tunneling from filled states into empty states. Therefore, for energies above the Fermi level of the left electrode, there are no filled electron states on either side. For energy below the Fermi level of the right electrode, there are no empty states in either side. In fact the transmission probability is

highest when the electron energy is at the Fermi level. Therefore we are mapping the surface contour of local Fermi level.

Since the work function for most materials is around 4-5 eV, then κ is $\sim 1 \text{ \AA}^{-1}$. This implies that for a 0.1 nm change in the tip sample separation, the current will change by an order of magnitude. Furthermore, if the tip shape near the apex is a cone shape, on which one atom protrudes, the tunneling current through that atom's cross section is $\sim 90 \%$ of the total measured tunneling current. Typically, on atomically flat surfaces, STM has a vertical resolution of 0.01 nm and a lateral resolution of 0.1 nm.

3.2 Instrumentation

In STM design, one needs to consider the critical aspects of the technique, particularly, vibration isolation, tip, scanner, and electronics. We have incorporated a commercial STM head (Park Scientific Instrument VP) into our existing UHV system. In this section we will discuss general issues regarding each component and any modification that we made to accommodate the STM into our system.

3.2.1 Microscope

The UHV STM used in this work is shown in Fig. 3.3. The sample stage has been modified to accommodate a custom sample holder chuck. Piezoelectric inertial motors are used for coarse sample approach with x and z motion. Since the design was for motion of the sample in x-z direction, this represented the most significant problem to solve in improving the resolution of the microscope. The sample stage has a heavier mass compared to that of the tip holder. Although the sample stage is held with magnet it is subject to small vibrations. If we consider the microscope as a simple harmonic oscillator,

the heavier mass sample holder gives a lower resonant frequency. This inherent low frequency noise can couple with the real signal to give a mixed signal that is sometimes very hard to delineate.

To isolate the mechanical and acoustic noise from the system, a two-stage suspension system with a double spring and magnetic eddy current damping is used. In addition, the whole UHV system rests on a pneumatic air suspension table for vibration isolation from the floor. Typically, building vibrations result in low frequency noise (10 ~30 Hz), and it is advised to check the inherent mechanical noise of the site for STM using a seismographic spectrum analyzer.

3.2.2 Scanner

In virtually all scanning probe microscopy, a piezoelectric scanner is used as a fine positioning stage to move the probe over the sample (or the sample under the probe). A piezoelectric scanner is usually made of a lead zinc titanate (PZT) ceramic. The Curie temperature for PZT materials is ~ 150 °C, and care should be taken not to exceed this temperature when baking the system. There are two types of scanners popularly used in STM. Earlier designs used a tripod shaped scanner while tube scanners are becoming more common for current systems. In this work, a tube scanner was used which has a higher piezoelectric constant (~ 100 Å/V) and higher resonance frequency compared to a tripod scanner. The tube scanner has operation ranges of ~ 10 μm in the x-y directions and ~ 3 μm in the z direction. The actual resolution of an STM is determined by dividing the maximum scan range by the number of steps in the digital-to-analog converter (DAC). We used a 20 bit DAC for x and y scan and 16 bit DAC for z scan in this work which

allows resolution of 2×10^{-5} $\mu\text{m}/\text{step}$ in the x-y direction and 3×10^{-4} $\mu\text{m}/\text{step}$ in the z direction.

Although piezoelectric scanners have many desirable properties for STM applications, there are also some drawbacks; 1) nonlinearities in the piezoelectric relation, 2) hysteresis, and 3) cross coupling. Nonlinearities are inherent in all piezoelectric materials. In the first order approximation, the strain in a piezoelectric scanner is expected to vary linearly with applied voltage. In practice, the piezoelectric displacements show deviation from the simple linear relationship and are often represented as an S-shaped curve. In addition, there is some degree of hysteresis in the piezoelectric ceramic. Cross coupling is termed as the tendency of the x or y scanner movement to have a spurious z component. The x-y motion of the scanner tube is produced when one side contracts and the other side expands. As a result, the scanner tube scans in an arc and not in a plane.

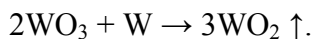
Effects of the above behaviors can be quite large and calibration procedures must be developed to account for the effects. Calibration is performed using a standard height sample and a standard lateral patterned sample as well as known atomically clean surfaces. In our system, the scanner was calibrated to second order assuming a parabolic displacement response to the applied field.

3.2.3 Tip

To achieve a consistent tip interaction with the materials of interest, it is desirable to have a high density of states near E_p . For example, d-band metals such as W, Pt, and Ir are commonly employed. In this work electrochemically etched W tips were used. There

are two electrochemical etching methods for producing sharp tips: DC bias etching and AC bias etching. Generally, the DC bias method yield tips more slowly and in this work an AC bias etching was used with a 2M KOH aqueous solution and a 15~20V AC bias.

After the etching process a residual oxide and contaminants from the etching solution remain on the tip surface. In order to remove the oxide as well as residual contaminants, tip annealing is usually performed. The usual oxide formed on a tungsten tip is WO_3 which is stable up to 725 °C [5]. Above 725 °C the WO_3 phase begins to decompose to solid W and solid WO_2 , which then sublimates to the vapor phase. The tip annealing process utilizes this thermal decomposition of WO_3 , and the reaction is



A clean tungsten surface is exposed when the tip is heated to 800 °C. In the process the tip must be heated carefully since excessive heat may blunt the tip. In our system electron bombardment of tip apex is employed. High current (~5A), flows through the filament for hot electron emission. The tip is placed very close to the filament (2~3 mm), and a high field between the tip (+) and the filament (-) attracts electrons toward the tip apex that are emitted from the hot filament. The chamber pressure is kept lower than 2×10^{-9} Torr.

Our STM can store 5 tips at a time. However tips can be degraded quickly during operation or the initial tip quality may not be sufficient for high resolution. Also, tips undergo irreversible shape change and these tips also need to be replaced. Furthermore, the quality of the tip is not known until the actual operation, and it could be costly to open up the chamber just to replace the bad tips. Therefore, we have designed a tip

exchanger that allows tip transfer using the load-lock chamber. The tip exchanger is shown in Fig. 3.4. It uses magnet to hold the tip cassette and is transferred to the STM by the transferring fork of the VP. This exchanger eliminates unnecessary bake outs of the system that could lead to a week of dead time. The system has gone without bake-out for more than a year when there was no need for maintenance.

3.2.4 Sample

The sample as well as the tip is also an important part of the tunnel junction. For STM, we need to consider the following properties of the sample: conductivity, density of states, and surface roughness. A sample with a large resistivity results in a decreased bias voltage across the tunnel junction. Because the equivalent resistance of a tunnel junction is estimated to be of the order of $\sim 1\text{G}\Omega$, it is preferred that the sample has a resistance of less than $\sim 100\text{M}\Omega$.

A sample should have available DOS to accommodate the tunneled electrons or to be able to provide electrons for tunneling. Because a bias voltage can alter the electric potential of the electrodes, this condition is often related to the band gap. A sample with a wider band gap may require a higher bias voltage to provide available DOS or tunnel electrons.

Surface roughness of the sample is an important factor for optimization of the feedback control. For a very smooth surface and a high gain setting, an oscillation in the feedback may occur leading to periodic tip crashing. In contrast, a very rough surface and a low gain setting also tends to crash the tip due to the slow response. Optimum values of feedback gain and scan rate are needed for the best image results [3].

3.3 Scanning Tunneling Spectroscopy

Generally we can interpret STM images as surface topography if the feature size is larger than the nanometer scale. But as the resolution of the STM approaches atomic scale, it is not necessarily correct to term the image as a topograph. The most reasonable definition of the STM image of a metallic surface would be that it is a contour of the surface Fermi level, since tunneling involves mostly electrons near the surface Fermi level.

The ability to adjust the bias voltage between the tip and sample enables us to probe local electronic properties of the surface. The tunneling current between tip and sample can be written by Fermi's golden rule as follows:

$$I(V) = \frac{2\pi e}{\hbar} \sum_{t,s} (f(E_s)[1 - f(E_t - eV)] - f(E_t - eV)[1 - f(E_s)]) |M_{t,s}|^2 \delta(E_t - E_s). \quad (3.4)$$

In this equation, V is the applied voltage to the sample, $f(E)$ is the Fermi-Dirac distribution function, E_t and E_s are the energies of the tip and sample relative to the Fermi level of each surface, and $M_{t,s}$ is the matrix element between the state ψ_s of the sample and the ψ_t of the tip in the absence of tunneling as given by Bardeen's model,

$$M = \frac{\hbar}{2m} \int (\psi_t^* \nabla \psi_s - \psi_s^* \nabla \psi_t) \cdot d\vec{S} \quad (3.5)$$

where the integral is over any surface lying entirely within the barrier region.

Under the assumption that (1) the tip has uniform density of states, (2) only the s-wave tip wave function is important, (3) the unperturbed wave functions of the tip and sample can be used when the tip-sample interaction is weak, and (4) the bias voltage is

low (<10 mV), Tersoff and Hamann predicted that the tunneling current is proportional to the local density of states (LDOS) of the sample [6].

The low bias approximation is often violated since many STS experiments are conducted at more than 1 V. Using the WKB approximation, the tunneling current can be expressed as

$$I = \int_{-\infty}^{\infty} [f(-eV + E) - f(E)] \rho_s(r, E) \rho_t(r, -eV + E) T(E, eV, z) dE \quad (3.6)$$

where $\rho_s(r, E)$ and $\rho_t(r, -eV + E)$ are the density of states (DOS) of the sample and tip at location r and energy E measured with respect to their individual Fermi levels. For negative sample bias, $eV < 0$, and $eV > 0$ for positive bias. The transmission probability function $T(E, eV, z)$ for electrons with energy E , applied bias voltage V , and tip to sample distance z is given in the WKB approximation as

$$T(E, eV, z) = \exp \left[-\frac{2z\sqrt{2m}}{\hbar} \sqrt{\frac{\phi_t + \phi_s}{2} + \frac{eV}{2} - E} \right], \quad (3.7)$$

where ϕ_t and ϕ_s are the work functions of tip and sample, respectively. $T(E, eV, z)$ will be a function of position r of the sample and tip when ϕ_t and ϕ_s have local variation. In the limit of low surface temperature ($k_B T \ll eV$), the tunneling current is then,

$$I = \int_0^{eV} \rho_s(r, E) \rho_t(r, eV + E) T(E, eV, z) dE. \quad (3.8)$$

If $eV < 0$ (negative sample bias), the transmission probability function is largest for $E=0$ corresponding to electrons at the Fermi level of the sample, and if $eV > 0$ (positive sample bias), the transmission probability function is largest for $E=eV$ corresponding to electrons

at the Fermi level of the tip. Therefore, the tunneling probability is always largest for electrons at the Fermi level of whichever electrode is negatively biased.

Fig. 3. 4 shows an energy level diagram illustrating the effect of the bias voltage polarity. If the tip and sample are close to each other, the Fermi levels of the tip and sample will be in the equilibrium with no bias. At a negative sample bias, the energy level of the sample will shift upward. In this case, electrons will tunnel from the occupied states of the sample into the unoccupied states of the tip. At a positive sample bias, the energy level of the tip will shift upward. In this case the electrons will tunnel from the occupied states of the tip into the unoccupied states of the sample. Therefore, the STM tip follows the contour of occupied states of the sample at negative sample bias, while it follows the contour of unoccupied states of the sample at positive sample bias.

Examples of application of the voltage-dependent imaging include the Si(111)7x7 surface [7], the Si(111)2x1 surface [8], and the GaAs(110) surface [9]. Fig. 3. 5 shows images obtained using our system with different biases on the silicon(111)7x7 surface. We can observe a clear dependence of the bias voltage from the images. The images demonstrate that different sites contribute to the tunneling thereby enabling LDOS identification of specific structures.

Tunneling spectroscopy provides information complementary to the information obtained in conventional topographic imaging [10]. By measuring the detailed dependence of the tunneling current on the applied voltage, it is possible to work backwards through the tunneling equations and to extract a measure of the electronic

density of states of the sample. By knowing both the energies and the spatial locations of the electronic states, it is often possible to make direct comparisons with theory.

Tunneling spectroscopy can be accomplished in a number of ways. The common goal of all tunneling spectroscopy experiments is to measure how the tunneling current depends on the applied voltage. The experimental implementation of tunneling spectroscopy can vary depending on the energy range accessed, the amount of spectroscopic detail required, and whether or not high spatial resolution is simultaneously required.

Most tunneling spectroscopy investigations today are made under conditions of constant separation, which is accomplished by momentarily interrupting the feedback controller and then ramping the applied voltage over the desired interval while simultaneously measuring the tunneling current. If no spatial resolution is required, the method is straightforward [11].

Analysis of tunneling spectroscopy is complicated by two facts. Firstly, the electronic density of states of the tip is usually unknown. Secondly, the voltage dependence of the tunneling probability is usually not known. The first issue is typically addressed by making comparisons between different locations on the same surface and by ensuring that all results are reproducible using different tips and different samples. Even though the electronic structure of the tips is unknown, it is at least constant, independent of spatial location. Thus, in tunneling spectra obtained at different locations on a surface with the same tip, the tip electronic structure contributes a constant background, but spatially dependent variations in the electronic structure can usually be determined free of

tip effects. The second complication can also be addressed in several ways, depending on the details of the situation. In some cases, the effects of the voltage dependence of the tunneling probability can often be minimized by presenting the data as plots of $(dI/dV)/(I/V)$ vs. V (or equivalently, $d(\log I)/d(\log V)$ vs. V). In the WKB approximation, this is equivalent to:

$$\frac{dI/dV}{I/V} = \frac{\rho_s(eV)\rho_t(0) + \int_0^{eV} \frac{\rho_s(E)\rho_t(-eV+E)}{T(eV,eV)} \frac{dT(E,eV)}{dV} dE}{\frac{1}{eV} \int_0^{eV} \rho_s(E)\rho_t(-eV+E) \frac{T(E,eV)}{T(eV,eV)} dE}. \quad (3.9)$$

Feenstra et al. [11] have argued that since $T(eV, eV)$ and $T(E, eV)$ appear as ratios in the second term in the numerator and denominator, their dependences on separation and applied voltage tend to cancel. Thus, the normalization reduces the data to a form like

$$\frac{dI/dV}{I/V} = \frac{d(\log I)}{d(\log V)} = \frac{\rho_s(eV)\rho_t(0) + A(V)}{B(V)}, \quad (3.10)$$

which by definition is equal to unity at $V=0$. Assuming that $A(V)$ and $B(V)$ vary slowly with voltage, this effectively normalizes that data. Unfortunately, for semiconductors this normalization may not be valid because both $A(V)$ and $B(V)$ tend to vary rapidly with voltage, particularly at the band edges. In addition, the numerator in Eq. 3.9 vanishes at the band edges, making the normalized data very distorted near the band edges. Due to the shape of the tunneling barrier, for voltages greater than ~ 0.5 V the tunneling electrons will typically arise from a relatively wide band ~ 0.3 eV wide below E_F . As a result, the tunneling transmission probability cannot vary rapidly with voltage changes of less than a few tenths of a volt. For many studies directed at understanding the density of states near the band edges then, the voltage dependence of the tunneling barrier over this narrow

voltage range can simply be ignored, and plots of I vs. V , dI/dV vs. V , or $d(\log I)$ vs. V are presented instead.

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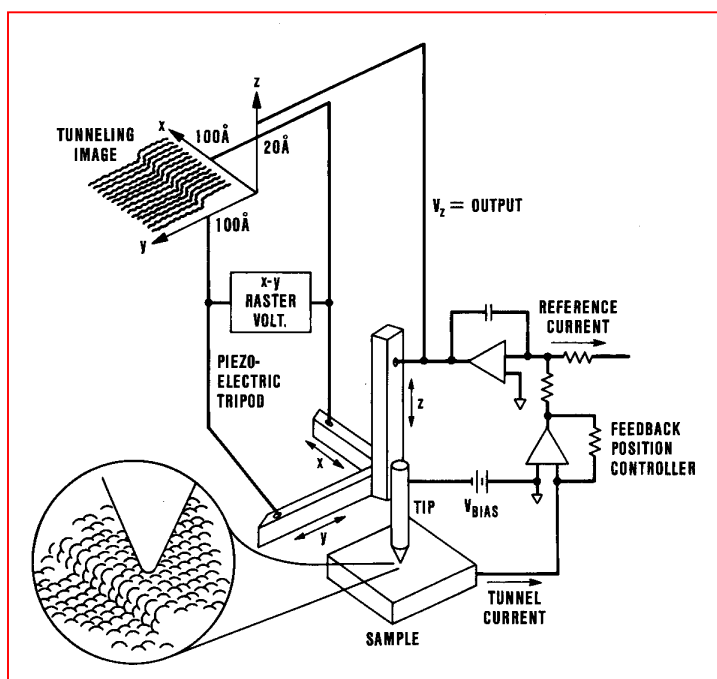


Fig. 3.1 Simplified view of operation principle of STM.

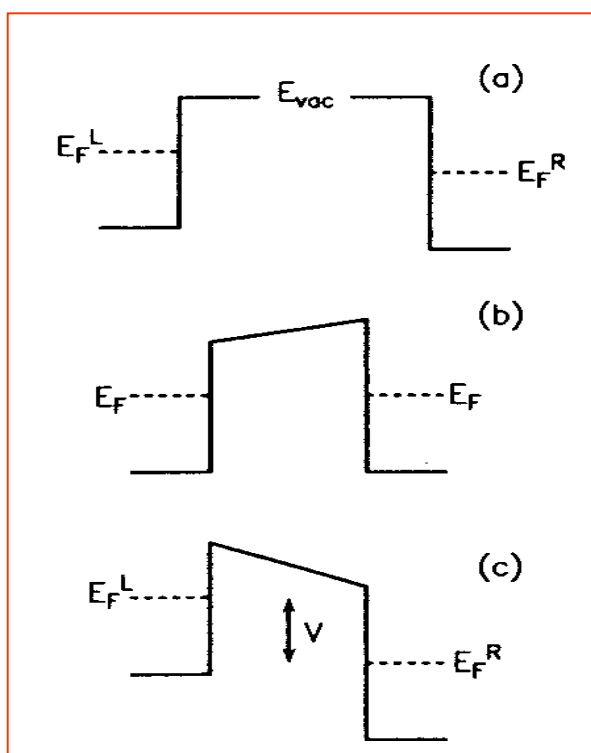


Fig. 3.2 Schematic of the potential barrier for tip and sample in an STM: (a) before equilibrium, (b) in equilibrium with no bias voltage, (c) with an applied bias voltage V . The left electrode is the tip and the right electrode is the sample.

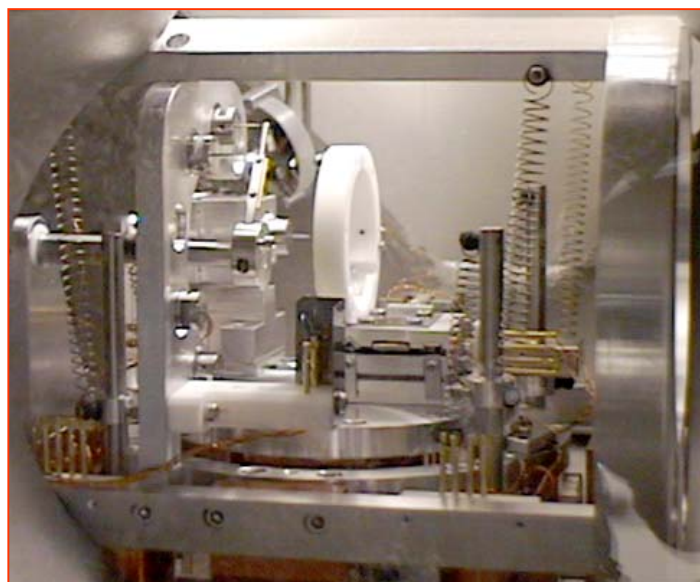


Fig. 3.3 Photograph of the STM (Park Scientific, VP) employed in our experiments. The large white circle is the ceramic that accepts the sample holder.

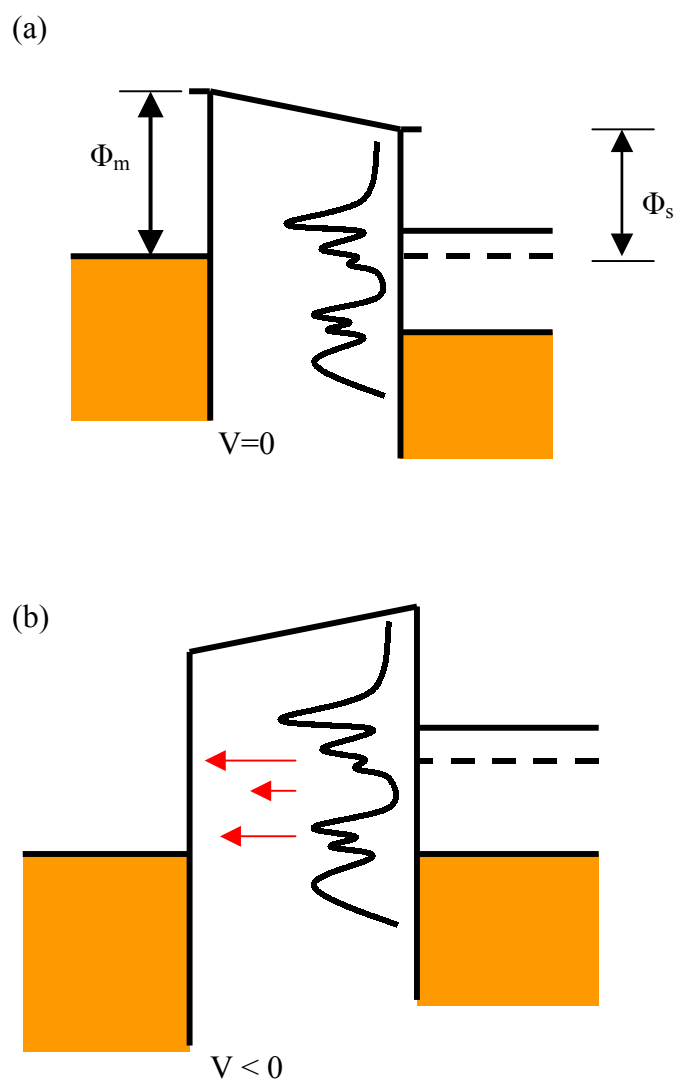


Fig. 3.4 Energy level diagrams of tip and sample: (a) tip and sample are in equilibrium with no bias, (b) sample is biased negatively, (c) sample is biased positively.

(c)

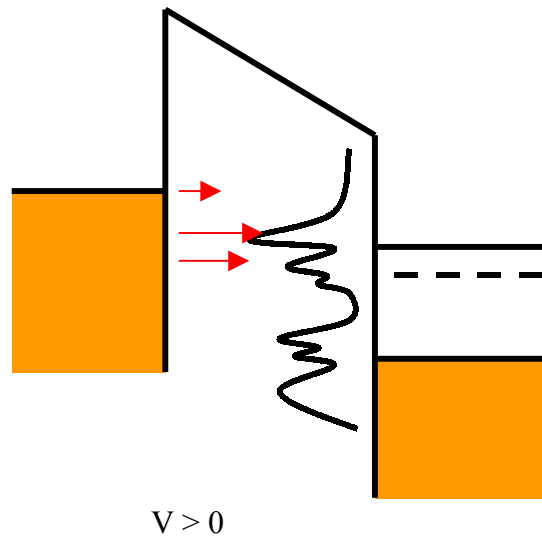


Fig. 3.4 (continued)

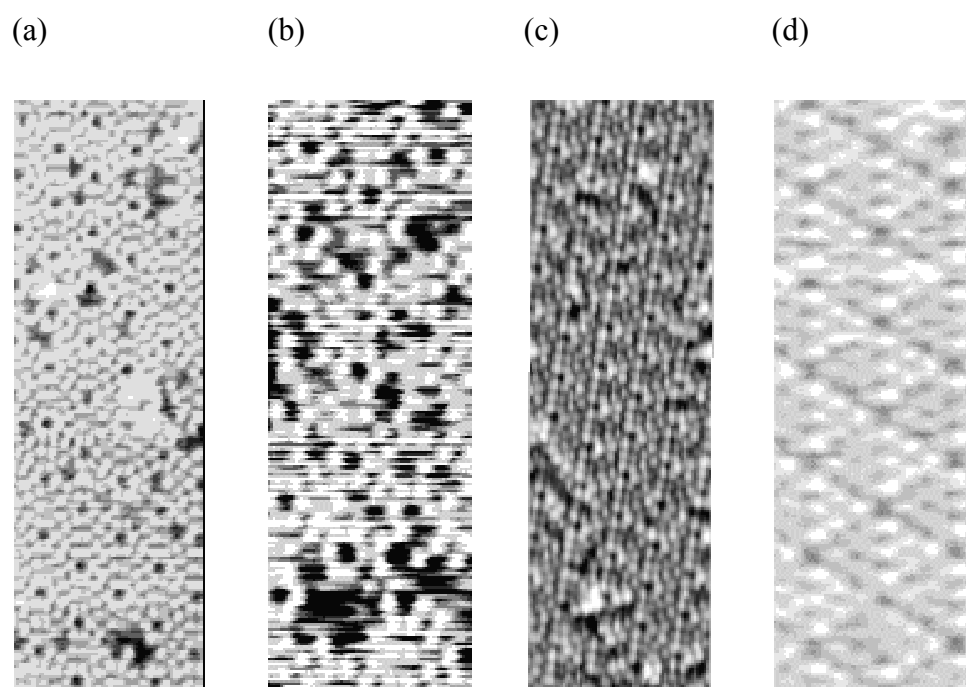


Fig. 3.5 STM images with various sample biases: (a) 1.6V, (b) 1.05V, (c) -1V, and (d) -2.5V. The images demonstrate that different sites contribute to the tunneling thereby enabling LDOS identification of specific structures.

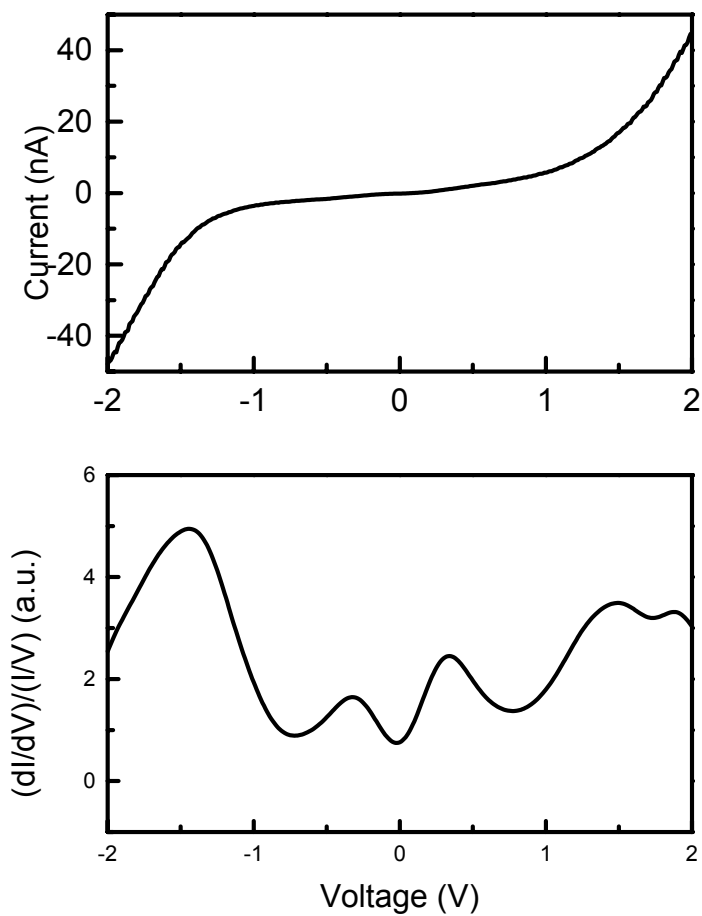


Fig. 3.6 I-V and $(dI/dV)/(I/V)$ of a clean silicon (7 X 7) surface. The two peaks within the bandgap are due to the surface states.

Chapter 4. Conducting AFM and electrical characterization

4.1 Introduction

The atomic force microscope (AFM) was introduced as a new instrument originated from STM using a different mechanism for imaging the surface [1]. AFM has become a widely used surface characterization tool in many laboratories these days. STM measures the local density of states (LDOS) on the sample thus true sample topography may not be revealed [2]. On the contrary, AFM measures sample topography using the atomic force due to the tip-sample interaction. Also in AFM, the sample surface to be imaged can be either conducting or non-conducting, making it much more versatile for many surface studies. Depending on the measurement scheme, AFM can be modified to measure different interaction between the tip and the sample. Some examples are electrostatic force microscopy (EFM) [3], magnetic force microscopy (MFM) [4], and local piezoelectric measurement [5].

Force sensing is the most important part of AFM, and it is done with microcantilevers. The cantilevers are the most important component of AFM and are typically made of silicon or silicon nitride. By using a conducting tip, it is possible to modify a conventional AFM to probe the electrical properties of a surface or interface. This is called conducting AFM (c-AFM) or conducting-probe AFM (cp-AFM). The nm scale imaging capability of AFM combined with the ability to probe electrical characteristics in c-AFM is becoming important for probing nanometer scale electrical properties on surfaces. In this chapter we discuss AFM techniques in general. Conducting AFM is also reviewed for its role in electrical characterization of local surface structures.

4.2 Review of AFM

The imaging mechanism of AFM is based upon attraction and repulsion force between the tip and sample surface. For approaching atoms or molecules, the interaction energy is given by the Lennard-Jones potential as shown in fig. 4.1. The actual geometry of the AFM does not correspond to two closely spaced atoms, rather it resembles a sphere above a plane. However, the general feature of force vs. distance remains unchanged [6]. On the left side of the force minimum, the force between the tip and the sample is repulsive and an AFM operating in this regime is normally referred as contact mode operation. For the right side of the minimum, the force is attractive and operating in this condition called non-contact mode. The distinction between these two modes will be described in detail later in this section. Also it should be noted that it is not the force but the gradient of the force that the AFM actually measures.

A basic atomic force microscope consists of three major components [1]: a force sensor in the form of a micro-cantilever, a mechanism for detection of the deflection of the cantilever, and a mechanism to move the tip or sample.

4.2.1 Force sensing

The cantilevers are typically made of Si_3N_4 or Si, and have a triangular or rectangular shape [7]. The force constants of these cantilevers are of the order of 10^{-2} to 10 N/m. So forces on the order of nano newtons can result in easily measurable tip deflection. Using lithographic techniques, a sharp inverted pyramid is formed at the end of the cantilever. The radius of curvature at the tip of the pyramid is typically 10 nm or less.

AFM tips are generally made of silicon or silicon nitride. In making AFM tips, anisotropic etching of silicon is utilized [8]. Starting with a Si (001) surface, the intended tip area is opened by exposing a photo resist layer. Then in KOH, the Si (111) surface etches more slowly compared to other orientations, and the resulting shape is an inverted pyramid. When the etching is complete, a Si₃N₄ film is deposited onto the surface. After defining the cantilever by another lithography step, the underlying silicon is etched away leaving a Si₃N₄ cantilever with a pyramid tip attached to the end. Silicon tips are made through a similar process.

The spring constant k of the cantilever relates the displacement of the end of the cantilever Δz to the force F applied by

$$F = k\Delta z. \quad (4.1)$$

The resonance frequency of the cantilever ω is approximated by

$$\omega = (k/m)^{1/2}, \quad (4.2)$$

where m is the mass of the cantilever. However the force at the end of the cantilever varies with the z , and above relation needs to be modified in most cases. The force varies with the distance between the tip and sample and can be written as

$$F = F_0 + (\partial F/\partial z)\Delta z = k\Delta z, \quad (4.3)$$

$$F_0 = (k - \partial F/\partial z)\Delta z.$$

The effective spring constant changes in the presense of a gradient in the force field. The resonant frequency of the cantilever also changes accordingly

$$\omega = [(k - \partial F/\partial z)/m]^{1/2}.$$

The change provides a method for controlling the distance between the tip and sample. The cantilever can be moved in z in such a manner as to keep the resonance frequency constant. The tip moves in the space where the force gradient is constant. Since the gradient is a single valued function of the z spacing, the tip spacing is also constant.

4.2.2 Detection mechanism

In AFM the deflection of the microcantilevers is measured and not the actual force between the tip and sample. There are many approaches for measurement of the deflection of the cantilever. Early in the development stage of AFM, a second tip was placed on top of the cantilever to measure the tunneling current between them and it was used as a means to detect the cantilever deflection [9]. These days, optical detection of the deflection is commonly used [10]. A laser and a position sensitive photodetector (PSPD) combination is used in our AFM (Park Scientific Instruments M5) to detect the cantilever deflection. The PSPD is four photodiodes built into one circular structure. The top half of the PSPD is called "A" and the bottom half is called "B". The difference in intensity between A and B is termed as "A-B" or "error signal". The laser is reflected from the cantilever and enters the photodetector. The reflected beam is adjusted such that A-B is minimized, meaning that the reflected laser intensity is equally divided between sections A and B. When the cantilever is deflected during the scan, the beam will be reflected at a slightly different angle, and A-B will change. This change is recorded as a function of the x and y coordinates of the tip, which results in topographic information of the surface.

Two different force schemes (attractive and repulsive) that were discussed earlier are used for imaging in AFM. In attractive force imaging, termed non-contact mode, the tip is oscillated at near its resonance frequency and scanned over the surface with a spacing of 5~20 nm. This spacing is controlled by monitoring the resonance frequency of the cantilever. The amplitude of the tip deflection depends upon the force gradient. A large force gradient exists at a sample surface, so the position of the surface can be accurately detected by this method.

The second imaging method uses the repulsive force, and this method is referred to as contact mode. In this mode the tip is placed much closer to the sample, and the tip is raster scanned to obtain an image of the surface. The tip experiences a repulsive force set by pushing the cantilever against the surface with a piezoelectric positioning element. The scanner extends and contracts in the z direction in order to maintain a constant force between the tip and the sample.

In contact mode, the sample topography can be imaged in either constant height or constant force mode. The constant force mode is equivalent to a constant tip deflection, which translates to a constant A-B photodiode signal. In constant force mode, a feedback loop is used to adjust the scanner's z extension so as to maintain a constant A-B signal. The scanner voltage in the z direction is called the "topography signal". Contact mode imaging is more convenient in that tip approaching can be achieved fairly easily whereas in non-contact mode it is more complicated. Also contact mode is better suited for when the sample surface is not subject to a change during the scan. In our experiment we have used contact mode with a constant force.

4.2.3 Scanner

The third component of an AFM is the mechanism for scanning. Either the tip or sample can be scanned. Our AFM is a tip-scanning system, meaning that the tip is rastered to generate a topographic image. In this system, the tip is mounted at the end of a PZT scanner with a maximum lateral deflection of 100 μm . In the sample-scanning AFM systems, the tip is stationary, and the sample stage is mounted to a PZT scanner. Generally, the sample-scanning systems are smaller and have better resolution. One advantage of the tip-scanning system is that it can accommodate larger samples. A more detailed description of the scanner can be found in chapter 3 of this thesis.

4.3 Conducting AFM

In this study, we have modified an existing AFM through combination with a conducting probe to characterize the electrical properties of nanoscale structures. This is the most direct way of probing electrical characteristics of nanoscale structures. However, achieving reliable contact to the surface has been the largest obstacle to obtaining meaningful data. In the c-AFM experiment, the main issues are fabrication of the conducting tip, and control of the mechanical and electrical properties of the tip-sample contact[11]. In this section, a brief review of various kinds of conducting probes is presented.

Commercially available conducting probes include heavily doped silicon tips, metal-coated tips, and boron-doped diamond tips. Due to the additional resistance of the tip-sample contact that is present in all conducting probes, the analysis is not

straightforward. Once a tip is selected one has to characterize its electrical contact to the sample before any interpretation of the properties of samples can be made. The contact resistance of the specific tip-sample combination can be measured, and this should be considered in obtaining information about the interface of interest.

4.3.1 conducting tip

In AFM imaging, we are usually only concerned about the sharpness of the apex of the tip. In c-AFM we also need to worry about the conductivity of the tip and the wear of the tip apex. In this section we begin by reviewing the tip fabrication process and later we will discuss how to select a tip appropriate for c-AFM.

The standard silicon tip formation process can employ heavy doping to produce conductive tips. Another method is to sputter deposit a metal film onto the surface of regular tips. These two methods have resulted in tips that showed good overall conduction but suffer a lack of wear resistance, and the tips become blunt or form a surface oxide. Therefore, the lifetime of these tips are severely limited when frequent electric measurements are made. Also deposition of the metal film creates extra stress on the cantilever, and sometimes it is difficult to achieve sufficient beam bounce off the backside of the cantilever. Annealing of the tip at moderate temperature (less than 300°C) could relieve the stress and result in appreciable beam reflection. This method was not pursued fully in our study but could be part of a future study.

Another method in achieving a conducting tip is the fabrication of CVD deposited diamond on top of the silicon tip. For high conductivity the diamond film is doped with boron. A CVD deposited boron doped-diamond tip was used in obtaining nanometer

scale steps on Au(111) layer on mica and demonstrated finite conductivity at zero bias in an STM I-V measurement [12]. Another study showed a small contact resistance ($\sim 1\text{k}\Omega$) on a metallic sample [13].

Diamond coated tips provide excellent wear resistance but sometimes suffer lack of electrical conduction. In this study we have used diamond coated tips with a high force constant that can provide high force of contact. The tips are commercially available from the manufacture of the AFM. In our experiments, many tips showed low conductance, but once a low resistivity was achieved, we found that the tip lasted for a long duration before it showed significant degradation. In addition, by applying a high voltage across the tip and sample contact, it was possible to recover the good conduction of the tip. The nature of electrical conduction at the sample will be discussed in the next section.

4.3.2 Tip-sample contact

Before any reasonable measurement and analysis can be made, we need to assure that the tip-sample contact is reliable. When considering the tip-sample contact, we need to consider the mechanical and electrical properties. First, we consider the mechanical nature of the tip-surface nano-contact. Modeling of the tip-surface nanocontact has been considered by Hertz [14]. The elastic contact radius is given as

$$a = \left(\frac{3Pr}{4E^*} \right)^{1/3}, \quad (4.4)$$

where a is the radius of contact, P the applied load, r the tip radius, and $E^* = [(1-\nu_1^2)/E_1 + (1-\nu_2^2)/E_2]^{-1}$ is the effective elastic modulus combined from Young's moduli E_1 , E_2 and Poisson's numbers ν_1, ν_2 of the tip and surface materials, respectively. For a diamond tip

and TiSi_2 substrate, the estimated contact radius is less than 2 nm for 100 nN of contact force.

The electrical contact has two scenarios depending on the contact resistance. For effective metallic behavior, the contact resistance is described by Sharvin's law [15],

$$R = 4\rho l/3\pi a^2, \quad (4.5)$$

where a is the contact radius, ρ and l is the resistivity and the electron mean free path of the metal, respectively. A previous study by Beale showed that the contact of a gold tip on a gold film has a contact resistance of 10 ohms but they also reported that occasionally the contact resistance was above 10^5 ohms [16]. They attributed the high resistance to the development of an insulating layer on the film which was presumably hydrocarbons. In our study similar behaviors were observed. The contact resistance of the diamond tip on a gold film was on the order of $\text{k}\Omega$ but occasionally this conductance could not be achieved even with a few tens of volts applied across the tip-sample interface.

When there is a thin insulating layer ($< 1\text{nm}$) at the tip-sample interface, the electron crosses the junction by tunneling. The contact resistance in this case becomes larger than $1\text{M}\Omega$ and can be described as

$$R = V/(\pi a^2 J).$$

The current density, J , is given as follows:

$$J = (3.18 \times 10^{10} V \Phi^{1/2} / \Delta z) \exp(-1.025 \times \Delta z \Phi^{1/2})$$

where V is the applied voltage and Φ , Δz are the mean potential height and the width of the barrier, respectively [17]. Because of the experimental environment, the development of this insulating layer was unavoidable and was frequently observed.

Before I-V measurements on the silicide islands, we measured the contact resistance of our diamond tip on the surface of a gold film and the surface of highly oriented pyrolytic graphite (HOPG). The results are shown in Fig. 4.2 and Fig. 4.3. The values of the contact resistance on gold showed very little variation over the range of contact forces once a good contact is established above ~ 60 nN. The contact resistance for HOPG (~ 150 k Ω) is somewhat higher than that of gold (~ 40 k Ω). This is probably due to the difference in Young's modulus between these two substrates. However, since we do not know the exact values of Young's moduli for these materials in nanoscale contact, the exact estimation would be difficult. Even though the contact resistance on TiSi₂ film was not measured directly, we may expect the contact resistance somewhere in this range.

In conclusion the contact between the tip and the sample in our work is elastic and ohmic, but this contact is hindered by many other undesirable factors such as humidity, surface and tip contamination, and tip wear. Careful monitoring of the tip-sample contact was necessary to obtain meaningful data.

4.4 c-AFM for I-V measurement and conductance map of submicron TiSi₂ Schottky diode

Our I-V measurement technique for submicron TiSi₂ islands using c-AFM is a relatively straightforward extension of the conventional method for macroscopic diode measurement. A Keithley 236 source measure unit (SMU) was used to perform the I-V measurement. The Keithley 236 SMU can apply voltages in the range of 0 to 110V and

measure currents in the range 1pA to 100 mA. The SMU is computer programmed for various voltage scans and ramping times. Instead of using a tungsten probe that is commonly used in conventional I-V measurements, the conducting tip of an AFM was connected to the SMU (Fig. 4.4).

For I-V analysis of the Schottky diode, the following procedures are performed. First, the overall diode characteristic is measured from 3V to -10V. Diodes that did not show blocking in the reverse bias characteristics were excluded from the next measurement step. Once good diodes were identified, their forward bias characteristics were measured more carefully with smaller voltage steps. In analyzing the I-V data, we resort to the standard thermionic emission theory of the metal-semiconductor interface [18], which was also reviewed in chapter 2. The SBH and ideality factor for nanoscale Schottky diodes are obtained from this analysis. A typical I-V curve is displayed in Fig. 4.5.

Using a somewhat different experimental setup from the I-V measurement, the c-AFM can be employed to obtain electrical information specific to the location of the tip on the whole sample area. The schematic of the experimental setup is given in Fig. 4.6. A summed AC ($f=1\text{kHz}$, $V_{\text{rms}} = 0.5\text{V}$) and DC (from -2V to 2V in 0.5V step) signal is applied to the tip-sample contact. Using the AC signal as a reference signal and a dual-phase lock-in amplifier (Stanford Research 830), we can measure the amplitude and phase of the voltage across a known resistor, which is connected in series with the tip-sample contact. The outputs (amplitude and phase) from the lock-in amplifier are fed back to the interface module of the AFM for image construction. The voltage outputs are

proportional to the slope of the I-V curve at the voltage of the applied DC bias. The phase output is related to the phase shift of that location.

This frequency is chosen in such a way that the system will have enough time to record the response from the sample at each pixel and at the same time the response is still valid in the quasi-static regime so that we can apply static interface analysis. For example, with a scanning rate of 1 Hz and scan size 1 μm , the scanning speed is 2 $\mu\text{m}/\text{sec}$. The size of the image is normally 256 x 256 pixels or 0.004 X 0.004 μm pixels. For a 1 kHz signal as in our case, the tip moves 0.002 μm while one cycle is completed, i.e. a half of the pixel size. Thus, the reference frequency is fast enough to have meaningful relation to the image yet slow enough that we can apply static analysis for the Schottky diode.

As the DC bias is changed, areas with different conductivities will give different signals. Therefore, we can map the surface of different conductivities. From scans of the various samples with different surface topography it was verified that electrical image was independent of the topographic image. Fig. 4.7 shows the conductance maps obtained from the Ti/Si macroscopic diode.

In addition to this conductance mapping, we have observed that the scan can result in modification of surface electrical properties. Moreover, topographic images obtained before and after a conductance image did not show any changes. But with a high DC bias applied during a scan electrochemical surface modification is evident as large scale images show that the previously scanned area displays different conductivity from the unscanned areas (Fig. 4.8).

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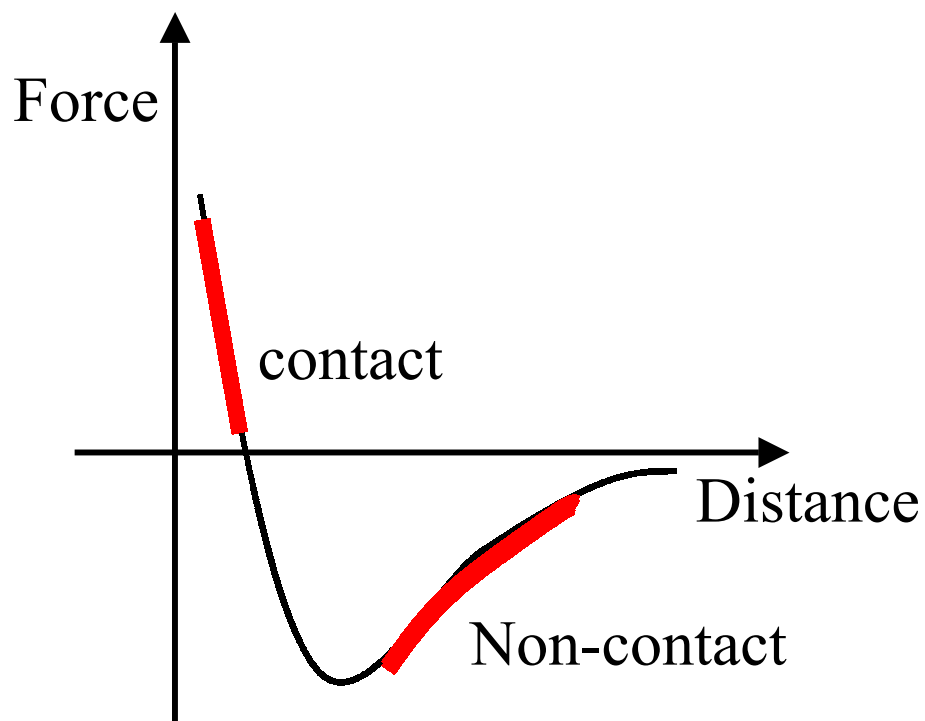


Fig. 4.1 The interaction energy is described by the Lennard-Jones potential for two closely spaced atoms or molecules. This force versus distance curve effectively depicts the AFM detection scheme.

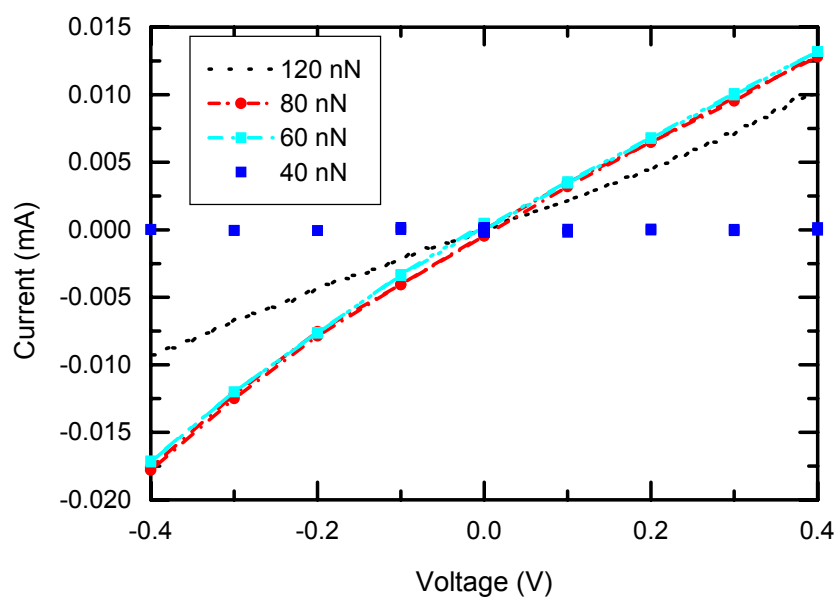


Fig. 4.2 The values of the contact resistance on gold showed very little variation over the range of contact forces once a good contact is established above ~ 60 nN.

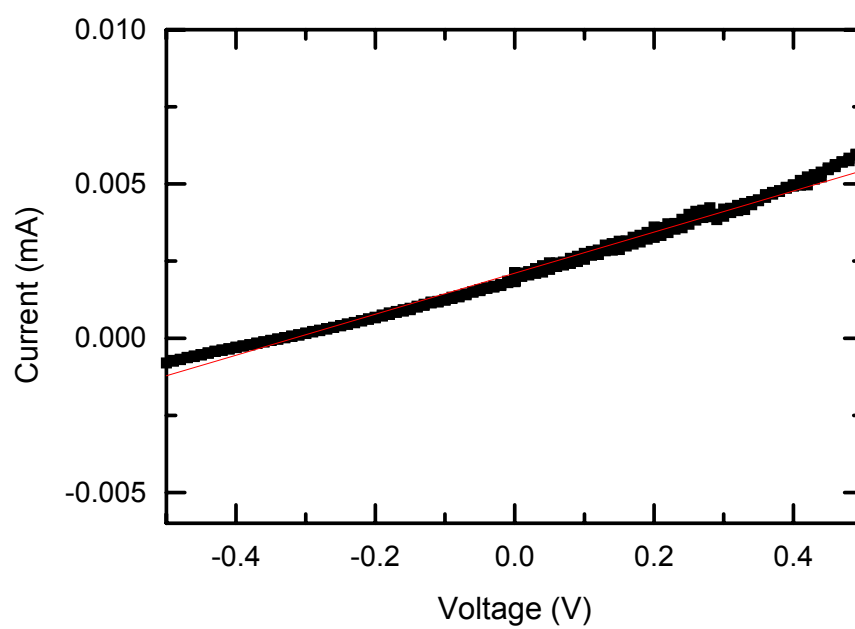


Fig. 4.3 I-V measurement on HOPG is shown. The contact resistance for HOPG (~ 150 k Ω) is somewhat higher than that of gold (~ 40 k Ω).

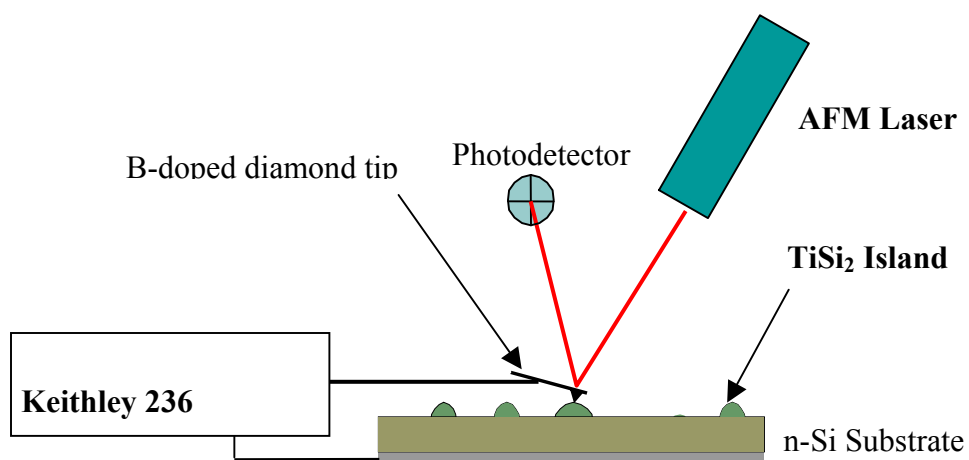


Fig. 4.4 Schematic of the AFM system used for I-V measurements of TiSi₂ islands.

Measurements are obtained with the tip sitting on top of the region of interest.

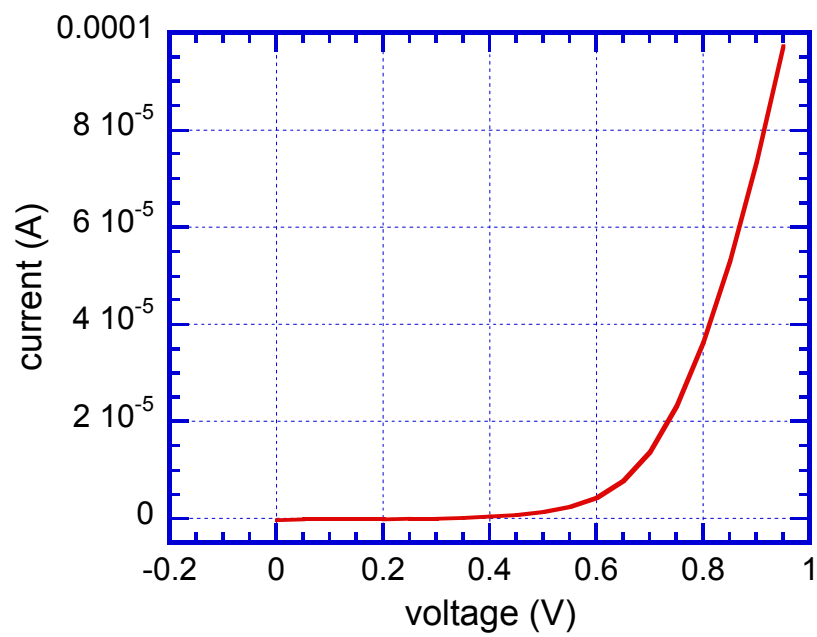


Fig. 4.5 Typical I-V measurement of TiSi₂ islands in forward bias is shown.

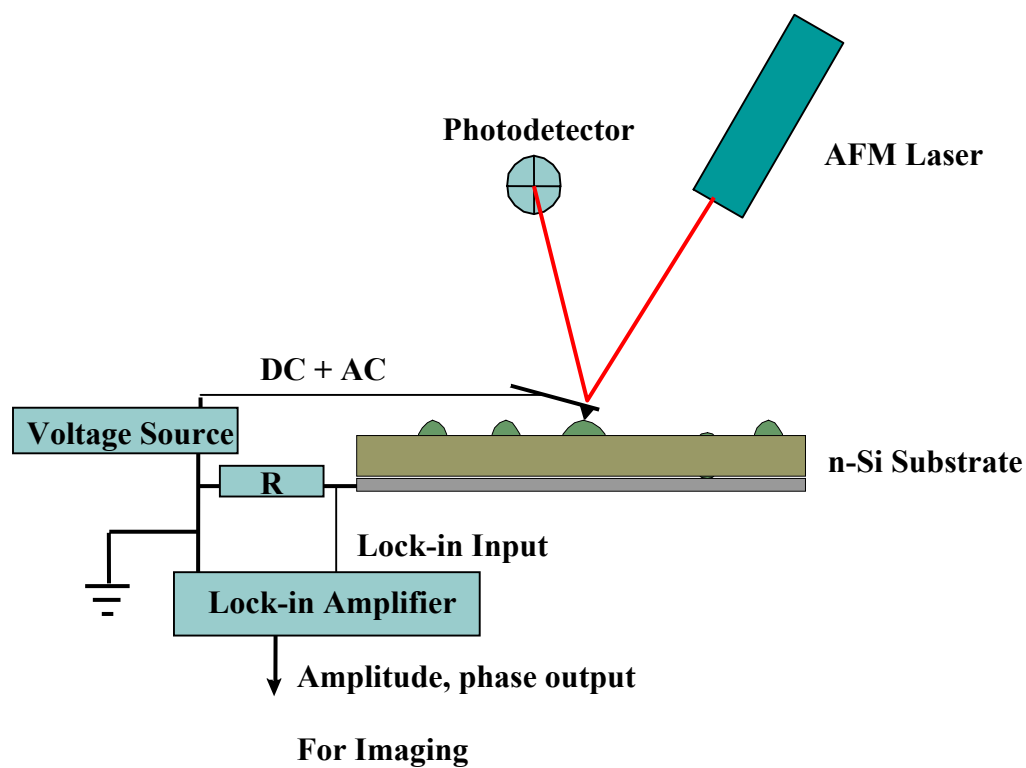


Fig. 4.6 Schematic of the AFM system used for imaging of TiSi_2 islands. Measurements are obtained with the tip scanning on the samples with DC bias changing between 0V and 2V. An AC signal (1 kHz, 0.5 V_{PP}) is added to the DC bias with a summing amplifier.

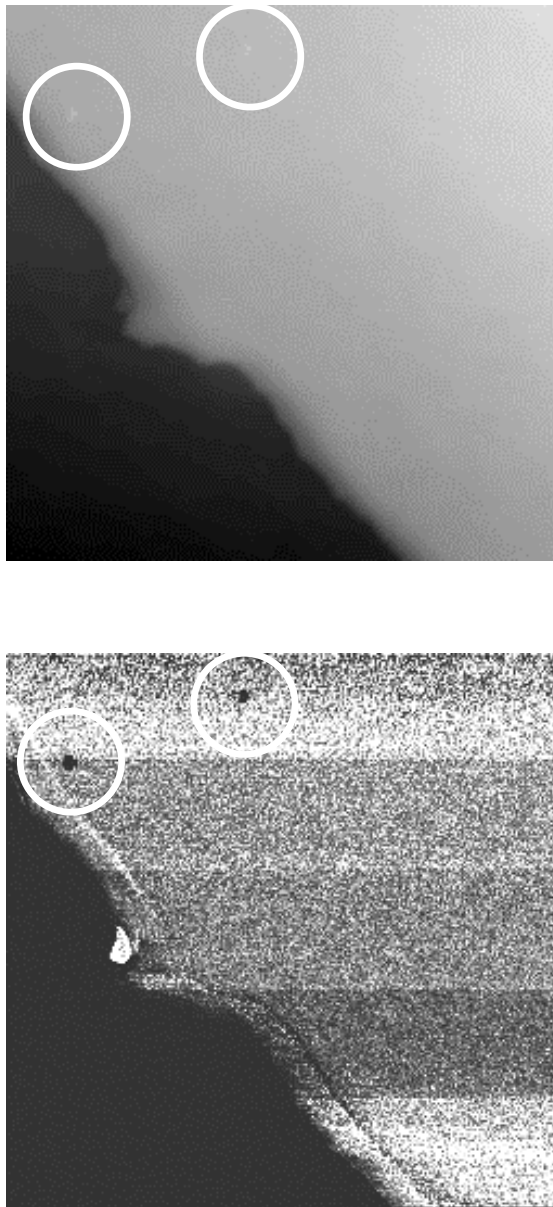


Fig. 4.7 $20 \times 20 \mu\text{m}^2$ scan of topograph and CN2 image (voltage output) on a macroscopic diode. Horizontal lines show where the DC bias is changed. Two circled regions shows no conduction in the electrical image.

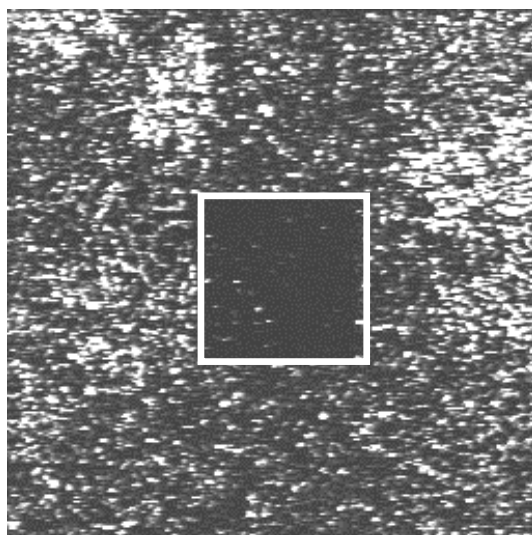
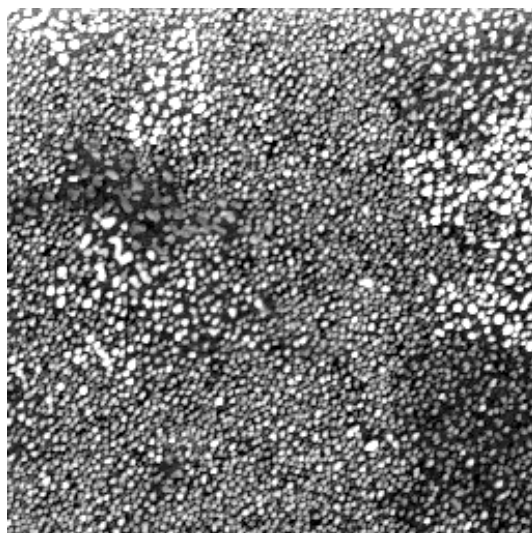


Fig. 4.8 $5 \times 5 \mu\text{m}^2$ scan of topograph and CN2 image obtained simultaneously. Marked region was previously scanned with voltage applied and shows less conduction while topography shows no difference from the rest of the surface.

Chapter 5. Experimental

5.1 Introduction

The main characterization tools that are used in this study such as UHV-STM and AFM/c-AFM were reviewed in separate chapters. Therefore, we will concentrate on the experimental facilities that are not mentioned in the earlier chapters.

To study the metal-semiconductor interface without an unwanted interfacial layer, an ultra high vacuum (UHV) environment is required. A high quality surface can be achieved and sustained in the UHV environment and UHV is generally termed as a pressure being less than 10^{-9} Torr. Our systems can achieve a chamber pressure less than 1×10^{-10} Torr. Even in UHV a surface is under impingement of molecules. At 1×10^{-11} Torr, the molecular incident rate is $\sim 4 \times 10^9$ molecules/cm²sec or $\sim 2 \times 10^5$ sec to form a monolayer [1]. Hence, an established clean surface can be maintained for several days under UHV. With the availability of UHV systems almost all studies of surface science are being undertaken in this environment.

Auger electron spectroscopy (AES) and low energy electron diffraction (LEED) are the most routinely used surface analysis tools. Chemical fingerprinting is possible with AES up to 0.02 atomic percent at the surface. Because of the characteristics of the Auger process, hydrogen and helium are not detectable. Quantitative analysis may be accomplished with varying degrees of accuracy by comparing the peak heights obtained from an unknown specimen with those from pure elemental standards or from compounds of known composition.

LEED is used to identify the structure of the surface after processing. It is established that surface layers dilate outwards by up to 5% of the bulk interlayer spacing [2]. Some surfaces may undergo rearrangement and have a different structure from that of the truncation of the bulk crystal. Information such as surface dynamics, lattice vibrations, and over layer arrangements can be deduced from LEED [3]. In our study, the technique was used primarily as a tool for *in situ* surface structure identification. In this chapter, the UHV systems and the above-mentioned surface analysis tools used in this study are described first, and the experimental procedures follow.

5.2 Equipments- UHV systems

There were two separate ultra high vacuum (UHV) systems used in this study. Each system is equipped with UHV pumping capability and standard surface analysis tools such as Auger electron spectroscopy (AES), low energy electron diffraction (LEED), and electron beam deposition. I will describe each system separately but duplicating components will not be re-described.

5.2.1 The metallization chamber (Dabney 28)

At the early stage of this dissertation work, for thicker titanium film depositions (1 to 4nm), the metallization chamber of the main system was used and is located in the basement of Dabney hall. It was used for sample preparation for the conducting AFM experiments. Detailed descriptions of the metallization chamber can be found in the thesis of Tracy [4].

The metallization chamber consists of a double walled 6-inch 6-way stainless steel cross, that is connected to a double walled 10-inch 6-way cross. The purpose of the

double wall is to act as a water-cooling jacket for the system. The process pump is a CTI Cryo-Torr 8. The base pressure of the system is $< 2 \times 10^{-10}$ Torr, and the attainable processing pressures are in the mid-to-high 10^{-9} Torr range.

The source material is placed in one of the five crucibles that are part of the water-cooled anode. The anode is on a linear motion feedthrough and can be positioned to have any of the five targets aligned for evaporation. The cathode is fixed to the system flange and aligned with the sample holder. Samples are positioned 38 cm above the cathode and can be rotated to face the cathode or positioned for removal from the system. Directly under the sample holder is a stainless steel shutter that is connected to a linear feedthrough. Adjacent to the heater equipped sample holder is a water-cooled film thickness/rate monitor. The thickness of the deposited metal is estimated *in situ* with a quartz crystal oscillating at ~ 6 MHz.

The AES/LEED system is connected between the integrated surface and growth systems (ISAGS) and the metallization systems. Isolation gate valves are located between the 6-way cross making up the AES/LEED system and the ISAGS and the E-Beam. The LEED system consists of a Princeton Instruments reverse view (RLV 6-120) optics and Princeton (11-020) LEED control electronics. The LEED images are projected onto a phosphor screen, which is located in front of the filament. Images are obtained using either a traditional camera or digital imaging equipment, which are mounted above the optics.

The Auger analyzer and electron beam source are located 180° from the filament for the LEED. This unit consists of a Perkin-Elmer/PHI 10-155 single pass cylindrical

mirror electron energy analyzer and a tungsten ribbon filament. Energy ranges from 0 to 3 keV can be scanned with this optics setup. The beam energy is selectable between 0.1 and 5.0 keV. Normal operation consists of a filament current of 2.0 mA and a 0.3 mA extraction current at a voltage of 3kV. These settings are appropriate for most semiconductors. The sample holder is capable of rotating 180° to accommodate alignment for either LEED or AES. The electronics for control of the analyzer are connected to a computer for automated data collection. The data is exported in DIF format and must be converted, using custom software, to an ASCII file prior to exporting to the data analysis software.

5.2.2 The small system (Cox 414)

A UHV system that houses the STM is called the small system in the surface science lab, and is located in 4th floor of Cox hall (Fig. 5.1). The small system consists of a deposition area, an analysis area and the STM. It is equipped with a load-lock for the fast sample entry. The system is pumped by an ion pump, which has a pumping speed of 230 liter/second. The base pressure of the system was better than 5×10^{-11} Torr after bake out.

For deposition of the initial films, an e-beam evaporator was used with titanium of 99.99% purity. Having titanium as a target material improved the vacuum performance of the system since while a film was deposited it was also deposited onto the chamber walls therefore, effectively functioning as a titanium sublimation pump. A mirror (bare silicon wafer) is located at 90° on a blank flange for visual inspection of the crucible during deposition.

Typical surface analysis tools such as AES/LEED and film thickness/rate monitor are also incorporated into the system enabling routine surface analysis. A magnetically coupled transfer mechanism that is standard in SSL is used for sample movement, tip exchange and sample storage. These are electrically isolated from the system chassis but a sample can be connected to an electrode located outside of the vacuum chamber through a feedthrough for resistive heating or for detection of the sample current in LEED and AES.

The whole system rests on an air suspension table for vibration reduction during STM operation. In the STM experiments noise reduction is critical to obtaining high quality images. This vibration isolation complements the existing double spring suspension in the STM head. Overall, the vibration isolation was satisfactory, although experiments at night showed better background noise reduction.

The sample holder/heater in the small system is different from the other heaters that are installed in the SSL [5]. The direct heating method is employed for less outgassing while heating to the high temperatures necessary for cleaning Si surfaces. The sample holder was designed to accommodate the requirements for sample transport compatibility. The sample holder consists of low vapor pressure materials such as molybdenum, tantalum, and alumina. External wire connections were provided by an electrical feedthrough for positive connection and an additional feedthrough is employed to maneuver the connector, as shown in Fig. 5. 2.

5.3 Experimental procedures

5.3.1 wafer preparation

The silicon substrates used in this study are sections cleaved from (001) and (111) wafers. Moderate doping levels of $10^{16} \sim 10^{17} \text{ cm}^{-3}$ were used for both n and p type substrates. The thickness of the wafers is $\sim 0.25 \text{ mm}$. For thicker film depositions in the c-AFM experiments, 25 mm diameter Si(001) wafers were used as substrates. These were cleaned using the recipe developed at SSL. First, a bare wafer is illuminated under a UV ozone lamp for 5 min. This densifies the native oxide on the surface and removes surface hydrocarbon molecules. It is followed by an HF spin etch. The solution for the spin etch is a 1:1:10 mixture of HF: DI water: ethanol. After this *ex situ* cleaning the wafer is visually inspected, and the procedure is repeated when residue is evident on the surface. After loading the wafer, *in situ* heat clean is performed at 900 or 1000 °C for 10 min. AES scans after the cleaning steps are shown in Fig. 5.3.

In STM experiments, the 7x7 reconstructed Si(111) surface provides verification of atomic scale resolution. The 7x7 reconstructed (111) surface is stable up to several days in UHV, and is ideal for many fundamental studies including spectroscopic investigations. Therefore, it was an obvious choice to investigate TiSi_2 nanoscale islands on the Si(111)7x7 surface with UHV-STM for SET.

For the STM measurements, Si(111) wafers are cut into small pieces of approximately 1.3cm x 0.5 cm. No *ex situ* preparation was done for these samples. The sample is loaded into the sample holder for STM and introduced into the load-lock chamber. After transferring into the main chamber, the sample is degassed overnight at

600 °C. The chamber pressure increases initially but remains in the mid 10^{-10} Torr range during the degas. The sample is cooled to room temperature before the ‘flashing’ begins. The sample temperature is raised to 1200 °C rapidly. There are many different recipes among the STM community, and we followed one similar to that from the Boland group [6]. The chamber pressure rises sharply in the beginning and drops quickly as the flashing continues. However, due to heating of the surrounding materials, the chamber pressure begins to rise again. Therefore, pressure monitoring is important, and care was taken not to exceed a chamber pressure of 2×10^{-9} Torr. The total amount of time that the sample is held at 1200 °C is about 1~2 min. The resulting surface exhibits a clean 7×7 reconstruction as well as monatomic steps in large-scale images as shown in Fig. 5. 4.

5.3.2 TiSi₂ island formation

In both chambers titanium was deposited from an e-beam evaporator. The operation principle of e-beam evaporation can be found from standard textbooks. In the metallization chamber, the deposition rate was 0.1nm/sec for 2-4 nm deposition. A slower rate of 0.1nm/min was used for the small system for deposition of 0.05nm to 0.1 nm. The chamber pressure rises during deposition to $\sim 5 \times 10^{-8}$ Torr.

After deposition, annealing was done either by radiative heating (metallization chamber) or direct heating (small system). Durations for annealing were 1 min. for thin film and 10 min. for thicker films, respectively. In the small system, the ramping time from room temperature to the final temperature (800 °C or 900 °C) was very short (~ 10 sec). The ramping time for the conventional heating in metallization chamber took several hours (the ramping rate was ~ 50 C/min). In principle there should be no effect from this

difference in ramping rate, but the comparison of ramping time could have implication in practical aspects. After transfer, the resulting surfaces were imaged either by UHV-STM after several hours of cooling or by an ambient AFM for thicker silicides (Fig. 5.5).

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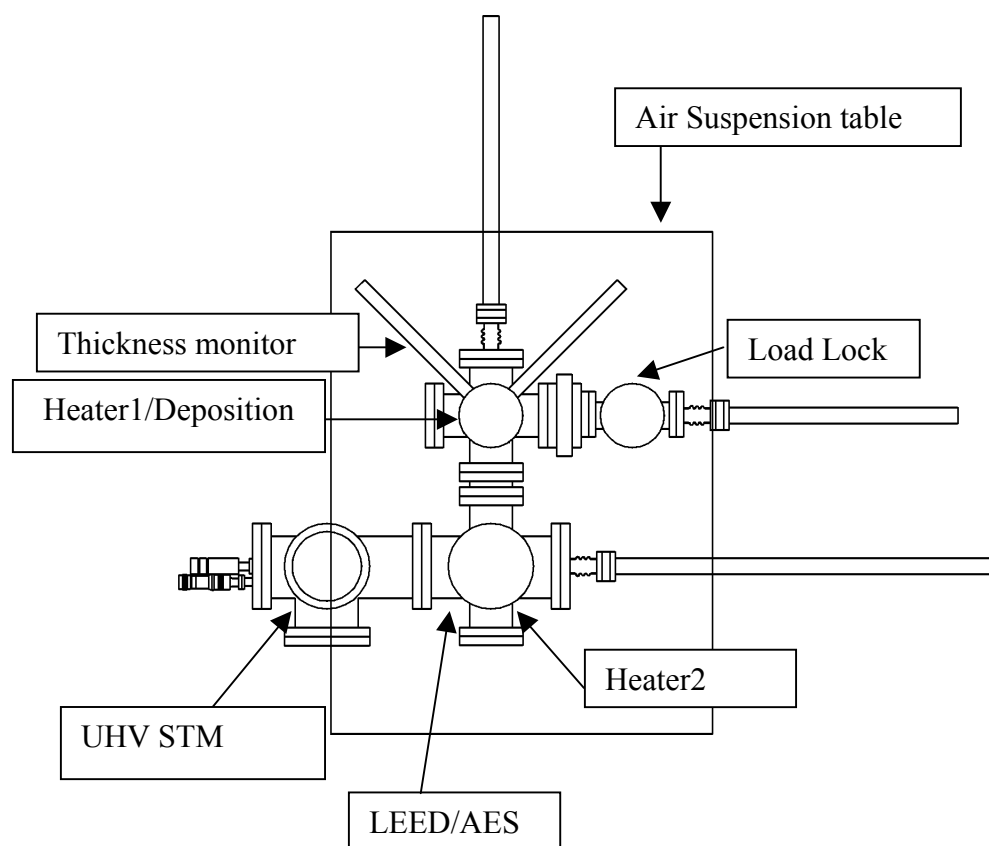


Fig. 5.1 A schematic of the “small system” that contains the UHV-STM.

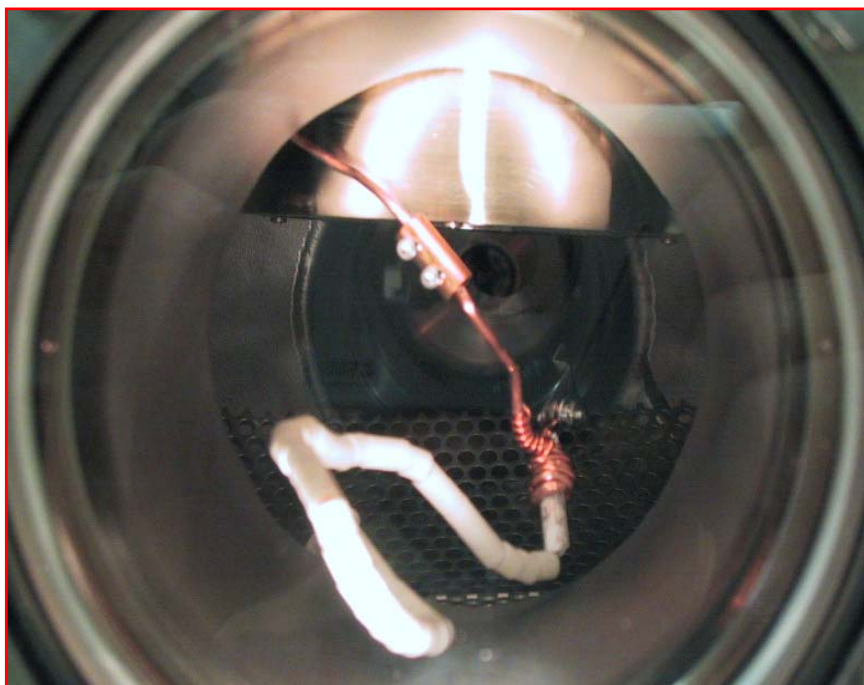


Fig. 5.2 The electrical connection for direct heating of sample. Sample holder is not in position for heating.

AES for cleaning steps

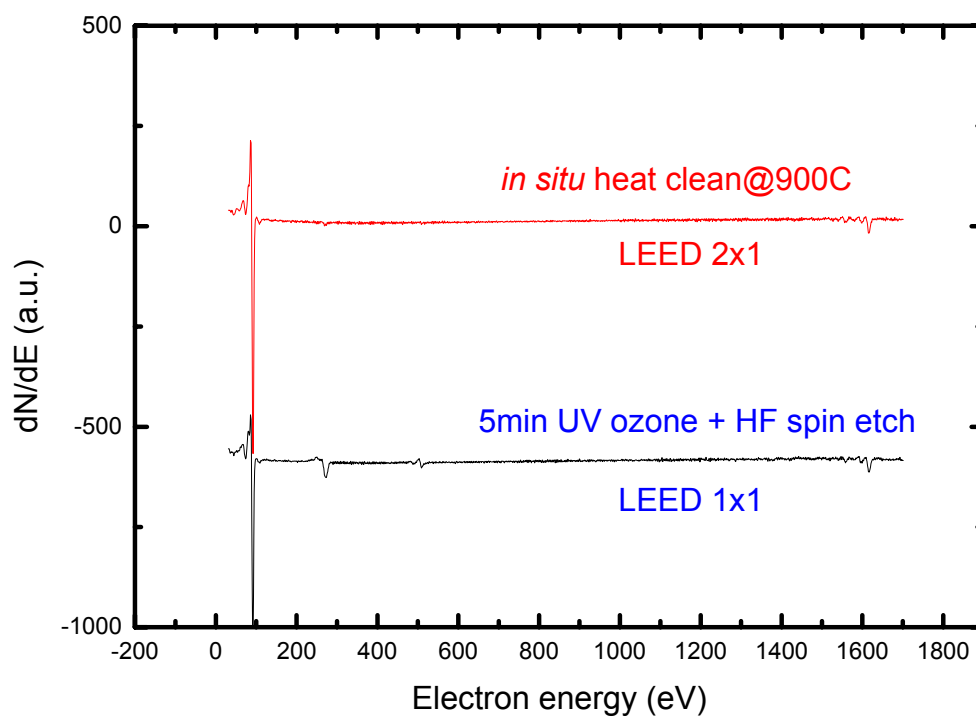


Fig. 5.3 AES obtained after wet clean and after heat cleaning in UHV. Carbon and oxygen is detected in the *ex situ* cleaned surface.

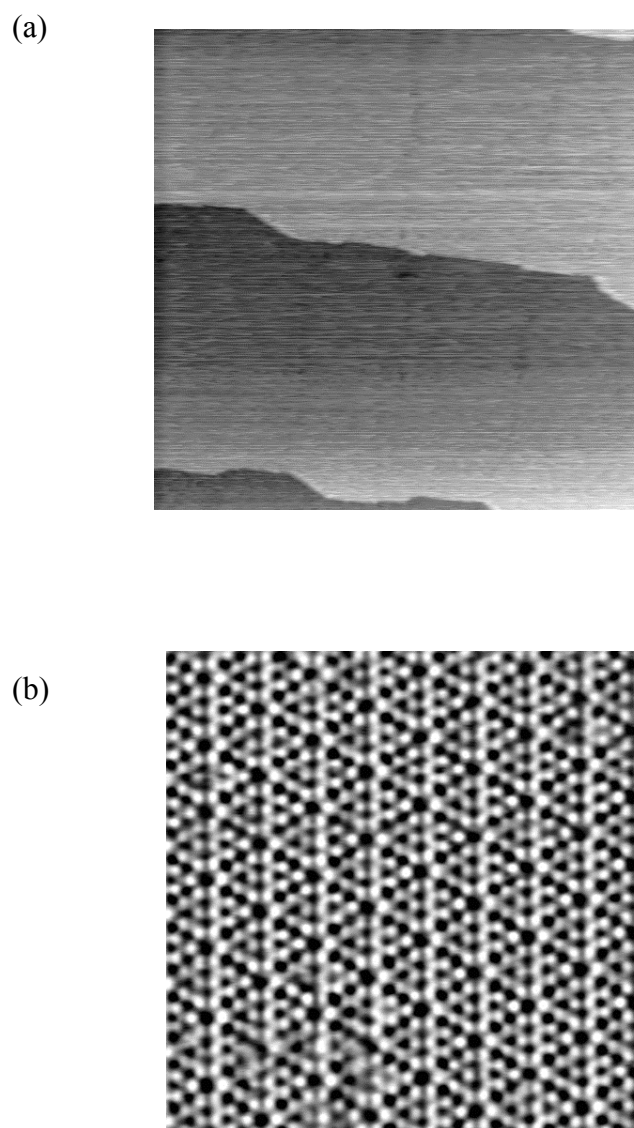


Fig. 5.4 STM images of a Si(111) surface after ‘flashing’; (a) 0.5 μm scan (b) 25 nm scan.

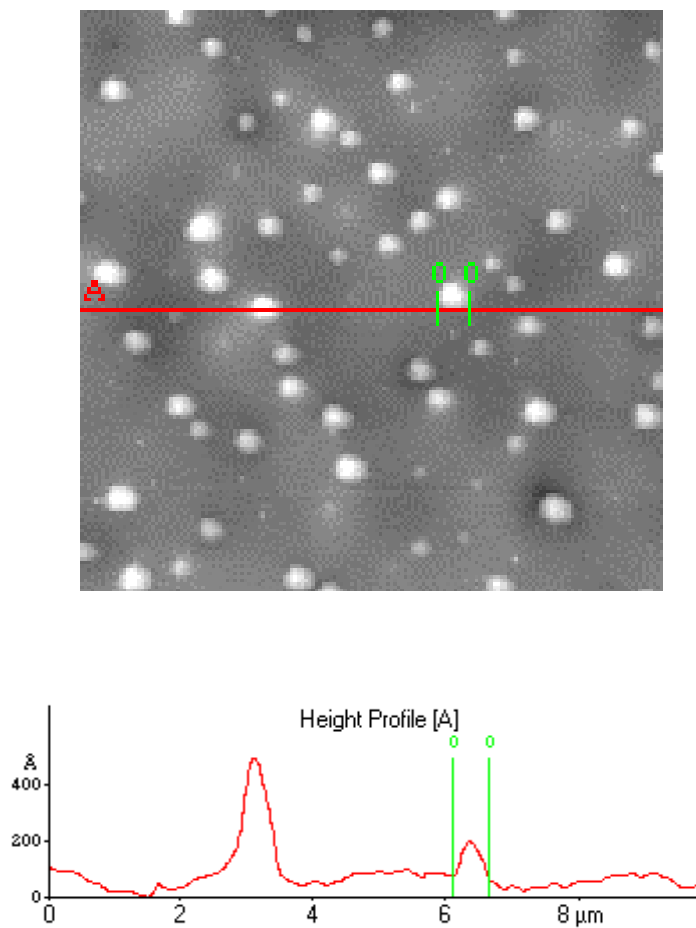


Fig. 5.5 AFM scan ($10 \times 10 \mu\text{m}^2$) of a surface with TiSi_2 islands. The islands were produced from 2nm Ti deposited at room temperature and annealed at 900°C for 10 min. The line scan displays the height of the islands.

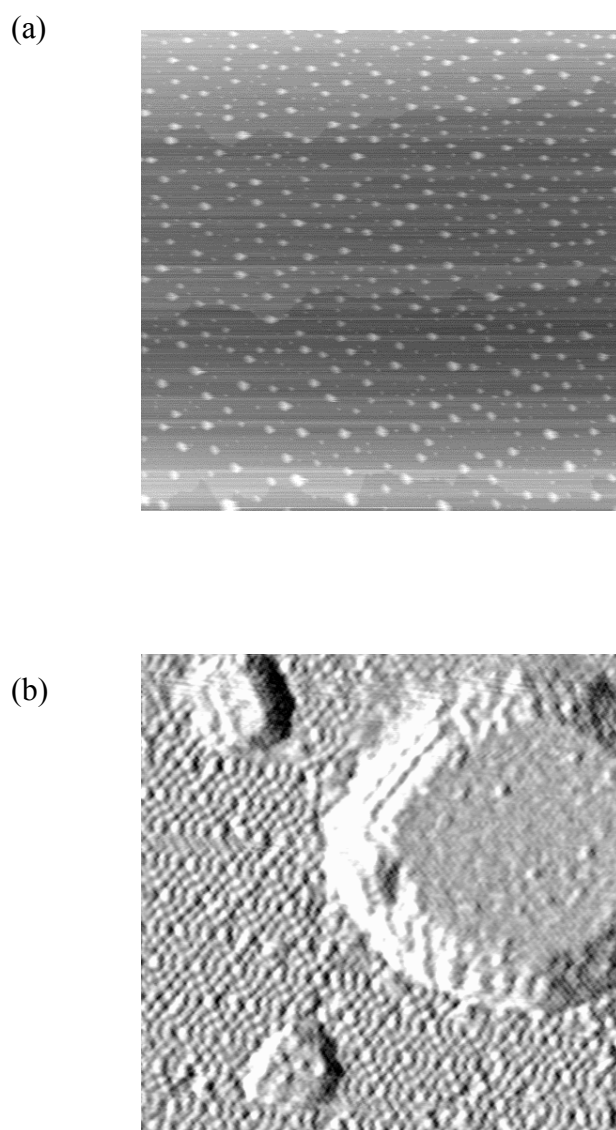


Fig. 5.6 STM scans; (a) $0.5 \times 0.5 \mu\text{m}^2$ and (b) $0.5 \times 0.5 \mu\text{m}^2$ of a surface with TiSi_2 islands. The islands were produced from 0.2nm Ti deposited at room temperature and annealed at 900°C for 1 min.

Chapter 6 Conducting Tip AFM for Current-Voltage and Imaging of TiSi₂ islands on Si(001) Surfaces

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6.1 Abstract

Using conducting tip atomic force microscopy (c-AFM), we have measured the current voltage characteristics of individual sub-micron islands of TiSi₂ on Si(100) surfaces and we have developed an imaging approach that distinguishes the electrical properties of the islands. The Schottky barrier height (SBH) of the sub-micron TiSi₂ islands was deduced from the I-V measurements. The results indicate that there is a significant variation of SBH among the islands on the same surface. The measurements employ a conventional AFM with a heavily B-doped diamond tip to obtain the current-voltage relations. In contact mode AFM, electrical signals are extracted independently from the topographic image. In addition, we have developed a new imaging method to probe the local electrical properties of a surface with regions of different conductivity. Using a lock-in technique both phase and amplitude images were obtained, and the resultant image is essentially a map of the differential surface conductivity. Using this method, TiSi₂ islands on a Si(100) surface were imaged. This approach can be readily extended to other materials systems.

6.2 Introduction

As device structures approach the nanometer scale it is necessary to characterize electrical properties on the same scale. In this size regime conventional electrical characterization approaches are limited by lithographic dimensions and probe positioning. Surface spectroscopic tools such as x-ray or ultra violet photoelectron spectroscopy (XPS or UPS) give area-averaged information even though they provide important information about the surface and interface electronic properties. Therefore, more approaches based on scanning probe techniques are being considered.

Since the inception of scanning tunneling microscopy (STM) in 1981 by Binnig and Rohrer, many variations of STM have been introduced [1]. These scanning probe microscopies (SPM) can provide location specific information. This information can be electrical, magnetic, friction or chemical according to the imaging mechanisms. In contrast to STM, AFM uses the repulsive and attractive forces between the tip and the surface for imaging the surface; therefore, it does not require the sample to have a conducting surface. The morphological and electrical properties can be separated more distinctly in c-AFM, and the technique can provide electrical properties of the surface that are not accessible from STM. For instance, it can be used as a micro-probe for I-V measurements after identifying regions of interest.

For local electrical properties there are established techniques such as electrostatic force microscopy (EFM) [2] and scanning capacitance microscopy (SCM) [3]. However, EFM operates in non-contact mode for detection of the surface charges and capacitance [4], but it cannot provide electronic transport information of the surface. Similarly, SCM

measures capacitance but does not provide, conductivity information. It is necessary to have local electrical information that EFM or SCM cannot provide, and the most direct approach is to use c-AFM to obtain local I-V measurements at the regions of interest. Prior studies using c-AFM have explored a variety of aspects such as surface conductivity [5], 2-dimensional dopant profiling [6], and nano-patterning [7]. However, there have been only a few studies where the electrical characteristics were measured directly on nanoscale structures using c-AFM [8], [9].

Previous studies have shown that a thin layer of titanium reacts with the silicon substrate to form nanometer scale silicide island structures [10-12]. These studies have mainly explored the morphological aspects of the islands. The silicide island formation process depends on the surface and interface energies, and for thin titanium layer (<25nm), the phase transition from the C49 phase to the C54 phase was not observed [13]. Another study using STM and transmission electron microscopy (TEM) by Williams et al. confirms the presence of the C49 phase for TiSi_2 islands on Si(001) that are incommensurate with the substrate [14]. These results demonstrated that it may be possible to control the surface dynamics to achieve the desired silicide nanostructures. In addition to the morphological study of these TiSi_2 islands, understanding their electrical characteristics is necessary in order to make an assessment for future electronic applications. Previously, we studied the electrical property of an assembly of TiSi_2 islands by using an over layer of platinum. The SBH was compared for structures with and without TiSi_2 islands, and the interface with the TiSi_2 islands showed a lower barrier

[15]. It is evident that direct electrical probing of individual nano-islands is necessary to develop an understanding of these effects.

It has been argued that the Schottky barrier heights (SBH) may be non-uniform even for intimate metal-semiconductor contacts due to variations of the interface structures and defects. Moreover, nanostructures may exhibit variations in dimensions and interface structure, which will significantly affect the local electronic properties [16]. Because of these effects, the sub-micron sized diodes may exhibit different SBH properties from that of macroscopic diodes. Therefore it is anticipated that there may be a significant fluctuation in the SBH of different islands on the same surface. Also, we may expect that transport mechanisms such as field-enhanced thermionic field emission (TFE) and hole injection that are normally negligible in macroscopic diodes may become important in the smaller size regimes.

It is our intention to enable local electrical measurements utilizing a c-AFM to explore the variations of the Schottky barrier and to clarify the issues of the SBH of nanostructures. In this work we have measured the local I-V characteristics of TiSi_2 nanoscale islands. We have also developed a new imaging method that enables identification of areas of different conductivities using a lock-in detection technique. The resulting map of differential conductivities of the surface is combined with the results from the I-V measurements to give a more detailed picture of sub-micron Schottky barriers.

6.3. Experimental

The substrates used in this study were 25 mm diameter Si(001)-oriented wafers with a resistivity of 0.8 - 1.2 Ωcm (n type, P doped, $N_D = 10^{16}\text{cm}^{-3}$). Prior to loading, the substrates were cleaned by UV-ozone exposure for 5 minutes followed by spin etching with HF:H₂O:ethanol, 1:1:10 at room temperature. Atomically clean surfaces were obtained after *in situ* thermal desorption at 900 °C as confirmed by low energy electron diffraction (LEED) and Auger electron spectroscopy (AES). The base pressure of the system was better than 5×10^{-10} Torr. The chamber pressure was typically better than $\sim 1 \times 10^{-9}$ Torr during the heat cleaning.

For deposition of the initial films electron beam evaporation was used with titanium of 99.99% purity, and the substrate was at room temperature. The deposition was measured using a quartz crystal monitor, and a nominal deposition rate of 0.2nm/min was used to obtain thicknesses varying from 1 to 2 nanometers. Following the deposition, the film was heated to 800 or 900 °C *in situ* for 10 min to initiate TiSi₂ island formation.

The AFM used in this study for both conventional imaging and electrical characterization is from Park Scientific Instruments (Model Autoprobe M5). All measurements were in ambient atmosphere. The conducting tips were also provided by the same manufacture, and the cantilevers had different spring constants allowing various contact forces. The typical radius of curvature of the AFM tips used is reported by the manufacture to be approximately 10nm. The imaging resolution was verified using a standard gold grid sample of 1 μm linewidth.

After scanning for normal imaging, an I-V measurement is taken while the conducting tip is fixed on top of an island or at an appropriate surface structure of interest. A schematic of the apparatus for the I-V measurements is given in Fig. 6.1. The bias voltage and resulting current can be both supplied and measured respectively using the same connection to the Keithley 236 source measure unit (SMU). The SMU was programmed for various voltage ramping rates and bias ranges. First, forward and reverse diode characteristics were measured. On some islands the I-V relations showed high resistance with no appreciable rectifying behavior. Only islands that demonstrated rectifying diode behavior were measured for forward bias I-V measurement. The I-V curves were fit with the standard expression for thermionic emission;

$$I(V) = I_s \exp(qV / nkT) [1 - \exp(-qV / kT)] \quad (6.1)$$

where q is the electronic charge, k is the Boltzmann constant, T is the absolute temperature, V is the applied bias, and n is the ideality factor. In the above equation, I_s is the saturation current, given by

$$I_s = A^* AT^2 \exp\left(-\frac{q\Phi_B}{kT}\right), \quad (6.2)$$

where A is the area of the diode, Φ_B is the Schottky barrier height (SBH) of the junction, and Richardson's constant, A^* , of $110 \text{ A/cm}^2\text{K}^2$ for n-type silicon was used [17]. For $V > 3kT/q$, Eq. 6.1 can be rewritten as

$$I = I_s \left[e^{\frac{qV}{nkT}} - 1 \right], \quad (6.3)$$

and we will use this expression to determine the SBH and the ideality factor for the islands. The measured forward I-V curve is described on a semi-logarithmic plot. The

linear region is fitted to obtain the slope and the y-intercept. The ideality factor and SBH are found from the slope of the linear region ($d\ln I/dV$) and the saturation current (I_s), respectively, i.e.

$$\frac{1}{n} = \frac{kT}{q} \frac{d(\ln I)}{dV}, \quad (6.4)$$

$$\Phi_B = \frac{kT}{q} \ln \left(\frac{A^* AT^2}{I_s} \right) \quad (6.5)$$

Calibration of the contact and tip resistance was obtained from the I-V measurements on freshly cleaved highly oriented pyrolytic graphite (HOPG) and gold films as well as on Ti/n-Si macroscopic Schottky diodes. At several hundred nN of contact force, the tip-surface contacts on HOPG and gold films were both ohmic up to $\pm 0.5V$. The contact resistances were on the order of several tens of $k\Omega$ for both HOPG and gold films. The small contact resistance values contributed little to the overall electrical characteristics of the islands as will be discussed later.

The I-V curves measured on macroscopic Schottky diodes (Ti 50nm/n-Si; 300 and 500 μm in diameter) using conducting tip-AFM and a standard tungsten probe are compared in Fig. 6.2. For tips with lower force constant, the current did not reach the same values as those by the tungsten probe presumably due to the lower force. Therefore, it was assumed that the tip-surface contact in this case was highly resistive and/or non-ohmic. Some tips showed no measurable current ($I < 10^{-11}$ A) up to 50V suggesting that contamination or an insulating layer may develop on the tip or island. Usually, supplying a high voltage ($\sim 10V$) between the tip and the sample generated a sharp increase of current after which the conduction showed significant improvement. During this so-

called ‘pulsing’ process, some tips showed degradation of their apex as evidenced by topographic images showing double tip imaging or a blurred image. Also, this process occasionally created a large crater on the sample indicating that there was surface melting or arcing. Therefore, images were carefully analyzed before and after each I-V measurement to ensure that the tip did not experience such abrupt changes.

For our technique of imaging the conductance map of the surface, the setup is given in Fig. 6.3, and it is somewhat similar to that of Christman’s [18], which was used for piezoelectric measurement of PZT films. A summed AC ($f=1\text{kHz}$, $V_{\text{rms}} = 0.5\text{V}$) and DC (from -2V to 2V in 0.5V step) signal is applied to the tip-sample contact. Using the AC signal as a reference signal and a dual-phase lock-in amplifier (Stanford Research 830), we can measure amplitude and phase of the voltage across the known resistor, which is connected in series with the tip-sample contact. The outputs (amplitude and phase) from the lock-in amplifier are supplied to the interface module of the AFM for constructing an image.

Fig. 6.4 is the simple schematic of the circuit for this measurement assuming that the island is a combination of resistance and capacitance. The output voltage and phase for the lock-in amplifier are extracted from the known resistor R_0 . The voltage outputs are proportional to the slope of the I-V curve, i.e. the differential conductivity. The phase output is related to the phase shift of that location. The fact that there is a significant phase variation confirms that each island has some capacitive component, which can be expected assuming the depletion region capacitance will be varying from one spot to

another. Therefore we are measuring the differential conductivity and time lag of each point.

For successive images at the same area, the DC bias was increased by 0.5 V from 0 to 2 V. As the DC bias is changed, areas with variations in differential conductivities will give different signals. Therefore we can map the differential conductivities of the surface. The electrical images obtained are effectively independent from topographic images as evident by the variations demonstrated in Fig. 7.

6.4. Results and Discussion

6.4.1 Formation of nanoscale Schottky barriers

In this work, we have used boron-doped diamond tips with two different force constants ($k= 17.1$ N/m, 2.1 N/m respectively). Generally, tips with higher force constant showed better contact characteristics but occasionally the tips with lower force constant also provided good contact. When the tip conduction was high, the tip lasted for more than 100 I-V scans before showing signs of degradation as indicated by blurred images or multiple tip imaging. The combination of the small area of contact, weaker contact force, and unknown nature of tip apex resulted in a contact resistance sometimes larger than several 10's of $M\Omega$ or even reaching $G\Omega$ values. With this in mind, only tips with low contact resistance were used for data collection. These tips showed contact resistances of ~ 10 $k\Omega$ which remained constant. Therefore, this additional resistance must be taken into account when analyzing the results. Since the maximum current through the structure is very low ($< 10^{-9}$ A) at low forward bias, the additional voltage across the tip-sample

contact was on the order of $1 \mu\text{V}$. The analysis showed that the overall I-V characteristics were not affected significantly after subtraction of this voltage.

Fig. 6.4 (a) displays an AFM image of a surface with several TiSi_2 islands of different sizes. From our previous studies, the resulting TiSi_2 islands have the C-49 crystal structure when the deposited films were less than 2.5 nm [13]. Cross sectional TEM showed that the island-substrate interface is formed below the surface, indicating that the surface and interface energies play a role in determining the island shapes [19]. From the TEM images, the interface between the island and the substrate was shown to vary for different island shapes. Some islands showed a flat interface while others showed a sharp v-shaped interface. This variation of the island-substrate interface may have a significant effect on the electrical properties of the TiSi_2 islands. In fact, the same diameter islands demonstrated a large variation of SBH. This indicates that the interface shape can affect the SBH of individual islands.

The I-V curves from individual islands, were fitted with the thermionic emission theory [20]. The SBH and the ideality factor were extracted from the saturation current and the slope of a semi-logarithmic plot. Fig. 6.4(b) and 6.4(c) display the measured I-V for the smaller and larger islands shown in Fig. 6.4 (a), respectively. We have measured I-V for islands varying in size from 0.1 to $1 \mu\text{m}$ in diameter for 20 islands. On each island 4~5 I-V measurements were taken with a good repeatability. The SBH's obtained are scattered from 0.45 eV to 0.58 eV with no direct correlation with the island sizes. In Fig. 6.5 (a) and (b), we showed the SBH's plotted versus their ideality factors and their size, respectively.

For macroscopic (several hundred microns in diameter) Schottky diodes of TiSi_2 on n-type silicon, the reported values are ~ 0.6 eV [21]. Therefore we have observed a reduced SBH for sub-micron Schottky diodes. [16]. This result is consistent with our previous result, which showed lowering of the SBH of an assembly of TiSi_2 islands [15], which was inferred from the I-V measurement with a platinum top electrode sandwiching the TiSi_2 islands.

6.4.2 Ideality factor

It was observed that the ideality factor for the sub-micron Schottky diodes are higher than unity ($1.2 < n < 2.5$). In Fig. 6.5 we show the distributions of SBH with their ideality factors. A nearly linear relationship between SBH and ideality factor is observed. An ideality factor close to unity implies that the diode is uniform and has a high quality interface with the substrate. This also implies that the current transport is described by thermionic emission theory. Thus, if the ideality factor deviates from unity, the thermionic emission theory alone cannot explain the result. The non-ideality can be accounted for by introducing a bias dependent barrier height [22]. A bias dependent barrier height can originate from several mechanisms such as image force lowering, interface states, hole injection and generation-recombination, and enhanced thermionic field emission (TFE). The effect of image-force lowering on the forward bias I-V is negligible when the doping density is low to moderate ($N_D < 10^{17} \text{ cm}^{-3}$) [20]. Therefore, the increase of ideality factor by image force lowering is not significant for our samples [22]. Also we can rule out effects from interface states since the islands with the lowest ideality values give results similar to bulk values. The island-substrate contact is an

intimate contact in the sense that there is no interfacial layer as confirmed by our earlier TEM studies [23].

Hence, we are left with enhanced TFE and hole injection to explain the higher ideality factors. As pointed out earlier, the interface between the island and the substrate was not uniform and showed various faceted shapes. Since the radius of curvature for the islands can be very small for sharp faceted islands, the effect of field enhancement will be greater for these islands. This could lead to enhanced thermionic field emission for the island.

On the other hand, as the contact area for the Schottky diode becomes smaller, it was found that the decay of injected minority carriers was more rapid [24]. This enhances the minority-carrier diffusion current density. For a theoretical diode with a SBH of 0.9 eV (radius of the diode was 0.2 μm), the minority injection ratio as high as 0.95 was obtained from the calculation [24]. At this stage we do not know which process dominates for deviation from the ideal case. Additional studies such as the temperature dependence of the I-V could clarify issues related to this phenomenon.

6.4.3 non-uniformity of SBH observed from conductance map

In Fig. 6.6, we show sequences of differential conductance images as the dc bias on the sample is changed. As the bias voltage increases the island shape becomes clearer. This indicates that with higher bias the differential conductance becomes larger relative to the substrate. Clearly, we observe differences between islands that have nearly the same sizes. One aspect to note is that some islands are not seen at all even though their

topography shows island shapes. This demonstrates the ability of this technique to delineate the conductivity differences between the islands.

Occasionally in these conductance images, some islands show higher conductances at the edge as seen in the higher bias images in Fig. 6.6. When enhanced edge conduction is observed, it was independent of scan direction; thus, the possibility of anisotropic tip effects were ruled out. As stated earlier, previous cross-section TEM studies showed that islands formed faceted interfaces with the substrates. Therefore, if the island has formed facets at the edges, it is possible that the electric field will be bunched leading toward a lowering of the SBH at the edge.

The lock-in amplifier detects the output voltage and phase across the resistor, which are proportional to the slope of the current and the RC time delay at each point, respectively. Since different areas have different conductivity and capacitance, it may be possible to generate a map of resistance and capacitance of the whole surface with assumption that the island capacitance and resistance act in parallel. Preliminary results indicate that calculated resistances and capacitances of each island are in good agreement with this assumption. On one of the island we have obtained the resistance and capacitance of several $M\Omega$ and $\sim 10^{-10}$ F, respectively. However, the implementation of this approach to obtain the whole area map would require intensive computing.

This again is based on the assumption that each island has a different barrier height since the imaging electrical signals is purely based on the differential conductivity. This technique can be applied to mapping out the surface with unknown conductivities.

6.5 Conclusion

In this study we have successfully measured the electrical properties of TiSi_2 islands that are $< 1 \mu\text{m}$ in diameter. To our knowledge this is the first study of electrical properties of nanometer sized silicide islands on a silicon substrate which display diode-like behavior. Specifically the Schottky barrier heights of these nanoscale islands have been measured. High ideality factors have been discussed in light of several possible transport mechanisms. It was observed that the reduced SBH for many islands had no direct correlation with the size of the islands rather we suggest that the interface structure plays a more critical role in the lowering of the SBH. We have also developed a method for mapping the surface conductivity and topography simultaneously and independently. The data shows that individual islands with different but similar electrical properties can be identified. This mapping technique can be used to quantitatively identify the conducting regions on the surface. The technique developed in this study can be readily extended to other nanoscale structures on semiconducting surfaces.

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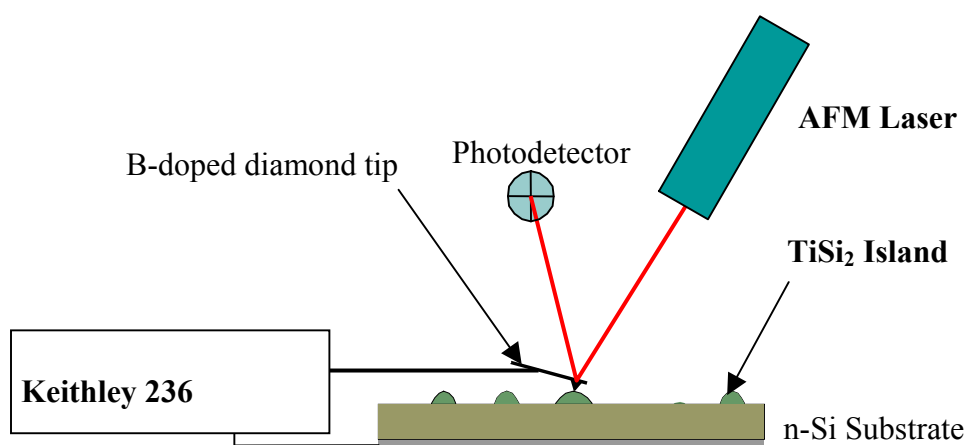


Fig. 6.1 Schematic of the AFM system used for I-V measurements of TiSi₂ islands. Measurements are obtained with the tip located on top of an island or other region of interest.

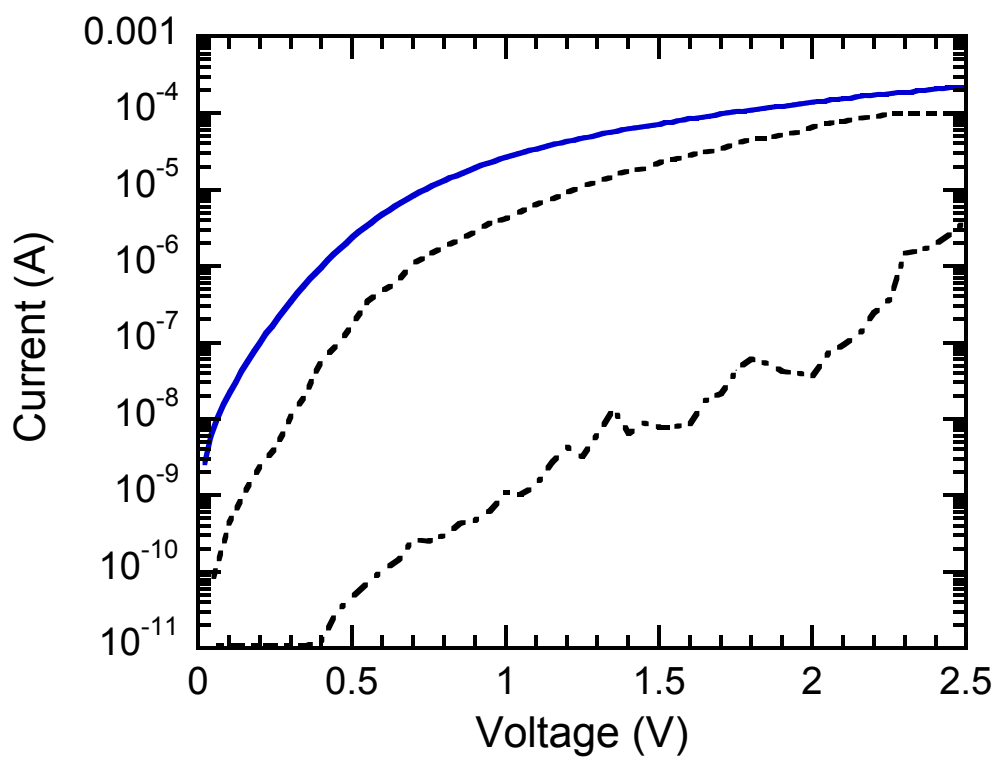


Fig. 6.2 Typical forward I-V curves on the same diode using different probes: tungsten electrical probe (solid), diamond coated AFM tips with $k = 17$ N/m (broken); and with $k = 1.7$ N/m (dot – dash).

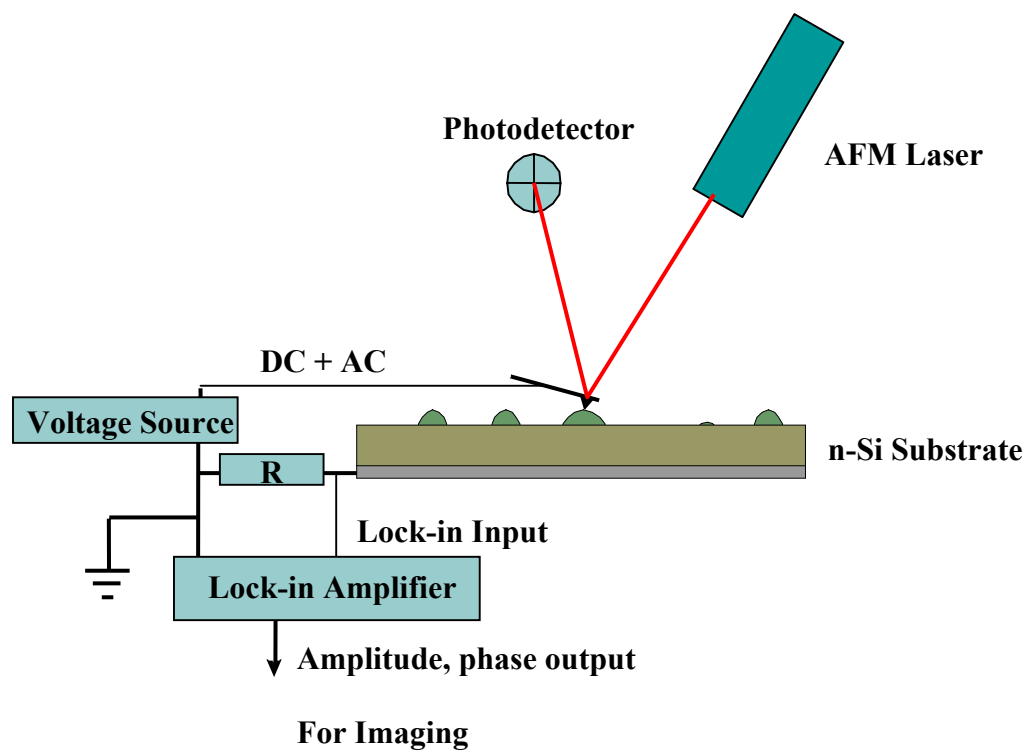


Fig. 6.3 Schematic of the AFM system used for imaging of TiSi_2 islands. Measurements are obtained with the tip scanning the samples with a fixed DC. The DC bias can be changed to emphasize the variation in the differential conductance of islands and substrate, an AC signal (1 kHz, 0.5 V_{PP}) is added to the DC bias with a summing amplifier.

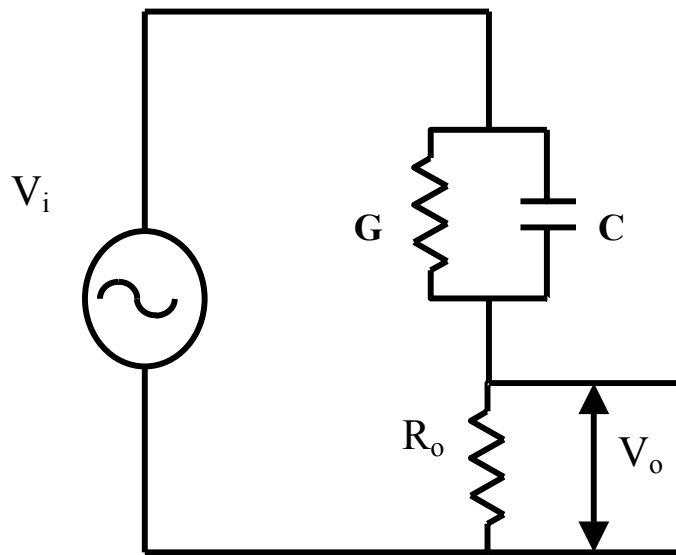


Fig. 6.4 A simplified circuit for G, C model of an island. V_o can be calculated assuming the island as a parallel combination of a conductance and a capacitance.

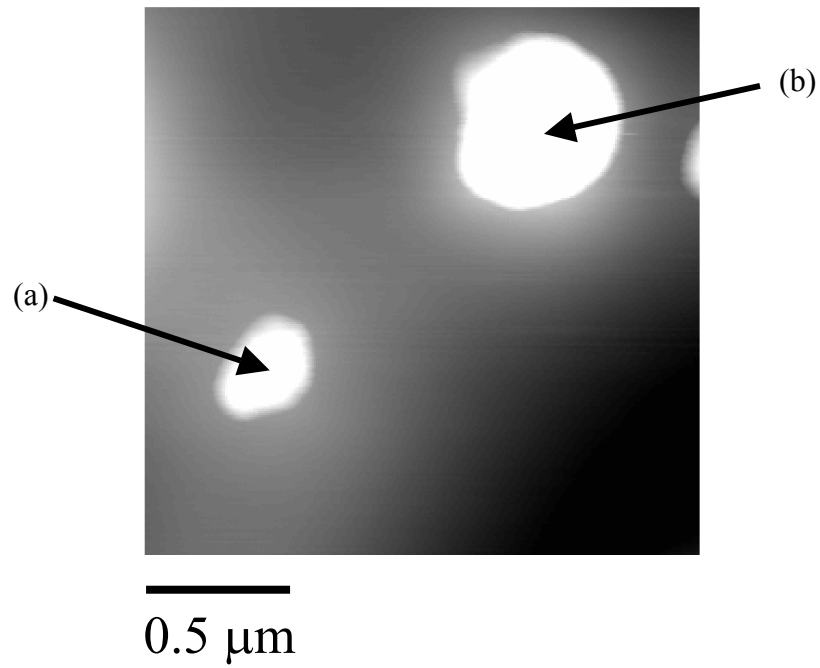


Fig. 6.5. I-V measurements are made after the AFM scan.

(a) I-V curve on smaller island with $d = 0.36 \mu\text{m}$; SBH = 0.47 eV, $n = 1.70$

(b) I-V curve on bigger island with $d = 0.62 \mu\text{m}$; SBH = 0.43 eV, $n = 2.25$

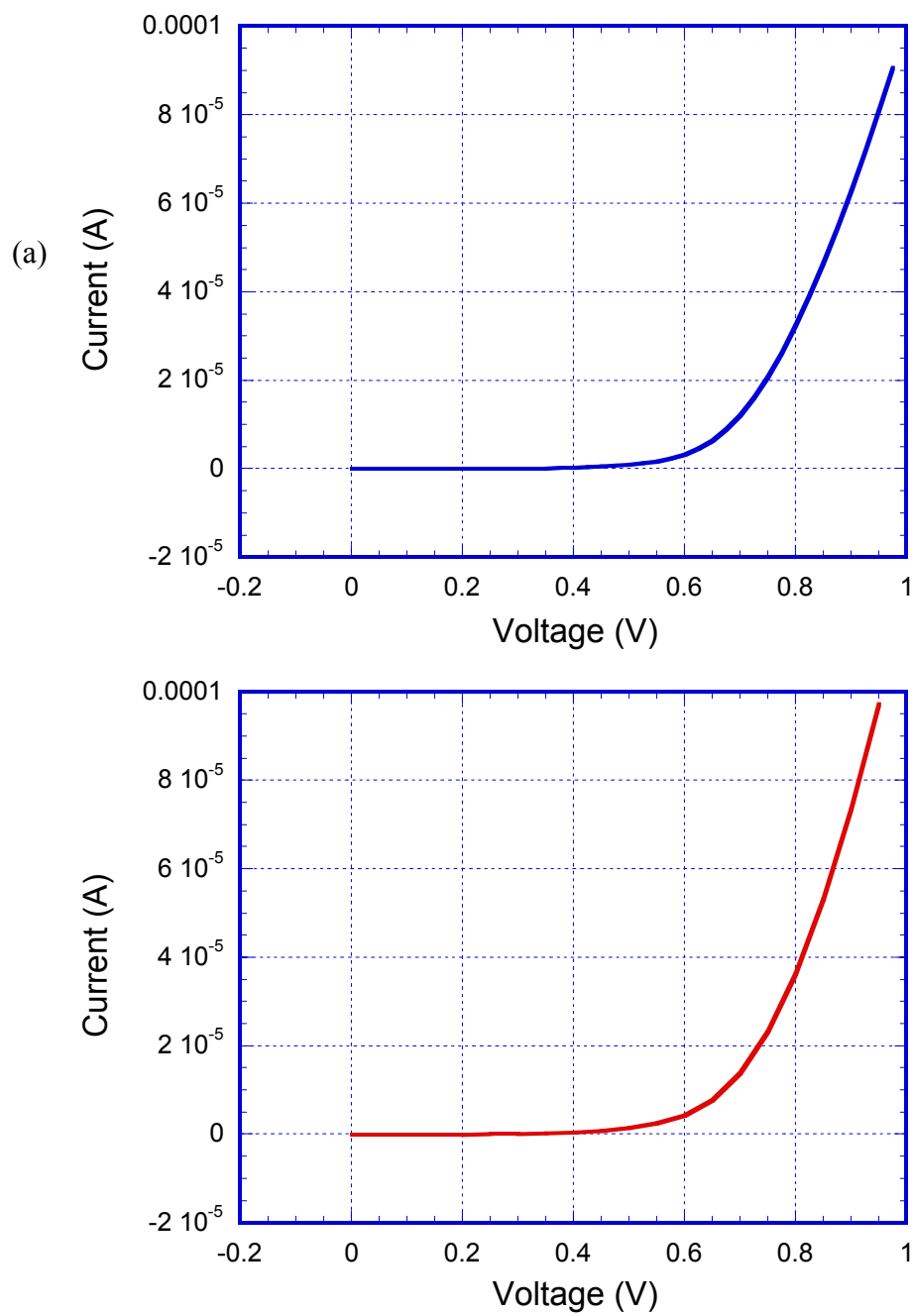


Fig. 6.5. (continued)

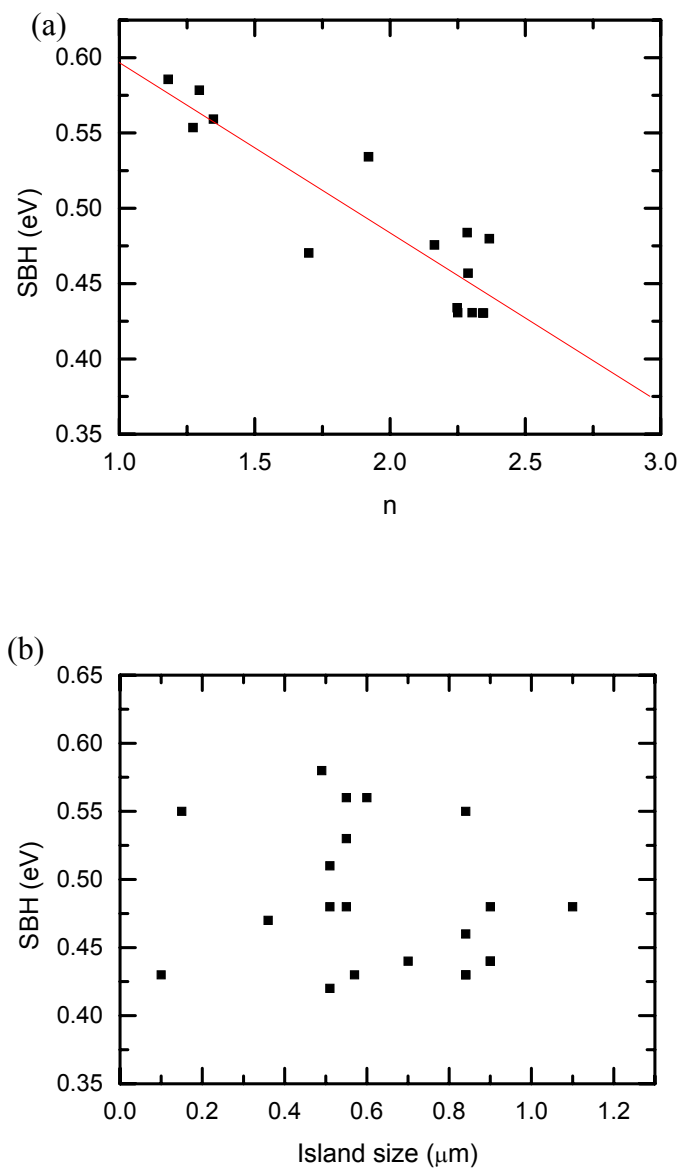


Fig. 6.6 (a) SBH vs. ideality factor; a nearly linear relationship is obtained. (b) SBH vs. island size. No relationship is seen.

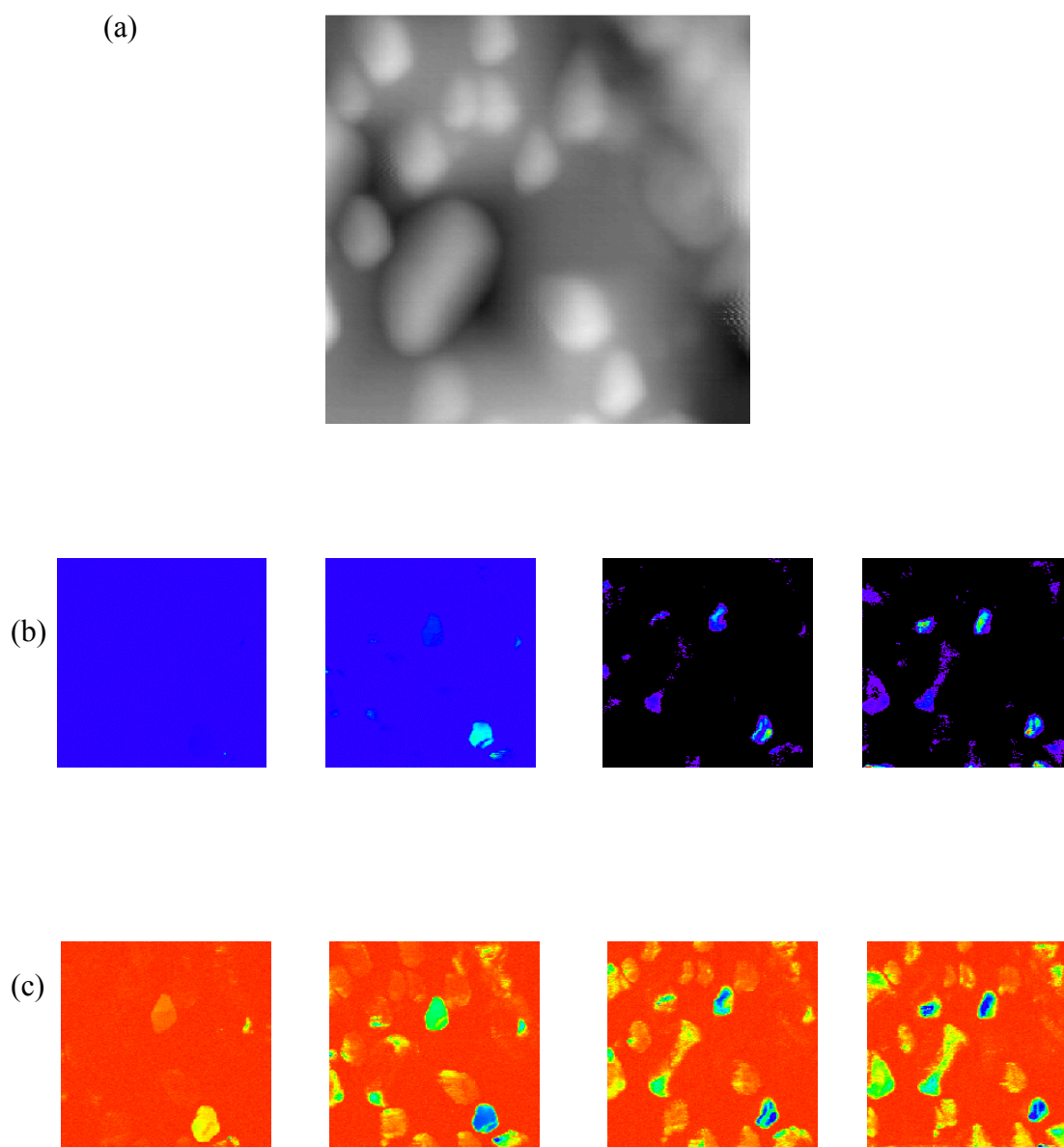


Fig. 6.7 Topography and sequence of images with different dc bias: (a) topography with scan size $0.5 \mu\text{m}$ (b) amplitude images with bias values of 0.5V, 1V, 1.5V, and 2V respectively, and (c) phase images with bias values of 0.5V, 1V, 1.5V, and 2V respectively.

Chapter 7. Single electron tunneling of nanoscale TiSi₂ islands on Si

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7.1 Abstract

Nanoscale TiSi₂ islands are formed by electron beam deposition of a few monolayers of titanium on an atomically clean silicon surface followed by *in situ* annealing at high temperatures (800-1000°C). The lateral diameter of typical islands are ~5 nm, and they form a nanoscale metal-semiconductor interface. Direct probing of the electrical characteristics of these islands was performed using ultra high vacuum scanning tunneling microscopy and scanning tunneling spectroscopy. With the vacuum between the tip and the island as a second tunnel junction, we thus form a double-junction system for observation of single electron tunneling effects such as Coulomb blockade and Coulomb staircase. Moreover, the small dimensions of the system allow room temperature observation. The experimental results are compared with the numerical fitting values and they are in good agreement. Utilizing the prediction by the standard theory, we can explain our observation within the framework of single electron tunneling. We have observed the dependence of single electron tunneling on the doping type of the

substrate. This result suggests that the nanoscale Schottky barrier in the island-substrate interface can play a role as a tunnel barrier.

7.2 Introduction

As the size of the electronic devices is continuously decreasing, the current micro-technology will eventually have to turn to nanotechnology. In terms of device size, this means that the current technology of $0.1\mu\text{m}$ will progress to 10nm devices. At the same time the basic physics of the devices will go through a transition from classical behavior to quantum effects. The new area of study often referred as mesoscopic physics has emerged [1]. There have been many new discoveries, and this field continues to develop as of today.

Although there is no clear consensus on how nanotechnology will be implemented in future applications, there is strong interest for understanding and exploration of mesoscopic phenomena. Among many options considered for mesoscopic devices, there has been a growing interest in single electronics based on single electron tunneling effects such as the Coulomb blockade and the Coulomb staircases. [2, 3].

As the dimensions of the semiconductor structures approach nanometer scale they show effects due to single electron transport properties. A nanoscale island ($d < 5\text{nm}$) between two tunnel barriers forms a double-barrier structure, which will exhibit these effects. When the energy required to add a single electron to the island becomes much larger than the thermal fluctuation energy, the electron transport is inhibited for a range of voltage. This phenomenon is known as Coulomb blockade [4]. In a double-barrier structure, each tunnel barrier is described as a parallel combination of R and C and they

are connected in series. With strongly asymmetric junctions ($R_1C_1 \gg R_2C_2$ or vice versa), as the applied bias becomes larger a stepwise increase of current in the current-voltage (I-V) relation appears in addition to the Coulomb blockade. This phenomenon is referred to as the Coulomb staircase.

The theory of single electron tunneling (SET) is based on the following assumptions [5]: First, a nanoscale island should be small enough that the charging energy of the island, e^2/C , is much larger than the thermal fluctuation energy, kT . For room temperature application, this condition, $e^2/C \gg kT$, requires the capacitance of an island to be in aF range ($a = 10^{-18}$). This translates into the size of an island being less than 5 nm. Secondly, the tunneling resistance, R_T , of the island should be larger than the quantum of resistance, R_K , $\sim 25.8 \text{ k}\Omega$, i.e. $R_T \gg R_K$. This requirement comes from the following consideration. The junction is characterized by three time scales: tunneling time, τ_t , uncertainty time, τ_c , and tunneling event time, τ_r . The tunneling time, τ_t , is roughly the time spent by the tunneling electron through the barrier ($\sim 10^{-15}$ sec). The uncertainty time is associated with the Coulomb energy $\tau_c = R_K C$ ($\sim 10^{-10}$ sec). The longest time scale is set by the tunneling resistance and the capacitance: $\tau_r = R_T C$. It is the reciprocal of the tunneling rate event for a junction biased at the Coulomb voltage e/C . The theory assumes a clear separation of time scales $\tau_t \ll \tau_c \ll \tau_r$. The first inequality states that the tunneling time is negligible while the second one states the requirement of $R_T \gg R_K$, which ensures a reasonably long lifetime of an excess electron on an island before it tunnels out of the island and onto another electrode [6]. The second inequality also implies the classical nature of the number of electrons on the island.

For the SET phenomena to be considered in future device structures, stable operation must be achieved at room temperature or higher. Although many nanostructures with double tunnel junctions have demonstrated SET at low temperature [7-9], only a few reports have successfully showed this effect at room temperature [10], [11]. The SET effects were observed in a double-barrier junction structure by tip-gold cluster-self-assembled monolayer of dithiol molecules on a Au substrate[12]. The gold cluster size was found to range between 2 and 5 nm. Other small metal clusters (less than 5 nm) such as gold [13], silver [10] or platinum [14] were deposited on an insulator/substrate forming well established double-barrier junction structures, which showed single electron tunneling effects. Also field evaporation of a tip was used to deposit gold islands on silicon by applying a short pulse between the gold tip and the silicon substrate in a scanning tunneling microscope (STM) [15]. In this case, the tunnel barrier is formed by the Schottky barrier between the metal island and the semiconductor substrate. Most room temperature SET results were observed using the spectroscopic function of a STM. In this approach, the separation between the tip and an island is used as one of the tunnel barriers (R_1 , C_1) while the island-substrate contact is the other (R_2 , C_2). The tip-island distance can be adjusted by changing the tunneling current feedback setpoint, and the I-V characteristics can be measured after freezing the feedback.

Although the prior results demonstrate SET effects, they usually suffer a lack of compatibility with current IC fabrication technology. For example, the insulating layer made of a polymer is not suitable for high temperature processes. We have previously introduced approaches to fabricate nanoscale silicide islands [16], but there has been no

reported work on single electron charging effects of nanoscale silicide islands. Our previous studies have shown that a thin layer of titanium reacts with the silicon substrate and through annealing leads to the formation of nanometer scale silicide island structures [17]. The phase transition from the metastable C49 phase to the equilibrium C54 phase was not observed in thin films of TiSi_2 [18]. Another study using STM and transmission electron microscopy (TEM) by Williams et al. confirms the presence of the C49 phase for TiSi_2 islands on Si(001) that are incommensurate [19]. It may be possible to control the growth mode of silicide islands to achieve the desired nanostructures for single electronics. However, there are still many technical hurdles to overcome to achieve precise control of the island dimensions.

Nonetheless, the TiSi_2 islands are often less than 5 nm in diameter, which is small enough to anticipate that the single electron charging effects will occur at room temperature. Our experiments were performed after forming TiSi_2 *in situ* on a Si(111)7x7 surface. The room temperature I-V results indicate Coulomb blockade and Coulomb staircases on these islands.

7.3 Experiment

The main component of the experimental setup is the ultra high vacuum STM system (Park Scientific, AutoProbe VP) with electron beam deposition, Auger electron spectroscopy (AES), and low energy electron diffraction (LEED). The system is pumped by an 230 liter/second ion pump. The base pressure of the system was better than 5×10^{-11} Torr. For deposition of the initial films, an e-beam evaporator was used with titanium of 99.99% purity. Having titanium as a target material improved the vacuum performance of

the system since while a film was deposited it was also deposited onto the chamber wall, therefore, effectively functioning as a titanium sublimation pump. Typical surface analysis tools such as AES and LEED are also incorporated into the system enabling routine surface analysis available. The LEED uses a Perkin-Elmer/PHI 11-020 LEED control electronics. The LEED images are projected onto a phosphor screen, which is located in front of the filament. Images are obtained using either a traditional camera or digital imaging equipment, which are mounted above the optics. The Auger unit consists of a Perkin-Elmer/PHI 11-500 Auger system control. We use the existing LEED optics as a retarding field analyzer by applying an alternating electric field between the grids and the chassis ground. A separate high voltage DC power supply is used to initiate the Auger process. A load-lock pumped by a turbo pump is used for sample introduction without breaking vacuum. A magnetically coupled transfer mechanism is used for sample movement and tip exchange. The whole system rests on an air suspension table for vibration reduction during STM operation.

Various combinations of substrates were used for this study: n-type and p-type wafers with a doping concentration of $N = 10^{17} \text{ cm}^{-3}$ for either type. The sample was scribed into rectangles of 0.3 cm x 1.5 cm and then fastened onto the sample holder. The sample holder is designed for direct current heating for flashing and annealing.

After several hours of outgassing at 600 °C (usually overnight), the sample was flashed at 1200 °C for duration of 30 to 120 seconds. The temperature was measured with an optical pyrometer operating at 0.9 μm with the emissivity of silicon about 0.65. Care was taken to keep the chamber pressure below 2×10^{-9} Torr during the flashing. The

pressure generally rises sharply after the temperature reaches 1200 °C and slowly returns to the base pressure. However, as the surrounding material becomes warmer the pressure again rises slowly. Hence, flashing was repeated as necessary in order to maintain the chamber pressure below 2×10^{-9} Torr. The reconstructed 7×7 surface, confirmed by LEED and STM, was achieved after the heat cleaning. STM revealed that there was no contamination on the surface as several scans of the surface with scan size up to a few microns showed no particular features on the surface other than steps. The clean surface was used as a starting surface for the subsequent titanium deposition.

Titanium was deposited with the substrate at room temperature by electron beam evaporation. The distance from the e-beam source to the substrate is 40 cm. The deposition rate was measured using a quartz crystal monitor. The crystal monitor was positioned next to the substrate using the feedthrough with bellows. The nominal deposition rate used for this study was 0.2nm/min for thicknesses varying from 1 to 2 monolayers. Following the deposition, the sample was annealed for 30 ~ 60 seconds at temperatures of 800, 900, and 1000°C. The ramping time from room temperature to the desired temperature was less than 10 seconds.

STM images obtained right after the annealing show large thermal drift. It usually takes several hours after each annealing before the images show acceptable minimal drift (≤ 1 nm/min) as measured from successive images. The typical thermal drift in our system was about ~ 20 nm/min an hour after annealing. The STM images were obtained in the constant current mode with a tunneling current between 0.5 to 1 nA, and a bias varying from -2 to 2 V. After identifying an appropriate island, I-V spectroscopy was obtained on

the island with the feedback loop frozen. For each I-V spectra, the signals were averaged from 5 to 10 times. Since it was suggested that oscillation of the system could lead to artificial current oscillation [20], I-V data were also obtained with different ramping rates to distinguish artifacts from real effects. We have occasionally observed similar oscillation artifacts, and these oscillations were discarded. The typical voltage range for the I-V measurements were from -3V to 3V. The I-V data was numerically differentiated to display dI/dV spectra.

7.4 Results

In TiSi_2 formation, there is a transition from the metastable C49 phase to the stable C54 phase upon annealing. However when the thickness of the film is less than 25 nm, the resulting TiSi_2 island phase is C49, and the transition from the C49 to the C54 phase is not observed [18]. Thus, it is assumed that for the thin titanium layer in our experiments, the islands are the C49 phase. A recent study using STM and transmission electron microscopy (TEM) by Williams et al. confirms the presence of the C49 phase of TiSi_2 for incommensurate islands on Si(001)[19].

Shown in Fig. 7.1 are the STM images of TiSi_2 islands obtained after annealing at 800 and 900 °C for 0.1 nm Ti deposition, respectively. After annealing at 900 °C, the average island size increases from that of 800 °C due to island coalescence and/or Ostwald ripening [17, 21]. The size distributions are given in Fig. 7.2.

In Fig. 7.3 (a) and (b), we show the single electron tunneling effect in the I-V spectra for TiSi_2 islands with ~5nm in diameter. The I-V curves were obtained with various ramping rates, and when the SET effect was observed it was independent of

ramping rate. We show results from islands with either n- or p-type substrate. For the n-type substrate, the conductance peak is more obvious for positive sample bias while, for the p-type substrates, the peak is present for negative sample bias. In Fig. 7.4 (a) and (b), we show I-V and dI/dV curves obtained from an island formed on a substrate with a Si epi-layer. The intrinsic Si layer was epitaxially deposited on n atomically clean silicon surface at 550 °C in a separate MBE system before titanium deposition and subsequent annealing take place in the STM chamber. The series of steps in the I-V curve are clearly observed on both sides of polarities in this case.

The conductance peaks show a dependence on the doping type of the substrates. This is evident as clear conductance peaks on the reverse biased side compared to the less obvious peaks on the forward biased side. Nevertheless, it is remarkable that conductance peaks are present for both polarities for the substrate with the additional intrinsic Si layer.

Using the double-barrier junction model [5], a least square fit of the I-V results was obtained as shown in Fig. 7.5. Overall, the Coulomb blockade behavior is well reproduced from the model fit while it failed to show the higher voltage current steps. In the following sections, we will discuss the significance of the silicide-silicon interface as a tunnel barrier, and the dependence of the SET on the extra layer of intrinsic silicon.

7.5 Discussion

7.5.1 On nanoscale m-s tunnel barrier

Most previous studies of SET at room temperature have employed an insulator as a tunnel barrier between the metallic island and the semiconducting substrate [10, 14] while the STM forms the second tunnel junction. One of the goals of this study was to

determine whether the Schottky barrier formed between the island and the silicon substrate could act as a tunnel barrier, thereby enabling SET effects. A silver nanoparticle on Sb-passivated silicon surface showed SET effects at room temperature [10]. A small silver island that is located near densely populated islands showed SET while the densely populated islands showed metallic behavior. The authors claimed that SET may be due to the lateral tunneling barrier between the islands rather than the tunneling barrier formed in the metal-semiconductor Schottky barrier [20]. Contrary to the above study in the case of silver particles on silicon, our STM images show that TiSi_2 islands are well separated from each other. Hence, lateral tunneling may not play a significant role in our case.

Although there have been no prior studies of SET effects utilizing a Schottky barrier itself as a tunnel barrier, our analysis indicates that SET effects should be possible for this nanostructure. Our results indicate that SET effects such as Coulomb blockade and Coulomb staircase are observed in the tip-metallic island-semiconductor double-barrier junction structures. These phenomena were observed in substrates with both doping types. The general trend is that the conductance peaks are more obvious when the metal-semiconductor interface is reverse biased regardless of the type of the substrate.

This phenomenon can be explained with a band model of the double junction structures by including the Schottky barrier for one junction and the vacuum gap as another. When the sample is biased positively in the n-type case, the metal-semiconductor interface is reverse biased as shown in Fig. 7.6 (b). It should also be noted that most of the bias voltage is applied on the vacuum gap, i.e. $V_1 > V_2$ at all times [22]. The reverse biased Schottky barrier height does not change significantly as the voltage is

swept. Therefore the established tunnel barrier height is almost constant throughout the voltage sweep in reverse bias. However when the polarity is reversed as in Fig. 7.6 (c), the Schottky barrier is in forward bias, and the barrier height for the electrons to go over the barrier is reduced. Thus, more electrons will transit over the barrier, i.e. thermionic emission is encouraged in forward bias. For the p-type substrate, the situation is reversed. The Schottky barrier is forward biased when the sample is positively biased. This argument explains the trend seen in Fig. 7.3 well, where conductance peaks are more obvious on reverse biased side for types of substrates.

As we add an undoped silicon layer between the silicide island and the doped substrate, more conductance peaks appear on the reverse biased side while peaks on forward bias also become visible. We consider two possible explanations for this behavior in terms of the resistance and the capacitance, respectively. First, we are increasing the resistance of the metal-semiconductor tunnel barrier by adding an intrinsic silicon layer. Even though the total resistance of the system did not increase significantly compared with the case of no silicon layer, the resistance between the island and the substrate is expected to increase slightly. The increased electron confinement time in the island will therefore lead to the observation of more conductance peaks in both polarities.

Another argument is in terms of the capacitance of the island. The capacitance of the island can be estimated assuming the island as a sphere between a conducting plane (substrate) and another sphere (the STM tip). The approximate solution to the sphere-plane capacitance is

$$C(R, s) = 2\pi\epsilon R(2+R/s)$$

where R is the radius of the sphere and s is the distance between the sphere and the plane [23]. As the distance between the island and the substrate increases, it results in a decrease of the island capacitance. In addition, the total capacitance of the island in our system includes depletion capacitance of the space charge region, which is dependent on the bias voltage. When the bias voltage is increased, the total capacitance, which is given as a series combination of the geometric capacitance and the depletion capacitance, will decrease also. This reduces the capacitance of the island and makes the charging energy larger.

Even though the exact role of the intrinsic layer is not clear at this time, the above arguments and experimental observation tend to agree.

7.5.2 Estimates from simple model and fitting

As noted above, we can model the tip-island-substrate structure as a pair of tunnel junctions in series. Each tunnel junction is modeled as a combination of a resistor and a capacitor in parallel. From the value of the distance of the steps in Fig. 4 (a) and (b), $\Delta V \sim 0.5$ V, we can estimate the total capacitance for the tip-island-substrate system as $C_{\text{total}} = e/\Delta V \sim 3.2 \times 10^{-19}$ F. We also note that from the point of view of the charge on the island, two capacitors are connected in parallel. Assuming the island as a perfect sphere in vacuum with a diameter of 4 nm, we can estimate the lower limit of the total capacitance of the island to be $C_{\text{total}} \sim 2.2 \times 10^{-19}$ F which is given by the self capacitance of a sphere in free space, $C = 4\pi\epsilon_0 R$. Obviously, in our situation we will obtain a higher value. For the tip and island, C_1 can be estimated using the image charge method assuming two spheres with the same radius [24]. This gives a value of $C_1 \sim 5.8 \times 10^{-19}$ F

for a 4nm diameter and a 1nm separation. On the other hand, assuming a sphere and a plane, C_2 , for the island-substrate junction, the C_2 is found as $\sim 4.4 \times 10^{-19}$ F for a sphere with a 4nm diameter and a 1nm separation [23]. Thus $C_{\text{total}} = C_1 + C_2$ from this calculation is found to be 1.0×10^{-18} F which is somewhat higher than the value of self-capacitance and the experimental value. This approach gives reasonable agreement despite the crude assumptions.

Another requirement for the charging effect is that both R_1 and R_2 are larger than the quantum of resistance, 25.8 k Ω and their magnitudes should be asymmetric to be able to observe the charging effect. We can estimate the R_{total} by inspecting the current at 2.5V for example. The current value of 5 nA at this voltage gives $R_{\text{total}} \sim 500$ M Ω . Our conducting AFM measurements in contact on a larger island ($d \sim 0.1 \mu\text{m}$) gave a contact resistance, R_2 , on the order of several M Ω . Since $R_{\text{total}} = R_1 + R_2$, we can approximate that $R_{\text{total}} \sim R_1$. This satisfies not only the requirement for long lifetime of the trapped electron, but also the asymmetry of the junctions ($R_1 C_1 \gg R_2 C_2$) that is necessary for the observation of the Coulomb staircase.

7. 6 Conclusion

We have successfully fabricated nanoscale TiSi_2 islands on an atomically clean Si(111) 7x7 surface. The island size distributions are dependent on processing parameters such as the initial deposition thickness, and the annealing temperature and time. Islands of ~ 5 nm diameter showed Coulomb blockade and Coulomb staircase effects at room temperature. These phenomena can be explained in terms of single electron charging of a metallic island in the tip-island-substrate double junction system.

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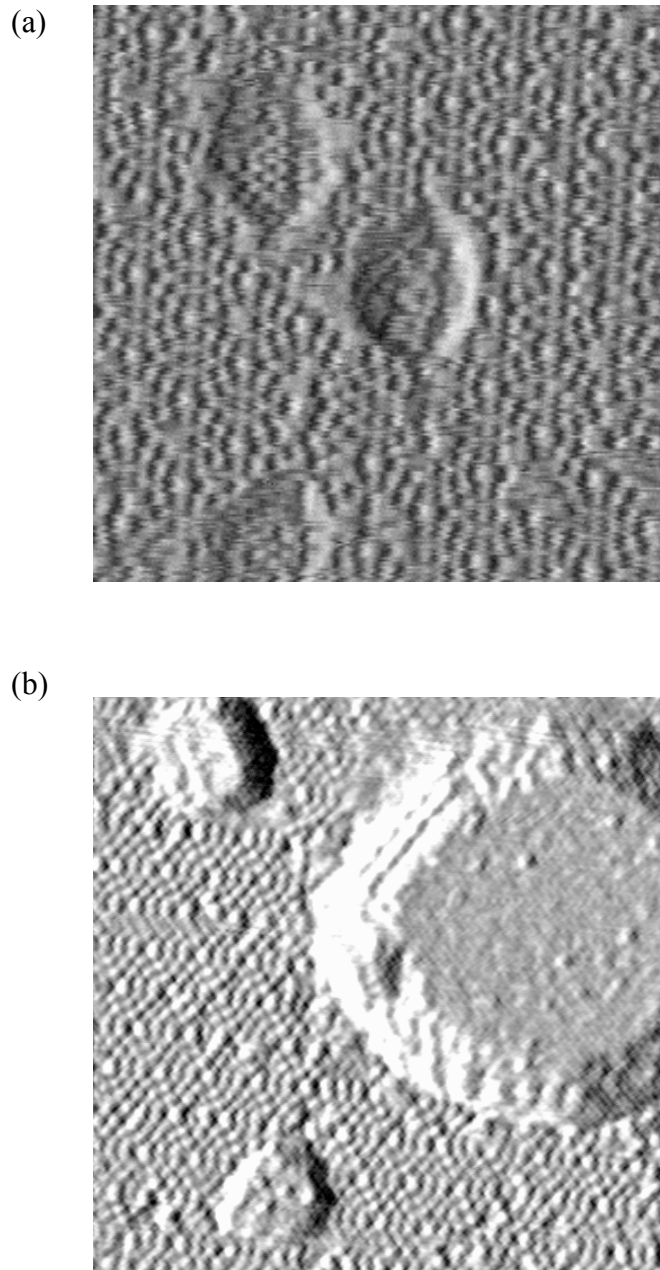


Fig. 7.1 STM images of TiSi_2 islands on a Si(111) surface.(a) After annealing at $800\text{ }^\circ\text{C}$, scan size is $30 \times 30\text{ nm}^2$. (b) After annealing at $900\text{ }^\circ\text{C}$, scan size is $40 \times 40\text{ nm}^2$.

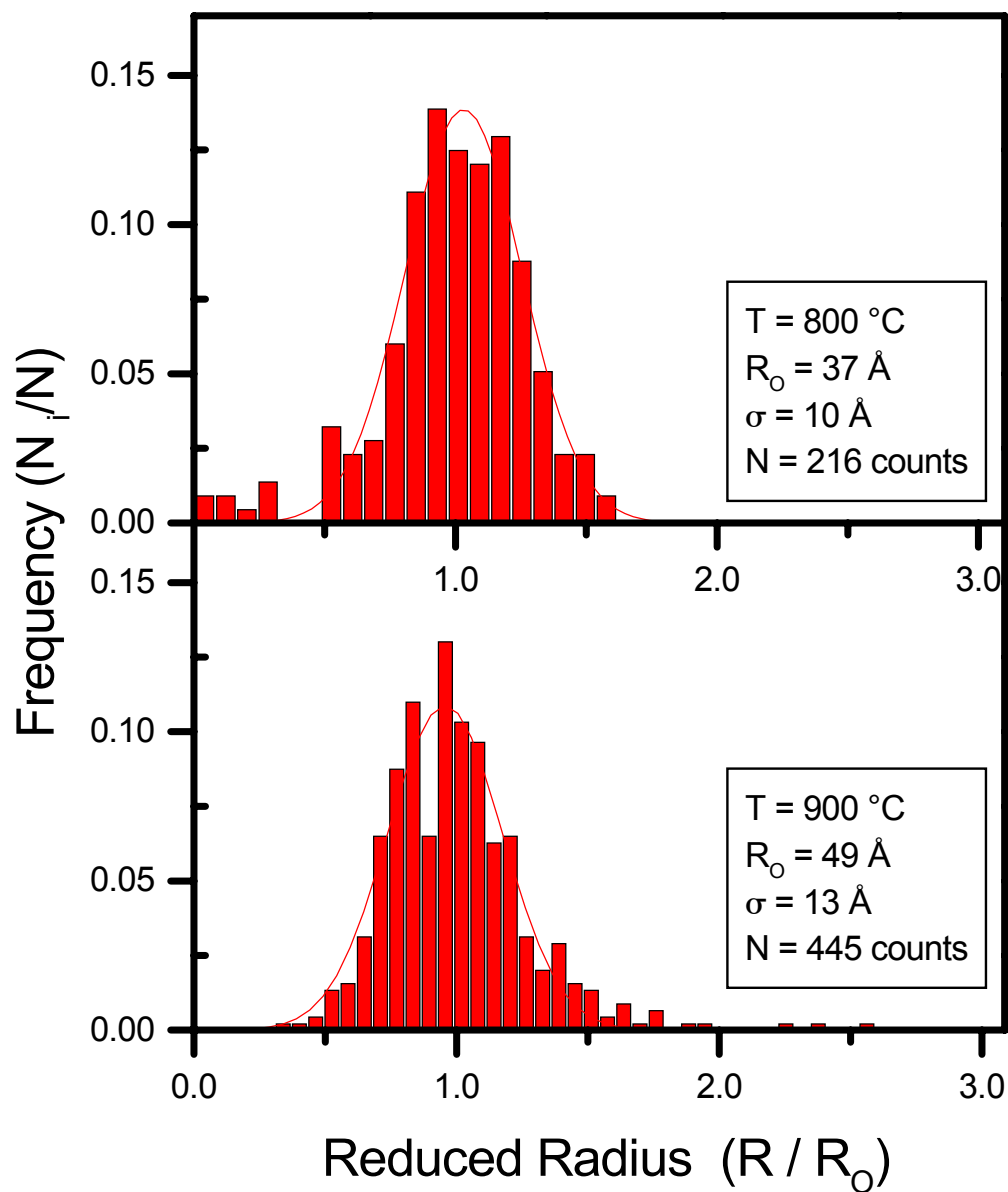


Fig. 7.2 Island size distribution from 0.2 nm Ti deposition on a Si(111) surface. The distribution was obtained by analysis of STM images with scan size $0.5 \times 0.5\text{ }\mu\text{m}^2$.

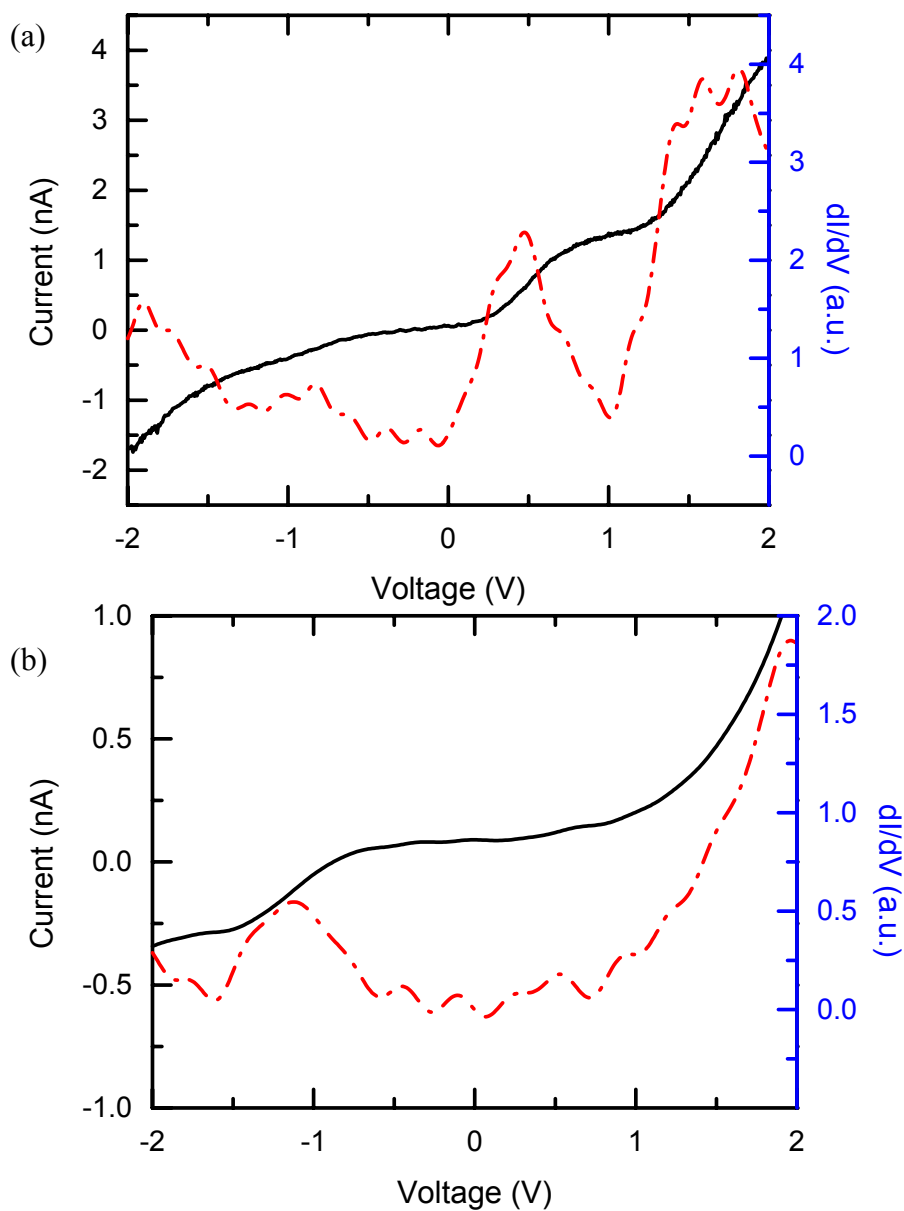


Figure. 7.3 (a) I-V and dI/dV spectrum of an island on an n-type substrate, displaying conductance peak in positive sample bias. (b) I-V and dI/dV of an island on p-type substrate, conductance peak in negative sample bias less obvious. Each I-V curves were numerically differentiated to obtain dI/dV .

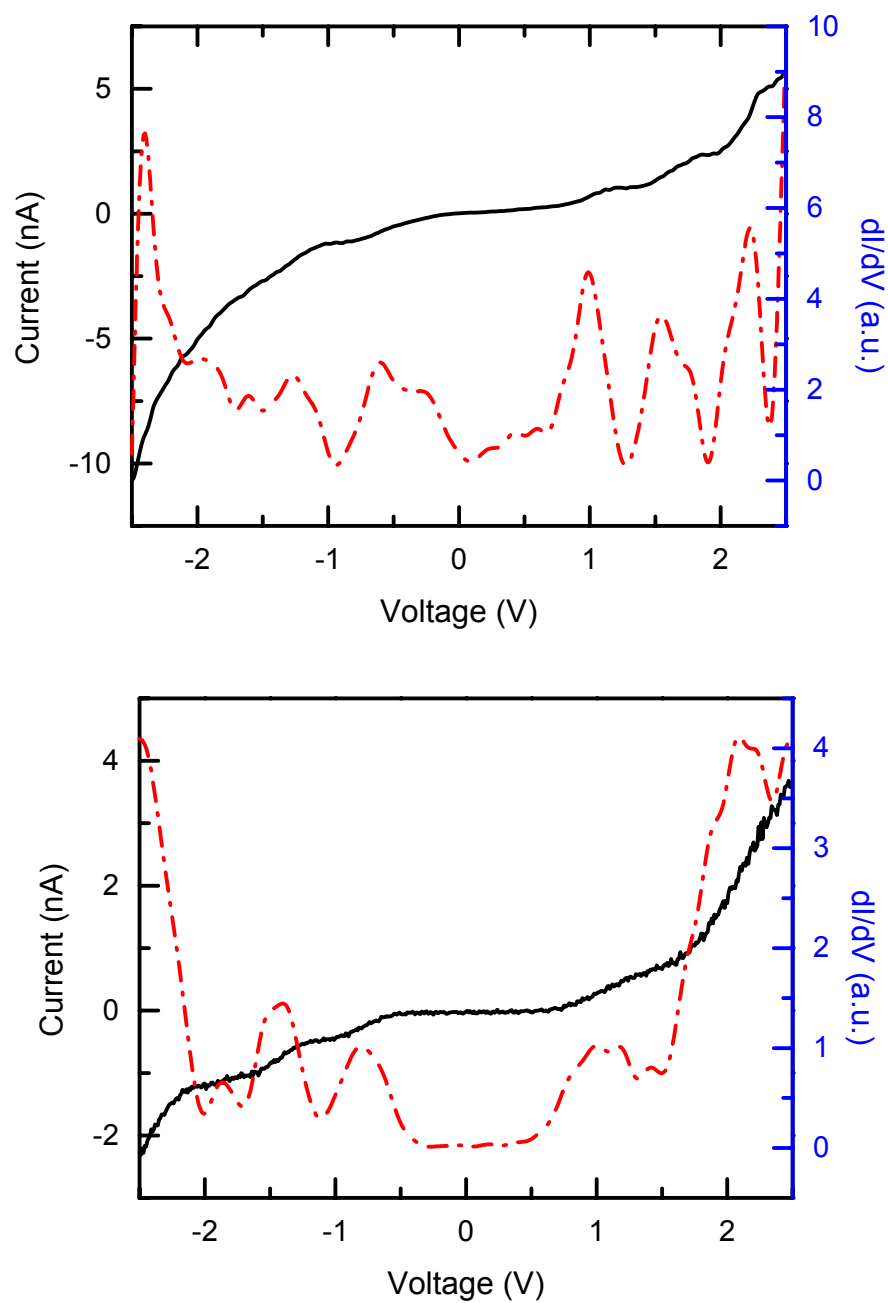


Figure. 7.4 I-V and dI/dV spectrum of an island on an n-type substrate with a 3nm intrinsic Si buffer layer(a), on a p-type substrate with a 5nm buffer layer (b).

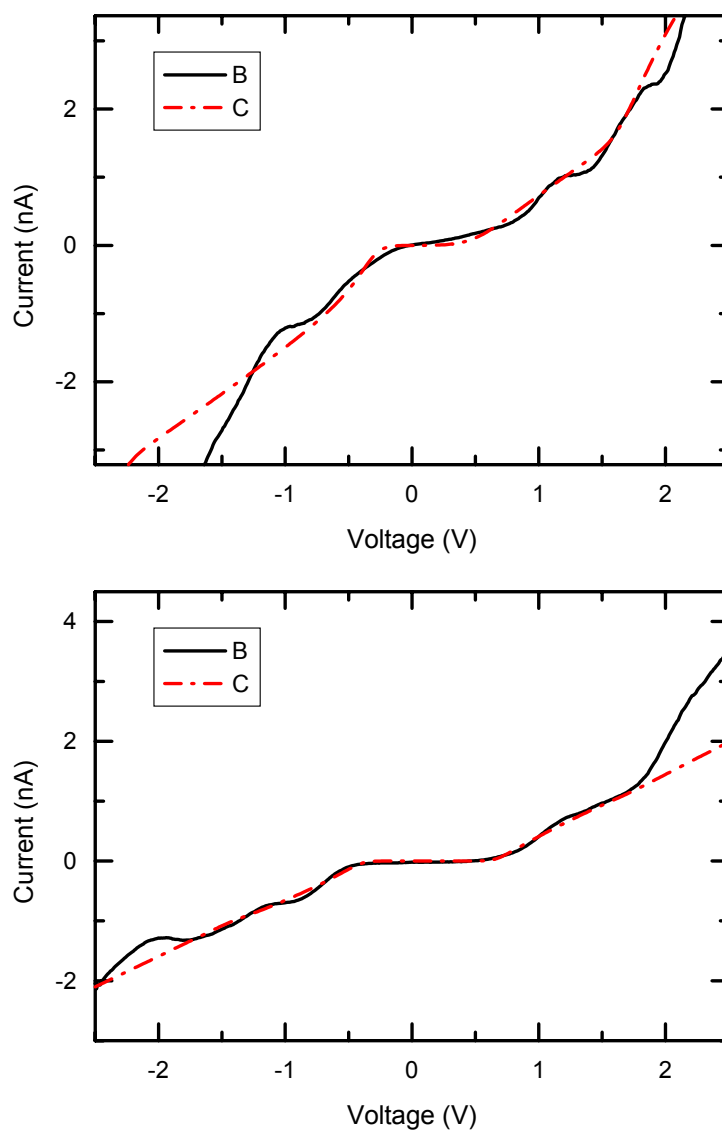


Fig. 7.5 Experimental I-V result (from Fig. 7.4) and a least square fit from the model show good agreement at low voltage but deviate from each other at higher voltage.

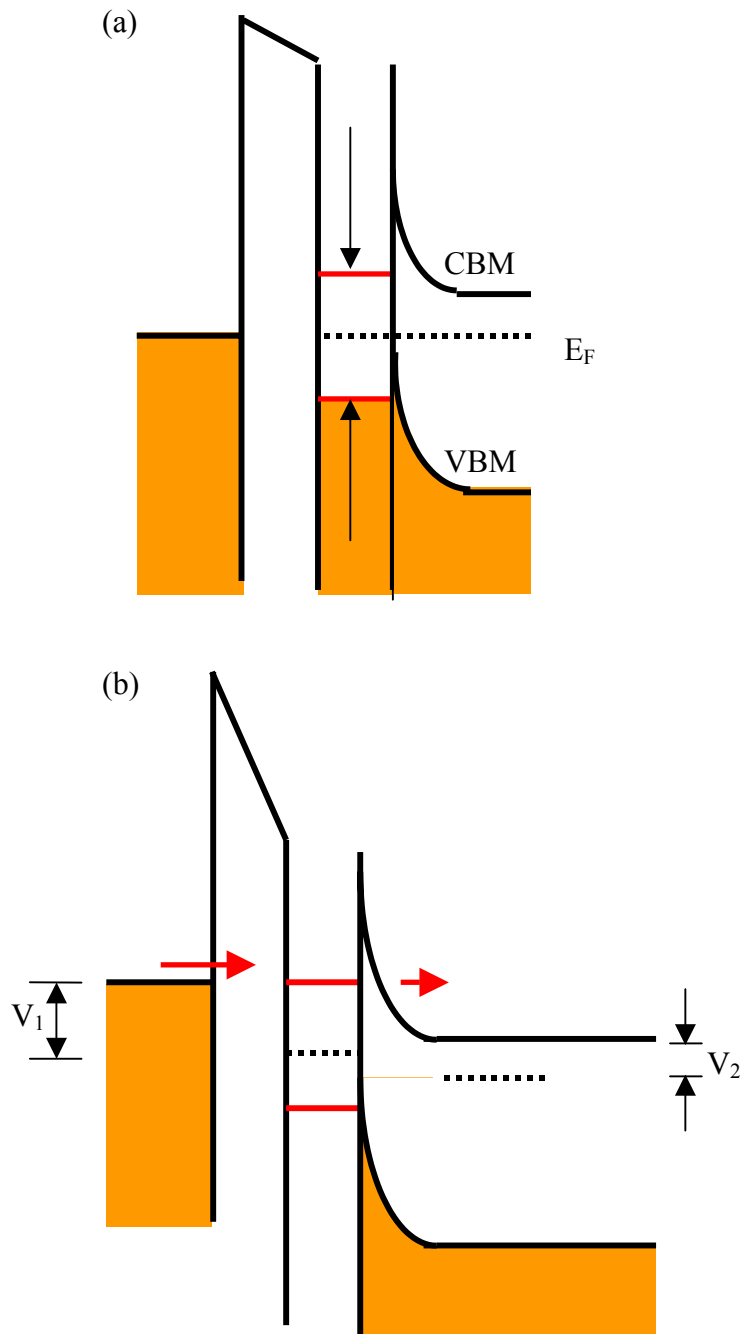


Fig. 7.6 Experimental model of a metallic island. (a) with no bias in equilibrium
(b) positive sample bias; metal-semiconductor interface is reverse biased

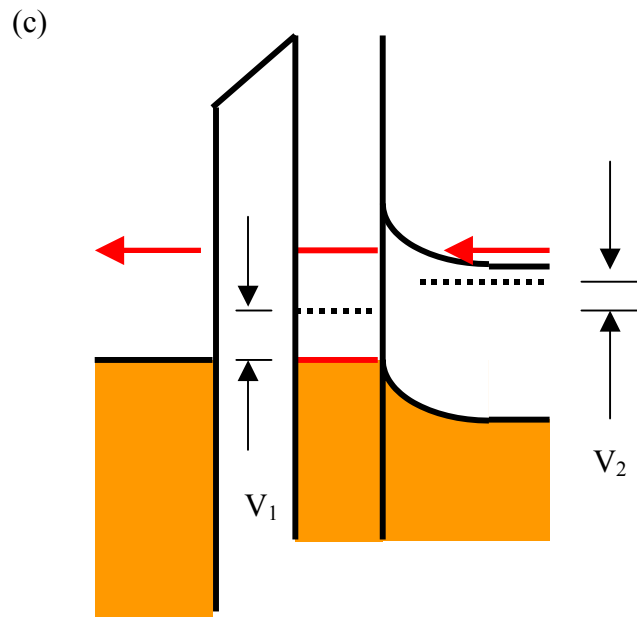


Fig. 7.6 (continued)

(c) negative sample bias; metal-semiconductor interface is forward biased.

Chapter 8. Summary and future works

We have studied the electrical characteristics of nanometer scale silicide island structures by c-AFM and UHV-STM. Specifically, we have measured the local I-V characteristics of TiSi_2 nanoscale islands of diameters from $0.1\mu\text{m}$ to $1\mu\text{m}$ using c-AFM. The Schottky barrier heights of these sub-micron islands have been measured. High ideality factors have been discussed in light of several possible transport mechanisms. It was observed that the reduced SBH for many islands had no direct correlation with the size of the islands. For reduced SBH, several mechanisms were suggested.

We also have developed a new imaging method that enables one to identify the areas of different conductivities using a lock-in detection technique. The resulting map of differential conductivities of the surface can be combined with the results from the I-V measurement to give a more detailed picture of sub-micron Schottky barriers. In the future, we may be able to achieve a combination of these two techniques.

We have also investigated the electrical properties of TiSi_2 islands that are less than 5 nm in diameter using STM. These TiSi_2 islands are small enough to anticipate the single electron charging effects to occur at room temperature. Our experiments were performed after forming TiSi_2 *in situ* on a $\text{Si}(111)7\times 7$ surface. The room temperature I-V results indicate Coulomb blockade and Coulomb staircase effects on these islands. In addition we have observed the dependence of these effects on the doping type of the substrates. The general trend is that the conductance peaks are more obvious when the metal-semiconductor interface is reverse biased regardless of the type of the substrate. These findings indicate that the nanoscale Schottky barrier can be used as a tunnel barrier

for single electron tunneling devices. Therefore it would be obvious to follow up with a different combination of materials systems such as a wide band gap semiconductor with a higher Schottky barrier metal as a top layer.

As we add an undoped silicon layer between the silicide island and the doped substrate, more conductance peaks appear on the reverse biased side while peaks on forward bias also become visible. Even though the exact role of the intrinsic layer is not clear at this time, we may further investigate these aspects.