

ABSTRACT

PARK, JINSEOK. Sample-Data Modeling for Double Edge Current Programmed Mode Control in High Frequency and Wide Range DC-DC Converters. (Under the direction of Dr. Alex Huang.)

This dissertation focuses on sample-data modeling for double edge current programmed mode control (DECPCM) and its application to high frequency and wide range DC-DC converters. Steady state conditions and subharmonic oscillation issues for DECPCM are addressed. By combining the conventional peak and valley current programmed mode control, a sample-data model for DECPCM is proposed. A small signal model for DECPCM is developed by deriving the modulation gains (F_m) and the sampling gains (H_e) for DECPCM from the proposed sample-data model. The sampling frequency dependence on the duty ratio and a large current loop gain at high frequency for DECPCM are emphasized. The analytical results are verified by the simulation. Finally, DECPCM is proposed as a method to control the high frequency and wide range DC-DC converters. A $10MHz$ four switch buck boost converter is implemented with DECPCM to verify the viability of its application to high frequency and wide range converters.

© Copyright 2010 by Jinseok Park

All Rights Reserved

Sample-Data Modeling for Double Edge Current Programmed Mode Control in High
Frequency and Wide Range DC-DC Converters

by
Jinseok Park

A dissertation submitted to the Graduate Faculty of
North Carolina State University
in partial fulfillment of the
requirements for the Degree of
Doctor of Philosophy

Electrical Engineering

Raleigh, North Carolina

2010

APPROVED BY:

Dr. Subhashish Bhattacharya

Dr. Doug Barlage

Dr. Kevin G. Gard

Dr. Alex Huang
Chair of Advisory Committee

DEDICATION

To my wife,

Hana Lee

and my parents,

Jongkyu Park and Younghee Suh

BIOGRAPHY

The author, Jinseok Park, was born in Daegu, Korea, on Oct. 6th. 1974. He received his B.Sc. degree from Kyungpook National University, Daegu, Korea, in 2000, and his M.Sc. degree from Pohang University of Science and Technology (POSTECH), Kyungbuk, Korea, in 2002, both in electrical engineering. He is working towards the Ph.D degree at the Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC. His research interests include analog and mixed signal IC design for power management applications and control modeling.

ACKNOWLEDGEMENTS

I wish first to thank my advisor, Dr. Huang, who brought me into this research area and continuously supported me throughout my Ph.D study. His extensive knowledge, broad vision and creative thinking have been a source of inspiration for me through my entire study and research work. I would also like to extend my gratitude to Dr. Bhattacharya, Dr. Gard and Dr. Barlage, for serving on my committee. Their knowledge in different fields is a valuable resource to my research work. I am indebted to the past friends and colleagues Dr. Xin Zhang, Dr. Heifei Deng, Dr. Xiaoming Duan, Dr. Xiaojun Xu, Mr. Ding Li, Dr. Yan Gao, Mr. Hongtao Mu, Mr. Ning Zhu, Mr. Jifeng Qin, Dr. Jeeseung Jung for their stimulating conversations and friendship. Here, I would like to express my special thanks to Mr. Jiwei Fan and Mr. Xiaopeng Wang. They are not only great partners, but also friends who are always willing to provide me help and encouragement. It would not be possible to complete this research project without their contributions. Of course, my gratitude goes out to all members of the Semiconductor Power Electronics Center (SPEC), including Mr. Sungkeun Lim, Mr. Sung, Woongje, Mr. Sunghun Baek, Mr. Jun Wang, Mr. Xin Zhou, Mr. Liyu Yang, Ms. Rong guo, Mr. Gurava Bawa, Ms. Jingzhen Hu, Mr. Pochih Lin, Mr. Anand Ramamurthy. We shared the good times working and studying in SPEC. My heartfelt thanks belong to my wife, Hana Lee. She supported me with her brilliant ideas and soothing manner. Her love accompanied me through ups and downs. Last but certainly not least, I would like to thank my parents, Jongkyu Park and Younghee Suh for their endless support, love and interest throughout my academic career. I certainly would not have been successful without them.

TABLE OF CONTENTS

List of Tables	vii
List of Figures	viii
Chapter 1 Introduction	1
1.1 Background : Wide range and High Frequency Applications for DC-DC converters	1
1.2 Dissertation Outline	4
Chapter 2 Review of the conventional Current Programmed Mode Control (CPM)	6
2.1 Introduction : Current Programmed Mode Control	6
2.2 Steady State condition and Subharmonic Oscillation	8
2.3 Sample-data modeling	14
2.3.1 Sample-data current feedback transfer function	16
2.4 Small Signal Model for CPM	17
2.4.1 Modulation gain (F_m) derivation	19
2.4.2 Sampling gain (H_e) derivation	20
Chapter 3 Double Edge Current Programmed Mode Control	24
3.1 Introduction: background and previous works on double edge modulation	24
3.2 Steady State condition and Subharmonic Oscillation	31
3.3 Sample-data modeling	37
3.3.1 Sample-data current feedback transfer function	37
3.3.2 Comparisons of current feedback transfer function	46
3.4 Small Signal Model for DECPM	48
3.4.1 Modulation gain (F_m) derivation	49
3.4.2 Sampling gain (H_e) derivation	50
3.4.3 Simulation results of DECPM and its comparison with the conventional single CPM	53
Chapter 4 Design of 10MHz CMOS 4 Switch Buck Boost Converter (4SBBC) with DECPM control	60
4.1 Architecture	61
4.2 Transistor level implementation	65
4.2.1 Current sensor	65
4.2.2 Ramp Generator	69
4.2.3 System summary	72

4.3 Measurement	74
Chapter 5 Power Stage Optimization of the 4SBBC for the Polar Modulation Application	80
5.1 Loss Breakdown of the 4SBBC	81
5.2 Polar modulation and EDGE standard	93
5.3 Average Efficiency and power stage optimization of 4SBBC with EDGE envelope signal	97
Chapter 6 Conclusions	106
6.1 Future works	108
References	116

LIST OF TABLES

Table 3.1	F_{ms} in different current programmed control	50
Table 3.2	$H_e s$ in different current programmed control	52
Table 4.1	Design parameters for 4SBBC	72

LIST OF FIGURES

Figure 1.1	Supply voltages to the components in the portable battery-powered electronic devices	2
Figure 2.1	Peak Current Programmed Mode control(CPM) (without ramp) block diagram	7
Figure 2.2	Peak Current Programmed Mode control(CPM) (with ramp) block diagram	9
Figure 2.3	Steady state waveform of the sensed inductor current in Peak CPM with ramp signal	10
Figure 2.4	Steady-state and perturbed sensed inductor current waveforms in peak CPM	11
Figure 2.5	α_p and α_v at the function of duty cycle without artificial ramp .	13
Figure 2.6	Peak CPM waveforms	15
Figure 2.7	Small signal model for CPM	18
Figure 2.8	Modulation in peak CPM	19
Figure 2.9	PWM switch model and current loop with fixed voltages	22
Figure 3.1	Trailing edge modulation	25
Figure 3.2	Leading edge modulation	25
Figure 3.3	Double edge modulation	25
Figure 3.4	Sampling scheme of the PWM comparator:(a) trailing-edge PWM, and (b) double-edge PWM.	26
Figure 3.5	G_{vc} with double edge-PWM in SIMPLIS simulation: (a) duty cycle is 50%, and (b) duty cycle is 10%.	27
Figure 3.6	The schematics of the pulse width modulators.	28
Figure 3.7	The transient waveforms with the pulse width modulators	29
Figure 3.8	Two sided latched PWM shematics	30
Figure 3.9	Steady state inductor current waveform in DECPM	31
Figure 3.10	Steady-state and perturbed inductor current waveforms	33
Figure 3.11	α , α_p and α_v at the function of duty ratio without ramp signal ($M_a = 0$)	35
Figure 3.12	α at the function of duty ratio with different ramp signals having the slopes of M_a ($K = M_a/M_2$)	36
Figure 3.13	Double edge current programmed mode waveforms	39
Figure 3.14	v_c to $R_i \cdot i_L$ responses when $V_{in} = 3.3V$ and $V_{out} = 0.1V$	43
Figure 3.15	v_c to $R_i \cdot i_L$ responses when $V_{in} = 3.3V$ and $V_{out} = 1.65V$	44
Figure 3.16	v_c to $R_i \cdot i_L$ responses when $V_{in} = 3.3V$ and $V_{out} = 3.2V$	44
Figure 3.17	v_c to $R_i \cdot i_L$ responses when $V_{in} = 3.3V$ and $V_{out} = 3.4V$	45

Figure 3.18	v_c to $R_i \cdot i_L$ responses when $V_{in} = 3.3V$ and $V_{out} = 5V$	45
Figure 3.19	v_c to $R_i \cdot i_L$ responses when $V_{in} = 3.3V$ and $V_{out} = 6.6V$	46
Figure 3.20	Small signal model for DECPM	48
Figure 3.21	G_{vc} when $V_{in} = 3.3V$ and $V_{out} = 0.1V$	54
Figure 3.22	G_{vc} when $V_{in} = 3.3V$ and $V_{out} = 1.65V$	54
Figure 3.23	G_{vc} when $V_{in} = 3.3V$ and $V_{out} = 3.2V$	55
Figure 3.24	G_{vc} when $V_{in} = 3.3V$ and $V_{out} = 3.4V$	55
Figure 3.25	G_{vc} when $V_{in} = 3.3V$ and $V_{out} = 5V$	56
Figure 3.26	G_{vc} when $V_{in} = 3.3V$ and $V_{out} = 6.6V$	56
Figure 3.27	G_{vc} in Peak CPM with different output voltage	57
Figure 3.28	G_{vc} in DECPM with different output voltage	58
Figure 3.29	G_{vc} in Peak CPM with different input voltage	58
Figure 3.30	G_{vc} in DECPM with different input voltage	59
Figure 4.1	Block diagram of 4SBBC	63
Figure 4.2	Implemented key signal waveforms for DECPM (a) Buck mode (b) Boost mode	64
Figure 4.3	LXA and Vsense for Buck and Boost mode	66
Figure 4.4	Current Sensor with the Differential Difference Amplifier	66
Figure 4.5	Transistor level schematic of the Differential Difference Amplifier for the current sensor	68
Figure 4.6	Input and output voltage of the current sensor at Buck mode	69
Figure 4.7	Input and output voltage of the current sensor at Boost mode	70
Figure 4.8	Ramp Generator circuit	71
Figure 4.9	SIMPLIS results of the voltage regulation loop gains ($T_2 _{DECPM}$) with the different output voltages when $V_{in} = 3.3V$	73
Figure 4.10	Micro photograph of the chip	75
Figure 4.11	Evaluation board for 4SBBC	76
Figure 4.12	Measurement of the V_{out} , LXA and LXB node with the different V_{in} (a) $V_{in}=2.8V$ (b) $V_{in}=3.3V$ (c) $V_{in}=4V$ (d) $V_{in}=4.7V$	77
Figure 4.13	Measurement of the V_{out} , LXA and LXB nodes at $V_{in} = 3.3V$ (a) When V_{out} change from 2V to 4V (b) When V_{out} change from 4V to 2V	78
Figure 4.14	Measured waveforms of the V_{ref} , V_{out} , and switching nodes waveforms with 100kHz sinusoidal reference (V_{ref}) at $V_{in} = 3.3V$	79
Figure 5.1	4SBBC power stage diagram	81
Figure 5.2	Curve fitting result for PMOS R_{dson}	82
Figure 5.3	Voltage drop model for M_D	84
Figure 5.4	Diode voltage(V_{diode}) and R_{dson} voltage drop(V_{DS}) across the M_D switch	84

Figure 5.5	Duty ratio comparison between Eq.(5.3) and ideal case	86
Figure 5.6	test bench for C_{iss}	89
Figure 5.7	Power loss breakdown @ $V_{in} = 3.3V$	90
Figure 5.8	Efficiency vs. V_{out} with different W_A and W_D when $W_B = W_C = 23mm$	91
Figure 5.9	Efficiency comparison between calculation and simulation @ $V_{in} = 3.3V$	92
Figure 5.10	Efficiency comparison between calculation and measurement @ $V_{in} = 3.3V$	92
Figure 5.11	Block diagram of polar modulation with buck boost converter as a envelope modulator	94
Figure 5.12	EDGE signal in time domain (provided by RFMD)	95
Figure 5.13	EDGE signal in frequency domain	96
Figure 5.14	Efficiency and the histogram of the EDGE envelope signal @ $V_{in} = 3.3V$	97
Figure 5.15	output voltage and the corresponding instantaneous efficiency in time domain @ $V_{in} = 3.3V$	98
Figure 5.16	Average efficiency with respect to W_B and W_C when $W_A = W_D = 69mm$	99
Figure 5.17	Average efficiency with respect to W_B and W_C when $W_C = 24mm, W_A = W_D = 69mm$ and $W_B = 24mm, W_A = W_D = 69mm$, respectively .	100
Figure 5.18	Average efficiency with respect to W_A and W_D when $W_B = W_C = 23mm$	101
Figure 5.19	Average efficiency with respect to W_A and W_D when $W_C = 72mm, W_B = W_C = 23mm$ and $W_A = 72mm, W_B = W_C = 23mm$, respectively .	101
Figure 5.20	Average efficiency with respect to W_A and W_D with $W_B = \frac{W_A}{3}, W_C = \frac{W_D}{3}$	103
Figure 5.21	Average efficiency with respect to W_A and W_D with $W_B = \frac{W_A}{2}, W_C = \frac{W_D}{2}$	103
Figure 5.22	Average efficiency with respect to W_A and W_D with $W_B = W_A, W_C = W_D$	104
Figure 5.23	Average efficiency with respect to W_A and W_D with $W_B = 2 \times W_A, W_C = 2 \times W_D$	105
Figure 6.1	Simulink time domain test bench for CPM	109
Figure 6.2	Simulink time domain test bench for DECPM	110
Figure 6.3	Quasi DC simulation of CPM with 3nsec internal delay	111
Figure 6.4	Control signals of CPM with 3nsec internal delay	111
Figure 6.5	Control signals of CPM in buck mode with 3nsec internal delay .	111
Figure 6.6	Control signals of CPM in boost mode with 3nsec internal delay .	111
Figure 6.7	Quasi DC simulation of CPM with 5nsec internal delay	112

Figure 6.8	Control signals of CPM with 5nsec internal delay	112
Figure 6.9	Control signals of CPM in buck mode with 5nsec internal delay .	112
Figure 6.10	Control signals of CPM in boost mode with 5nsec internal delay .	112
Figure 6.11	Quasi DC simulation of DECPM with 20nsec internal delay . . .	114
Figure 6.12	Control signals of DECPM with 20nsec internal delay	114
Figure 6.13	Control signals of DECPM in buck mode with 20nsec internal delay	114
Figure 6.14	Control signals of DECPM in boost mode with 20nsec internal delay	114
Figure 6.15	Quasi DC simulation of DECPM with 55nsec internal delay . . .	115
Figure 6.16	Control signals of DECPM with 55nsec internal delay	115
Figure 6.17	Control signals of DECPM in buck mode with 55nsec internal delay	115
Figure 6.18	Control signals of DECPM in boost mode with 55nsec internal delay	115

Chapter 1

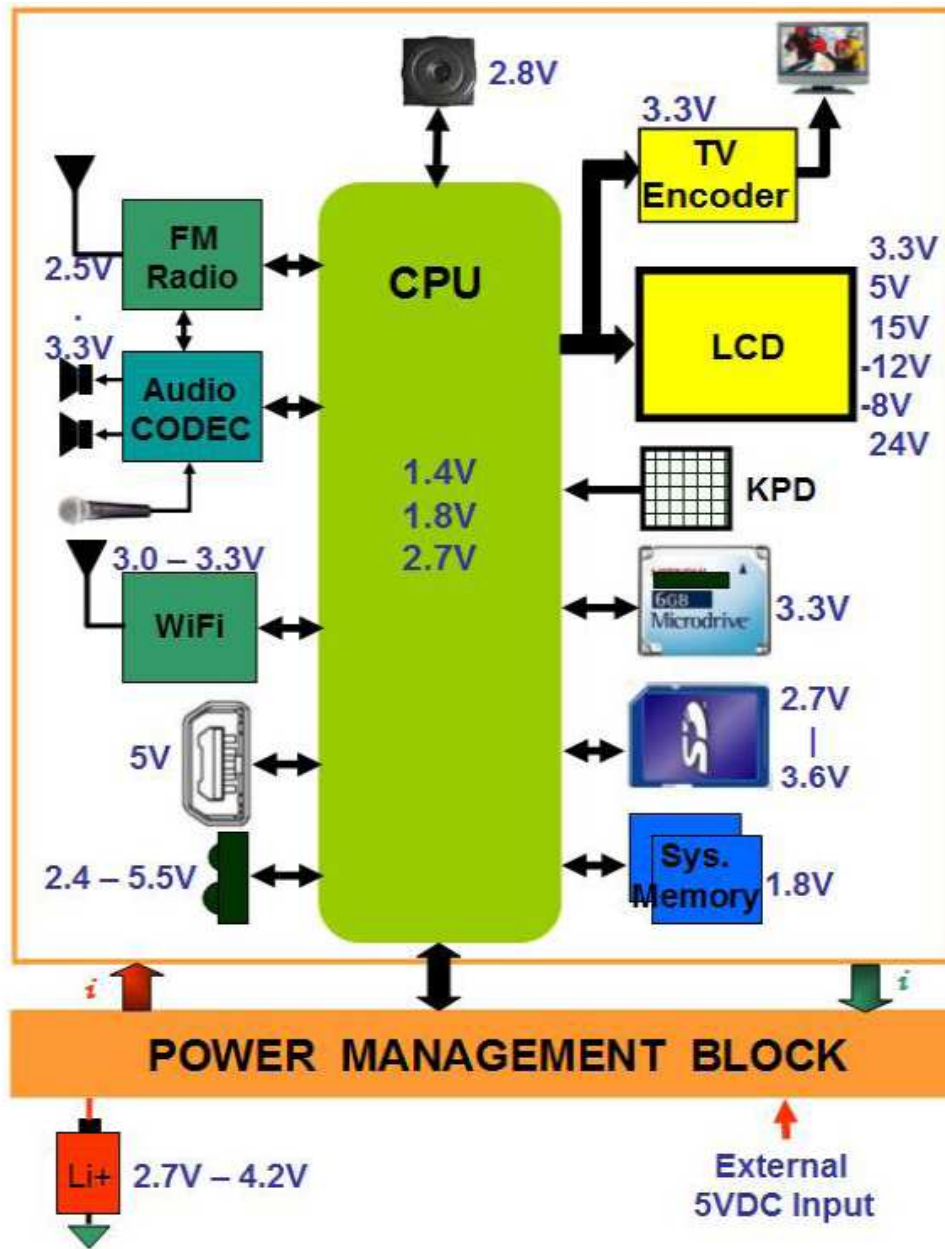
Introduction

1.1 Background : Wide range and High Frequency Applications for DC-DC converters

There is an ever-increasing demand for small power supplies capable of working with wide voltage range which uses the battery as a source. These applications are automotive [1], portable battery-powered electronic devices [2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19], and power factor correction (PFC) [20, 21].

Fig. 1.1 shows typical power supply rails used in the common portable battery-powered electronic devices. As shown in this figure, the battery voltage change from 4.2V to 2.7V and each components in the system needs the fixed or variable voltage irrespective of the battery voltage. In order for the system to have stable operation with wide voltage variation, the wide range DC-DC converter is necessary.

Currently, most controller of the wide range converter is compensated by external components which are out of the controller IC. TI's TPS54362 and Maxim's MAX8655 are the examples. When the operation range for these are determined, the compensation



Source : http://www.freescale.com/files/training_pdf/VFTF09_AC109.pdf

Figure 1.1: Supply voltages to the components in the portable battery-powered electronic devices

network is designed by the end users according to the worst case condition. This conventional design may lose the performance at other operating conditions and need the end users to discover the suitable compensation network to make the converter work stable. However, if the controller can make the power plant transfer functions as constant as possible for all operating points, the aforementioned issues are solved. That is that a fixed compensator can make the converter operate stable with higher performance and that the fixed compensator can be integrated into the controller for the end users not to think of designing a proper compensator.

It is well known that the line regulation of the current programmed mode control is superior to that of voltage mode control. It also has been reported that the conventional current programmed mode control shows the smooth transition between CCM (Continuous Conduction Mode) and DCM (Discontinuous Conduction Mode) [22]. It is shown in [22] that when using current-mode control, there is little change in either the stability margin or the closed-loop performance when crossing the boundary between continuous and discontinuous mode of operation. These characteristics shows that the conventional current programmed mode control is suitable to the wide voltage range converter.

Power density and response speed are important performance metrics in DC-DC power converters for mobile applications [23]. Both of these metrics can be improved by increasing the switching frequency of the converters. The higher switching frequencies are allowed to use the small valued passive components which make the physical size of the converters. These smaller passive components provide faster response to change in operating conditions with the help of a shorter switching period. This faster response is very crucial on some applications such as envelope modulator for polar modulation applications. Therefore, there has been strong motivation to move to increased switching frequencies if losses, switch driving, control, and other design challenges can be addressed.

This dissertation proposes a new double edge current mode control (DECPCM) for wide range and high frequency application. Detail analysis on the proposed DECPCM will be addressed and the physical implementation of the DECPCM into the high frequency 10MHz 4 switch buck boost converter will be shown. Therefore, DECPCM will be verified to overcome the aforementioned issues such as stable operation with wide voltage range and high frequency operation.

1.2 Dissertation Outline

In chapter 2, the conventional current programmed mode control (CPM) is reviewed. The steady state condition and the subharmonic issues are derived again. The sample-data model of the peak CPM is revisited and its small signal model is shown by deriving the modulation gain (F_m) and sampling gain (H_e). The Ridley's method is used for this modeling.

Chapter 3 introduces the double edge current program mode control (DECPCM) and its modeling. This chapter starts from the derivation the steady state conditions and the subharmonic oscillation issues. A sample-data model for DECPCM is proposed by mathematically combining the conventional peak CPM and valley CPM models. The dependence of the sampling frequency on the duty ratio is analyzed through this modeling. A small signal model for DECPCM is developed by deriving the modulation gains (F_m) and sampling gains (H_e). The proposed DECPCM model is compared with the conventional single CPM by SIMPLIS simulations. The larger current loop gain at high frequency for DECPCM than single CPM will be verified. This large current loop gain introduces DECPCM to the high frequency and wide range DC-DC converter applications, and this is demonstrated by the measurement results of the implemented 10MHz CMOS 4 switch

buck boost converter (4SBBC) in chapter 4.

Chapter 4 shows the architecture of the 4SBBC which is made of JAZZ $0.5\mu m$. This chapter also show the detail design of the key blocks for the 4SBBCS such as current sensor and ramp signal generator. The measurement results show that the implemented 4SBBC with DECPM works well with a switching frequency of $10MHz$ and with with wide range input and output voltage.

Chapter 5 show the power stage optimization of the 4SBBC for polar modulation application. Differ from the conventional DC-DC applications, the output voltage of the 4SBBC changes dynamically for the polar modulation. This chapter briefly introduces the polar modulation application for the DC-DC converter and the characteristics of the EDGE signal which is used as a reference signal to the 4SBBC. This chapter shows the detail power loss break-downs of the 4SBBC and its power stage optimization based on average energy efficiency for the EGDE signal.

Chapter 6 is the conclusion of the whole dissertation and the list of future works.

Chapter 2

Review of the conventional Current Programmed Mode Control (CPM)

2.1 Introduction : Current Programmed Mode Control

Current Programmed Mode control (CPM) is widely accepted and used in industry due to its inherent over-current protection, superior dynamic response, and ease of implementation of current sharing [22, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33]. Current Programmed Mode control (CPM) is also called as current mode control. CPM can be divided into peak CPM and valley CPM depending on the modulation scheme. As expected from the naming, the peak CPM modulates the PWM signal by limiting the peak value of the sensed inductor current signal and the valley CPM does it by limiting the valley value of the sensed inductor current signal.

Fig.2.1 shows a block diagram of the conventional CPM which is specifically a peak

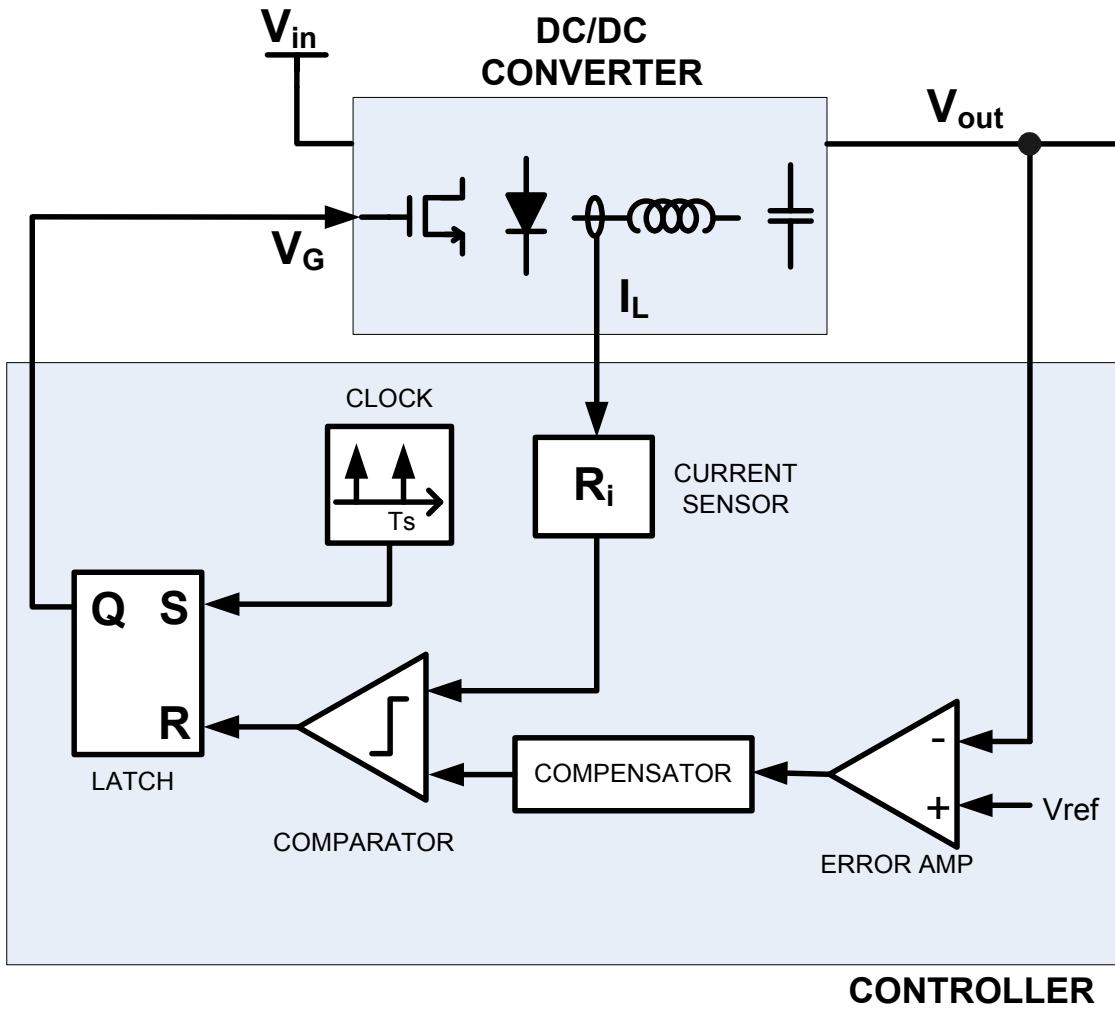


Figure 2.1: Peak Current Programmed Mode control(CPM) (without ramp) block diagram

CPM. Different from voltage mode control, CPM does not have saw tooth signal to modulate the PWM duty signal. Instead of the saw tooth signal, CPM uses the inductor current signal to modulate the PWM duty signal. In the Peak CPM, the power switch is turned off when the sensed inductor current is larger than control signal (v_c) which is the output of compensator in Fig. 2.1 [34][24]. As a result, the peak point of the sensed inductor current is controlled and this modulates the PWM duty signal.

Because of the well known subharmonic oscillation problem when duty cycle is larger than 0.5 in peak CPM [34], the conventional CPM needs a ramp signal added in the control loop. Fig.2.2 is a modified peak CPM block diagram with an additional ramp generator. In the steady state, the peak point of the sensed inductor current is limited by the control signal (v_c) and the ramp signal which is shown in Fig.2.3.

This chapter will revisit the conventional peak CPM. The steady state conditions are shown, and the subharmonic oscillation issue and its solution will be revised first. The sample-data modeling of the peak CPM will be shown here again. The step-by-step derivations of the sample-data modeling of the peak CPM is revisited and the bandwidth limitation due to the sample-hold effect at the switching frequency is shown.

2.2 Steady State condition and Subharmonic Oscillation

In this section, the steady state condition and subharmonic oscillation problem of the peak CPM are revisited.

Fig.2.3 shows the steady state waveforms of the sensed inductor current ($R_i \cdot i_L$), control signal (v_c) and ramp signal. Here, R_i is the gain of the current sensor, and the ramp signal with the slopes of M_a are added to the control signal (v_c) to control the peak

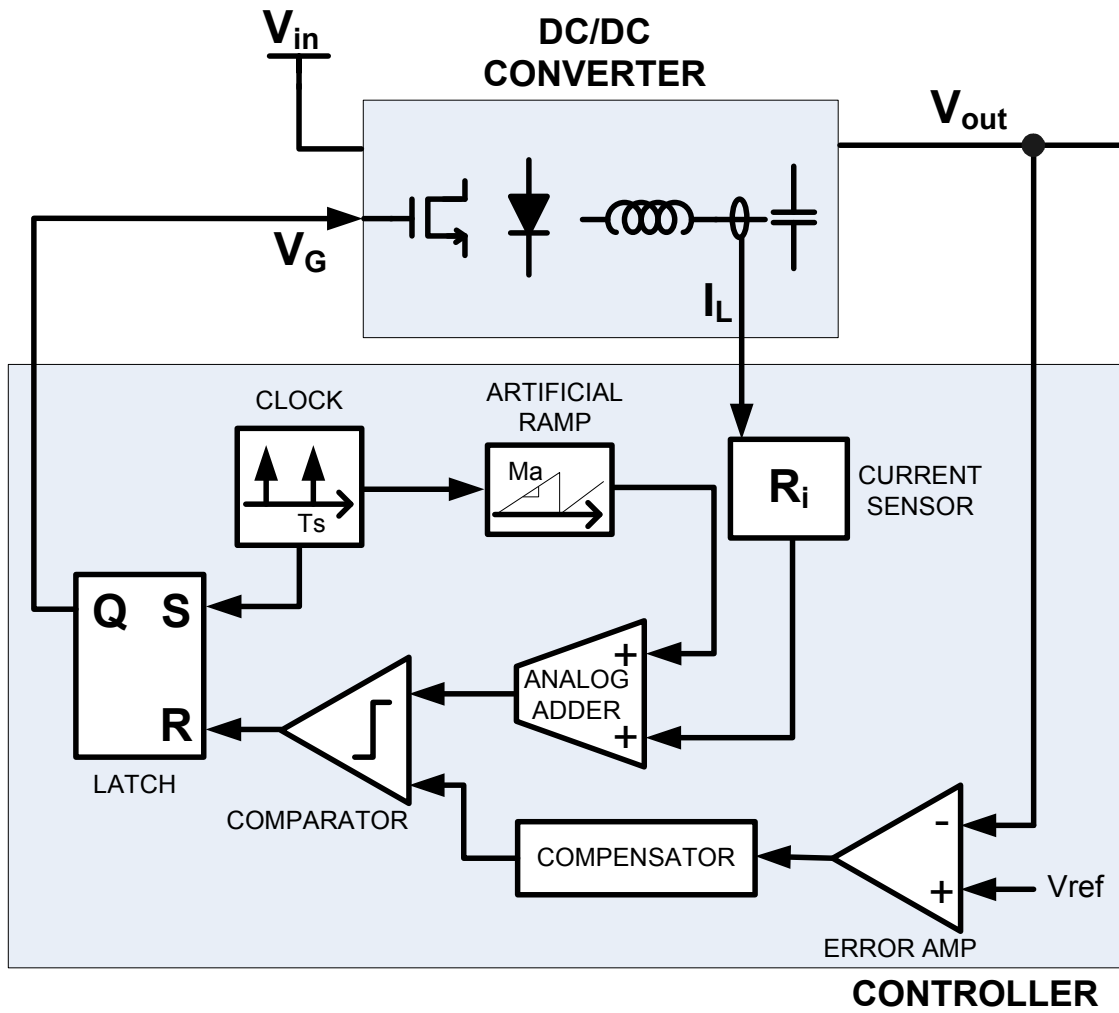


Figure 2.2: Peak Current Programmed Mode control(CPM) (with ramp) block diagram

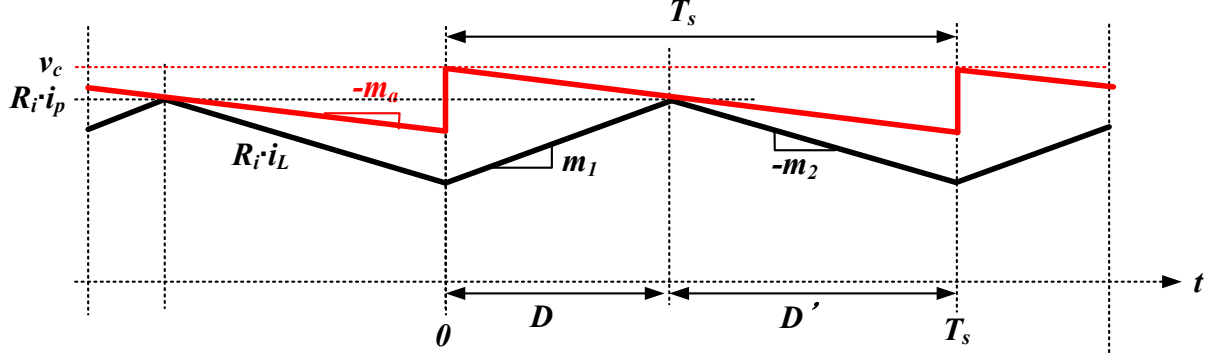


Figure 2.3: Steady state waveform of the sensed inductor current in Peak CPM with ramp signal

value of the sensed inductor current. From the Fig.2.3, the peak ($R_i \cdot i_p$) of the sensed inductor current are derived in terms of the control signal (v_c), the rising slope of the sensed inductor current (M_1) and duty (D).

$$R_i \cdot i_p = R_i \cdot i_L(DT_s) = v_c - m_a DT_s = R_i \cdot i_L(0) + m_1 DT_s \quad (2.1)$$

To see the steady state condition of the sensed inductor current ($R_i \cdot i_L$), the relationship of the sensed inductor currents between the adjacent switching periods are derived as shown below.

$$\begin{aligned} R_i \cdot i_L(T_s) &= R_i \cdot i_p - m_2 D' T_s \\ &= R_i \cdot i_L(0) + m_1 DT_s - m_2 D' T_s \end{aligned} \quad (2.2)$$

In steady state, the condition of $R_i \cdot i_L(T_s) = R_i \cdot i_L(0)$ should be satisfied. Thus, the

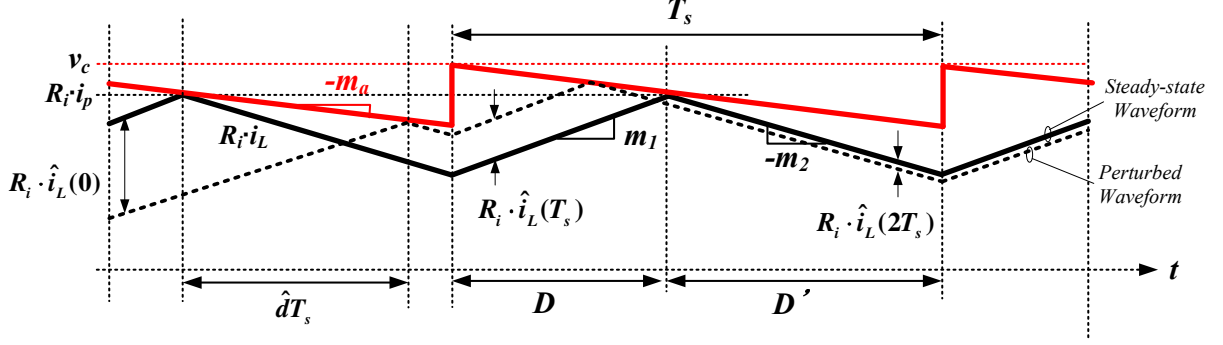


Figure 2.4: Steady-state and perturbed sensed inductor current waveforms in peak CPM

steady state condition of peak CPM is derived from (2.2), and is

$$\frac{m_2}{m_1} = \frac{D}{D'} \quad (2.3)$$

For analyzing the subharmonic oscillation issues [34] in peak CPM, the sensed inductor current is perturbed as shown in Fig. 2.4. Then, the subharmonic oscillation conditions can be derived from the natural response of the sensed inductor current perturbation ($R_i \cdot \hat{i}_L$).

From the simple trigonometric analysis of Fig. 2.4, the following equations are derived.

$$R_i \cdot \hat{i}_L(0) = m_a \hat{d}T_s + m_1 \hat{d}T_s = (m_1 + m_a) \hat{d}T_s \quad (2.4)$$

$$R_i \cdot \hat{i}_L(T_s) = m_a \hat{d}T_s - m_2 \hat{d}T_s = -(m_2 - m_a) \hat{d}T_s \quad (2.5)$$

From the above two equations, the following is derived directly.

$$\hat{i}_L(T_s) = -\frac{m_2 - m_a}{m_1 + m_a} \hat{i}_L(0) \quad (2.6)$$

By generalizing (2.6) with arbitrary timing, and it is

$$\begin{aligned}\hat{i}_L(nT_s) &= -\frac{m_2 - m_a}{m_1 + m_a} \cdot \hat{i}_L((n-1)T_s) \\ \hat{i}_L(nT_s) &= \alpha_p \cdot \hat{i}_L((n-1)T_s)\end{aligned}\quad (2.7)$$

$$\alpha_p = -\frac{m_2 - m_a}{m_1 + m_a}, \quad 1 - \alpha_p = \frac{m_1 + m_2}{m_1 + m_a} \quad (2.8)$$

(2.7) is a inductor current perturbation relationship between the adjacent switching periods in peak CPM. Here, α_p is the inductor current attenuation factor for the peak CPM. By using the steady state condition of peak CPM in (2.3), α_p in (2.8) is rewritten in terms of the duty ratio, the slope of ramp signal and the falling slope of the sensed inductor current as shown below.

$$\alpha_p = \frac{1 - \frac{m_a}{m_2}}{\frac{D'}{D} + \frac{m_a}{m_2}} \quad (2.9)$$

By doing similar derivation, the inductor current attenuation factor for the valley CPM (α_v) is derived like following.

$$\alpha_v = -\frac{m_1 - m_a}{m_2 + m_a} \quad (2.10)$$

$$= \frac{\frac{D'}{D} - \frac{m_a}{m_2}}{1 + \frac{m_a}{m_2}} \quad (2.11)$$

It is well known that, without the ramp signals ($M_a = 0$), α_p for peak CPM and α_n for valley CPM become larger than 1 when $D > 0.5$ and $D < 0.5$ respectively, which causes subharmonic oscillation. The inductor current attenuation factors of the peak and valley CPM without the ramp signals ($M_a = 0$) are derived below and showed in Fig.

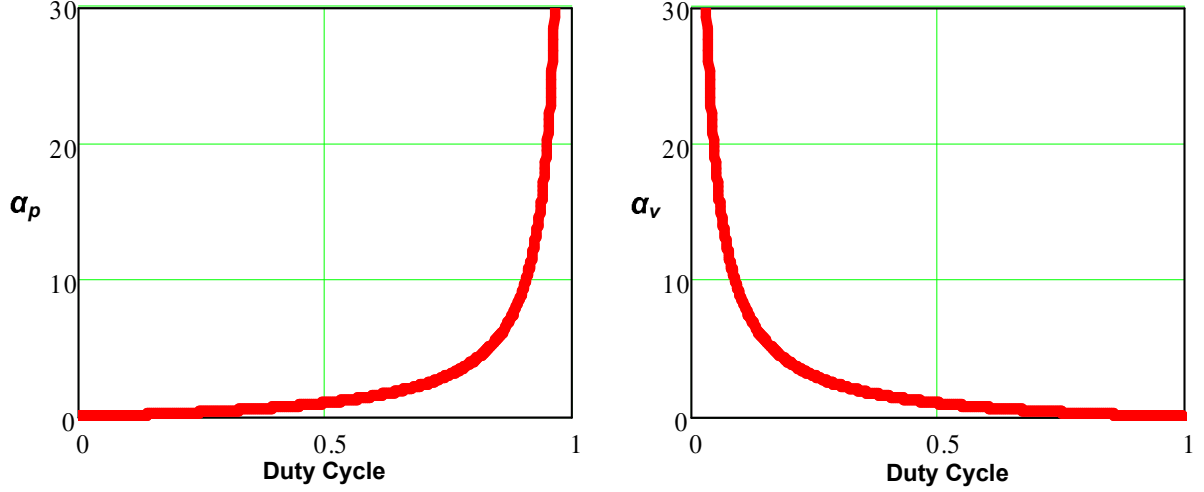


Figure 2.5: α_p and α_v at the function of duty cycle without artificial ramp

2.5.

$$\alpha_p|_{M_a=0} = \frac{D}{D'} \quad (2.12)$$

$$\alpha_v|_{M_a=0} = \frac{D'}{D} \quad (2.13)$$

To avoid subharmonic oscillations for the entire duty range, the inductor current attenuation factors should be less than 1 for all operating conditions (i.e. for all duty ratios). This is done by adding the ramp signal with an appropriate slope (m_a). One common choice of the m_a in peak CPM not to have subharmonic oscillation for all duty range is

$$m_a = \frac{1}{2} m_2 \quad (2.14)$$

With this choice of the m_a , $|\alpha_p| < 1$ for $0 \leq D < 1$ and $\alpha_p = -1$ at $D = 1$. This is the minimum value of m_a which make the system stable for all duty cycles. [34]

2.3 Sample-data modeling

There has been much research on control modelings for high frequency converters which can predict up to half the switching frequency [35, 36, 37, 24, 32, 31, 25]. In order to model the current programmed mode control accurately to high frequency including the sample and hold effects, the sample-data model is popular and widely accepted [24, 32, 31]. During this section, the sample-data modeling technique of the Ridley's method [24] to derive the current feedback transfer function of the peak CPM is reviewed. After this derivation, a popular small signal model of the peak CPM is used to derive the modulation gain (F_m) and sampling gain (H_e) by comparing with the derived the sample-data current feedback transfer function, which can apply to design the compensator for the outer voltage loop (T_2).

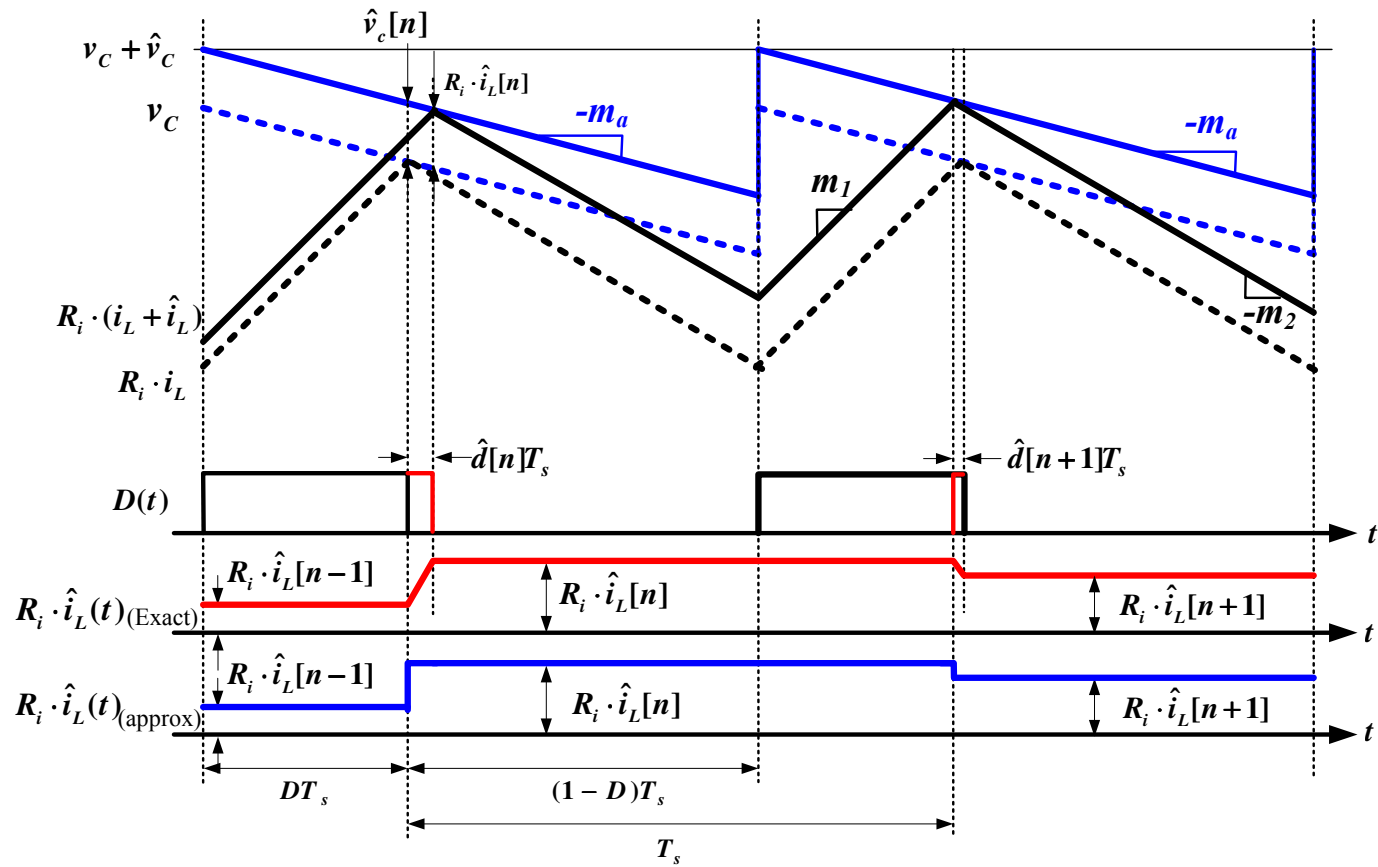


Figure 2.6: Peak CPM waveforms

2.3.1 Sample-data current feedback transfer function

Fig. 2.6 shows the waveforms to derive the sample-data model for the peak CPM. This figure shows the modulated duty signal (\hat{d}) and the sensed inductor current perturbation ($R_i \cdot \hat{i}_L$) as the results of the control signal perturbation (\hat{v}_c). As shown in Fig. 2.6, it can be observed that the sensed inductor current ($R_i \cdot \hat{i}_L$) is updated once in one switching period (T_s). The inductor current perturbation happens only once in each switching period and is held for one switching period [24]. This makes the sampling frequency of the control the same as the switching frequency of the power stage. Therefore, the conventional CPM (here, peak CPM) has a fixed switching frequency in the power stage and a fixed sampling frequency for the control. For this reason, the switching frequency and the sampling frequency of the conventional CPM is considered as a same.

For the following peak CPM modeling, the voltages applied across the inductor are kept constant and the current feedback loop is closed [24]. By using simple trigonometric analysis at the time of $(n - D)T_s$ from Fig. 2.6, the following two equations are derived.

$$R_i \cdot \hat{i}_L[n] = R_i \cdot \hat{i}_L[n - 1] + (m_1 + m_2)\hat{d}[n]T_s \quad (2.15)$$

$$\hat{v}_c[n] = R_i \cdot \hat{i}_L[n - 1] + (m_1 + m_a)\hat{d}[n]T_s \quad (2.16)$$

By eliminating $\hat{d}[n]T_s$ and combining (2.15) and (2.16), the following equation is derived.

$$R_i \cdot \hat{i}_L[n] = -\frac{m_2 - m_a}{m_1 + m_a} R_i \cdot \hat{i}_L[n - 1] + \frac{m_1 + m_2}{m_1 + m_a} \hat{v}_c[n] \quad (2.17)$$

With the definition of the inductor current attenuation factor of peak CPM (α_p) in (2.9),

(2.17) can be rewritten and it is

$$R_i \cdot \hat{i}_L[n] = \alpha_p \cdot R_i \cdot \hat{i}_L[n-1] + (1 - \alpha_p) \cdot \hat{v}_c[n] \quad (2.18)$$

This (2.18) is the well known discrete time inductor current dynamics of the peak CPM which shows the relation of the sensed inductor current perturbation ($R_i \cdot \hat{i}_L$) and the control signal perturbation (\hat{v}_c) during one switching period of T_s [32].

By applying the Z-transform equivalent to (2.18), the discrete time current feedback transfer function of the peak CPM in Z-domain is derived and it is

$$\frac{R_i \cdot \hat{i}_L[n]}{\hat{v}_c[n]} = \frac{1 - \alpha_p}{1 - \alpha_p z^{-1}} \quad (2.19)$$

In order to change it from the discrete time transfer function to a continuous time transfer function, $z = e^{-sT_s}$ and zero order hold function(ZOH) which hold the sampled value for T_s are applied to (2.19). Then, the sampled-Laplace domain current feedback transfer function of the peak CPM with ZOH for one switching period of T_s [24, 32] is

$$\frac{R_i \cdot \hat{i}_L(s)}{\hat{v}_c(s)} = \frac{1 - \alpha_p}{1 - \alpha_p e^{-sT_s}} \cdot \frac{1 - e^{-sT_s}}{sT_s} \quad (2.20)$$

2.4 Small Signal Model for CPM

In order to design feedback circuit and apply it to DC-DC converter, it is necessary to develop a small signal model of current programmed mode control scheme with average power stage model. Fig.2.7 shows the well known current mode control small signal model diagram with averaged power stage model [34].

Based on (2.20), a small signal model for the peak CPM is developed and shown in Fig.

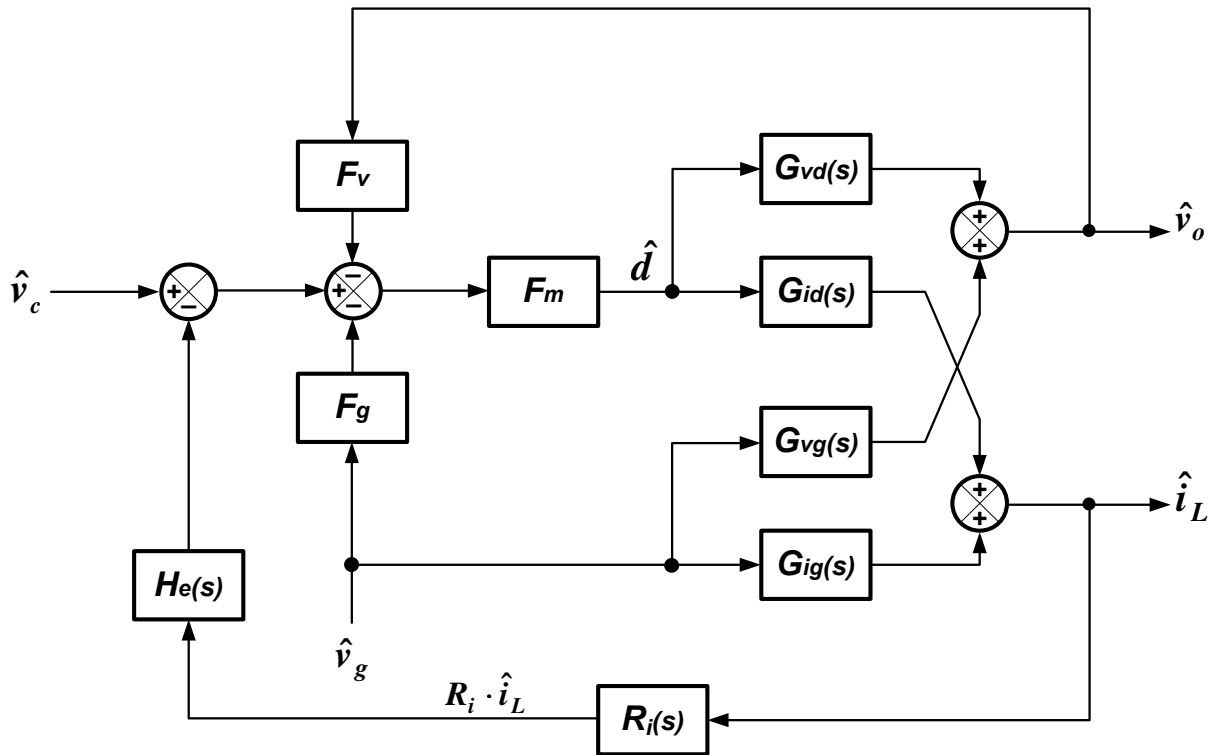


Figure 2.7: Small signal model for CPM

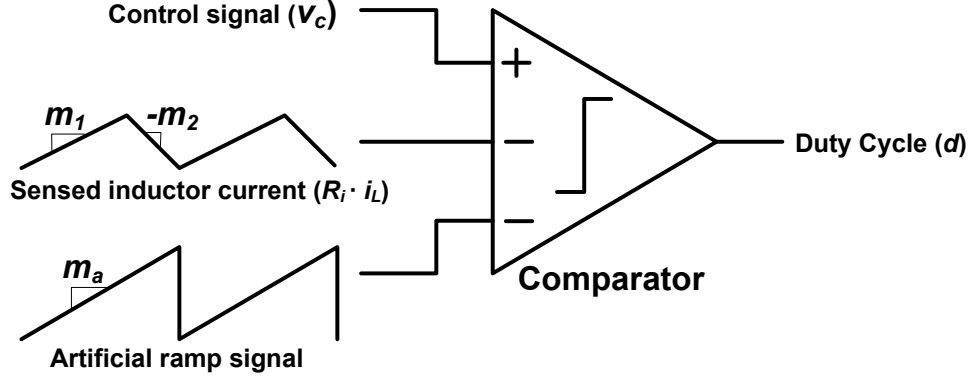


Figure 2.8: Modulation in peak CPM

2.7 [34]. G_{vd} is the duty to output voltage transfer function, G_{id} is the duty to inductor current transfer function, G_{vg} is the input voltage to output voltage transfer function and G_{ig} is the input voltage to inductor current transfer function. These transfer functions are from the well known average power stage model [34]. Peak CPM related blocks are F_m , H_e , F_v and F_g which are the modulation gain, the sampling gains, the feedforward gain from output voltage and the feedforward gain from input voltage respectively. And R_i represents the inductor current sensing gain.

In this section, the CPM related control blocks (gains) are revisited and the associated gains of peak CPM are derived. For valley CPM, readers can follow the method shown here to derive the equations.

2.4.1 Modulation gain (F_m) derivation

The F_m is known as a modulation gain. In peak CPM, the duty cycle is generated from the comparator with the control signal, the sensed inductor current, and the ramp signal. Fig.2.8 shows a diagram to explain the modulation gain [24]. From the Fig.2.8 and small

signal approximation, F_m can be derived like below.

$$F_m = \frac{1}{(m_1 + m_a)T_s} \quad (2.21)$$

This F_m also can be derived from the the small signal model of [24]. From the small signal model, the modulation gain (F_m) can be defined as the ratio of the ‘current’ duty perturbation ($\hat{d}[n]$) to the difference of the ‘current’ control signal perturbation ($\hat{v}_c[n]$) and the ‘previous’ sensed inductor current perturbation ($R_i \cdot \hat{i}_L[n-1]$), and it is

$$F_m \equiv \frac{\hat{d}[n]}{\hat{v}_c[n] - R_i \cdot \hat{i}_L[n-1]} \quad (2.22)$$

By assuming $F_v = 0$, $F_g = 0$, and $H_e = 1$ in Fig.2.7, the F_m is derived from the (2.16) like below and shows same as (2.21).

$$F_m = \frac{\hat{d}}{\hat{v}_c - R_i \cdot \hat{i}_L} = \frac{1}{(m_1 + m_a)T_s} \quad (2.23)$$

2.4.2 Sampling gain (H_e) derivation

The H_e is a sampling gain to model the sample-and-hold effect which is derived from the sample-data modeling shown in previous chapter. This gain has been derived with different ways from different authors so far. In this paper, Dr. Ridley’s method is used to derive the H_e [24].

From the Fig.2.7, the response of \hat{i}_L to \hat{v}_c can be written like below.

$$\frac{\hat{i}_L(s)}{\hat{v}_c(s)} = \frac{F_m G_{id}}{1 + F_m G_{id} R_i H_e} \quad (2.24)$$

And, by rewriting (2.20), the following equation is derived.

$$\frac{\hat{i}_L(s)}{\hat{v}_c(s)} = \frac{1}{R_i} \frac{1 - \alpha_p}{1 - \alpha_p e^{-sT_s}} \cdot \frac{1 - e^{-sT_s}}{sT_s} \quad (2.25)$$

Because (2.24) and (2.25) are same, the H_e can be derived by equating (2.24) and (2.25) like below.

$$\frac{F_m G_{id}}{1 + F_m G_{id} R_i H_e} = \frac{1}{R_i} \frac{1 - \alpha_p}{1 - \alpha_p e^{-sT_s}} \frac{1 - e^{-sT_s}}{sT_s} \quad (2.26)$$

At first, G_{id} which is independent to power stage topologies need to be derived. G_{id} is the gain from duty perturbation (\hat{d}) to inductor current perturbation (\hat{i}_L) as shown in Eq.(2.27)

$$G_{id} \equiv \frac{\hat{i}_L}{\hat{d}} \quad (2.27)$$

Fig.2.9 is the small signal model of the power stage and CPM model with fixed voltages [24][38]. From Fig.2.9, the G_{id} can be derived and expressed for all converters as follow.

$$\begin{aligned} G_{id}(s) &= \frac{V_{ap}}{s \cdot L} \\ V_{ap} &= V_{ac} + V_{cp} \\ m_1 &= \frac{R_i \cdot V_{ac}}{L}, \quad m_2 = \frac{R_i \cdot V_{cp}}{L} \\ G_{id}(s) &= \frac{1}{R_i} \frac{m_1 + m_2}{s} \end{aligned} \quad (2.28)$$

With this (2.28), (2.23) can be rewritten like below.

$$F_m \cdot G_{id} = \frac{1}{R_i} \frac{1 - \alpha_p}{s \cdot T_s} \quad (2.29)$$

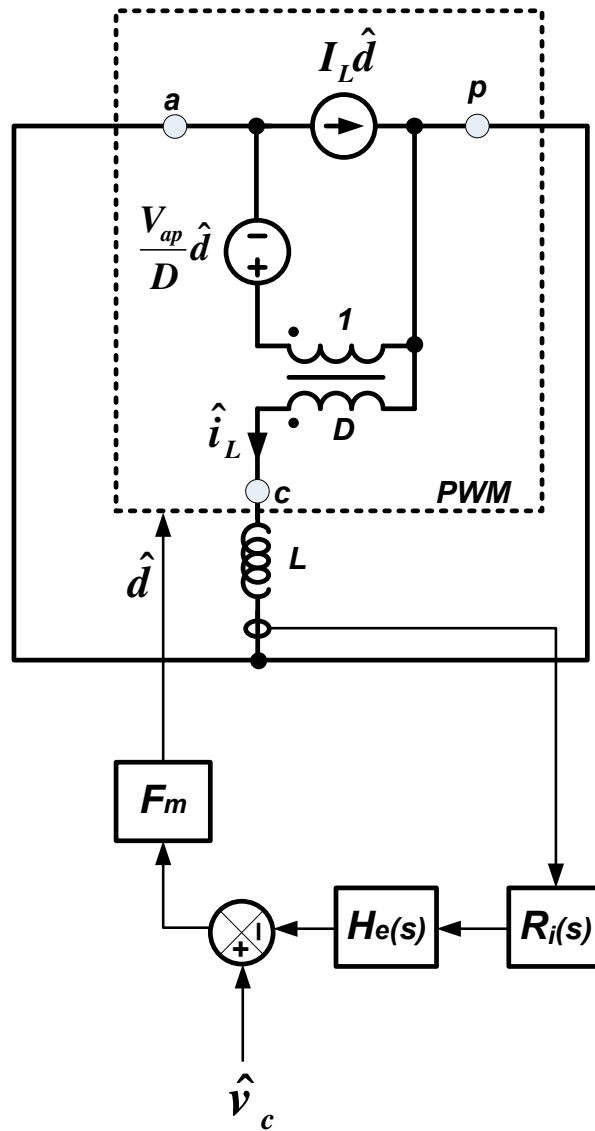


Figure 2.9: PWM switch model and current loop with fixed voltages

With (2.29) and (2.26), the following is derived,

$$1 + F_m \cdot G_{id} \cdot R_i \cdot H_e = \frac{e^{sT_s} - \alpha_p}{e^{sT_s} - 1} \quad (2.30)$$

From the above, the sampling gain (H_e) is derived and it is

$$H_e = \frac{sT_s}{e^{sT_s} - 1} \quad (2.31)$$

In [24], the (2.31) is approximated like below.

$$H_e(s) \cong 1 + \frac{s}{\omega_n Q_z} + \frac{s^2}{\omega_n^2} \quad (2.32)$$

where,

$$Q_z = \frac{-2}{\pi}$$

and,

$$\omega_n = \frac{\pi}{T_s}$$

This (2.32) is the second order model of (2.31) and shows that the sampling gain (H_e) has the complex double zeros at the half the switching frequency ($f_s = 1/T_s$). From the (2.24), it can be expected that the double zeros of the H_e will bring the double poles of the system. For this reason, it is well known that this double zeros of the H_e at the half the switching frequency limit the system performance which use the conventional CPM [24, 25, 32, 39, 31, 40].

Chapter 3

Double Edge Current Programmed Mode Control

3.1 Introduction: background and previous works on double edge modulation

In the previous chapter 2, we revisited Current Programmed Mode control (CPM). From the duty modulation point of view, the conventional CPM which is either the peak CPM or valley CPM is a single edge modulation scheme. The peak CPM only can modulate the trailing edge of the duty, and valley CPM only can modulate the leading edge of the duty during one switching period.

Fig.3.1 and Fig.3.2 shows the conceptual duty modulation examples for the peak CPM and valley CPM respectively. As shown Fig.3.1 and Fig.3.2, in conventional single edge current programmed mode control (hereafter referred to as “single CPM”), only one edge of the duty signal is modulated by the control scheme; the other edge of the duty signal

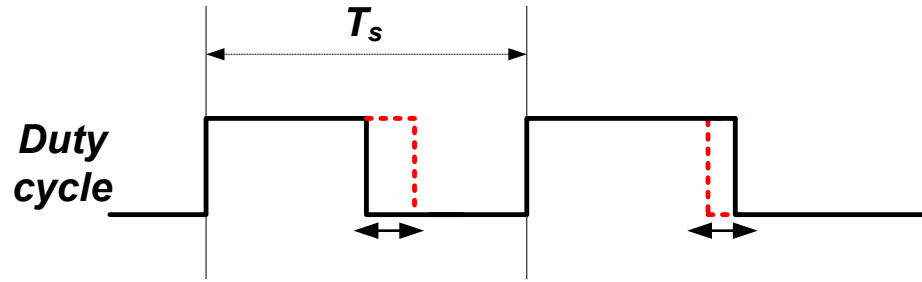


Figure 3.1: Trailing edge modulation

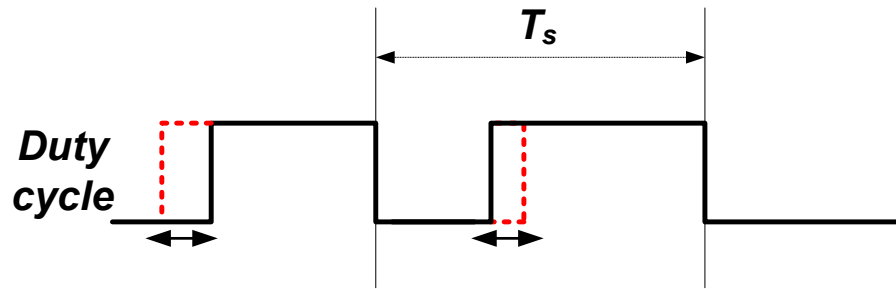


Figure 3.2: Leading edge modulation

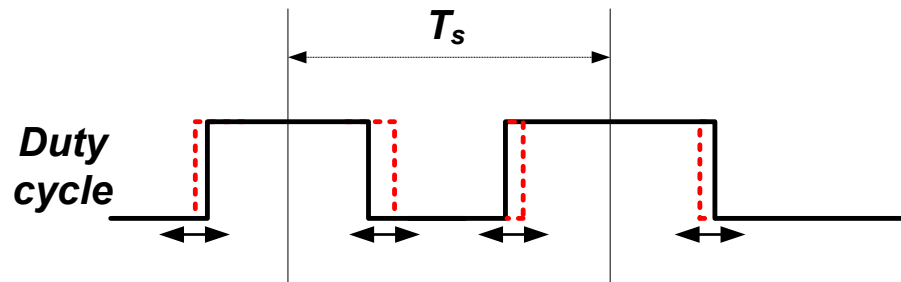


Figure 3.3: Double edge modulation

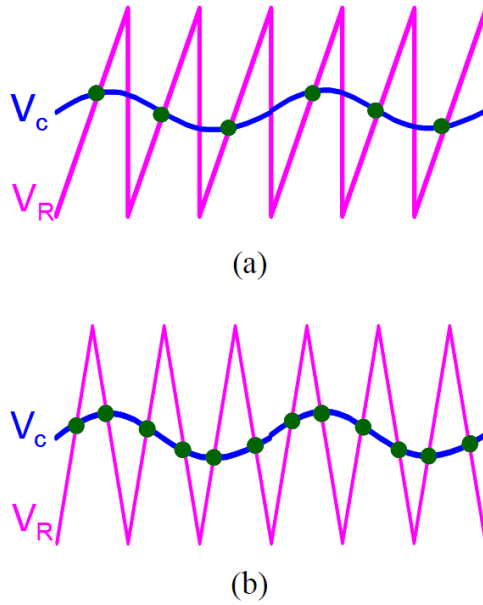
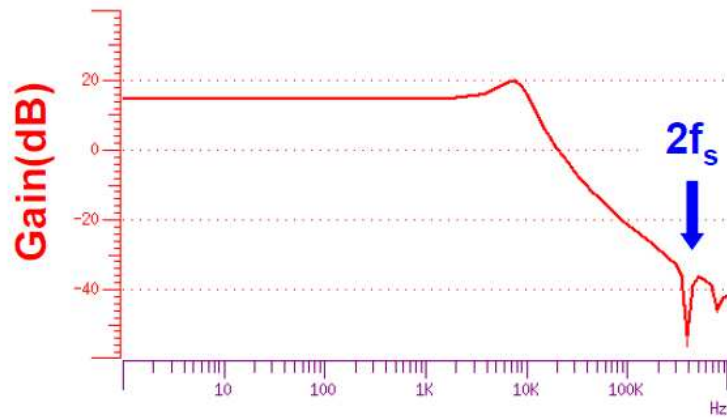


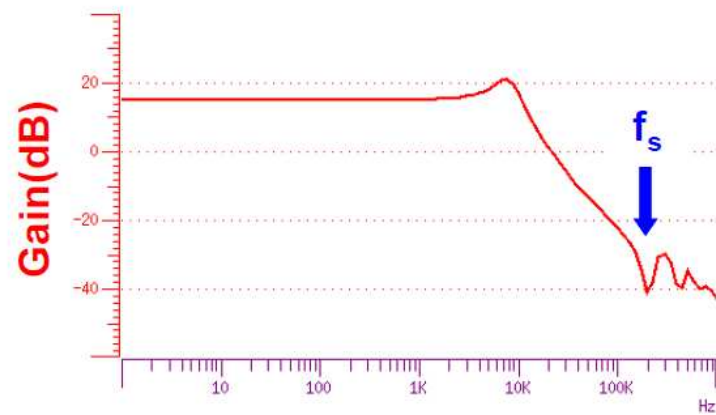
Figure 3.4: Sampling scheme of the PWM comparator:(a) trailing-edge PWM, and (b) double-edge PWM.

is unmodulated and determined by a fixed clock. In other words, the inductor current information is updated only once during a single switching period (T_s). Therefore, the bandwidth of a system utilizing single CPM is limited to half the switching frequency due to the corresponding sample and hold effects [24, 25, 31, 32, 39, 40].

Other authors have investigated double edge modulation schemes for converter applications. [41] addresses double edge modulation for voltage mode control and shows that the sampling frequency is doubled when the duty ratio is 0.5. Fig. 3.4 is the sampling scheme difference between trailing-edge PWM and the double-edge PWM in voltage mode control shown in [41]. In this reference, the author comments that “Intuitively, the double-edge PWM has a sampling frequency twice that of the trailing-edge PWM.” and shows that the dip on the transfer function of G_{vc} at two times of the switching frequency with duty cycle of 0.5. This is shown in Fig. 27.



(a)



(b)

Figure 3.5: G_{vc} with double edge-PWM in SIMPLIS simulation: (a) duty cycle is 50%, and (b) duty cycle is 10%.

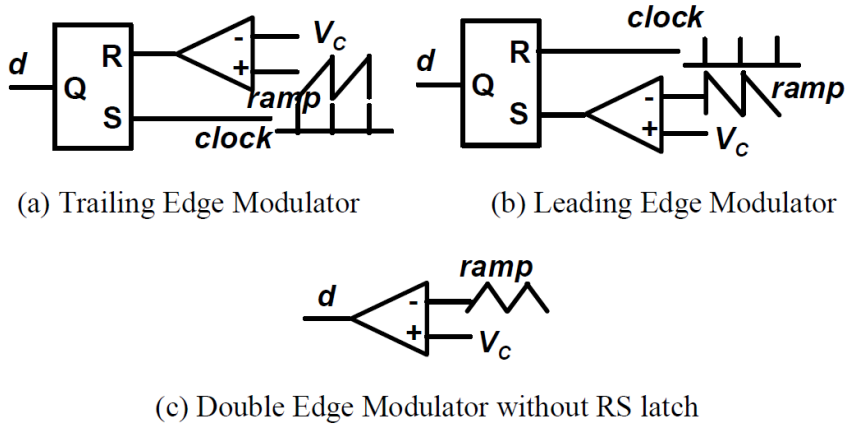
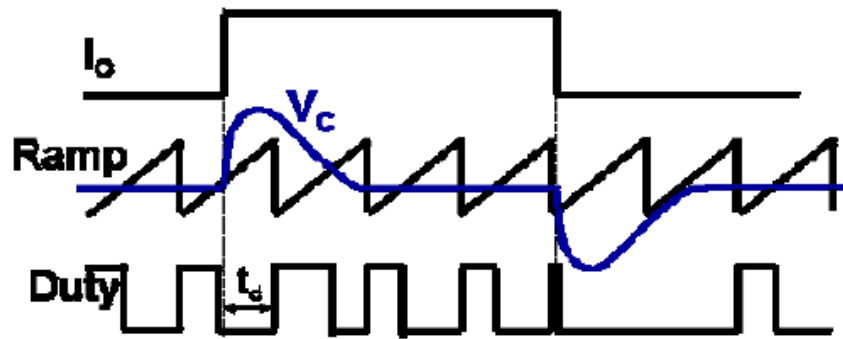


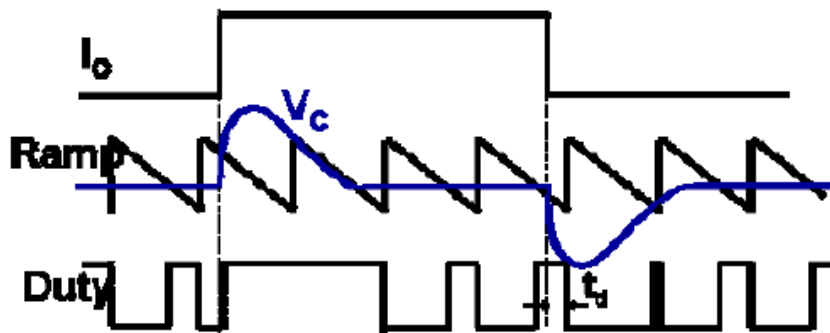
Figure 3.6: The schematics of the pulse width modulators.

[42] and [43] investigated the potential of a double (dual) edge controller for VRM applications to achieve the fast transient response. These papers emphasize the small switching delay in the control loop due to the double edge modulation scheme. [42] claims that dual edge controller reduces the switching action delay. Fig. 3.7 is the conceptual waveforms of the switching delays with different types of the pulse width modulators which is shown in Fig. 3.6 in [42]. The author explains that “The trailing edge modulator has a delay (t_d) when the load steps up and the leading edge modulation has delay when the load releases. This switching action delay causes undesirable charging or discharging of the output capacitors and results in the output voltage peaks or dips. In order to eliminate this delay, the dual edge modulator without RS latch is used. The dual edge controller should be well designed in IC level to be immune to the switching noise.”

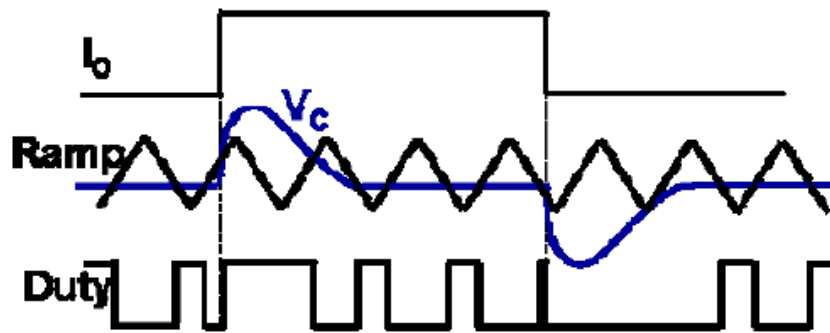
[44] comments that a double edge control scheme can improve the tracking accuracy of the output voltage to the reference signal. Fig. 3.8 is the schematic which is proposed in [44]. One comparison between the feedback signal (Sig) and a ramp is used to set the switch while another comparison between the offset feedback signal and the ramp is used



(a) Trailing Edge Modulator



(b) Leading Edge Modulator



(c) Dual Edge Modulator without RS latch

Figure 3.7: The transient waveforms with the pulse width modulators

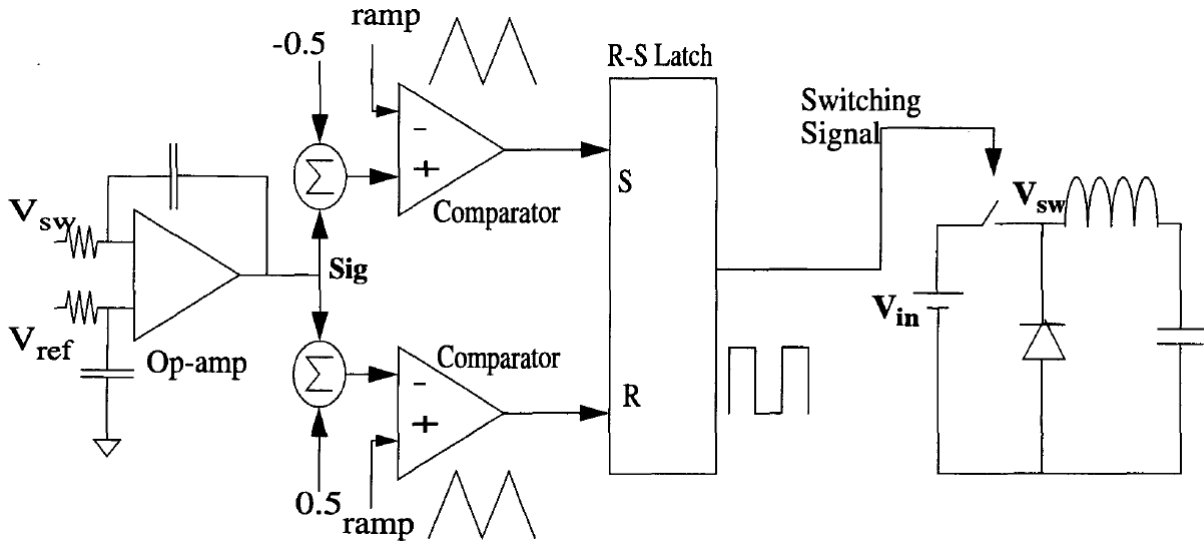


Figure 3.8: Two sided latched PWM schematics

to reset the switch. There is an extra comparator compared to a conventional PWM controller.

However, the sampling frequency dependence on the duty ratio and other characteristics of DECPM, such as the subharmonic oscillation issue and a larger current loop gain than conventional CPM, have not been analytically investigated from above research. This dissertation will address the detailed analysis of DECPM with a newly proposed model.

In this chapter, sample-data modeling of the double edge current programmed mode control (DECPM) is newly proposed and analyzed. The steady state conditions and the subharmonic oscillation issue of DECPM are analyzed first. Sample-data modeling for DECPM is proposed by mathematically combining the conventional peak CPM and valley CPM models. The dependence of the sampling frequency on the duty ratio is analyzed throughout this modeling. A small signal model for DECPM is developed by

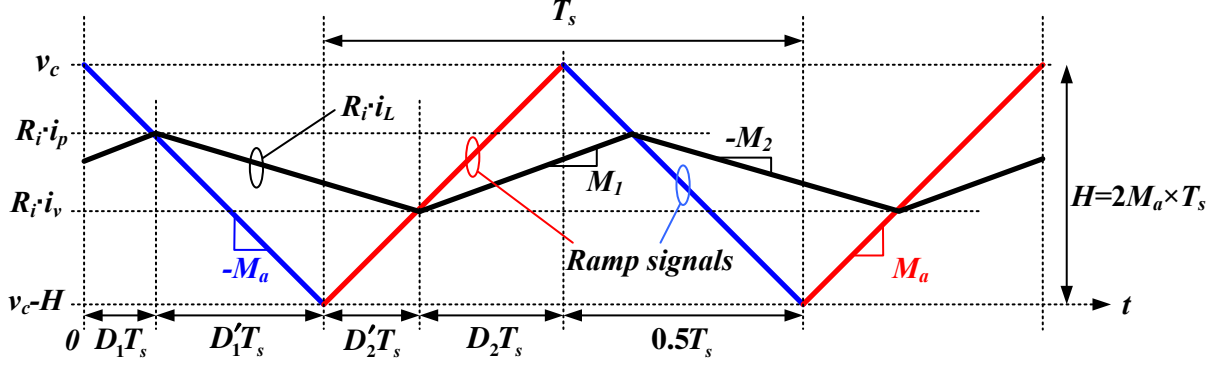


Figure 3.9: Steady state inductor current waveform in DECPM

deriving the modulation gains (F_m) and sampling gains (H_e). The proposed DECPM model is compared with the conventional single CPM by the SIMPLIS simulations. The larger current loop gain at high frequency for DECPM than the single CPM will be verified in this section.

3.2 Steady State condition and Subharmonic Oscillation

In this section, the steady state and subharmonic oscillation conditions of DECPM are discussed. Fig. 3.9 shows the steady state waveforms of the sensed inductor current ($R_i \cdot i_L$), control signal (v_c) and ramp signals in DECPM. Here, R_i is the gain of the current sensor. In DECPM, two ramp signals with the slopes of M_a and $-M_a$ are added to the control signal (v_c) to control the peak and valley value of the sensed inductor current. As shown in Fig. 3.9, because both peak and valley values of the sensed inductor current are controlled by DECPM, the resultant duty signals are modulated on both edges.

From Fig. 3.9, the peak ($R_i \cdot i_p$) and valley value ($R_i \cdot i_v$) of the sensed inductor current are derived in terms of the control signal (v_c).

$$\begin{aligned} R_i \cdot i_p &= R_i \cdot i_L(D_1 T_s) \\ &= v_c - M_a D_1 T_s = R_i \cdot i_L(0) + M_1 D_1 T_s \end{aligned} \quad (3.1)$$

$$\begin{aligned} R_i \cdot i_v &= R_i \cdot i_L((0.5 + D'_2) T_s) \\ &= R_i \cdot i_L(D_1 T_s) - M_2 \cdot (D'_1 + D'_2) \cdot T_s \end{aligned} \quad (3.2)$$

Here, D_1 and D_2 are the duty ratios in the peak and valley current control region respectively. Therefore, $D'_1 = 0.5 - D_1$ and $D'_2 = 0.5 - D_2$, and the whole duty ratio (D) is a sum of these D_1 and D_2 .

To see the steady state condition of the sensed inductor current ($R_i \cdot i_L$), the relationship of the sensed inductor currents between the adjacent switching periods are derived as shown below.

$$\begin{aligned} R_i \cdot i_L(T_s) &= R_i \cdot i_v + M_1 D_2 T_s \\ &= R_i \cdot i_L(0) + M_1 D_1 T_s - M_2 \cdot (D'_1 + D'_2) \cdot T_s + M_1 D_2 T_s \\ &= R_i \cdot i_L(0) + M_1 \cdot (D_1 + D_2) \cdot T_s - M_2 \cdot (D'_1 + D'_2) \cdot T_s \\ &= R_i \cdot i_L(0) + M_1 D T_s - M_2 D' T_s \end{aligned} \quad (3.3)$$

In steady state, the condition of $R_i \cdot i_L(T_s) = R_i \cdot i_L(0)$ should be satisfied. Thus, the steady state condition of DECPM is derived from (3.3), and is

$$\frac{M_2}{M_1} = \frac{D}{D'} \quad (3.4)$$

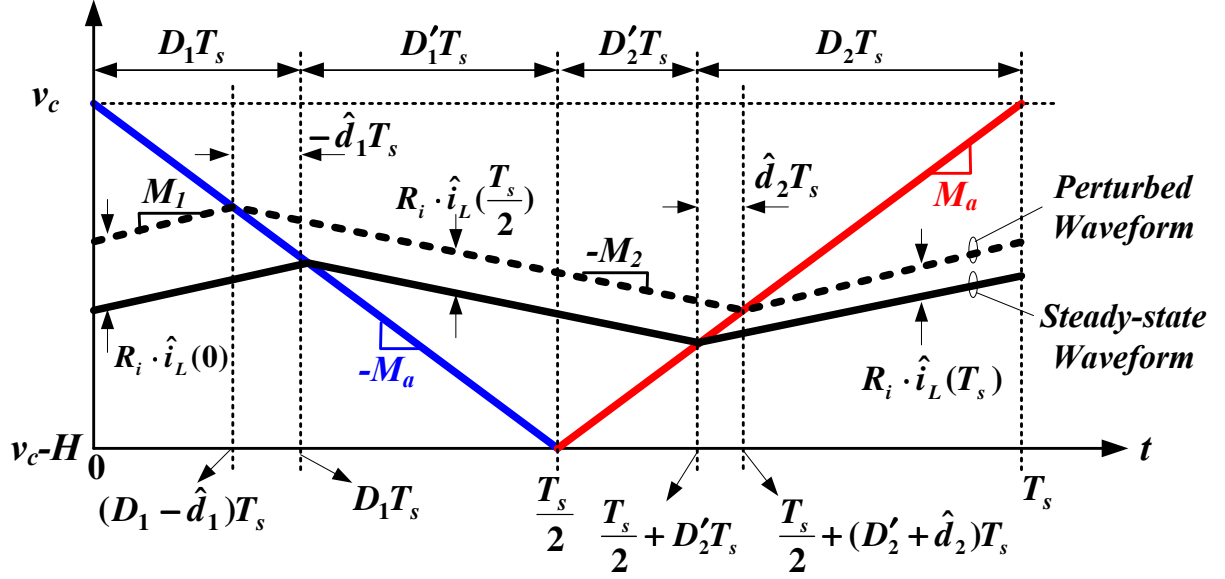


Figure 3.10: Steady-state and perturbed inductor current waveforms

This steady state condition of DECPM is same as that of the conventional single CPM. For analyzing the subharmonic oscillation issues [34] in DECPM, the sensed inductor current is perturbed as shown in Fig. 3.10. Then, the subharmonic oscillation conditions can be derived from the natural response of the sensed inductor current perturbation $(R_i \cdot \hat{i}_L)$.

From simple trigonometric analysis of Fig. 3.10, the following equations are derived.

$$R_i \cdot \hat{i}_L(0) = -(M_1 + M_a)\hat{d}_1 T_s \quad (3.5)$$

$$R_i \cdot \hat{i}_L\left(\frac{T_s}{2}\right) = -(M_a - M_2)\hat{d}_1 T_s \quad (3.6)$$

$$R_i \cdot \hat{i}_L\left(\frac{T_s}{2}\right) = (M_a + M_2)\hat{d}_2 T_s \quad (3.7)$$

$$R_i \cdot \hat{i}_L(T_s) = (M_a - M_1)\hat{d}_2 T_s \quad (3.8)$$

Because (3.6) and (3.7) are equal,

$$\hat{d}_2 = \frac{-(M_a - M_2)}{M_a + M_2} \cdot \hat{d}_1 \quad (3.9)$$

By plugging (3.9) into (3.8) and generalizing it to arbitrary timing,

$$R_i \cdot \hat{i}_L(nT_s) = -\frac{M_2 - M_a}{M_1 + M_a} \cdot -\frac{M_1 - M_a}{M_2 + M_a} \cdot R_i \cdot \hat{i}_L((n-1)T_s) \quad (3.10)$$

$$\hat{i}_L(nT_s) = \alpha_p \cdot \alpha_v \cdot \hat{i}_L((n-1)T_s) \quad (3.11)$$

$$= \alpha \cdot \hat{i}_L((n-1)T_s) \quad (3.12)$$

where,

$$\alpha = \alpha_p \cdot \alpha_v \quad (3.13)$$

$$\alpha_p = -\frac{M_2 - M_a}{M_1 + M_a}, \quad 1 - \alpha_p = \frac{M_1 + M_2}{M_1 + M_a} \quad (3.14)$$

$$\alpha_v = -\frac{M_1 - M_a}{M_2 + M_a}, \quad 1 - \alpha_v = \frac{M_1 + M_2}{M_2 + M_a} \quad (3.15)$$

(3.12) is a inductor current perturbation relationship between the adjacent switching periods. Here, α_p and α_v are the inductor current attenuation factors for the peak CPM and valley CPM respectively, and α is the inductor current attenuation factor for the DECPM which is a product of α_p and α_v as shown in (3.13). By using the steady state condition of DECPM in (3.4), α in (3.13) is rewritten in terms of the duty ratio, the slope of ramp signal and the falling slope of the sensed inductor current as shown below.

$$\alpha = \alpha_p \cdot \alpha_v = \frac{1 - \frac{M_a}{M_2}}{\frac{D'}{D} + \frac{M_a}{M_2}} \cdot \frac{\frac{D'}{D} - \frac{M_a}{M_2}}{1 + \frac{M_a}{M_2}} \quad (3.16)$$

It is well known that, without the ramp signals ($M_a = 0$), α_p for peak CPM and α_v for valley CPM become larger than 1 when $D > 0.5$ and $D < 0.5$ respectively, which

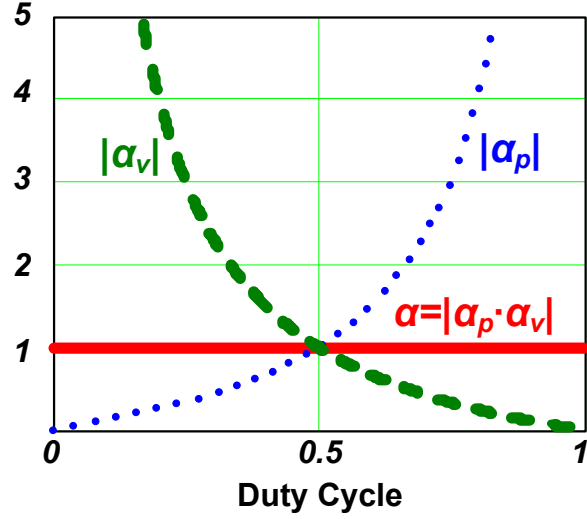


Figure 3.11: α , α_p and α_v at the function of duty ratio without ramp signal ($M_a = 0$)

causes subharmonic oscillation. The inductor current attenuation factors without the ramp signals ($M_a = 0$) are derived below and showed in Fig. 3.11.

$$\alpha_p|_{M_a=0} = \frac{D}{D'} \quad (3.17)$$

$$\alpha_v|_{M_a=0} = \frac{D'}{D} \quad (3.18)$$

$$\alpha|_{M_a=0} = 1 \quad (3.19)$$

Interestingly, the α in DECPM, which is a product of α_p and α_n is always 1 for the entire duty range without the ramp signals ($M_a = 0$). This means once perturbation is applied to inductor current, there is no amplification or attenuation of the disturbance in DECPM.

To avoid subharmonic oscillations for the entire duty range, the inductor current attenuation factors should be less than 1 for all operating conditions (i.e. for all duty ratios). Fig. 3.12 shows α in DECPM with the different ramp signals ($M_a \neq 0$) in

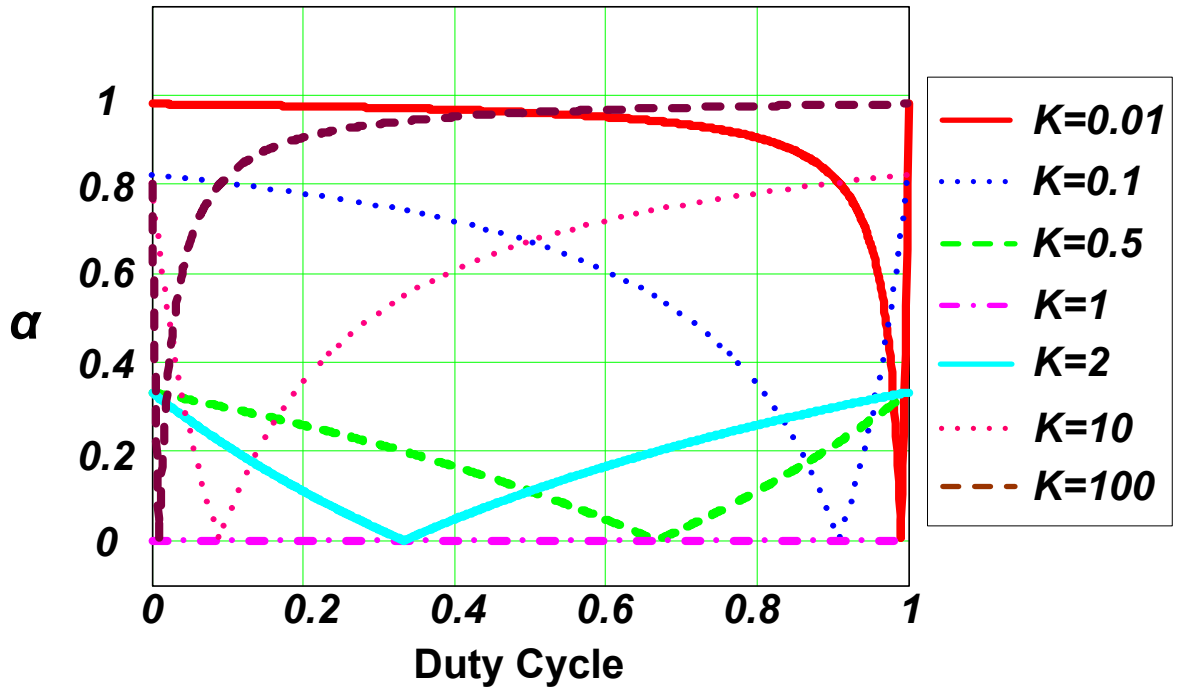


Figure 3.12: α at the function of duty ratio with different ramp signals having the slopes of M_a ($K = M_a/M_2$)

terms of the duty ratios. Here, K is the ratio of the slopes of the ramp signal and the falling slope of the sensed inductor current ($K = M_a/M_2$). Fig. 3.12 shows that α will always be less than 1 for the whole duty range, regardless of the slope of the ramp signal in DECPM. However, for conventional single CPM, the slope of the ramp signals (M_a) need to be chosen carefully to avoid subharmonic oscillation for all duty ranges [34].

3.3 Sample-data modeling

3.3.1 Sample-data current feedback transfer function

There has been much research on control modelings for high frequency converters which can predict up to half the switching frequency[35, 36, 37, 24, 32, 31, 25]. In order to model the current programmed mode control accurately to high frequency including the sample and hold effects, the sample-data model is popular and widely accepted[24, 32, 31]. Among the sample-data modelings for converters, Ridley’s method[24, 25] is referred and applied to model the DECPM in this dissertation.

Fig. 3.13 shows the waveforms to derive the sample-data model for DECPM. This figure shows the modulated duty signal (\hat{d}) and the sensed inductor current perturbation ($R_i \cdot \hat{i}_L$) as the results of the control signal perturbation (\hat{v}_c). As shown in Fig. 3.13, it can be observed that the sensed inductor current ($R_i \cdot \hat{i}_L$) is updated twice in one switching period (T_s). This is a major difference between DECPM and conventional single CPM. In conventional single CPM, the inductor current perturbation happens only once in each switching period and is held for one switching period [24]. This makes the sampling frequency of the control the same as the switching frequency of the power stage. However, in DECPM, the inductor current perturbations happen (are sampled) two times during

one switching period, and each updated inductor current perturbation is kept (held) for DT_s and $(1 - D)T_s$ respectively. Therefore, DECPM has a fixed switching frequency in the power stage but variable sampling frequency for the control with different operating points. More details are investigated through the following derivations.

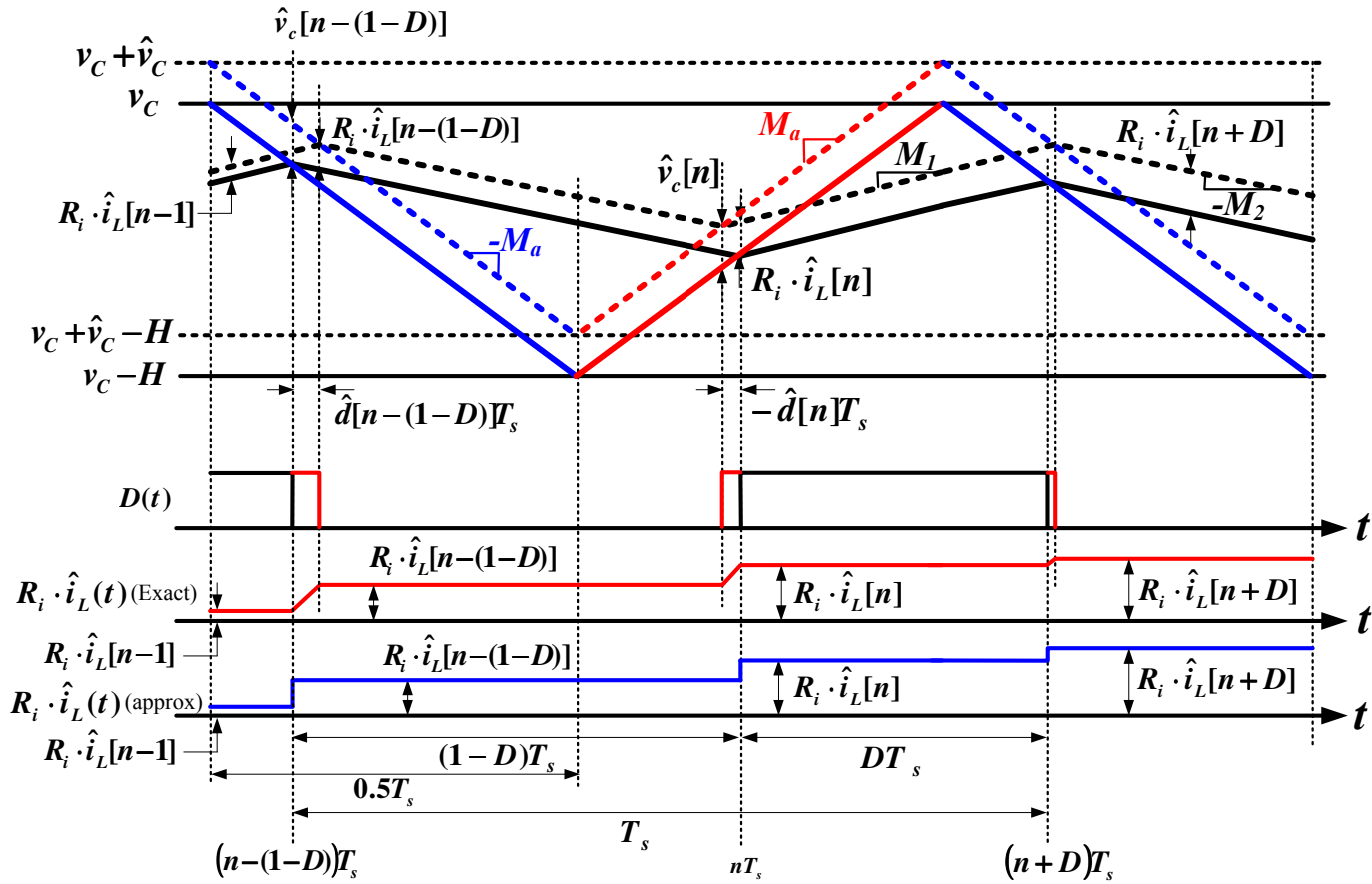


Figure 3.13: Double edge current programmed mode waveforms

For the following DECPM modeling, the voltages applied across the inductor are kept constant and the current feedback loop is closed as in conventional CPM modeling [24]. In addition, it is also assumed that the control signal perturbation (\hat{v}_c) does not change during one switching cycle (T_s). This assumption implies that, for one switching period, the first updated inductor current perturbation does not affect the control signal perturbation (\hat{v}_c) which is also used for the second update of the inductor current perturbation. Therefore, the first update and the second update of the inductor current perturbations are independent from each other with respect to the control signal perturbation (\hat{v}_c).

By using simple trigonometric analysis at the time of $(n - (1 - D))T_s$ from Fig. 3.13, the following two equations are derived.

$$R_i \cdot \hat{i}_L[n - (1 - D)] = R_i \cdot \hat{i}_L[n - 1] + (M_1 + M_2)\hat{d}[n - (1 - D)]T_s \quad (3.20)$$

$$\hat{v}_c[n - (1 - D)] = R_i \cdot \hat{i}_L[n - 1] + (M_1 + M_a)\hat{d}[n - (1 - D)]T_s \quad (3.21)$$

These (3.20) and (3.21) show the relationship among the control signal perturbation (\hat{v}_c), the peak point of the sensed inductor current perturbation ($R_i \cdot \hat{i}_L$) and the duty perturbation (\hat{d}). This relationship is called a ‘peak current control law’ in this dissertation.

With a similar derivation at the time of nT_s from Fig. 3.13, the other two equations are derived in (3.22) and (3.23). These two equations show the relationship between the control signal perturbation (\hat{v}_c), the valley point of the sensed inductor current perturbation ($R_i \cdot \hat{i}_L$) and the duty perturbation (\hat{d}). This relationship is called a ‘valley current control law’ in this dissertation.

$$R_i \cdot \hat{i}_L[n] = R_i \cdot \hat{i}_L[n - (1 - D)] + (M_1 + M_2)(-\hat{d}[n])T_s \quad (3.22)$$

$$\hat{v}_c[n] = R_i \cdot \hat{i}_L[n - (1 - D)] + (M_2 + M_a)(-\hat{d}[n])T_s \quad (3.23)$$

In conventional single CPM, either one set of (3.20),(3.21) or (3.22),(3.23) is used for peak CPM and valley CPM respectively, but DECPM needs both of them.

With (3.20) and (3.21), a following equation is derived.

$$R_i \cdot \hat{i}_L[n - (1 - D)] = \alpha_p \cdot R_i \cdot \hat{i}_L[n - 1] + (1 - \alpha_p) \cdot \hat{v}_c[n - (1 - D)] \quad (3.24)$$

By applying a Laplace transform, it's time shift property and hold function for $(1 - D)T_s$ to (3.24), the 'peak current control law' based current feedback transfer function of DECPM is derived in (3.25), which looks similar to that of peak CPM.

$$\left. \frac{R_i \cdot \hat{i}_L(s)}{\hat{v}_c(s)} \right|_{peak} = \frac{1 - \alpha_p}{1 - \alpha_p e^{-sDT_s}} \cdot \frac{1 - e^{-s(1-D)T_s}}{sT_s} \quad (3.25)$$

The difference between (3.25) and the conventional sampled data current feedback transfer function of peak CPM[24] is the duty information in the model. The DT_s in the first term of the right hand side of (3.25) means the derived transfer function is the result of the relationship between the control signal perturbation (\hat{v}_c) and the sensed inductor current perturbation ($R_i \cdot \hat{i}_L$) during DT_s , and the $(1 - D)T_s$ in the second term implies that the sampled (updated) information of the sensed inductor current perturbation is

held for $(1 - D)T_s$. Therefore, the duty information in the transfer function of DECPM shows that the sampling frequency of the control (not the switching frequency of the power stage) varies with the different operating points.

By doing a similar derivation with (3.22) and (3.23), the ‘valley current control law’ based current feedback transfer function of DECPM is derived in (3.26).

$$\left. \frac{R_i \cdot \hat{i}_L(s)}{\hat{v}_c(s)} \right|_{valley} = \frac{1 - \alpha_v}{1 - \alpha_v e^{-s(1-D)T_s}} \cdot \frac{1 - e^{-sDT_s}}{sT_s} \quad (3.26)$$

Similar to (3.25), the $(1 - D)T_s$ in the first term of the right hand side of (3.26) indicates that the derived transfer function is the result of the relationship between the control signal perturbation (\hat{v}_c) and the sensed inductor current perturbation ($R_i \cdot \hat{i}_L$) during $(1 - D)T_s$, and the DT_s in the second term implies that the sampled (updated) information of the sensed inductor current perturbation is held for DT_s .

The whole current feedback transfer function of DECPM during one switching period is a linear sum of the (3.25) and (3.26) and is shown in (3.27). This is deduced from the time domain waveform of $R_i \cdot \hat{i}_L(t)$ (approx) shown at the last waveform in Fig. 3.13. The value of $R_i \cdot \hat{i}_L[n]$ is a sum of the two updated values from DECPM and the value of $R_i \cdot \hat{i}_L[n - 1]$. These two updated values in time domain correspond to (3.25) and (3.26) in frequency domain. In other words, with the assumption of the constant control signal perturbation (\hat{v}_c) during one switching period as mentioned earlier, the two updates of the sensed inductor current perturbation in DECPM are independent each other. Therefore, the corresponding transfer functions of (3.25) and (3.26) are also independent of each other, and this lack of interdependence makes the whole current

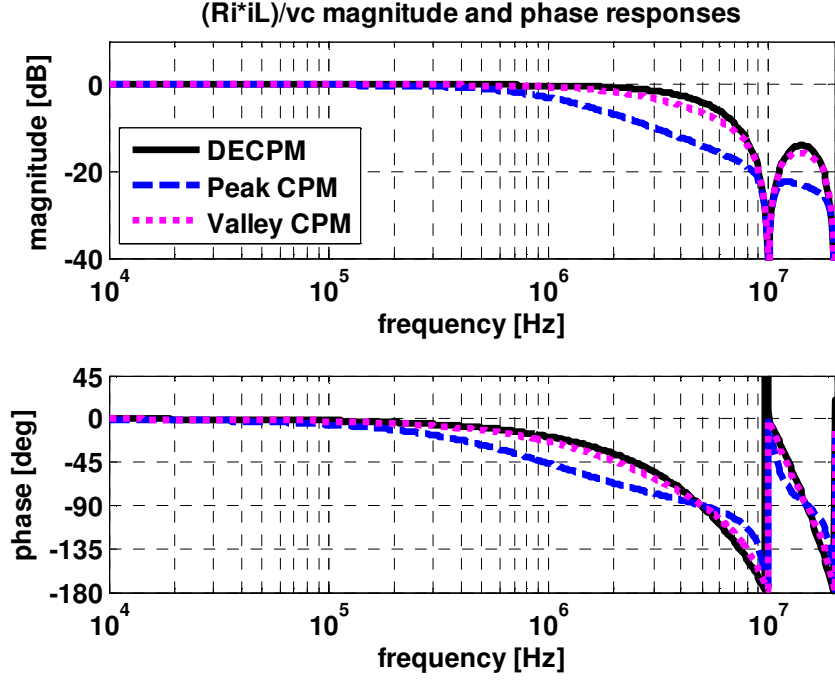


Figure 3.14: v_c to $R_i \cdot i_L$ responses when $V_{in} = 3.3V$ and $V_{out} = 0.1V$

feedback transfer function of DECPCM during one switching period the linear sum of the (3.25) and (3.26).

$$\begin{aligned}
 \frac{R_i \cdot \hat{i}_L(s)}{\hat{v}_c(s)} &= \frac{R_i \cdot \hat{i}_L(s)}{\hat{v}_c(s)} \Big|_{peak} + \frac{R_i \cdot \hat{i}_L(s)}{\hat{v}_c(s)} \Big|_{valley} \\
 &= \frac{1 - \alpha_p}{1 - \alpha_p e^{-sDT_s}} \cdot \frac{1 - e^{-s(1-D)T_s}}{sT_s} + \frac{1 - \alpha_v}{1 - \alpha_v e^{-s(1-D)T_s}} \cdot \frac{1 - e^{-sDT_s}}{sT_s} \quad (3.27)
 \end{aligned}$$

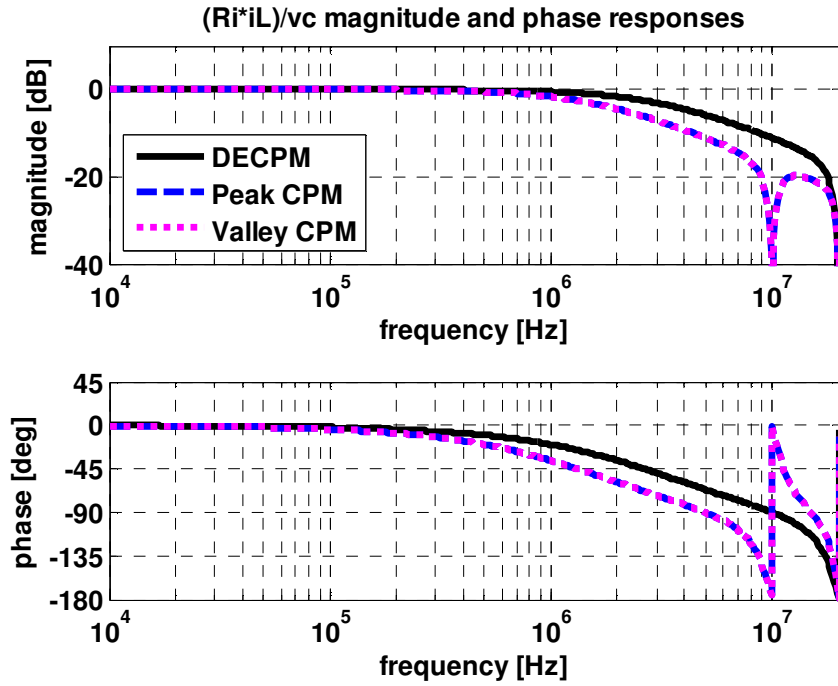


Figure 3.15: v_c to $R_i \cdot i_L$ responses when $V_{in} = 3.3V$ and $V_{out} = 1.65V$

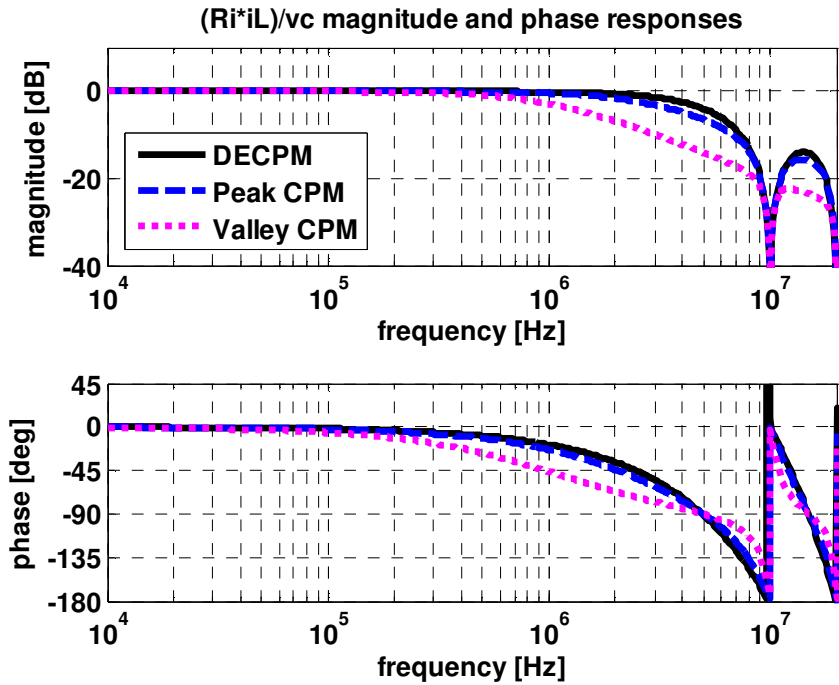


Figure 3.16: v_c to $R_i \cdot i_L$ responses when $V_{in} = 3.3V$ and $V_{out} = 3.2V$

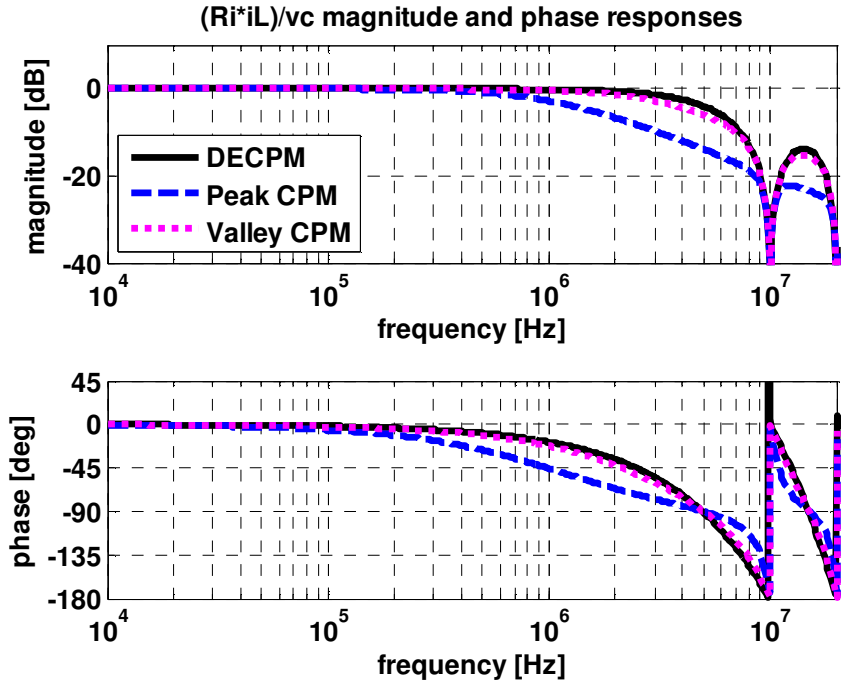


Figure 3.17: v_c to $R_i \cdot i_L$ responses when $V_{in} = 3.3V$ and $V_{out} = 3.4V$

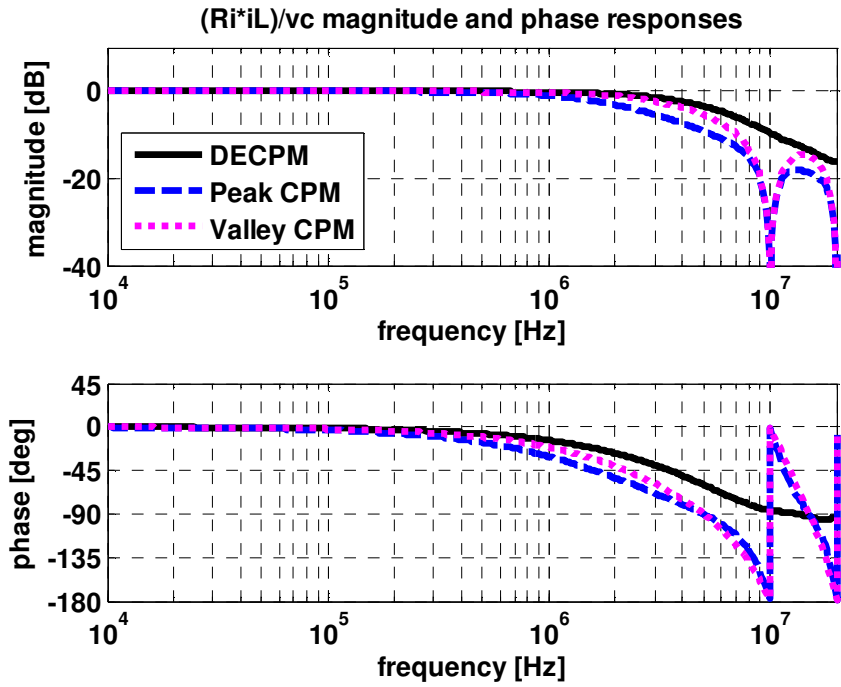


Figure 3.18: v_c to $R_i \cdot i_L$ responses when $V_{in} = 3.3V$ and $V_{out} = 5V$

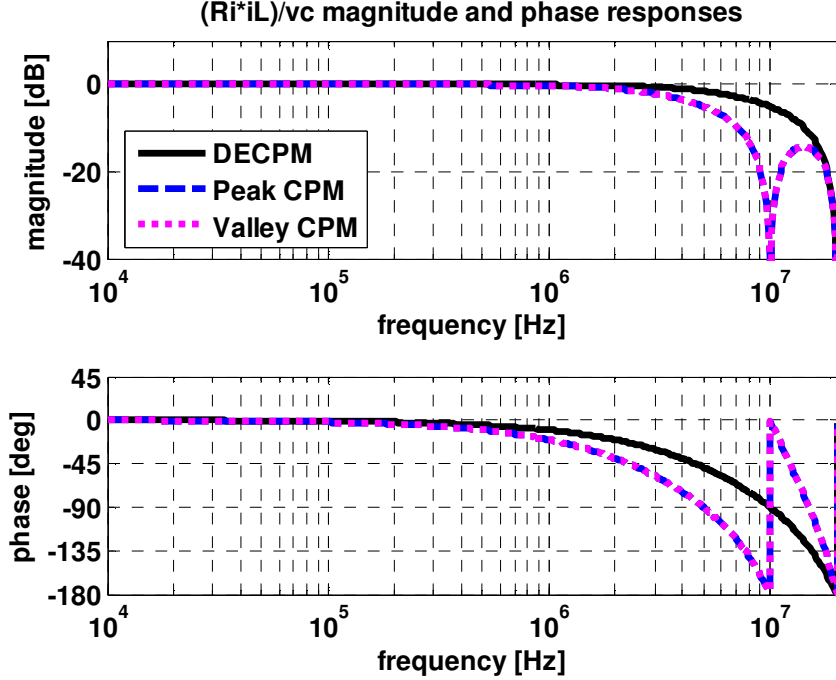


Figure 3.19: v_c to $R_i \cdot i_L$ responses when $V_{in} = 3.3V$ and $V_{out} = 6.6V$

3.3.2 Comparisons of current feedback transfer function

The waveforms from Fig. 3.14 to Fig. 3.19 show the comparisons of the current feedback transfer functions with different duty ratios. Fig. 3.14 to Fig. 3.16 are the cases of the buck converter when $D \approx 0$, $D = 0.5$ and $D \approx 1$, respectively. Fig. 3.17 to Fig. 3.19 are the cases of the boost converter when $D \approx 0$, $D = 0.34$ and $D = 0.5$, respectively. For these comparisons, the switching frequency is $10MHz$, where T_s is $100nsec$ and M_a set to $1.6/T_s$ for all DECPM, peak CPM and valley CPM.

From Fig. 3.14 to Fig. 3.19, two features of DECPM can be observed. One is that the sampling frequency of the control changes with the duty ratio. It is well known that the double edge modulation scheme has two times faster sampling frequency than single edge modulation scheme when the duty ratio is 0.5, but it has not been explicitly shown

that the sampling frequency decreases with other duty ratios and reaches the same value of switching frequency when the duty ratio is 0 or 1. From Fig. 3.14 to Fig. 3.16, peak CPM and valley CPM have a fixed $10MHz$ sampling frequency of the control by showing two complex poles at $10MHz$, which is same as the switching frequency of the power stage. However, DECPM has a variable sampling frequency which changes from $10MHz$ when $D \approx 0$ and $D \approx 1$ to $20MHz$ when $D = 0.5$.

The other feature of DECPM is a larger current loop gain than in single CPM. In a simple model of CPM [34], it is generally assumed that the inductor works as a voltage controlled current source, so the power stage with CPM is simplified into a first order system. In other words, as long as the sensed inductor current ($R_i \cdot i_L$) follows the control signal (v_c) well, the system is governed by current programmed mode control. This phenomenon can be explained clearly with the figures from Fig.3.14 to Fig.3.19. In Fig.3.14, which is when the duty ratio is close to 0, for example, the current feedback transfer function of the DECPM and the valley CPM have wider $0dB$ range than that of the peak CPM. Here, the wider $0dB$ range means that the sensed inductor current follows well the control signal at higher frequency. In Fig.3.16, which is when the duty ratio is close to 1, the current feedback transfer function of the DECPM and peak CPM have wider $0dB$ range than that of valley CPM. Specifically, when the duty ratio is 0.5 which is the case of Fig.3.15, the DECPM shows the widest $0dB$ range among all CPM with the help of the doubled sampling frequency. These features of DECPM could be beneficial to the wide range of converter applications which require stable operation for a wide duty range with a fixed compensator. Because DECPM's performance is always either as good as or better than convention peak / valley CPM, relatively constant current loop gain up to high frequency is achieved for all duty ratios. This relatively constant current loop gain at high frequency is shown even in buck and boost mode transition. Comparing

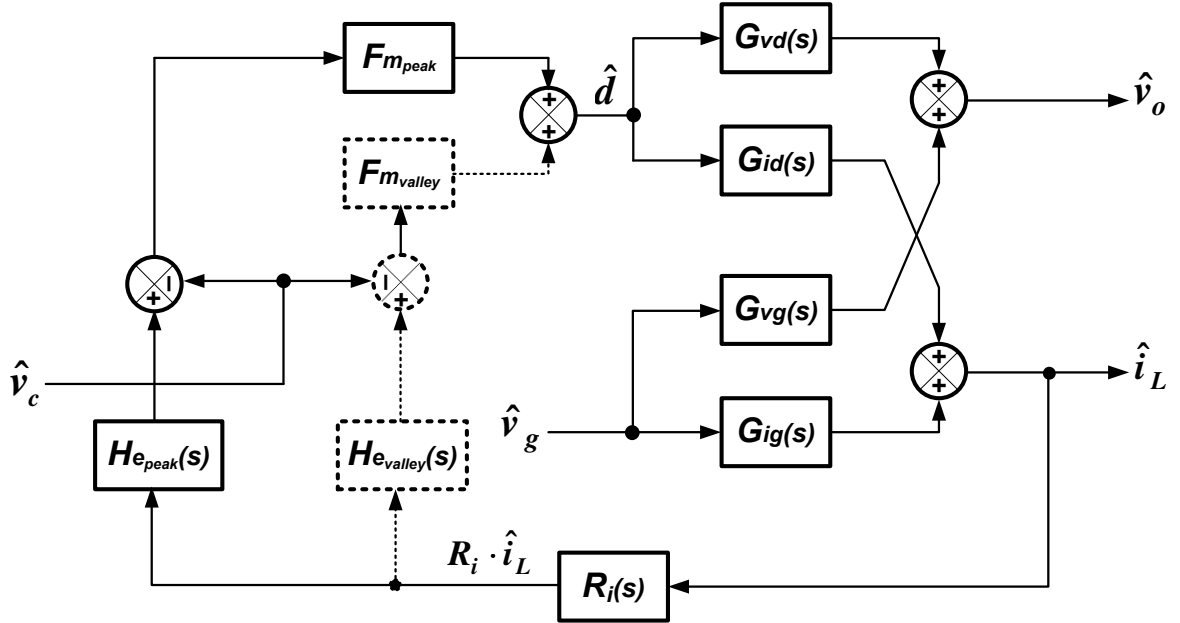


Figure 3.20: Small signal model for DECPM

Fig. 3.16 and Fig. 3.17, DECPM shows the smoother change of the current feedback transfer function at the transition of buck mode at $D \approx 1$ and boost mode at $D \approx 0$ than the single CPM does. This benefit of the constant current loop in DECPM will be reemphasized and verified in the simulation.

3.4 Small Signal Model for DECPM

In order to design feedback circuit and apply it to DC-DC converter, it is necessary to develop a small signal model of current programmed mode control scheme with average power stage model. Fig. 2.7 in previous section shows the well known current mode control small signal model diagram with averaged power stage model [34].

Based on (3.27), a small signal model for DECPM is developed and shown in Fig.

3.20. G_{vd} is the duty to output voltage transfer function, G_{id} is the duty to inductor current transfer function, G_{vg} is the input voltage to output voltage transfer function and G_{ig} is the input voltage to inductor current transfer function. These transfer functions are from the well known average power stage model [34]. DECPM related blocks are $F_m|_{peak}$, $F_m|_{valley}$, $H_e|_{peak}$, $H_e|_{valley}$, and R_i . $F_m|_{peak}$ and $F_m|_{valley}$ are the modulation gains for peak and valley control law respectively. $H_e|_{peak}$, $H_e|_{valley}$ are the sampling gains for ‘peak and valley control law’ respectively. And R_i represents the inductor current sensing gain. The dotted line of the $H_e|_{valley}$ block and $F_m|_{valley}$ in Fig. 3.20 represents that the peak and valley current control loop in DECPM are independent each other. Therefore, the transfer function from the control signal (\hat{v}_c) to the inductor current (\hat{i}_L) of DECPM shown in Fig. 3.20 is derived like (3.28).

$$\frac{\hat{i}_L(s)}{\hat{v}_c(s)} = \frac{F_m|_{peak} G_{id}}{1 + F_m|_{peak} G_{id} R_i H_e|_{peak}} + \frac{F_m|_{valley} G_{id}}{1 + F_m|_{valley} G_{id} R_i H_e|_{valley}} \quad (3.28)$$

Through the following subsections, the F_m s and H_e s will be derived.

3.4.1 Modulation gain (F_m) derivation

According to the small signal model of [24], the modulation gain (F_m) can be defined as the ratio of the ‘current’ duty perturbation ($\hat{d}[n]$) to the difference of the ‘current’ control signal perturbation ($\hat{v}_c[n]$) and the ‘previous’ sensed inductor current perturbation ($R_i \cdot \hat{i}_L[n-1]$), and it is

$$F_m \equiv \frac{\hat{d}[n]}{\hat{v}_c[n] - R_i \cdot \hat{i}_L[n-1]} \quad (3.29)$$

By using this definition, the modulation gains (F_m) of DECPM are derived directly from (3.21) and (3.23) for ‘peak current control law’ and ‘valley current control law’,

Table 3.1: F_m s in different current programmed control

$F_m _{peak}$	$\frac{1}{(M_1 + M_a)T_s}$
$F_m _{valley}$	$\frac{1}{(M_2 + M_a)T_s}$

respectively. Therefore, the modulation gains for DECPM are

$$F_m|_{peak} = \frac{\hat{d}[n-1+D]}{\hat{i}_c[n-1+D] - R_i \cdot \hat{i}_L[n-1]} = \frac{1}{(M_1 + M_a)T_s} \quad (3.30)$$

$$F_m|_{valley} = \frac{-\hat{d}[n]}{\hat{i}_c[n] - R_i \cdot \hat{i}_L[n-1+D]} = \frac{1}{(M_2 + M_a)T_s} \quad (3.31)$$

The derived $F_m|_{peak}$, $F_m|_{valley}$ in (3.30) and (3.31) are same as the modulation gains of the conventional single CPMs. F_m s in different current mode control are summarized in Table 3.1.

3.4.2 Sampling gain (H_e) derivation

From Fig. 3.20, the response from \hat{v}_c to \hat{i}_L can be written like following equation.

$$\frac{\hat{i}_L(s)}{\hat{v}_c(s)} = \frac{F_m|_{peak} G_{id}}{1 + F_m|_{peak} G_{id} R_i H_e|_{peak}} + \frac{F_m|_{valley} G_{id}}{1 + F_m|_{valley} G_{id} R_i H_e|_{valley}} \quad (3.32)$$

And, by rewriting (3.27),

$$\frac{\hat{i}_L(s)}{\hat{v}_c(s)} = \frac{1}{R_i} \frac{1 - \alpha_p}{1 - \alpha_p e^{-sDT_s}} \cdot \frac{1 - e^{-s(1-D)T_s}}{sT_s} + \frac{1}{R_i} \frac{1 - \alpha_v}{1 - \alpha_v e^{-s(1-D)T_s}} \cdot \frac{1 - e^{-sDT_s}}{sT_s} \quad (3.33)$$

By equating (3.32) and (3.33), following equations are derived.

$$\frac{F_m|_{peak} G_{id}}{1 + F_m|_{peak} G_{id} R_i H_e|_{peak}} = \frac{1}{R_i} \frac{1 - \alpha_p}{1 - \alpha_p e^{-sDT_s}} \cdot \frac{1 - e^{-s(1-D)T_s}}{sT_s} \quad (3.34)$$

$$\frac{F_m|_{valley} G_{id}}{1 + F_m|_{valley} G_{id} R_i H_e|_{valley}} = \frac{1}{R_i} \frac{1 - \alpha_v}{1 - \alpha_v e^{-s(1-D)T_s}} \cdot \frac{1 - e^{-sDT_s}}{sT_s} \quad (3.35)$$

By using (3.34) and (3.35), $H_e|_{peak}$ and $H_e|_{valley}$ can be derived respectively. The derivation of the $H_e|_{peak}$ is shown in the following.

At first, let's derive G_{id} which is independent power stage, which we done in CPM. G_{id} is the gain from duty perturbation (\hat{d}) to inductor current perturbation (\hat{i}_L) as shown in Eq.(3.36).

$$G_{id} \equiv \frac{\hat{i}_L}{\hat{d}} \quad (3.36)$$

From the Fig.2.9, the G_{id} can be expressed for all converters as

$$\begin{aligned} G_{id}(s) &= \frac{V_{ap}}{s \cdot L} \\ V_{ap} &= V_{ac} + V_{cp} \\ m_1 &= \frac{R_i \cdot V_{ac}}{L}, \quad m_2 = \frac{R_i \cdot V_{cp}}{L} \\ G_{id}(s) &= \frac{1}{R_i} \frac{m_1 + m_2}{s} \end{aligned} \quad (3.37)$$

With (3.30) and (3.37),

$$F_m|_{peak} \cdot G_{id} = \frac{1}{R_i} \frac{1 - \alpha_p}{s \cdot T_s} \quad (3.38)$$

Table 3.2: H_e s in different current programmed control

$H_e _{CPM}$	$\frac{sT_s}{e^{sT_s} - 1}$
$H_e _{peak}$	$\frac{1 - \alpha_p e^{s(1-2D)T_s}}{1 - \alpha_p} \cdot \frac{sT_s}{e^{s(1-D)T_s} - 1}$
$H_e _{valley}$	$\frac{1 - \alpha_v e^{s(-1+2D)T_s}}{1 - \alpha_v} \cdot \frac{sT_s}{e^{sDT_s} - 1}$

By plugging (3.38) into (3.34), the following equation can be derived,

$$1 + F_m|_{peak} \cdot G_{id} \cdot R_i \cdot H_e|_{peak} = \frac{1 - \alpha_p e^{-sDT_s}}{1 - e^{-s(1-D)T_s}} \quad (3.39)$$

Therefore, the sampling gain for peak current control law ($H_e|_{peak}$) can be derived like

$$H_e|_{peak} = \frac{1 - \alpha_p e^{s(1-2D)T_s}}{1 - \alpha_p} \cdot \frac{sT_s}{e^{s(1-D)T_s} - 1} \quad (3.40)$$

By doing a similar derivation, the sampling gain for valley current control law ($H_e|_{valley}$) is

$$H_e|_{valley} = \frac{1 - \alpha_v e^{s(-1+2D)T_s}}{1 - \alpha_v} \cdot \frac{sT_s}{e^{sDT_s} - 1} \quad (3.41)$$

The sampling gains (H_e) for CPM and DECPM are summarized in Table 3.2.

3.4.3 Simulation results of DECPM and its comparison with the conventional single CPM

The SIMPLIS simulation tool was used to verify the DECPM model. The SIMPLIS simulation results have shown the accurate predictions of the converter transfer functions in various literature [41, 45, 46]. Fig. 3.21 to Fig. 3.26 shows the comparisons of the G_{vc} (control to output voltage transfer function) for the proposed DECPM model, the peak CPM model and the SIMPLIS simulation result. The G_{vc} of DECPM can be written from the small signal model shown in Fig. 3.20, and it is

$$G_{vc}|_{DECPM} = \frac{\hat{v}_o(s)}{\hat{v}_c(s)} = \frac{F_m|_{peak} G_{vd}}{1 + F_m|_{peak} G_{id} R_i H_e|_{peak}} + \frac{F_m|_{valley} G_{vd}}{1 + F_m|_{valley} G_{id} R_i H_e|_{valley}} \quad (3.42)$$

The parameters of the converters for the comparisons are as follows; $V_{in} = 3.3V$, $L = 235nH$, $C = 280nF$, and $R_o = 5\Omega$, and all control has 10MHz of the switching frequency and M_a set to $1.6/T_s$. Fig. 3.21 to Fig. 3.23 are buck mode, and Fig. 3.24 to Fig. 3.26 are boost mode. It is shown that the proposed DECPM model matches well with the SIMPLIS simulation results. As consistent with the current loop gain mentioned in the previous section, DECPM shows the larger gain than the peak CPM at high frequency for all duty ratio.

The transfer function changes with the different duty ratios for the DECPM and the peak CPM are compared from Fig. 3.27 to Fig. 3.30. The Fig. 3.27 and Fig. 3.28 are the transfer functions of G_{vc} in peak CPM and DECPM with different output voltages at the input voltage of 3.3V. In the peak CPM, the magnitude variation is $2dB$, the phase variation is 44.12° at $1MHz$. In the DECPM, the magnitude variation is $2.27dB$, but the phase variation is 29.13° at $1MHz$. The Fig. 3.29 and Fig. 3.30 are the transfer functions

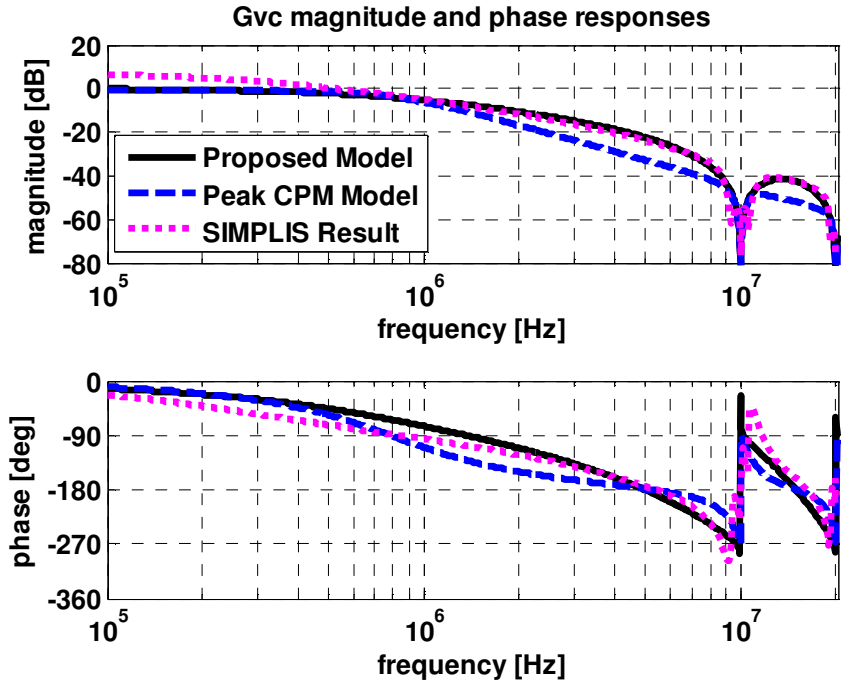


Figure 3.21: G_{vc} when $V_{in} = 3.3V$ and $V_{out} = 0.1V$

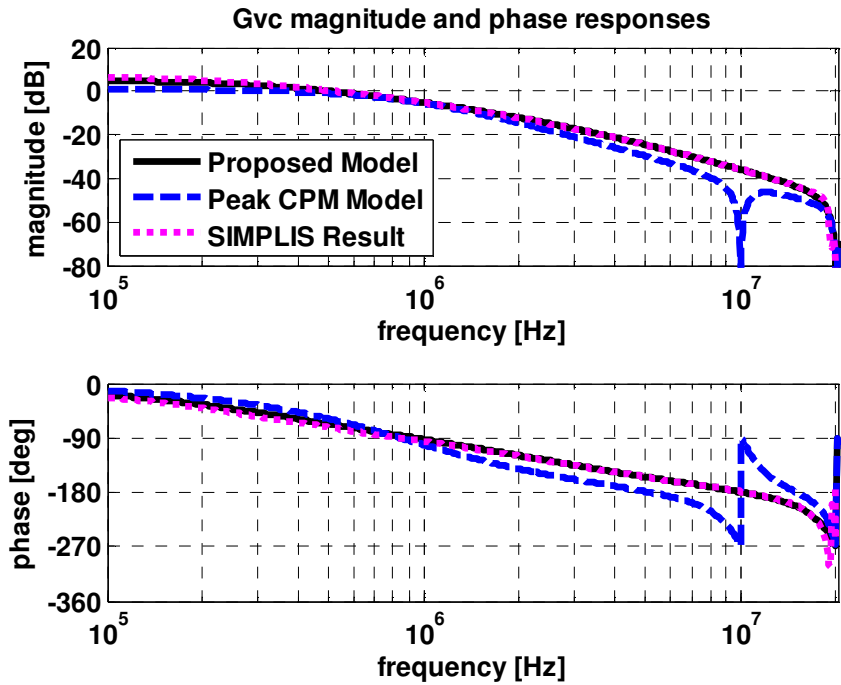


Figure 3.22: G_{vc} when $V_{in} = 3.3V$ and $V_{out} = 1.65V$

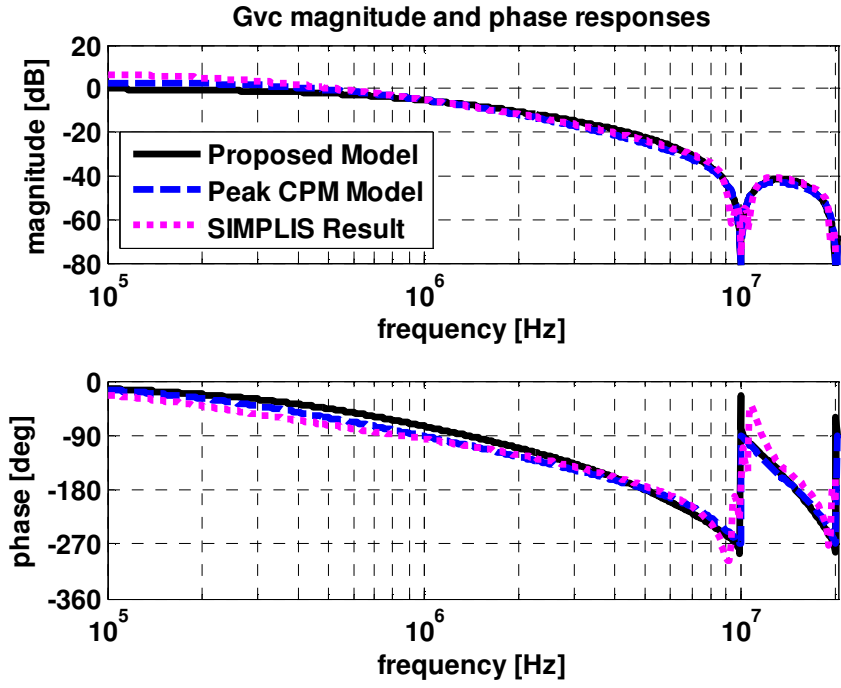


Figure 3.23: G_{vc} when $V_{in} = 3.3V$ and $V_{out} = 3.2V$

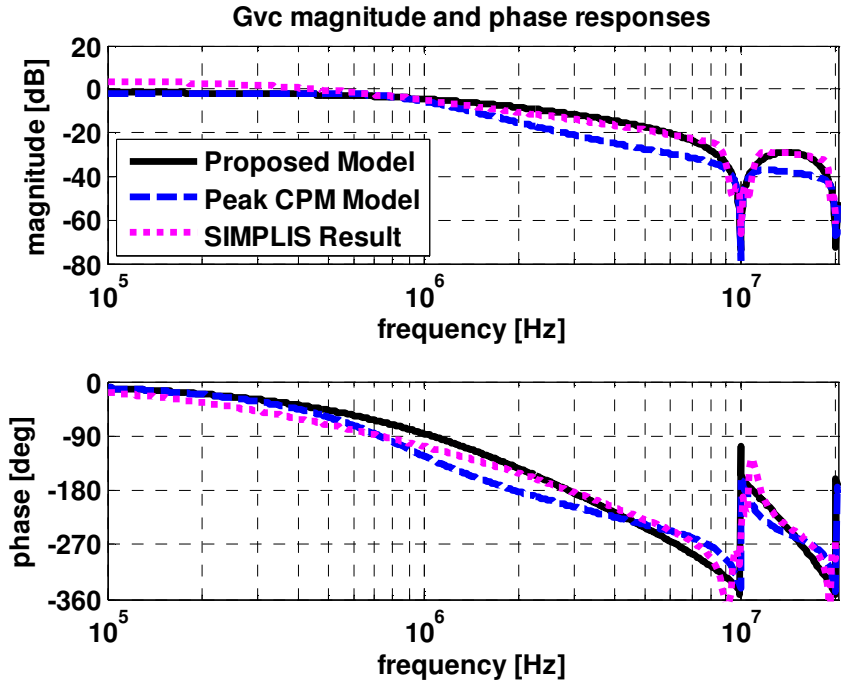


Figure 3.24: G_{vc} when $V_{in} = 3.3V$ and $V_{out} = 3.4V$

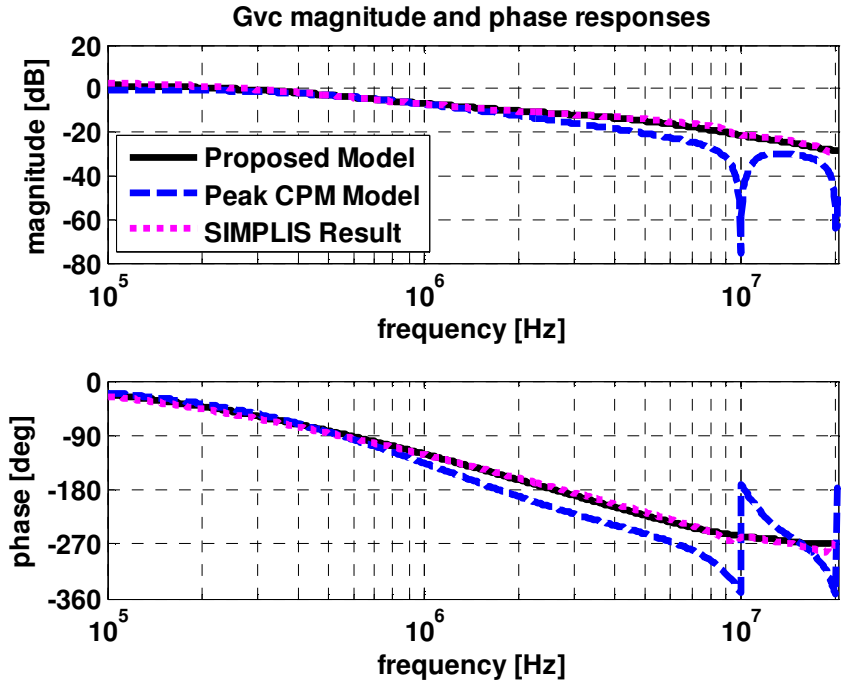


Figure 3.25: G_{vc} when $V_{in} = 3.3V$ and $V_{out} = 5V$

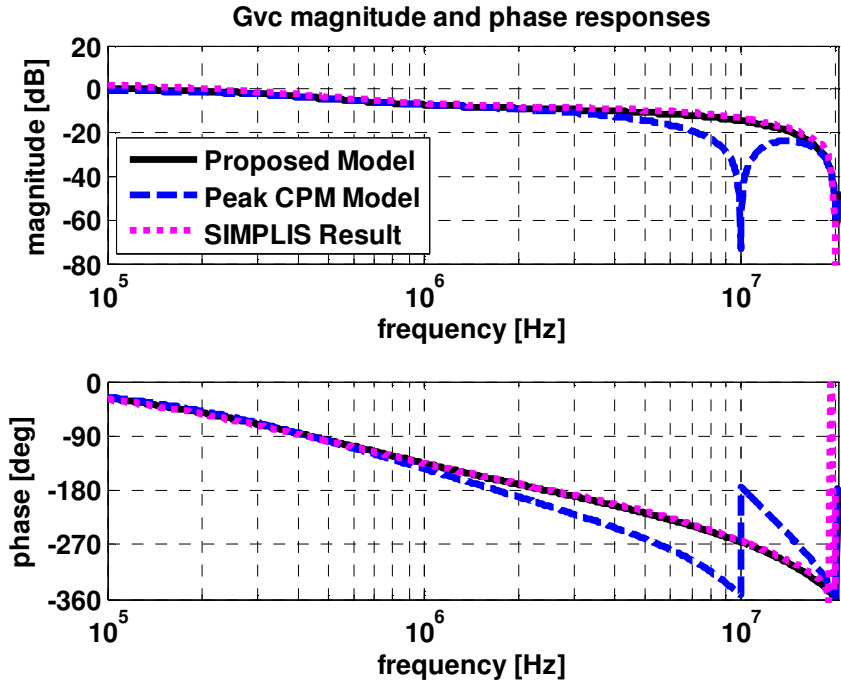


Figure 3.26: G_{vc} when $V_{in} = 3.3V$ and $V_{out} = 6.6V$

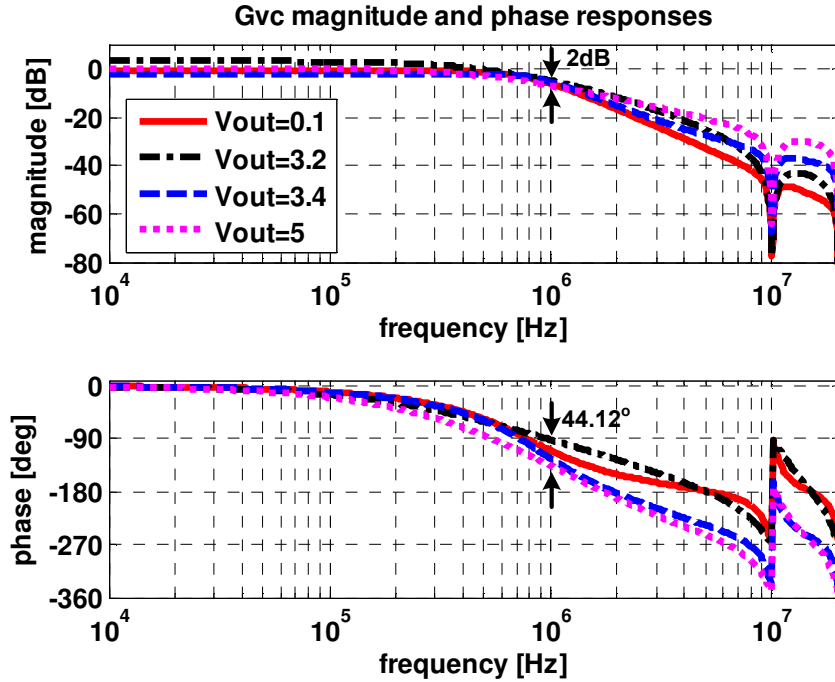


Figure 3.27: G_{vc} in Peak CPM with different output voltage

of G_{vc} in peak CPM and DECPM with different input voltages at the output voltage of 3.3V. In the peak CPM, the magnitude variation is $1.9dB$, the phase variation is 45° at $1MHz$. In the DECPM, the magnitude variation is $1dB$, but the phase variation is 24.4° at $1MHz$. These comparisons tell that the DECPM shows less phase lag and more constant dynamics than the peak CPM at high frequency. Therefore, more optimized compensator can be designed to achieve a stable system by the DECPM than by the peak CPM for the high bandwidth and wide voltage range applications.

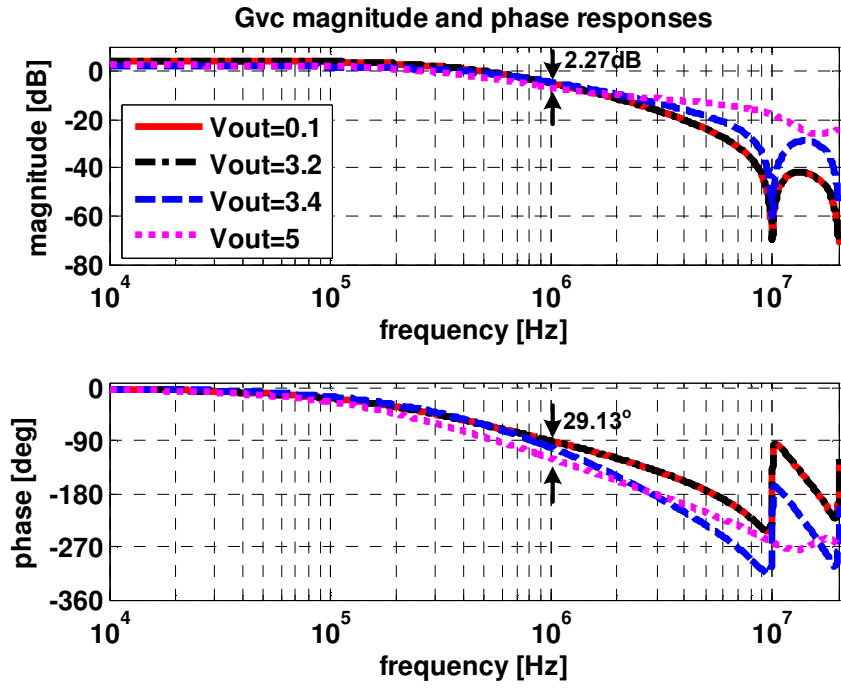


Figure 3.28: G_{vc} in DECPM with different output voltage

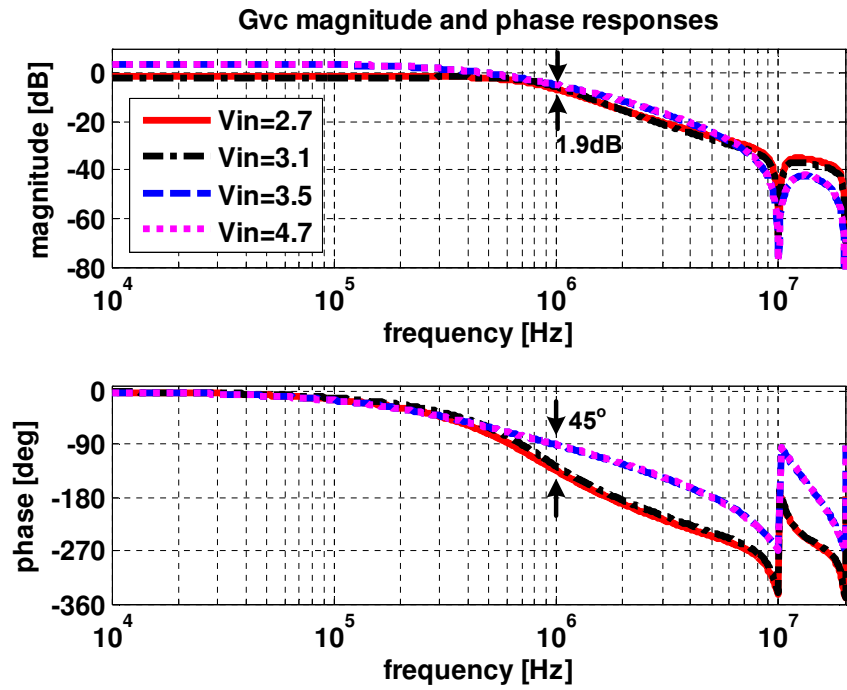


Figure 3.29: G_{vc} in Peak CPM with different input voltage

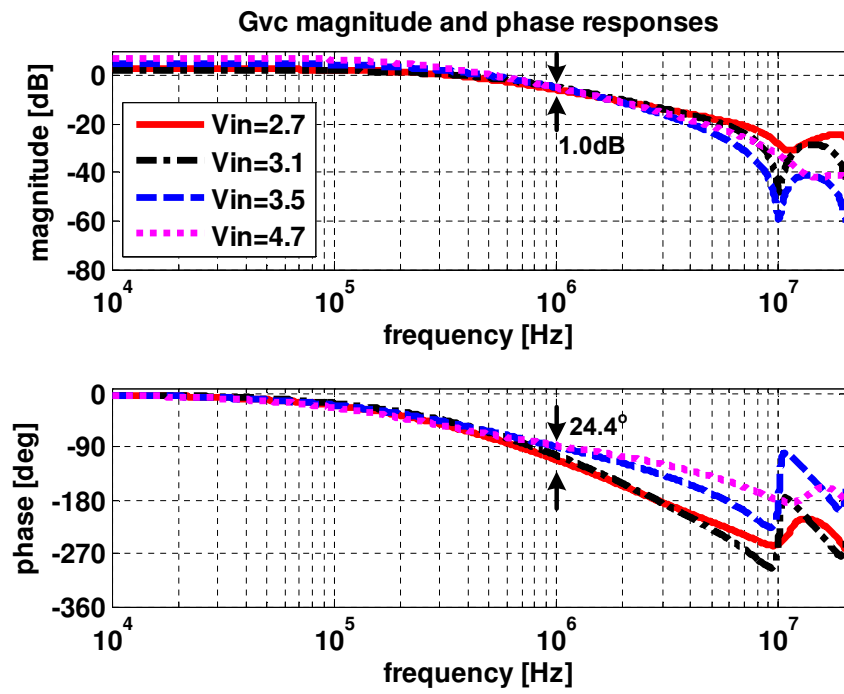


Figure 3.30: G_{vc} in DECPM with different input voltage

Chapter 4

Design of 10MHz CMOS 4 Switch Buck Boost Converter (4SBBC) with DECPM control

In this chapter, a 10MHz CMOS 4 Switch Buck Boost converter with DECPM control is introduced. Due to its wide input and output voltage range capability, a four switch buck boost converter (4SBBC) is getting more popular in the portable and vehicle applications which use a battery as an input source and require longer battery operation time [2, 3, 4, 18]. However, a stable control of this converter for the wide input and output voltage range applications is not easy to achieve because the transfer function of the system changes with different operating points (duty cycles). Especially, the 4SBBC mostly works in either buck or boost mode to save power consumption by operating only two switches in a switching cycle. In this case, the transfer function change is even more severe due to the different system dynamics from each buck and boost modes. Therefore, a smooth mode change in the 4SBBC is an issue[4, 47, 48]. The conventional current

programmed mode (CPM) control makes the converter dynamics less sensitive to the changes of the input and output voltages than the voltage mode control at the relatively low frequency range, but, in the high speed converter design, it is necessary to have constant dynamics up to high frequencies.

Due to the fact that DECPM has a higher sampling frequency of the control than the switching frequency of the power stage and has a larger current loop gain at high frequency than conventional CPM, as mentioned in previous chapter, DECPM is a preferred candidate to control high frequency and wide range DC-DC converters such as a 4BSSC. A 10MHz 4SBBC is designed with double edge current programmed mode (DECPM) control in a JAZZ $0.5\mu m$ process. Fig. 4.1 shows a block diagram of the proposed 4SBBC with DECPM control. The DECPM eliminates a subharmonic oscillation which is a well known problem in the conventional CPM, and it makes the 4SBBC have more constant dynamics for wide input and output voltage range up to high frequency. Therefore, a stable operation and a smooth mode change between the buck and boost mode are achieved with a peak efficiency of 80% at the switching frequency of 10MHz.

4.1 Architecture

Fig. 4.1 shows the block diagram of the implemented 4SBBC with DECPM. This diagram shows two parts of the system which are the ‘power stage’ and the ‘controller’. The power stage is composed of 4 power switches(A, B, C, D), output inductor (L) and output capacitor (C_o). The resistor (R_f) and capacitor (C_f) are for the current sensing network and the resistor (R_o) represents the load. The controller is the bottom block of the Fig. 4.1 and is composed of current sensor, ramp generator, analog adder, comparator, digital logic, compensator, voltage/current references and gate drivers.

The power switches are made of 2 PMOSes and 2 NMOSes. To reduce the dynamic power loss of the converter, the converter was designed to operate in either buck or boost mode. When input voltage (V_{in}) is higher than output voltage (V_{out}), only the A and B switches are operating and the switch C keep on and the switch D keep off for all switching period (T_s) to work like a buck converter. When input voltage (V_{in}) is lower than output voltage (V_{out}), only the C and D switches are operating and the switch A keep on and the switch B keep off for all switching period (T_s) to work like a boost converter.

Fig. 4.1 shows the implementation of the aforementioned function into a DECPM scheme. A ramp generator provides two ramp signals (V_{ramp} and $-V_{ramp}$) which are 180° phase shifted and have a frequency of half the switching frequency. Each ramp signal has positive and negative slopes (M_a and $-M_a$). Both ramp signals are added to the sensed inductor current signal ($R_i \cdot I_L$) through an analog adder. These added signals are denoted by V_u and V_s . These V_u and V_s are compared with the control voltage (V_c) which is the output of compensator. The outputs of comparator (V_{uo} and V_{so}) are processed through a digital logic block to generate the PWM signals for the buck and boost mode. The PWM digital logic block is implemented based on (4.1). The V_r and $-V_r$ in (4.1) stand for the portion of the positive slope (M_a) and negative slope ($-M_a$) of both ramp signals (V_{ramp} and $-V_{ramp}$) respectively.

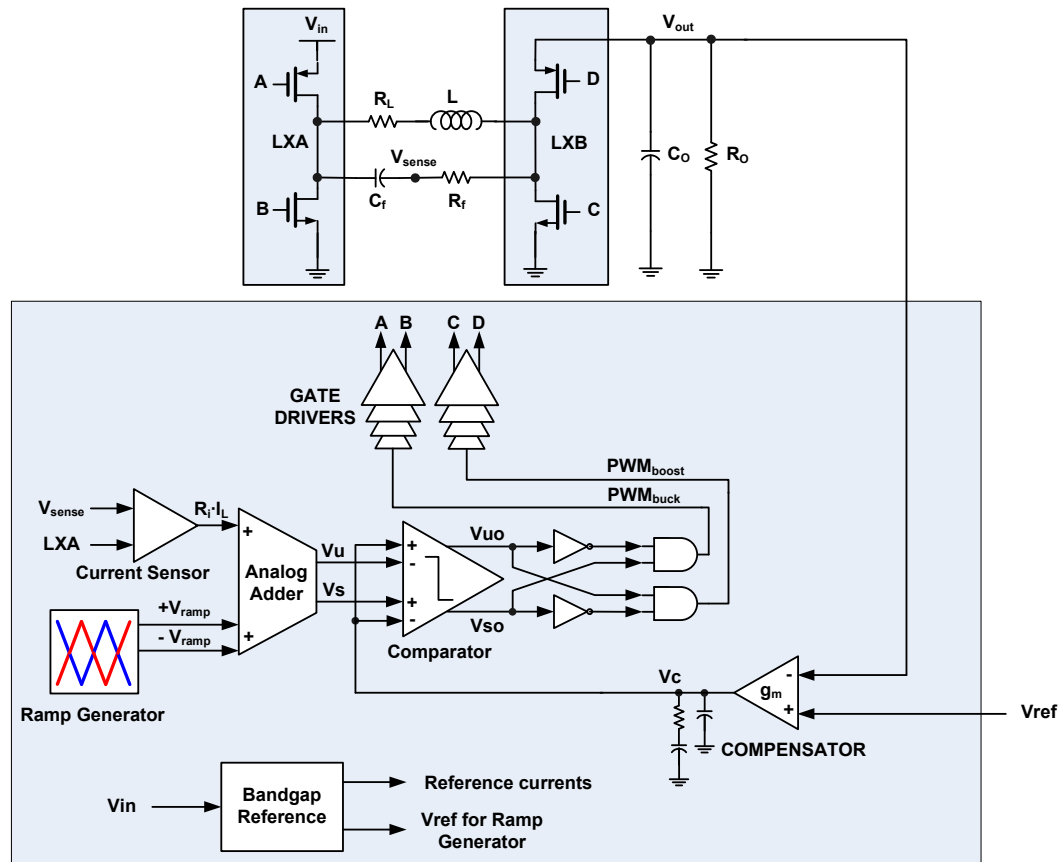


Figure 4.1: Block diagram of 4SBBC

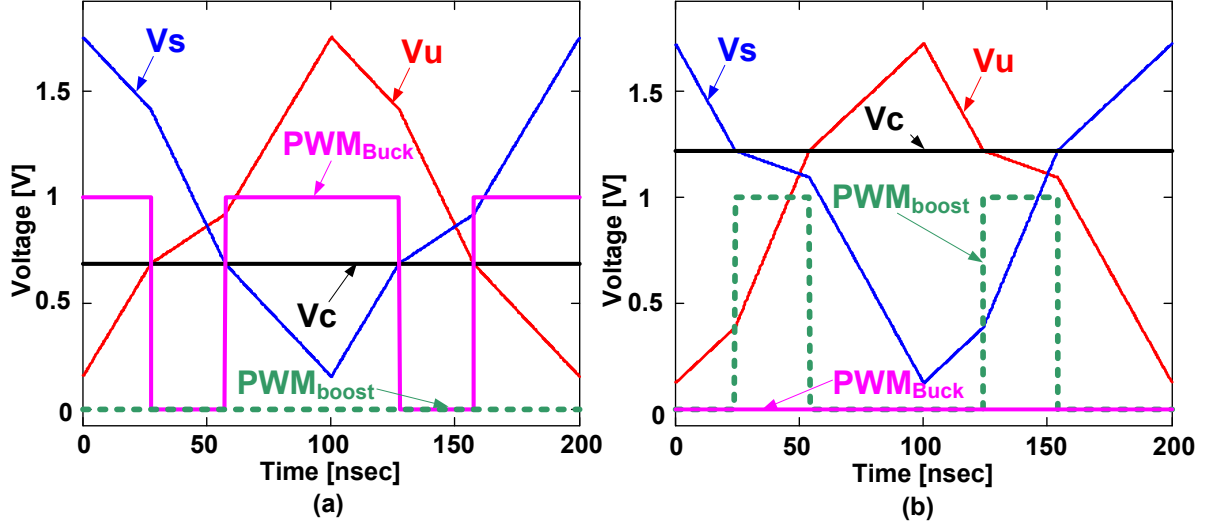


Figure 4.2: Implemented key signal waveforms for DECPM (a) Buck mode (b) Boost mode

Fig. 4.2 shows the key signal waveforms of the implemented DECPM control for the 4SBBC. Fig. 4.2 (a) is the case of the buck mode with a duty ratio of 0.7, and Fig. 4.2 (b) is the boost mode with a duty ratio of 0.3. It is explicitly shown here that PWM ON is controlled by limiting the valley point of the inductor current, and PWM OFF is controlled by limiting the peak point of the inductor current. Therefore, double edge modulation of the PWM signals is achieved.

$$PWM\ ON = V_c - (I_L - V_r) \quad (4.1)$$

$$PWM\ OFF = (I_L + V_r) - V_c \quad (4.2)$$

4.2 Transistor level implementation

4.2.1 Current sensor

In order to sense the continuous current information, the ‘Filer-Sense the inductor’ technique [49] is used. This technique uses a RC network (R_f, C_f) to filter the voltage across the inductor and sense the current through the equivalent series resistance (R_L) of the inductor (L) as shown in Fig. 4.1. The design equation of the sensing network is shown in (4.3).

$$V_{C_f} = V_{sense} = I_L \cdot R_L \quad (4.3)$$

$$, \text{ where } \frac{L}{R_L} = R_f \cdot C_f \quad (4.4)$$

To sense the inductor current information by using above technique, there are two major design issues. One is wide voltage swing at LXA and Vsense nodes in Buck mode. During the buck mode operation, power switch A and B are operating in each cycle, so the voltage at LXA and Vsense nodes change from V_{in} to ground and vice versa. Fig. 4.3 shows the waveforms of LXA and Vsense nodes for buck and boost modes. As expected, the voltage swing is rail to rail during the buck mode operation. To sense the differential voltage across the C_f with such a wide common mode voltage change, the input stage of the current sensor should cover the rail to rail common mode range. Another design issue is that wide bandwidth of the current sensor is required. The switching frequency used here is 10MHz. To sense such a high frequency current information without distortion, a high speed current sensor scheme is needed. Therefore, Differential Difference Amplifier (DDA) architecture which is shown in Fig.4.4 is used for such a high speed current sensor [50, 51]. The DDA provides a beneficial separation between the signal input and

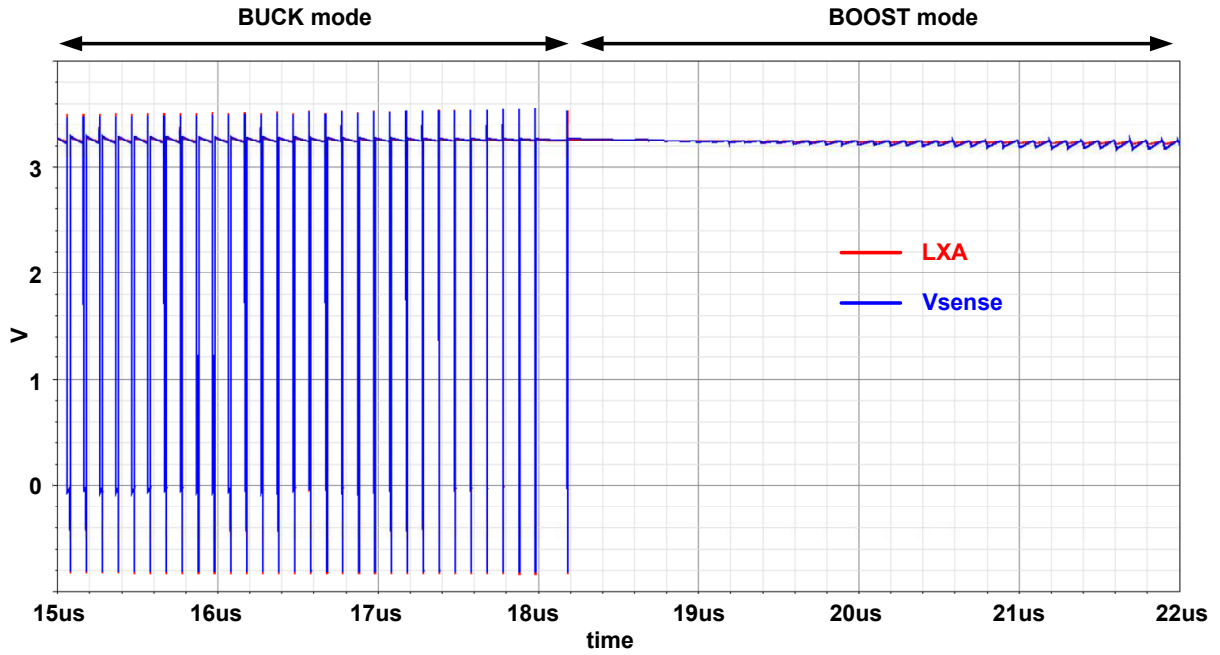


Figure 4.3: LXA and Vsense for Buck and Boost mode

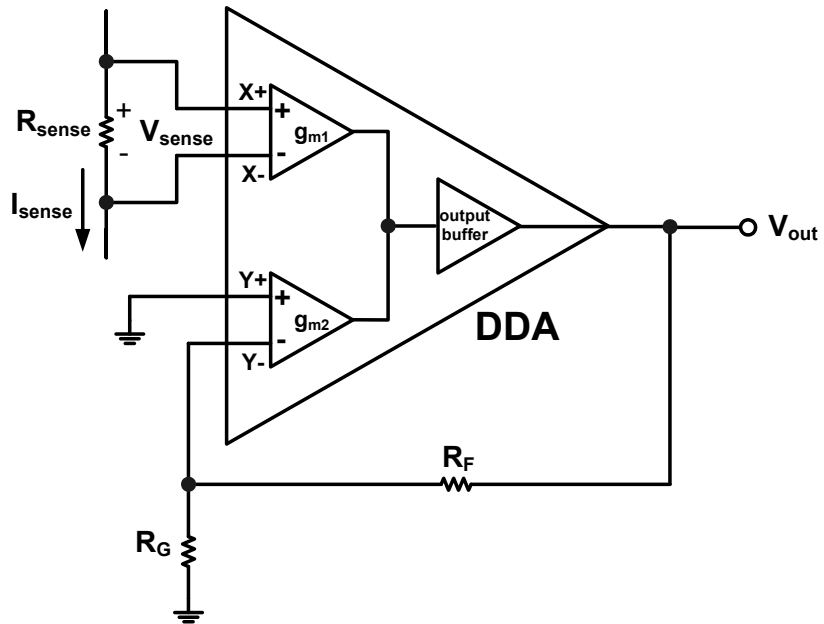


Figure 4.4: Current Sensor with the Differential Difference Amplifier

the feedback network. The brief operation of DDA is like following. Because of the infinite input impedance of output buffer in DDA, all the current generated by the G_{m1} block which senses the V_{sense} flows into output node of another G_{m2} block. This makes the input voltage of the bottom G_m block copy the same voltage as V_{sense} but with different polarity if those G_{m1} and G_{m2} blocks are identical. This copied voltage will be applied across the R_G and amplified to V_{out} which corresponds to (4.5). The CADENCE simulation shows that the 3dB bandwidth of this DDA is more than 20MHz for rail-to-rail input voltage range.

$$V_{out} = \left(1 + \frac{R_F}{R_G}\right) \cdot V_{sense} \quad (4.5)$$

Fig.4.5 is the transistor level schematic of the implemented DDA for the current sensor. In order for the DDA to operate with rail-to-rail input range during the buck mode operation, both PMOS and NMOS input stages are used for both g_{m1} and g_{m2} . And class-AB output stage is designed for high output current capability and low power consumption.

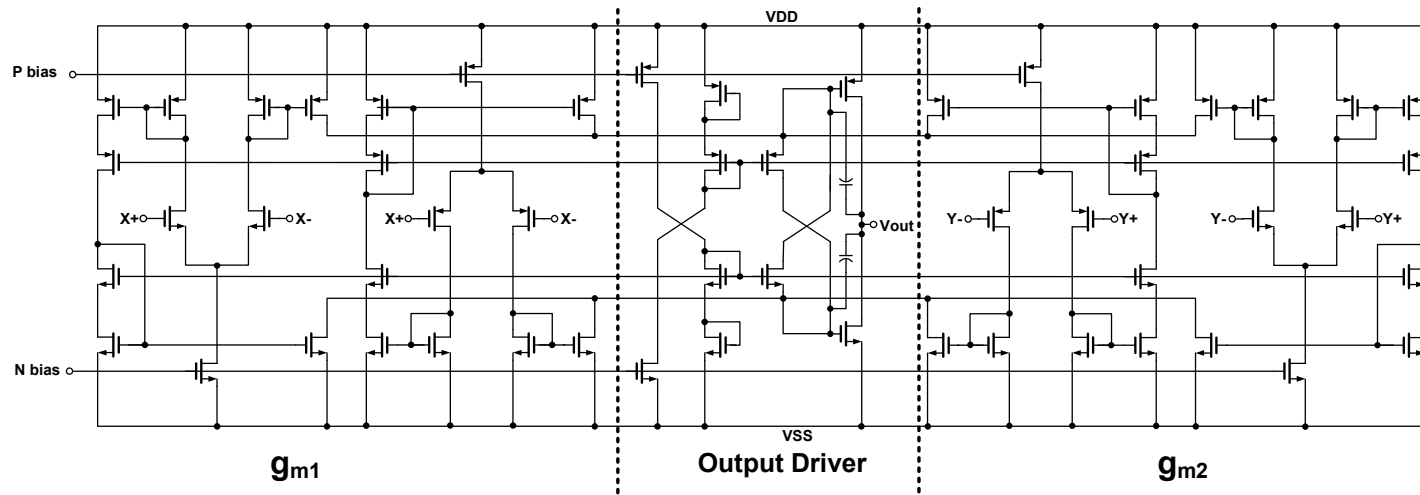


Figure 4.5: Transistor level schematic of the Differential Difference Amplifier for the current sensor

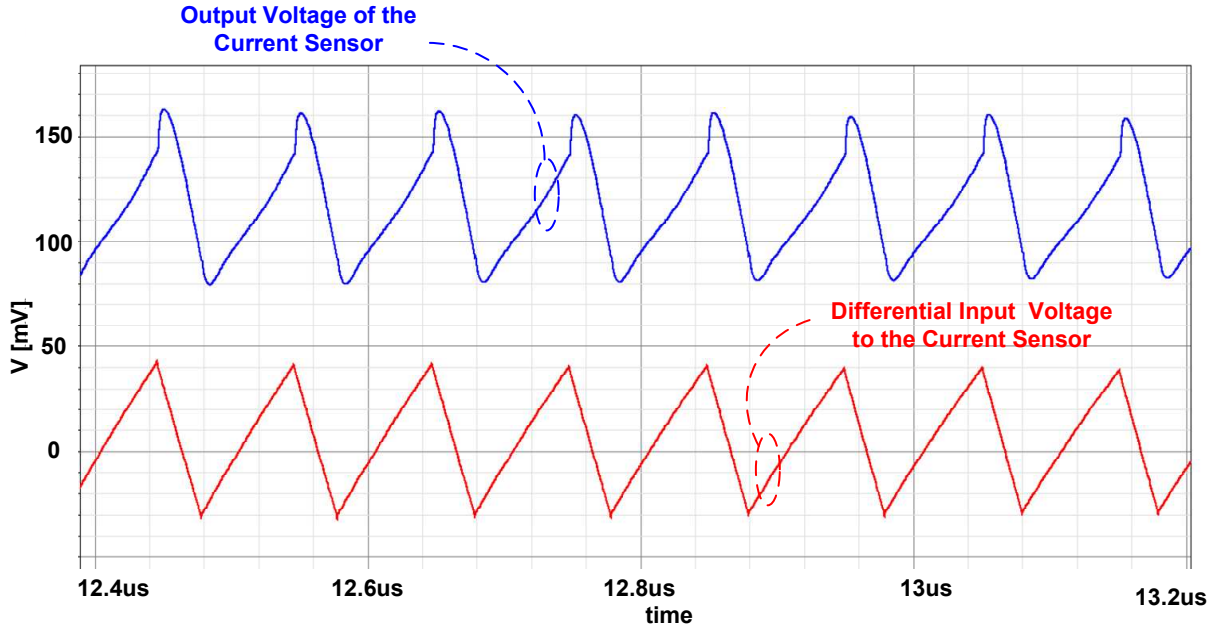


Figure 4.6: Input and output voltage of the current sensor at Buck mode

Fig.4.6 and Fig.4.7 are the CADENCE simulation results of the current sensor for buck and boost mode operation respectively. This simulation results show that the implemented circuit senses the high frequency current information well.

4.2.2 Ramp Generator

To implement the double edge current programmed mode control explained in the previous section, Two double side ramp signals are needed which are 180° phase shifted accurately each other and keep the maximum and minimum values of each signals same. The Fig.4.8 shows the block diagram of the ramp generator performing the functions mentioned just above. To generate the double side ramp signals, two current sources (I_1 and I_2) are used. These two current sources charge and discharge the capacitors. The M_1 , M_2 , M_3 and M_4 work as switches to change the current path from V_{ramp} or $-V_{ramp}$.

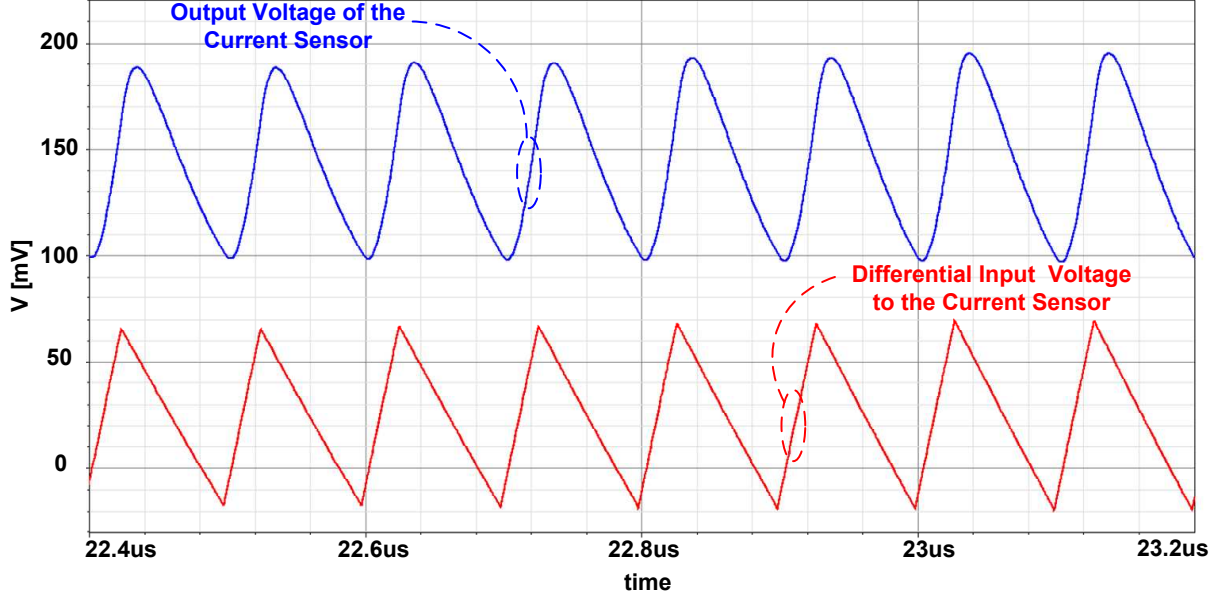


Figure 4.7: Input and output voltage of the current sensor at Boost mode

When the voltage at either V_{ramp} or $-V_{ramp}$ reaches maximum voltage (V_H), the comparator generates signals to switch the current path to V_{ramp} or $-V_{ramp}$ nodes. If the values of the current sources are not matched, the peak to peak voltage of V_{ramp} and $-V_{ramp}$ keep increasing or decreasing as time goes by. To accurately control the both rising and falling slopes of the ramp signal and the 180° phase shift of the two ramp signals, the common mode feedback (CMFB) scheme was implemented to keep the average voltage of V_{ramp} and $-V_{ramp}$ to (V_M) which is half the peak to peak ramp signal. The frequency of these ramp signals is determined by the Equ.(4.6) and it is half the switching frequency of the power stage. The FreqSA, FreqSB and FreqSC represent digital input pins used for changing the current value to vary frequency.

$$f_{ramp} = \frac{I}{4 \cdot C \cdot (V_H - V_M)} = 0.5 \times f_s \quad (4.6)$$

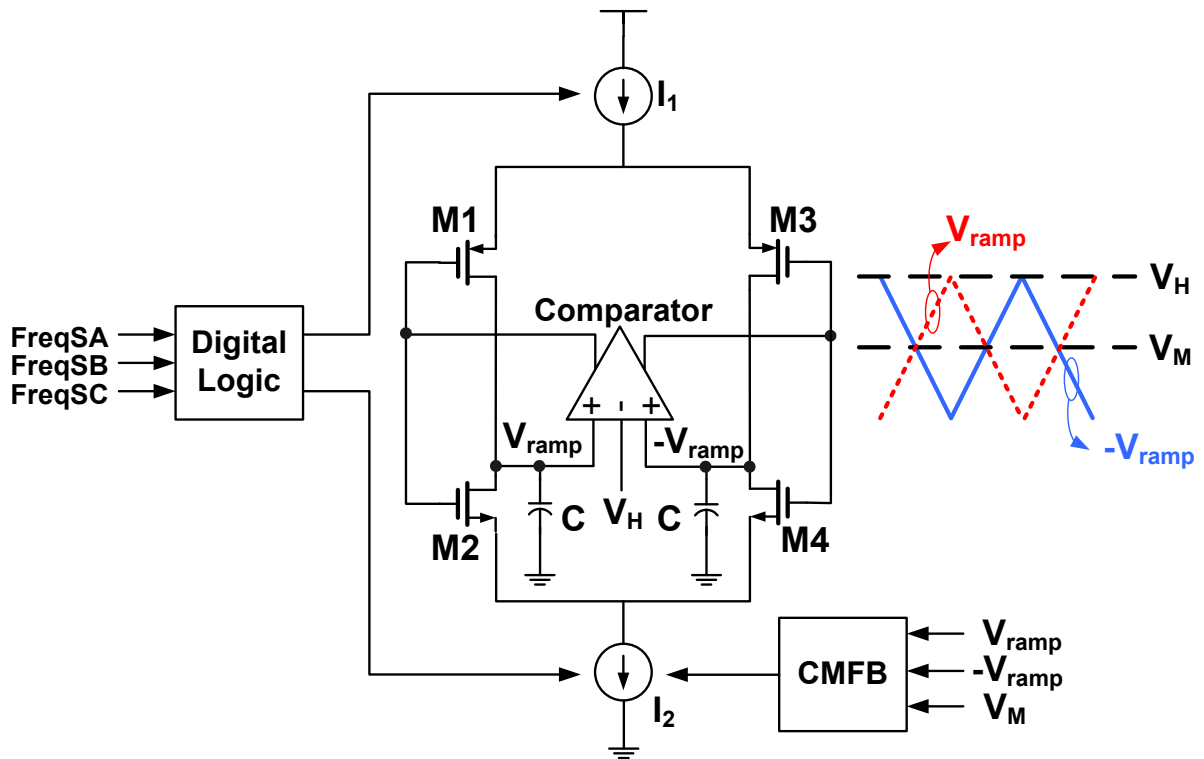


Figure 4.8: Ramp Generator circuit

Table 4.1: Design parameters for 4SBBC

Input nominal voltage	V_{in}	3.3V
Output voltage range	V_{out}	0.7V – 5V
Switching frequency	f_{sw}	10MHz
Output inductor	L	235nH
Output capacitor	C_o	280nF
Load resistor	R_o	10Ω
Output filter resonant frequency	$\frac{1}{2\pi\sqrt{LC}}$	620kHz
Compensator	F_c	$2.06 \times 10^6 \frac{1 + \frac{s}{2\pi \times 254.65 \times 10^3}}{s(1 + \frac{s}{2\pi \times 3.183 \times 10^6})}$
Worst case cut off frequency	f_c	1.1MHz

4.2.3 System summary

Table 4.1 shows the summary of design parameters of the implemented 4SBBC with an appropriate compensator. A two-pole and single zero network was used for the compensator to compensate the outer voltage loop.

Fig. 4.9 shows the SIMPLIS simulation results of the voltage regulation loop gains ($T_2|_{DECPM}$) with the current loop closed for the designed 4SBBC. According to the small signal model from the previous section, the voltage regulation loop gain for DECPM ($T_2|_{DECPM}$) is derived below.

$$T_2|_{DECPM} = \frac{T_v|_{peak}}{1 + T_i|_{peak}} + \frac{T_v|_{valley}}{1 + T_i|_{valley}} \quad (4.7)$$

where,

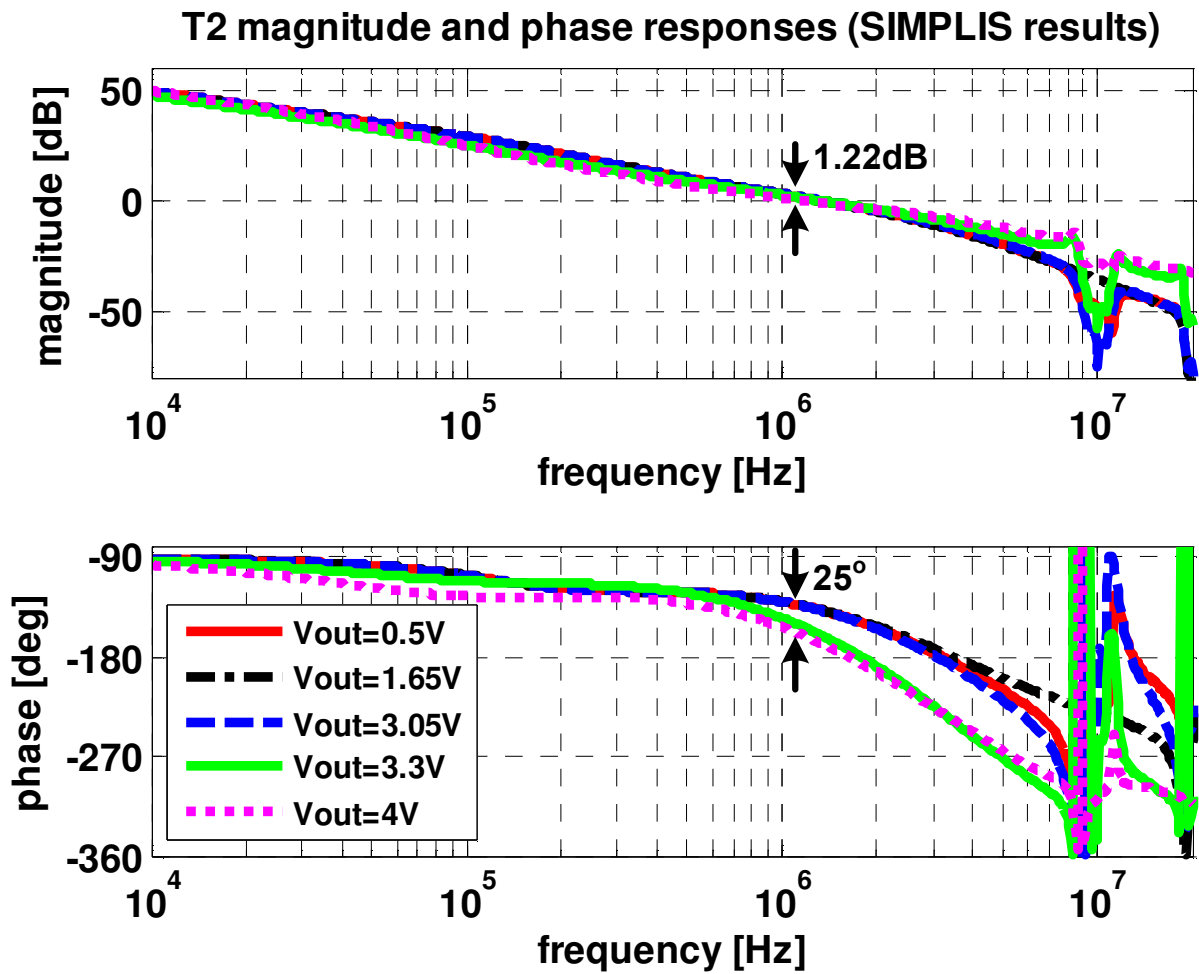


Figure 4.9: SIMPLIS results of the voltage regulation loop gains ($T_2|_{DECPM}$) with the different output voltages when $V_{in} = 3.3V$

$$T_v|_{peak} = F_c F_m|_{peak} G_{vd} \quad (4.8)$$

$$T_i|_{peak} = F_m|_{peak} G_{id} R_i H_e|_{peak} \quad (4.9)$$

$$T_v|_{valley} = F_c F_m|_{valley} G_{vd} \quad (4.10)$$

$$T_i|_{valley} = F_m|_{valley} G_{id} R_i H_e|_{valley} \quad (4.11)$$

Here the F_c represents the transfer function of the compensator. The results in Fig. 4.9 were obtained with a fixed input voltage of 3.3V and different output voltages. This figure shows the worst case cutoff frequency of 1.1MHz and the worst case phase margin of 30°. The magnitude and phase variation at 1.1MHz are 1.22dB and 25°, respectively.

4.3 Measurement

The proposed 4SBBC with DECPM was implemented in a JAZZ 0.5 μ m 5V CMOS technology. It measures 2 mm x 1.7 mm and uses the QFN32 package. Fig. 4.11 shows a micro photograph of the chip. Fig. 4.11 is an evaluation board for the 4SBBC. Fig. 4.12 shows the measurement waveforms to verify the wide range operation of the implemented converter. The LXA and LXB stand for the buck and boost switching nodes respectively which are designated in Fig. 4.1. In all cases, a 10kHz saw tooth reference signal is applied to generate the output voltage (V_{out}) from 1V to 5V, but different input voltages are applied to each case which has a range from 2.8V to 4.7V. As shown in Fig. 4.12, the implemented converter with DECPM has the stable operation with a wide input and output voltage range. The waveforms of LXA and LXB nodes show clearly that the implemented converter works in either only buck or boost mode for a wide voltage range. Fig. 4.13 shows the smooth transition between buck and boost mode. In this figure, a 10kHz saw tooth reference signal (V_{ref}) is applied to change the output voltage (V_{out})

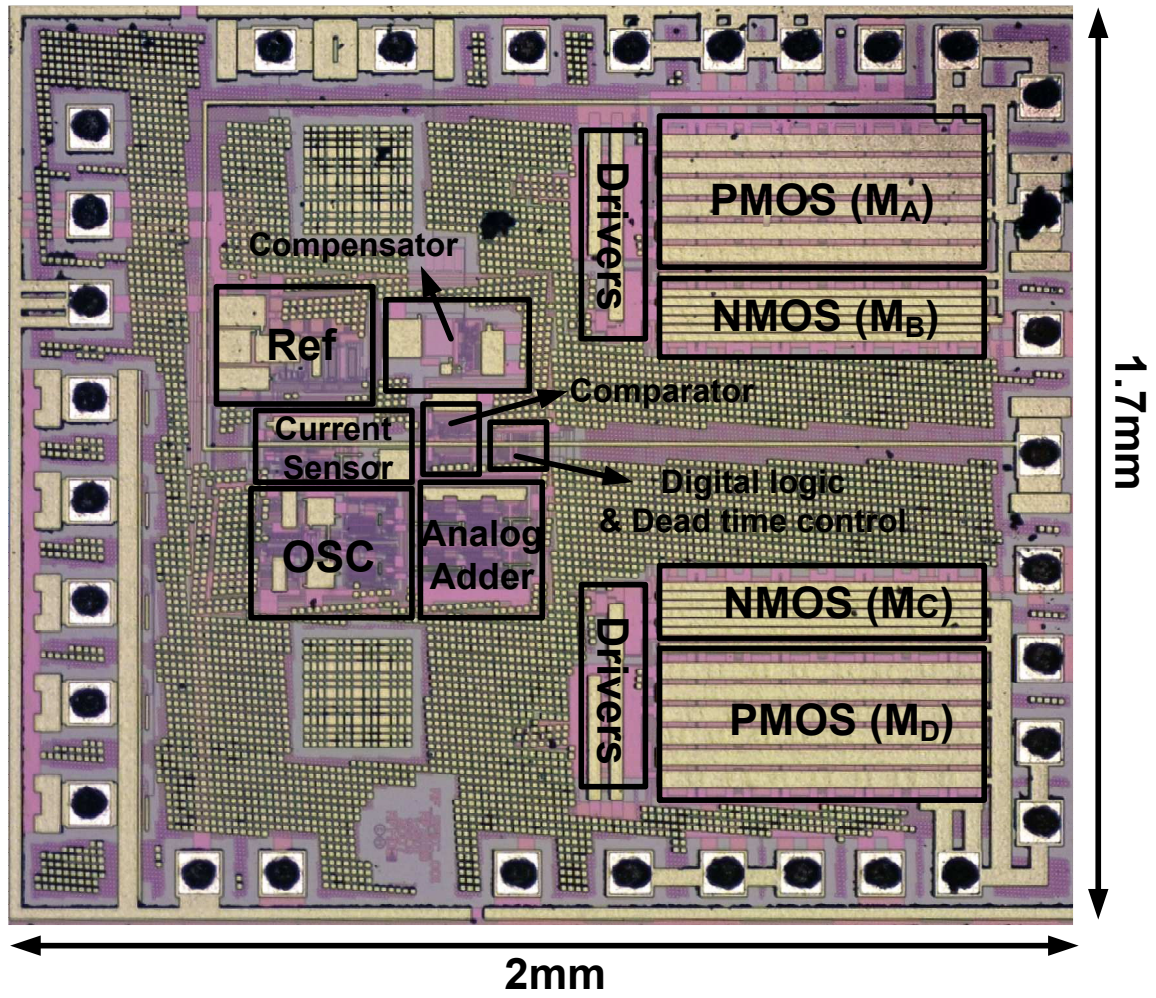


Figure 4.10: Micro photograph of the chip

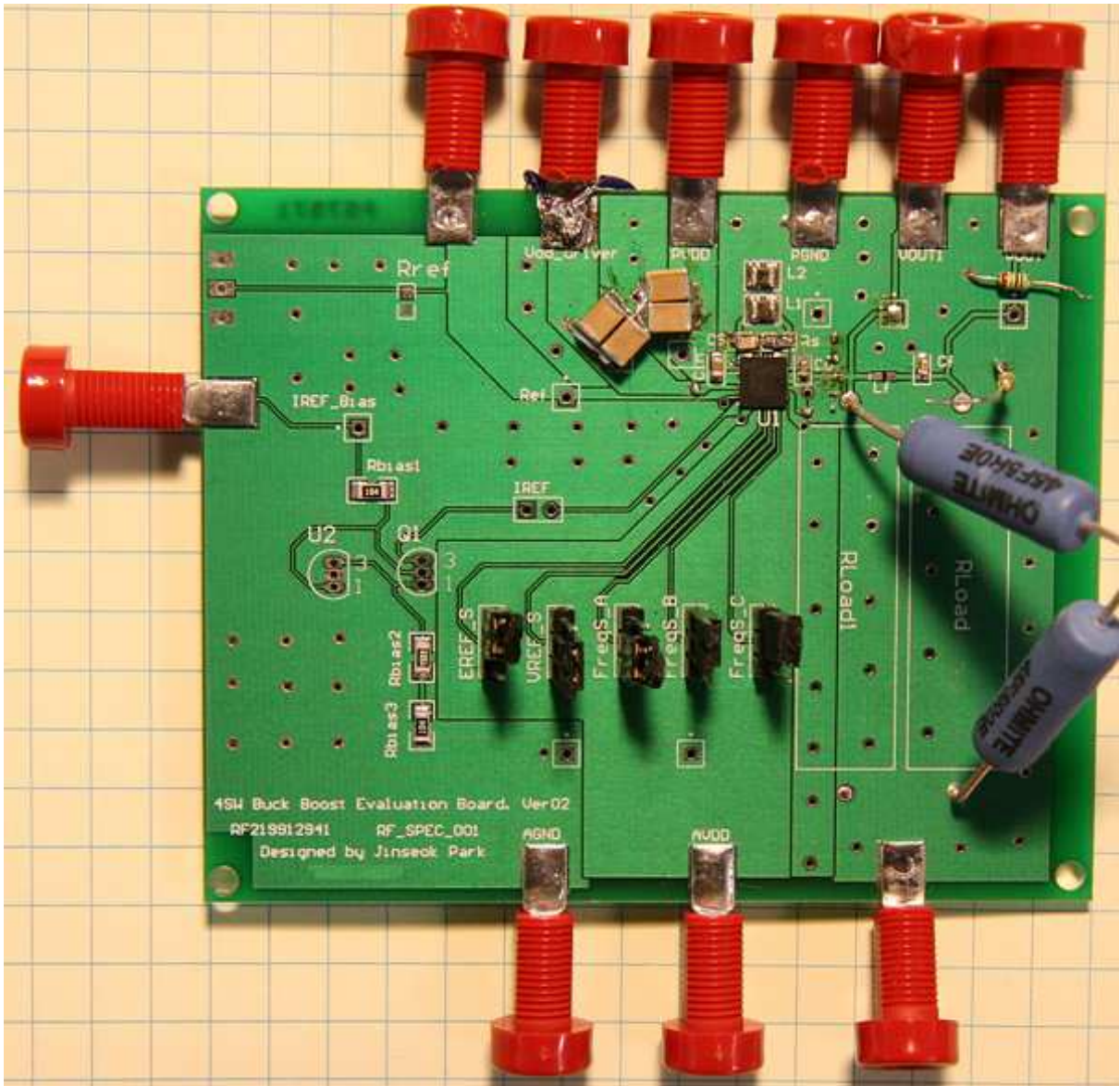


Figure 4.11: Evaluation board for 4SBBC

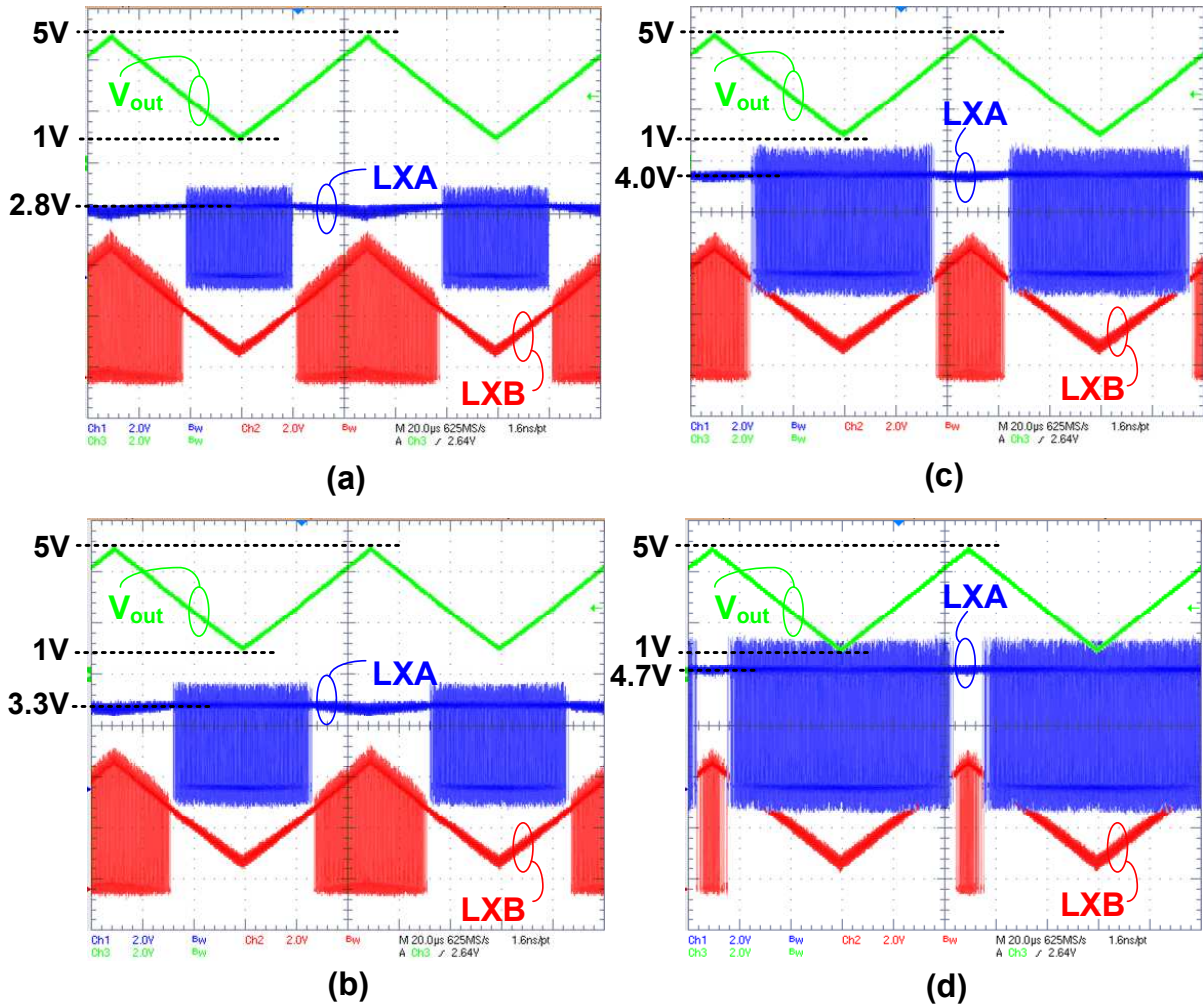
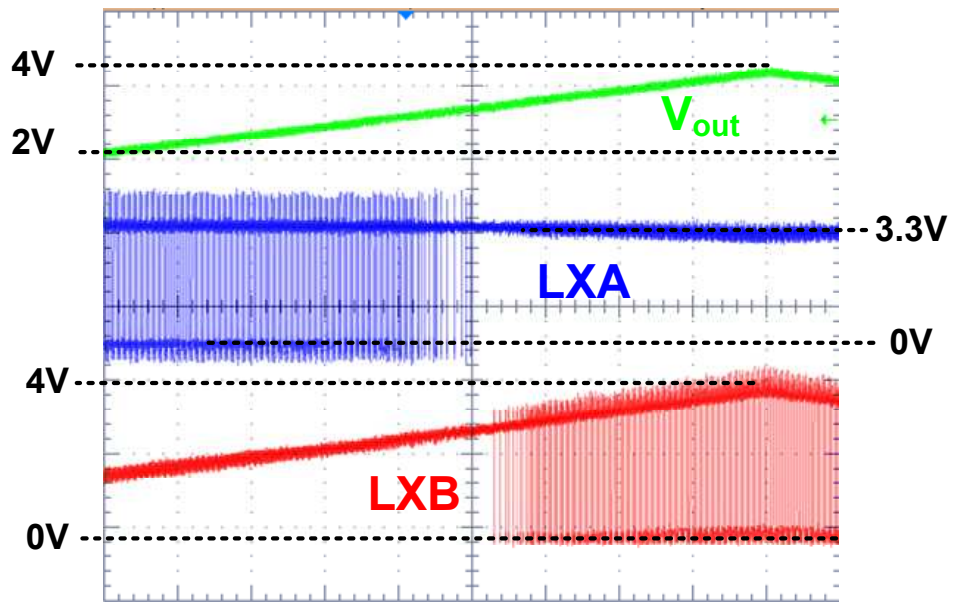
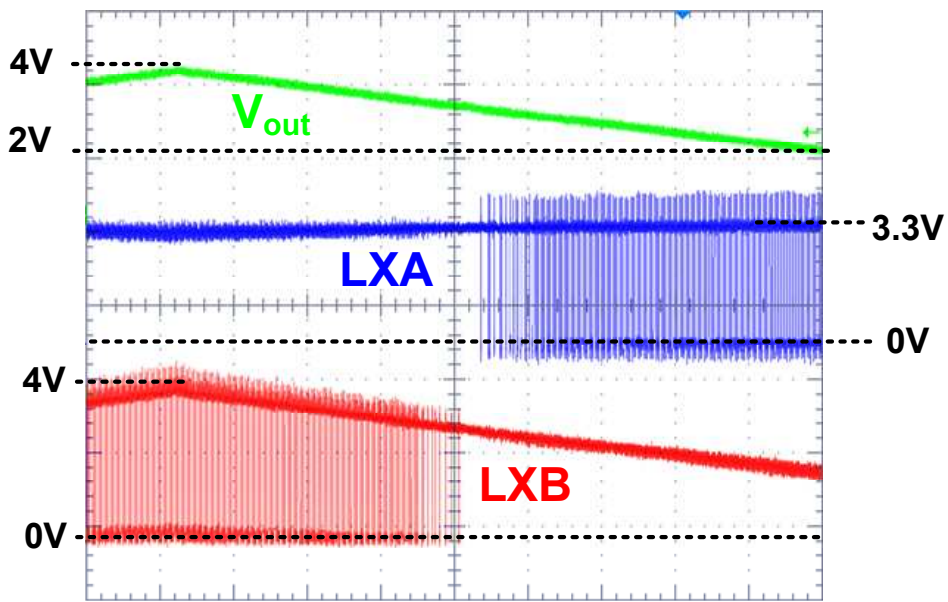


Figure 4.12: Measurement of the V_{out} , LXA and LXB node with the different V_{in} (a) $V_{in}=2.8V$ (b) $V_{in}=3.3V$ (c) $V_{in}=4.0V$ (d) $V_{in}=4.7V$



(a)



(b)

Figure 4.13: Measurement of the V_{out} , LXA and LXB nodes at $V_{in} = 3.3V$ (a) When V_{out} change from 2V to 4V (b) When V_{out} change from 4V to 2V

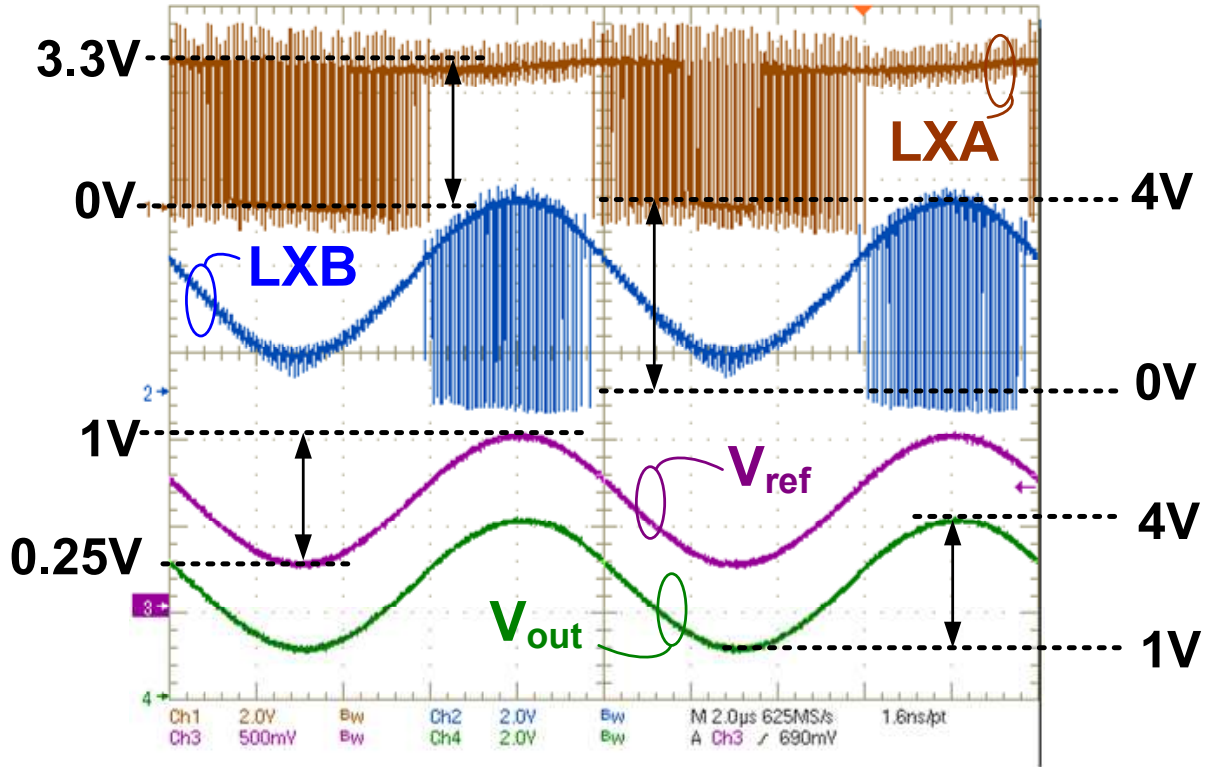


Figure 4.14: Measured waveforms of the V_{ref} , V_{out} , and switching nodes waveforms with $100kHz$ sinusoidal reference (V_{ref}) at $V_{in} = 3.3V$

from 2V to 4V with a fixed input voltage (V_{in}) of 3.3V. Fig. 4.13(a) is the case when V_{out} changes from 2V to 4V and Fig. 4.13 (b) is when V_{out} changes from 4V to 2V. It is observed that the mode change between buck and boost mode happens smoothly and there is no overlap between the LXA and LXB nodes during the mode change period. Fig. 4.14 shows the $100kHz$ sinusoidal reference signal (V_{ref}), V_{out} and the switching nodes (LXA, LXB) at $V_{in} = 3.3V$. As shown in this figure, the output voltage follows the fast $100kHz$ sinusoidal reference signal well. This figure shows that the converter with DECPM responds well to the high frequency reference signal.

Chapter 5

Power Stage Optimization of the 4SBBC for the Polar Modulation Application

In this chapter, the loss mechanisms of the 4SBBC and its power stage optimization for polar modulation will be discussed. During this chapter, it is assumed that the 4SBBC converter is used as a dynamic power supply for the polar modulation application. In this application, the load for the 4SBBC is a power amplifier which is generally modeled as a constant resistor. Fig.5.1 is a diagram for the 4SBBC power stage. This chapter starts with the power loss mechanisms of the 4SBBC. The 4SBBC is designed to operate in either buck or boost mode which allows only 2 switches are working during a single switching period. Therefore, the loss mechanisms for each mode are broken down and analyzed in detail. After this, the polar modulation scheme and the EDGE signal which is used as a reference signal for the 4SBBC in this application is briefly introduced. In contrast to the conventional DC-DC converter application, in the polar modulation

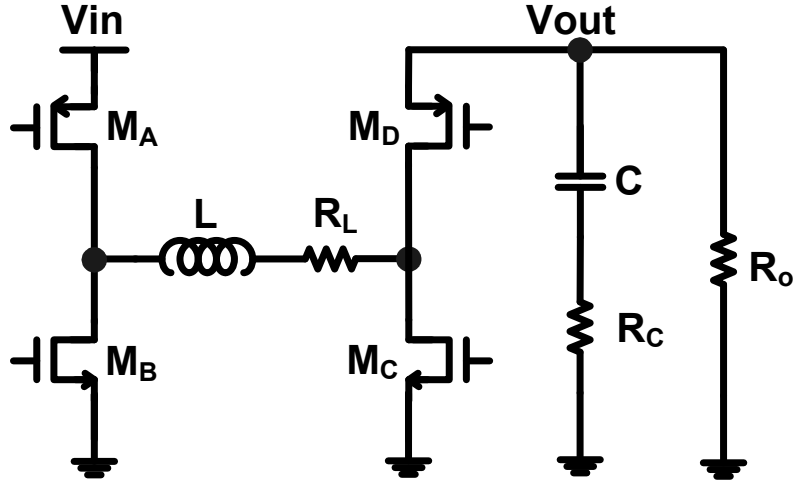


Figure 5.1: 4SBBC power stage diagram

application, the time-varying signal is used as a reference signal to change the output voltage, and the average efficiency is introduced and used for power stage optimization. Finally, the size of the 4 switches are determined and optimized based on the average efficiency for the polar modulation application.

5.1 Loss Breakdown of the 4SBBC

The power losses of the 4SBBC to be considered in this sections are the conduction loss, dynamic loss and controller loss. The conduction loss (power stage loss) includes R_{dson} loss, inductor ESR loss, capacitor ESR loss and these losses are all related to the resistive power loss. Gate charge loss is the only Dynamic loss to considered here. Controller loss is a power consumption of the controller and is a multiple of V_{in} and quiescent current (I_q) to the controller.

From the Fig.5.1, M_A and M_D are PMOS power switches and M_B and M_C are NMOS

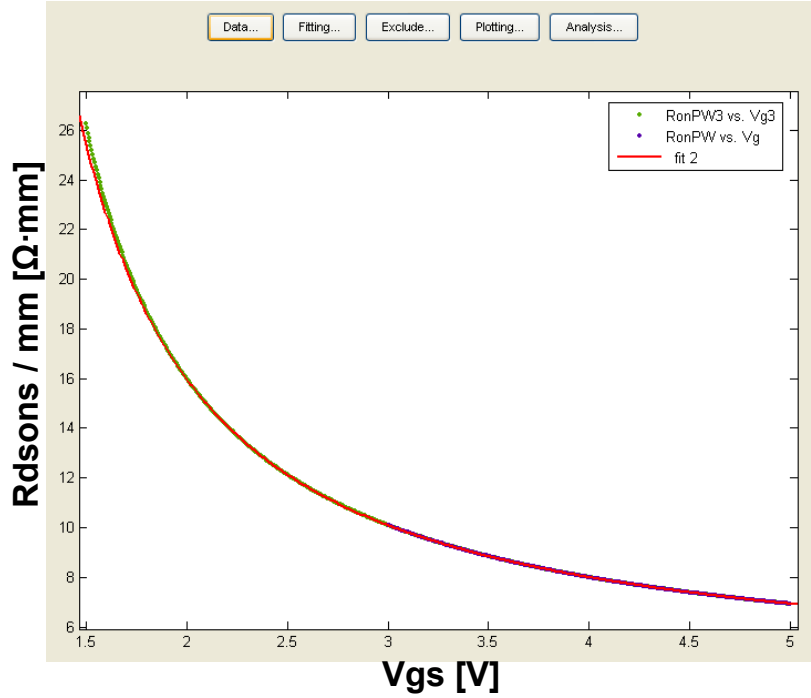


Figure 5.2: Curve fitting result for PMOS R_{dson}

power switches. L and C are the power filter inductor and capacitor respectively. R_L and R_C are the parasitic series resistances for L and C respectively. R stands for the equivalent output load resistance. Because the input voltage (V_{in}) and output voltage (V_{out}) of the 4SBBC are not constant, the effective gate to source voltages ($|V_{gs}|$) for M_A and M_D are also not constant. Therefore, the R_{dson} s of M_A and M_D are function of input and output voltage (V_{in} and V_{out}), respectively and these relationship between voltage and R_{dson} are carefully determined. In this dissertation, the curve fitting method is used to extract the relationship from the CADENCE simulation.

Fig.5.2 is the curve fitting result of PMOS R_{dson} with respect to the effective gate to source voltages ($|V_{gs}|$). For this curve fitting, the level 2 model of the MOSFET is used.

From the result of Fig.5.2, the resultant R_{dson} per $1mm$ width for PMOS is

$$R_{dsonP}(|V_{GS}|) = \frac{1 + 0.4373(|V_{GS}| - 0.6031)^{1.296}}{0.06379(|V_{GS}| - 0.6031)^{1.485}} [\Omega \cdot mm] \quad (5.1)$$

Because PMOS is used for M_D switch, it is necessary to analyze buck mode with two different cases. One is a ‘body-diode conduction mode’ of M_D switch and the other is a ‘synchronous mode’ of M_D switch. When V_{out} is less than the threshold voltage ($|V_{thp}|$) of M_D , M_D cannot be turned on even with the gate voltage of zero. Therefore, the output current can only flow through body diode of M_D switch. This is called a ‘body-diode conduction mode’ of M_D switch in this dissertation. But, when V_{out} is larger than the threshold voltage of the M_D , the output current can flow through the M_D switch and the voltage drop of the M_D switch is related to the (5.1). This is called a ‘synchronous mode’ of M_D switch in this dissertation.

The body diode voltage drop is curve-fitted and its result is shown in (5.2).

$$V_{diode}(V_o, W) = \frac{1}{31.65} \cdot \ln \left(\frac{V_{out}}{R_o \times (514.1 \times 10^{-15} \times W)} + 1 \right) \quad (5.2)$$

Fig. 5.3 is a simple schematic to show the voltage drop of the M_D switch in either the ‘body-diode conduction mode’ or ‘synchronous mode’. By using (5.1) and (5.2), the conduction mode of the M_D switch can be separated and shown in Fig. 5.4. Fig. 5.4 shows the body diode voltage drop (V_{diode}) and R_{dson} voltage drop (V_{DS}) across the M_D with respect to the output voltage (V_{out}). For the following analysis, the lower voltage drops across M_D switch between the body diode voltage drop (V_{diode}) and R_{dson} voltage drop (V_{DS}) is chosen for the voltage drop of the M_D switch.

Based on the previous analysis, the duty cycle can be determined like a (5.3). The

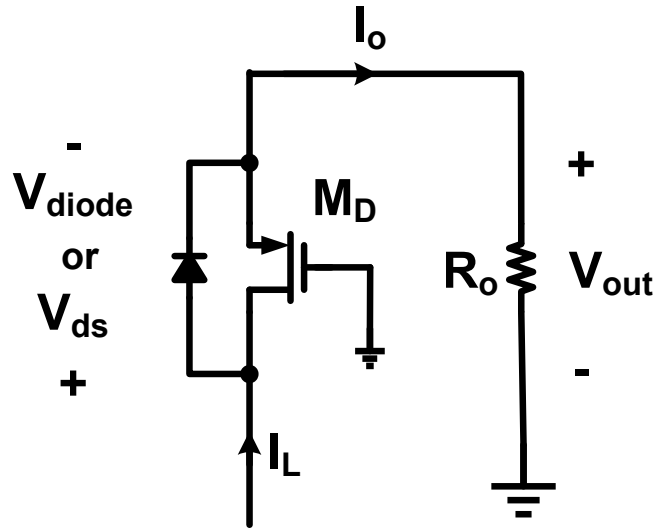


Figure 5.3: Voltage drop model for M_D

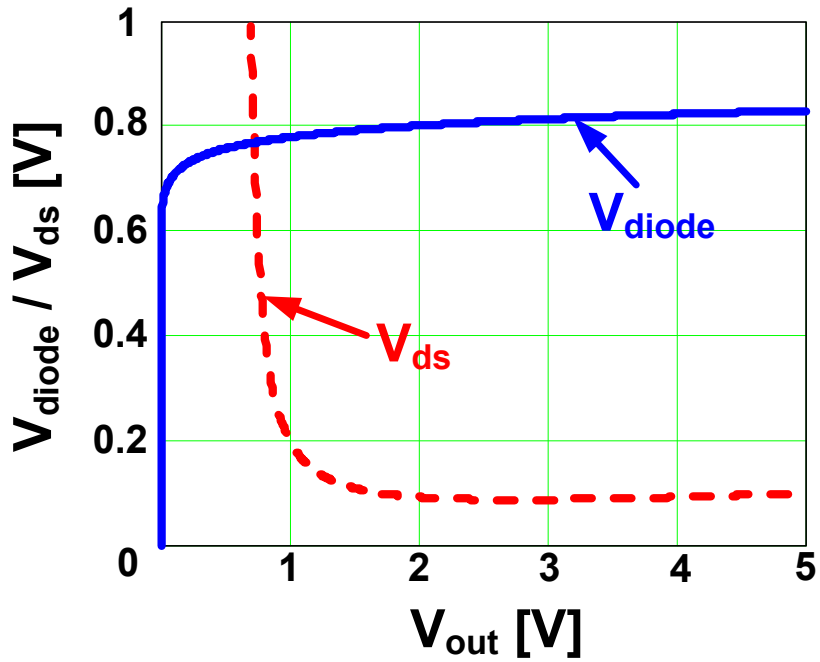


Figure 5.4: Diode voltage (V_{diode}) and Rdson voltage drop (V_{DS}) across the M_D switch

3 different modes described above are included in this (5.3). The first equation of the (5.3) is the buck operation with the ‘body-diode conduction mode’ of M_D switch, and the second is the buck operation with the ‘synchronous mode’ of M_D switch, and the last equation is the boost operation mode . This (5.3) also include the voltage drop of the switches and the series resistance of the inductor to estimate accurate duty information.

$$D = \begin{cases} \frac{\frac{V_{out}}{V_{in}} \left(1 + \frac{R_B}{R_o} + \frac{R_L}{R_o} + \frac{V_{out} + V_{diode}}{R_o} \right)}{1 - \frac{R_A}{R_o} \frac{V_{out}}{V_{in}} + \frac{R_B}{R_o} \frac{V_{out}}{V_{in}}} & \text{if BUCK } \wedge (V_{ds}@M_D > V_{diode}) \\ \frac{\frac{V_{out}}{V_{in}} \left(1 + \frac{R_B}{R_o} + \frac{R_L + R_D}{R_o} \right)}{1 - \frac{R_A}{R_o} \frac{V_{out}}{V_{in}} + \frac{R_B}{R_o} \frac{V_{out}}{V_{in}}} & \text{if BUCK } \wedge (V_{ds}@M_D < V_{diode}) \\ 0.5 \cdot \left(2 + \frac{R_D}{R_o} - \frac{R_C}{R_o} - \frac{V_{out}}{V_{in}} \right) \\ - \sqrt{\left(2 + \frac{R_D}{R_o} - \frac{R_C}{R_o} - \frac{V_{out}}{V_{in}} \right)^2 - 4 \left(1 + \frac{R_D}{R_o} + \frac{R_L + R_A}{R_o} - \frac{V_{out}}{V_{in}} \right)} & \text{if BOOST} \end{cases} \quad (5.3)$$

Fig. 5.5 shows the difference of the (5.3) and the ideal duty which ignores the voltage drop of the parasitic resistance and diode voltage drop of the M_D switch with respect to the output voltage (V_{out}). As the output voltage (V_{out}) increases, the difference of the duty of these two cases increases as well. Here, the R_A , R_B , R_C and R_D are the R_{dson} of the switch M_A , M_B , M_C and M_D of the Fig. 5.1 respectively. And R_L is the parasitic series resistance of the inductor (L) and R_o is the output load resistance of the Fig. 5.1. For the Fig. 5.5, $V_{in} = 3.3V$, $W_A = W_D = 69.12mm$, $W_B = W_C = \frac{1}{3}W_A$, $R_o = 5\Omega$, $R_L = 0.1\Omega$ are used.

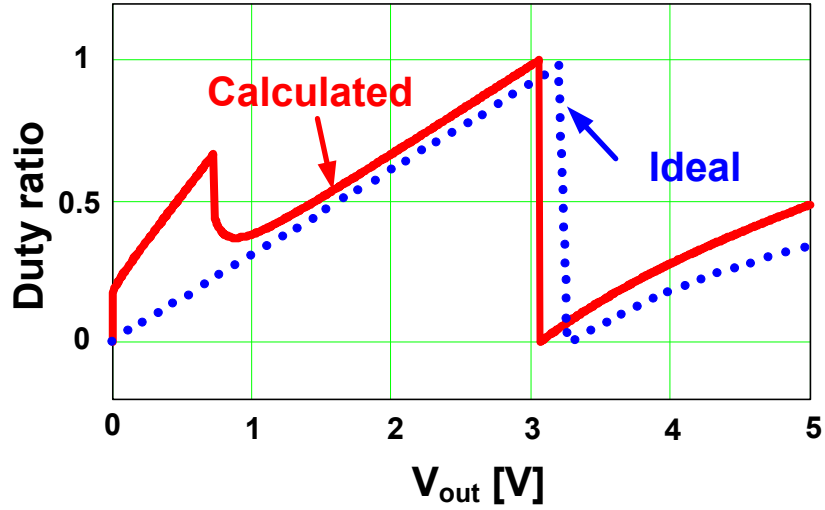


Figure 5.5: Duty ratio comparison between Eq.(5.3) and ideal case

$$I_L = \begin{cases} I_{out} = \frac{V_{out}}{R_o} & \text{if BUCK} \\ \frac{I_{out}}{(1-D)} = \frac{V_{out}}{(1-D) \cdot R_o} & \text{if BOOST} \end{cases} \quad (5.4)$$

(5.4) is the equation to calculate the DC inductor current (I_L) from the load (output) current (I_o) which is the function of output voltage (V_o) and load resistance (R_o).

$$\Delta i_L = \begin{cases} \frac{(1-D) \cdot V_o}{L \cdot f_{sw}} & \text{if BUCK} \\ \frac{D \cdot V_{in}}{L \cdot f_{sw}} & \text{if BOOST} \end{cases} \quad (5.5)$$

(5.5) is the equation to calculate the peak-to-peak inductor current ripple (Δi_L).

$$P_{loss} |_{R_{dson}} = \begin{cases} \frac{R_{dsonP}(V_{in})}{W_A} \cdot \left(I_L^2 + \frac{\Delta i_L^2}{12} \right) \cdot D \\ + \frac{R_{dsonN}}{W_B} \cdot \left(I_L^2 + \frac{\Delta i_L^2}{12} \right) \cdot (1 - D) + I_L \cdot V_{diode}(W_D, V_o) \\ \text{if BUCK} \wedge (V_{ds}@M_D > V_{diode}) \\ \\ \frac{R_{dsonP}(V_{in})}{W_A} \cdot \left(I_L^2 + \frac{\Delta i_L^2}{12} \right) \cdot D \\ + \frac{R_{dsonN}}{W_B} \cdot \left(I_L^2 + \frac{\Delta i_L^2}{12} \right) \cdot (1 - D) + \frac{R_{dsonP}(V_o)}{W_D} \cdot \left(I_L^2 + \frac{\Delta i_L^2}{12} \right) \\ \text{if BUCK} \wedge (V_{ds}@M_D < V_{diode}) \\ \\ \frac{R_{dsonN}}{W_C} \cdot \left(I_L^2 + \frac{\Delta i_L^2}{12} \right) \cdot D \\ + \frac{R_{dsonP}(V_o)}{W_D} \cdot \left(I_L^2 + \frac{\Delta i_L^2}{12} \right) \cdot (1 - D) + \frac{R_{dsonP}(V_{in})}{W_A} \cdot \left(I_L^2 + \frac{\Delta i_L^2}{12} \right) \\ \text{if BOOST} \end{cases} \quad (5.6)$$

(5.6) is the analytic equation to calculate the R_{dson} losses of the 4SBBC in each operation modes. The Δi_L is a peak to peak inductor current ripple and (5.6) is derived from the RMS loss which include the inductor current ripple loss [34]. Here, R_{dsonP} is the R_{dson} of the PMOS and R_{dsonN} is the R_{dson} of the NMOS. V_{diode} is the voltage drop of the M_D switch in the ‘body-diode conduction mode’. And W_A , W_B , W_C and W_D are the width of the power transistors of M_A , M_B , M_C and M_D , respectively.

$$P_{loss} |_{R_L} = R_L \cdot \left(I_L^2 + \frac{\Delta i_L^2}{12} \right) \quad (5.7)$$

(5.7) is the equation to calculate the R_L losses of the 4SBBC, which is the parasitic series

resistance of the inductor (L).

$$P_{loss|RC} = \begin{cases} R_C \cdot \frac{\Delta i_L^2}{12} & \text{if BUCK} \\ R_C \cdot I_{out}^2 \cdot D + R_C \cdot \left\{ (I_L - I_{out})^2 + \frac{\Delta i_L^2}{12} \right\} \cdot (1 - D) & \text{if BOOST} \end{cases} \quad (5.8)$$

(5.8) is the equation to calculate the R_C losses of the 4SBBC, which is the parasitic series resistance of the capacitor (C) for both buck and boost mode operations.

$$P_{loss|gate} = \begin{cases} f_{sw} \cdot C_{iss} \cdot (W_A + W_B) \cdot V_{in}^2 & \text{if BUCK} \\ f_{sw} \cdot C_{iss} \cdot (W_C + W_D) \cdot V_{in}^2 & \text{if BOOST} \end{cases} \quad (5.9)$$

(5.9) is the equation to calculate the gate charge loss which is consumed during the turn-on and turn-off the power switches. This loss emulates the gate driver losses but only contains the the last stage of the driver loss. For this equation, the C_{iss} is the equivalent input capacitor of the power switches during turn-on and turn-off. This C_{iss} is the process dependent parameter, and is extracted from the CADENCE simulation. Fig. 5.6 is the simulation test bench to extract the C_{iss} . Here, I_{gate} is the current source to be applied to gate node of the power switch and I_{load} is emulating the inductor current. From this test bench, the C_{iss} can be simulated and calculated with the equation of (5.10). Under this, the C_{iss} for both PMOS and NMOS is $2.36pF/mm$.

$$C_{iss} = AVG \left\{ \frac{I_{gate}}{dV_{gs}/dt} \right\}_0^{V_{driver}} \quad (5.10)$$

(5.11) shows the controller loss which is a multiple of the input voltage (V_{in}) and the quiescent current (I_q) to the controller.

$$P_{loss|controller} = V_{in} \cdot I_q \quad (5.11)$$

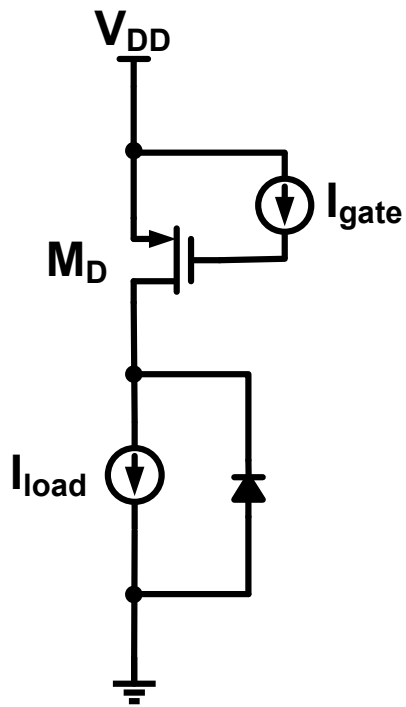


Figure 5.6: test bench for C_{iss}

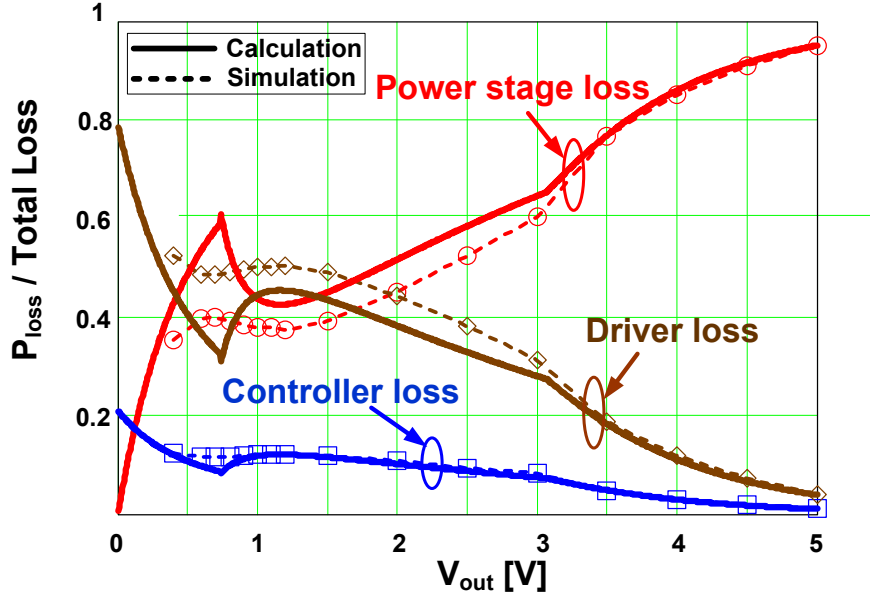


Figure 5.7: Power loss breakdown @ $V_{in} = 3.3V$

Fig. 5.7 shows the loss ratio breakdown of the 4SBBC with respect to the output voltage (V_{out}), and it shows the comparison between the calculation and the simulation results. The power stage loss is the sum of the R_{dson} loss ((5.6)), R_L loss ((5.7)), and R_C loss ((5.8)). The driver loss stands for the gate charge loss which is shown in (5.9), and the controller loss is from the (5.11). The loss ratio is the ratio of the each losses to the total loss.

Fig. 5.8 shows the efficiency vs. output voltage (V_{out}) with different sizes of transistors M_A and M_D in Fig. 5.1. For this figure, the sizes of the transistors M_B and M_C set to be $23mm$. It is easily expected that, bigger size of M_A makes more gate losses but less R_{dson} loss during the buck operation, and bigger size of M_D makes more gate losses but less R_{dson} loss at boost operation. Large size of the M_D helps to have high efficiency at buck mode due to the small R_{dson} loss of M_D but degrades the efficiency at boost mode due to the increased gate loss of M_D . In similar way, large size of the M_A helps to

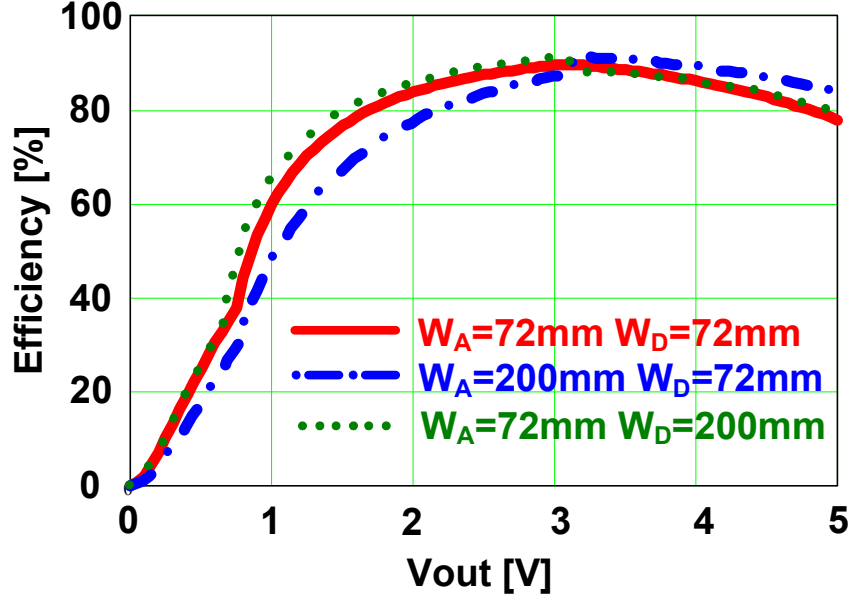


Figure 5.8: Efficiency vs. V_{out} with different W_A and W_D when $W_B = W_C = 23mm$

have high efficiency at boost mode due to the small R_{dson} loss of M_A but degrades the efficiency at buck mode due to the increased gate loss of M_A . This is shown clearly in Fig. 5.8.

Fig. 5.9 shows the comparison of the efficiency between the CADENCE simulation and the calculation based on above analysis. The input voltage (V_{in}) is 3.3V and the load resistor (R_o) is 5Ω. As shown in this figure, the loss analysis derived above was well match with the simulation results.

Fig. 5.10 shows the comparison of the efficiency between the measurement data of 4SBBC and the calculation. The input voltage (V_{in}) is 3.3V and the load resistor (R_o) is 10Ω. This figure shows that the loss analysis match well with the measurement data at buck mode but not at boost mode. It is because during the boost mode, the measured R_{dson} value is higher than the desired value due to the weak driving voltages to the boost switches (M_C, M_D).

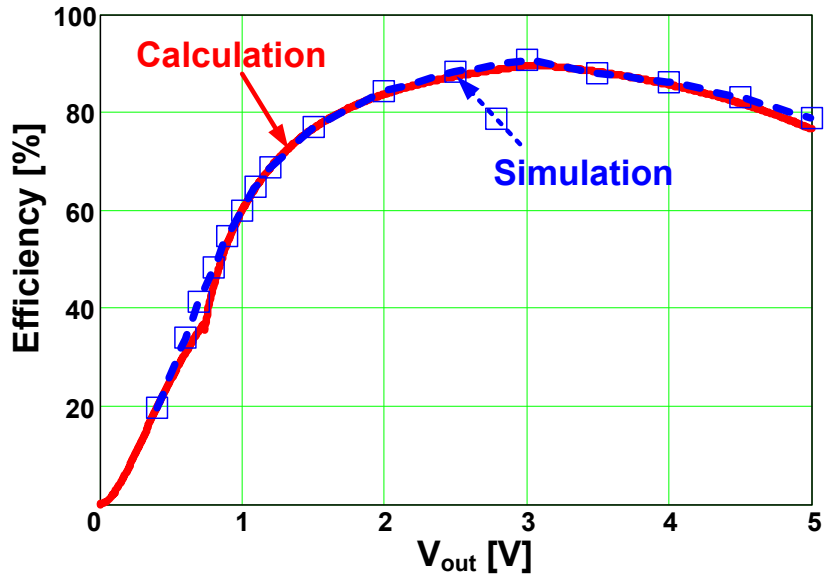


Figure 5.9: Efficiency comparison between calculation and simulation @ $V_{in} = 3.3V$

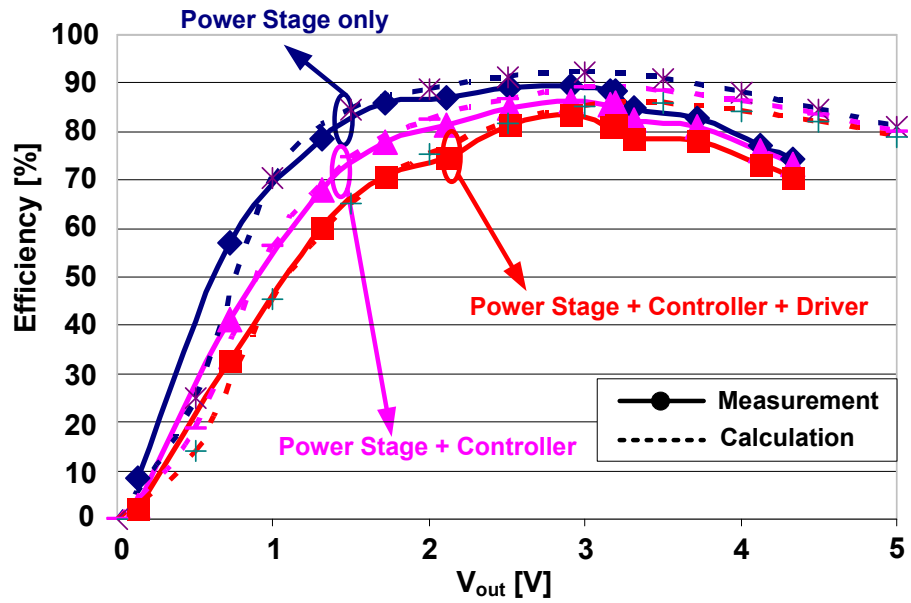


Figure 5.10: Efficiency comparison between calculation and measurement @ $V_{in} = 3.3V$

5.2 Polar modulation and EDGE standard

High efficiency RF power amplifiers (RF PAs) are critical in portable battery-operated wireless communication system because they dominate the power consumption of the system. Especially, EDGE system uses the envelope varying signal to increase its data rate. This envelope variation requires the linear or linearized RF power amplifier. However, linear power amplifiers, such as class A, class B or class AB have a drawback of low efficiency which degrades battery run time [5].

One popular architectural solution to transmit envelope varying signal with high efficiency is the polar modulation which is shown in Fig. 5.11 [5, 7, 9, 10, 52]. Polar modulation uses two signal paths; one is envelope path, $A(t)$, and another is phase path, $\phi(t)$. This phase path contains no envelope variation, so high efficient nonlinear power amplifier such as Class E can be used to transmit phase information. Then the envelope variation is restored by modulating the supply voltage of power amplifier through the envelope path.

The block diagram of typical polar modulation is shown in Fig. 5.11. In this figure, the envelope modulator is implemented with 4SBBC. The essence of polar modulation is separating the envelope signal, $A(t)$ and phase signal, $\phi(t)$ from transmitting information. In polar modulation, the power amplifier is only processing phase modulated signal which has a constant envelope. This means the power amplifier do not need linear amplification. So a switched mode power amplifier such as class E can be used in this system whose power consumption is theoretically zero[5, 53]. The time varying envelope signal is recombined at power amplifier by modulating supply voltage through the envelope modulator. Now the linearity of the transmitter depends on the linearity of the envelope modulator. Any conventional power supply like linear regulator or switched

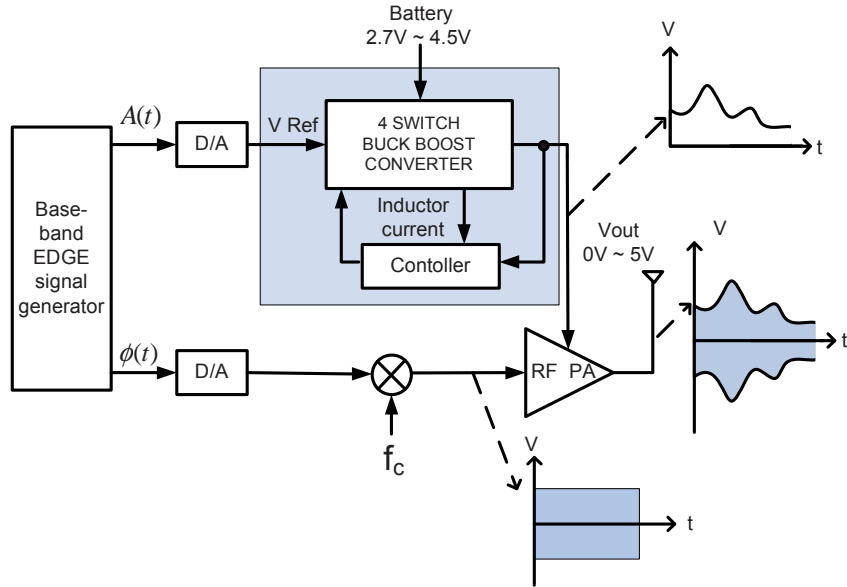


Figure 5.11: Block diagram of polar modulation with buck boost converter as an envelope modulator

mode power supply can be used as an envelope modulator, even if the response of the power supply from V_{ref} to V_{out} has a linear relationship, and the closed loop gain is wide enough to envelope signal bandwidth. Even to the envelope modulator, switched mode power supply has theoretically 100% power efficiency. So with polar modulation architecture, both high efficiency and high linearity can be achieved if we have a good enough envelope modulator.

In order to design the envelope modulator properly in polar modulation architecture, the understanding of the signal which will be used in this system is necessary. In this chapter, EDGE standard is used as a transmitting signal.

An EDGE standard is the evolution of the current GSM standard to provide higher bit rates of 812.5 kbps by using $3\pi/8$ offset 8-PSK as opposed to GSM bit rates of 270.8 kbps, which use GMSK modulation. The symbol rate of EDGE is equal to the bit rate of GSM because in EDGE mode, each symbol represents 3 bits [54, 9]. Fig. 5.12 shows the EDGE

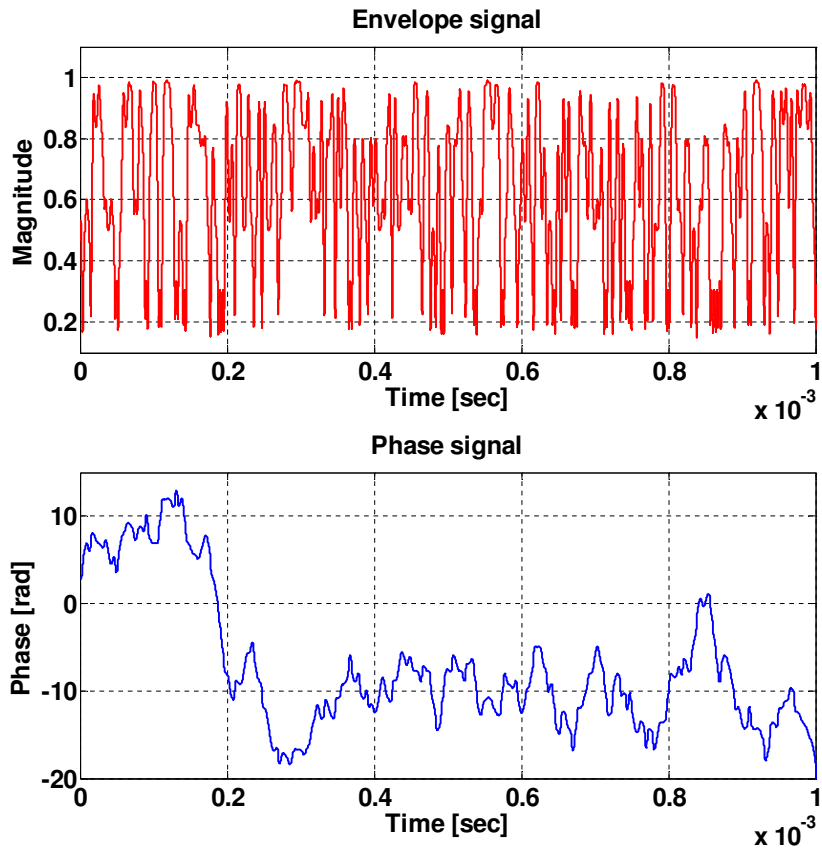


Figure 5.12: EDGE signal in time domain (provided by RFMD)

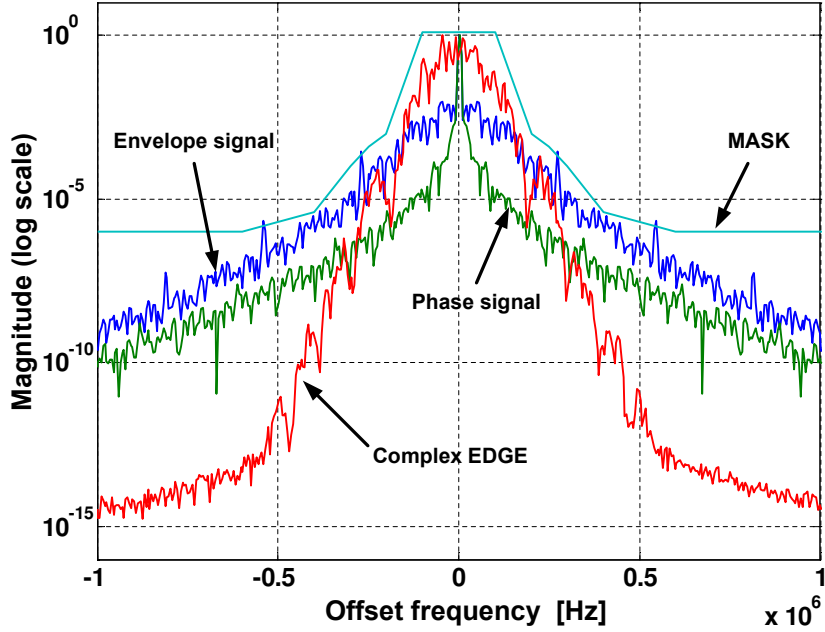


Figure 5.13: EDGE signal in frequency domain

signal in time domain. Fig. 5.12(a) is the envelope signal waveform $A(t)$ and Fig. 5.12(b) is the phase signal waveform $\phi(t)$ in time domain respectively. The envelope variation in EDGE system is 17dB peak to minimum ratio, and this corresponds to voltage variation of 0.706V to 5V. This means the proposed envelope modulator must have wide output voltage range, regardless of input voltage variation.

Another feature of the EDGE signal can be revealed by its frequency domain information. Fig. 5.13 shows the the envelope and phase components of EDGE signal with composite complex EDGE signal and transmit mask together. As shown in Fig. 5.13, the composite complex EDGE signal has most energy within 200KHz offset from center frequency. However, envelope and phase signal has wider spectrum than composite complex EDGE signal spectrum. Several papers discussed this issue and proposed different bandwidths for envelope and phase path which are around 1–2 MHz. [9], [52].

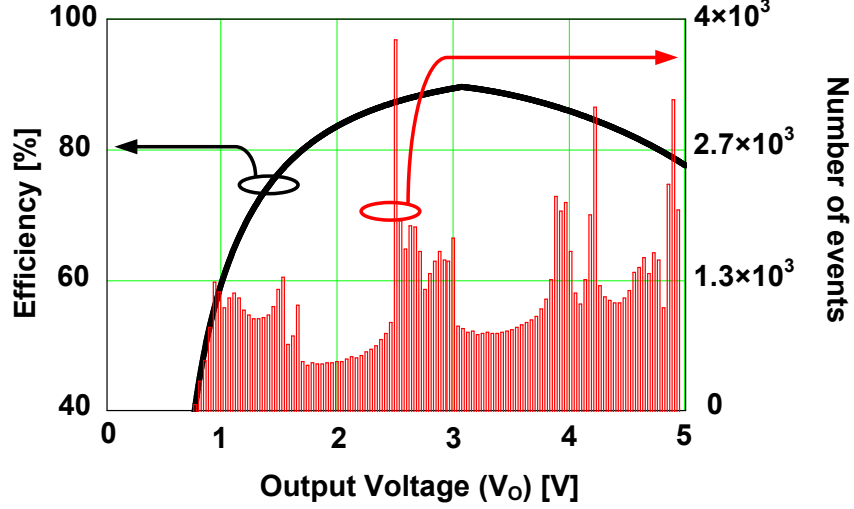


Figure 5.14: Efficiency and the histogram of the EDGE envelope signal @ $V_{in} = 3.3V$

5.3 Average Efficiency and power stage optimization of 4SBBC with EDGE envelope signal

Fig. 5.14 shows the efficiency of the 4SBBC and the histogram of the EDGE envelope signal with respect to the output voltage. For the efficiency, the size of the power transistors are $W_A = W_C = 69.12mm$ and $W_B = W_D = 1/3W_A$, and the switching frequency is $10MHz$ and input voltage is $3.3V$. As shown in Fig. 5.14, the output voltage range is from $0V$ to $5V$. For the histogram, this is redrawn from the $1.5msec$ long EGDE envelope signal. This histogram shows the relative voltage distribution of the EDGE envelope signal which is normalized to maximum $5V$. As shown in this figure, maximum efficiency of the 4SBBC is obtained the transition point of the buck and boot mode which is around $3.3V$.

Fig. 5.15 is the time domain waveforms of the EDGE envelope signal ($V_{out}(t)$) and its corresponding instantaneous efficiency ($\eta(V_{out}(t))$) which is calculated from the diagram

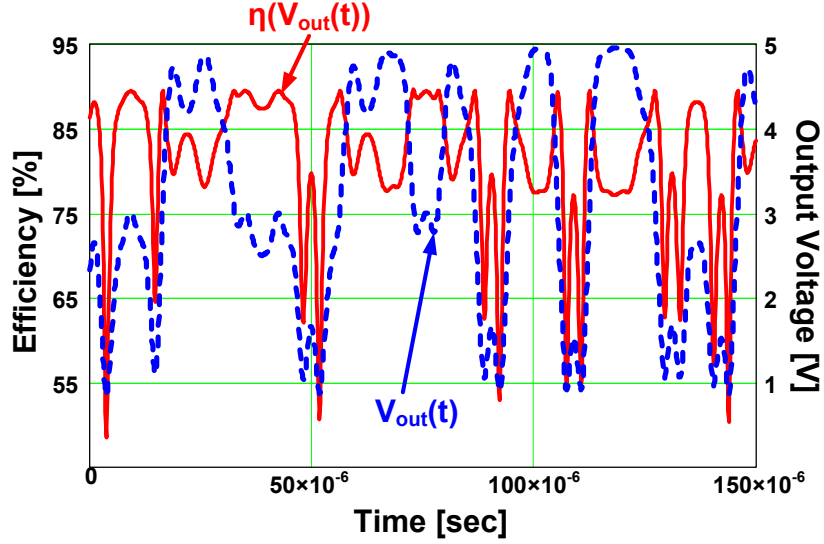


Figure 5.15: output voltage and the corresponding instantaneous efficiency in time domain @ $V_{in} = 3.3V$

shown in Fig. 5.14. As consistent with the Fig. 5.14, the maximum efficiency is shown when the $V_{out}(t)$ is around 3.3V.

By using the above two figures (Fig. 5.14 and Fig. 5.15), the following equation (5.12) can be derived for average efficiency of the 4SBBC with a EDGE envelope signal as a reference. The σ is the time range of the reference signal which is the EDGE envelope signal and is 1.5msec long for here. This equation is deduced from the similarity of the efficiency measurement. At the measurement, the efficiency can be measured from the ratio of the measured output power and the measured input power. As with the measurement described above, the numerator in the integral of (5.12) stands for the output power and the denominator in the integral is the input power of the system. Therefore, the average efficiency of the system in (5.12) is the ratio of the integral of the output power and input power for long enough period. Here, long enough period means all possible output voltage values should be included during the period.

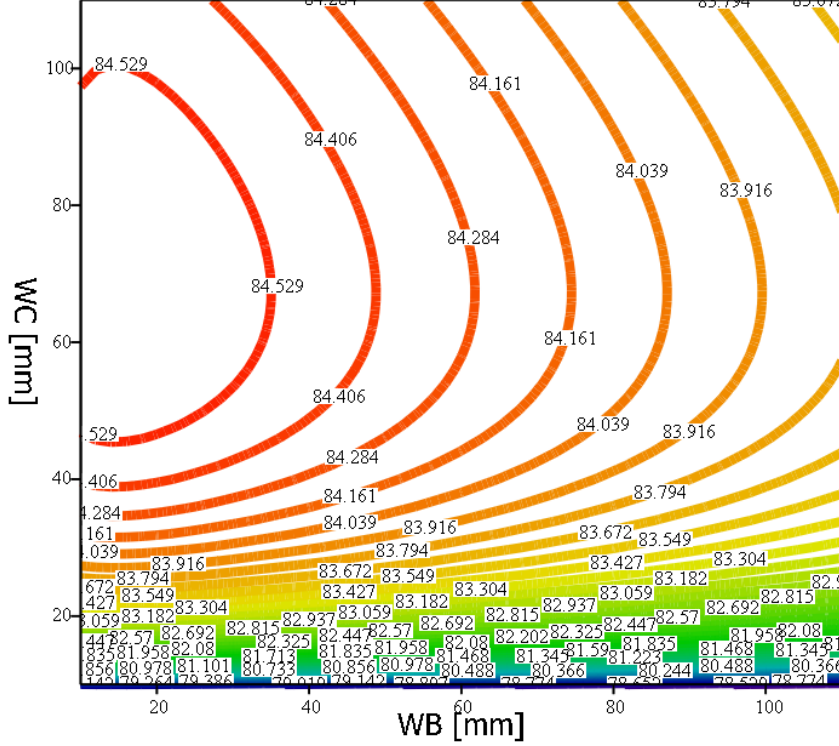


Figure 5.16: Average efficiency with respect to W_B and W_C when $W_A = W_D = 69mm$

$$\eta_{average} = \frac{\int_0^\sigma V_{out}^2(t) dt}{\int_0^\sigma \{V_{out}^2(t)/\eta(V_{out}(t))\} dt} \quad (5.12)$$

As a comparison, with the sizes of the power transistors of $W_A = W_C = 69.12mm$ and $W_B = W_D = 1/3W_A$, and the switching frequency of $10MHz$ and input voltage of $3.3V$ and load resistor of 5Ω , the calculated average efficiency from (5.12) is 83.3% and cadence simulation result shows 82% . This verify that the average efficiency calculation proposed in (5.12) expects quite accurate number.

(5.12) can be used to determine the size of the power transistors of the 4SBCC for high efficiency with EDGE signal. Fig. 5.16 is the average efficiency of the 4SBBC with an EDGE envelope signal as a reference at the function of W_B and W_C which are the

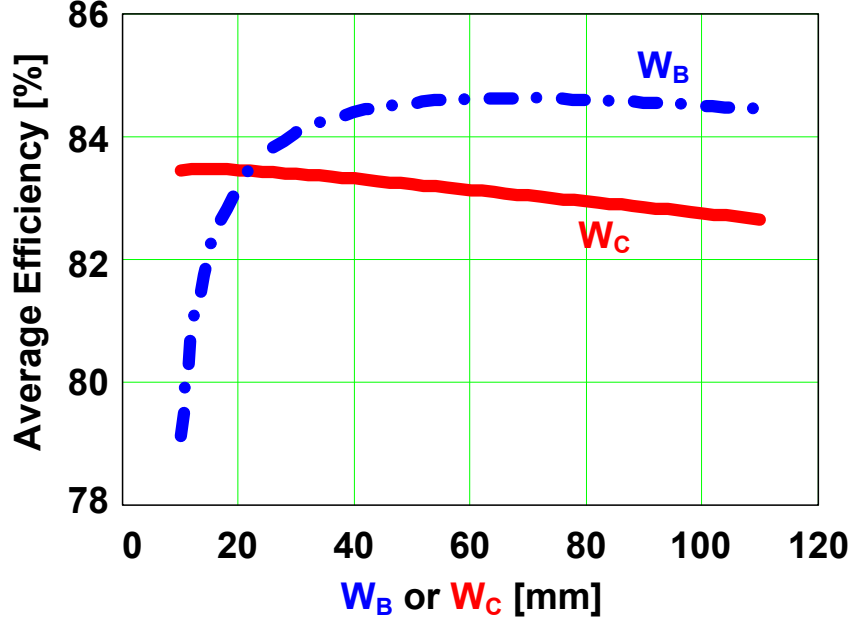


Figure 5.17: Average efficiency with respect to W_B and W_C when $W_C = 24mm$, $W_A = W_D = 69mm$ and $W_B = 24mm$, $W_A = W_D = 69mm$, respectively

widths of the power transistor M_B and M_C in Fig. 5.1 respectively. For this, W_A and W_D set to $69mm$. Fig. 5.17 comes from Fig. 5.16. The average efficiency curve of W_B is drawn at the condition of $W_C = 24mm$, $W_A = W_D = 69mm$, and that of W_C is drawn at the condition of $W_B = 24mm$, $W_A = W_D = 69mm$. From these Fig. 5.16 and Fig. 5.17, it is observed that there exist optimum values of each transistor width to achieve the maximum efficiency. As shown in Fig. 5.16, when $W_A = W_D = 69mm$, $W_B \approx 10mm$ and $W_C \approx 70mm$ give the maximum average efficiency

Fig. 5.18 and Fig. 5.19 show the average efficiencies of the 4SBBC with a EDGE envelope signal as a reference at the function of W_A and W_D which are the widths of the power transistor M_A and M_D in Fig. 5.1. For this, W_B and W_C set to $23mm$. Especially, for the Fig. 5.19, the average efficiency curve of W_A in is drawn at the condition of $W_D = 72mm$, $W_B = W_C = 69mm$, and that of W_D is drawn at the condition

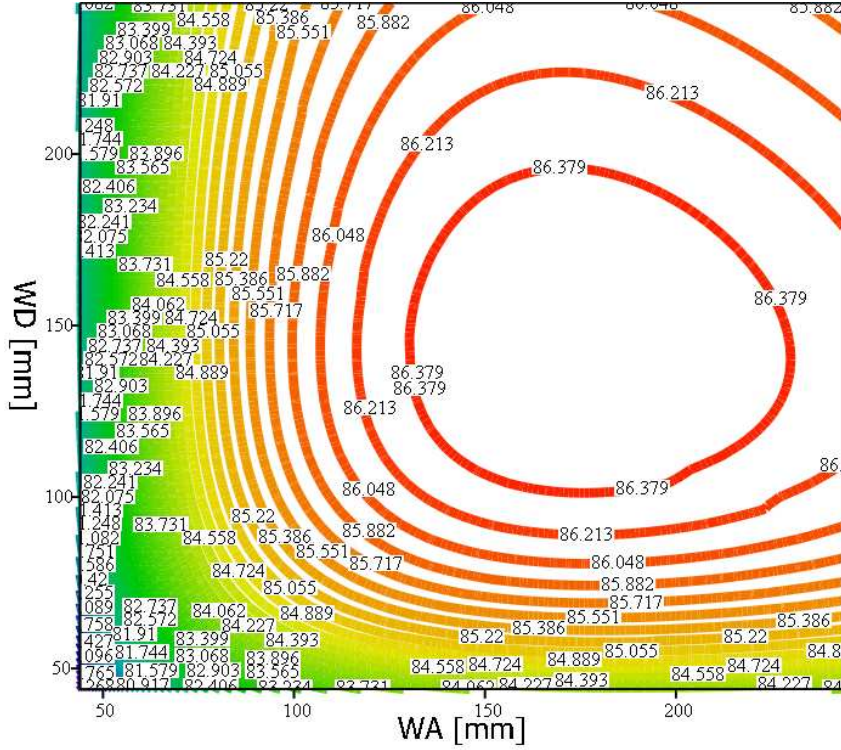


Figure 5.18: Average efficiency with respect to W_A and W_D when $W_B = W_C = 23mm$

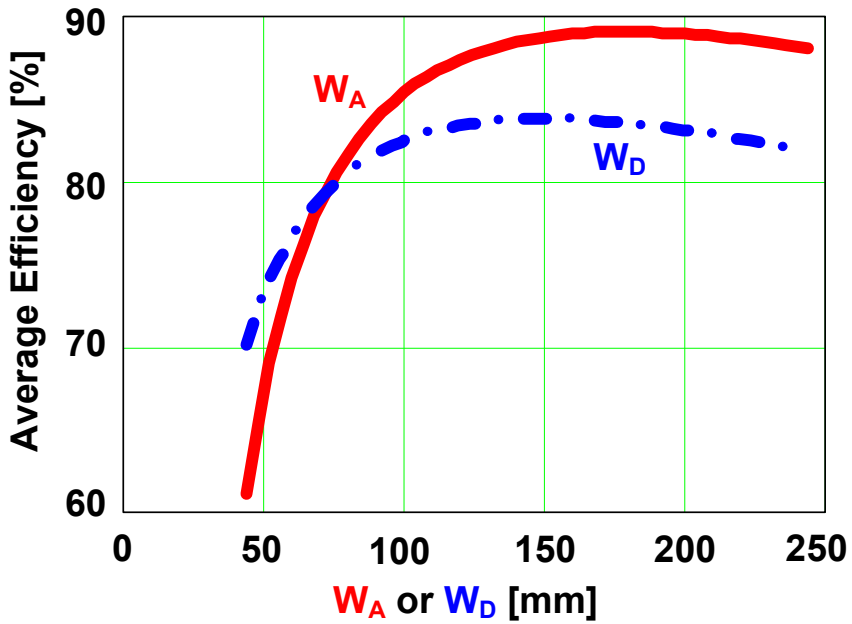


Figure 5.19: Average efficiency with respect to W_A and W_D when $W_C = 72mm$, $W_B = W_C = 23mm$ and $W_A = 72mm$, $W_B = W_C = 23mm$, respectively

of $W_A = 72mm, W_B = W_C = 23mm$. From these Fig. 5.18 and Fig. 5.19, it is also observed that there exist optimum values of each transistor width to achieve the maximum efficiency. As shown in Fig. 5.18, when $W_B = W_C = 23mm$, $W_A \approx 170mm$ and $W_C \approx 150mm$ give the maximum average efficiency.

When the high efficiency is the only parameter, it is possible to choose any numbers of the sizes to each power transistors, but there is one things to consider to decide the transistor sizes for the 4SBBC. Let's look at the Fig. 5.8 again. This figure shows that the efficiency graph with different W_A and W_D . As shown this figure, when W_A and W_D have different values, the efficiency graph shows the abrupt change at the transition point between buck and boost modes. It is deduced that when W_A and W_D has different value and W_B and W_C are different, its resultant R_{dson} s change. This results that the transfer functions between these modes also abruptly change, and the smooth mode transition fails. Therefore, the sizes of W_A and W_D and that of W_B and W_C keep same respectively to achieve the smooth mode transition for 4SBBC.

Following from Fig. 5.20 to Fig. 5.23 show the average efficiency graphs with the condition of $W_A = W_D$ and $W_B = W_C$ as mentioned just above. Fig. 5.20 is at the condition of and $W_B(= W_C) = W_A(= W_D)/3$, Fig. 5.21 is at the condition of $W_B(= W_C) = W_A(= W_D)/2$, Fig. 5.22 is at the condition of and $W_B(= W_C) = W_A(= W_D)$, and Fig. 5.23 is at the condition of and $W_B(= W_C) = W_A(= W_D) \times 2$.

For each diagram, there exists the optimum sizes of the transistors, but Fig. 5.20 shows the highest average efficiency at the optimum sizes of the transistors. And also Fig. 5.20 shows that the average efficiency is less sensitive to the sizes of the transistors. In real chip implementation, the die size of the converter is another factor to consider. Therefore, the optimum sizes of the transistor need to be determined both by the efficiency and size of the total converter.

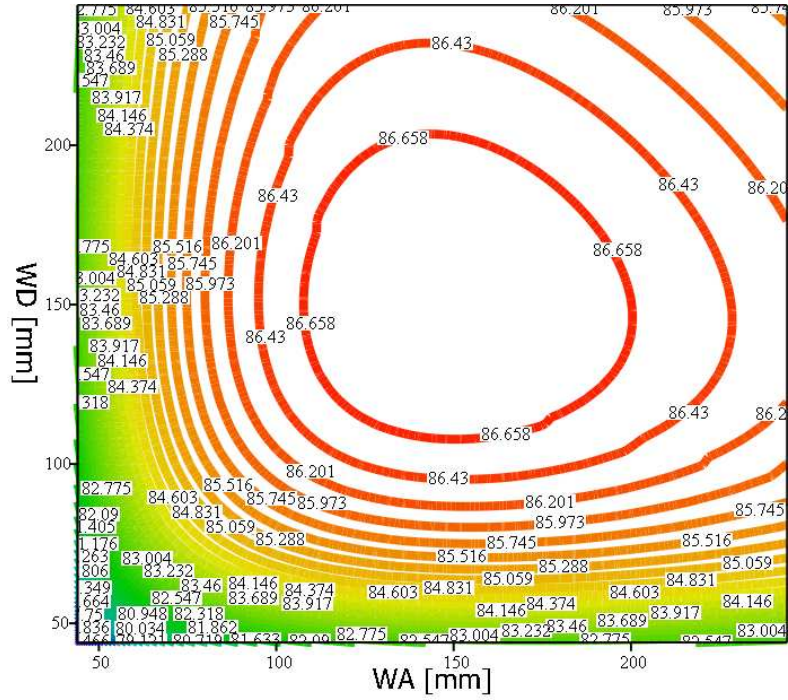


Figure 5.20: Average efficiency with respect to W_A and W_D with $W_B = \frac{W_A}{3}$, $W_C = \frac{W_D}{3}$

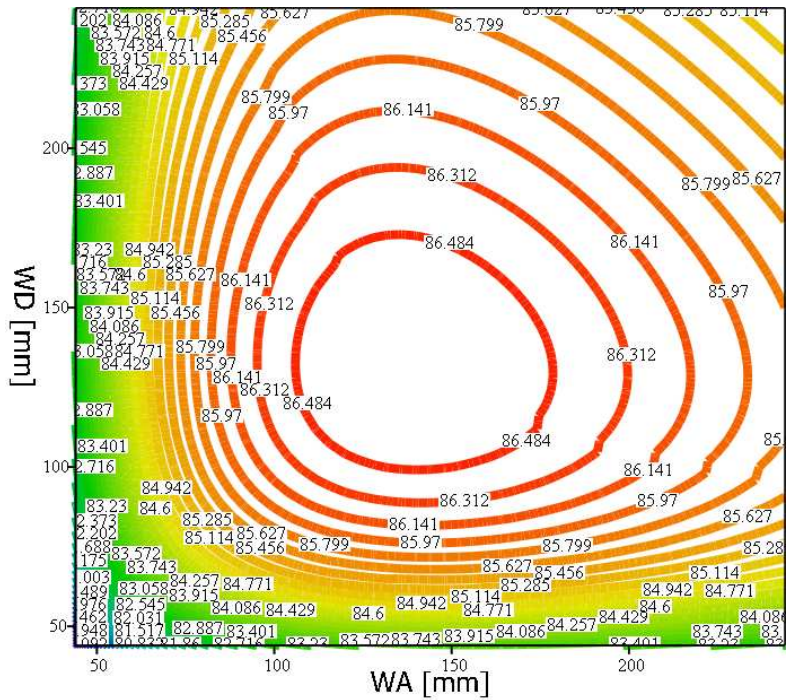


Figure 5.21: Average efficiency with respect to W_A and W_D with $W_B = \frac{W_A}{2}$, $W_C = \frac{W_D}{2}$

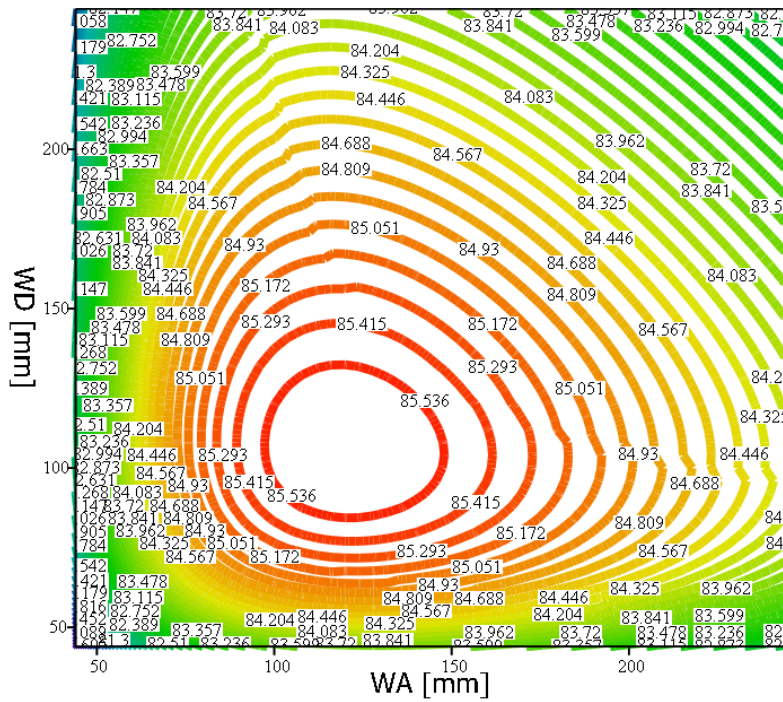


Figure 5.22: Average efficiency with respect to W_A and W_D with $W_B = W_A$, $W_C = W_D$

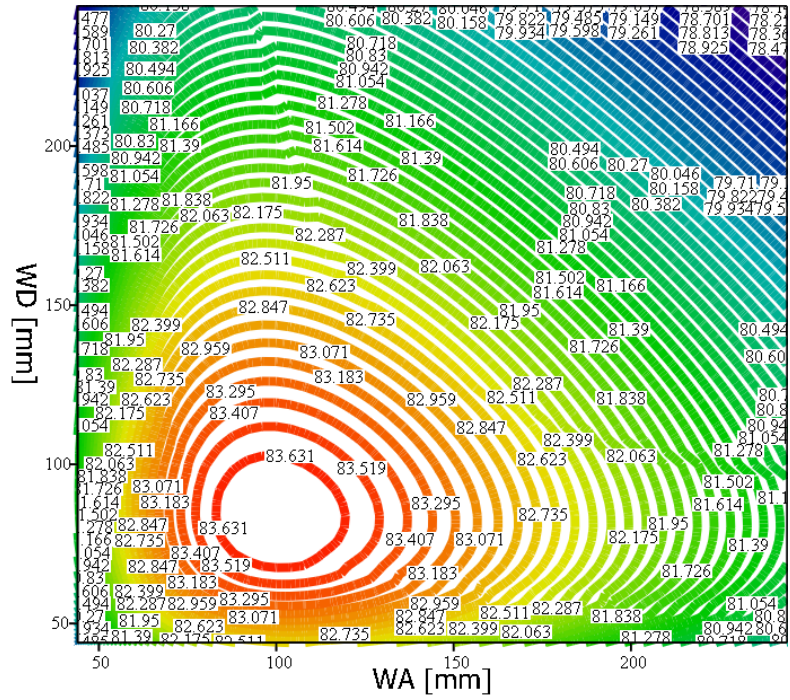


Figure 5.23: Average efficiency with respect to W_A and W_D with $W_B = 2 \times W_A$, $W_C = 2 \times W_D$

Chapter 6

Conclusions

This dissertation proposed a new sample-data modeling of double edge current programmed mode control (DECPCM). This DECPCM controls the peak and valley value of the sensed inductor current. By inserting double slopes of the ramp signal into the control signal, this DECPCM has a fixed frequency which is two times of the frequency of the ramp signal. The steady state condition is derived to be same as that of the conventional current programmed mode control (CPM). The subharmonic oscillation is analyzed. The inductor current attenuation factor (α) of the DECPCM has always one irrespective of the duty ratio when the ramp signal is not applied. Once ramp signal is applied, the inductor current attenuation factor of the DECPCM has always less than one, and no subharmonic oscillation occurs for all duty range.

The sample-data model of DECPCM is derived with a similar method done by Ridley. In conventional single CPM, the inductor current perturbation happens only once in each switching period and is held for one switching period. This makes the sampling frequency of the control the same as the switching frequency of the power stage. However, in DECPCM, the inductor current perturbations happen (are sampled) two times during

one switching period, and each updated inductor current perturbation is kept (held) for DT_s and $(1 - D)T_s$ respectively. Therefore, DECPM has a fixed switching frequency in the power stage but variable sampling frequency for the control with different operating points. The sample-data model of the DECPM is derived by mathematically combining the conventional peak and valley current programmed mode control model. With the assumption that the control signal perturbation (\hat{v}_c) does not change during one switching cycle (T_s), each modeling of peak and valley current mode control for DECPM derived independently. From the results of the modeling, DECPM shows two major difference from the conventional CPM. One is the sampling frequency dependence on the duty ratio. The conventional CPM has a constant sampling frequency of the control which is same frequency with the switching frequency of the power stage. For this reason, the system is always limited by the switching frequency. However, the sampling frequency of DECPM change from switching frequency of power stage (at $D=0$ or $D=1$) to two times of the switching frequency (at $D=0.5$). Therefore, DECPM can have wider bandwidth than CPM when duty ration is not zero or one. The other feature of DECPM is a larger current loop gain than in single CPM. For example, the peak CPM has larger current loop gain at high duty ratio and the valley CPM has larger one at low duty ratio. But DECPM follows the larger current loop gains of either peak CPM or valley CPM at both high and low duty ratio. These features make DECPM possible to have as constant dynamics upto high frequency for all duty ratio and to be applicable to the wide range DC-DC converter application.

A 10MHz CMOS 4 switch buck boost converter (4SBBC) is designed and implemented with DECPM. A $0.5\mu m$ CMOS JAZZ process is used and the power stage and all controller including compensator are integrated into a single die. Experimental results show that the 4SBBC generates the output voltage range of 0.7V to 5V with a nominal input

voltage of 3.3V and exhibits a smooth mode change between buck and boost modes. The maximum load current is 460mA, and the peak efficiency of 80% is measured at a 10MHz switching frequency.

The power stage optimization of 4SBBC for polar modulation is showed. The detail power breakdown is analyzed for each buck and boost mode condition. Due to the fact that the high side switch is implemented with PMOS, the diode conduction model is included at low output voltage. The analytical loss model of 4SBBC is verified by CADENCE simulation and measurement results. With a EDGE envelope signal which is used as a reference signal to 4SBBC for polar modulation, the average efficiency is used for the optimization process.

6.1 Future works

As switching frequency is getting higher, the internal delay of the controller affect to the stability of the system [42]. These internal delay comes from driver, current sensor, voltage loop compensator, comparator, etc. In single CPM, one edge of duty cycle is determined by control law which experience signal delay through the loop, but another edge is set by clock which does not experience control delay. Therefore, in single CPM case, signal delay may affect switching period/frequency and cause system to be unstable even with small internal signal due to asymmetric signal delay on both edge of duty information. However, in DECPM, both edge of the duty cycle is determined by the control laws and experience same control delay on them. So, even if there exists signal delays through the control path, this delay does not affect to switching period/frequency. Therefore, it can be assumed that DECPM have an advantage of insensitiveness to the internal delay.

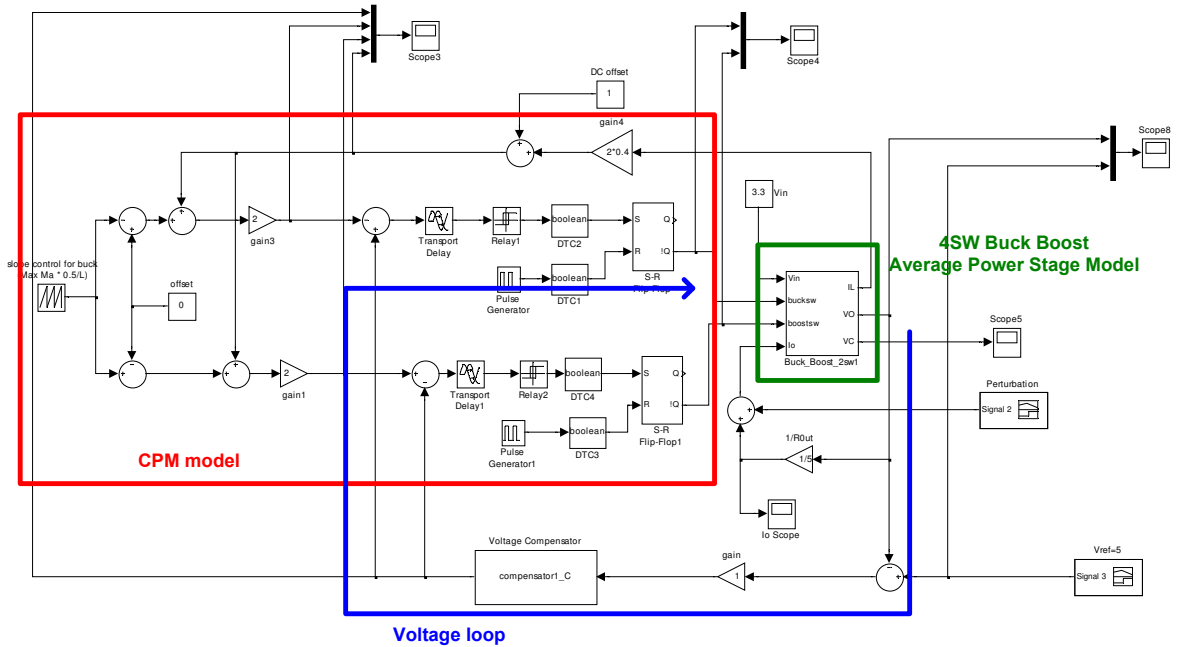


Figure 6.1: Simulink time domain test bench for CPM

Fig.6.1 and Fig.6.2 are the time domain test benches for CPM and DECPM respectively designed in MATLAB Simulink. The 10MHz 4SBBC is used for the comparison. In these simulations, the input voltage V_g is 3V, and reference signal is applied to change the output voltage from 0V to 5V.

Fig.6.3 to Fig.6.6 show the simulation results of CPM with 3nsec internal delay added. Fig.6.3 shows the quasi DC simulation of the reference signal and the corresponding output voltage. Fig.6.4 shows the control signals for CPM; control signal, ramp signal, and inductor current waveforms. Here, peak CPM is used for buck mode and valley CPM is used for boost mode. Fig.6.5 and Fig.6.6 are zoomed-in diagram of Fig.6.4 in buck mode and boost mode respectively. As shown these diagrams, CPM runs stable with 3nsec internal delay. From Fig.6.7 to Fig.6.10 are the simulation results of CPM

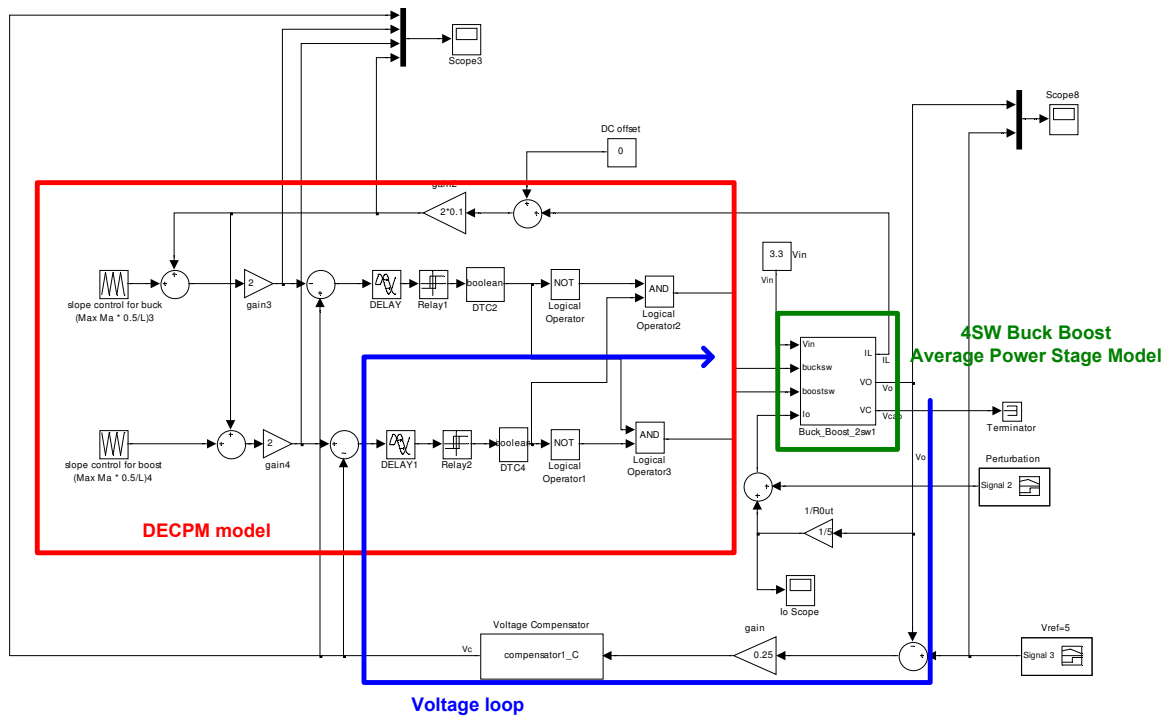


Figure 6.2: Simulink time domain test bench for DECPM

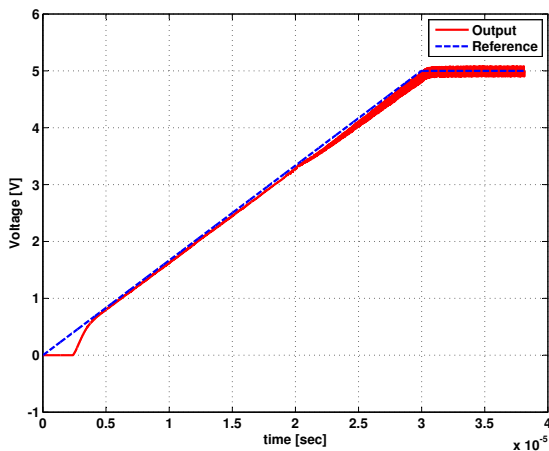


Figure 6.3: Quasi DC simulation of CPM with 3nsec internal delay

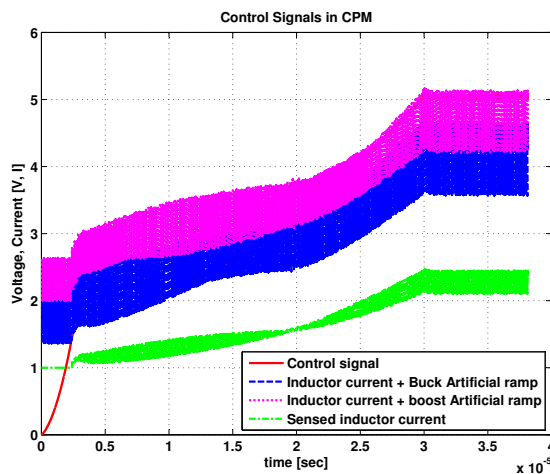


Figure 6.4: Control signals of CPM with 3nsec internal delay

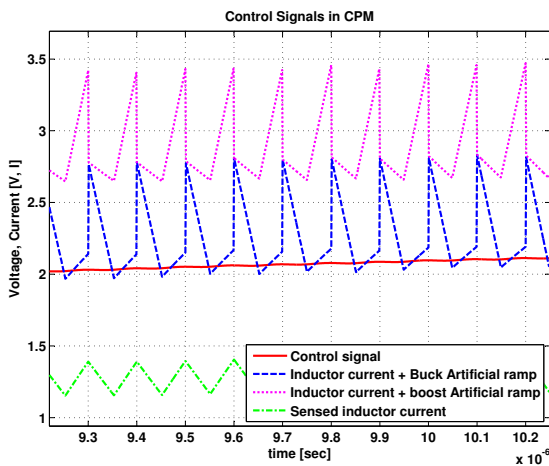


Figure 6.5: Control signals of CPM in buck mode with 3nsec internal delay

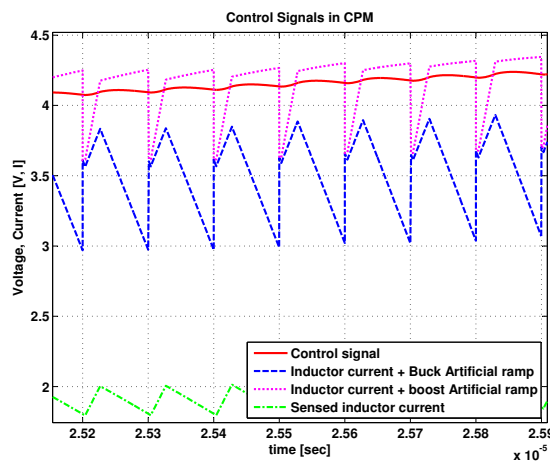


Figure 6.6: Control signals of CPM in boost mode with 3nsec internal delay

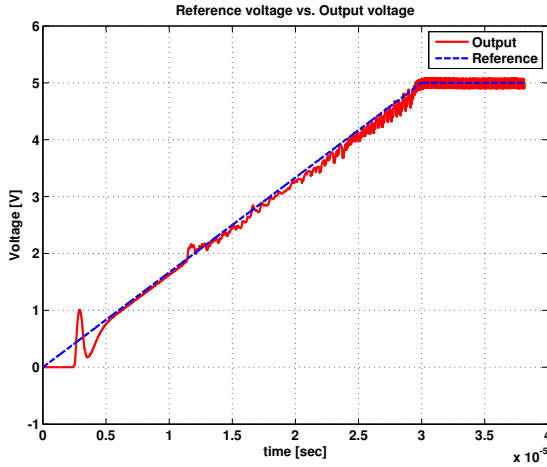


Figure 6.7: Quasi DC simulation of CPM with 5nsec internal delay

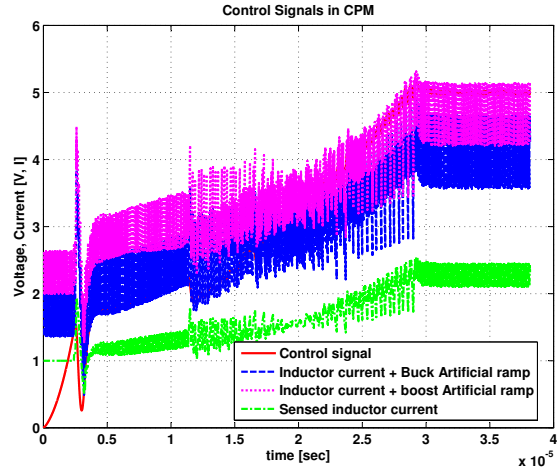


Figure 6.8: Control signals of CPM with 5nsec internal delay

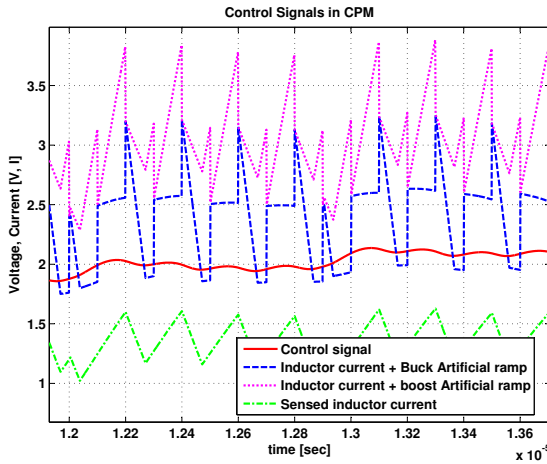


Figure 6.9: Control signals of CPM in buck mode with 5nsec internal delay

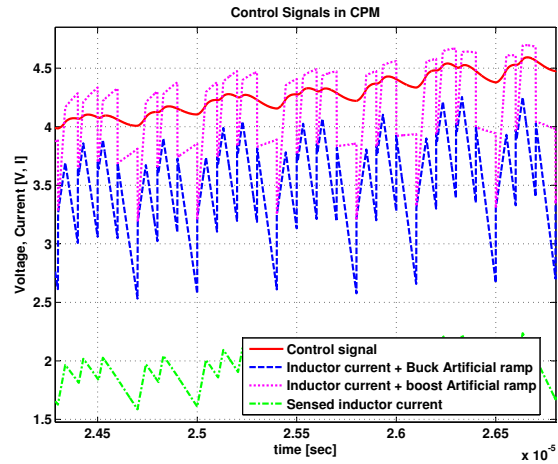


Figure 6.10: Control signals of CPM in boost mode with 5nsec internal delay

with 5nsec internal delay added. As shown these results, 5nsec internal delay makes the system with CPM unstable. This simulation shows that when CPM controller is designed for the converter, the each components in the controller need to be designed to have less than total 5nsec internal delay.

From Fig.6.11 to Fig.6.14 are the simulation results of DECPM with 20nsec internal delay added. Interestingly, in DECPM, the system runs stable still with 20nsec delay into control loop. From Fig.6.15 to Fig.6.18 are the simulation results of DECPM with 55nsec internal delay added. By adding 55nsec internal delay into DECPM, the system start to be unstable in both buck and boost mode.

According to the above simulation, DECPM can tolerate internal delay of almost half of the switching period. This means when you design a high frequency converter, you have much more freedom for delay issues in DECPM than in CPM. This would be design benefit to high frequency converter control. More analytical and mathematical proofs are needed on this delay insensitivity as a future work.

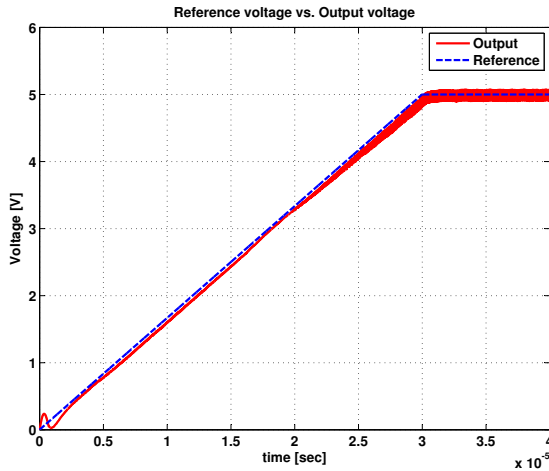


Figure 6.11: Quasi DC simulation of DECPM with 20nsec internal delay

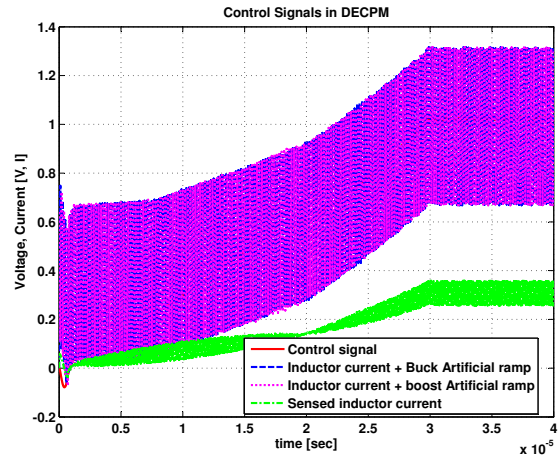


Figure 6.12: Control signals of DECPM with 20nsec internal delay

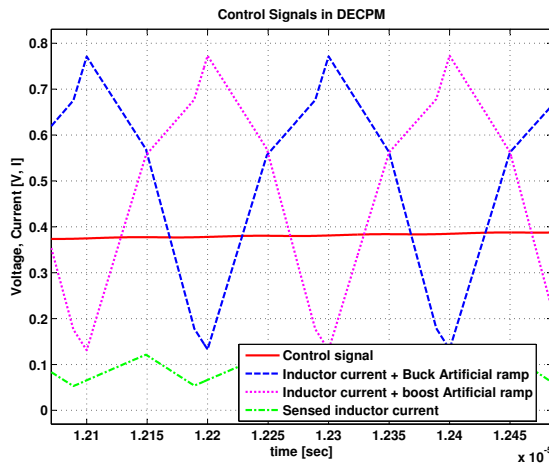


Figure 6.13: Control signals of DECPM in buck mode with 20nsec internal delay

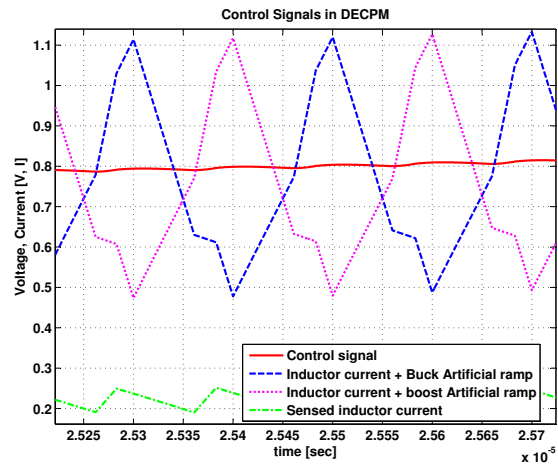


Figure 6.14: Control signals of DECPM in boost mode with 20nsec internal delay

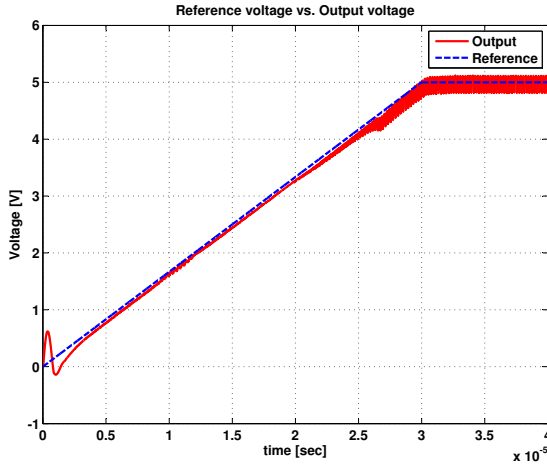


Figure 6.15: Quasi DC simulation of DECPM with 55nsec internal delay

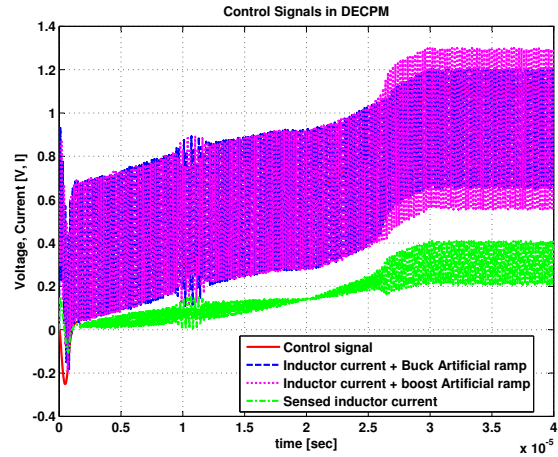


Figure 6.16: Control signals of DECPM with 55nsec internal delay

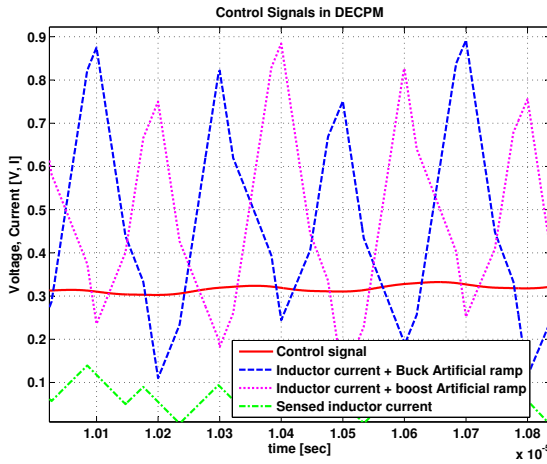


Figure 6.17: Control signals of DECPM in buck mode with 55nsec internal delay

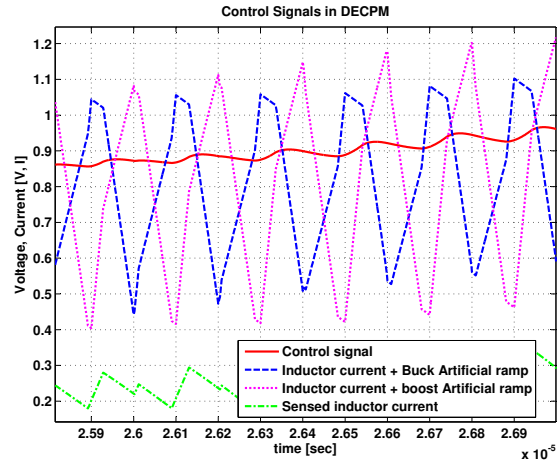


Figure 6.18: Control signals of DECPM in boost mode with 55nsec internal delay

REFERENCES

- [1] H. Qiao, Y. Zhang, Y. Yao, and L. Wei, "Analysis of buck-boost converters for fuel cell electric vehicles," in *Vehicular Electronics and Safety, 2006. ICVES 2006. IEEE International Conference on*, Dec. 2006, pp. 109–113.
- [2] M. Gaboriault and A. Notman, "A high efficiency, noninverting, buck-boost DC-DC converter," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, vol. 3, June 2004, pp. 1411–1415.
- [3] P. Midya, K. Haddad, and M. Miller, "Buck or boost tracking power converter," *IEEE Trans. Power Electron. Lett.*, vol. 2, no. 4, pp. 131–134, Dec. 2004.
- [4] R. Paul, L. Corradini, and D. Maksimovic, " $\Sigma - \Delta$ modulated digitally controlled non-inverting buck-boost converter for WCDMA RF power amplifiers," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2009, pp. 533 – 539.
- [5] D. K. Su and W. J. McFarland, "An IC for linearizing RF power amplifiers using envelope elimination and restoration," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 2252–2258, Dec. 1998.
- [6] P. Nagle, P. Burton, E. Heaney, and F. McGrath, "A wide-band linear amplitude modulator for polar transmitters based on the concept of interleaving delta modulation," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1748–1756, Dec. 2002.
- [7] M. R. Elliot *et al.*, "A polar modulator transmitter for GSM/EDGE," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2190–2199, Dec. 2004.
- [8] N. Schlumpf, M. Declercq, and C. Dehollain, "A fast modulator for dynamic supply linear RF power amplifier," *IEEE J. Solid-State Circuits*, vol. 39, no. 7, pp. 1015–1025, July 2004.
- [9] T. Sowlati *et al.*, "Quad-band GSM/GPRS/EDGE polar loop transmitter," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2179–2189, Dec. 2004.
- [10] P. Reynaert and M. S. J. Steyaert, "1.75-GHz polar modulated CMOS RF power amplifier for GSM-EDGE," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2598–2608, Dec. 2005.
- [11] G. Hanington, P. F. Chen, V. Radisic, T. Itoh, and P. M. Asbeck, "Microwave power amplifier efficiency improvement with a 10MHz HBT DC-DC converter," in *IEEE MTT-S International Microwave Symposium Digest*, vol. 2, June 1998, pp. 589–592.

- [12] F. H. Raab, B. E. Sigmon, R. G. Myers, and R. M. Jackson, "L-band transmitter using kahn EER technique," *IEEE Trans. Microwave Theory Tech.*, vol. 46, no. 12, pp. 2220–2225, Dec. 1998.
- [13] G. Hanington *et al.*, "High-efficiency power amplifier using dynamic power-supply voltage for CDMA application," *IEEE Trans. Microwave Theory Tech.*, vol. 47, no. 8, pp. 1471–1476, Aug. 1999.
- [14] M. Ranjan, K. H. Koo, G. Hanington, C. Fallesen, and P. Asbeck, "Microwave power amplifiers with digitally-controlled power supply voltage for high efficiency and high linearity," in *IEEE MTT-S International Microwave Symposium Digest*, vol. 1, June 2000, pp. 493–496.
- [15] D. R. Anderson and W. H. Cantrell, "High-efficiency high-level modulator for use in dynamic envelope tracking CDMA RF power amplifiers," in *IEEE International Symposium on Circuits and Systems (ISCAS'05)*, vol. 3, May 2001, pp. 1509–1512.
- [16] B. Sahu and G. A. Rincon-Mora, "A high-efficiency linear RF power amplifier with a power-tracking dynamically adaptive buck-boost supply," *IEEE Trans. Microwave Theory Tech.*, vol. 52, no. 1, pp. 112–120, Jan. 2004.
- [17] B. Sahu and G. A. Rincon-Mora, "A high efficiency WCDMA RF power amplifier with adaptive, dual-mode buck-boost supply and bias-current control," *IEEE Microwave Wireless Compon. Lett.*, vol. 17, no. 3, pp. 238–240, Mar. 2007.
- [18] B. Sahu and G. A. Rincon-Mora, "Noninverting, synchronous buck-boost converter for portable applications," *IEEE Trans. Power Electron.*, vol. 19, pp. 443–452, Mar. 2004.
- [19] M. Manninger, "Power management for portable devices," in *Solid State Circuits Conference, 2007. ESSCIRC 2007. 33rd European*, Sept. 2007, pp. 167–173.
- [20] J. Chen, D. Maksimovic, and R. Erickson, "Buck-boost PWM converters having two independently controlled switches," in *Power Electronics Specialists Conference, 2001. PESC. 2001 IEEE 32nd Annual*, vol. 2, 2001, pp. 736–741 vol.2.
- [21] —, "Analysis and design of a low-stress buck-boost converter in universal-input PFC applications," *Power Electronics, IEEE Transactions on*, vol. 21, no. 2, pp. 320–329, March 2006.
- [22] D. Sable, R. Ridley, and B. Cho, "Comparison of performance of single-loop and current-injection-control for pwm converters which operate in both continuous and discontinuous modes of operation," in *Power Electronics Specialists Conference, 1990. PESC '90 Record., 21st Annual IEEE*, Jun 1990, pp. 74–79.

- [23] V. Pinon, B. Allard, and C. Garnier, “High-frequency monolithic dc/dc converter for system-on-chip power management,” in *Power Semiconductor Devices and IC’s, 2006. ISPSD 2006. IEEE International Symposium on*, June 2006, pp. 1–4.
- [24] R. B. Ridley, “A new, continuous-time model for current-mode control,” *IEEE Trans. Power Electron.*, vol. 6, no. 2, pp. 271–280, Apr. 1991.
- [25] —, “A new continuous-time model for current-mode control with constant frequency, constant on-time, and constant off-time, in CCM and DCM,” in *Power Electronics Specialists Conference (PESC)*, June 1990, pp. 382 – 389.
- [26] R. Ridley, “Current mode or voltage mode?” *Switching Power Mag.*, Oct 2000.
- [27] B. Bell and D. Pace, “Buck regulator topologies for wide input/output voltage differentials,” *Power Designer, National Semiconductor*.
- [28] C.-C. Yang, C.-Y. Wang, and T.-H. Kuo, “Current-mode converters with adjustable-slope compensating ramp,” in *Circuits and Systems, 2006. APCCAS 2006. IEEE Asia Pacific Conference on*, Dec. 2006, pp. 654–657.
- [29] J. Guo, “Investigating feedforward mechanism in current mode control,” in *Applied Power Electronics Conference and Exposition, 2006. APEC ’06. Twenty-First Annual IEEE*, March 2006, pp. 6 pp.–.
- [30] Y. Qiu, J. Sun, M. Xu, K. Lee, and F. Lee, “Bandwidth improvements for peak-current controlled voltage regulators,” *Power Electronics, IEEE Transactions on*, vol. 22, no. 4, pp. 1253–1260, July 2007.
- [31] F. D. Tan and R. Middlebrook, “A unified model for current-programmed converters,” *IEEE Trans. Power Electron.*, vol. 10, no. 4, pp. 397 – 408, July 1995.
- [32] F. Azcondo, C. Bracas, R. Casanueva, and D. Maksimovic, “Approaches to modeling converters with current programmed control,” in *Power Electronics Education, 2005. IEEE Workshop*, 16-17, 2005, pp. 98–104.
- [33] B. Choi, “Step load response of a current-mode-controlled dc-to-dc converter,” *Aerospace and Electronic Systems, IEEE Transactions on*, vol. 33, no. 4, pp. 1115–1121, Oct. 1997.
- [34] R. W. Erickson and D. Maksimovic, Eds., *Fundamentals of Power Electronics*, 2nd ed. Norwell, Massachusetts: Kluwer Academic Publisher, 2001.
- [35] J. Sun, “Small-signal modeling of variable-frequency pulsewidth modulators,” *IEEE Trans. Aerosp. Electron. Syst.*, vol. 38, pp. 1104 – 1108, July 2002.

- [36] R. Redl, “High-frequency extension of the small-signal model of the constant-frequency current-mode-controlled converter,” in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 1991, pp. 466 – 472.
- [37] —, “Small-signal high-frequency analysis of the free-running current-mode-controlled converter,” in *IEEE Power Electronics Specialists Conference (PESC)*, 1991, pp. 897 – 906.
- [38] V. Vorperian, “Simplified analysis of PWM converters using the model of the PWM switch ; part I and II,” *IEEE Aerosp. Electron. Syst. Mag.*, vol. 26, no. 2, Mar. 1990.
- [39] D. J. Perreault and G. C. Verghese, “Time-varying effects and averaging issues in models for current-mode control,” *IEEE Trans. Power Electron.*, vol. 12, pp. 453–461, May 1997.
- [40] G. C. Verghese, C. A. Bruzos, and K. N. Mahabir, “Averaged and sampled-data models for current mode control: a re-examination,” in *IEEE Power Electronics Specialists Conference (PESC)*, June 1989, pp. 484 – 491.
- [41] Q. Yang, Y. Kaiwei, M. Yu, X. Ming, F. Lee, and Y. Mao, “Control-loop bandwidth limitations for multiphase interleaving buck converters,” in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, vol. 2, 2004, pp. 1322 – 1328.
- [42] K. Lee, P. Harriman, and H. Zou, “Analysis and design of the dual edge controller for the fast transient voltage regulator,” in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2009, pp. 1184 – 1189.
- [43] W. Qiu, G. Miller, and Z. Liang, “Dual-edge pulse width modulation scheme for fast transient response of multiple-phase voltage regulators,” in *IEEE Power Electronics Specialists Conference (PESC)*, 2007, pp. 17 – 21.
- [44] P. Midya and K. Haddad, “Two sided latched pulse width modulation control,” in *IEEE Power Electronics Specialists Conference (PESC)*, vol. 2, June 2000, pp. 18–23.
- [45] J. Li and F. Lee, “New modeling approach for current-mode control,” in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Feb. 2009, pp. 305–311.
- [46] Y. Qiu, J. Sun, M. Xu, K. Lee, and F. Lee, “High-bandwidth designs for voltage regulators with peak-current control,” in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Feb. 2006, pp. 24–30.

- [47] Y. Lee, A. Khaligh, and A. Emadi, "A compensation technique for smooth transitions in non-inverting buck-boost converter," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2009, pp. 608 – 614.
- [48] R. Paul and D. Maksimovic, "Analysis of PWM nonlinearity in non-inverting buck-boost power converters," in *IEEE Power Electronics Specialists Conference (PESC)*, 2008, pp. 3741–3747.
- [49] H. P. Forghani-zadeh and G. A. Rincon-Mora, "Current-sensing techniques for DC-DC converters," in *The 2002 45th Midwest Symposium on Circuits and Systems, 2002*, vol. 2, Aug. 2002, pp. 577–580.
- [50] J. Pearson, "Design ideas, active-feedback ic serves as current-sensing instrumentation amplifier," *EDN*, p. 86, July 2003. [Online]. Available: <http://www.edn.com/contents/images/72403di.pdf>
- [51] E. Brunner and B. Gilbert, "The active feedback amplifier. a versatile analog building block," in *Proc. Northcon '94*, Oct. 1994, pp. 131–136.
- [52] A. Hadjichristos *et al.*, "A highly integrated quad band low EVM polar modulation transmitter for GSM/EDGE applications," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC'04)*, Oct. 2004, pp. 565–568.
- [53] F. H. Rabb *et al.*, "Power amplifiers and transmitters for RF and microwaves," *IEEE Trans. Microwave Theory Tech.*, vol. 50, no. 3, pp. 814–826, Mar. 2002.
- [54] A. Mashhour, "Understanding offset 8-PSK. modulation for GSM EDGE," *Microwave Journal*, vol. 42, pp. 78–92, Oct. 1999.