ABSTRACT

KANG, INKUK Formation of N^+P Junctions Using In-situ Phosphorus Doped Selective $Si_{1-x}Ge_x$ Alloys for CMOS Technology Nodes Beyond 50nm. (Under the direction of Dr. Mehmet C. Öztürk.)

As CMOS integrated circuits are scaled beyond the 50nm regime, conventional source/drain junction and contact technologies can no longer satisfy the requirements of MOSFETs, which require super-abrupt doping profiles and extremely low contact resistivities. To address these challenges, selective $Si_{1-x}Ge_x$ source/drain technology was proposed by this laboratory. In this approach, in-situ doped $Si_{1-x}Ge_x$ layers are selectively deposited in recessed source/drain regions. Since the dopants occupy substitutional sites during epitaxial growth, high temperature annealing is not required for dopant activation, which eliminates diffusion and provides abrupt doping profiles. Furthermore, smaller bandgap of $Si_{1-x}Ge_x$ reduces the metal-semiconductor barrier height, an essential requirement for achieving a substantial reduction in contact resistivity.

This thesis focuses on selective rapid thermal chemical vapor deposition of in-situ phosphorus doped $Si_{1-x}Ge_x$ alloys intended for this application. Experiments were carried out to study electrical properties of the in-situ doped layers with emphasis on maximizing the active carrier concentration. Active phosphorus levels in the range of $2 - 5 \times 10^{20}$ cm^{-3} were obtained.

The deposited layers were used to fabricate pn junctions with excellent reverse leakage characteristics. Junctions fabricated on lightly doped substrates exhibited behavior equivalent to best junctions in spite of the lattice mismatch between the Si substrate and the phosphorus doped $Si_{1-x}Ge_x$. Junctions fabricated on heavily doped substrates suffered from band to band tunneling, which is expected regardless of the junction formation technique.

Deposition selectivity of the process was studied and determined that high flows of PH_3 could degrade the selectivity. An alternative deposition process based on alternating periods of deposition and etching was developed, which provided substantial improvements in deposition selectivity.

FORMATION OF N^+P JUNCTIONS USING
IN-SITU PHOSPHORUS DOPED SELECTIVE $SI_{1-X}GE_X$ ALLOYS FOR
CMOS TECHNOLOGY NODES BEYOND 50 NM

by

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Biography

Inkuk Kang was born on May 11, 1961 to Inseon Kang-Oh and Changhee Kang in Seoul, Korea. In 1981, he pursued his undergraduate studies at Kon-Kuk University. In May, 1985, he received his Bachelor of Science degree in Physics. After spending several years in military service and personal business, he came to US to study Physics in Stevens Institute of Technology in 1992. He received Master of Science in May, 1994. After spending another two years in the Physics department of the State University of New York at Buffalo, New York, he transferred to North Carolina State University to study electrical engineering in the field of microelectronics. In 2001, he joined Advanced Micro Devices, INC and expects to finish his Ph.D. degree at North Carolina State University in June, 2003.

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I.1   Source/Drain (S/D) Junction Requirements for Technology Nodes Beyond 50nm

In order to improve the performance of Complementary Metal Oxide Semiconductor (CMOS) integrated circuits, aggressive scaling of MOSFETs has been continued for the past 30 years. One of the key device parameters that needs to be scaled is the source/drain junction depth [1 - 3]. Currently used junction technologies rely on low-energy ion-implantation followed by rapid thermal annealing (RTA) [4]. However, as MOSFETs are scaled beyond the 50nm regime, this approach can no longer satisfy the source/drain requirements. According to the 2001 edition of the International Technology Roadmap for Semiconductors (ITRS), future junctions will require (a) junctions as shallow as 10 nm; (b) above equilibrium dopant activation; (c) super abrupt doping profiles; (d) contact resistivity near $\sim 10^{-8}$ ohm-cm^2 [5].

The main challenge in source/drain engineering is to form ultra-shallow junctions with a small parasitic series resistance. It is required that the total series resistance is limited to a small fraction of the channel 'on' resistance. In ITRS 1999, total series resistance was limited to 10% of the channel resistance [6]. In ITRS 2001, the percentage depends on the technology node and it varies from 17 % at 100 nm to 35 % at 22 nm.
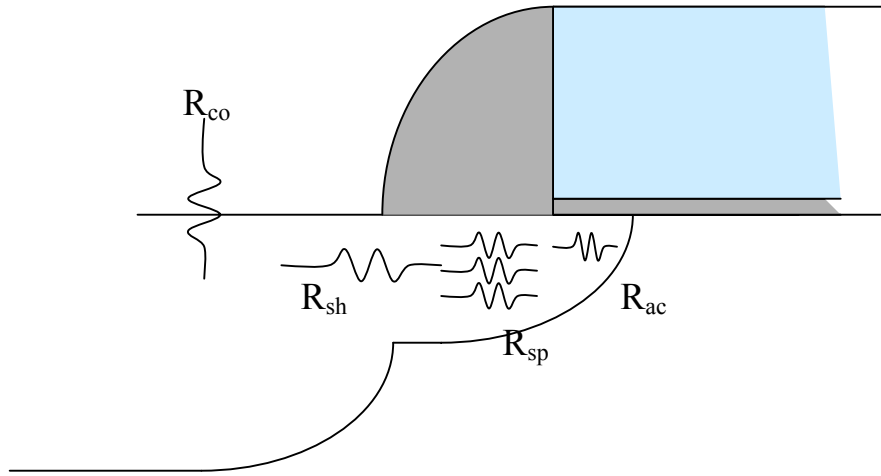
Figure I. 1   The schematic cross-sectional view of a source/drain region with associated series resistance components.

The total junction resistance, R_j, can be modeled as:

$$R_j = R_{ac} + R_{sp} + R_{sh} + R_{co},$$

(1.1)

where R_{ac} is accumulation resistance, R_{sp} is spreading resistance, R_{sh} is sheet resistance of the junction under the sidewall spacer, and R_{co} is the contact resistance [2]. Shown in Figure I.1 is a cross-sectional view of a typical source/drain region illustrating these

components. R_{ac} (not shown in Figure I. 1) is the resistance of the tip of the extension under the gate. Its contribution to the total resistance is small compared to other components. R_{sp} is a strong function of the extension lateral doping gradient. MOSFETs at the end of the roadmap require lateral abruptness figures as small as 2nm/decade. Such values are impossible to achieve by techniques that involve thermal diffusion of dopants. R_{sh} is determined by the resistivity and the depth of the source/drain extension under the sidewall spacer.
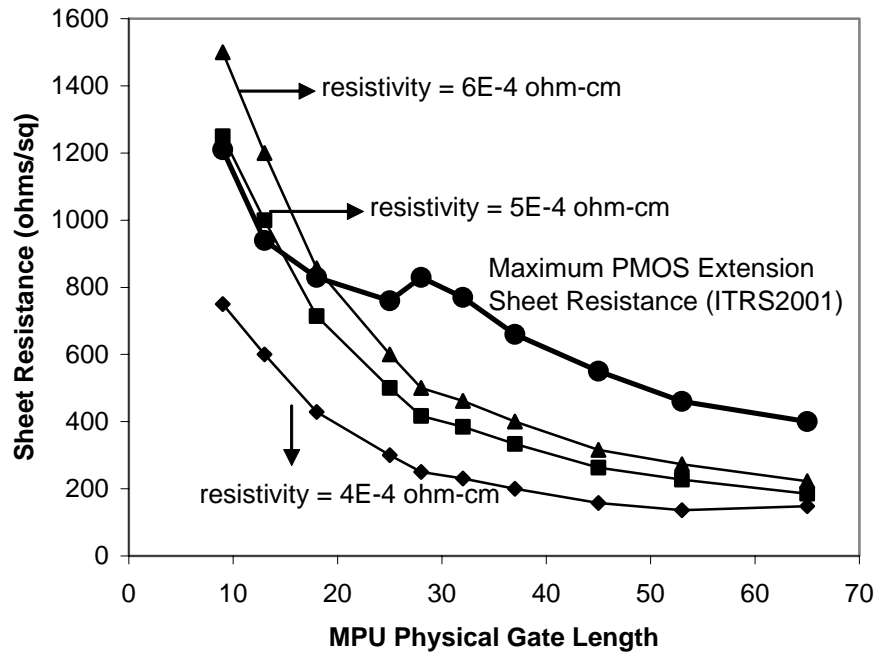
Figure I.2   Calculated sheet resistance using a resistivity of $4 - 6 \times 10^{-4}$ ohm-cm and the maximum PMOS extension sheet resistance from ITRS2001.

Shown in Figure I.2 is the maximum allowable extension sheet resistance as a function of the MPU gate length for different technology nodes. Solid lines correspond to box profiles with different doping densities. As shown, a resistivity of 5 x 10^{-4} ohm-cm is sufficient to satisfy the roadmap requirements for the extension resistance.
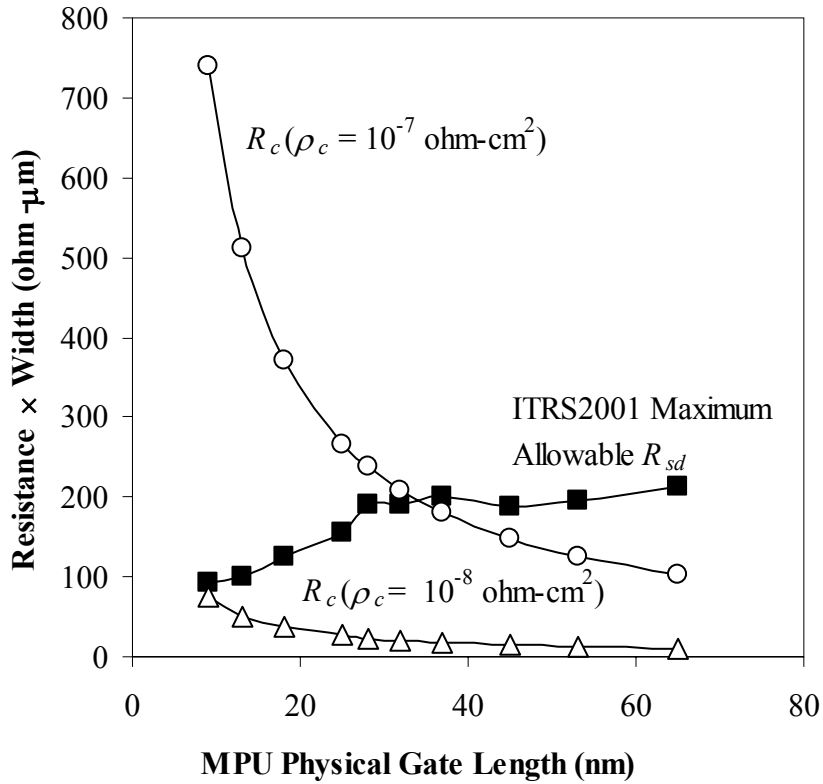
Figure I.3   Maximum allowable source/drain series resistance plotted as a function of MPU physical gate length (solid squares). Also shown is the contact resistance calculated using two different contact resistivities of 10^{-7} (open circles) and 10^{-8} ohm-cm^2 (open triangles).

Shown in Figure I.3 is the maximum allowable series resistance predicted in ITRS 2001 for different technology nodes. The maximum allowable series resistance is obtained

from the proposed values for the power supply voltage (V_{dd}), drive current (I_{dd}) and the parasitic S/D resistance percentage of the channel resistance (V_{dd}/I_{dd}) given in ITRS 2001 [2]. Also plotted in Figure I.3 is the contact resistance for two specific contact resistivity values of 10^{-7} and 10^{-8} ohm-cm^2 calculated assuming the junction length is three times that of the physical gate length. As shown, if the contact resistivity is kept at its current value of $\sim 10^{-7}$ ohm-cm^2, just the contact resistance alone will produce series resistance values that will be unacceptable for CMOS technology nodes with physical gate lengths smaller than $\sim$ 30 nm. According to the ITRS 2001, future CMOS technology nodes will require contact resistivity values as low as 10^{-8} ohm-cm^2, as shown in Figure I.3. It is clear that such low contact resistivity values cannot be achieved on n$^+$ or p$^+$ Si using a single mid-gap contact material. In order to meet the contact resistivity requirements for future CMOS technology nodes, smaller contact barrier heights and/or above equilibrium dopant activation levels are required. This means that fundamentally new approaches will be required to decrease the contact resistivity by an order of magnitude during the next 10 years.

The resistivity of an ohmic contact is determined by the Schottky barrier height at the metal-semiconductor interface and the doping density under the metal as illustrated in Figure I.4. Due to Fermi level pinning, the Fermi level on the metal side lies near the Si midgap, which results in a contact barrier height of approximately $E_g/2 \sim 0.6$ eV. Using this barrier height and the boron solid solubility limit of ~ 2 x 10^{20} cm^{-3} in Si, we obtain a contact resistivity of $\sim 10^{-7}$ cm^2, which is an order of magnitude higher than what we need at the end of the roadmap [7]. Since contact resistivity is an exponential function of the

barrier height, a large improvement in contact resistivity can be achieved by a small reduction in barrier height. For technology nodes beyond 50nm, ITRS 2001 predicts that the contact resistance will dominate the series resistance.
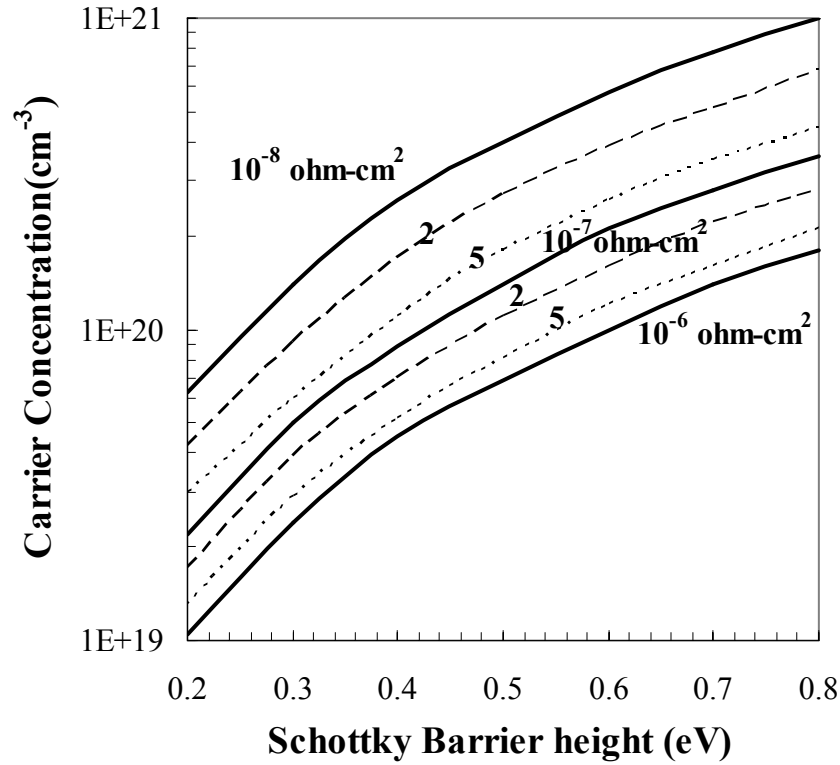
Figure I.4   Dependence of contact resistivity on carrier concentration and Schottky barrier height.

The source/drain challenges mentioned above are imposed by the fundamental limits of silicon, which requires new doping and contact formation technologies for future MOSFETs. A variety of junction formation methods are currently under investigation. Of these, laser thermal annealing of implanted dopants is standing out, and has been shown to

be capable of achieving abrupt profiles and above equilibrium dopant activation levels [8]. However, the technique results in metastable activation, which can be lost upon annealing at moderate temperatures. Furthermore, areas surrounding the junctions must be protected against melting with masking layers, which significantly adds to the process complexity. Much research needs to be carried out before the technology can be used in integrated circuit manufacturing.

I.2   Selective $Si_{1-x}Ge_x$ Source/Drain Technology

Recently, a new junction formation technology based on selective deposition of in-situ doped $Si_{1-x}Ge_x$ alloys was proposed and demonstrated for p^+-n junctions using boron as the dopant [7]. In this technology, the source/drain regions are defined by isotropic etching and subsequently filled by selective $Si_{1-x}Ge_x$ deposition. The etch depth determines the junction depth.

The objective of this thesis is to extend this concept to n^+-p junctions using phosphorus as the dopant. It is shown in this thesis that the method can meet all requirements of n^+-p junctions for future technology nodes. Shown in Figure I.5 are the basic fabrication steps for the proposed method for planar MOSFETs. The technology can also be used to form elevated junctions by depositing a $Si_{1-x}Ge_x$ layer thicker than the etch depth. This provides a sacrificial layer to self-aligned contact formation via solid phase reactions between a metal and $Si_{1-x}Ge_x$ [9 - 12]. This is one of the key challenges in forming reliable contacts to ultra-shallow junctions.

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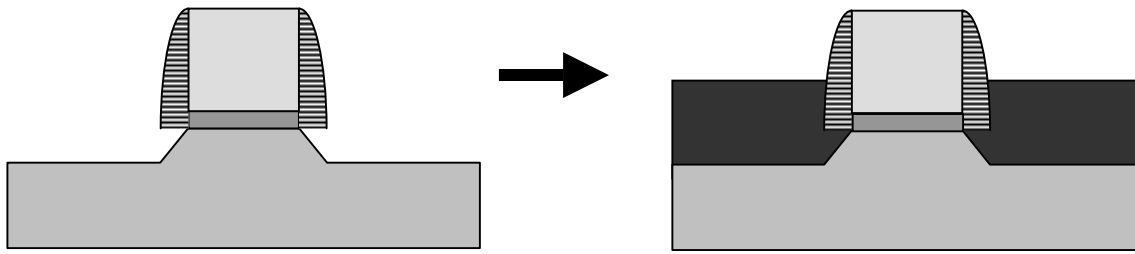
- Isotropic Si-etch to form junction recess

- Selective Si-Ge Deposit
- In-situ above equilibrium doping
- Very abrupt doping gradient
- Low Temperature process
- Raised S/D MOSFET

Figure I.5   Proposed method for fabricating junctions using the selective $Si_{1-x}Ge_x$ technology.

The advantages of the technology include:

a)   In-situ doping results in an abrupt doping profile since no thermal annealing is required to activate the dopants.

b)   Dopant activation in $Si_{1-x}Ge_x$ is higher than it is in Si.

c) $Si_{1-x}Ge_x$ provides a smaller bandgap for low contact resistance.

d)   Low temperature (< 800°C) deposition provides compatibility with high-K dielectrics.
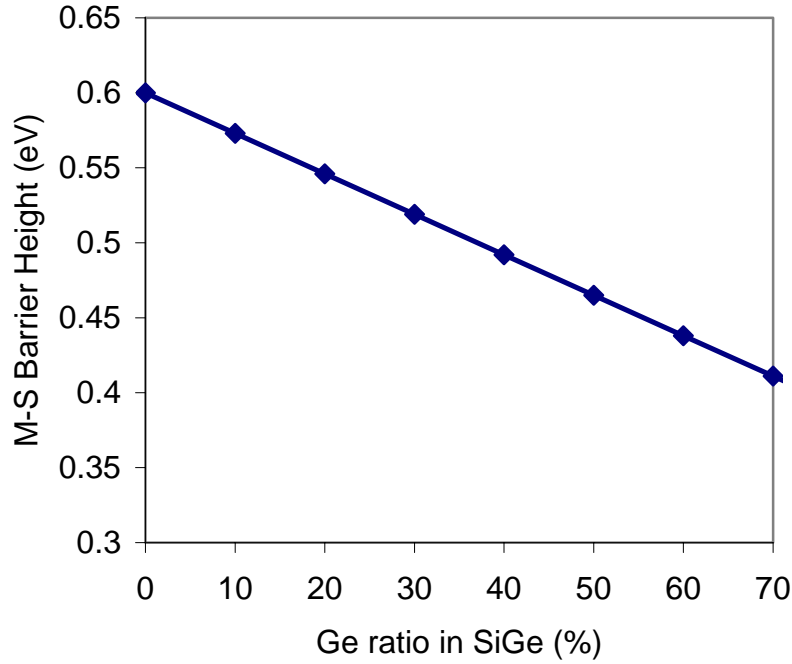
Figure I.6   Metal-Si (MS) contact barrier height using a mid-level metal.

There are several critical process integration issues, which needs to be taken into account. First and foremost, the etched region is required to reach the channel under the gate dielectric in other to realize the connection between the heavily doped junction and the channel. It has been suggested that some small distance can be tolerable without using a substantial increase in the series resistance [13]. Second, the etch chemistry has to be selective with respect to the gate dielectric. Finally, the surface should be suitable for $Si_{1-x}Ge_x$ growth after etching. The very first advantage of $Si_{1-x}Ge_x$ over Si is its smaller bandgap. Figure I.6 shows how the Ge content in $Si_{1-x}Ge_x$ decreases the metal – Si barrier height assuming the Fermi level is pinned at the $Si_{1-x}Ge_x$ midgap and the contact barrier

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height is roughly equal to one half the semiconductor bandgap. It should be noted however that the figure can only provide an approximate guide since the $Si_{1-x}Ge_x$ bandgap depends on the strain. To fully utilize the bandgap advantage of $Si_{1-x}Ge_x$, Ge concentration in the alloy must be raised preferably without forming misfit dislocations at the interface, which may lead to leaky junctions. However, with junction depths approaching a few nanometers, it will be easier to preserve the strain in the alloy.

I.3   Previous Work on Chemical Vapor Deposition of In-Situ Phosphorus Doped Si

Chemical vapor deposition (CVD) of in-situ phosphorus and arsenic doped Si has been extensively studied by many research groups. The results show that unlike CVD of in-situ boron doped Si, n-type doping presents unique challenges. Phosphorus atoms adsorbed on Si surface can reduce the number of available sites and result in significantly reduced growth rates. Another problem is that n-type dopants tend to segregate at the growth surface making it very difficult to grow heavily doped layers. Growing delta doped layers is also difficult due to the same reason.

In this section, we present a brief summary of previous work on CVD of in-situ phosphorus doped Si films. We begin with adsorption-desorption processes on Si and their impact on the deposition rate. We then discuss mechanisms responsible for surface segregation and its effect on phosphorus incorporation. We focus on phosphorus as the n-type dopant of interest.
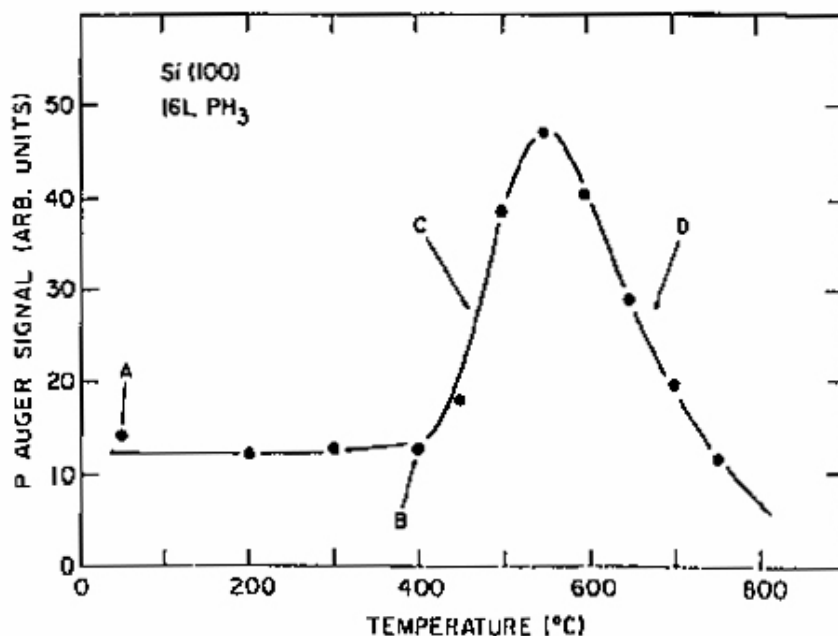
Figure I.7   Phosphorus Auger signal after flowing 1.6×10^{-7} Torr of PH_3 on (100) Si as a function of exposing temperature [15].

a)   Adsorption and Desorption of Phosphorus on Silicon

Yu and Meyerson studied adsorption and desorption of PH_3 on (100) Si [14, 15]. Figure I.7 shows the phosphorus Auger signal after flowing 1.6×10^{-7} Torr-sec of PH_3 on (100) Si at various temperatures [15]. As shown, PH_3 readily adsorbs on the Si surface associatively even at room temperature and the phosphorus level stays constant up to 400°C (A → B). The phosphorus signal starts to rise rapidly above 400°C and reaches a maximum at 550°C due to hydrogen desorption, which provides more available sites to phosphorus atoms (B → C → Max. at 550°C). Over 550°C, phosphorus starts to desorb and phosphorus coverage of the surface decreases (D).

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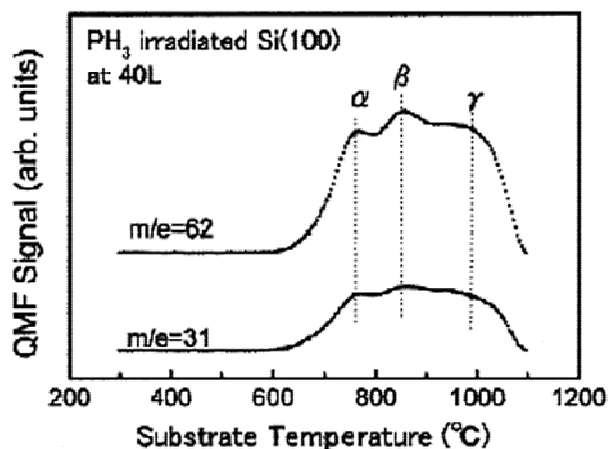
Figure I.8   Thermal desorption spectroscopy (TDS) spectra as a function of substrate temperature for P (m/e= 31) and P_2 (m/e= 62) at 40 L [17].

Hirose and Sakamoto studied phosphorus desorption from Si using thermal desorption spectroscopy (TDS) [16]. After exposing (100) Si surface to 40 langmuirs (1 langmuir = 1 x 10^{-6} Torr-sec) of PH_3 at 600°C, the detected desorption species were P_2 (mass number, m/e=62) and P (m/e=31) only and the P signal was mainly from ionization of P_2 in the quadruple mass filter (QMF) as shown in Figure I.8. Based on this finding, they concluded that desorbed species are mostly P-P. Figure I.9 shows the P_2 signal with three peaks α, β, and γ at 750, 850, and 1000°C, respectively. For low PH_3 exposure, only the β peak exists and it shifts to higher temperatures as the phosphine exposure is reduced. Hirose and Sakamoto claim that the β peak is the desorption of P_2 following the reactions:

2 Si-P (Migrating hetero-dimers) → 2 Si + 2 P (migration) → P_2
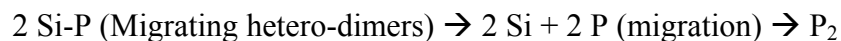
and α peak is the direct desorption of P_2 as

P-P (Migrating mono-dimer) → 2 P (migration) → P_2.
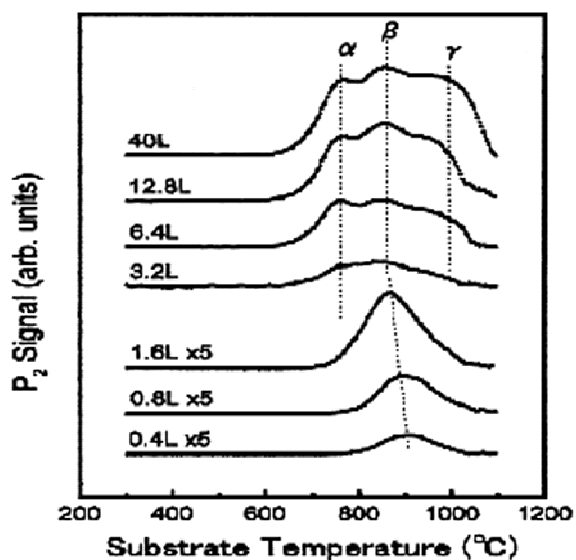
Figure I.9   Thermal desorption spectroscopy (TDS) spectra as a function of substrate temperature for P_2 for different PH_3 exposures [17].

Their arguments are well supported by scanning tunneling microscopy (STM) or Fourier transform infrared spectroscopy (FTIR) studies [17 - 21]. Phosphorus atoms mostly form P-Si hetero-dimers for low exposures of PH_3, and Si-P and P-P dimers for high PH_3 flows.

b)   Deposition Rate

Growth rate reduction for gas source molecular beam epitaxy (GS-MBE) or ultra-high vacuum chemical vapor deposition (UHV- CVD) of silicon with in-situ P or As doping using PH_3 or AsH_3 is well established [22 - 29]. It has been shown that phosphorus atoms passivate the Si surface and block adsorption sites for Si precursors such as SiH_4 or Si_2H_6, which results in reduced growth rates. Soares et.al. claim that each surface arsenic atom has a lone pair of electrons instead of a dangling bond since an As atom has one more electron than a Si atom [29]. They claim that a Si-As dimer acts as if it has a single dangling bond.   It has been reported that the overall activation energy of silane decomposition increases from ~ 10 kcal/mol without arsine to ~ 40 kcal/mol with arsine [30].   Farrow and Filby concluded that arsine acts as a poison in silane pyrolysis deactivating the adsorption sites [31]. J. Shan et.al. have observed that surface phosphorus atoms can form PSiH "hydrided heterodimers" in the presence of surface hydrogen. PSiH has stronger Si-H bonding energy than Si-SiH does, which can degrade the Si growth [21].

c)   Phosphorus Incorporation during CVD of Si

Shown in Figure I.10 is the phosphorus concentration in a multi-layer Si epitaxial structure grown by UHV-RTCVD at NC State University by Ibrahim Ban [27]. The profile was obtained by secondary ion mass spectroscopy (SIMS). Different doping levels were obtained by changing 50 ppm PH_3 flow (diluted in H_2) between 0.3 and 10 sccm. The silicon precursor was 10% Si_2H_6 diluted in He and its flow was kept constant at 130 sccm.
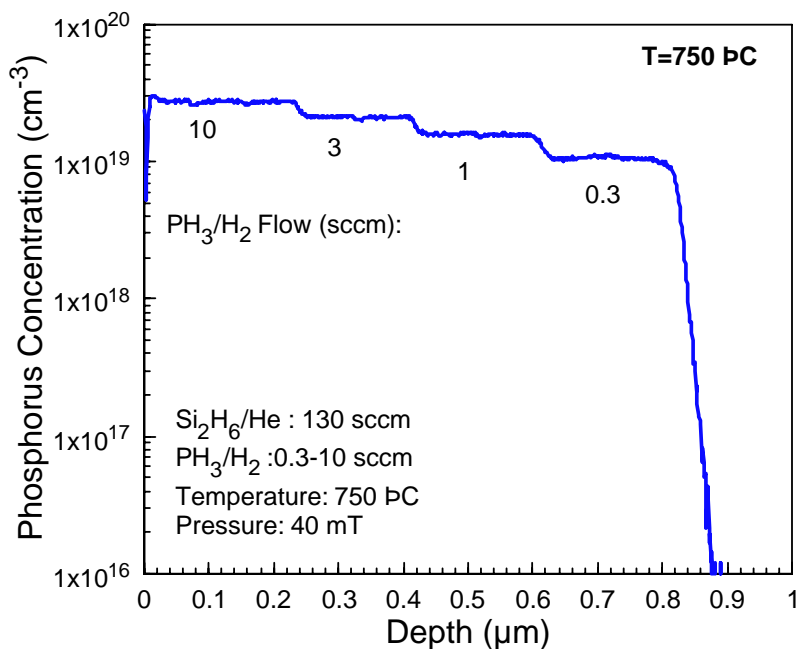
Figure I.10   Phosphorus profile in a multi-layer Si structure obtained by SIMS.

Each step in Figure I.10 corresponds to a growth cycle of one minute at 750 ˚C, except for the last layer (10 sccm case) which was grown for 1.5 min. Figure I.11 shows the phosphorus levels observed in Figure I.10 as a function of the PH_3 partial pressure. Under these conditions, the phosphorus level increases monotonically with the PH_3 partial pressure in the growth ambient [27]. Figure I.12 shows another SIMS multi-layer profile obtained by depositing the layers at 800ºC and 150 mtorr. In an attempt to increase the P incorporation, PH_3 dilution in H_2 was changed from 50 ppm to 1 %. PH_3 flows of 0, 4, 20, 80, 140, and 200 sccm were used to obtain a multi-layer structure. As shown, phosphorus incorporation saturates above a PH_3 flow of approximately 20 sccm.
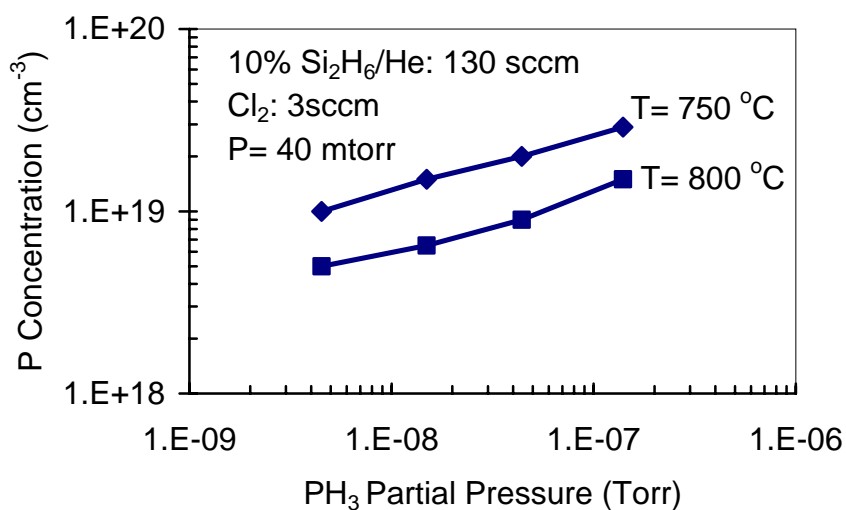
Figure I.11   Phosphorus concentrations extracted from Figure I. at different PH_3 partial pressures.
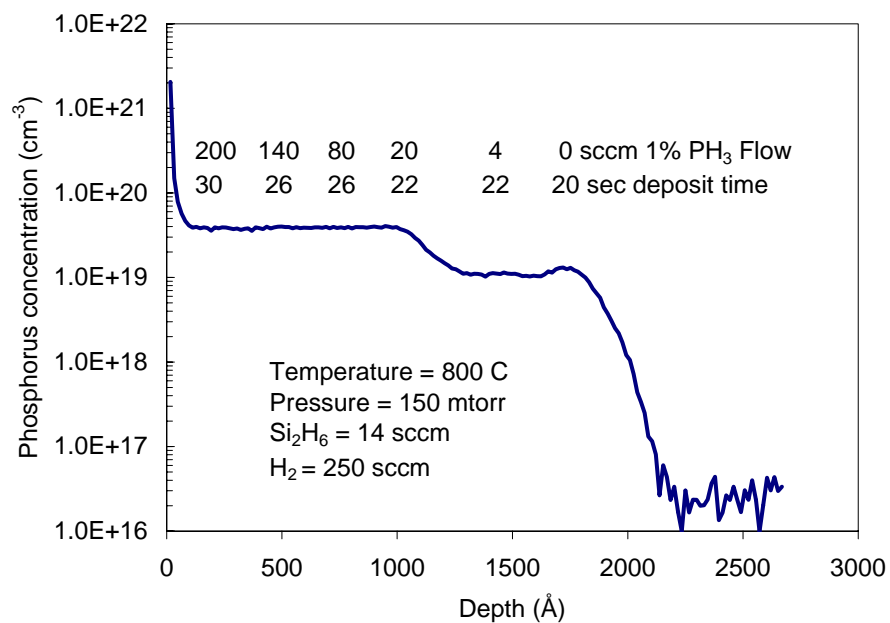
Figure I.12   Phosphorus profile in a multi-layer Si structure obtained by SIMS.
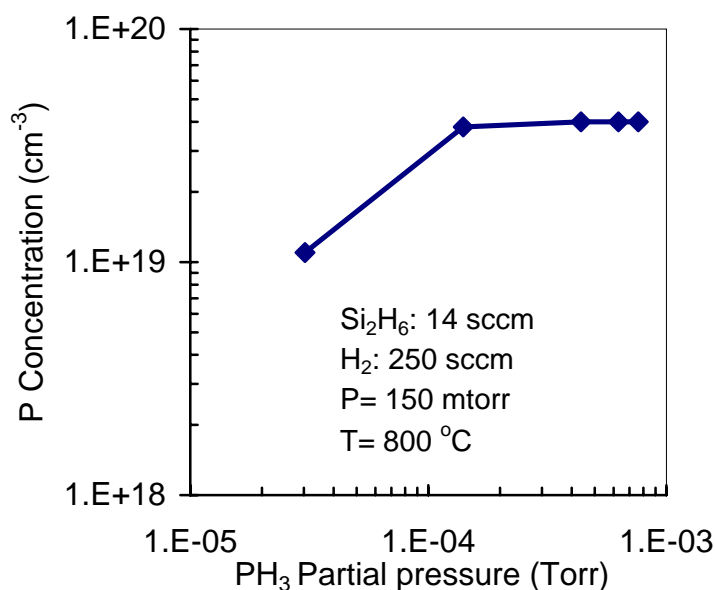
Figure I.13   Phosphorus concentrations extracted from Figure I. at different PH_3 partial pressures.

As shown in Figure I.13, at higher PH_3 partial pressures (three orders of magnitude higher), phosphorus concentration saturates at around 4×10^{19} cm^{-3}.

Similar behavior has been observed by others [22, 23, 25, 28 - 32]. While P-P desorption is enhanced when PH_3 partial pressure is increased, it can not fully explain saturation of phosphorus concentration. Instead, segregation coupled with coulomb repulsion has been proposed to explain this phenomenon.

d)   **Phosphorus segregation**

Surface segregation of n-type dopants, including As [33], P [34 - 38], and Sb [39 -

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47] has been extensively studied by different groups. H. Jorke proposed a two state model to explain the phosphorus segregation [48]. Using rate equations he examined the sub-surface and surface states at the growing boundary. Shown in Figure I.14 is the energy diagram used in the two-state model. On this figure, θ_b and θ_s are the percent coverages of the dopant atoms at the sub-surface and surface, E_d is the desorption energy, E_b is the activation energy for segregation, and E_s is the segregation (Gibb's free) energy. Two atoms, A and B referred to as sub-surface and surface atoms take part in the exchange mechanism. In this model, the critical energies are the desorption energy, E_d, activation energy for segregation, E_b and the segregation energy, E_s. During the formation of a monolayer, a phosphorus atom (A) at the sub-surface exchanges its position with a surface Si atom (B). The driving force for this exchange originates from the difference in the bonding energies of Si – P and Si – Si bonds [46]. The difference is Gibb's free energy or the segregation energy, E_s. For this exchange to occur the sub-surface phosphorus atom should overcome the activation barrier energy, E_b. The segregation probability can be expressed as:

$$P = \exp(- E_s / kT) \tag{1.1}$$

Gibb's energies for P, As, and Sb are known as around 0.63, 0.8, and 1.2 eV, respectively [34, 35, 37, 49].
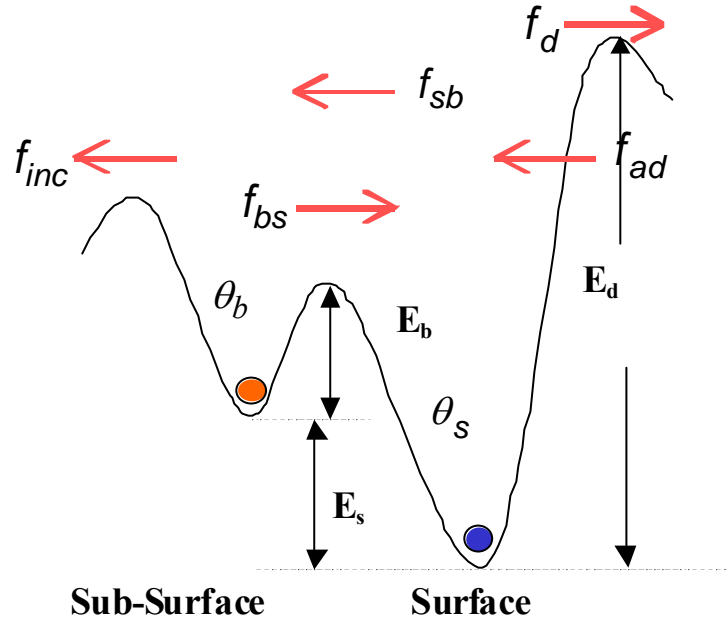
Figure I.14   Schematic view of surface and sub-surface state in Two State Model, where θ_b and θ_s are the dopant coverages at the sub-surface & surface, E_d is the desorption energy, E_b is the activation energy, and E_s is the segregation (Gibb's free) energy.

Another phenomenon that should be taken into account is Coulomb repulsion. During in-situ doping, large numbers of Si-P or Ge-P heterodimers exist on the surface. When a Si or Ge atom is adsorbed on a surface phosphorus atom, the phosphorus atom becomes electrically active. A coulomb repulsive force is applied to the ionized and positively charged phosphorus atom by the other, previously incorporated positively charged phosphorus atoms in the deposited film. The coulomb repulsion energy, E_i^{coul} for an incorporated phosphorus atom at layer "i" is given by

$$E_i^{Coul} = \frac{q}{2\varepsilon} \sum_{j=1,2\ldots}^{i} \sigma_j \lambda_j \exp(-x_{ij}/\lambda_j), \tag{1.2}$$

where σ_j is the conductivity and λ_j is the screeening length at j^{th} plane defined as,

$$\lambda_j = \frac{2\pi\varepsilon \; \hbar^2}{m^* q^2} \left(\frac{1}{3}\pi\right)^{1/6} \left(n_j \frac{4\pi\varepsilon \; \hbar^2}{m^* q^2}\right)^{-1/6}, \tag{1.3}$$

where x_{ij} is the distance between "i" and "j" planes, $\varepsilon = \varepsilon_0$ x 11.8 for Si, m^* is the effective mass, and n_j is the carrier density at layer j. By using a phosphorus box profile in the Si layer, $\lambda_1 = \lambda_2 = \ldots = \lambda_j$ and $\sigma_1 = \sigma_2 \ldots = \sigma_j$ are assumed in equations 1.2 and 1.3.
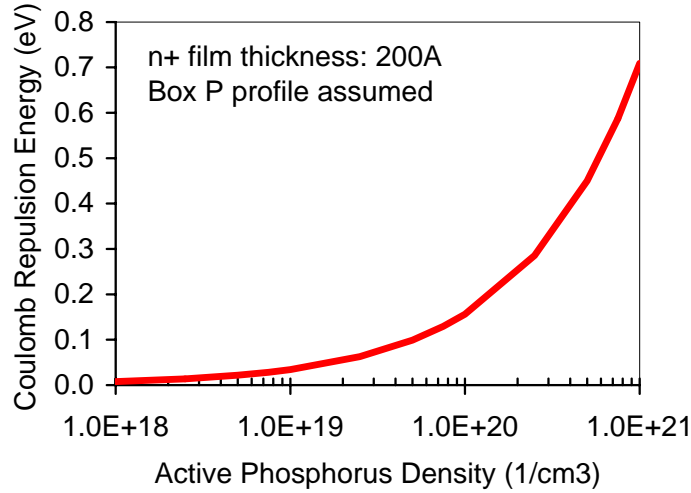
Figure I.15   Calculated coulomb repulsion energy plotted as a function of dopant density.
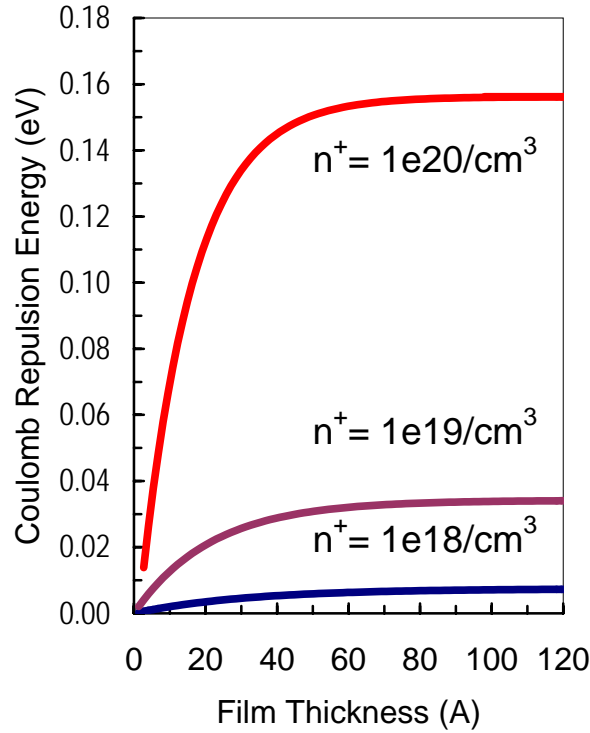
Figure I.16   Calculated coulomb repulsion energy plotted as a function of phosphorus doped film thickness

At $i = 150$ (total layer thickness ~ 200 Å), the calculated coulomb repulsion energy is shown in Figure I.15. It can be observed that as the doping level is increased, the repulsion energy increases exponentially. In Figure I.15, the Coulomb repulsion energy at $n = 1 \times 10^{21} cm^{-3}$ is around 0.71 eV, which is higher than the reported segregation energy resulting from the difference in bonding energies of Si-P and Si-Si. Figure I.16 shows the Coulomb repulsion as a function of the phosphorus doped film thickness. As shown, the accumulated repulsion energy sharply increases with thickness and levels off above a critical thickness due to charge screening. Consequently, the contribution of the repulsion

energy from an initial layer to the surface layer becomes negligible. In summary, the strong coulomb repulsion enhances phosphorus segregation, limiting phosphorus incorporation in the deposited layer.

Since segregation is a thermally activated process, deposition at very low temperatures (~ 250°C or less) can yield films with high phosphorus levels. Using Photo-CVD, a phosphorus level near 1 x 10^{21} cm-3 was obtained at 250°C [50]. Nützel and Abstreither observed that while segregation still exists at temperatures as low as 300°C segregation length begins to decrease exponentially at 500°C [49]. The segregation length was measured from the phosphorus tale in undoped Si layer, which was grown on a phosphorus covered Si surface. They also reported that antimony segregation lengths are 35, 18, 11 and 6nm for undoped Si growth rates of 0.36, 1.2, 3.6 and 12 nm/min, respectively. Thus, lower growth rates can result in enhanced segregation.

e)   Phosphorus Incorporation in $Si_{1-x}Ge_x$

By introducing germane to the deposition chemistry, phosphorus incorporation is greatly enhanced and the $Si_{1-x}Ge_x$ growth is not degraded as the phosphine flow is increased. Jang, Liao, and Reif reported an order of magnitude higher phosphorus incorporation and six times higher growth rate in $Si_{1-x}Ge_x$ with a Ge content of 20% [23]. They proposed that P-P dimerization is retarded by the presence of Ge ad-atoms on the surface. Since the Ge-P bond is weaker than the Si-P bond, phosphorus desorption is enhanced, which increases the number of available sites for adsorption and enhances the growth rate.

Enhanced phosphorus incorporation in $Si_{1-x}Ge_x$ may come from a higher density of monatomic phosphorus atoms on the surface, which results in retarded phosphorus segregation. As discussed before, P-P dimers are easily desorbed or segregated. Nützel et al reported that phosphorus segregation lengths are 300, 100, 40 and 4 nm in 0, 3, 7 and 20 % of Ge in $Si_{1-x}Ge_x$, respectively [52]. The films were grown at 490°C using MBE. For 20 % Ge in $Si_{1-x}Ge_x$, the segregation length is reduced by nearly two orders of magnitude. They proposed that reduced segregation comes from the competition between P and Ge atoms although the germanium segregation lengths are significantly lower than those of phosphorus. Unfortunately too much germane can also degrade phosphorus incorporation. Xie et.al. also reported that the presence of Ge surface atoms can degrade phosphorus incorporation due to the enhanced P desorption in the form of Ge-P heterodimers [28].

I.4 Deposition System Used in This Work

In this work, in-situ phosphorus doped Si and $Si_{1-x}Ge_x$ alloys were deposited in an Ultra-High Vacuum Rapid Thermal Chemical Vapor Deposition (UHV-RTCVD) reactor shown in Figure I.17. The system is capable of processing both 6" and 8" wafers. The system was designed and built at North Carolina State University. Construction of this system was accomplished as part of this thesis jointly with Dr. Nemanja Pesovic, who was also a graduate student in my research group. The system consists of three separate chambers: a load-lock (sample entry chamber), an intermediate chamber, and a main process chamber. The load lock is pumped by a dry molecular drag pump to a base pressure of 10^{-5} Torr. The intermediate chamber serves as a vacuum buffer between the

sample entry and main process chambers and it is pumped by a cryopump to a base pressure of 10^{-9} Torr. Another cryopump maintains a base pressure of 10^{-9} Torr in the main chamber. During growth, a turbomolecular/molecular-drag combination pump backed up by a dry mechanical pump is used. All pumps and gate valves on the system are oil-free to minimize hydrocarbon contamination. The main chamber is double walled (circulated with oil to heat up the chamber) stainless steel chamber with a quartz dome on top. Under the quartz dome, the seal consists of two o-rings with differential pumping between the O-rings by a small turbomolecular pump to maintain a pressure of $\sim 10^{-6}$ Torr. The wafer is heated through the quartz dome by tungsten-halogen lamps on top and around the dome. Two optical pyrometers ($\lambda = 4.9 - 5.3 \ \mu m$) focused at the edge and center of the wafer are used the measure the wafer temperature. The pyrometer focused at the wafer center is used in a closed-loop feedback control system. The wafer transfer mechanism was designed to load five wafers at a time. Figure I.18 is the detailed cross-sectional view of the main process chamber.
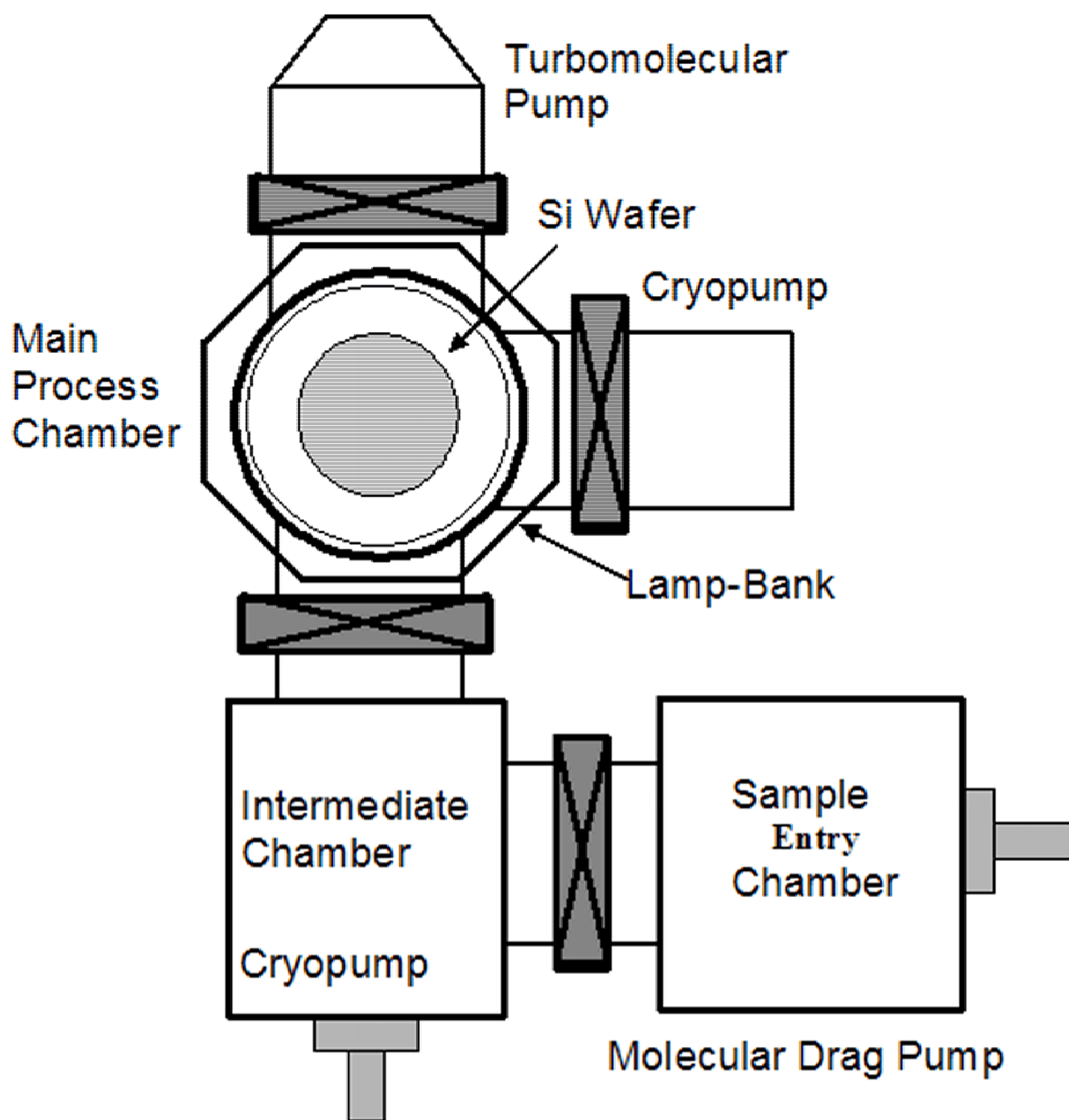
Figure I.17   Top view of the UHV-RTCVD System used in this work.
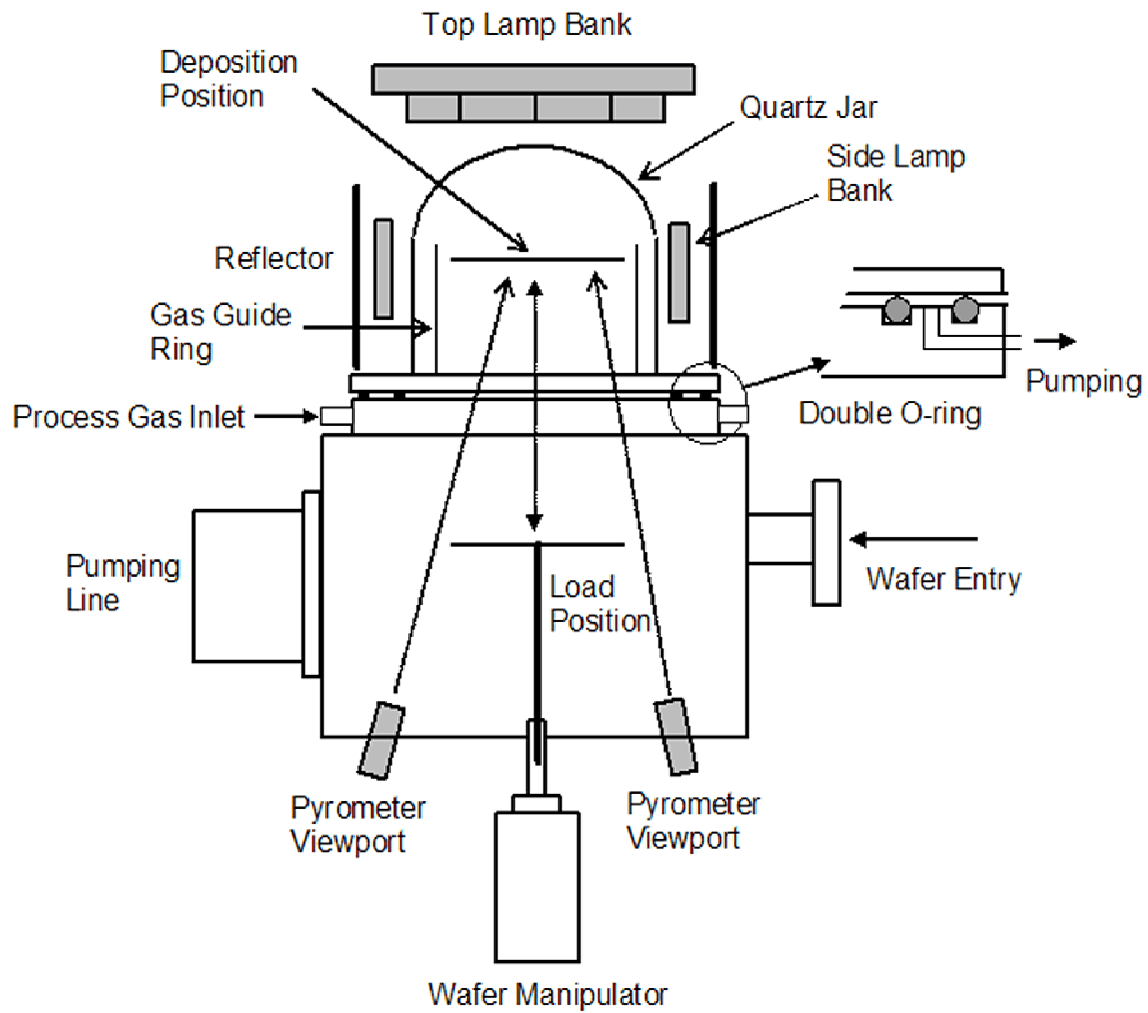
Figure I.18   Deposition Chamber of the UHV-RTCVD Chamber consists of a quart dome with lamps on top of and around the dome.

I.5   Surface Preparation Prior to Si$_{1-x}$Ge$_x$ Deposition

Wafers were cleaned *ex-situ* using a standard RCA clean (SC1/SC2). Immediately before loading into the system, the wafers were dipped in a 1 % HF solution for 30 seconds followed by a rinse in deionized water for 15 seconds. The purpose of the HF dip is to

remove protective oxide grown during RCA clean. In addition, hydrogen passivates the Si dangling bonds to protect against contamination.

After the HF dip, a wafer cassette containing five wafers is loaded into the load-lock. The procedure for transferring a wafer to the deposition chamber is as follows: Queue time before loading the wafer cassette into the vacuum chamber was $10 - 15$ min. After reaching a pressure of 10^{-5} Torr in the load-lock, the wafer cassette is transferred into the intermediate chamber, which can be pumped down to 10^{-7} Torr in a few minutes by the cryopump. After reaching 10^{-8} Torr a single wafer from the cassette is transferred to the main chamber. The main chamber is first pumped by the cryopump. Upon reaching the base pressure a gate valve isolates the cryopump and the chamber is switched to the turbomolecular/molecular drag combination pump used to pump the process gasses.

An *in-situ* vacuum bake was performed at 800°C for 10-15 seconds to remove any residual oxygen and carbon on the wafer surface. Under ultra-high vacuum, it has been reported that 800ºC, 10 s is enough to reduce the oxygen below the SIMS detection level and the carbon level below $\sim 10^{18}$ cm^{-3} [53, 54]. Epitaxial growth is initiated by gas switching and terminated by both gas and temperature switching.

Gases used in this work were 100% Si_2H_6, 10% GeH_4 mixed with H_2, 1% PH_3 mixed with H_2, and 100% H_2.

I.6   Overview of Thesis

The experimental work carried out during the course of this research has been summarized in three chapters. Electrical and structural properties of the deposited layers can be found in Chapter II. In these experiments, Hall Effect measurements were heavily relied on to determine the active carrier concentration in the grown layers as well as film resistivity and carrier mobility. Chapter III provides a detailed account of the properties of diodes fabricated using the in-situ doped layers. The emphasis in Chapter III is on the reverse leakage current and different mechanisms that contribute to the overall junction leakage. Chapter IV focuses on selective deposition and methods to improve the process selectivity.

I.7   References

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II Deposition of In-situ Phosphorus Doped Silicon-Germanium Alloys

Ban's results on phosphorus incorporation reviewed in Chapter I are typical of in-situ phosphorus doped Si epitaxial layers [1]. While in-situ doped polycrystalline layers deposited at higher temperatures can reach phosphorus levels in excess of 10^{20} cm^{-3}, epitaxial layers are in general limited to concentration levels below this regime. Fortunately, higher phosphorus levels can be obtained in $Si_{1-x}Ge_x$ alloys as discussed in Chapter I. This chapter examines in-situ P doped Si and $Si_{1-x}Ge_x$ growth by UHV-RTCVD. The Si and $Si_{1-x}Ge_x$ films were characterized by atomic force microscopy (AFM), secondary ion mass spectroscopy (SIMS), X-ray diffraction (XRD), and Hall-Effect measurements. In this work, we have used high resistivity (8-10 ohm-cm) and low resistivity (0.02 - 0.013 ohm-cm), 150 mm, p-type (100) silicon wafers.

II.1 Phosphorus Incorporation in $Si_{1-x}Ge_x$

Figure II.1 shows typical phosphorus profiles obtained in this work in heavily doped Si and Si-Ge epitaxial films. The phosphorus profiles "A" and "B" were obtained from $Si_{1-x}Ge_x$ layers grown at 800^oC and 720^oC respectively. For comparison, C and D are from Si layers grown at the same temperatures. The detailed growth conditions for these samples and others prepared in this study are summarized in Table 2.1. As shown, addition of GeH_4 to the Si_2H_6-PH_3 chemistry provides a significant enhancement in phosphorus

incorporation. This is in agreement with previous work summarized in Chapter 1 [2 – 6].
As discussed , the presence of germanium retards P-P dimerization increasing the
phosphorus concentration on the growth surface. Phosphorus can exist in the form of Si-P
and Ge-P heterodimers.

A and B are Si-Ge grown
at 800 and 720°C.
C and D are Si grown at
800 and 720°C.
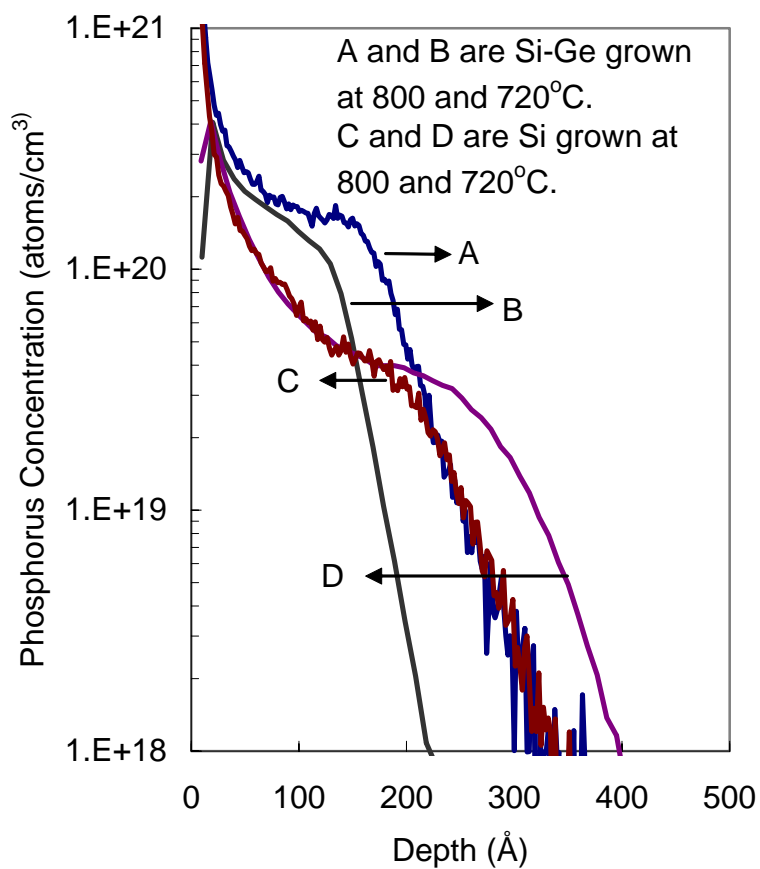
Figure II.1   Phosphorus profiles of Si and $Si_{1-x}Ge_x$ films obtained by SIMS.

Table 2.1   Deposition conditions used in the experiment to study the effects of temperature and GeH_4/Si_2H_6 ratio on growth rate and film properties.

Samples	T (^{o}C)	1% PH_3 (sccm)	100% Si_2H_6 (sccm)	8% GeH_4 (sccm)	H_2 (sccm)	Total Pressure (mtorr)
A	810	200	10	37.5	0	100
B	720	200	10	37.5	0	100
C	810	200	12	0	35	100
D	720	200	12	0	35	100
E	830 - 670	140	14	0	0	43
F	830 - 670	140	12	37.5	0	74
G	830 - 670	140	8	50	0	80

As discussed in Chapter 1, phosphorus atoms adsorbed on the Si surface form P-P dimers and desorb readily. Increasing the phosphine flow increases the density of adsorbed phosphorus atoms, which in turn enhances P-P dimerization and subsequent desorption. This is one of the reasons why increasing the partial pressure of phosphine does not result in a proportionate increase in phosphorus concentration. It has also been mentioned in Chapter 1 that phosphorus has a tendency to segregate to the surface during growth, which is responsible for the surface peak observed in Figure II.1. Surface segregation makes it more difficult to reach high concentrations in the $Si_{1-x}Ge_x$ layer. Nevertheless, as shown in Figure II.1, the phosphorus concentration in both $Si_{1-x}Ge_x$ layers is above 10^{20} cm^{-3}. The surface segregation may actually be helpful by providing a large amount of phosphorus to the metal - $Si_{1-x}Ge_x$ interface, which is a key requirement for achieving low contact resistivity.

II.2 Growth Rate
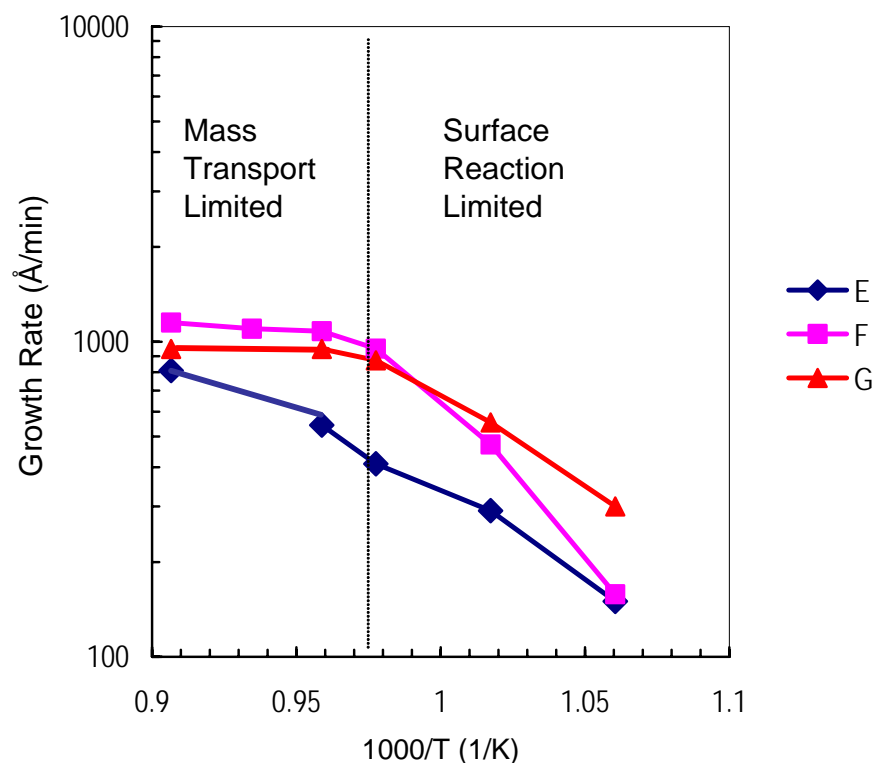
Figure II.2 Si and $Si_{1-x}Ge_x$ growth rate with respect to inverse temperature.

Shown in Figure II.2 is the growth rate plotted as a function of inverse temperature obtained from samples E - G whose deposition conditions are given in Table 2.1. For the sample set E, one can conclude that the silicon growth rate is increasing with temperature in the entire temperature range considered. A straight line fit to sample set E yields an activation energy of ~18 kcal/ mol which is much lower than the reported activation energies for hydrogen and P-P dimer desorption (47 kcal/ mol and 200 kCal/ mol

respectively) [7]. On the other hand for sample sets F and G, the $Si_{1-x}Ge_x$ growth rate appears to saturate above T ~ 750°C indicative of mass transport limited growth. Below this temperature, the growth rate drops exponentially with temperature indicative of surface reaction limited growth. However, the number of data points is not sufficient to conclude if the growth is entirely controlled by the surface reactions. It is possible that a large portion of the temperature range includes the transition region between the two regimes and the growth rate may very well be limited by both mechanisms. Another complication arises from the fact that the Ge content of the epitaxial layers in Figure II.2 is also affected by the growth temperature. At lower temperatures, GeH_4 can decompose more readily than Si_2H_6.

Table 2.2   Deposition conditions used in the experiment to study the effects of temperature and phosphine flow rate on growth rate and film properties. Same samples are also used to study resistivity, mobility and active carrier concentration.

Samples	T (°C)	1% PH_3 (sccm)	100% Si_2H_6 (sccm)	8% GeH_4 (sccm)	H_2 (sccm)	Total Pressure (mtorr)
A	810	20 - 200	16	50		
B	760	20 - 200	13.6	83.7		
C	760	20 - 200	10	125	variable	140
D	720	20 - 200	13.6	83.7		
E	720	20 - 200	10	125		

Consequently, the Ge content is expected to increase as the temperature is reduced.

Shown in Figure II.3 is the growth rate as a function of the phosphine flow. The deposition parameters are included in Table 2.2. As expected, $Si_{1-x}Ge_x$ growth rate decreases as the PH_3 flow increases in the temperature range considered. At 810°C, the growth rate decreases from 120 nm/min to 60 nm/min corresponding to a reduction of ~

50%. At 720°C, the reduction is more than 75%. It is interesting to note that at 760°C for the highest GeH_4/Si_2H_6 ratio of 1/1, PH_3 has a lesser impact on growth rate. However, variations in system conditions and/or measurement errors may be responsible for this behavior. Nevertheless, the general conclusion remains the same: PH_3 can significantly reduce the growth rate. The impact of temperature is also clear. A significant enhancement in growth rate is obtained by raising temperature from 720°C to 810°C. This is especially evident for higher PH_3 flows, which can be attributed to passivation of the surface adsorption sites at lower temperatures. It is interesting to note that 760°C is close to the temperature needed for P_2 desorption originating from P-P migrating mono-dimers in Figure I. [8]. P desorption from the Si-P hetero-dimers require ~ 850°C, hence, its contribution to P desorption should be small.

II.3   Resistivity, Mobility and Carrier Concentration

Numerous samples were grown in the course of this study to determine the optimum growth conditions to maximize phosphorus incorporation in $Si_{1-x}Ge_x$ layers. Samples were grown to study factors including temperature, gas flows, total pressure and film thickness. Because of these repetitive experiments and the large number of samples, it was not possible to employ Secondary Ion Mass Spectroscopy (SIMS) to analyze the samples due to high costs involved. As a partial solution, we have used Hall Effect measurements to study phosphorus incorporation in epitaxial layers. A 1000 Å thick thermal oxide layer on the silicon wafers was patterned by photolithography and wet etching to define active areas for clover shaped Van der Pauw structures.
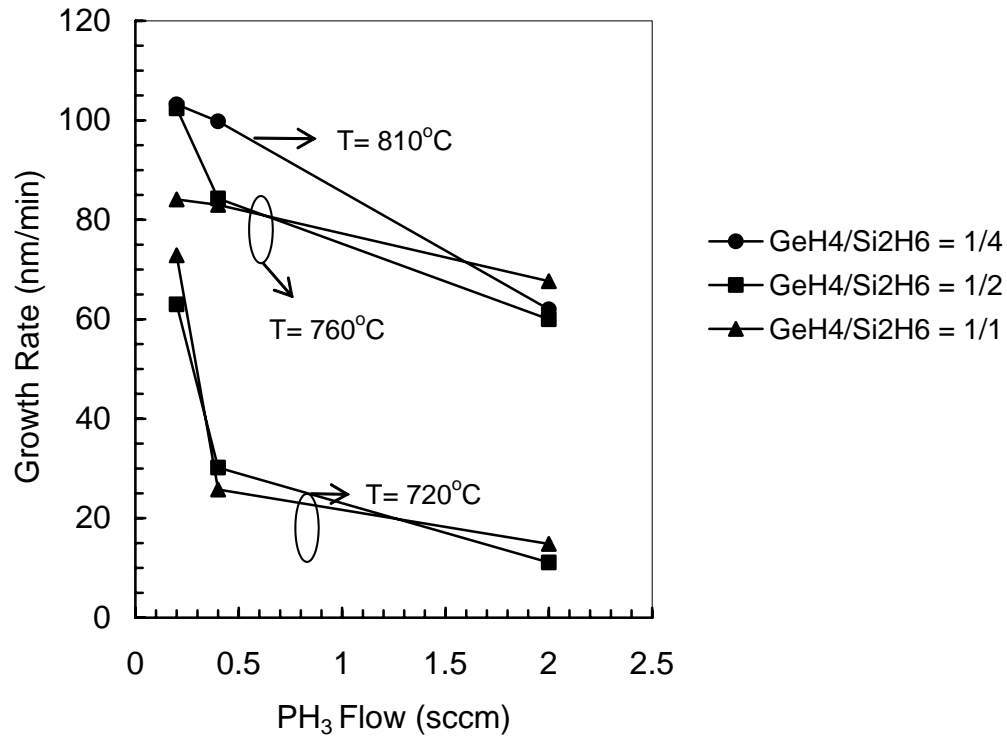
Figure II.3 $Si_{1-x}Ge_x$ growth rate as a function of PH_3 flow at various temperatures.

The Hall Effect measurement suffers from several sources of error in determining the phosphorus incorporation. First, as shown in Figure II.1 due to phosphorus segregation at the growth surface it is not possible to obtain a uniform phosphorus concentration in the grown layers. Thus, the active phosphorus level obtained from this type of measurement can only represent an average concentration. Furthermore, this corresponds to the average value of the *active* phosphorus distribution, which is expected to be varying with depth as suggested by the SIMS profiles shown in Figure II.1. Finally, in extracting the active phosphorus concentration, we assume a Hall scattering factor of unity for all grown layers,

which is most likely not true. The importance of Hall coefficient on the extraction process can be explained as follows: The expression for electron concentration is given by [9],

$$n = -\frac{r}{qR_H},$$

where r is the Hall scattering factor and R_H is the Hall coefficient. Several reports have been published on application of Hall Effects measurements to $Si_{1-x}Ge_x$. These reports have shown that the coefficient can vary greatly depending on the Ge concentration and the doping level and have values as low as 0.5 [10, 11]. Therefore, measurements of the active carrier concentration can only provide an approximate guide unless the Hall factor is known.

Table 2.3   Detailed growth conditions used in the experiment to study the effects of temperature and GeH_4/Si_2H_6 flow ratio on resistivity, mobility and carrier concentration using Hall Effect measurements.

Samples	T (^{o}C)	1% PH_3 (sccm)	100% Si_2H_6 (sccm)	8% GeH_4 (sccm)	H_2 (sccm)	Total Pressure (mtorr)
A			20	0		
B			16	50		
C	670 - 810	40	13.6	83.7	variable	140
D			10	125		
E			6.7	170		

In the first experiment, the phosphine level was kept constant as we changed the Si_2H_6 and GeH_4 flows. The PH_3 flow was kept constant at 40 sccm (including H_2 used for dilution) for all samples. Si and Ge precursors were 100% Si_2H_6 and 8% GeH_4 diluted in

H$_2$. Experimental conditions are summarized in Table 2.3. For each sample set (A - E), the hydrogen flow rate was adjusted to bring the total pressure to 140 mtorr.
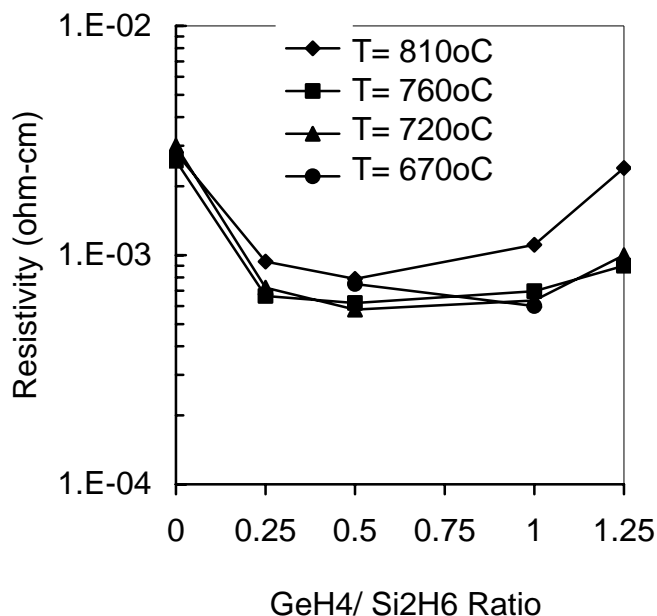
Figure II.4 Resistivity as a function of GeH$_4$/ Si$_2$H$_6$ flow ratio at various temperatures.

Resistivity of the deposited films is shown in Figure II.4. A resistivity minimum is observed at around the GeH$_4$/ Si$_2$H$_6$ flow ratio of ~ 0.5. The minimum resistivity obtained in Figure 2.4 is ~ 6 x 10^{-4} Ω-cm. There appears to be a weak dependence of resistivity on temperature. It is important to note that the film composition is determined by both the gas flow ratio and the deposition temperature. At lower temperatures the Ge composition is expected to be somewhat higher since GeH$_4$ decomposes at surface temperatures as low as 400ºC, while this is not true for Si$_2$H$_6$. As such, the resistivity minimum shifts from lower

Ge compositions to higher as the deposition temperature is raised.
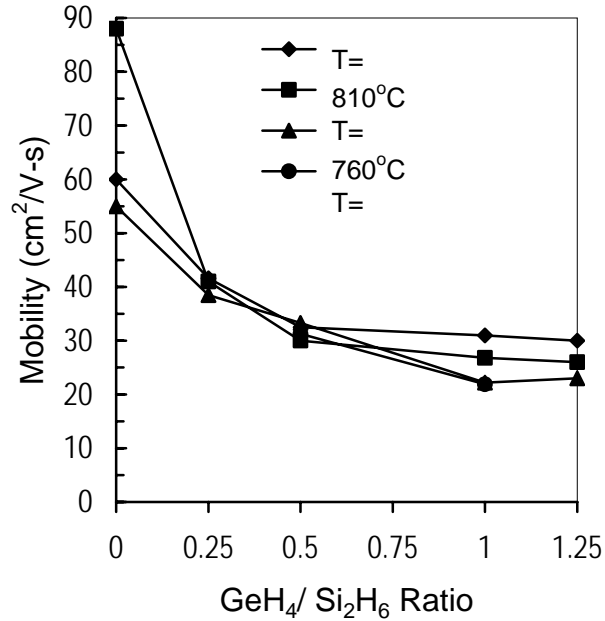
Figure II.5   Mobility as a function of GeH$_4$/ Si$_2$H$_6$ flow ratio at various temperatures.

Shown in Figure II.5 is the carrier mobility as a function of the GeH$_4$/ Si$_2$H$_6$ ratio. It can be seen that the mobility drops rather quickly as we move further away from the pure Ge case as expected. However, this reduction significantly slows down around a GeH$_4$/ Si$_2$H$_6$ ratio of 0.5 and levels off around 30 cm^2/ V-s, which is typical for heavily doped n-type Si.
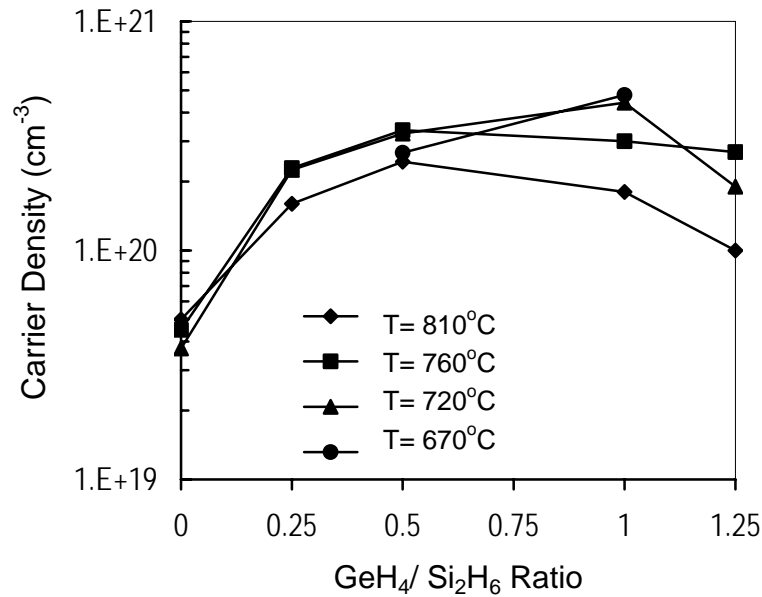
Figure II.6   Electrically active carrier density as a function of GeH$_4$/ Si$_2$H$_6$ flow ratio at various temperatures.

From resistivity and mobility values determined above, active carrier concentration in the deposited layers can be calculated. Shown in Figure II.6 is the active carrier concentration as a function of GeH$_4$ to Si$_2$H$_6$ flow. As shown, the active carrier concentration is enhanced as the GeH$_4$/Si$_2$H$_6$ ratio is increased. However, as the ratio is further increased, a maximum concentration is reached after which the phosphorus incorporation begins to decrease. The ratio where the maximum incorporation shifts to higher GeH$_4$/Si$_2$H$_6$ ratios as the deposition temperature is decreased. Clearly, this behavior requires optimization of the GeH$_4$ flow relative to the Si$_2$H$_6$ flow for each temperature. The highest active carrier concentrations in Figure II.6 are 2.3, 3.4, 4.4 and 4.8 X 10^{20} cm^{-3} at

810°C, 760°C, 720°C, and 670°C, respectively. Due to reasons mentioned above, these values can only serve as a guide. The reduction in mobility with GeH_4/Si_2H_6 ratio can be attributed to alloy scattering coupled with ionized impurity scattering since phosphorus level also increases with this ratio.

As discussed above, both Hall mobility and carrier concentration measurements rely on the knowledge of the Hall scattering coefficient. Since this coefficient is not available for films with varying concentrations of germanium and phosphorus, errors in measured values should be expected. However, the resistivity measurement does not depend on the Hall coefficient and it can be used as a reliable parameter to compare different $Si_{1-x}Ge_x$ films.

In a second experiment, the effects of phosphine flow on electrical properties of the films were examined. The same samples were used to determine the growth rate in the previous section and the deposition conditions can be found in Table 2.2.

Shown in Figure II.7, is film resistivity plotted as a function of PH_3 flow rate at 720°C and 760°C. An interesting behavior is observed. At 760°C, the resistivity first drops with PH_3 addition and then levels off at around 0.2 sccm. At 720°C, resistivity begins to increase rapidly beyond 0.2 sccm, this behavior is observed for two different GeH_4/Si_2H_6 flow ratios of 0.25 and 1.0.
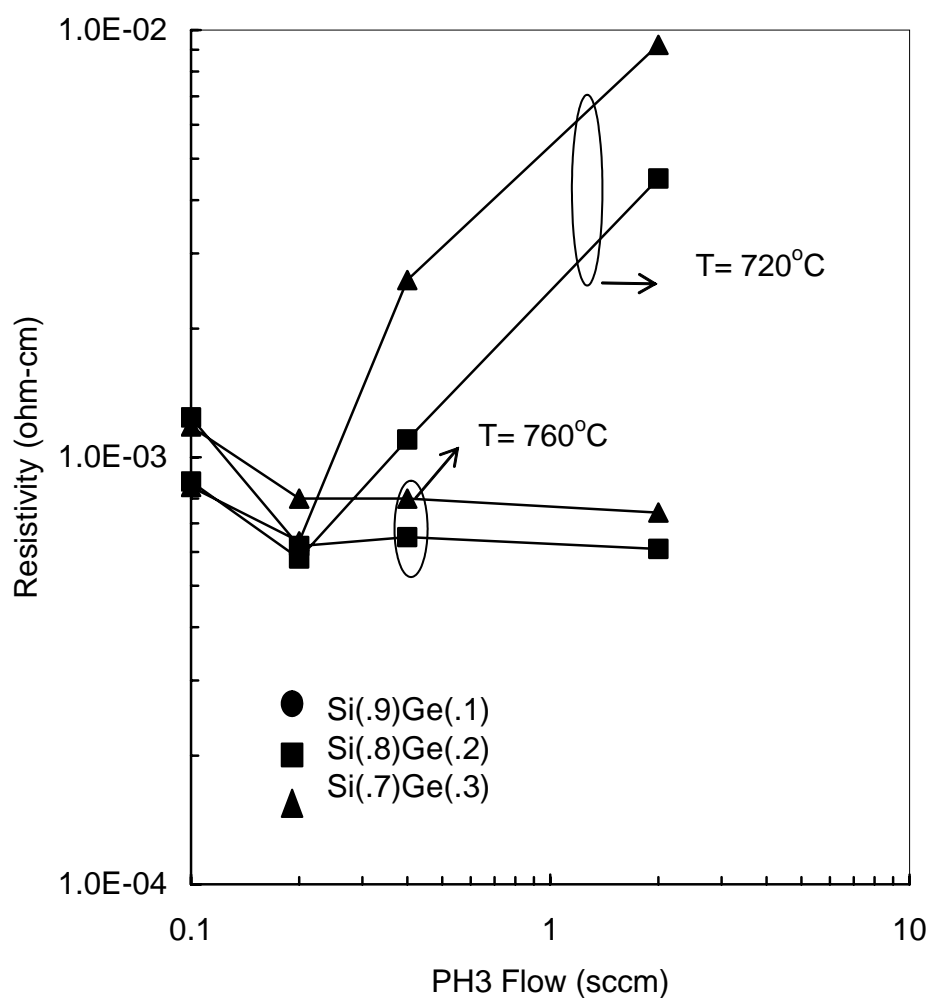
Figure II.7   Resistivity as a function of PH$_3$ flow.

Figure II.8 shows variations in film mobility with deposition conditions. Initially, mobility appears to drop with PH$_3$ and levels off at around 0.2 – 0.4 sccm of PH$_3$. At both temperatures, higher mobility is obtained for the lower GeH$_4$/Si$_2$H$_6$, which may be due to increased alloy scattering. At the same time, GeH$_4$ addition impacts phosphorus incorporation, which will impact the amount of ionized impurity scattering. The rapid

increase in resistivity observed at 720°C cannot be explained based on the variations in mobility suggestive of large changes in active carrier concentration at 720°C.
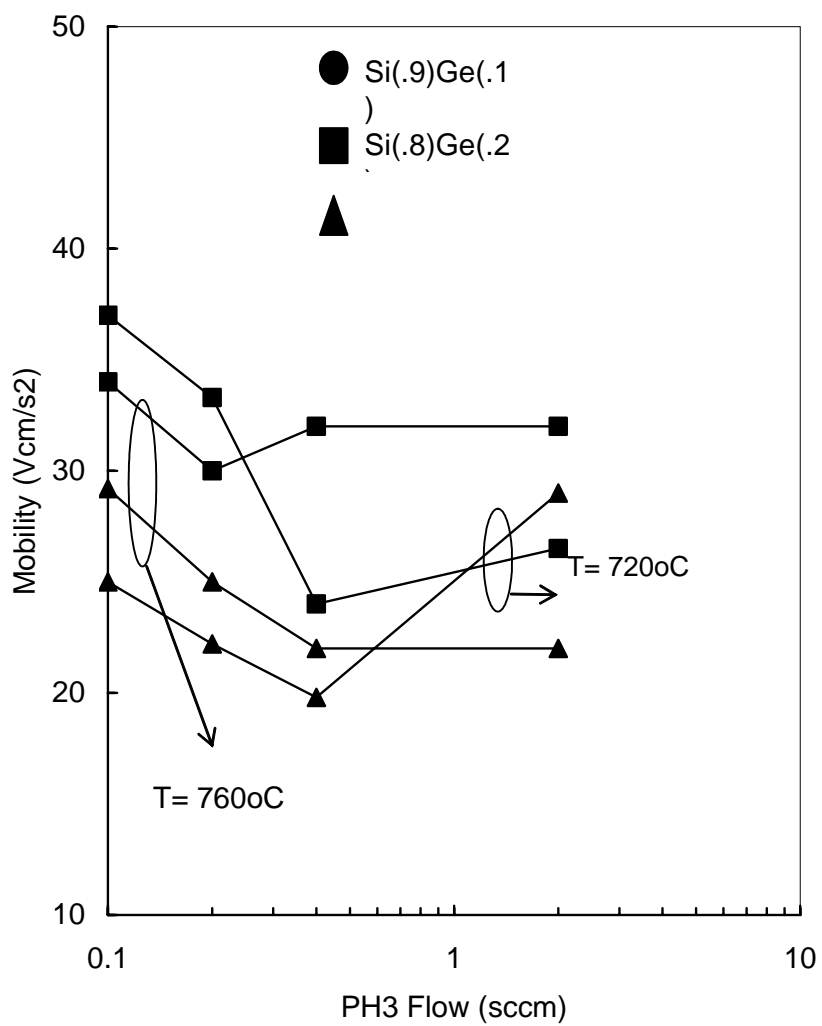
Figure II.8 $Si_{1-x}Ge_x$ mobility as a function of the PH_3 flow.

Shown in Figure II.9 is active carrier concentration as a function of the PH_3 flow at these growth temperatures of 720, 760 and 810°C. It can be seen that at 760°C, the phosphorus concentration is gradually increasing with increasing PH_3 flow for flow rates between 0.1 and 0.5 sccm. At higher PH_3 flows, phosphorus concentration is constant and it is independent of the flow rate. At 810°C, a quite similar behavior is observed. The active carrier concentration is slightly below the level achieved at 760°C; however, several factors such as diffusion of phosphorus may affect the average level obtained by the measurement. At 720°C, phosphorus incorporation drops with increasing PH_3 flow exhibiting a behavior similar to the growth rate. As discussed in Chapter 1, phosphorus segregation is closely related to phosphorus incorporation. In the two state model (TSM), impurity atoms at the sub-surface continuously exchange their positions with adsorbed Si atoms until the sub-surface becomes the third layer with adsorption of another layer [12]. A lower growth rate can provide more time for phosphorus atoms at sub-surface to segregate, which results in a lower phosphorus incorporation. As the growth rate is reduced, increased segregation length of n-type dopant was observed by Nützel and Abstreither [13]. Since P-P dimer desorption cannot occur effectively at 720°C, they block available adsorption sites, resulting in the severe growth rate reduction.

Figure II.9   Active phosphorus density as a function of PH_3 flow at various temperatures.

II.4 Attempts to Increase the Phosphorus Incorporation

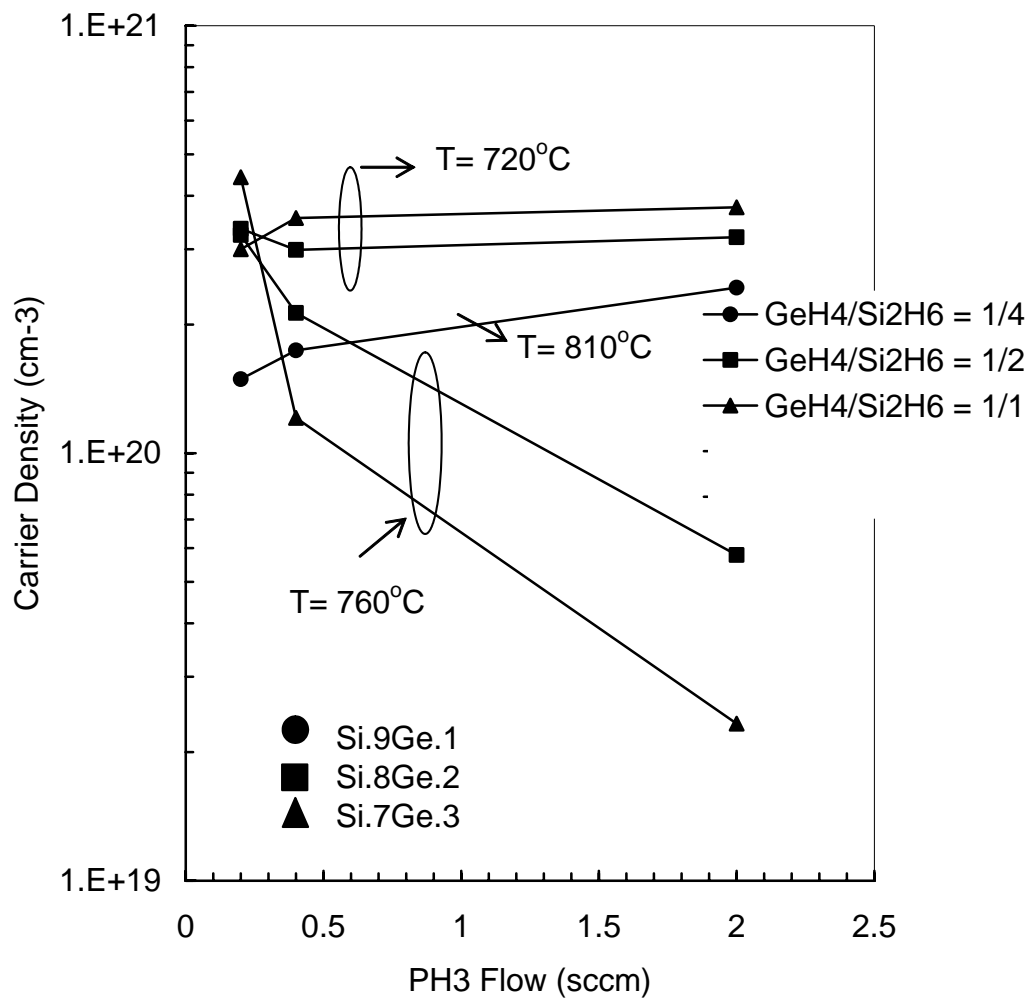We have shown that phosphorus incorporation can be greatly enhanced by adding GeH_4 to the Si_2H_6 and PH_3 chemistry. However, phosphorus segregation at the surface is

still evident. In MBE growth, Sb has been used to decrease the surface energy of the growing Ge or $Si_{-x}Ge_x$ film on a Si wafer to suppress three dimensional growth or islanding [14, 15]. Similar to phosphorus, Sb has a tendency to diffuse to the surface. It has been reported that hydrogen can also play a similar role [16]. The method relies on passivating the surface reducing the need for the Sb atoms at the surface. P.E. Thompson et.al. has reported that atomic hydrogen can enhance Sb incorporation in Si by greater than two orders of magnitude [17, 18]. They deposited Sb doped Si layers using elemental Si and Sb at $500^{\circ}C$, 5×10^{-7} Pa without H_2. While maintaining Si and Sb flow, H_2 was introduced to the growth chamber. The deposition pressures were 1×10^{-4} and 5×10^{-3} Pa. Incorporated Sb concentrations using SIMS were around 1×10^{17} (SIMS background level) without H_2, 1×10^{18} at 1×10^{-4} Pa, and 1×10^{19} Pa at 1×10^{-3} Pa. By comparing segregation ratio between doping profile with and without hydrogen, it is shown that H_2 could reduce surface segregation ratio of Sb by nearly two orders of magnitude.

We have tried two similar approaches with the hope of enhancing the phosphorus incorporation in $Si_{1-x}Ge_x$. H_2 was added to reduce the surface energy to discourage the phosphorus atoms from diffusing to the surface. The second approach involved addition of B_2H_6 to reduce the Coulomb repulsion energy arising from the ionized phosphorus atoms in the film.

In these experiments, we have used high resistivity (8-10 ohm-cm) and low resistivity (0.02 - 0.013 ohm-cm), 150 mm, p-type (100) silicon wafers. A 1000Å thick thermal oxide was grown and patterned by photolithography and wet etching to define

active areas for clover shaped Van der Pauw structures.
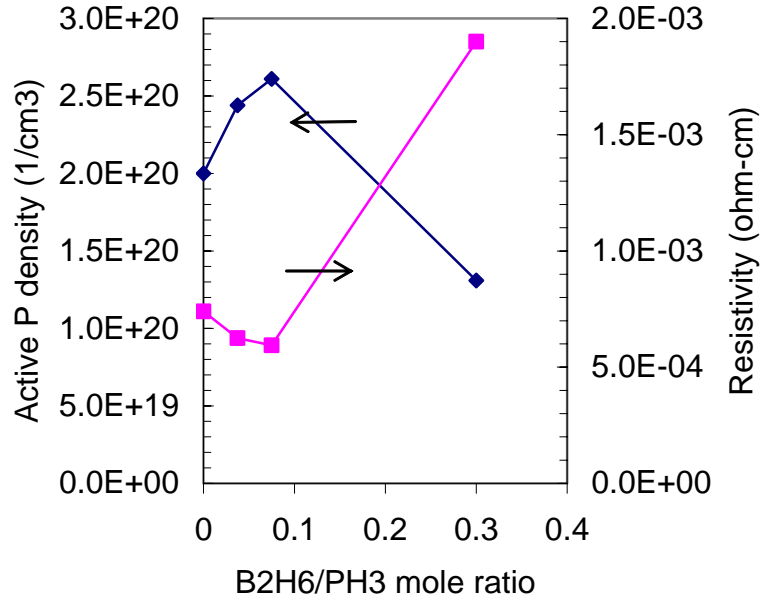
Figure II.10   Active P-density and resistivity as a function of the B_2H_6/ PH_3 mole ratio.

a)   Effects of B_2H_6 on Phosphorus Incorporation

In order to relax the Coulombic repulsion energy, B_2H_6 is added to the Si_2H_6 – GeH_4 – PH_3 chemistry. Figure II.10 and Figure II.12 show active carrier density, resistivity mobility and RMS roughness of these films. As shown, the active phosphorus level only increases from 2 x 10^{20} to 2.6 x $10^{20}cm^{-3}$ with a B_2H_6/ PH_3 mole ratio of 0.075. Then, the active P level decreases to 1.3 x $10^{20}cm^{-3}$ at 0.3 B_2H_6/ PH_3 mole ratio, which may be due to excessive boron incorporation compensating the P level in the film. In these experiments, $Si_{1-x}Ge_x$ layers became p-type at a mole ratio of 0.5 B_2H_6/ PH_3. In Figure II.12, electron

mobility is around 40 V-cm/sec below a B_2H_6/ PH_3 mole ratio of 0.1 and it drops down to

28.3 V-cm/sec at 0.3 B_2H_6/ PH_3 mole ratio due to high impurity scattering.
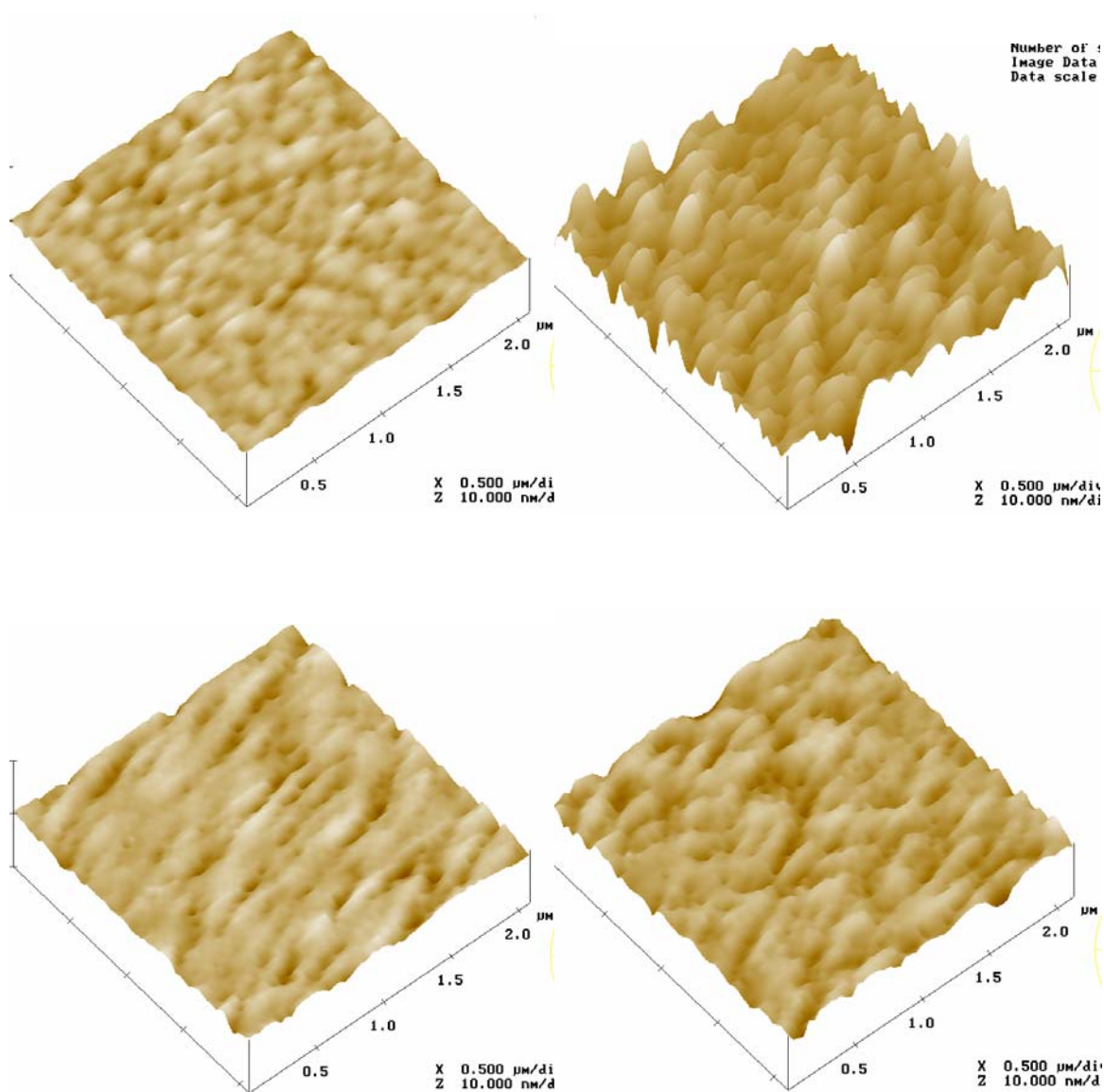
Figure II.11   AFM micrographs of $Si_{1-x}Ge_x$ layers grown with B_2H_6 flows of (a) 0 sccm, (b) 1 sccm, (c) 2 sccm, and (d) 10 sccm of.
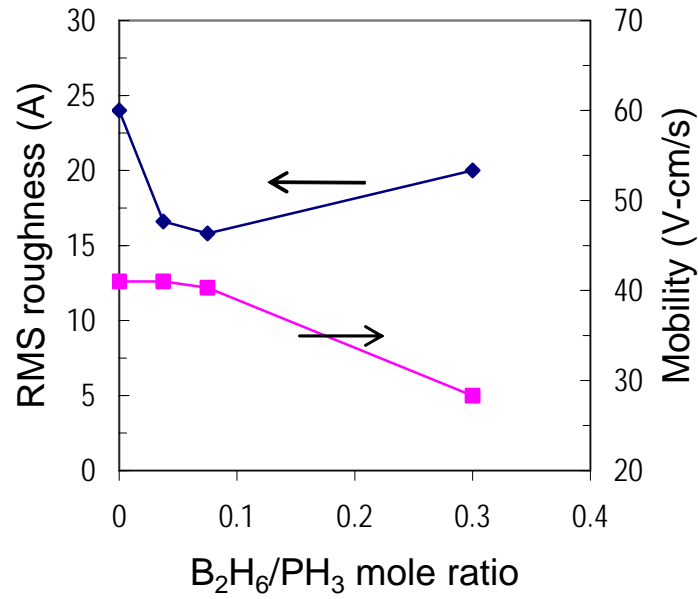
Figure II.12 RMS roughness and mobility as a function of B$_2$H$_6$/ PH$_3$ mole ratio.

As shown in Figure II.11 and Figure II.12, diborane addition also impacts the surface morphology. It is interesting to note that the films are smoother when the carrier mobility is high. This behavior indicates that the surface roughness is linked to structural changes in the film which affect the carrier mobility.

b) Effects of H$_2$ on Phosphorus Incorporation

With Hydrogen, segregation probability can be expressed as

$$P^{eff} = \exp\left(-E_s^{eff}/kT\right) = \frac{P}{1-\theta_H} \qquad (3.5)$$

where P is the probability without H_2, θ_H is the hydrogen coverage on the surface and E_s^{eff} is effective segregation energy with hydrogen where $E_s^{eff} \langle E_s$. By comparing Equations 3.1 and 3.5, one can easily see that addition of hydrogen reduces the segregation probability, which should reduce the phosphorus segregation. Based on this hypothesis, we have carried out experiments with different hydrogen levels. Unfortunately, due to the limitations of the system, we were limited to hydrogen flow rates of $200-800$ sccm.
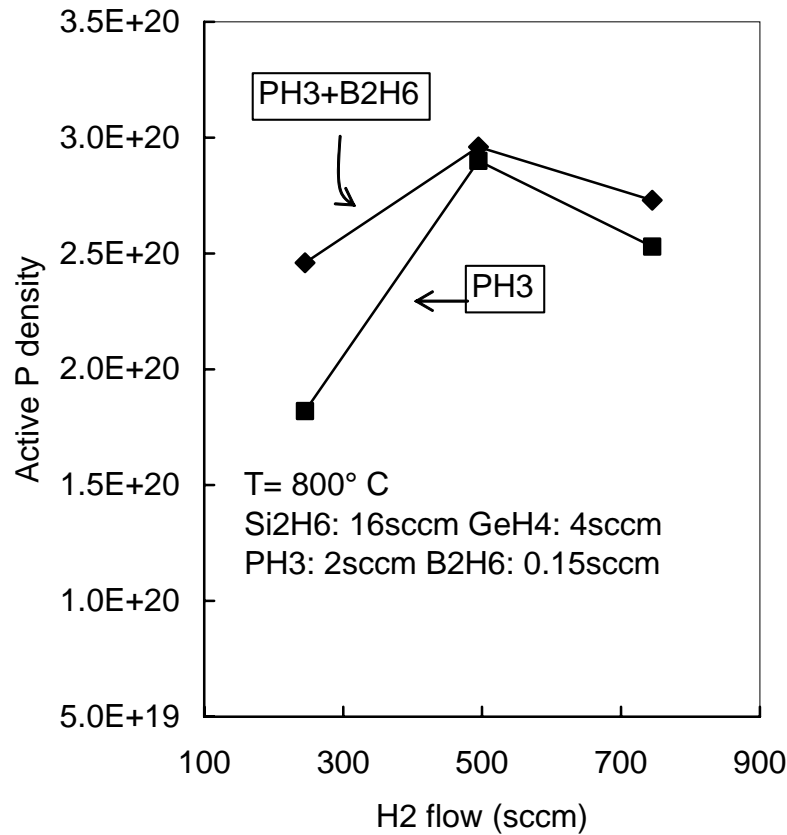
Figure II.13   Electrically active carrier density as a function of H_2 flow.
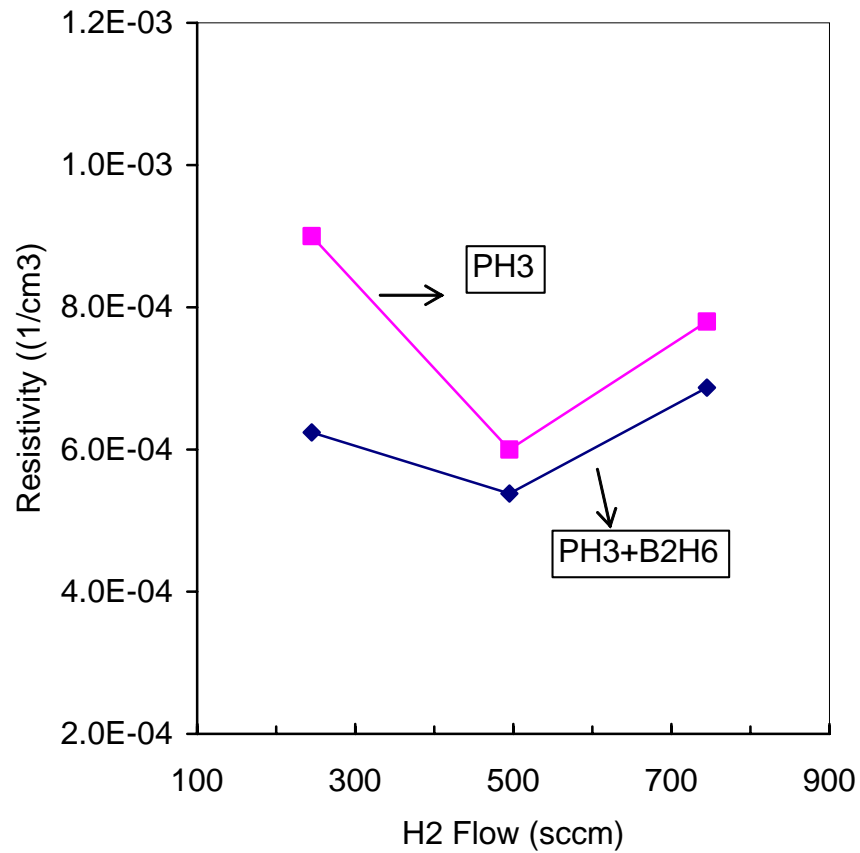
Figure II.14   Resistivity as a function of H_2 flow with and without B_2H_6.

Figure II.13 and Figure II.14 show active phosphorus density and resistivity as a function of the H_2 flow, respectively. We see that the P incorporation is somewhat enhanced as the H_2 flow is increased from 250 sccm to 495 sccm. However, the phosphorus level drops back to a lower level when the hydrogen flow is further increased. The added B_2H_6 also increases the phosphorus incorporation further. As shown in Figure II.14, at 500 sccm of hydrogen flow and with a small amount of B_2H_6 (0.15 sccm), the lowest resistivity, 5.38×10^{-4} cm^{-3} of this work has been accomplished.

The above results indicate that phosphorus incorporation can be somewhat improved by adding of H_2 and B_2H_6 to the deposition chemistry. However, the variations appear to have an effect within a factor of two of the original phosphorus concentration. It should be noted however that these experiments were carried out at 800°C. Since the H_2 desorption from Si can take place at much lower temperatures, it is possible that the impact of H_2 can be much more pronounced at lower temperatures. As shown in Figure II.9, the active carrier concentration is highest at 720°C and it is already at $\sim 3x10^{20}$ cm^{-3}. Therefore, it is plausible that if H_2 is added to the chemistry at this temperature a more pronounced effect could be observed.

It is clear that is room for future work in understanding the deposition chemistry better to find ways to increase the phosphorus incorporation. The results from the experiments presented in this chapter indicate that there exists an optimum GeH_4/Si_2H_6 flow ratio and it corresponds to a Ge concentration of approximately 20 %. At the same time, temperature plays a key role. To enhance phosphorus incorporation, the films must be grown the lowest possible temperature to minimize phosphorus diffusion and segregation. Additions of H_2 and B_2H_6 may further improve the enhancement even though their impact on phosphorus incorporation was minimal in our experiments. However, in these experiments, we did not have the chance to try these additions for different gas flow ratios and temperatures, hence, the results cannot be considered conclusive.

II.5 References

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III Electrical Characterization of PN Junctions Formed Using In-situ Phosphorus Doped Si$_{1-x}$Ge$_x$

The focus of this chapter is electrical properties of n$^+$-p junctions fabricated using in-situ doped Si$_{1-x}$Ge$_x$ alloys onto p-type Si substrates. Electrical characterization was achieved using reverse bias I-V and C-V measurements.
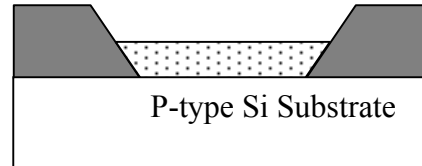
III.1 Diode Fabrication

Shown in Figure III.1 are the critical fabrication steps used in fabrication of the junctions and the schematic view of a gated diode. Two different wafer sets were used with background doping densities of $N_A = 1.0$ x 10^{15}/cm^3 and 5.0 x 10^{18}/cm^3. A 100 nm thermal oxide was grown in a batch furnace. Photolithography and wet etching in 10% dilute HF were used to define the active areas in the oxide. The junction active areas were 300 x 300 μm^2, 500 x 500 μm^2, and 800 x 800 μm^2. Si$_{1-x}$Ge$_x$ layers were deposited in the active areas selectively by UHV-RTCVD following the procedures discussed in the previous chapter. LPCVD was used to deposit a 300 nm thick oxide layer. Photolithography and wet etching in 1% dilute HF was used to open the contact holes in the deposited oxide. Evaporation was used to deposit 50 nm thick Ti as a barrier metal and 400 nm thick Al as the contact metal. Metal pads were defined by wet etching the Al/Ti stack.

- Wafer Scribe/ RCA clean/ 100 nm thick thermal oxide
- Active Mask – 1st Mask / Oxide etch
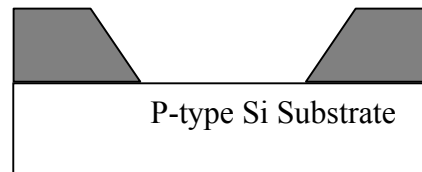
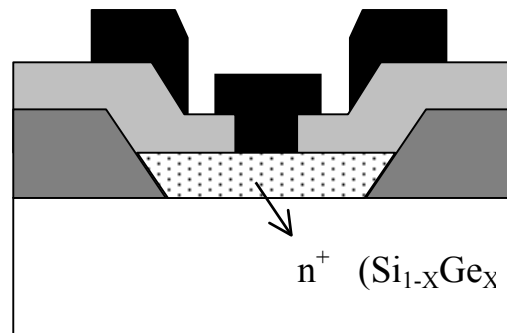- RCA clean/ Selective Si or $Si_{1-x}Ge_x$ growth

- LPCVD Oxide deposition
- Contact Mask – 2nd Mask / Oxide etch
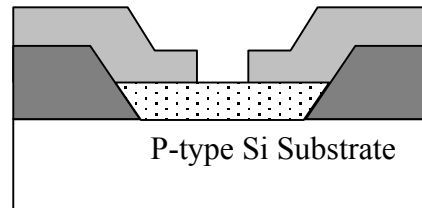
- Ti/Al deposition
- Metal Mask – 3rd Mask / Al/Ti etch

n^+ $(Si_{1-x}Ge_X$

Active Area:

300 x 300 μm^2

500 x 500 μm^2

800 x 800 μm^2
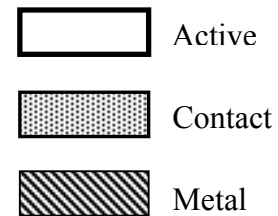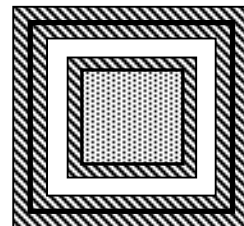
Active

Contact

Metal

Figure III.1   Diode Fabrication Steps

III.2 Leakage Current

a) Junctions Fabricated on Lightly Doped Substrates

Figure III.2 shows a typical gated diode leakage versus gate bias plot for junctions fabricated on lightly doped substrates. The junction was reverse biased at 1.0 V. As shown, the leakage current exhibits two distinct regions. At large positive biases, the p- type region surrounding the junction is depleted and a high leakage current is induced due to generation of carriers in the depletion region under the oxide [1]. It is noted that the positive oxide charge can deplete the lightly doped Si substrate even at zero bias. As the gate bias becomes more negative, the Si surface under the gate enters accumulation and the leakage current is reduced significantly.

Junction leakage current (I_{tot}) can be modeled as the sum of areal and peripheral leakage currents:

$$I_{tot} = J_a A + J_p P \tag{3.1}$$

where J_a is the areal leakage current density, J_p is the peripheral leakage current density, A is the junction area, and P is the perimeter. Dividing each side of the equation (3.1) by A or P yields:

$$I_{tot} / P \left(ampere / \mu m \right) = J_a (A/P) + J_p, \tag{3.2}$$

and

$$I_{tot} / A \left(ampere / \mu m^2 \right) = J_a + J_p (P / A)$$ (3.3)
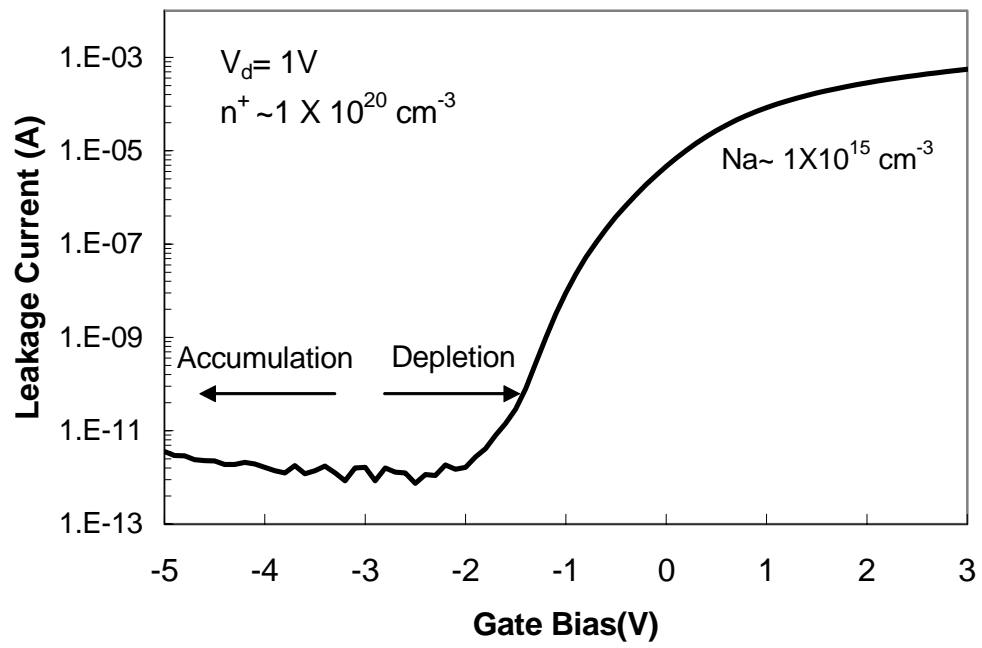
Figure III.2 Leakage current at 1V as a function of gate bias.
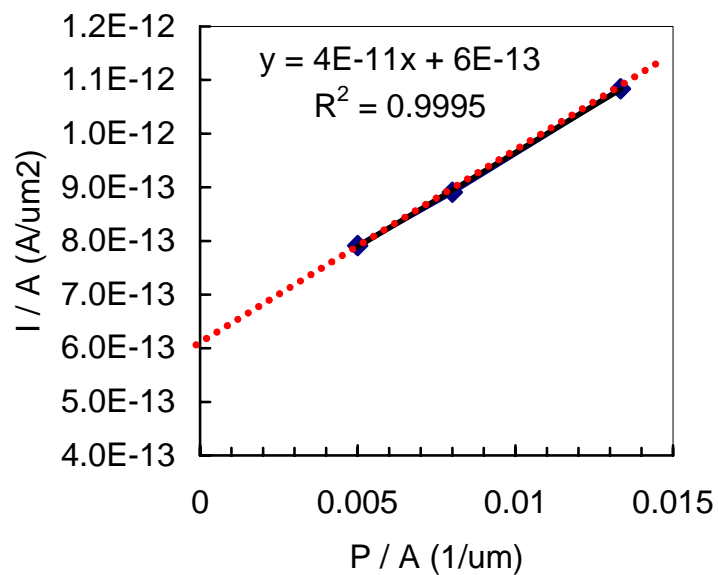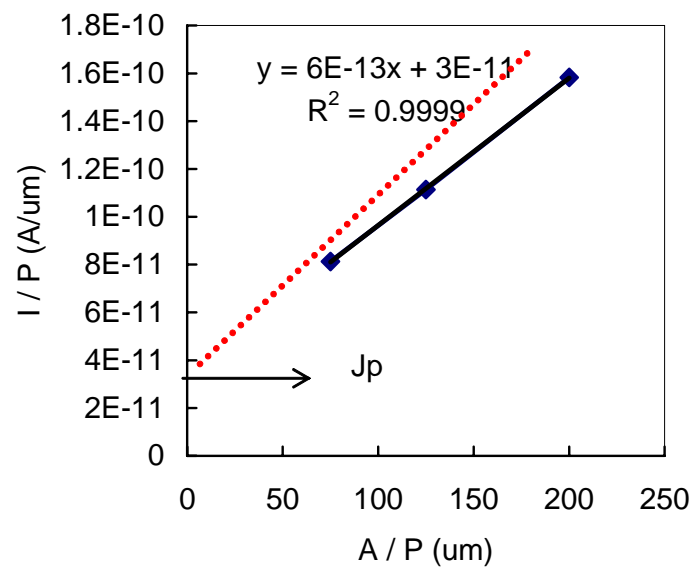
Figure III.3   Areal and peripheral leakage current density of the pn junction diodes.

Figure III.3 shows extraction of areal and peripheral current densities (J_a and J_p, respectively) from the measured currents (I_{tot}) on three different size diodes fabricated on substrates with a doping density of 10^{15} cm^{-3}. The measurements were made at a reverse bias of 1.0 V and a gate bias of –2 V. As shown, excellent straight line fits were obtained for the data points with a linear regression coefficient of almost unity. Extracted areal and peripheral components of the reverse current are shown as functions of the deposition temperature in Figure III.4. On each wafer, 50 - 90 measurements were carried out and the error bars show the standard deviations ($\pm \sigma$).

Figure III.4   Areal and peripheral components of the reverse leakage current as a function of the Si$_{1-x}$Ge$_x$ deposition temperature. The measurements were taken at a reverse bias of 1V.

It can be seen that the areal leakage current density is reduced as the deposition temperature is increased. A potential explanation for the improvement of the junction leakage at higher deposition temperatures is the likely improvement in the quality of the epitaxial layers. Since the portion of the depletion region on the heavily doped side of the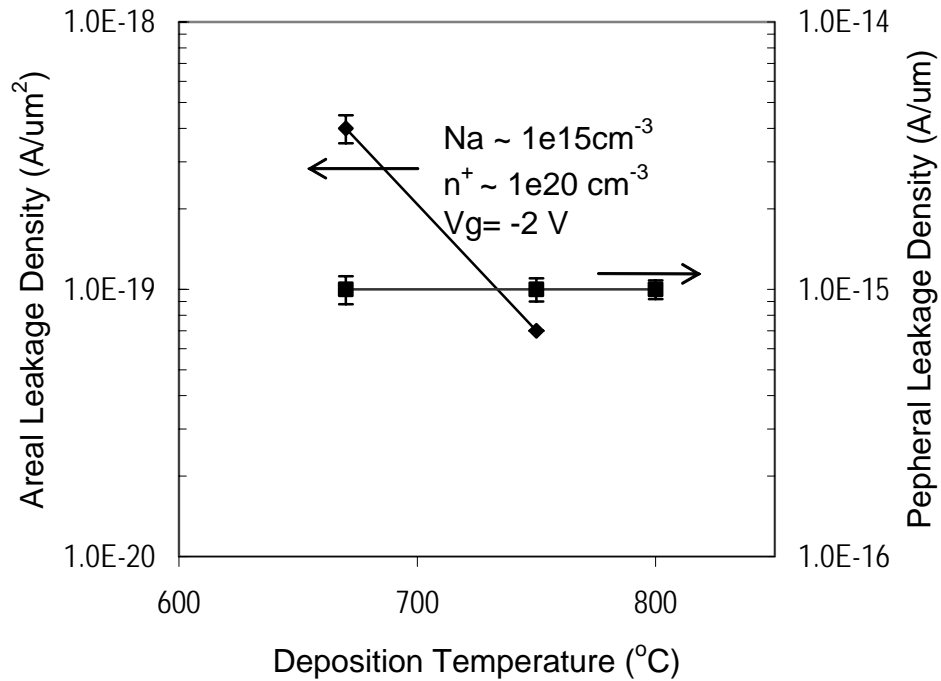 junction includes the n^+ $Si_{1-x}Ge_x$ layer, an improvement in generation lifetime will reduce the generation current. At the same time, Ge content of the deposited layers decrease as the temperature is raised, reducing the lattice mismatch between $Si_{1-x}Ge_x$ and Si. Higher Ge levels will increase the lattice mismatch and the density of misfit dislocations at the interface. The peripheral leakage is independent of the temperature possibly because the origin of this leakage is mainly carrier generation at the Si/oxide and $Si_{1-x}Ge_x$/oxide interfaces.

Figure III.5 shows the reverse-bias leakage current measured at different temperatures ranging from 20 to 200 ^{o}C. The diode active area is $500 \, \mu m$ x $500 \, \mu m$. Depending on the reverse bias voltage, we observe different slopes indicative of contributions of the generation and diffusion current components as shown in Figure III.5. Using the activation energy as an indicator, one can distinguish between I_{gen} and I_{dif} [4,8,9]. The data shown in Figure III.5 indicates that the transition from I_{gen} to I_{dif} shifts to higher temperatures as the depletion width increases at larger biases.
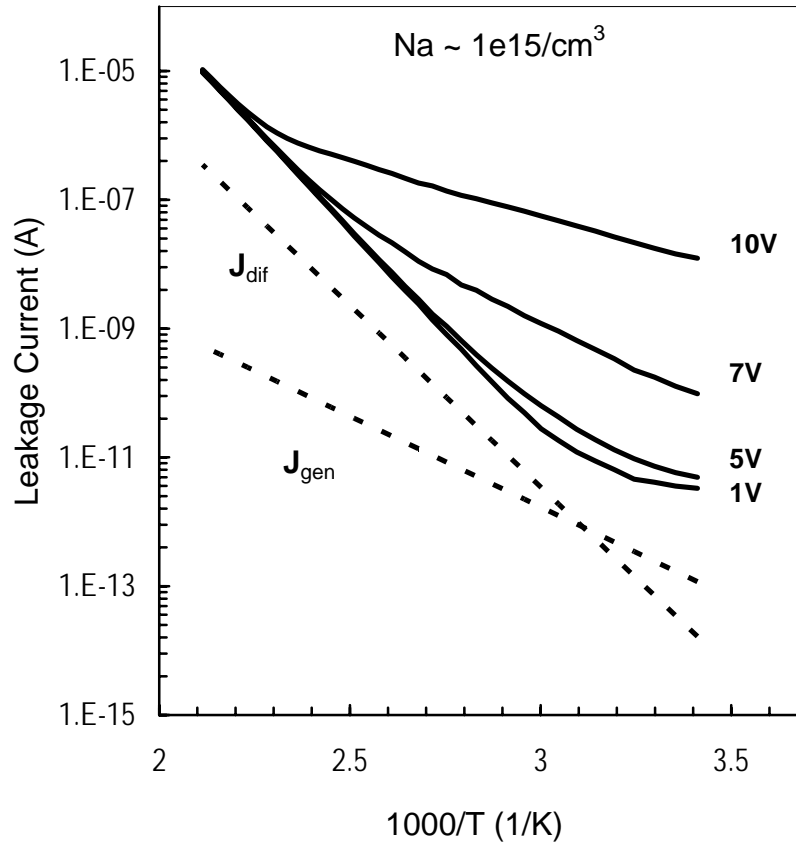
Figure III.5   Temperature dependence of leakage current on a low background doping.

Figure III.5 indicates that at room temperature, we have contributions from both current components. Nevertheless, the total leakage current is on the order of 20 pA for voltages up to 5 V, which is indicative of an excellent interface between the phosphorus doped $Si_{1-x}Ge_x$ and the lightly doped substrate. It should be noted that any defects at this interface are expected to contribute to the generation component of the leakage current.

b)   Junctions Fabricated on Heavily Doped Substrates

For junctions fabricated on heavily doped substrates the gate bias was found to have very little effect on leakage current as shown in Figure III.6. It was not possible to observe accumulation and depletion regions distinctly as the case in Figure III.2, which was suggestive of a much stronger leakage current component.
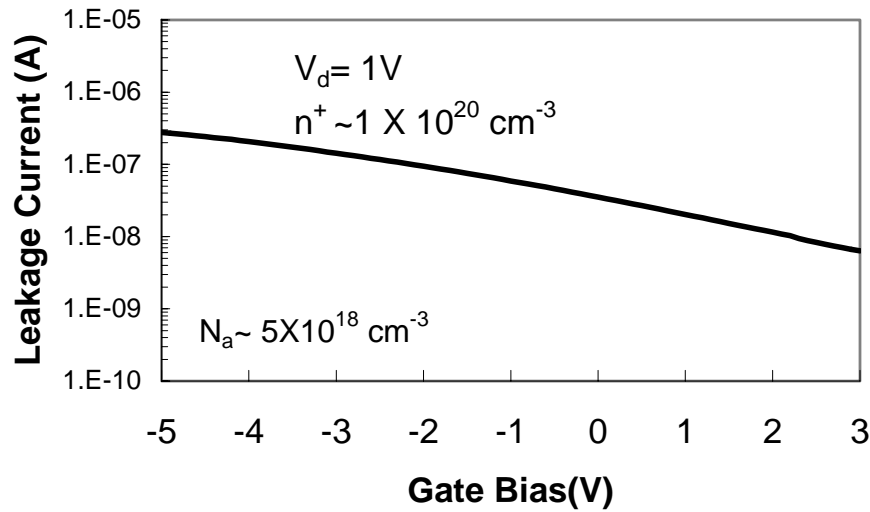
Figure III.6   Leakage current at 1 V reverse bias plotted as a function of gate bias.

Figure III.7 shows areal and peripheral components of the reverse leakage current at a reverse bias of 1.0 V. Again, the peripheral leakage current density is independent of the growth temperature. However, it is at least four orders of magnitude higher than the peripheral leakage current density observed in Figure III.4 for the lightly doped substrates. Areal leakage current density is also significantly higher. While the high peripheral leakage may be attributed to the lack of gated diode operation, the high areal leakage is expected to

result from the properties of the diode. A potential cause of high leakage might be the wider depletion region in $Si_{1-x}Ge_x$ on top of the heavily doped substrate. At the same time, epitaxial quality of the layers may be less than that observed on lightly doped substrates. However, as we shall show later in this chapter, the most likely cause of high leakage is band-to-band tunneling, which is a major concern for pn junctions of CMOS ICs at the end of the roadmap [6,7].
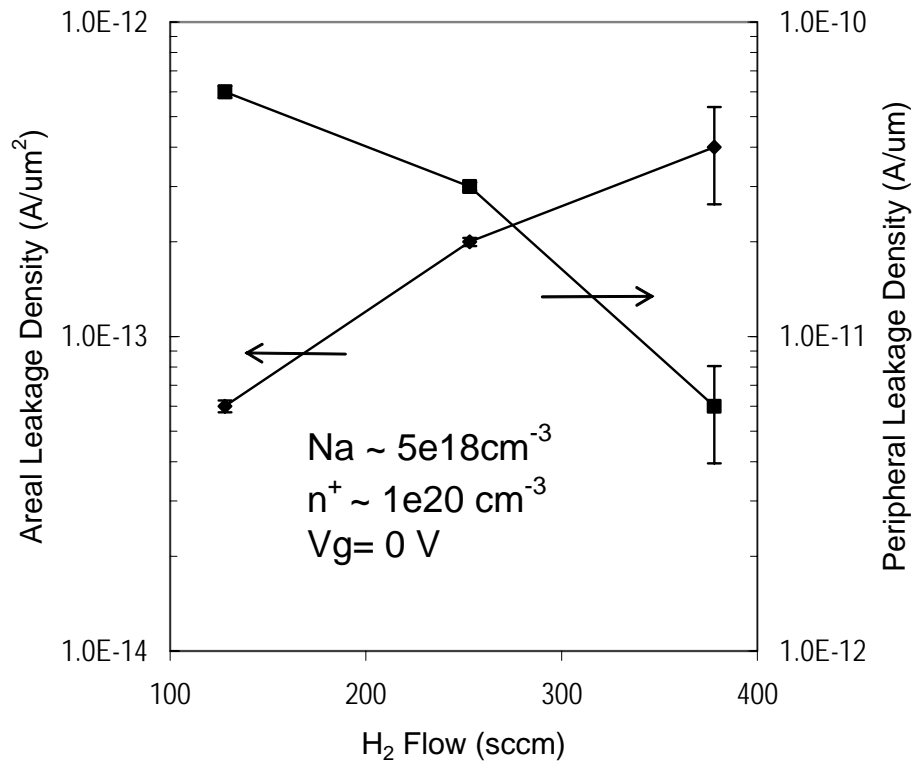
Figure III.7   Impact of H_2 addition to the areal and peripheral component of the reverse leakage current components of diodes fabricated on wafers with a high background doping density of (5×10^{18} cm^{-3}). The measurements were made at a reverse bias voltage of 1V.
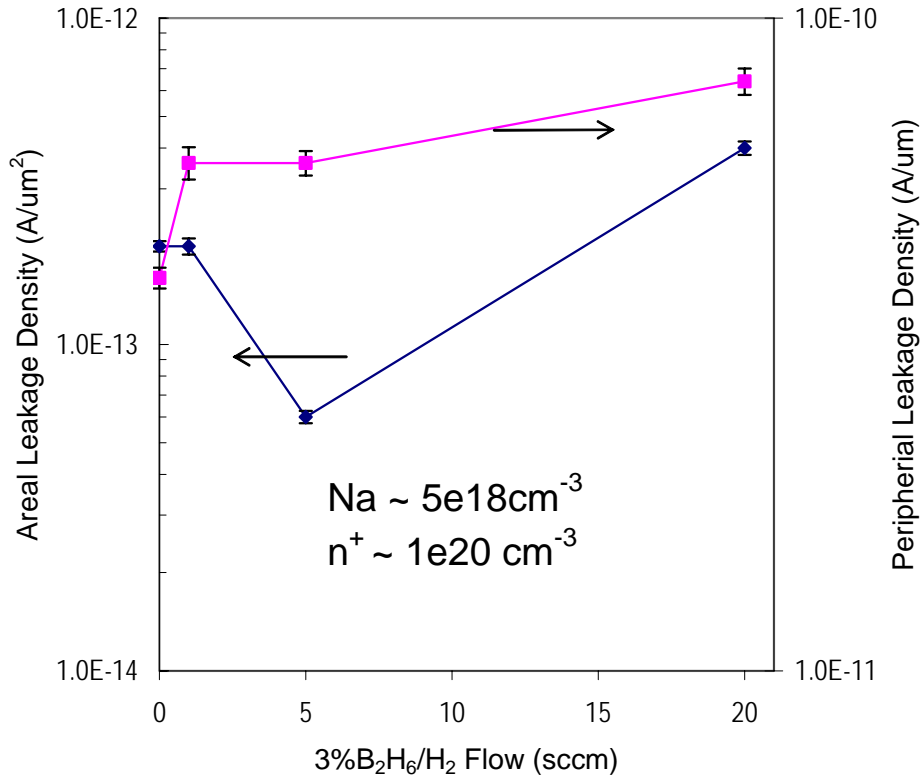
Figure III.8   Impact of B_2H_6 addition to the areal and peripheral component of the reverse leakage current components of diodes fabricated on wafers with a high background doping density of (5×10^{18} cm^{-3}). The measurements were made at a reverse bias voltage of 1V.

The impact of adding H_2 and/or B_2H_6 to deposition chemistry is shown in Figure III.7 and Figure III.8. As shown, the areal leakage density is slightly increased, but the peripheral leakage is decreased with hydrogen. In chapter II, we have observed that additional hydrogen slightly enhances phosphorus incorporation and possibly increases the defect density. The drop in peripheral leakage with hydrogen may come from passivation of the unsatisfied bonds at the interface between the thermal oxide and Si, which act as

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generation/recombination centers [2,4]. As shown in Figure III.8, the addition of diborane

results in a slightly higher peripheral leakage. Its effect of areal leakage does not follow a

definite pattern.
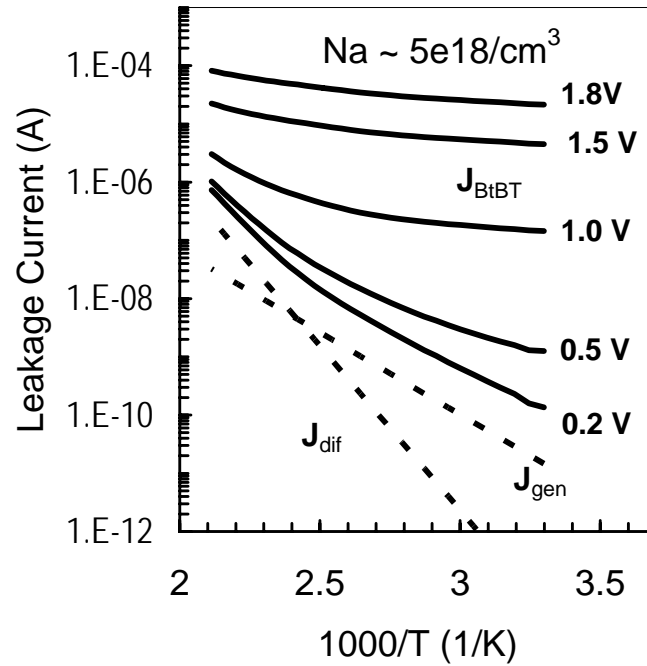
Figure III.9   Temperature dependence of the leakage current of diodes fabricates on
                wafers with a high background doping density.

On heavily doped substrates, band to band tunneling is expected to play an

important role.   Carrier generation at the Si/SiO_2 interface is expected to increase

contributing to the generation current [9]. Finally, carriers at the junction edge can tunnel

through via traps (trap assisted tunneling) [11-13]. Figure III.9 shows the reverse-bias

leakage current measured at different temperatures. At very low bias voltages (0.2 – 0.5V), the generation current is dominant. However, at higher voltages, the leakage current becomes nearly independent of temperature indicative of band-to-band tunneling induced leakage (J_{BTBT}). This behavior can be observed more clearly in Figure III.10, which shows the leakage current measured at different ambient temperatures as a function of the applied reverse bias voltage.
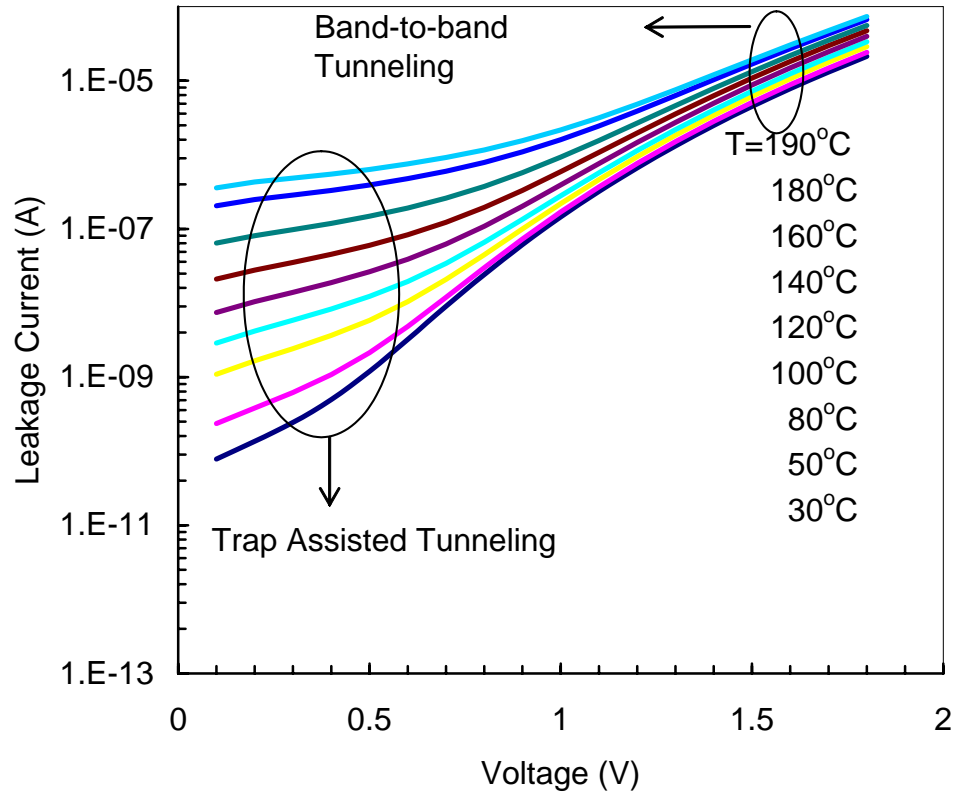
Figure III.10   Reverse current as a function of applied bias on a high background doping.
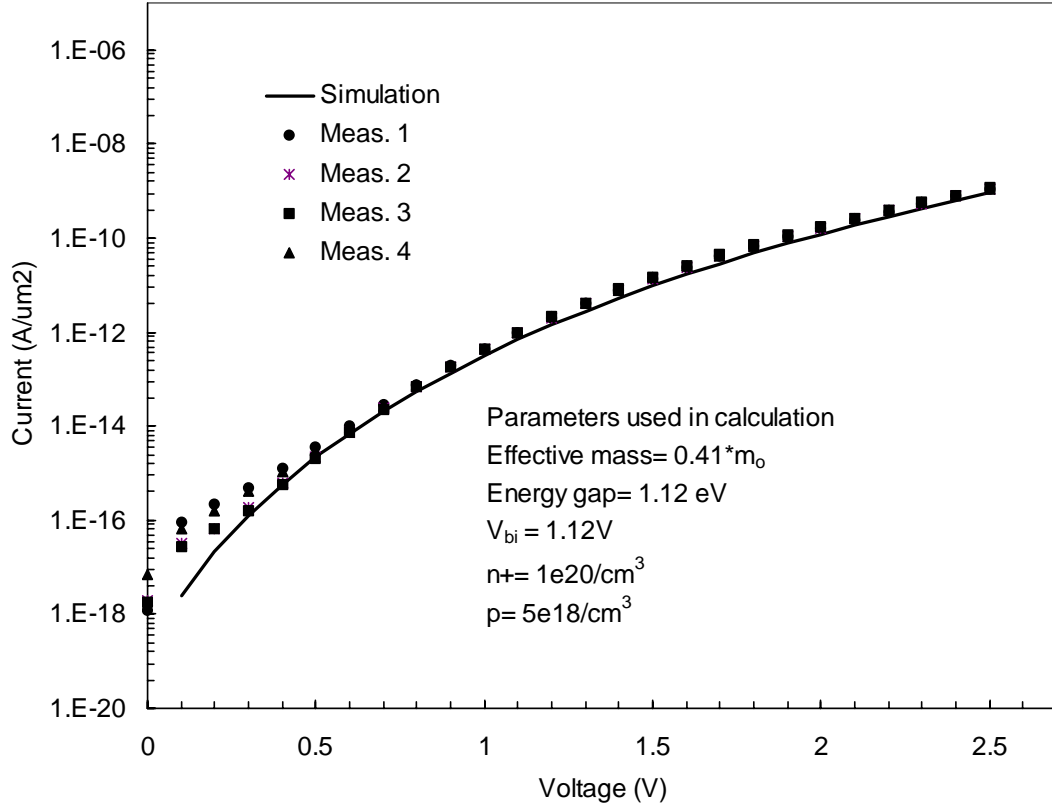
Figure III.11   Comparison between the calculated band-to-band tunneling current and the measured leakage current.

When the background doping density is high, the electric field strength can be so high that band to band tunneling (BTBT) begins to play a dominant role. The BTBT current is given by [6]:

$$J_{BTBT} = \frac{\sqrt{2m^*}q^3 E_J V_a}{4\pi^3 h^2 \sqrt{E_g}} \exp\left[\frac{-4\sqrt{2m^*}E_g^{3/2}}{3qE_J h}\right],$$

(3.5)

where E_J is the maximum electric field defined as:

$$E_J = \sqrt{2qN_A(V_a + V_{bi})/\varepsilon}\,, \tag{3.6}$$

and m^* is the effective mass, E_g is the energy gap, V_a is the applied bias, and V_{bi} is built-in potential across the n^+/p junction. In Figure III.11, the measured leakage and the current calculated using Equation (3.5), are both shown. The parameters used for the calculation are electron effective mass ($m_o^* = 0.41m_o$), energy gap (E_g=1.12 eV), built-in-potential ($V_{bi} \sim 1.12$), substrate doping ($p \sim 5\mathrm{x}10^{18}$ cm^{-3}), and P-level in Si$_{.95}$Ge$_{.05}$ ($n^+ \sim 1\mathrm{X}10^{20}$-cm^{-3}).

As the applied bias voltage across the junction is increased, the measured leakage current begins to follow the calculated tunneling current. Figure III.12 shows J_{BTBT} (A/μm^2), J_a (A/μm^2), and J_p (A/μm^2) as a function of the bias-voltage. Before the BTBT begins, the areal component of the leakage current is negligibly small similar to the lightly doped substrate case, as shown in Figure III.12. On the other hand, a very high peripheral leakage is induced even below 0.6 V when the BTBT begins. When electrical field is not strong enough for BTBT, carriers can still tunnel through the forbidden energy gap via traps.
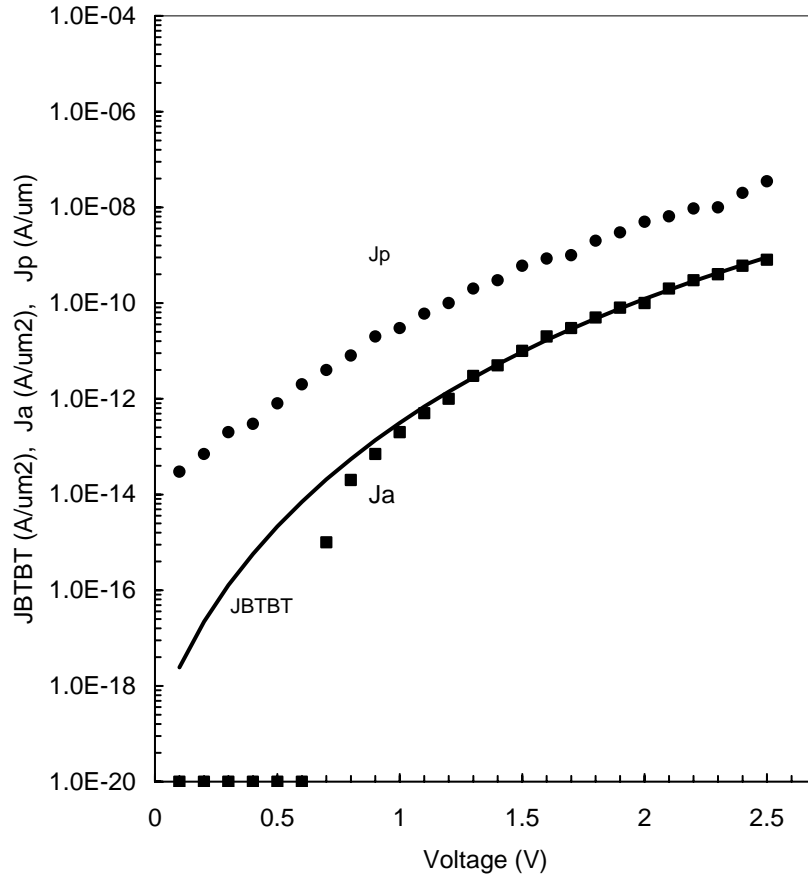
Figure III.12   Comparison between the calculated current and the areal and peripheral
component from a measurement.

III.3 Off-State Source/Drain leakage current for 45-22 nm technology nodes

In ITRS 2001, the sub-threshold leakage current requirements in low power logic devices are 0.3, 0.7, 1, 3, and 10 nA/μm for 53 – 37, 32, 22, 16, and 11 nm physical gate lengths respectively [14]. In order to compare the measured junction leakages and ITRS requirements, we have calculated the subthreshold leakage using the measured values of

areal and peripheral leakage current densities. The "3λ" design layout shown in Figure III.13 was used to determine the dimensions of the diodes. Based on the "3λ" design rule, the off-state junction leakage current can be expressed as:
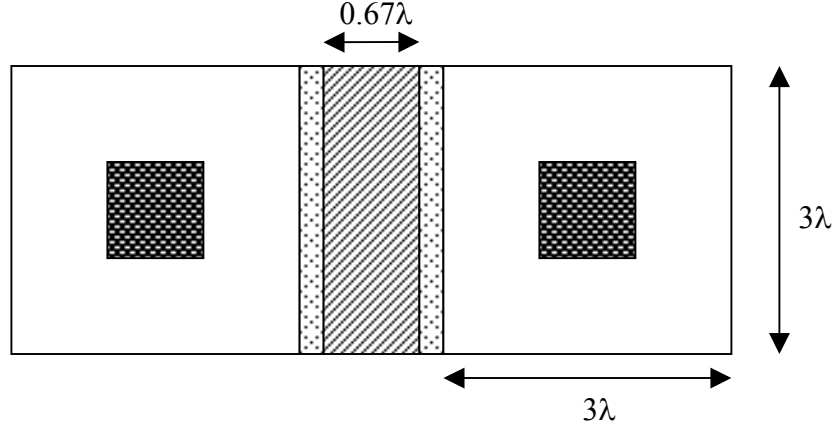
Figure III.13   3λ design layout

$$I_{off} = J_{off}\, 3\lambda = J_a (3\lambda)^2 + J_p\, 3\lambda \times 4 \,. \qquad (3.7)$$

By substituting J_a and J_p from Figure III.4 and Figure III.7 into Equation 3.7, one can extract the expected leakage current for different physical gate lengths. Figure III.14 shows the results of these calculations as well as the ITRS 2001 requirements. As shown, the junction leakage current on lightly doped substrates is negligibly small. The leakage current on heavily doped substrates (Na ~ 5 x 10^{18} cm^{-3}) is larger than the requirements until the gate length is down to 32 nm. It should be noted however that BTBT leakage is dominant on heavily doped substrates and it drops exponentially as the substrate doping

concentration is reduced. In ITRS 2001, the channel doping concentration ranges from 1.5 x 10^{18} cm^{-3} to 4 x 10^{18} cm^{-3} for 53 – 37 nm gate lengths. The figure also indicates that there is room for improvement. It is shown that when the hydrogen amount is increases, the leakage drops by an order of magnitude to satisfy all ITRS requirements.
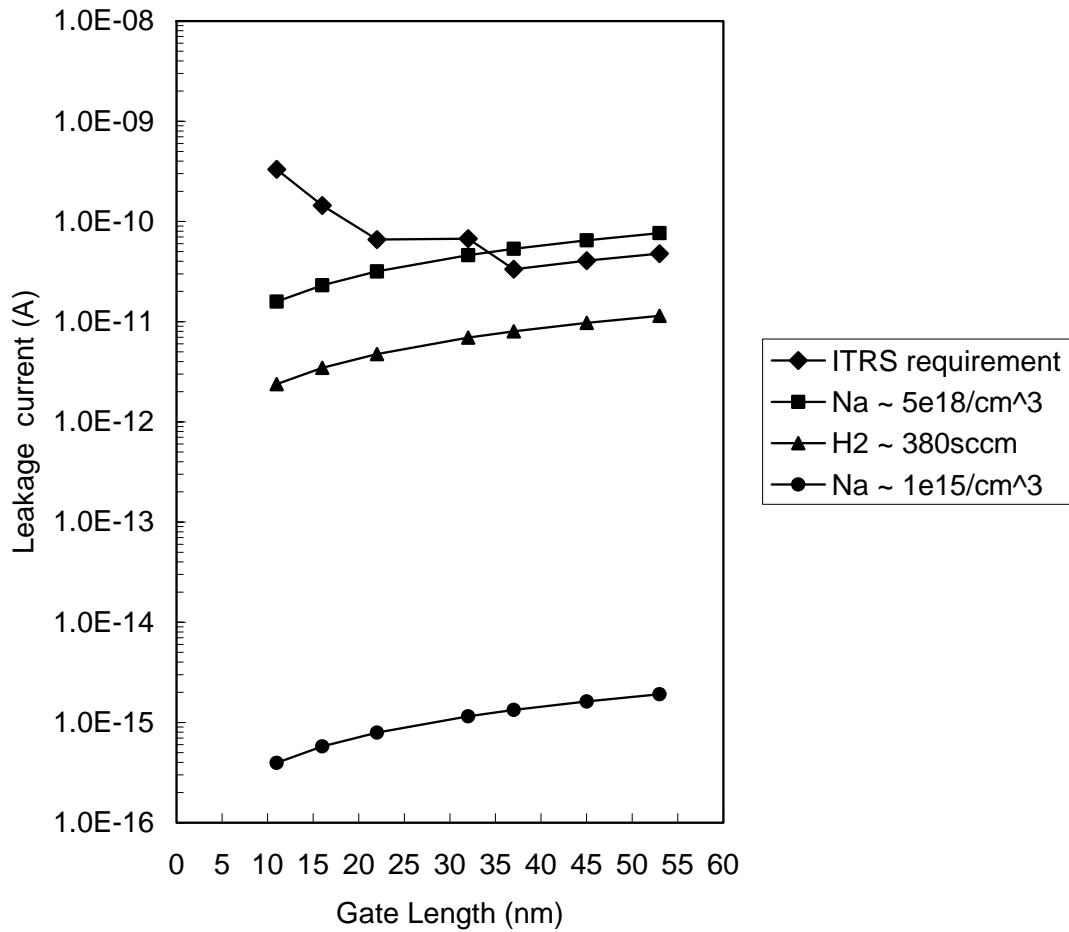
Figure III.14   ITRS 2001 requirements for sub-threshold leakage and extracted values using areal and peripheral components of measured leakage currents.

III.4 Junction Abruptness

We have employed a reverse-bias C-V technique that makes use of the junction depletion capacitance to determine the profile abruptness. The depletion region capacitance can be expressed as [15]:

$$C_J = C_{Jo}\left(1 - \frac{V}{V_{bi}}\right)^{-1/n} ,\qquad\qquad (4.10)$$
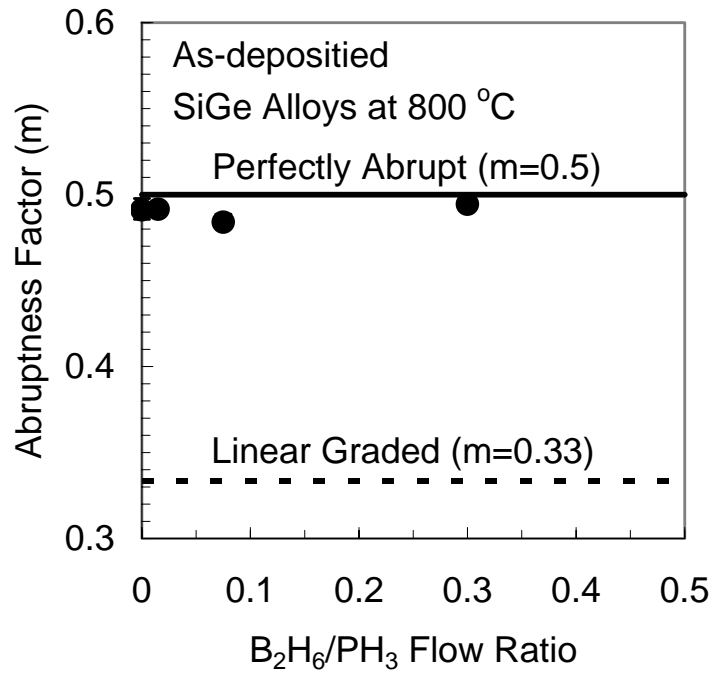
Figure III.15   Extracted phosphorus profile abruptness factors from reverse bias C-V measurements.

where C_{Jo} is the depletion capacitance at zero-bias. The abruptness (=1/n) changes from 0.5 for a perfectly abrupt junction to 0.333 for a linearly graded junction. After differentiating with respect to the applied voltage and arranging the terms we obtain:

$$Log\left(\frac{dC}{dV}\right) = (n+1)Log(C) - Log\left(nV_{bi}C_{j0}^{n}\right).$$ (4.11)

When Log(dC/dV) is plotted verses Log(C) we obtain a straight line with a slope equal to n+1. The results are shown in Figure III.15. As expected, all as-deposited films show nearly perfect abruptness.

III.5 References

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IV   Selective Deposition

IV.1 Introduction

Selective Si [1-6] or $Si_{1-x}Ge_x$ [7-11] epitaxy has been extensively studied by previous groups. Commercial CVD reactors for Si or $Si_{1-x}Ge_x$ epitaxy typically use SiH_2Cl_2 as the silicon precursor. These reactors rely on a large flow of hydrogen and operate at much higher pressures (10 – 100 Torr), which can introduce contaminants (mostly water vapor and oxygen) if not purified [3]. For selectivity, HCl is required in addition to the Cl supplied by the Si precursor [3,4,7].

UHV-CVD or UHV-RTCVD rely on a much cleaner growth environment and operate at much lower pressures, These systems typically use non-chlorinated Si precursors including SiH_4 and lower growth temperatures (600 – 800°C) [1,2,5,6,7-10]. It is known that both Si and $Si_{1-x}Ge_x$ epitaxy exhibits an intrinsic selectivity to insulators such as SiO_2 and Si_3N_4 at low deposition pressures [1,2,6-10]. However, the selectivity is typically lost after the deposited film reaches a critical thickness after an incubation period [1,9]. By adding a small amount of Cl_2 to the Si_2H_6 or Si_2H_6-GeH_4 chemistry, the selectivity can be greatly enhanced by surface passivation and/or etching Si or $Si_{1-x}Ge_x$ nuclei on oxide [2,7,8]. Unfortunately, we have observed that when large amounts of PH_3 are introduced into the growth environment selectivity can degrade. We have also discovered that Cl_2 addition cannot improve the selectivity appreciably when the growth temperature is within

$600 - 800^{o}C.$

T. Aoyama et al. introduced a Cl_2 pulsed molecular method, in which growth and etching occurs alternatively at a constant temperature [13]. In this work, a similar method was applied to grow in-situ phosphorus doped $Si_{1-x}Ge_x$ epitaxial layers without nuclei formation on the surrounding oxide. The effects of phosphorus incorporation in $Si_{1-x}Ge_x$ and its surface morphology owing to the addition of Cl_2 are also demonstrated.

IV.2 Impact of Cl_2 on Selective Epitaxy of In-Situ Phosphorus Doped $Si_{1-x}Ge_x$

a)   Selectivity and Growth Rate

Shown in Figure IV.1 is the AFM image obtained from a 34 nm thick heavily phosphorus doped $Si_{1-x}Ge_x$ layers grown without Cl_2. The flow rates of the precursors were Si_2H_6: 10 sccm, 8% GeH_4 (diluted in H_2): 37 sccm, and 1% PH_3 (diluted in H_2): 200 sccm. In spite of the high phosphine flow, excellent selectivity to thermal oxide is evident. Shown in Figure IV.2 is the AFM image obtained from a 50 nm thick film grown with 10 sccm Cl_2. The rough morphology of the oxide surface is indicative of nuclei formation and selectivity loss. Clearly, selective growth is not further improved by the addition of Cl_2. A slight increase in film thickness resulted in the selectivity loss. While adding Cl_2 during growth does not appear to be helpful, we will show that Cl_2 can be used as an etchant in a cycling process, which can be used to improve the selectivity substantially.
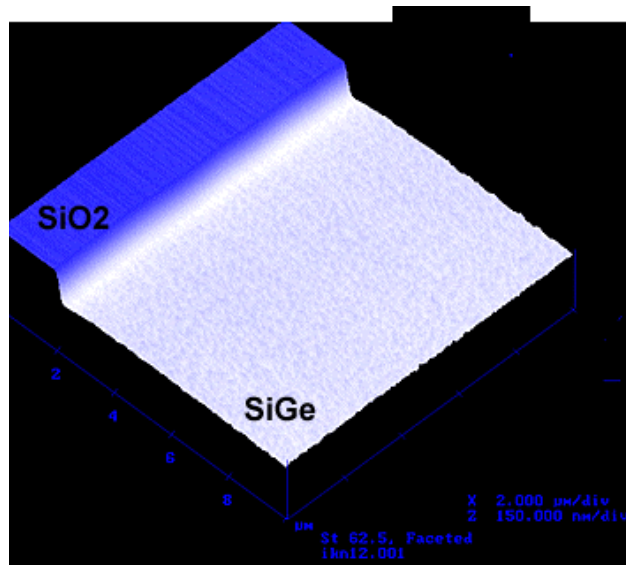
Figure IV.1   AFM image of selectively deposited in-situ P doped epitaxial $Si_{1-x}Ge_x$ film. No nuclei are formed on the surrounding insulator surface.
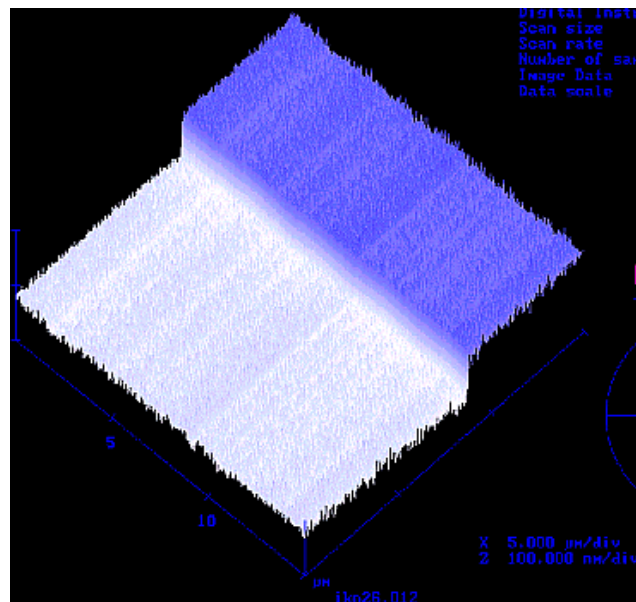
Figure IV.2   AFM image of selectively deposited in-situ P doped epitaxial $Si_{1-x}Ge_x$ film. Selectivity is lost and nuclei are formed on the surrounding insulator surface.

Hence, it is necessary to explore the impact of Cl_2 to the properties of the films in general. A series of experiments were carried out for this purpose and the results are presented in the remainder of this section.

Figure IV.3   Effect of Cl_2 on $Si_{1-x}Ge_x$ growth rate.

Shown in Figure IV.3 is the in-situ P-doped $Si_{1-x}Ge_x$ growth rate as a function of Cl_2 flow at $760^{\circ}C$. The reduction in growth rate with the Cl_2 flow can be attributed to passivation of the $Si_{1-x}Ge_x$ surface or etching.
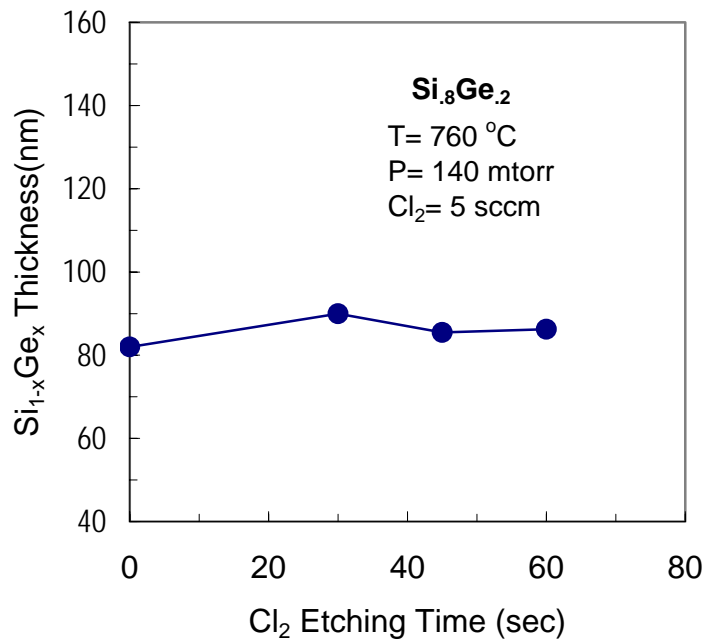
Figure IV.4 $Si_{1-x}Ge_x$ Thickness as a function of Cl_2 etching time.

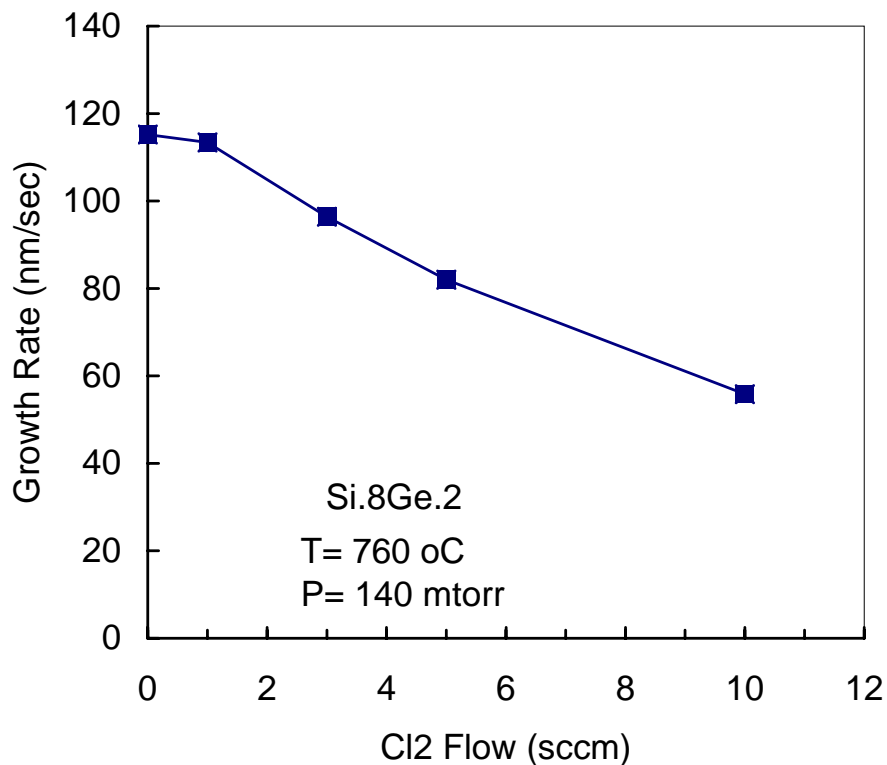It is possible to verify the etching contribution by simply exposing the surface to Cl_2. Four 80 nm thick in-situ P doped $Si_{1-x}Ge_x$ films were grown and annealed in 5 sccm of Cl_2 for 0, 30, 45, and 60 s. As shown in Figure IV.4, Cl_2 does not etch the $Si_{1-x}Ge_x$, which is interesting because previous results obtained in a similar system showed considerable Si etching under similar conditions. On Si, etching occurs via desorption of $SiCl_2$, which can provide Si etch rates on the order of micron/minute at 800°C, when the Cl_2 pressure is conducive to etching. It should be noted that the etching process is highly temperature sensitive. While almost no etching occurs at 700° very fast etching can be obtained at 800°C.   Therefore, one possible explanation for the discrepancy is a

temperature difference between the two systems, which can easily arise due to errors in temperature measurement by pyrometry. Another important variable is the Cl_2 partial pressure, which may not be sufficient to provide any significant etching at the growth temperature. In fact, on Si it is possible to move from etching to passivation simply by increasing the Cl_2 pressure. In any event, we can conclude that under the experimental conditions used in this experiment the decreased growth rate observed in Figure IV.3 is mainly due to Cl_2 passivation.

Shown in Figure IV.5 is the growth rate of in-situ phosphorus doped $Si_{1-x}Ge_x$ as a function of deposition temperature with and without Cl_2. We can observe that below 650ºC, the growth rate is negligibly small due to surface passivation. Since the same behavior is observed without Cl_2, we conclude that the surface is already passivated by the phosphorus atoms, which is expected for growth processes involving group V impurities. Above 650ºC, the growth rate increases almost linearly with temperature independent of Cl_2. It is evident that the addition of Cl_2 drops the growth rate only by a small amount. However, as we have shown in Figure IV.3, higher flow rates of Cl_2 can significantly reduce the growth rate. Therefore, in a selective process, the amount of Cl_2 should be optimized to remove the ad-atoms on the insulator surface without reducing the growth rate.
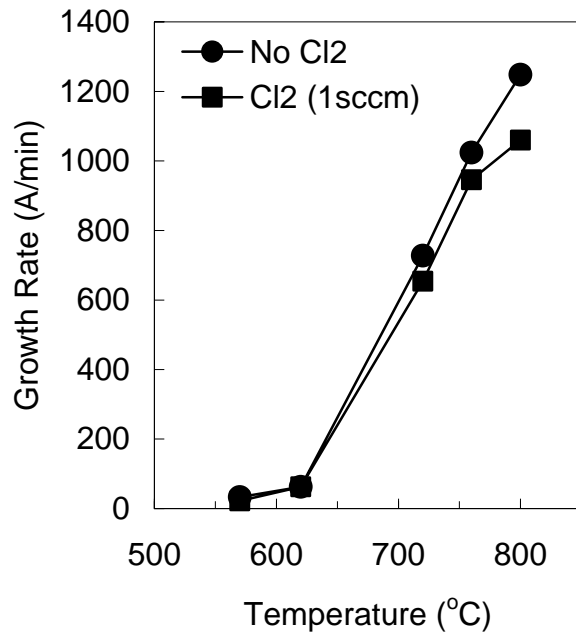
Figure IV.5   Growth rate of in-situ phosphorus doped $Si_{1-x}Ge_x$ as a function of deposition temperature with and without Cl_2.

b)   Carrier concentration, resistivity and mobility

The electrically active carrier density and resistivity determined by Hall Effect measurements are shown in Figure IV.6. We can see that the active carrier concentration goes down slightly with the addition of Cl_2, which results in a higher $Si_{1-x}Ge_x$ resistivity. This behavior can be the direct result of a reduced P incorporation or degradation in film quality. Shown in Figure IV.7 is the Hall mobility from the same experiment. The data demonstrates that the mobility is independent of the Cl_2 flow rate. Therefore, it is likely that P incorporation is somewhat reduced when Cl is present on the surface. Since Cl atoms tend to poison the growth surface at moderate temperatures, addition of Cl_2 may lead to a

competition between Cl and P atoms for available surface sites. At the same time, as we have seen in Figure IV.3, Cl_2 reduces the growth rate, which should provide more time to the P atoms to diffuse to the surface and reduce P incorporation in the bulk.
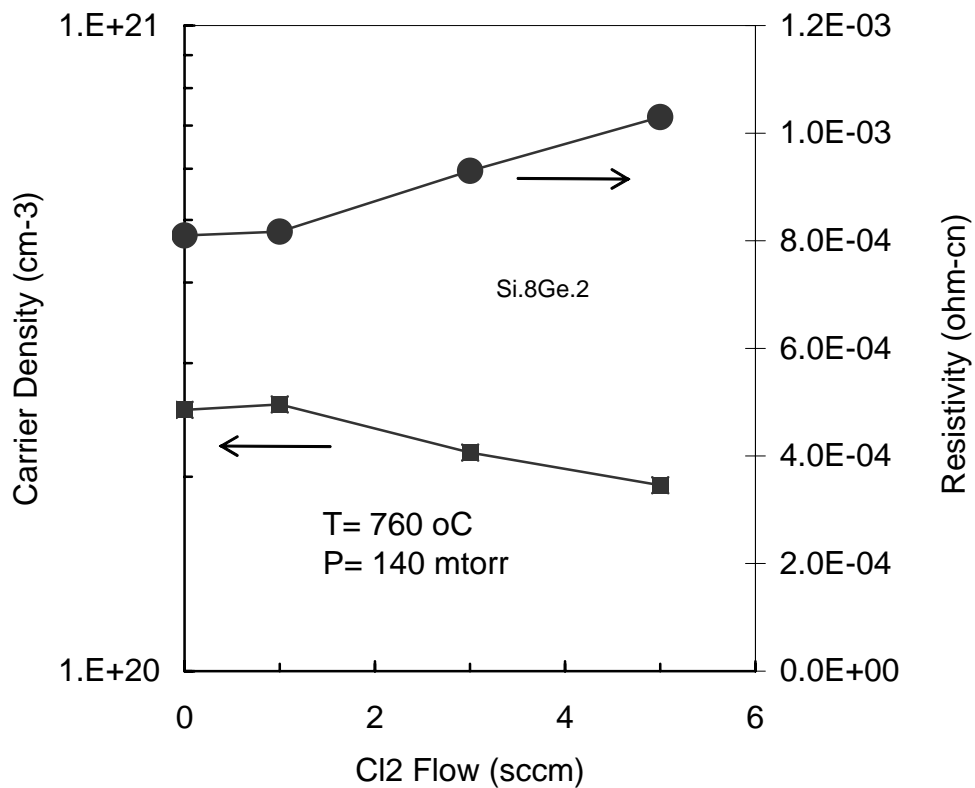

Figure IV.6   Active phosphorus concentration and $Si_{1-x}Ge_x$ resistivity as a function of the Cl_2 flow rate.
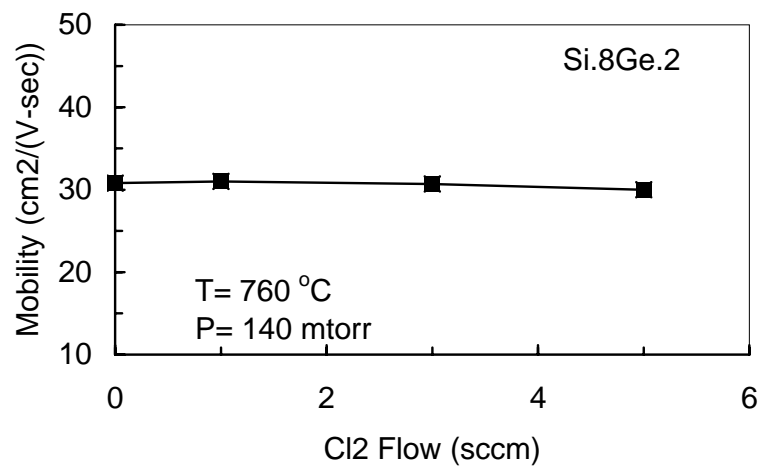
Figure IV.7   Hall mobility as a function of the Cl_2 flow rate.
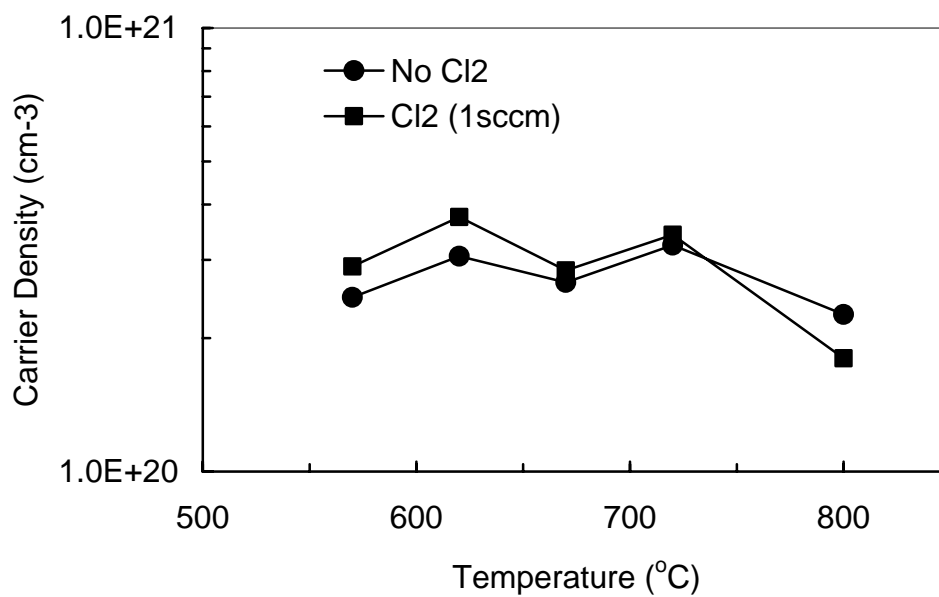

Figure IV.8   Active carrier concentration with and without Cl_2 at different temperatures.

Shown in Figure IV.8 is the active carrier concentration obtained with and without Cl_2 at different deposition temperatures. The Cl_2 flow rate is only 1 sccm. We can see that the impact of Cl_2 on phosphorus incorporation is negligibly small regardless of the deposition temperature. Therefore, provided the Cl_2 flow rate is small, its impact on film properties can be ignored.

IV.3 Selective $Si_{1-x}Ge_x$ Epitaxy Using Cycling

The gases used for the experimental results presented in this chapter are 100 % Si_2H_6 (13.6 sccm), 10 % GeH_4 diluted in H_2 (67 sccm), 1 % PH_3 diluted in H_2 (20 sccm), 100 % H_2 (200 sccm), and 100 % Cl_2 (1-10 sccm). $Si_{1-x}Ge_x$ deposition was carried out at a pressure and temperature of 140 mtorr and 760°C, respectively. After the ex-situ RCA clean and immediately before each deposition, the wafers were individually annealed in vacuum at 800°C for 10 – 15 s to remove any residual oxygen on the surface. Then, the process gasses including Cl_2 were introduced into the chamber. The deposition was initiated by turning on the lamps to heat the wafer to the deposition temperature of 760°C. After ~ 30 s, all gasses except Cl_2 were turned off while maintaining the temperature at 760°C to etch any nuclei forming on the insulator surface. After ~ 30 s etching, the deposition gasses were introduced back to the chamber to grow another layer of $Si_{1-x}Ge_x$. The deposition and etching cycles were continued until the desired film thickness was achieved. The process is illustrated in Figure IV.9.
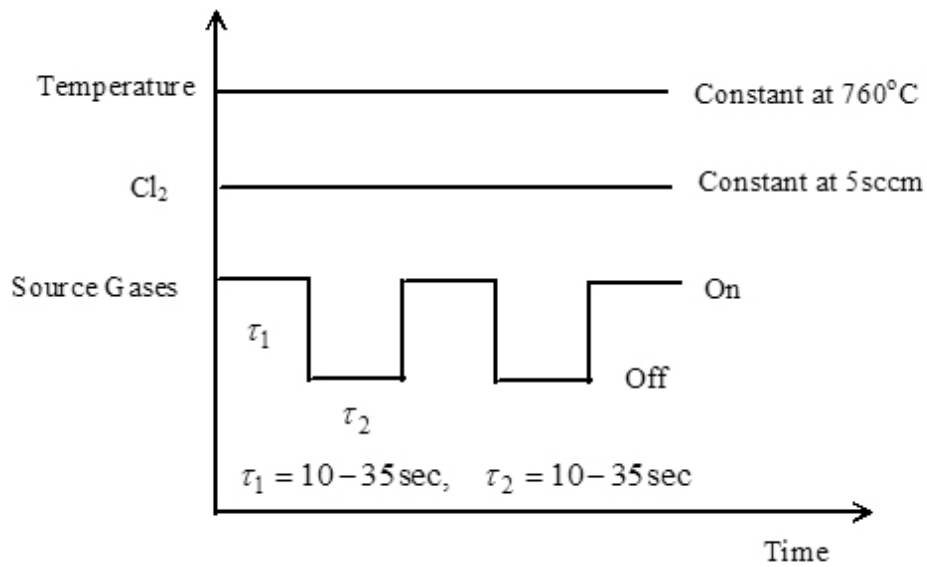
Figure IV.9   Cycling process used to improve the selectivity of in-situ phosphorus doped $Si_{1-x}Ge_x$ layers.

Figure IV.10 shows AFM scan images of four P-doped $Si_{.8}Ge_{.2}$ layers deposited by the cycling process. The thickness of the surrounding oxide is ~ 1050 Å. All four films have identical deposition and etching periods ranging from 35 s to 10 s. The number of deposition – etch cycles was changed from 2 to 7 in order to deposit about the same $Si_{1-x}Ge_x$ thickness of ~ 1100 Å in all four cases.

Figure IV.10   AFM images obtained from samples grown by the cycling method (a) (35 s deposition/35 s etch) – 2 cycles (b) (20 s deposit/20 s etch) - 5 cycles (c) (15 s deposition/15 s etch) – 4 cycles (d) (10 s deposition/10 s etch) – 7 cycles

The samples c – d show excellent selectivity. On the other hand, sample (a) clearly exhibits nuclei visible on the surrounding oxide indicative of loss of selectivity. Therefore, it appears that in samples a – c that the deposition period is not sufficient to form stable nuclei on the surface. During the etching period the ad-atom densities of Si and Ge are

reduced via desorption in the form of $SiCl_2$ or $GeCl_2$, which in turn reduce the probability of reaching the critical nucleus size during the next deposition period. Alternatively, tiny nuclei form during the deposition periods but etched rather quickly during the etching periods due to their three-dimensional shapes, which allow etching from all three directions.

Another interesting observation we can make from the AFM images in Figure IV.10 is that the film quality degrades as the number of cycles is increased. On samples a – c, pyramid defects appear with an increasing density and sample (d) exhibits a very rough $Si_{1-x}Ge_x$ surface. Since the temperature is kept high during the entire cycling process, surface contamination is not likely. One potential explanation for the degradation might be phosphorus spikes that could form when the growth rate decreases substantially at the beginning or end of each deposition cycle. More work is necessary to explain these experimental observations.

In order to see the etching effect on such tiny nuclei, Cl_2 etching time was varied for a constant deposition time of 20 s. AFM images from the samples grown are shown in Figure IV.11. It can be seen that when the etching period is only 10 s, the selectivity is lost. On the other hand, when the etching time is increased by only 5 s, the selectivity is regained.

These results show that the cycling process can be used to improve the selectivity of the $Si_{1-x}Ge_x$ deposition process substantially. The deposition and etching periods have to

be optimized to preserve selectivity while minimizing the probability of forming the pyramid defects. The preliminary results indicate that the density of pyramid defects increases if the deposition and etching periods are reduced.
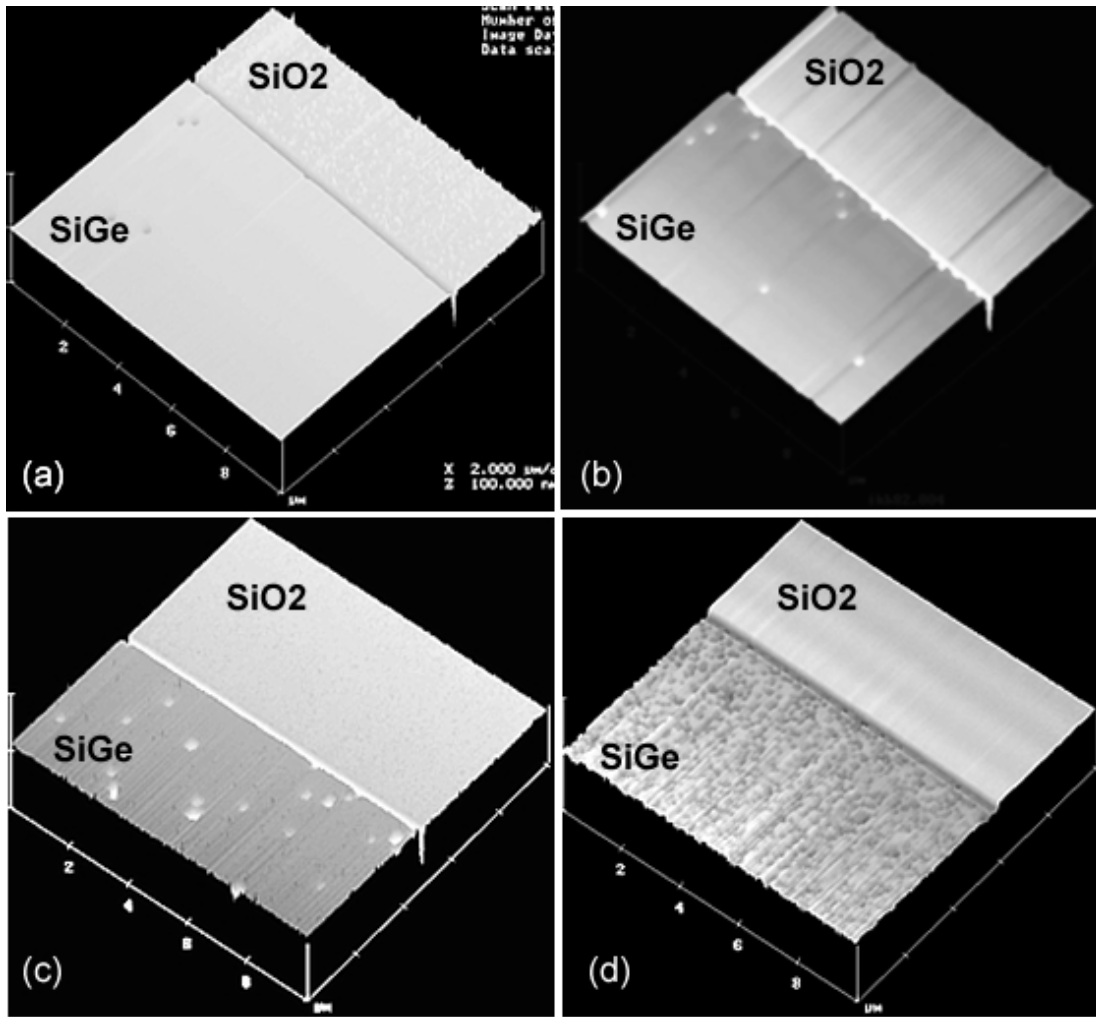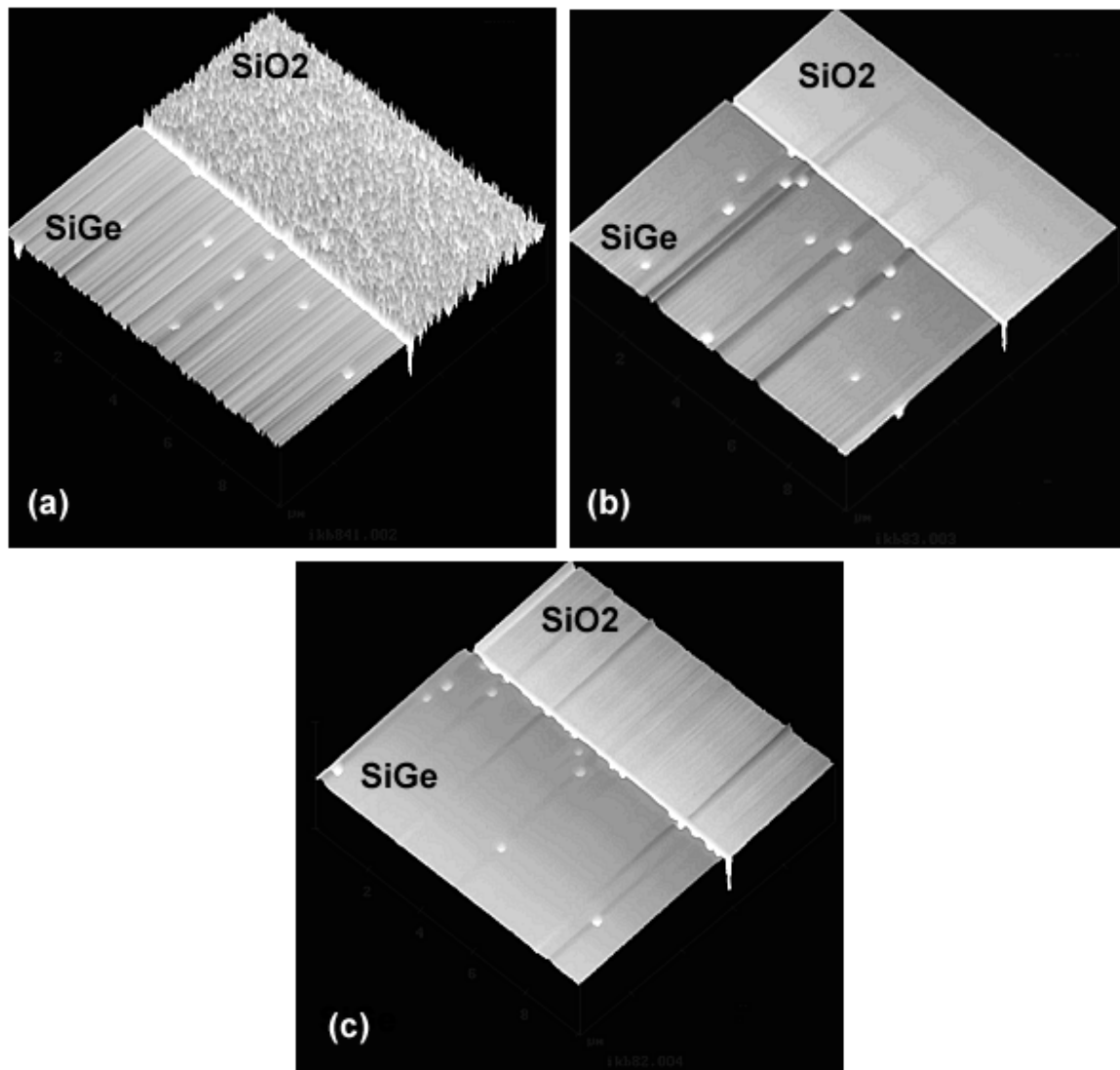

Figure IV.11   AFM images obtained from samples grown by the cycling method. (a) (20 sec. deposition / 10 sec. etch) – 4 cycles(b) (20 sec. deposition/ 15 sec. etch) – 4 cycles(c) (20 sec. deposition/ 20 sec. etch) – 4 cycles
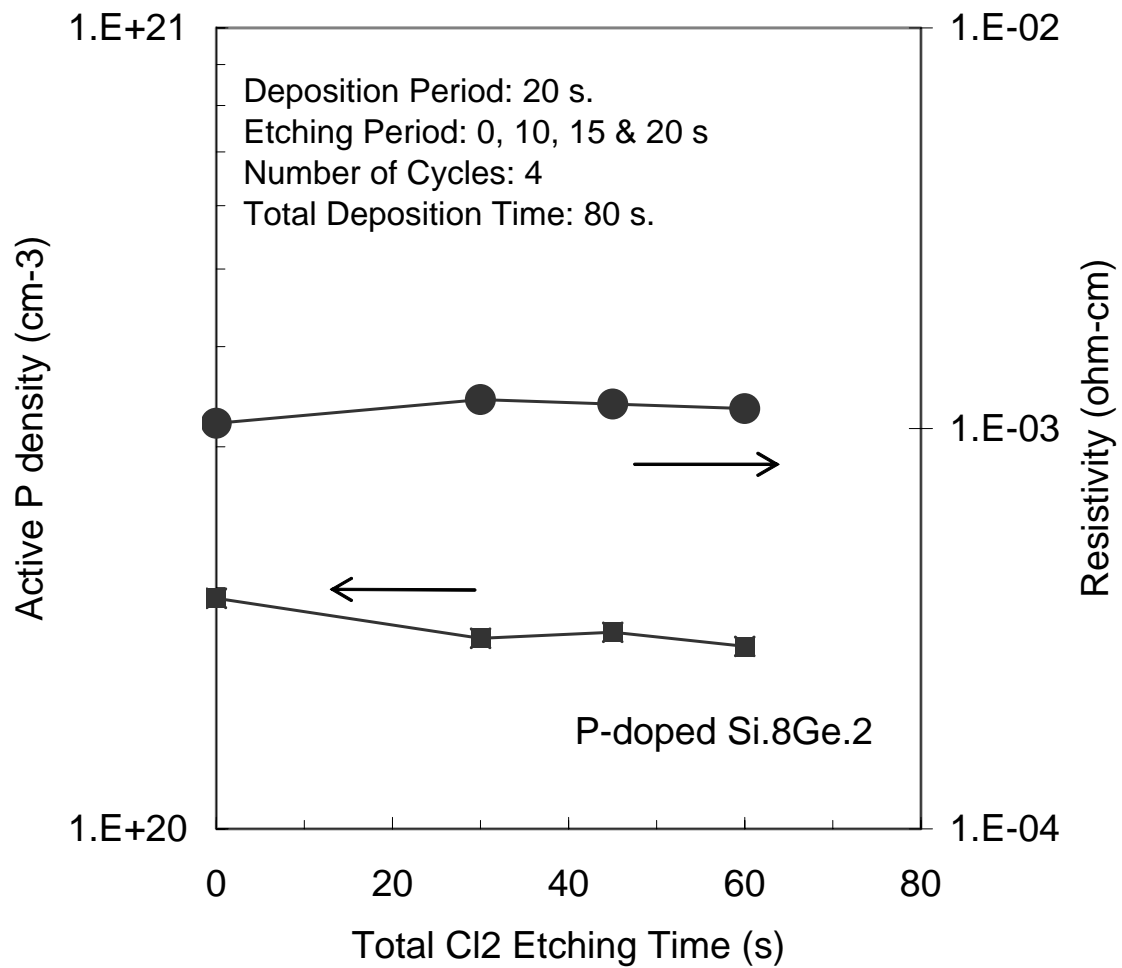
Figure IV.12   Active phosphorus concentration and $Si_{1-x}Ge_x$ resistivity obtained by cycling.

Figure IV.12 shows the active carrier concentration and resistivity as a function of the total Cl_2 etching time in $Si_{.8}Ge_{.2}$ films grown by the cycling method. The Cl_2 flow during the deposition and etching periods was 5 sccm. As shown, both the carrier density and resistivity are independent of the Cl_2 etching time. In fact, all data points are identical

to the data obtained from a sample with no etching. Shown in Figure IV.13 is the Hall mobility as a function of the total etching time obtained from the samples of Figure IV.12. It can be seen that the cycling method does not degrade the mobility of the layers.
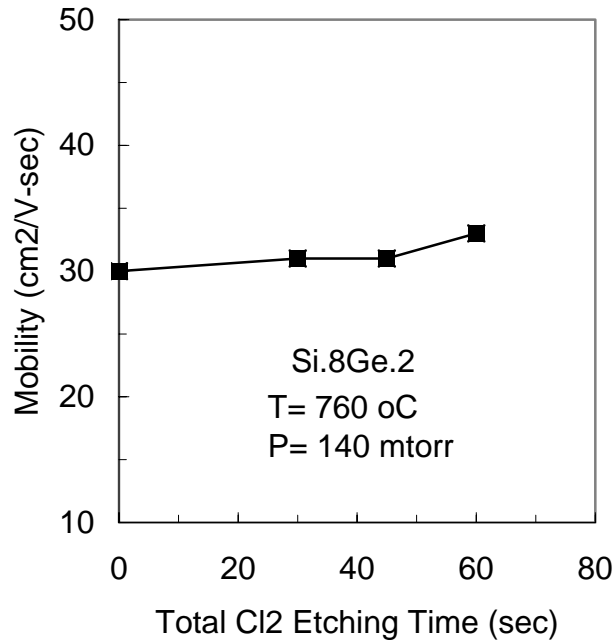
Figure IV.13   Hall mobility as a function of etching time in samples grown by the cycling method.

IV.4 Conclusions

The results presented in this chapter have shown that Cl_2 cannot improve the selectivity if it is simply added to the deposition chemistry. The experimental results indicate that Cl_2 can poison the surface and reduce the growth rate. This is accompanied by a slight reduction of the phosphorus level, which may be attributed to the slower growth

rate or reduction in the density of the available sites for phosphine adsorption. Etching experiments in Cl_2 indicate that negligible etching takes place if $Si_{1-x}Ge_x$ layers are exposed to the typical Cl_2 flows used for growth.

The results in this chapter also demonstrate that the process selectivity can be substantially improved by using a cycling process in which deposition and etching cycles are alternated until the desired film thickness is achieved. The etching is performed in pure Cl_2 without reducing the temperature. It is interesting to note that while similar Cl_2 flows cannot etch the $Si_{1-x}Ge_x$ layers by any measurable amount, the tiny nuclei that form on the oxide can be removed. The results indicate that the durations of the deposition and etching cycles must be optimized in order to achieve selective growth while keeping the density of pyramid defects as low as possible. The defects appear when the durations of the deposition and etching cycles are kept short requiring a larger number of cycles to reach the desired film thickness.

V Conclusions and Future Work

In this work, we have examined selective epitaxy of heavily phosphorus doped $Si_{1-x}Ge_x$ alloys for source/drain junctions of future CMOS technology nodes. In-situ doped junctions do not require annealing at high temperatures to activate the dopants since dopant atoms naturally occupy substitutional sites during growth. Since $Si_{1-x}Ge_x$ deposition can be carried out at temperatures less than 800ºC, dopant diffusion is effectively suppressed resulting in super-abrupt junctions, which is a key requirement for reducing the spreading resistance. Furthermore, the smaller bandgap of $Si_{1-x}Ge_x$ reduces the metal-semiconductor barrier height, a key requirement for reducing the contact resistance.

The deposition chemistry used in this work consisted of disilane, germane, phosphine, hydrogen and chlorine. The depositions were carried out in a UHV-RTCVD reactor constructed as part of this thesis.

The results presented in Chapter 2 show that in-situ phosphorus doped $Si_{1-x}Ge_x$ alloys with an active phosphorus concentration of $\sim 2 - 4 \times 10^{20}$ cm^{-3} can be obtained in $Si_{1-x}Ge_x$ films with 10 - 30% Ge. It is also shown that the phosphorus incorporation is tied to the surface chemistry determined by the Si and Ge precursors. As such, the P concentration cannot be adjusted independent of the Ge content in the layer.

The optimum growth temperature was found to be around 750ºC. At lower

temperatures, phosphorus atoms poison the growth surface and reduce the density of available sites for Si and Ge ad-atoms. At ~ 750°C, the PH_3 flow can be optimized to obtain an active phosphorus level of at least 2×10^{20} cm^{-3}.

Many attempts were made to boost the phosphorus level such as adding H_2 and B_2H_6 to the deposition chemistry, which were unsuccessful. Nevertheless, the phosphorus concentration achieved in $Si_{1-x}Ge_x$ is a significant improvement over the Si case in which the maximum phosphorus concentration cannot exceed ~ 5×10^{19} cm^{-3}. Furthermore, analysis of the layers by SIMS indicates that the film surface may have a much higher concentration of phosphorus due to phosphorus segregation during growth. This may prove helpful in achieving a low contact resistivity.

Junctions formed on lightly doped substrates without any post-deposition annealing demonstrate excellent reverse leakage behavior. This was surprising given the fact that the Si substrate and the $Si_{1-x}Ge_x$ layer are lattice mismatched and the strain compensation is not likely with the relatively low levels of phosphorus. It is possible that some strain compensation does occur increasing the critical thickness of the $Si_{1-x}Ge_x$ layers grown. However, more work is clearly necessary to reach a better understanding of the $Si/Si_{1-x}Ge_x$ interface. When the junctions were formed on heavily doped substrates (N_A ~ 5×10^{18} cm^{-3}), the leakage current was dominated by band to band tunneling.

Addition of high levels of PH_3 was found to degrade the selectivity of the deposition process. A cycling process, which consisted of alternating cycles of deposition

and etching was developed to improve the selectivity. Cycling was achieved simply by switching the source gas flow on and off. Hall Effect measurements showed that cycling did not degrade the electrical properties of the layers.

The experimental results in this work were obtained using disilane as the Si precursor. Future work should consider dichlorosilane and silane as alternative gasses for improved selectivity and higher phosphorus incorporation. This is especially important given the fact that dichlorosilane is the preferred gas in commercial reactors in spite of its several disadvantages.

The surface chemistry involving phosphorus, Si and Ge has to be better understood before predictive models can be developed. The experimental results from this work indicate that the process exhibits a fairly complex surface chemistry. Partial pressures of the P, Si and Ge precursors, H_2, Cl_2 and temperature influence the growth rate and phosphorus and germanium incorporation rates. Consideration of different chemistries is suggested to develop a process less sensitive to process conditions.

The ultimate success of this process relies on the ability to provide a contact resistivity on the order of 10^{-8} ohm-cm^2. Future work has to focus on contact resistivity obtained with different self-aligned germanosilicides. The films grown in this work had an active phosphorus level of $\sim 2 - 4 \times 10^{20}$ cm^{-3}, which is not particularly high. According to Figure I., with this doping concentration, the barrier height has to be ~ 0.35 eV to achieve a contact resistivity of $\sim 10^{-8}$ ohm-cm^2. Unfortunately, this is not possible with a Ge

concentration of 10 – 30% especially if the $Si_{1-x}Ge_x$ layer is relaxed. At the same, we should remember the fact that Hall Effect measurements can only provide an average value for the non-uniform phosphorus profile obtained due to phosphorus segregation. It is quite possible that the active phosphorus level at the surface is well above the number given by the Hall Effect measurements. Furthermore, it may be possible to find a germanosilicide material, which rejects phosphorus atoms resulting in a snow-plow effect or promote P segregation at the germanosilicide/$Si_{1-x}Ge_x$ interface. Preliminary results by Hongxiang Mo, another fellow graduate student in my research group indicate that nickel germanosilicide contacts can deliver a contact resistivity of $\sim 10^{-8}$ ohm-cm^2 using the n-type $Si_{1-x}Ge_x$ process developed in this work.