

ABSTRACT

Mathur, Guruvayurappan S. **Redox-active organic molecules on silicon and silicon dioxide surfaces for hybrid silicon-molecular memory devices.** (Under the direction of **Dr. Veena Misra**)

The focus of this dissertation is on creating electronic devices that utilize unique charge storage properties of redox-active organic molecules for memory applications. A hybrid silicon-molecular approach has been adopted to make use of the advantages of the existing silicon technology, as well as to study and exploit the interaction between the organic molecules and the bulk semiconductor. As technology heads into the nano regime, this hybrid approach may prove to be the bridge between the existing Si-only technology and a future molecule-only technology.

Functionalized monolayers of redox-active molecules were formed on silicon surfaces of different doping types and densities. Electrolyte-molecule-silicon test structures were electrically characterized and studied using cyclic voltammetry and impedance spectroscopy techniques. The dependence of the oxidation and reduction processes on the silicon doping type and density were analyzed and explained using voltage balance equations and surface potentials of silicon. The role played by the silicon substrate on the operation of these memory devices was identified. Multiple bits in a single cell were achieved using either molecules exhibiting multiple stable redox states or mixed monolayer of different molecules.

Self-assembled monolayers of redox-active molecules were also incorporated on varying thickness of silicon dioxide on n- and p- silicon substrates in an attempt to create non-volatile memory. The dependences of read/write/erase voltages and retention times of these devices were correlated to the SiO₂ thickness by using a combination of Butler-Volmer and semiconductor theories. The region of operation of the silicon surface (accumulation, depletion or inversion) and the extent of tunneling current through the silicon dioxide were found to influence the charging and discharging of the molecules in the monolayer. Increased retention times due to the presence of SiO₂ can be useful in realizing non-volatile memories.

Polymeric films of molecules were formed on Si and SiO₂ substrates and exhibited very high surface densities. Metal films were deposited directly on these films and the resultant devices were found to exhibit redox-independent behavior. A combination of metal gate and dielectric was deposited on molecules in an attempt to create solid-state hybrid silicon-molecular devices. The metal gate and dielectric can replace the electrolyte and electrolytic double-layer to create an electronic cell instead of an ionic cell. The redox properties of the molecules were retained after the deposition of dielectric and metal, which augurs well for a solid-state device.

FET type structures were fabricated and molecules incorporated on them in order to modulate the characteristics of the FETs by charging and discharging the molecules. Drain current and transfer characteristics of electrolyte-gated "moleFETs" were modulated by oxidizing and reducing molecules on the channel region. Hybrid moleFET devices may be ideal tools for creating non-volatile FLASH type memory devices.

This work has recognized the interaction of organic molecules and bulk silicon and utilized the advantages of current CMOS technology along with the unique properties of molecules, such as discrete quantum states, low voltage operation etc., to create a class of hybrid memory devices. A way to create solid-state molecular devices retaining the inherent properties of molecules has been proposed and demonstrated. This work might be useful in providing a smooth transition from silicon electronics to molecular electronics.

**REDOX-ACTIVE ORGANIC MOLECULES ON SILICON AND SILICON
DIOXIDE SURFACES FOR HYBRID SILICON-MOLECULAR
MEMORY DEVICES**

By
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BIOGRAPHY

Guruvayurappan S. Mathur, also known as Guru Mathur, was born to Mr. Sankaranarayanan M. G. and Mrs. Narayani R., on Monday, July 21 1980, in Madras, India. He has a younger brother, Mani, who was born in October 1982. Guru joined kindergarten when he was 2 years and 11 months old. After two years in kindergarten, he enrolled in primary school at S. B. O. A. School & Junior College located in Annanagar, Madras, India. He continued his entire schooling from first to twelfth grade at SBOA. During the first ten years of schooling, he developed an avid interest in Science and Mathematics and received many award certificates for academic achievements. In his eleventh and twelfth grades, he majored in Science with Math, Physics, Chemistry and Computer Science as the major subjects. In the All India Senior School Certificate Examination (AISSCE) held in the year 1997, Guru secured 100% in Math & Chemistry and 99% in Physics and stood first among all students in the state of Tamil Nadu in these subjects. He also participated in the Indian National Math Olympiad in the year 1996.

In September 1997, he joined the Indian Institute of Technology (IIT), Madras for undergraduate studies in Electrical Engineering after securing an All India Rank of 129 in the Joint Entrance Examination held for admissions to the IITs. During his time at IIT, he became interested in Solid-State and pursued his final year project investigating stacked silicon nitride/silicon dioxide layers as high-k dielectrics in CMOS. He graduated in July 2001 with a Bachelor of Technology degree in Electrical Engineering.

After spending 21 years of his life in Madras, India, he moved to Raleigh, USA to join the PhD program in the department of Electrical and Computer Engineering at North Carolina State University in August 2001. Since then, he has been working on hybrid silicon-molecular technology for applications in future-generation memory devices, under the guidance of Dr. Veena Misra. During the course of his graduate studies and research, he has acquired a strong understanding of CMOS technology and molecular electronics. He has authored and co-authored more than 15 papers in referred journals and conferences. He received the Best Student Paper Award at the IEEE NANO 2005, the 5th IEEE conference on Nanotechnology, held in Nagoya, Japan, during July 11-15 2005. He also received the Best Presentation award at the ECE GSA seminar event held in Fall 2005 at NCSU. He will be receiving his Doctor of Philosophy degree in Electrical Engineering in December 2005. He will start his post-student phase of life as a Process Integration Engineer at Texas Instruments, Dallas, where he'll be working on 65-nm and 32-nm CMOS technologies.

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1. INTRODUCTION

1.1 Past, Present and Future of CMOS

Scaling of CMOS technology for the last 4 decades has seen the minimum feature size of a MOSFET decrease from 10 μm in 1971 to a predicted 45 nm in 2009. In order to sustain this scaling trend to and beyond the end of CMOS, there have been intensive research activities on two highly challenging thrusts. One is in creating non-classical CMOS technologies to extend the realm of CMOS to the 45 nm node. The other is in creating new technologies, which rely on electronics at the level of individual atoms and molecules. The era of microelectronics has led us into an era of “nanotechnology”, which refers to the creation of materials, structures and devices by manipulating individual atoms and molecules.

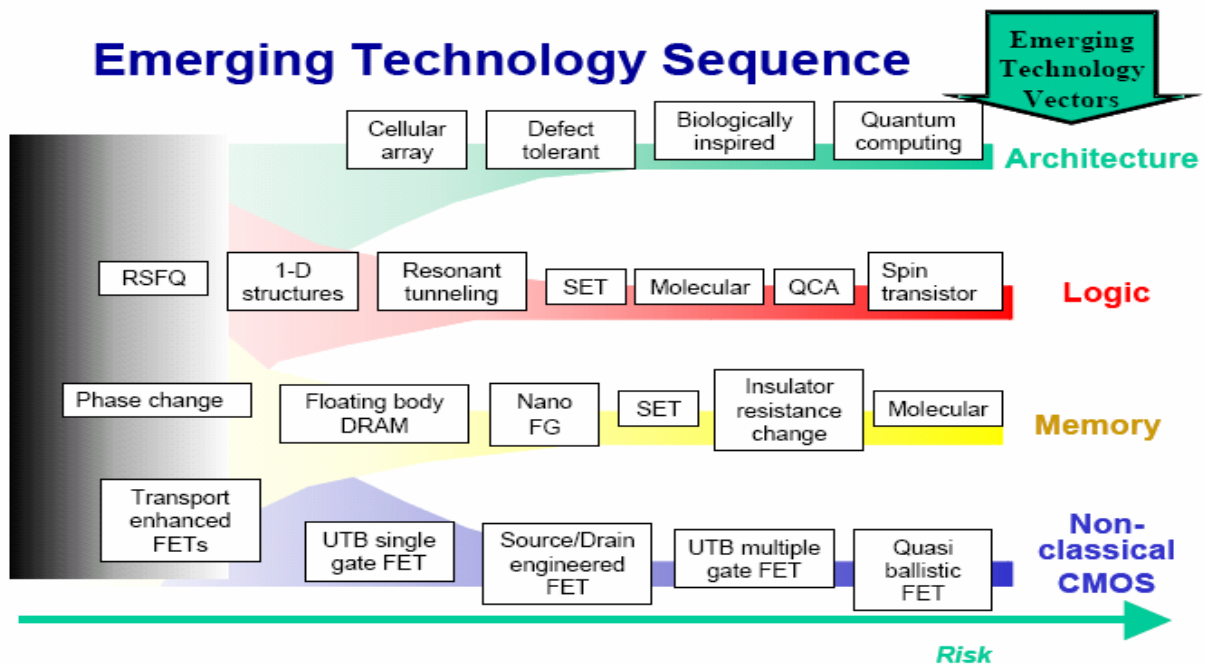


Figure 1.1 ITRS Emerging Technology Sequence

Fig. 1.1 shows the ITRS' emerging technology sequence for various technology vectors [1], listing the different technologies in the order of their risk factors. Non-classical CMOS, which includes advanced MOSFETs with new transistor structural designs and new materials, is tipped to extend CMOS until the end of the Roadmap. Some of these non-classical CMOS technologies are

- (i) *Transport enhanced FETs* – strained Si or other semiconductor channel for increased mobilities and drive currents [2, 3].
- (ii) *Fully depleted SOI* – Si-on-insulator instead of the conventional bulk Si, which can lead to improved transistor characteristics [4, 5].

(iii) *Schottky source, drain barrier* – to decrease source and drain resistances [6].

(iv) *Multiple gated FinFETs* – higher drive currents, improved short channel effect and potential for 3D integration [7-9].

These technologies, coupled with the development of immersion lithography [10], can extend CMOS beyond the 32 nm node. But fundamental thermal, quantum and power dissipation limits are expected to be reached with further scaling [11]. This leads to the evolution of new technologies that utilize quantum effects, single electron transport and intramolecular nanoelectronics. Fig. 1.1 also lists the various emerging technologies for logic and memory devices. Although these new technologies may not involve bulk Si, it would still be preferable for them to be compatible with CMOS, which has been the workhorse of the electronics industry more than 30 years. The enormous infrastructure and knowledge base in CMOS technology, along with its numerous applications, make it irreplaceable in the foreseeable future.

1.2 Non-molecular Emerging Technologies

1.2.1 1D Structures

One-dimensional device structures include devices such as carbon nanotubes (CNT) and nanowires (NW) where energy quantization occurs in one dimension. The major advantage that these devices provide is enhanced mobility compared to bulk Si due to ballistic electron transport, which may lead to faster transistors. Ballistic transport refers to the transport mechanism where the mean free path of charge carriers is longer due to fewer collisions, which leads to increased mobility. Some of the devices demonstrated using these structures include CNTFETs [12], semiconductor NW FETs [13], NW heterostructures [14] and crossbar nanostructures [15].

CNTs are hollow tube-like structures of carbon, which can be thought of as graphite sheets rolled into cylinders. The diameter of these tubes can be as low as 1 nm. CNTs can be either metallic or semiconducting with bandgaps varying from 0 to 1.1 eV depending on the chirality of the nanotube. The semiconducting nanotubes can be doped p-type or n-type. These structures offer the possibility of creating metal-semiconductor and semiconductor-semiconductor junctions at the nanoscale. Some logic devices have been demonstrated using CNTs [16]. There have also been efforts to create n- and p- CNTFETs via chemical doping of the nanotubes and Schottky drain and source junctions, which result in very high I_{ON}/I_{OFF} ratios [17]. Further, CNTs have also shown promise in the field of imaging, interconnects and sensing [18-20].

NW FETs can either be a device with the channel made out of a semiconductor NW or a crossover of two NWs with an insulator in between. In the latter case, one of the NWs will be semiconducting while the other will be metallic. Some of the demonstrated NW FETs show I_{ON}/I_{OFF} ratios of 10^4 to 10^5 [13].

There are numerous challenges in realizing 1D structures into manufacturability. Repeatable and controlled growth, alignment and doping of CNTs and NWs have yet to be achieved. Another major challenge is in making contacts to these 1D structures. Although the electron transport maybe ballistic in the nanostructures, they might be limited by the transport across the electrical contacts.

1.2.2 Spintronics, Single Electronics and Quantum Devices

Spintronics is the field of electronics that involved devices made using the spin properties of electrons (or any other particle, for that matter) instead of conventional charge-based devices. In this class of devices, information is encoded in the spin state of the particle. One of the main advantages of spin-based devices is their low power operation. Since spin devices do not involve the movement of charges for storage or transport of information, in theory, it is possible to make logic and memory devices that consume extremely low power. Spintronic analogs of conventional FETs and bipolar junction transistors (BJTs) have been demonstrated [21, 22]. But, even in an ideal scenario, these may not perform any better than conventional charge-based transistors [23].

Another application of spin is in the field of quantum computing, where spin (instead of charge) is used to encode logic 0 and 1. A quantum bit or “qubit” is a superposition of the classical bits 0 and 1. Hence, computational prowess can be enhanced exponentially because N qubits can store 2^N numbers at a given time. The most important applications of quantum computing are in the fields of cryptography and algorithms for problem solving. However, this concept does not have any impact in memories.

Single Electronics is the class of logic and memory devices that function at the precision of single to few electrons. The main advantages are low power and high density. In memory devices, small 3D islands or “quantum dots” are used to store one to few electrons. In these confined spaces, electrons can only occupy discrete energy states and are electrostatically confined in all three dimensions. Electrons can tunnel to and from these quantum dots one by one through tunneling barriers and is controlled by the “Coulomb blockade” effect. Some concepts of single electron memories have been experimentally demonstrated at cryogenic temperatures [24, 25].

The basis of single electron memories is the Single Electron Transistor (SET), which can also be used in logic devices. It consists of a quantum dot sandwiched between two electron sinks separated by tunneling barriers. Electrons are transferred between the source and drain one by one through the quantum dot and are controlled by a gate electrode. Since the quantum dot acts as the channel, the transistor is much smaller (~ 2 nm) than a conventional FET.

Quantum mechanics also finds its application in another set of logic devices known as Rapid Single Flux Quantum (RSFQ) logic [26], which are based upon a superconducting quantum effect. The storage and transmission of flux quanta (Fluxons) in a superconducting inductive loop defines the device operation. The basic cell consists of a superconducting ring with a Josephson Junction (JJ)

along with an external resistance. The primary advantage of this class of devices is the ability to perform at speeds of up to 800 GHz.

All these above mentioned technologies require extremely low cryogenic temperatures. Most of the practical devices demonstrated using these techniques are at temperatures below 20 K. Hence, room temperature operation and cost are big challenges in implementing these technologies. Another significant barrier is in developing new materials to fabricate these novel devices.

1.2.3 Emerging Memory Devices

Among emerging memory devices, Phase Change Memory (PCM), also called Ovonic Unified Memory (OUM) [27], is predicted to be the earliest to get into manufacturability (Table 1.1). Currently in the development stage, this technology utilized the rapid reversible phase changes in some materials under applied electric currents. Chalcogenides are the most commonly used material for these devices. They change their phase from crystalline to amorphous under an applied current pulse through a MOSFET, which in turn changes the resistivity of the material. Speed, scalability, multiple-bit and non-volatility are some of the key advantages of this technology. However, the programming currents required are fairly high (lowest reported is 0.1 mA/device), thereby limiting the size of the MOSFET required to apply the current pulses [28].

Floating body DRAM and nano-floating gate memory are the other technologies which may come into the memory market in the next few years. The former is a capacitor-less 1-transistor DRAM architecture, which stores data by charging the body of the transistor, thereby enabling very high density [29-31]. The latter is a slight modification of conventional floating gate memory (or FLASH memory) where data is now stored in nanocrystals instead of a continuous film [32]. This can significantly improve the endurance and retention of the memory cells.

Table 1.1 Summary of various emerging memory technologies

Storage Mechanism	PCM	Floating body DRAM	Nano-floating gate memory	Single Electron Memories	Insulator Resistance Change Memories	Molecular Memories
Device type	OUM	1TDRAM	Nanocrystal	SET	MIM	Stable states
Availability	2006	~ 2006	> 2006	> 2007	~ 2010	> 2010
Maturity	Development	Demonstrated	Research	Research	Research	Research
Non-volatility	Non-volatile	Volatile	Non-volatile	Volatile	Volatile	Depends

Another non-molecular approach to memory that is still in its early research stage is the Insulator Resistance Change Memory, where a metal-insulator-metal structure is used and the change in resistance of the insulator under applied voltages [33]. This technology offers low operating voltages

and multiple-bit capabilities. The main challenge in this technology is in the development of new materials and integration.

Table 1.1 gives a summary of the various emerging memory technologies and their projected availability dates. This table has been adapted from the ITRS Roadmap for Semiconductors.

1.3 Molecular Electronics

The founding of the field of molecular electronics is widely believed to have occurred when Aviram and Ratner proposed a rectifier using a single organic molecule in 1974 [34]. They theoretically calculated and demonstrated that the current-voltage characteristics of a molecule consisting of a donor pi system and an acceptor pi system, separated by a sigma-bonded tunneling bridge, behaved like a rectifying diode similar to a semiconductor p-n junction. Ever since their pioneering work, there have been numerous research efforts in creating molecular devices for logic and memory applications and understanding the properties of individual organic molecules under applied electric fields. These properties include electron transport, charge storage, structural changes etc. In order to understand these properties, it is useful to learn about molecular orbitals, chemical bonds and electron sharing. A brief review is provided below. Extensive discussions of these topics are available in references [35-37].

1.3.1 Molecular Orbital (MO) Theory

When atoms come together to form molecules, the atomic orbitals (AOs) of individual atoms overlap with one another to create molecular orbitals (MOs). Like AOs are regions of space around an atom where electrons can be found, MOs are regions of space around a molecule. A MO belongs to all the atoms whose AOs combine to form the MO. The number of MOs formed is equal to the number of AOs overlapping. Thus, a MO can be described by the linear combination of atomic orbitals (LCAO). When AOs overlap, the interaction between the orbitals can either be in-phase, which leads to a bonding interaction, or out-of-phase, which results in a node between the nuclei of the atoms. MOs can either be bonding or antibonding depending on the number of bonding interactions and nodes. A MO is bonding if the number of bonding interactions is greater than the number of nodes, and a MO is antibonding if the number of bonding interactions is fewer than the number of nodes. Typically, bonding MOs have lower energies than the AOs, whereas antibonding MOs have higher energies compared to that of the AOs. The aufbau principle, the Pauli exclusion principle and Hund's rule are followed when electrons occupy MOs. The aufbau principle states that electrons fill orbitals starting at the lowest available energy states before filling higher states. Pauli exclusion principle, which states that no two identical fermions can occupy the same quantum state, limits the number of electrons that can occupy an orbital to two. Hund's rule states that a greater spin state makes the resulting atom or molecule more stable. The filled MO with maximum energy is termed as the Highest Occupied Molecular Orbital (HOMO) and the empty MO with least energy is

called the Lowest Unoccupied Molecular Orbital (LUMO). MO theory is very useful in explaining resonance structures, understanding the structures and stability of aromatic compounds (benzene being a prime example) and also in calculating the discrete electron energy levels in organic molecules. The basis of this theory is quantum mechanics and the Schrodinger's equation.

1.3.2 Sigma (σ) Bond

When two AOs overlap end-to-end, the resulting bond is called a σ bond and the MOs are called σ bonding and antibonding MOs. In organic molecules, σ bonds are formed by the overlap of 2 sp_n hybridized AOs or an sp^n hybridized orbital and an s orbital or 2 s orbitals. Two electrons, one from each of the 2 overlapping atoms, are shared between the atoms and occupy the bonding MOs. These electrons are symmetrically distributed about the internuclear axis and are shared equally between the bonding atoms. Fig. 1.2 depicts the formation of σ MOs from two s atomic orbitals. Fig. 1.4 shows the formation of a σ bond between two sp^2 hybridized carbon atoms. All single bonds in organic compounds are σ bonds. Alkanes are a class of compounds which consist of only C-C and C-H σ bonds. Due to the equal sharing of electrons in all the bonds, none of the atoms in an alkane have any significant charge. This means they neither accept nor donate electrons inter- or intramolecularly. From a MO point of view, the σ bonding orbital is too low in energy for the bond to function as an electron donor to unoccupied orbitals. Likewise, the antibonding orbital is too high in energy to function as an electron acceptor from occupied orbitals. Consequently, alkanes, or even a section of an organic molecule with only σ bonds, behave like electrical insulators. The separation between the bonding and antibonding σ is large, analogous to a large bandgap in an insulator. There are exceptions to σ bonds being neither donors nor acceptors when there are substituents present adjacent to the bonds. These substituents can either raise the energy of the bonding MO or lower the energy of the antibonding MO, thereby facilitating interactions with other occupied or unoccupied MOs.

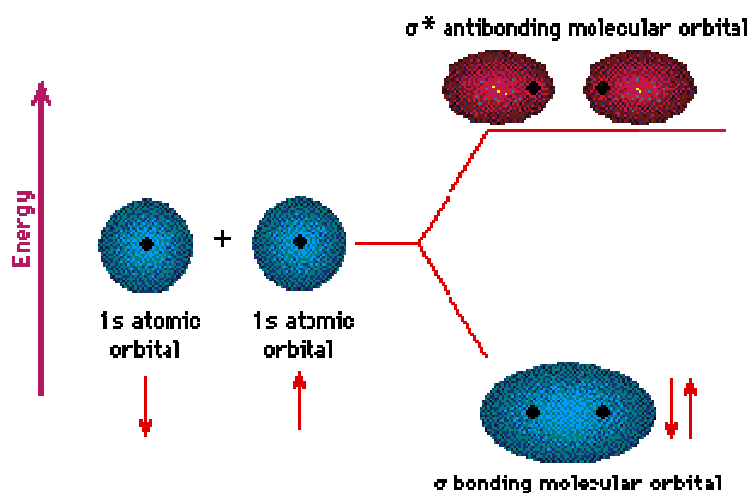


Figure 1.2 Formation of σ molecular orbitals from two s atomic orbitals

1.3.3 Pi (π) Bond

Bonds resulting from side-to-side overlap of two or more p AOs are called π bonds. In-phase overlap leads to π bonding MOs, while out-of-phase overlap leads to π antibonding MOs. A π bond is not spherically symmetric – the maximum probability of finding an electron is on either side of the internuclear axis. Unlike the σ bond which is formed by the overlap of only two AOs (and hence two atoms), the π bonds could be formed by the overlap of any number of p AOs, as shown in Fig. 1.3. Fig. 1.4 also shows the formation of a π bond by overlap of p orbitals of two sp^2 hybridized carbon atoms. When more than two p AOs overlap to form π MOs, the electrons from all the p orbitals become delocalized among the resulting MOs. In other words, all the p electrons involved in the overlap are shared between all the atoms involved in the overlap. This delocalization of π electrons is the reason for unusual stabilities among some organic molecules. For example, benzene has a six-carbon ring like structure with six π electrons delocalized among the six carbon atoms. Each carbon atom is σ bonded to two adjacent carbon atoms to form a planar ring and the six π electrons are delocalized above and below this planar structure. Benzene like compounds, with a planar ring and an odd number of pairs of π electrons are called aromatic compounds. These compounds are very stable because they have completely filled π bonding MOs and completely empty π antibonding MOs. π bonds are also found in other non-aromatic compounds in the form of double bonds and triple bonds. π bonds, due to the presence of π electrons above and below the internuclear axis, attract electrophiles (Y^+) and are hence very reactive.

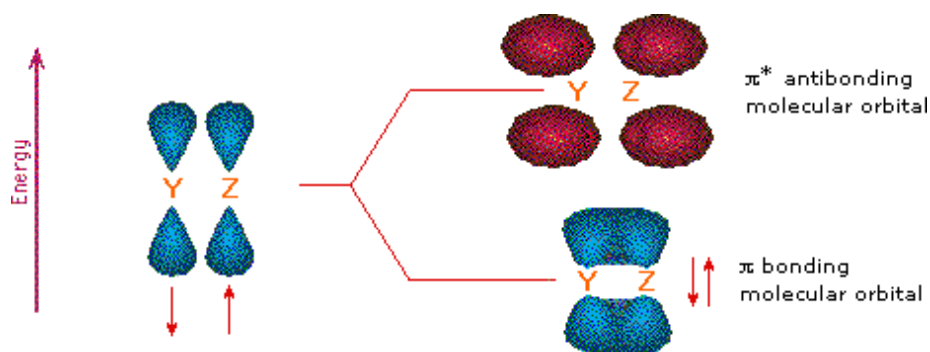


Figure 1.3 Formation of π molecular orbitals from two p atomic orbitals

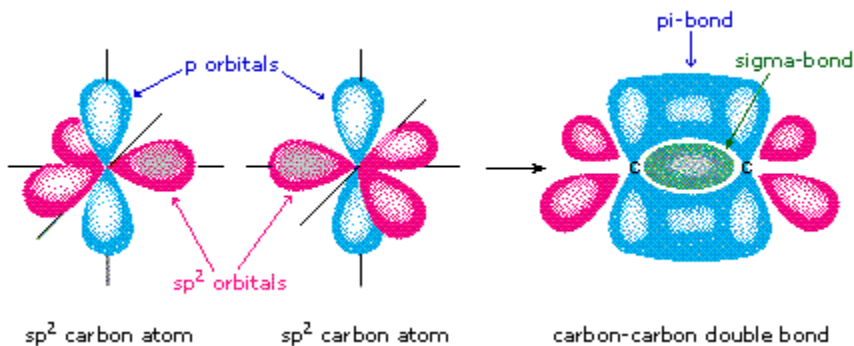


Figure 1.4 Formation of σ and π bonds between two sp^2 hybridized carbon atoms

1.3.4 Conjugated Systems

Conjugated molecules are planar organic molecules which consist alternate π and σ bonds (double and single bonds). 1, 3, 5 – hexatriene, benzene and other aromatic compounds are some examples. The chemical structure of benzene is shown in Fig. 1.5. The left structure shows alternating σ and π bonds, which is one of the resonance structures of benzene. The structure to the right in Fig. 1.5 shows delocalization of the three π bonds among the six carbon atoms. In such systems, all the π electrons involved in conjugation are delocalized in a vast MO made out of inter-overlapping AOs which cover the entire molecular framework. This leads to a strong electronic “coupling” between the atoms of the conjugated chain. Furthermore, conjugation raises the energy of the HOMO and lowers the energy of the LUMO, thereby decreasing the “bandgap” within the molecule. Hence, conjugated organic molecules do not behave like insulators, but instead strongly aid electronic conduction. In other words, electrical influences are easily propagated from one part of the molecule to another.



Figure 1.5 Structure of benzene showing (a) alternating σ and π bonds, and (b) delocalization of the three π bonds among the six carbon atoms

1.4 Molecular Logic and Memory Devices

As Fig. 1.1 and Table 1.1 suggest, molecule-based technologies for emerging logic and memory devices are still in the early research stage and are currently categorized as “risky” options by the ITRS. However, since the theoretical demonstration of a rectifier using a single organic molecule in 1974, there have been many significant developments in the field of molecular electronics, particularly in trying to developing molecular devices and characterizing them. But, the physics of molecular devices and the specific role played by molecules have yet to be understood well. Another big challenge is in making microscale solid state contacts to these nano-sized molecules. This section outlines some of the recent works in the field of molecular electronics. The challenges in this field are detailed in the following section.

1.4.1 Metal-molecule-metal Approaches

The most common approach in this field to date has been the metal-molecule-metal approach [38-42]. This approach relies on a change in conductance of organic molecules placed between two metal electrodes under applied electric fields. In memory devices, high and low resistance values of molecules are used as the erased and programmed states [39]. One approach to logic devices is to employ molecules with two conductance states at the junctions of a crossbar array, along with a defect-tolerant architecture [40]. This approach involves a simple architecture and also has the advantage of scalability to very high densities. Another approach is to use molecules that have shown

negative differential resistance (NDR) to connect metal nanostructures in a random array [41]. Sophisticated algorithms are then used to identify which nanostructures are connected and program the cells to desired functionalities. In all of these approaches, the organic molecules are covalently bonded to the bottom metal electrode via self-assembly and the top metal electrode is evaporated on the molecules, which typically does not result in the formation of covalent bonds. One such example is shown in Fig. 1.6, where the molecule is sandwiched between two gold electrodes. The molecule is covalently linked to the bottom electrode via sulfur, whereas the top electrode does not form any covalent bonds. The absence of covalent bonds between metal and molecules results in variations in the metal-molecule interface from device to device. This may lead to a large variation in the electrical characteristics from one device to another. Some of the proposed explanations for the change in conductance and NDR behavior have been (i) presence of a metastable state in the molecules, (ii) reversible structural change in the molecules or (iii) reconfiguration of the molecular components. However, none of these have been verified yet. Recent reports also indicate that some of the switching behaviors are molecule-independent and can be hugely dependent on the top metal electrode [43, 44]. Consequently, the knowledge base of these devices needs further work [45].

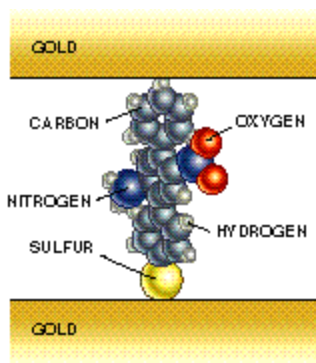


Figure 1.6 Schematic of a metal-molecule-metal structure. The molecule is covalently linked to the bottom gold substrate via sulfur, whereas the top contact does not have any covalent linkages.

1.4.2 Molecular Quantum Cellular Automata (QCA)

In the QCA paradigm, four quantum dots or individual molecules are placed at four corners of a square-type geometry [46-49]. Each square constitutes a cell and contains two electrons, which occupy the diagonal molecular elements due to electrostatic repulsion. Two states, coded as logic '0' and '1' are possible depending on which diagonal is occupied. The molecules used in this technology must be capable of reversibly tunneling an electron. Many QCA cells can be placed next to each other to create logic devices. The alignment of electrons in these cells is governed by Coulombic forces between adjacent cells, and not wires. Hence, there is negligible power consumption. The main drawback arises from the fact that these devices depend on tunneling of single electron per molecules. Therefore, background charge is a big issue and hence only very low operation temperatures have been demonstrated. Furthermore, the intermolecular distance in a cell needs to be precise and requires exact positioning of the molecules.

1.4.3 Hybrid Si-Molecular Devices

Hybrid Si-molecular approach refers to the incorporation of organic molecules on a Si platform to create logic and memory devices [50-54]. One such approach is for memory applications proposed by scientists at NCSU and University of California, Riverside, where monolayers of redox-active molecules are formed on Si or SiO₂ and the multiple stable charged states of the molecules are utilized to store information [50-52]. Fig. 1.7 shows a schematic representation of incorporating organic molecules on a silicon platform to create hybrid silicon-molecular devices. These devices can be used for DRAM and Flash type memories. The memory cell is written by oxidizing the molecules (removing electrons) at appropriate voltages, thereby creating a positively charged layer. A reducing voltage results in electrons tunneling back into the molecules, bringing them back to their neutral state (erase). A written memory cell can be read in two ways: (i) applying a reducing voltage and monitoring the current – destructive read for DRAM applications; (ii) monitoring the change in transistor characteristics when these molecules are incorporated in FETs – non-destructive read for Flash applications. The advantages and challenges of this approach are discussed in the next section.

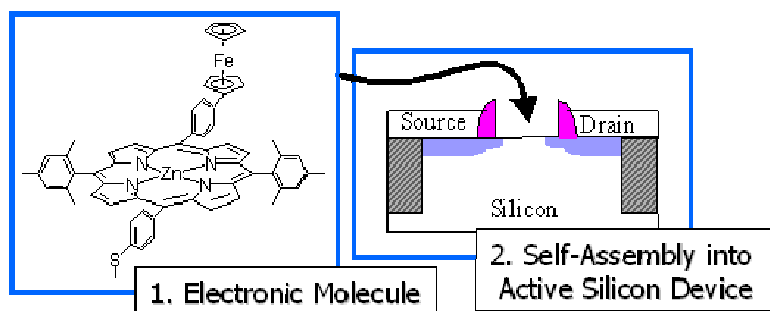


Figure 1.7 Schematic showing the incorporation of organic molecules in a silicon platform to create hybrid silicon-molecular devices

There have also been some other reports on metal-molecule-semiconductor devices [55, 56], that try to utilize the properties of the semiconductor to modulate the electronic properties of the molecules. Some groups have also tried to incorporate molecules in NW FETs to modulate the characteristics of the FETs [57]. The surface potentials created by the incorporation of molecules seem to affect the FET characteristics, but this reasoning is not very clear. Organic molecules have also been used to create insulating monolayers for applications in organic TFTs [58, 59].

1.4.4 Theoretical Modeling and Simulations

The core of modeling and simulations for molecular devices is quantum mechanics. It involves solving the Schrodinger's equation to find the discrete energy levels of MOs in the organic molecules. Since the number of atoms and electrons involved in the Schrödinger's equation is quite large, exact mathematical solutions are impossible. However, numerical approximations and simulations can be performed to get an approximate model for the molecules. Modeling the electron transport in molecules under applied electric fields is an even harder task. Nevertheless, there have been many

reports on modeling and simulations for molecular devices, transport through molecules, molecular transistor etc. [60-64].

1.5 Advantages and Challenges of Hybrid Silicon-Molecular Memories

1.5.1 Advantages

The CMOS industry has invested billions of dollars in developing an infrastructure to make silicon based electronic devices. At this point, it is difficult to envision a new technology completely replacing silicon and making CMOS obsolete. Mankind might get there in a few decades, when all electronic devices will probably be made out of individual molecules and atoms, but in the meantime, a hybrid silicon-molecular technology may prove useful in extending the life of CMOS. Some of the key advantages of this technology are listed below:

1. Easy integration with existing fabrication process – the number of additional steps involved in incorporating organic molecules on a silicon platform may be minimal. Molecular monoayers can be easily self-assembled on a variety of different substrates, including silicon, dielectrics and metal, by functionalizing them with appropriate linkers [65, 66].
2. Synthetic tailorability of molecules – organic molecules with up to 8 multiple stable redox states have been synthesized [67], which can provide multiple bits in a single memory cell. Furthermore, the write/erase voltages and retention times can be tailored by varying the tethers attached to the end of the molecules.
3. Discrete energy levels – the discrete nature of the MOs are preserved in a monolayer of molecules, resulting in discrete electronic states within the monolayer that electrons can tunnel to and from. Hence, the amount of charge stored will only depend on the number of molecules and not on the applied voltage.
4. Engineering the substrate and surface – the write/erase voltages and retention times can also be tuned by varying the properties of silicon and silicon dioxide that the molecules are attached to. This can also lead to novel functionalities [68].

1.5.2 Challenges

The main challenges in this field are:

1. Stability of molecules – organic molecules need to be stable at elevated temperatures of at least 400 °C in order to be able to integrate with the existing CMOS technology. The porphyrin molecules have shown stable behavior even after being exposed to 450 °C [69], so there are reasons to believe that this challenge can be overcome. The stability of linkers and tethers that covalently bond molecules to substrates, and the role of contaminants, moisture and oxygen in stability of molecules are some other stability issues that need to be addressed.

2. Reliability and endurance under electrical stress – this is an unknown quantity in this field, and there aren't many demonstrations of molecular stability after millions of cycles.
3. Contact engineering – although there have been demonstrations of metal evaporation directly on molecules, it is still unclear whether the inherent molecular properties are retained after metal deposition.
4. Characterization techniques – there is need to identify efficient techniques or develop new techniques to characterize hybrid silicon-molecular devices.

In order to overcome all the challenges and utilize all the advantages that this field offers, it is essential to fabricate, characterize and understand the physics of these devices with an engineering rigor.

1.6 Focus of my research

My research focuses on fabricating hybrid silicon-molecular memory devices with monolayers and polymers of redox-active ferrocenes and zinc porphyrins on silicon and silicon dioxide surfaces, characterizing these devices using a variety of techniques and studying the device physics. Particularly, the role played by silicon doping type and density, minority carriers in silicon and the oxide thickness on the write/erase voltages and retention properties of these devices are analyzed in detail. Furthermore, an attempt to eliminate the liquid electrolyte and create a complete solid-state hybrid device has also been investigated.

1.7 Dissertation Overview

This dissertation is divided into six chapters, excluding 'Introduction'. The next chapter is "Experimental and Characterization", which details the experimental procedures and characterization techniques employed in this research. It also discusses the various organic molecules used in this study. This is followed by a chapter on "Molecules on Si", which describes the role of silicon doping type and density on the device characteristics. The chapter on "Molecules on SiO₂" is a detailed study of the memory properties of hybrid silicon-molecular devices. A chapter on solid State approach to molecular electronics follows, which presents the results from the attempts to create a complete solid-state hybrid device. The final chapter titled "Outlook" summarizes the dissertation and discusses the road that lies ahead in this field.

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2. MOLECULES, EXPERIMENTAL AND CHARACTERIZATION

This research involves the incorporation of redox-active organic molecules on silicon and silicon dioxide surfaces. [An organic molecule is termed redox-active if it is capable of reversibly losing and gaining electron(s) and remaining stable in its neutral and charged states.] For this purpose, a variety of different organic compounds have been synthesized [1-10]. These compounds can exist in at least two stable states (neutral and cationic), with some molecules capable of exhibiting up to 8 different redox states. The compounds are functionalized with tethers and linkers for attachment to silicon and silicon dioxide surfaces via covalent bonds. This chapter lists the various compounds used in this study along with their properties. The attachment procedures, the fabrication of test structures and their electrical characterization techniques are also discussed.

2.1 Redox-active Organic Compounds

The two basic classes of molecules used in this study are ferrocenes and metalloporphyrins. Typically, a redox-active compound consists of a charge storage group, a tether that may or may not be an insulating barrier, and a linker for covalent attachment to different electroactive surfaces. The charge storage group of the molecule shares its π electrons in π MOs. These redox-active molecules can lose electrons from their MOs, resulting in stable positively charged cations. Further, since MOs are discrete, quantized energy states, the voltages at which molecules oxidize (lose electron) are discrete too. This ability of these molecules to store positive charges has been utilized to create hybrid silicon-molecular memories where the organic molecules are the storage elements.

2.1.1 Two-state Molecules

The most commonly used molecules in this study are the ferrocenes (Fig. 2.1 a). Ferrocene, $\text{Fe}(\text{C}_5\text{H}_5)_2$, is an organometallic compound consisting of two cyclopentadienyl rings bound on opposite sides of a central iron atom. The π electrons of both the aromatic cyclopentadienyl rings are shared with the central iron ion. Ferrocene demonstrates reversible one-electron redox behavior, thus exhibiting two redox states. Both ferrocene (neutral) and ferrocenium ion (formed by oxidation – loss of electron – of ferrocene) are very stable in air. A substitution group can be introduced to the cyclopentadienyl rings, which are very reactive, enabling the attachment of ferrocenes to different surfaces via covalent bonds [1]. The stable redox property of ferrocenes and the ability to attach them to different surfaces make these molecules very attractive for investigating molecule-based memory devices.

2.1.2 Three-state Molecules

Three-state molecules used in this study are metalloporphyrins (Fig. 2.1 b). Porphyrin is an aromatic compound that combines readily with metals (Zn, Co, Cu etc.) to form metalloporphyrins,

which exhibit 3 stable redox states. For examples, a neutral zinc-porphyrin can lose one electron to form a stable monocation, and lose an additional electron to form a bication. Porphyrins, like ferrocenes, can also be functionalized with various tethers and linkers for attachment to different surfaces.

2.1.3 Multiple-state Molecules

Organic molecules with multiple states are attractive because of the opportunity they provide to create memory devices with more than 1 bit per cell, thereby increasing the memory density. Several such molecular architectures have been synthesized (Fig. 2.1 c, d & e). Typically, europium triple-decker sandwich molecules composed of porphyrins and phthalocyanines afford four cationic states and a larger number of states can be achieved by combinations of triple deckers that afford interleaved oxidation potentials [10]. The possibility of integrating multiple bits in a single cell is a significant advantage of molecular devices over conventional semiconductor and other memory technologies.

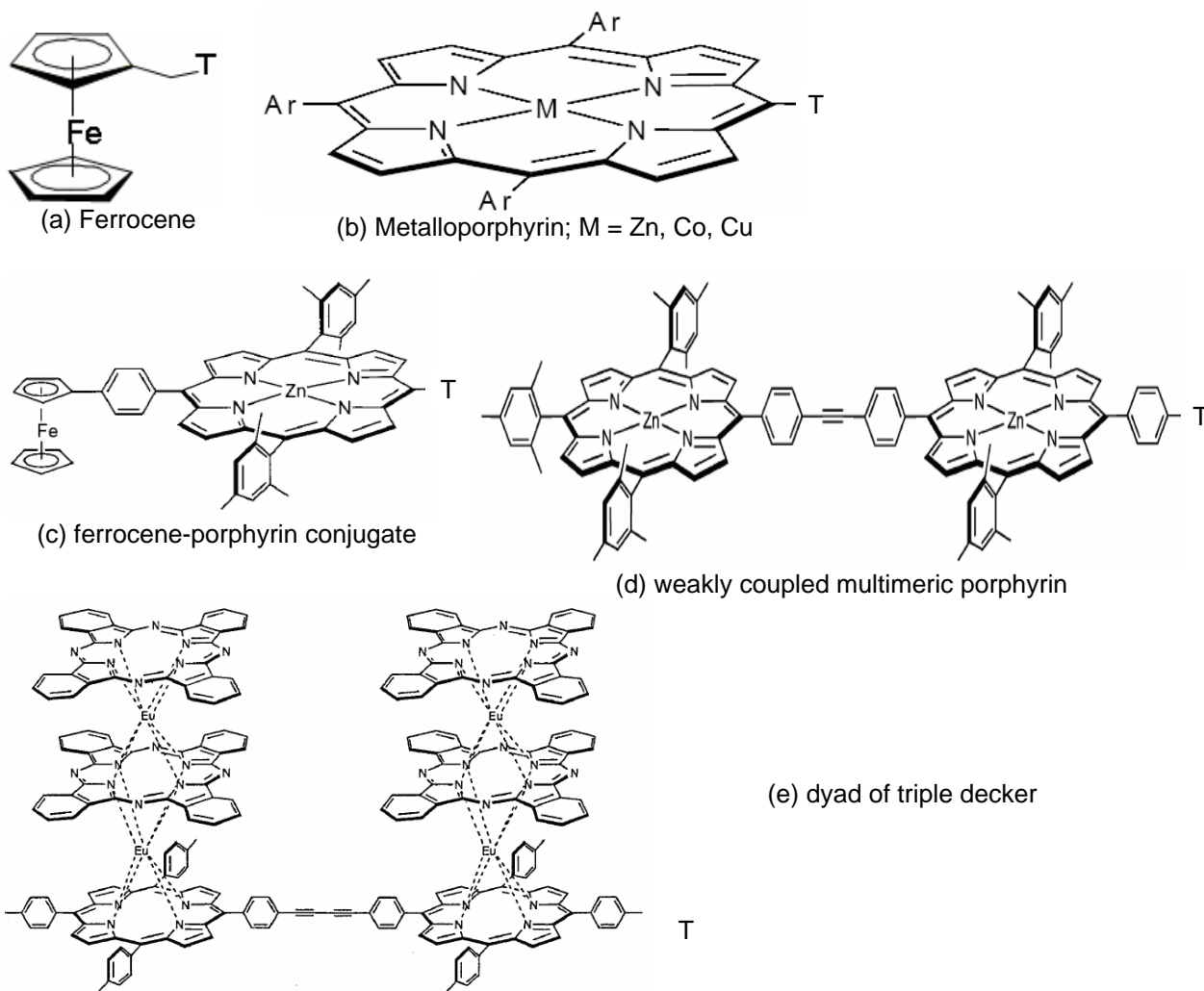


Figure 2.1 Chemical structures of redox-active organic molecules. T refers to tether and linker. See references [1-10].

2.2 Tethers and Linkers

As mentioned in the previous section, the redox-active organic molecules are functionalized with tethers and linkers for stable attachment to different surfaces via formation of covalent bonds between the molecules and the substrate. Fig. 2.2 shows various tethers and linkers that have been synthesized. In this work, the two commonly used linkers are (i) the alcohol linker (-OH) for attachment to silicon surfaces and (ii) the phosphonate linker (-P[11]₂O) for attachment to silicon dioxide surfaces. Self-assembled monolayers of molecules are formed on Si and SiO₂ surfaces via is strong covalent O-Si and P-O-Si bonds, respectively [12, 13]. While the O-Si bonds have shown to withstand temperatures as high as 450 °C [14], the P-O-Si bonds or the phosphonate linkers themselves may not be as robust. Covalent bonds between molecules and substrate are necessary in order to create strong chemical contacts. Without covalent bonds, the interface between molecules and the substrate may not be the same from device to device and from attachment to attachment.

The tether, which is the unit between the charge storage group and the linker, can be useful for tuning the redox voltages and charge retention times [15, 16]. A sigma bonded tether may act as an insulating barrier, thereby resulting in improved charge retention, at the expense of slower oxidation and reduction kinetics [15]. The length of the insulating tether can be varied to achieve a balance between speed and retention depending on the application. On the other hand, if the tether has π electrons, then that might change the redox potentials of the molecule, thereby enabling tuning of write/erase voltages.

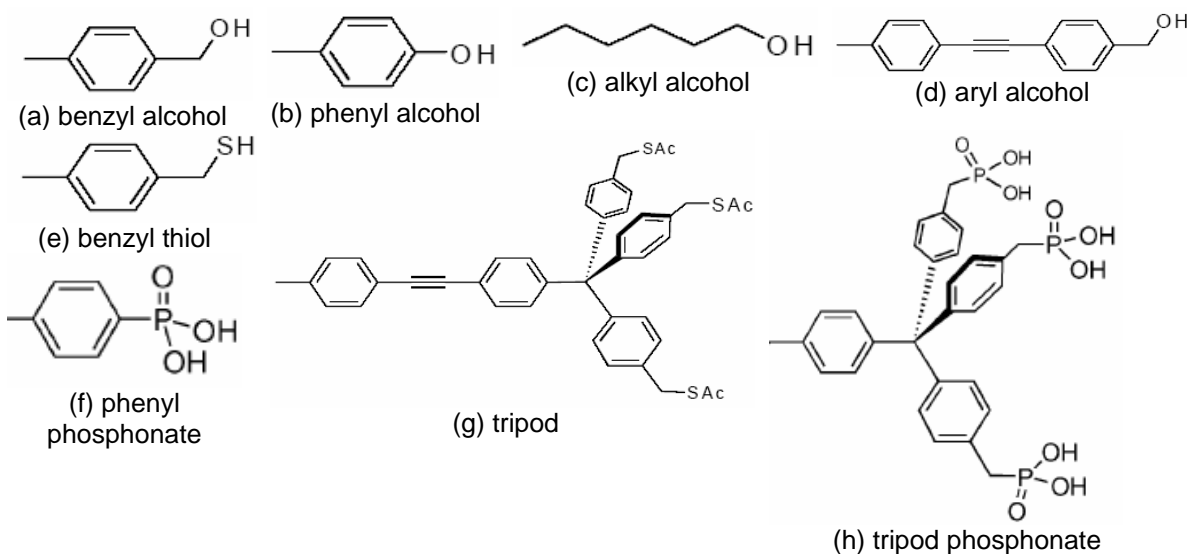


Figure 2.2 Chemical structures of linkers and tethers. (a), (b), (c) and (d) have alcohol linkers for attachment to Si. (f) and (h) have phosphonic acid linkers for attachment to SiO₂ surfaces.

2.3 Redox-active Polymer

Metalloporphyrin molecules have also been synthesized with acetylene groups at two ends (Fig. 2.3). These molecules polymerize when exposed to elevated temperatures, forming a cross-

linked chain of porphyrins covalently linked with each other. The attachment procedure of these molecules result in the formation of a polymer film wherein porphyrins are covalently bonded to one another and the base layer is covalently attached to silicon surfaces via carbosilane linkages [17]. However, they were not found to form covalent linkages to SiO₂ surfaces. The energy levels were found to be discrete in these polymer films, similar to their monolayer counterparts. Experimental results will be discussed in the next chapter.

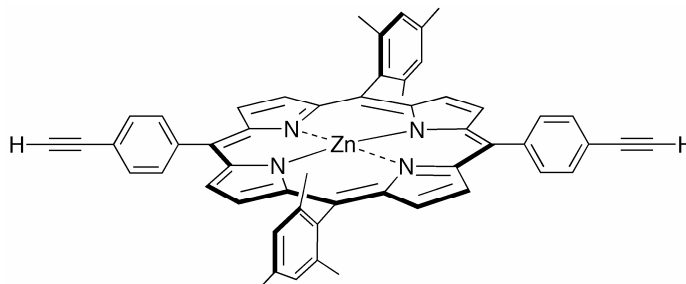


Figure 2.3 Metalloporphyrin with acetylene groups at two ends. This compound polymerizes at high temperatures.

2.4 Non-redox Control Compounds

In order to verify that the redox behavior of the molecules are indeed the reason for the molecular devices to exhibit memory properties, non-redox compounds were also employed for control experiments. Biphenyl molecules with alcohol, phosphonate and acetylene linkers have been synthesized for attachment to Si, SiO₂ and for formation of polymers, respectively. The chemical structures of these compounds are shown in Fig. 2.4.

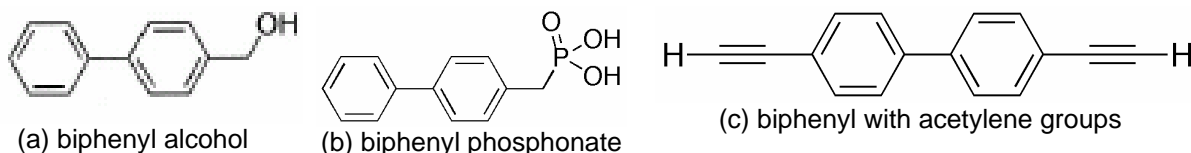


Figure 2.4 Chemical structures of non-redox control molecules for attachment to Si (a) and SiO₂ (b). (c) forms a polymer at high temperatures.

2.5 Test Structures and Devices

The primary applications for this hybrid silicon-molecular technology are DRAM and Flash memory devices. In DRAM, the conventional capacitor which stores charges can be replaced by a molecular capacitor. Unlike in a conventional transistor, the amount of charges stored in a molecular capacitor is dependent not on the applied voltage, but on the number of molecules. Discrete, multiple states accessible at low voltages can provide low power, high density DRAM chips. The inherent charge retention times of these organic molecules are of the order of a few seconds [18], thereby facilitating lesser number of refresh cycles. Also, the density of charges in a molecular capacitor is at least an order of magnitude greater than that possible using a conventional capacitor [12, 19]. For Flash applications, organic molecules have the potential to replace the floating gate as the charge storing element. Apart from all the above advantages, non-volatility may be achieved by engineering

the silicon substrate and silicon dioxide barrier. In order to understand the interaction of molecules with CMOS and study their memory properties, capacitor and FET test structures were fabricated.

2.5.1 EMS and EMOS Capacitors

Fig. 2.5 shows the schematic structures of electrolyte-molecule-Si (EMS) and electrolyte-molecules-oxide-Si (EMOS) capacitors. The process flow for fabricating these capacitors is shown in Fig. 2.6. Starting from a (100) oriented Si substrate (n- or p- type), conventional semiconductor fabrication techniques are employed to lithographically define active areas of sizes varying from 5×5 to $200 \times 200 \mu\text{m}^2$, isolated by a thermally grown 400 nm thick field SiO_2 . A thin sacrificial oxide of 150 nm is then grown in the active areas and etched using 1 % HF to create a highly passivated Si surface. Another oxidation step is used to grow a 150 nm thick gate oxide. This gate oxide is etched back using 1 % HF to obtain desired thicknesses just prior to molecular attachment, which is discussed in the next section. After molecular attachment, an electrolyte is used as a conducting gate for electrical measurements. The electrolyte area is confined by employing a micropipette tip filled with the electrolyte. Silver wire, which is used as the gate electrode, is immersed in the electrolyte, and the pipette tip is lowered until an electrolyte drop from within the pipette makes contact with the active area via capillary action. Choice of electrolyte, its properties and role in electrical measurements are discussed later in this chapter as well as in Chapter 6.

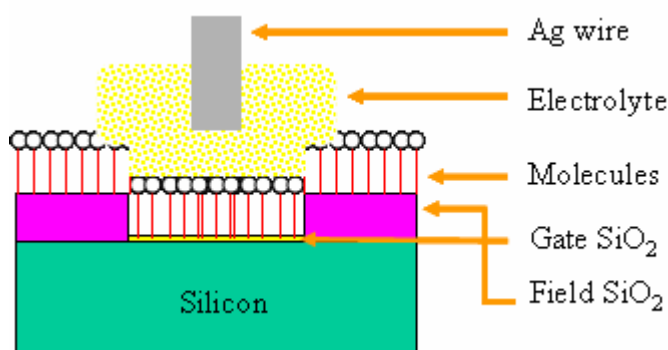


Figure 2.5 Schematic structure of EMS/EMOS capacitor. The thin gate SiO_2 (yellow) thickness was varied between 0 and 3 nm in this study. Electrolyte gate and silver wire gate electrode were used for electrical characterization. Molecules might be attached to the field SiO_2 as well, but they do not participate in electrical measurements.

2.5.2 MoleFET

In order to verify that organic molecules can indeed replace the floating gate in Flash memory devices, FET test structures were fabricated. A 5-level mask process using replacement gate technology was employed to fabricate these structures. Both PFETs and NFETs were fabricated with gate areas varying from 10×10 to $100 \times 100 \mu\text{m}^2$. The source and drain overlap regions varied between 2.5 and 5 μm . Contact metal pads to the source and drain regions were well separated from the gate region in order to facilitate electrical characterization using an electrolyte gate. Details about the layout of the masks and the processing steps involved in fabricating these FET structures will be

provided in another student's dissertation. Gate oxide, when needed, was thermally grown at low temperatures (400 °C). Organic molecules were attached to the gate regions to create molecular-FETs or "MoleFETs", which were characterized using an electrolyte gate.

Other test devices like back-gated MOSFETs, solid-state silicon-molecular hybrids etc., were also fabricated during this study. The fabrication process for these devices will be described as and when they are discussed in this dissertation.

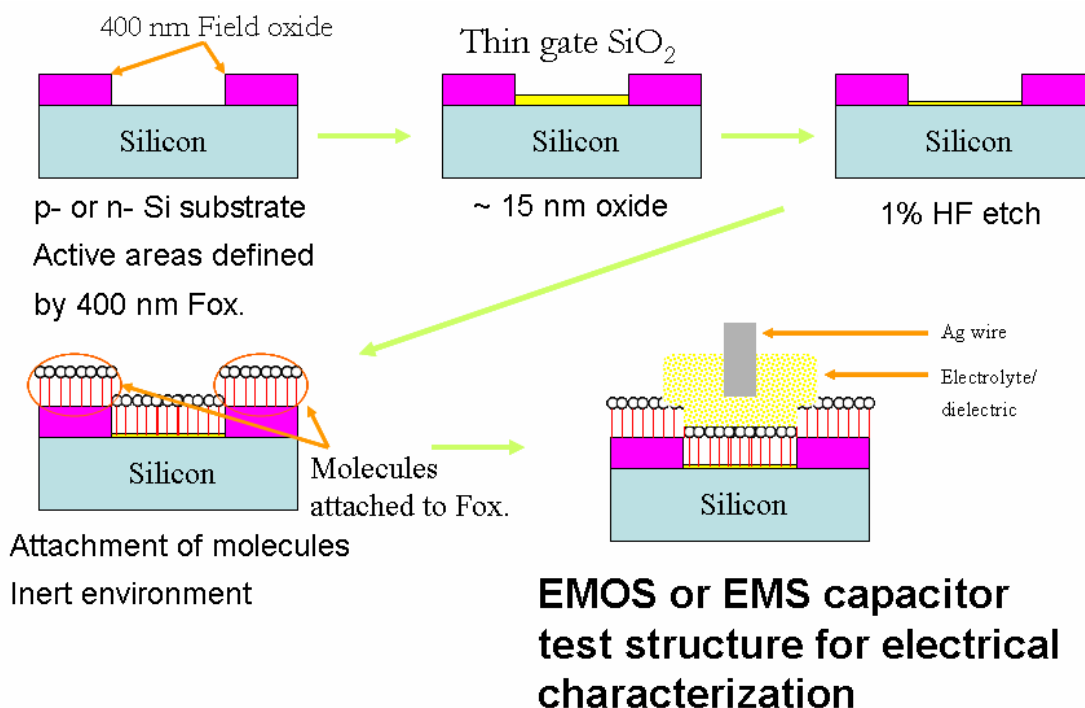


Figure 2.6 Process flow for fabricating EMS/EMOS capacitors.

2.6 Attachment Procedures

Prior to the attachment, the samples are etched in 1 % HF to obtain desired SiO₂ thickness or highly passivated Si surface. The samples are immediately transferred into vials, which are then sealed and purged with inert Argon. The samples remain in Ar purged environment throughout the attachment procedure. Fig. 2.7 shows the chemical structures of the most commonly used redox-active molecules, along with their tethers and linkers, in this study. **Fc-BzOH** and **Por-BzOH** are ferrocene and zinc-porphyrin molecules, respectively, functionalized with benzyl alcohol for attachment to Si surfaces. **Fc-P** and **Por-P** are ferrocene and zinc-porphyrin molecules functionalized with a phosphonate linker for attachment to SiO₂ surfaces. **Por-m** is zinc-porphyrin functionalized with acetylene on two ends. This molecule forms a polymer at high temperatures.

Self-assembled monolayers (SAM) of these molecules are formed on the samples via the use of chemical solutions. 1 mM solution of the desired compound is prepared in an organic solvent. The organic solvents that have been used are benzonitrile [BN], dimethylformamide [DMF] and tetrahydrofuran [THF]. A small quantity (4 μl) of the molecular solution is placed on the active areas of

the samples. Samples are maintained at elevated temperatures to initiate the formation of covalent bonds between the molecules and the surface. The number of drops and the time between drops required for the creation of a saturated monolayer have been optimized during earlier studies [20]. The samples are then rinsed and ultrasonicated in dichloromethane [DCM] (or THF) three times in order to remove any unattached molecules left behind on the surface. Table 2.1 summarizes the attachment procedures (solvents, temperatures, number of drops, time between drops etc.) used for different molecules.

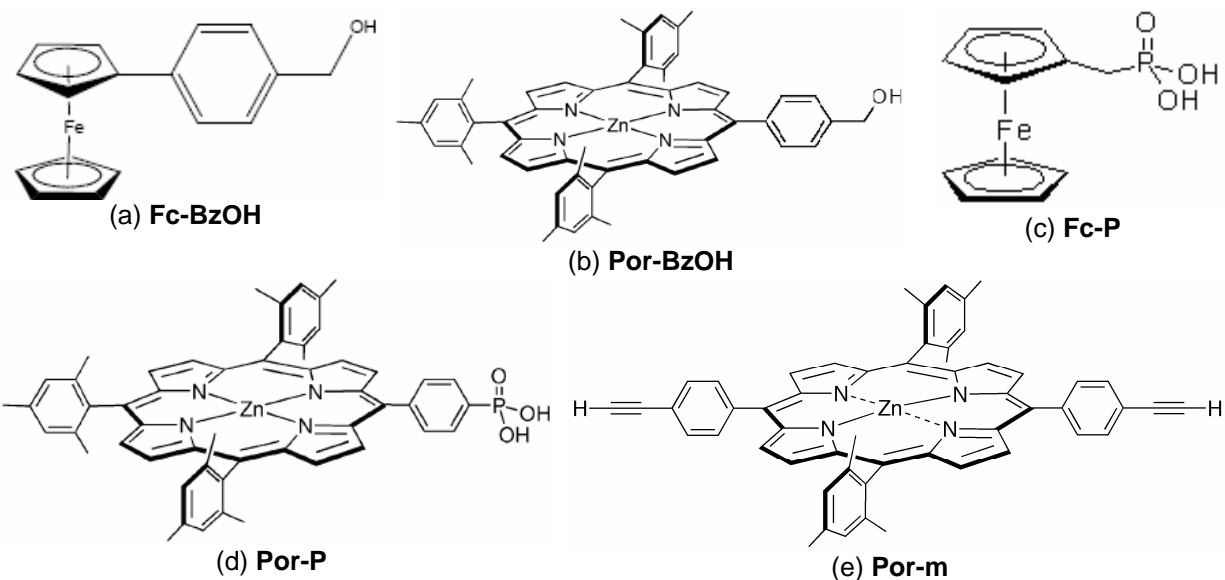


Figure 2.7 Chemical structures of the most commonly used redox-molecules in this study. **Fc-BzOH** and **Por-BzOH** attach to Si; **Fc-P** and **Por-P** attach to SiO₂; **Por-m** polymerizes at high temperatures.

Robust attachments to Si and SiO₂ surfaces are achieved via covalent bond formation, except in the case of **Por-m**. As mentioned earlier, these molecules do not have any functional groups to form covalent bonds with Si or SiO₂. Instead, the acetylene groups at 2 ends enable polymerization of the molecules to form a thin film of cross-linked polymer. The elevated temperature, in this case, is to initiate the polymerization reaction.

Table 2.1 Summary of attachment conditions for all the redox-molecules used in this study.

Molecule	Attachment surface	Solution & concentration	Attachment temperature	# drops	Time btn. Drops	Coverage (10 ¹⁴ /cm ²)
Fc-BzOH	Si	BN; 1 mM	80 °C	8	10 min.	1.5
Por-BzOH	Si	BN; 1 mM	170 °C	8	10 min.	0.45
Fc-P	SiO ₂	DMF; 1 mM	80 °C	8	10 min.	1.5
Por-P	SiO ₂	DMF/THF; 1 mM	200 °C	8	10 min.	0.45
Por-P	SiO ₂	DMF/THF; 1 mM	400 °C	1	2 min.	0.45
Por-m	Si, SiO ₂	THF; 0.1 – 1 mM	400 °C	1	2 min.	0.45 – 15

2.7 Electrical Characterization

For electrical characterization, a 1 M solution of tetrabutyl ammonium hexafluorophosphate (TBA-PF₆) in propylene carbonate (PC) was used as a conducting electrolyte gate. Silver wire was used as the gate electrode. This organic solvent electrolyte was chosen because of its inertness to the organic molecules, which are susceptible to moisture. The electrolyte also helps in the formation of a double layer capacitance at the interface between the electrolyte and the molecules. The PF₆⁻ ions in the electrolyte on the solution side of the double layer balance the positive charges created in the molecular monolayer. The electrolyte, the double layer and the role played by these in electrical measurements are discussed in more detail in Chapter 6. The electrical characterization techniques employed in this research are (i) cyclic voltammetry, (ii) impedance spectroscopy, (iii) charge retention measurements and (iv) MOSFET characterization. All electrical measurements were performed at room temperature.

2.7.1 Cyclic Voltammetry [21, 22]

Cyclic Voltammetry (CyV) is a reversible voltage-controlled experiment, where a dc voltage sweep is applied and the transient current is monitored. When the gate voltage is swept in the negative direction, the energy levels of the MOs of the molecules are raised and results in electron tunneling from the molecules to the Si substrate (oxidation) leaving behind a positively charged monolayer. The reverse process (reduction), where electrons tunnel back from Si to the molecules, happens during the reverse sweep when the gate voltage is brought back to the starting point. Fig. 2.8 shows a typical voltage sweep and the resulting current-voltage characteristics. The peaks in the current are associated with oxidation (negative current) and reduction (positive current) of the molecules. Key parameters involved in this technique are the starting voltage, scan rate and the voltage range. Observations that can be made from this technique are as follows:

1. Oxidation and reduction peak voltages – these give the write and erase voltages that need to be applied to a memory cell.
2. Area under the oxidation and reduction peaks – quantifies the density of molecules in the monolayer.
3. Peak separation – depicts the speed of electron-transfer to and from the molecules. This also portrays the read window available for a non-destructive read of the memory cell when employed as a Flash device. The separation between the charging and discharging peaks increase with increasing scan rates, indicating that input scan rate is becoming comparable to the electron-transfer rate. Peak separation can also arise due to series resistance present in the system.

4. Scan rate dependence – a linear dependence of the peak current on the scan rate indicates that the molecules are strongly adsorbed to the underlying substrate. The area under the peaks vs. scan rate can also give a picture of the speed of electron-transfer.

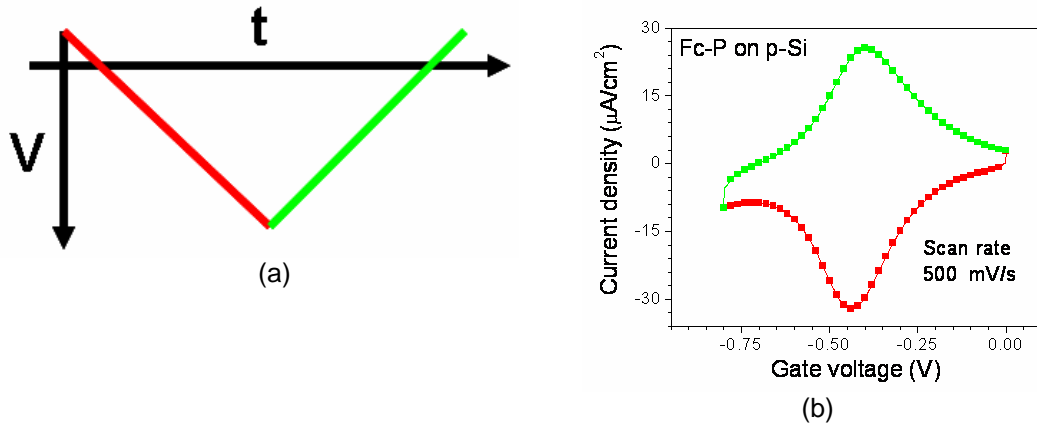


Figure 2.8 Typical voltage waveform (a) and current-voltage characteristics (b) in a cyclic voltammetry (CyV) experiment. The forward scan (red) represents oxidation (loss of electron from molecules) and the reverse scan (green) represents reduction (electron tunneling to the molecules).

The capacitances present in the system introduce a charging current in this type of measurement. Hence, to clearly see the effect of charging and discharging of molecules, the faradaic current needs to be much higher than the charging current. This is usually the case for the kind of densities that are dealt with in this study. Detailed theories about kinetics of electron transfer will be discussed in subsequent chapters. All the CyV measurements were made using a CHI600 electrochemical analyzer.

2.7.2 Impedance Spectroscopy

Frequency dependent impedance measurements were also performed on hybrid silicon-molecular devices. Fig. 2.9 shows the equivalent circuit of these devices, where the Randles equivalent circuit [21] has been used to represent the “electrolyte-molecule” system. C_d represents the double-layer capacitance and the series combination of R_F and C_F represents the charging and discharging impedances associated with the molecules. Contributions from the semiconductor and thin oxide are represented by C_{Si} and C_{ox} respectively. While C_d and C_{ox} can be considered ideal and constant for a given device, the other elements in the equivalent circuit have strong dependences on the applied voltage and the measurement frequency.

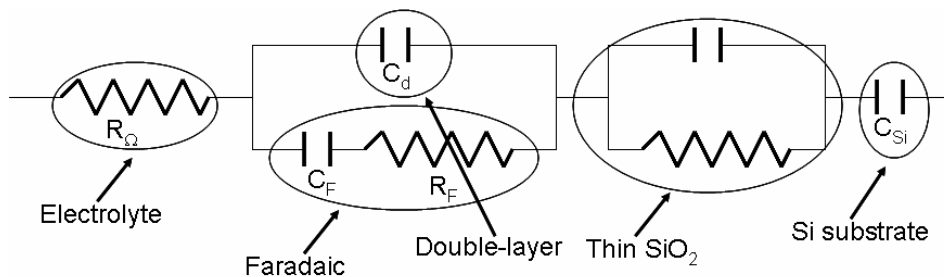


Figure 2.9 Small-signal equivalent circuit for EMS/EMOS capacitors.

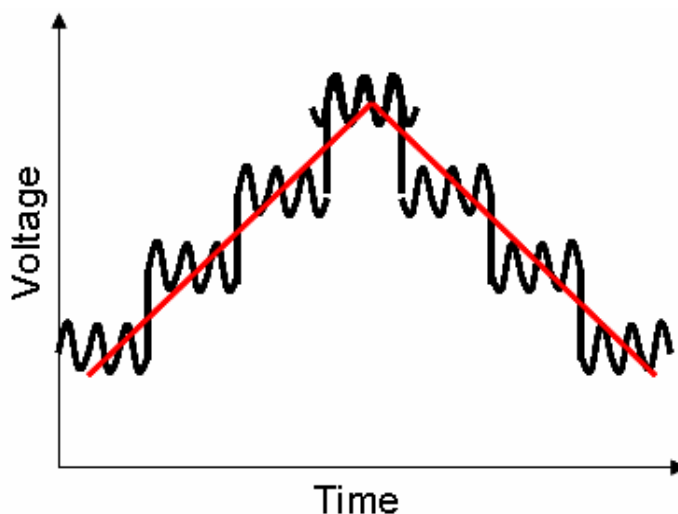


Figure 2.10 Input waveform for impedance spectroscopy measurements. The input voltage consists of a dc voltage ramp (red curve) superimposed with a frequency dependent ac small-signal.

A characteristic input voltage waveform is shown in Fig. 2.10. Some of the parameters involved in the input are (i) dc ramp rate, (ii) small-signal frequency, (iii) small-signal amplitude and (iv) voltage range. There are different ways of looking at the outputs of these measurements.

1. Capacitance-voltage (CV) and conductance-voltage (GV) plots: These can be extracted similar to conventional semiconductor CV and GV measurements. Typically, at a given frequency, these plots will exhibit peaks, both in capacitance and conductance, associated with redox property of the molecules. The distinct peaks in CV and GV arise from the voltage-dependent impedances, R_F and C_F . Different regions of operation of the semiconductor (accumulation, depletion and inversion) can also be observed in these plots.
2. AC current and cotangent of phase vs. voltage: These plots would also show peaks associated with oxidation and reduction of molecules. Expressing the outputs in these forms has been conventionally followed in the field of electrochemistry and is called AC voltammetry [21].
3. DC ramp rate dependence: Peaks in CV and GV can be observed both in the forward and reverse voltage scans. The voltages at which the forward the reverse peaks occur depend on the DC ramp rate (similar to scan rate in CyV). If the DC ramp rate is much slower compared to the electron-transfer rate – which is the case for most of the experiments in this dissertation – then both the forward and reverse peaks will occur at the same voltage.
4. Frequency and amplitude dependence: At any given DC voltage, an effective small-signal measurement scan rate can be defined as $v_{eff} = f_{ac} \times v_{ac}$. The conductance peak amplitude will increase with increasing f_{ac} and v_{ac} as long as v_{eff} remains slower than the electron-transfer rate. Once v_{eff} increases beyond the electron-transfer rate, the conductance peak

amplitude will start to decrease [23, 24]. Although this frequency dependence is impeded by the slowness of ion conduction in the electrolyte, this technique can give a very good idea about the rate of electron-transfer.

All impedance spectroscopy measurements were performed using a HP 4284a LCR meter.

2.7.3 Charge retention measurements

Charge retention time is a very significant metric for memory devices – it is one of the key aspects that any new memory technology is evaluated based on. Non-volatile memory technologies like Flash require retention times as long as 10 years. While DRAM does not require such stringent rules, it will certainly help to have longer retention times while not sacrificing speed. In any case, the retention times of any new DRAM technology has to at least match that of the existing technology (64 ms). With this in mind, charge retention measurements were performed on the hybrid devices in order to assess the usefulness of this technology. These measurements were made using two different techniques.

1. Open Circuit Potential Amperometry – This technique was developed by Roth et al. [18] and is similar to the pulse measurement technique in some ways. The device's OCP (open circuit potential, which is the voltage at which no current flows across the device) is first empirically calculated by applying a series of voltages and monitoring the current. The OCP of these devices are not 0 V because of charging of the double layer capacitance. The device is then written using a voltage pulse large enough to oxidize the molecules and the current across the device is measured at OCP after a wait time, which is varied. The resultant current will be purely due to the presence of charges in the monolayer. The amount of charge remaining after different wait times can be calculated from the current-time relationship and a plot of charge vs. time will give an estimate of the retention time of the device. Instead of the OCP, 0 V can also be applied and correction factors can be used to accurately estimate the retention times.
2. Variation of CyV – As will be discussed in later chapters, the oxidation and reduction processes in a hybrid capacitor are completely separated from each other beyond a certain thickness of SiO₂ due to the additional barrier introduced [13, 23, 25]. For such devices, a variation of CyV can be used to evaluate the charge retention times. As shown in Fig. 2.11, an oxidizing scan is first applied to the device to charge all the molecules. Subsequently, either another oxidizing scan or a reduction scan is applied after a wait time, which is varied. The amount of charges oxidized during the second oxidizing scan (or the amount reduced during the reduction scan) gives an estimate of the number of charges that remained after the wait time [25].

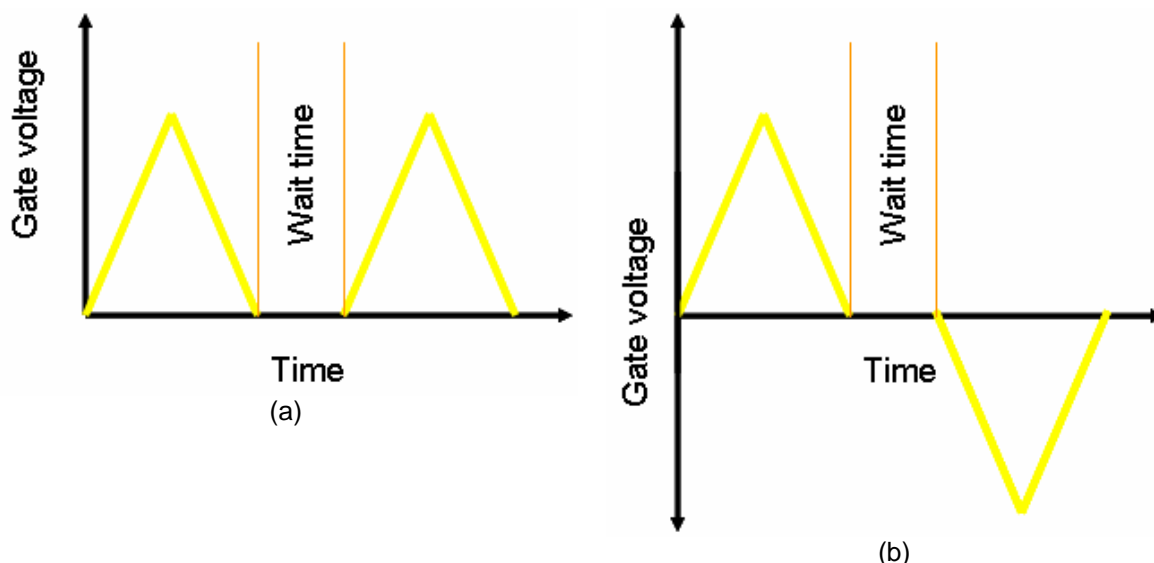


Figure 2.11 Voltage-time inputs for charge retention measurements using CyV. An oxidation scan is applied, which is followed by either another oxidation scan (a) or a reduction scan (b), separated by a wait time. The wait time is varied and charge retained vs. wait time is calculated.

2.7.4 MoleFET Characterization

Apart from CyV, CV and GV, the MoleFETs were also characterized using a HP 4155B Semiconductor Parameter Analyzer to derive I_d - V_d device characteristics and I_d - V_g transfer characteristics. The extent to which the drain currents and threshold voltages were modulated by charging and discharging of the molecules was interpreted from the MoleFET characteristics.

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3. MOLECULES ON SILICON

3.1 Introduction

Many research activities are currently focused on developing novel technologies to replace the existing silicon technology beyond its fundamental scaling limits [1-3]. One such field is molecular electronics, which involves the use of one to few organic molecules to make logic and memory elements. Although there have been many recent developments in this field [2, 4, 5], there are still a lot of challenges and fundamental questions which need to be addressed. In the meanwhile, while the silicon technology has a few more years to go before it reaches its limits [6], a hybrid silicon/molecular approach might help in providing a smooth transition from the Si-only technology to a molecule-only technology. Our approach involves formation of a monolayer to a few layers of redox-active molecules on Si and SiO₂ substrates for memory applications [7-10]. These molecules possess discrete quantum states from which electrons can tunnel to the Si substrate at discrete applied voltages (oxidation process), leaving behind a positively charged layer of molecules. The reduction process, which is the process of electrons tunneling back from Si to the molecules, neutralizes the positively charged molecular monolayer. The ability to write and erase charges in the redox molecules at discrete voltages makes this hybrid approach an attractive candidate to be used in charge-storage memory devices such as DRAM or FLASH. Furthermore, the densities of charges that can be achieved (5×10^{13} charges/cm² and higher) are a few orders of magnitude higher than that in a conventional DRAM capacitor. The write/erase voltages and the retention times of these hybrid memory devices can also be tuned by varying the thickness of SiO₂ and/or engineering the Si substrate [9-11]. Multiple-bit memory can be created in a single cell by employing mixed molecular monolayers [12] or chemical synthesis of molecules [13, 14]. Apart from these salient properties, the hybrid approach also takes advantage of existing Si technology and is easy to integrate with the current CMOS process flow [15].

This chapter discusses the fabrication and electrical properties of molecules attached to silicon surfaces. Monolayers of redox-active molecules have been incorporated onto p- and n- type silicon substrates of varying doping concentrations. Distinct peaks in current, capacitance and conductance were observed in cyclic voltammetry (CyV) and impedance spectroscopy measurements. Energy band diagrams, showing the relative position of the energy levels of electrons in the molecular monolayer and the silicon energy bands, have been used to explain the occurrences of these distinct peaks, which are associated with electron transfer between the molecules and the Si substrate. The gate voltage at which the peaks occurred (redox potential) shifted to a more positive value for an n- Si substrate compared to a p- Si substrate. Further, the redox potential for molecules on p-Si was

independent of the doping concentration, whereas it became more negative with increasing doping density for molecules on n-Si. As will be discussed, these dependences of the redox potential on the Si doping type and density arise due to the need for holes in the Si substrate for the oxidation process (electron transfer from molecules to Si), which drive the p-Si into accumulation region and the n-Si into inversion region. Voltage-balance and charge-balance equations have been used to quantify these effects and were found to match the experimental results. This need for holes has been further demonstrated by the use of light, which acts as a source of minority carriers (holes in n-Si). The silicon substrate can hence be engineered to tune the write/erase voltages in hybrid silicon/molecular memory devices incorporating redox-active molecules.

3.2 Experimental

P- and n- type silicon substrates, with (100) orientation, were used as substrates. The doping densities of the substrates varied from 5×10^{15} to 1×10^{18} cm^{-3} . Active areas of sizes varying from 2.5×10^{-5} to 4×10^{-4} cm^2 were defined using a 400-nm thick thermally grown field oxide. A sacrificial oxide of 10-nm was grown in these active areas and etched using 1% HF to obtain a smooth Si surface. The redox-active molecules selected for attachment to Si are **Fc-BzOH** and **Por-BzOH**, as discussed in the previous chapter. **Por-m** was also used to form a redox-active polymer film on Si. The attachment procedures for these molecules are detailed in chapter 2. A 1 M solution of tetrabutyl ammonium hexafluorophosphate, which is an organic electrolyte inert toward the molecules, was used as an electrolyte gate for electrical characterization. Silver wire was used as the gate electrode. These electrolyte-molecule-silicon (EMS) capacitor structures were characterized using cyclic voltammetry (CyV), capacitance-voltage (CV) and conductance-voltage (GV) measurement techniques. CyV was performed using a CHI600A electrochemical analyzer and the CV and GV characteristics were obtained using a HP 4284a LCR meter.

3.3 Ferrocenes on Si

3.3.1 Cyclic Voltammetry

Fig. 3.1(a) shows the chemical structure of **Fc-BzOH**. This molecule possesses two stable redox states – neutral and mono-positive. The alcohol (-OH) linker facilitates attachment to Si via the formation of O-Si covalent bonds. Typical CyV characteristics for EMS capacitor with **Fc-BzOH** on p-Si at varying voltage scan rates are shown in Fig. 3.1(b). The Si doping density for this capacitor was 5×10^{17} cm^{-3} . The peaks observed in the current-voltage characteristics are associated with charging and discharging of molecules on Si. As the gate voltage is swept in the negative direction, the energy levels in the molecules are raised, which results in electron tunneling from the molecules to Si substrate. This process of losing electrons, which leaves the molecular layer positively charged, is termed oxidation. The transient current resulting from the tunneling of electrons is observed as a peak in the bottom half of the CyV characteristics (negative current). In the reverse voltage sweep,

electrons tunnel back from Si to the molecules, thereby bringing them back to their neutral state (reduction process). This is observed as a peak in the positive current. An expression for the current can be derived from electrochemical theories as follows.

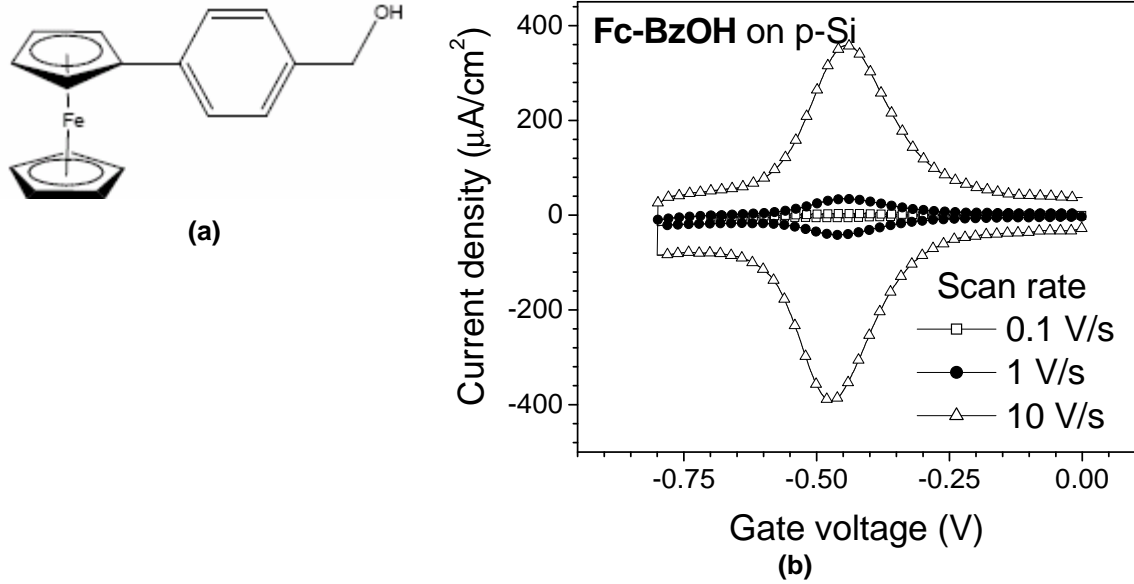


Figure 3.1 (a) Chemical structure of **Fc-BzOH**, ferrocene molecule with benzyl alcohol functional group for attachment to Si surfaces. **(b)** CyV characteristics of an EMS capacitor with **Fc-BzOH** on p-Si at varying scan rates. Peaks in current correspond to oxidation (negative current) and reduction (positive current) of molecules. The peak current linearly increases with scan rate. The density of molecules, obtained from the area under the peaks, is 1.5×10^{14} molecules/cm².

3.3.1.1 Nernst relation and Electron transfer

The equilibrium electron transfer process from a redox species can be described by Nernst relation [16]. Let V^0 represent the reversible potential for the redox-active species attached to Si. This is the voltage at which the rates of electron transfer from and to the molecules are equal to each other. In other words, there is an equal probability of electrons tunneling from or to the molecules. If the CyV voltage scan rate is much slower than the electron transfer rates, then equilibrium will be maintained as the voltage is scanned. Nernst equation can then be used to relate the voltage applied to the fraction of neutral and positively charged molecules.

$$V = V^0 + \frac{RT}{nF} \ln \frac{\Gamma_0}{\Gamma_+} \quad (1)$$

Here, V is the applied voltage, R is the universal gas constant, T is the temperature, F is the Faradaic constant, Γ_0 and Γ_+ are the fraction of coverage of the neutral and positively charged molecules, respectively. The current is directly related to the rate of charging/discharging and is given by

$$I = -nFA \frac{d\Gamma_+}{dt} = nFA \frac{d\Gamma_0}{dt} \quad (2)$$

where A is the active area of the device. Combing (1) and (2) and using the relationship for total coverage

$$\Gamma_t = \Gamma_0 + \Gamma_+ \quad (3)$$

gives the expression for current in terms of the voltage and the scan rate.

$$I = \frac{n^2 F^2 A \Gamma_t n}{RT \left[1 + e^{\frac{nF}{RT}(V-V^0)} \right]^2} e^{\frac{nF}{RT}(V-V^0)} \quad (4)$$

where $n = \left| \frac{dV}{dt} \right|$ is the voltage scan rate. As this expression indicates, the charging and discharging currents are equal in magnitude, which is observed experimentally in Fig. 3.1(b). The current peaks occur at V^0 and are given by the following expression.

$$I_p = \frac{n^2 F^2}{4RT} n A \Gamma_t \quad (5)$$

As the gate voltage is made more negative (positive), electrons start to flow from (to) the molecules to (from) the Si substrate thereby oxidizing (reducing) them. The current, which is a measure of the rate of change of oxidized or reduced molecules, begins to increase as oxidation or reduction starts. When more than half the total number of molecules is converted from one state to another, the rate begins to drop until all (almost all) of the molecules are either in the neutral or positively charged state. Thus, there appears a peak in the current-voltage relationship in both the forward and reverse scans. As indicated by (5), the peak current scales linearly with the scan rate as long as the electron transfer rates are much faster than the measurement scan rate. This is observed in Fig. 3.1(b), where the charging and discharging currents are symmetrical and the current peaks increase linearly with scan rate. The total coverage of the molecules on the Si surface can be obtained from the area under the peaks. Integrating expression (4) gives the area under the peaks as

$$Area = nFA n \Gamma_t \quad (6)$$

For **Fc-BzOH** on p-Si, the coverage obtained from experimental results of Fig. 3.1(b) is 1.5×10^{14} molecules/cm². Since the footprint of a single **Fc-BzOH** molecule is approximately 1 nm², this coverage indicates that a saturated monolayer of the molecules are formed on Si. The density of Si atoms on (100) plane is approximately 6.8×10^{14} cm⁻², which implies that about 77% of Si atoms are attached to molecules.

If the measurement scan rate is faster than the electron transfer rates, then the charging and discharging currents will no longer be symmetrical. This will cause the current to lag behind the voltage, which results in a separation of oxidation and reduction peaks. This peak separation will

further increase with increase in scan rate. For EMS capacitors with **Fc-BzOH** on Si, the peaks were observed to be symmetrical at least up to 100 V/s, indicating the fast nature of electron transfer.

3.3.2 Impedance Spectroscopy

Fig. 3.2 shows the capacitance-voltage (CV) and conductance-voltage (GV) characteristics of an EMS capacitor with **Fc-BzOH** on p-Si at 100 Hz and 1 kHz. Redox peaks are observed in CV and GV at the same gate voltage (-0.45 V) as CyV peaks. The inset in Fig. 3.3 shows the GV characteristics of the same capacitor at positive gate voltages. A peak at 0.5 V is observed, which is related to the depletion of the p-Si surface. This indicates that the p-Si substrate is in the accumulation region during the redox process.

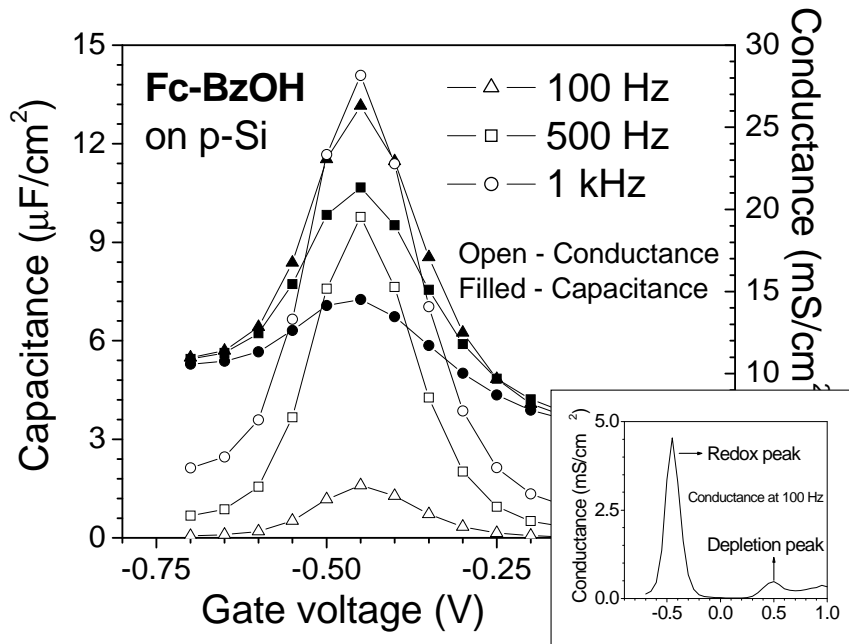


Figure 3.2 CV and GV characteristics of an EMS capacitor with **Fc-BzOH** on p-Si at varying frequencies. Peaks in both capacitance and conductance are observed at the same voltage as CyV peaks. Only oxidation scans are shown. Inset shows GV characteristics at positive voltages as well. Peak at +0.5 V corresponds to the depletion peak of Si surface.

The electrolyte, which is an ionic conductor, facilitates measurements at very low frequencies due to its low conductivity. The quality factor for these measurements, given by $Q = \frac{wC}{G}$ is greater than 5, indicating that the measurements are good even at low frequencies such as 100 Hz [17].

3.3.3 Energy Band Diagram

Fig. 3.3 shows the energy band diagram of this EMS structure during the oxidation and reduction processes. When a molecule is formed from its constituent atoms, the atomic orbitals combine in a certain way to create molecular orbitals, which are discrete quantum energy states for electrons in the molecules [18]. The highest energy state occupied by a valence electron of the molecule is called HOMO (Highest Occupied Molecular Orbital). Since there is only a monolayer of

molecules on the Si substrate, there exist minimal interactions between individual molecules to create energy bands. Hence, the energy levels of the molecules in the monolayer remain discrete with respect to the energy bands of Si, as shown in Fig. 3.3. When there is no applied gate voltage, the HOMO of the molecules can be thought of as being at a lower electronic potential than the conduction band edge, E_C , of the Si band structure. A negative gate voltage raises the energy of the electrons in the molecules and results in the tunneling of an electron from the molecule to the Si substrate, through the thin potential barrier that exists due to the linker (not shown in figure), when the HOMO lines up with E_C . This voltage corresponds to V^0 , the voltage at which CyV, CV and GV peaks occur. The exact voltage at which this happens depends on the difference between Fermi levels of the electrolyte and Si (ϕ_{ms}), the surface potential in Si (ψ_{Si}), the resistive drop across the electrolyte (V_{el}) and the voltage drop across the double-layer capacitor due to the charges at the Si surface (V_{dl}). The voltage-balance equation can, therefore, be written as

$$V_G = f_{ms} + V_{el} + y_{Si} + V_{dl} = f_{ms} + V_{el} + y_{Si} - \frac{Q_{Si}}{C_{dl}} \quad (7)$$

V_{dl} is the voltage across the parallel combination of molecules and the electrolytic double-layer capacitor. This is explained in detail in chapter 5. As the gate voltage is swept in the negative direction, V_{dl} increases, thereby increasing the probability of electron tunneling from the molecule to the Si substrate. Since this voltage appears across all the individual molecules in the monolayer, this increased probability results in an increasing oxidation current due to oxidation of some of the molecules in the monolayer. As the voltage is further increased, the current reaches a maximum and then begins to decrease until all the molecules in the monolayer are oxidized. Likewise, a reverse voltage sweep results in electrons tunneling from the Si substrate to the monolayer, thereby reducing the molecules to their neutral state. This is observed as a peak in the reduction current. Peaks in CV and GV can be explained using the same argument.

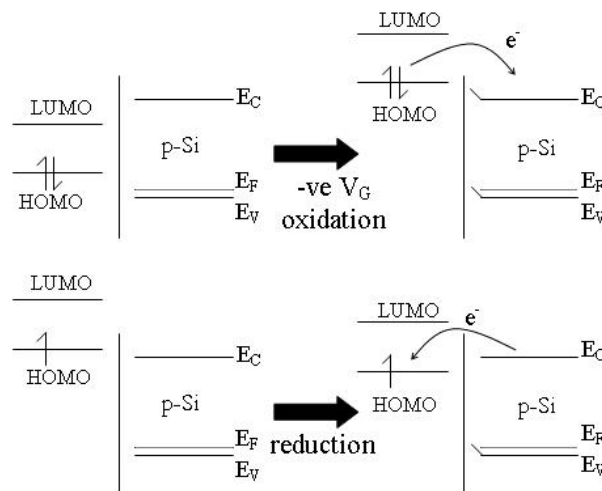


Figure 3.3 Energy band diagrams depicting oxidation and reduction processes of molecules on p-Si. Electron from HOMO tunnels into Si at negative gate voltages. p-Si surface goes into accumulation.

3.3.4 p-type versus n-type Si substrate

The primary difference between molecules on n-type and p-type substrates is in the region of operation of the substrate during the oxidation process. Under negative gate biases, the surface of p-Si is accumulated (more holes than in bulk), whereas, the surface of n-Si is depleted and inverted. The availability of holes at the surface of the n-type substrate is necessary for the oxidation process to take place in order for the electrons coming from the molecules to recombine with holes. Holes, which are minority carriers in an n-type substrate, are created at the surface either thermally or by the formation of an inversion layer. This need for holes is further evidenced at fast voltage scan rates in CyV and in the presence of light. This will be discussed in the next section.

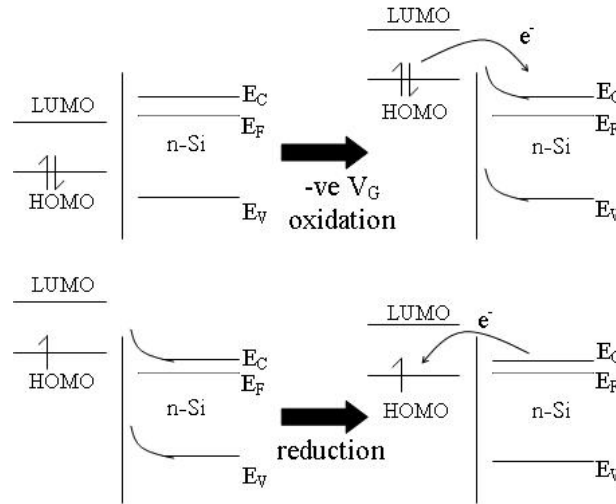


Figure 3.4 Energy band diagrams depicting oxidation and reduction processes of molecules on n-Si. The surface of n-Si goes into depletion and inversion during the redox process.

Fig. 3.4 shows the energy band diagrams for an EMS structure with an n-type Si substrate. The voltage-balance equations for n- and p- substrates can be written as [19]

$$V_{Gn} = f_{msn} + V_{el} + y_{n-Si} - \frac{Q_{dep}}{C_{dl}} \quad (8)$$

$$V_{Gp} = f_{msp} + V_{el} + y_{p-Si} - \frac{Q_{acc}}{C_{dl}} \quad (9)$$

As shown in Figs. 3.3 and 3.4, the Si energy bands at the surface of the substrate bend upward during the oxidation process resulting in a negative surface potential. Q_{dep} and Q_{acc} in (8) and (9) are depletion and accumulation charges in n-Si and p-Si substrates, respectively. The expressions for Q_{dep} and Q_{acc} are given as [19]

$$Q_{dep} = \sqrt{2qe_{Si}N_D} \left(\sqrt{y_{n-Si} + \frac{kT}{q} e^{-\frac{q(y_{n-Si} - 2f_F)}{kT}}} \right) \quad (10)$$

$$Q_{acc} = \sqrt{2qe_{Si}N_A} \left(\frac{kT}{q} \sqrt{e^{-\frac{q\psi_{p-Si}}{kT}}} \right) \quad (11)$$

For p-Si substrates, it can be assumed that V_{di} , and hence Q_{acc} , are same at V^0 for different doping densities. This leads to the following relation.

$$N_{A1} e^{-\frac{q\psi_{p1}}{kT}} = N_{A2} e^{-\frac{q\psi_{p2}}{kT}} \quad (12)$$

Here, the subscripts $_1$ and $_2$ indicate two different doping densities. From (9) and (12), we have

$$V_{Gp1} - V_{Gp2} = (f_{msp1} - f_{msp2}) + (\psi_{p1} - \psi_{p2}) = \frac{kT}{q} \ln \left(\frac{N_{A2}}{N_{A1}} \right) + (\psi_{p1} - \psi_{p2}) = 0 \quad (13)$$

Hence, the redox peak voltages for molecules on p-Si don't vary much with changing doping density.

On the other hand, for an n-type substrate, the surface potential in depletion/inversion, ψ_{n-Si} , is not small and is dependent on the doping concentration of Si. Hence, there is a strong dependence of the redox voltages on the doping density for molecules on n-Si. The surface potential, ψ_{n-Si} , can be

approximated to $2\phi_F$, where ϕ_F is the Fermi potential given by $-\frac{kT}{q} \ln \left(\frac{N_D}{n_i} \right)$. Approximating the

difference between the Fermi levels of n-Si and p-Si to 1 eV (bandgap of Si is 1.1 eV), the following relations for the redox peak voltages can be obtained from (8) and (9).

$$V_{Gn} - V_{Gp} = 1(V) + 2f_{Fn} = 1(V) - 2 \frac{kT}{q} \ln \left(\frac{N_D}{n_i} \right) \quad (14)$$

$$V_{Gn1} - V_{Gn2} = 2 \frac{kT}{q} \ln \left(\frac{N_{D2}}{N_{D1}} \right) \quad (15)$$

where the subscripts $_1$ and $_2$ indicate two different doping densities. As shown in Fig. 3.5, redox peaks for **Fc-BzOH** on p-Si were observed at a gate voltage of -0.66 V for 2 different doping densities of Si, as predicted by (13). The difference between redox peak voltages for **Fc-BzOH** on n-Si for varying doping densities can also be seen in Fig. 3.5. Table 3.1 summarizes the experimental results for **Fc-BzOH** on n-Si and p-Si substrates for 2 different doping densities each. As can be seen from the table, the theoretical predictions from (13), (14) and (15) very closely match the experimental results. However, these are only approximations. In order to accurately predict the redox voltages for molecules on n-Si and p-Si substrates with varying doping densities, the work function differences between the electrolyte gate and silicon substrate has to be known precisely for varying Si doping

types and densities. Furthermore, the surface potential in n-Si can be different from $2\phi_F$. The exact dependence of the ψ_{n-Si} versus gate voltage for varying doping densities need to be calculated.

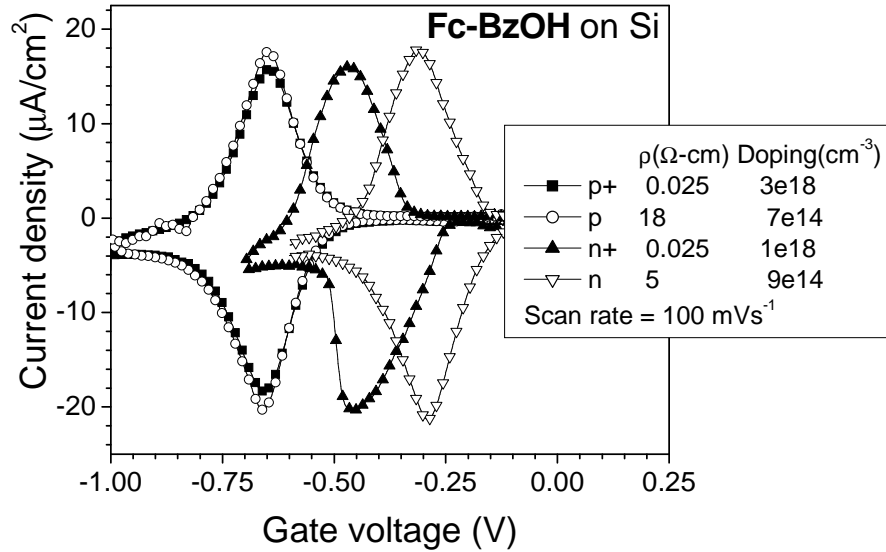


Figure 3.5 CyV characteristics of EMS capacitors with **Fc-BzOH** on n-Si and p-Si with 2 different doping densities: effect of Si doping type and density on redox voltages. The scan rate is 100 mV/s.

Table 3.1 Theoretical and experimental values of redox voltages for **Fc-P** on n-Si and p-Si

N_D (cm^{-3})	Theoretical		Experimental	
	$2\phi_{Fn}$ (V)	$V_{Gn} - V_{Gp}$ (V)	V_{Gn} (V)	$V_{Gn} - V_{Gp}$ (V)
9×10^{14}	-0.570	0.430	-0.27	0.390
10^{18}	-0.933	0.067	-0.51	0.150

3.3.5 Minority carriers and effect of light

As discussed in the previous section, during the oxidation process, the Si substrate is in the accumulation region if it is p-type and in the depletion and inversion regions if it is n-type. In order to observe the current due to oxidation in CyV, the electrons tunneling from the molecules have to recombine with holes at the surface of the Si substrate. Holes are majority carriers in p-Si and hence are available in plenty. Therefore, even at relatively fast scan rates, charging current from all the molecules in the monolayer is observed, as shown in Fig. 3.1(b). On the other hand, holes are minority carriers in n-Si. For oxidation to take place, holes have to be generated thermally, which is a slow process. Hence, the extent of oxidation is limited by the amount of holes available at the surface of n-Si and the measurement scan rate.

In Fig. 3.5, the scan rate is 100 mV/s, which is slow enough for thermal generation of holes. Hence, all molecules in the monolayer take part in the redox process, as indicated by coverage of

$1.5 \times 10^{15} \text{ cm}^{-2}$. However, at faster scan rates, not all molecules were observed to be involved in charging and discharging. This is evident in Fig. 3.6, which shows the CyV of an EMS capacitor with **Fc-BzOH** on n-Si doped with 10^{15} dopant atoms/ cm^3 , at scan rates of 1 and 10 V/s. At 1 V/s, the observed coverage was equal to that of a saturated monolayer, indicating that the scan rate was slower than the thermal generation rate of holes. As the scan rate was increased, the extent of oxidation was found to decrease (10 V/s scan in Fig. 3.6) due to the limited availability of holes. At this scan rate, there is not enough time for the generation of sufficient minority carriers at the surface of n-Si for oxidation of all the molecules. An external light source can increase the minority carrier generation rate. Hence, the presence of light can impact the extent of oxidation for molecules on n-Si. This was indeed observed, as shown in Fig. 3.6, where the presence of light increased the coverage to $1.5 \times 10^{15} \text{ cm}^{-2}$ at 10 V/s. This effect of a steady-state optical excitation was also observed in CV and GV characteristics, where redox peaks were more prominent in the presence of an external light source (Fig. 3.7).

The density of holes in the Si substrate also depends on the doping concentration of the substrate. As the n-Si doping density increases, the concentration of holes decreases. Therefore, the extent of oxidation will be lower for heavily doped n-Si than for a lightly doped substrate. This is depicted in the bar graph in Fig. 3.8, which shows the amount of molecules oxidized for EMS capacitors with **Fc-BzOH** on n-Si with two different doping concentrations, 9×10^{14} (n) and 10^{18} (n^+) cm^{-3} , with and without light. The charge densities were obtained by integrating the area under the peak current in CyV at 10 V/s. As can be seen from this figure, in the absence of any external light source (dark), the charge density is lower for the heavily doped substrate than for the lightly doped substrate ($2 \times 10^{13} \text{ cm}^{-2}$ for n^+ compared to 8×10^{13} for n). In the presence of light, the charge density increased to $1.5 \times 10^{14} \text{ cm}^{-2}$ for the lightly doped substrate, whereas it increased only to $1.2 \times 10^{14} \text{ cm}^{-2}$ for the n^+ substrate.

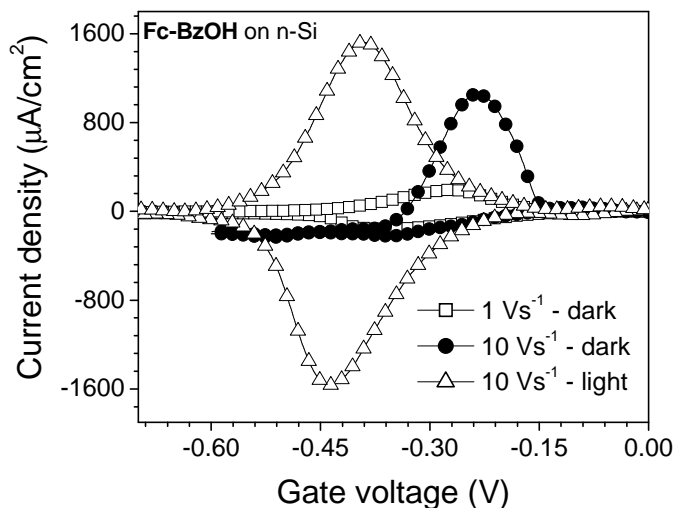


Figure 3.6 CyV characteristics of an EMS capacitor with **Fc-BzOH** on low-doped n-Si substrate showing the effect of minority carriers and light on the extent of oxidation of molecules.

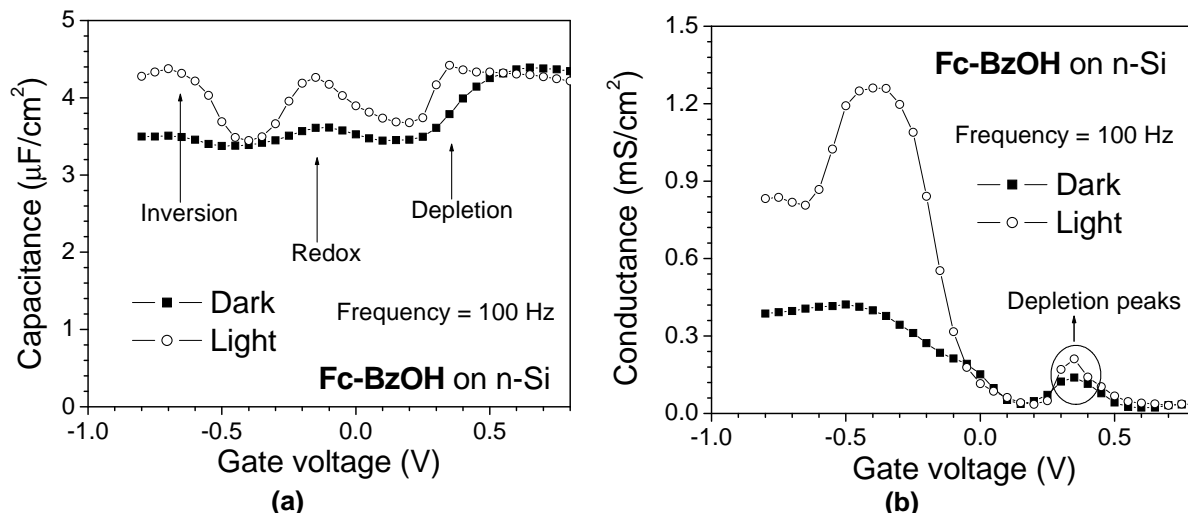


Figure 3.7 CV (a) and GV (b) characteristics of EMS capacitor with **Fc-BzOH** on n-Si with and without an external light source. Only oxidation scans are shown. Redox peaks are more prominent in the presence of light. n-Si depletion peaks are observed at 0.35 V. Inversion of Si can be observed in the CV characteristics in the presence of light.

All these results clearly indicate the strong dependence of oxidation on the availability of minority carriers in n-type substrates. No such dependences were observed for molecules directly on p-Si or a metal surface. However, reduction molecules on SiO_2 showed dependence on the availability of electrons. These results will be discussed in the next chapter.

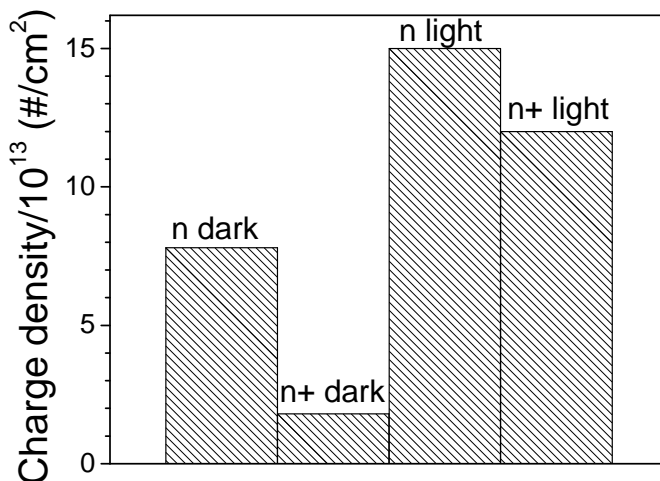


Figure 3.8 Effect of light and doping density on the extent of oxidation of **Fc-BzOH** on n-Si. The charge densities were obtained by integrating the area under the oxidation current in CyV at a scan rate of 10 V/s.

3.3.6 Conclusions and Applications

Monolayers of **Fc-BzOH** have been incorporated on both p-Si and n-Si substrates with varying doping densities. The redox voltages of these immobilized molecules were found to be independent of doping densities on p-Si. For molecules on n-Si, the gate voltages at which oxidation occurred became more negative with increasing doping concentrations. These dependencies arise from the

differences in Fermi levels and surface potentials of n-Si and p-Si. Theoretical predictions based on simple voltage-balance equations were found to closely agree with experimental results. The p-type substrate is driven into accumulation region, whereas the n-type substrate is driven into depletion/inversion regions during the oxidation process. The extent of oxidation is limited by the amount of holes in the substrate, which was demonstrated at fast measurement scan rates for molecules on n-Si. Presence of light during the measurement introduces additional minority carriers (holes in n-Si), thereby increasing the amount of molecules oxidized.

The differences in redox potentials for molecules on n-Si and p-Si and the dependences on doping concentrations can be used to tune the write voltages of these hybrid memory elements. Engineering the silicon substrate provides new opportunities to enable multi-bit and other novel functionalities using redox-active molecules on Si. For example, the number of distinct states can be increased to more than the number of stable states of the molecule by attaching them to structures with n-Si pockets in p-well [11]. These hybrid silicon-molecular capacitors can be used as the charge storage element in DRAM memory applications [20]. MOSFET characteristics (drain current, threshold voltage etc.) can be modulated by incorporating redox-active molecules in p-MOSFETs [21], and hence be used for Flash type memory applications. The miniature size of molecules, combined with the ability to tune the redox voltages by engineering the Si substrate can give rise to novel functionalities in the nanoscale.

3.4 Porphyrins on Si

3.4.1 Monolayers of Porphyrins

As discussed in the previous chapter, metalloporphyrins have three stable redox states – neutral, mono-positive and bi-positive. **Por-BzOH**, whose chemical structure is shown in Fig. 3.9(a), is a zinc-porphyrin molecule with a benzyl alcohol functional group for attachment to Si surfaces. Monolayers of **Por-BzOH** have been incorporated on n-Si and p-Si.

Fig. 3.9(b) shows the CyV characteristics of EMS capacitors with **Por-BzOH** on p-Si and n-Si. Two current peaks each in the forward and reverse scans were observed. The first peak at lower negative voltage corresponds to oxidation of neutral porphyrin to its mono-positive state. The 2nd peak that occurs at a higher negative gate voltage is associated with the tunneling of 2nd electron from the porphyrin molecule, leaving behind a bi-positively charged porphyrin monolayer. As with ferrocenes on Si, the peak voltages for n-Si and p-Si are not the same due to differences in Fermi potential, region of operation of Si and surface potentials. The coverage obtained from the area under either of the 2 peaks is 4.5×10^{13} molecules/cm². Since the porphyrin molecule is bigger than the ferrocene molecule, the density of molecules in a monolayer of porphyrins is less than that in a monolayer of ferrocenes. For **Por-BzOH** on p-Si, separation between charging and discharging peaks did not increase appreciably at least up to 100 V/s for both the peaks. This indicated that the rate of electron

transfers for both the peaks were relatively fast, similar to that for **Fc-BzOH** on p-Si. Two redox peaks were also observed in CV and GV characteristics, as shown in Fig. 3.10.

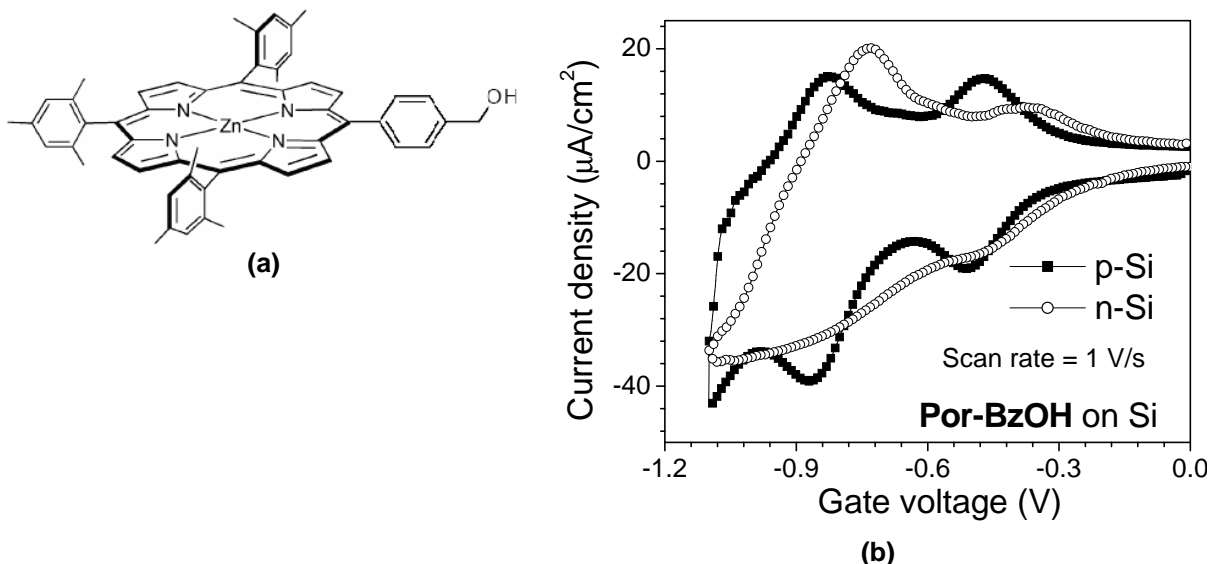


Figure 3.9 (a) Chemical structure of **Por-BzOH**, zinc-porphyrin molecule with benzyl alcohol functional group for attachment to Si surfaces. (b) CyV characteristics of EMS capacitors with **Por-BzOH** on n-Si and p-Si showing 2 peaks corresponding to 3 states – neutral, mono-positive and bi-positive. The characteristics on n-Si are in the presence of light.

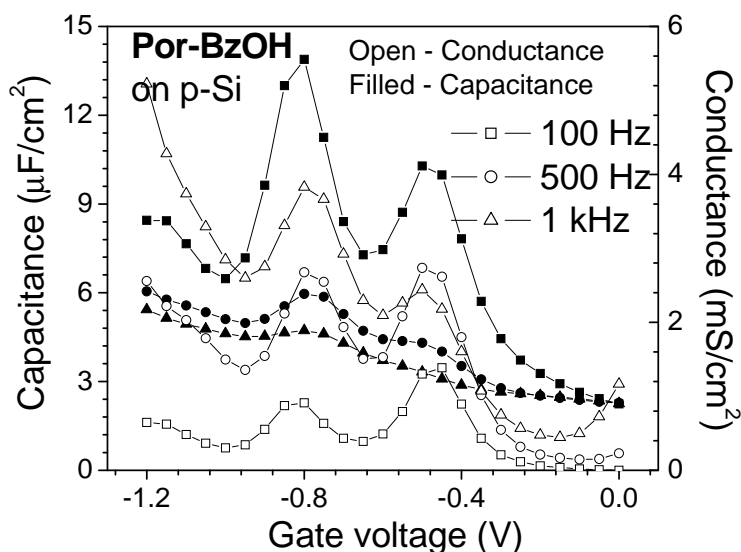


Figure 3.10 CV and GV characteristics of EMS capacitor with **Por-BzOH** on p-Si showing 2 redox peaks at 3 different measurement frequencies. Only oxidation scans are shown.

The use of **Por-BzOH** on Si demonstrates three distinct states in a single memory cell. Mixed monolayers of ferrocenes and porphyrins have also been incorporated on Si for multiple-bit memory applications [12, 20]. Such a configuration provides three distinct peaks in CyV, CV and GV characteristics – one corresponding to oxidation of ferrocenes and two corresponding to oxidation of porphyrins – thereby facilitating four states or two bits in a single cell. Four states have also been achieved by forming monolayers of stacked ferrocene-porphyrin molecule on Si. Details about

characteristics of multiple-bit devices can be found in [20]. Redox-active molecules with higher number of states have been synthesized, but yet to be incorporated in hybrid Si-molecular devices. The ability to achieve up to 3 bits in a single cell using appropriate molecules is very attractive for high density memory applications.

3.4.2 Porphyrin polymers

3.4.2.1 Polymer Films

In the previous section, it was seen that the porphyrin molecule forms a less dense monolayer than the ferrocene molecule due to its bigger size. In order to increase the density of molecules, multiple layers or polymer films of porphyrin molecules were employed by using **Por-m**, whose chemical structure is shown in Fig. 3.11(a). This molecule is functionalized with two acetylene groups at either ends. The attachment procedure, as detailed in the previous chapter, involves placing a single drop of the molecule solution on the sample at 400 °C for 2 minutes. The sample is maintained in an Argon environment during the attachment procedure. The surface is then rinsed thoroughly in THF along with ultrasonication. The high temperature initiates the polymerization of the individual porphyrin molecules. At the end of the attachment procedure, a purple-colored film visible to the naked eye was formed on the attachment surface. This indicates the presence of polymer film strongly attached to the underlying substrate. Multiple drops were also used during attachment in order to increase the thickness of the polymer film.

Fig. 3.11(b) shows cross-sectional SEM images of samples after attachment of **Por-m**. The polymer films are capped with a 20 Å Ti/1000 Å Au film deposited by resistive-heating evaporator. The field oxide regions adjacent to the active areas are shown in these images for better contrast. The polymer films are formed on the active areas as well as the field oxide surrounding them. The thickness of the field oxide was 3000 Å, which can be verified in these images. Fig. 3.11(b) indicates a polymer film thickness of approximately 20 nm for one drop of molecule solution. If the height of a porphyrin molecule is approximated as 2.5 nm, then a polymer film thickness of 20 nm corresponds to 8 layers of porphyrins. However, the individual molecules need not be vertically aligned within the polymer. Hence, the polymer film is not exactly equivalent to multiple layers of porphyrins. Increasing the number of drops increased the thickness of the film to as high as 100 nm, as indicated in Figs. 3.11(c) and (d).

Por-m and other ethynyl porphyrins have shown to undergo thermal polymerization at 400 °C to produce films on Si surfaces [22]. The porphyrins in the polymer film are covalently linked to one another and the base layer is covalently bound to the surface via carbosilane linkages. A detailed analysis of porphyrin film formation can be found in reference [22].

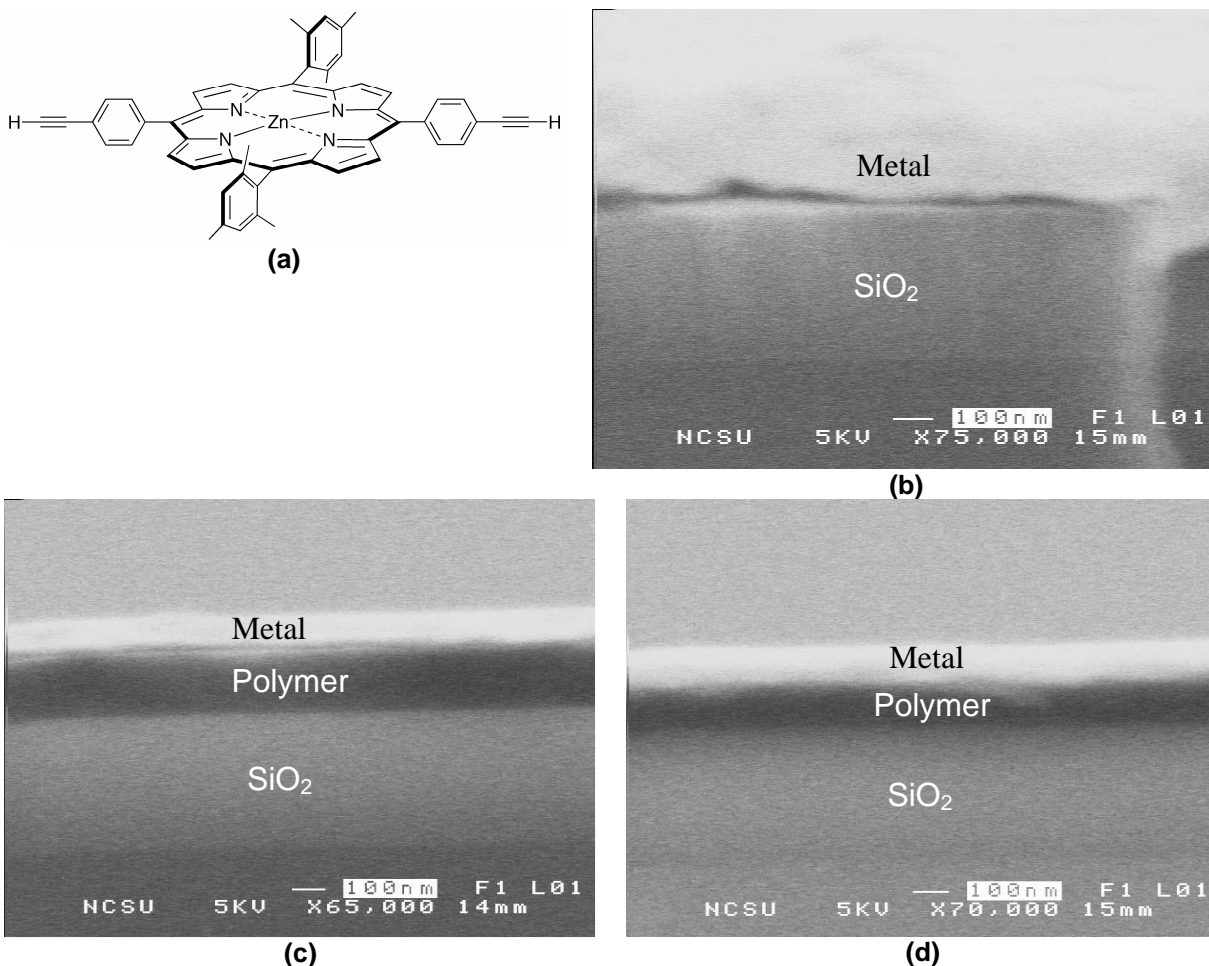


Figure 3.11 (a) Chemical structure of **Por-m**, zinc-porphyrin molecule with 2 acetylene functional groups at the ends. This molecule polymerizes and forms a film on Si and SiO₂ at elevated temperatures. (b-d) Cross-sectional SEM images of polymer film on field SiO₂. The polymer layer is capped with Ti/Au metal layers. The number of drops of molecule solution during attachment was 1 (b), 2 (c) and 3 (d).

3.4.2.2 Electrical Properties of Polymer films

CyV, CV and GV characteristics were performed for EMS capacitors with **Por-m** on p-Si and n-Si. Fig. 3.12 shows CyV characteristics of an EMS capacitor with **Por-m** on p-Si at different scan rates. At a low scan rate of 500 mV/s, the two porphyrin peaks observed were at distinct voltages, similar to those for **Por-BzOH** on p-Si (shown in inset). This indicates that the discrete nature of the energy levels in the molecules was preserved even in the polymer films. In other words, the polymer film, although a few tens of nm thick, does not behave like a bulk material, but retains the properties of individual porphyrin molecule instead. However, the peak separation between oxidation and reduction started to increase at a smaller scan rate than that for the monolayer (Fig. 3.13). This is indicative of the slow kinetics of electron transfer in the polymeric system. The maximum coverage obtained from a single drop attachment of **Por-m** on p-Si is 2.2×10^{15} molecules/cm². As mentioned in reference [22], this is more than an order of magnitude greater than that of a monolayer, which suggests that most of the molecules in the polymer film were involved in the redox process. Such

high densities can only correspond to a film that grows off the surface because this surface concentration would correspond to a molecular footprint of $\sim 3 \text{ \AA}^2$ per molecule on a flat surface. Such a small footprint is unrealistic; the minimum footprint of porphyrins in a monolayer is 50 \AA^2 .

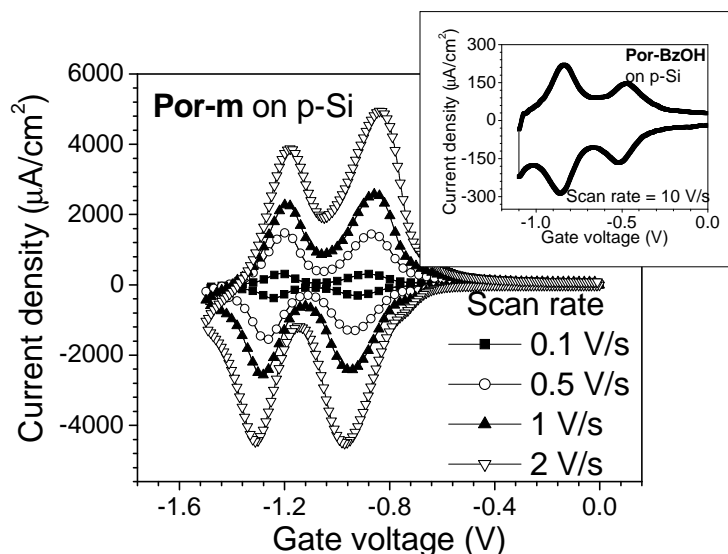


Figure 3.12 CyV characteristics of EMS capacitor with **Por-m** on p-Si at varying scan rates. Two distinct peaks are observed similar to those in **Por-BzOH** on p-Si shown in the inset. Peak separation starts to increase even at low scan rates (compared to porphyrin monolayer) indicating the slowness of electron transfer. Maximum density of molecules obtained from area under peaks is $\sim 10^{15} \text{ cm}^{-2}$.

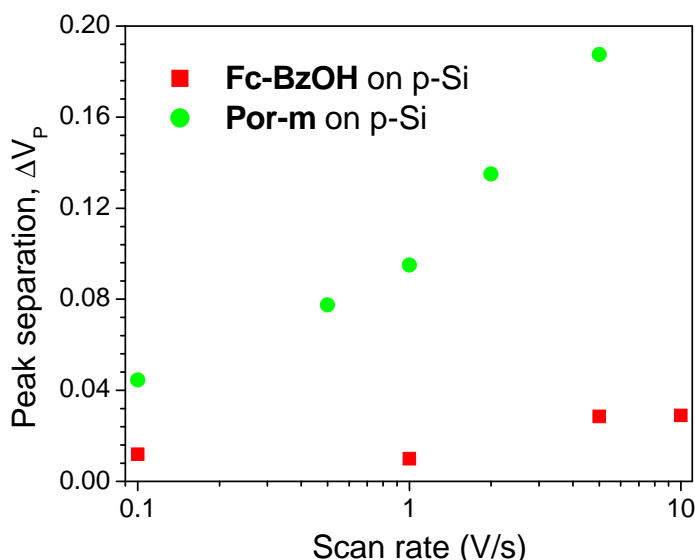


Figure 3.13 Peak separation versus scan rate (from CyV characteristics) for a polymer film of **Por-m** and a monolayer of **Fc-BzOH** on p-Si. The values for **Por-m** correspond to those for the first peaks.

Fig. 3.14 shows CyV characteristics of EMS capacitors with **Por-m** on p-Si and n-Si at 100 mV/s. As expected from earlier discussions, the redox peaks for n-Si occurred at less negative values. Also, the number of molecules participating in redox was much less for n-Si than for p-Si. As explained earlier in this chapter, this is due to the limited availability of minority carriers (holes) in n-Si. Two peaks in CV and GV characteristics were observed for **Por-m** on p-Si and n-Si, as shown in Fig. 3.15. Again, the peaks for **Por-m** on n-Si are much less pronounced.

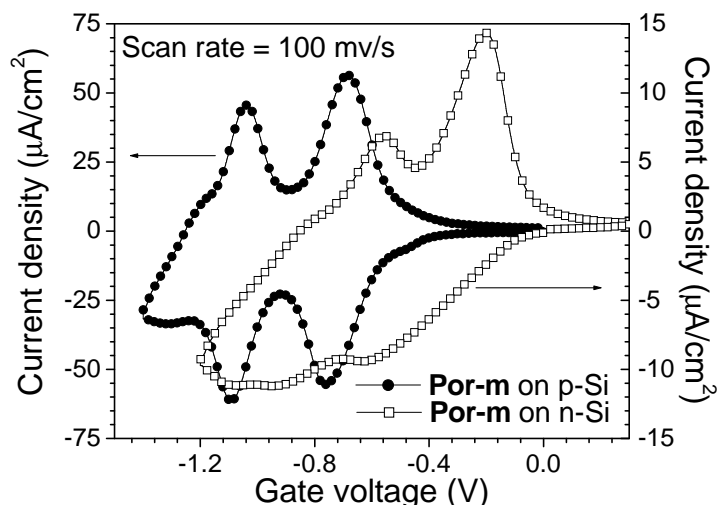


Figure 3.14 CyV characteristics of EMS capacitors with **Por-m** on n-Si and p-Si substrates. The extent of oxidation is limited on n-Si, indicated by the lower coverage, due to limited availability of holes (minority carriers) at the surface of n-Si.

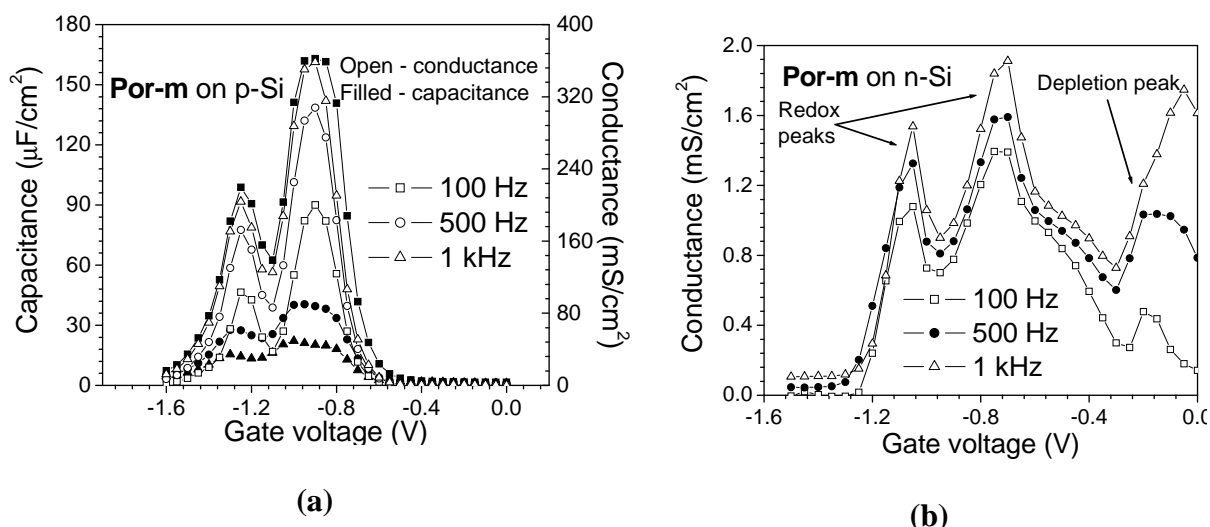


Figure 3.15 (a) CV and GV characteristics of EMS capacitor with **Por-m** on p-Si showing 2 peaks in capacitance and conductance at different frequencies. Only oxidation scans are shown. **(b)** GV characteristics of **Por-m** on n-Si showing 2 peaks. Only reduction scans are shown: peaks are not well defined in the oxidation scans. Depletion peaks are observed at 0.2 V.

3.4.2.3 Timing Effect

The maximum coverage obtained from a single drop attachment of **Por-m** polymer film on Si is greater than 10^{15} molecules/cm². However, this maximum coverage does not always show up in the very first CyV scan. Fig. 3.16(a) shows the CyV scans of an EMS capacitor with **Por-m** on p-Si. The first CyV scan, performed immediately after placing the electrolyte gate on the active area, indicated very low coverage of the order of 10^{13} molecules/cm². As the capacitor was progressively scanned, the charging/discharging currents started to increase, thereby increasing the area under the peaks as well. This increase continued until the coverage obtained from the area under the peaks was equal to 1.5×10^{15} molecules/cm², after which there was no increase with further scanning. This phenomenon

of increasing “apparent coverage” with increasing scans is unique to the polymeric system and does not occur in EMS capacitors with monolayers. In effect, the number of molecules involved in the redox process increases with increasing number of measurements, until all the molecules participate. This “timing effect” is not observed if there is a long time delay between placing the electrolyte on the active are and making the first measurement. However, in this case, a reverse timing effect is observed. Fig. 3.16(b) shows degradation of CyV characteristics with increasing scans. There was a 30 minutes delay between electrolyte placement and the first measurement in the case of Fig. 3.16(b). The first scan exhibited maximum coverage, which decreased during subsequent scans. As is evident from the figure, the coverage obtained from the first measurement was high (1.5×10^{15} molecules/cm²) and did not increase with increasing scans. In other words, there was no “timing effect”. This reverse timing effect is attributed to the degradation of molecules in the polymer film due to moisture and oxygen in the environment.

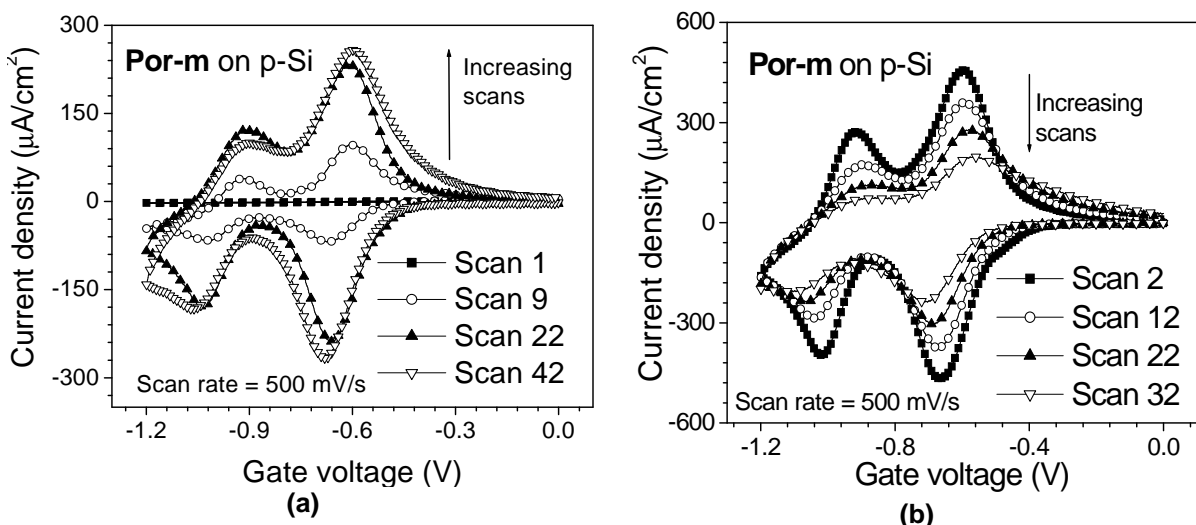


Figure 3.16 CyV characteristics of EMS capacitors with **Por-m** on p-Si showing “timing effect”. In (a), the peak amplitude increases with increasing scans, whereas in (b), there is no such increase. The degradation of coverage observed in (b) is probably due to the presence of moisture.

One of the possible reasons for observing this timing effect could be electrolyte seeping in through the polymer film. When molecules are oxidized, the resulting positive charges on the molecules have to be balanced by equivalent negative charges within the device. In a monolayer, these negative charges are readily provided by negatively charged PF_6^- ions within the electrolyte. However, with a polymer film, if the electrolyte is initially in contact only with the top layer of the film, then it may not be possible to balance all the positive charges within the entire film. Hence, only the molecules in the topmost layer, the ones which are in direct contact with the electrolyte, may take part in the redox process. If the polymer film is porous, then the electrolyte can seep in through the film and thereby be in close proximity with all the molecules in the entire film. As the electrolyte is seeping through, molecules closer to the Si surface can also participate in the redox process because the positive charges can now be balanced by PF_6^- in the electrolyte. This results in the timing effect

observed in CyV measurements. If sufficient time is provided for the electrolyte to seep in before making the first measurement, then the timing effect may not be observed, as seen in Fig. 3.16(b).

Although the above explanation seems plausible, the presence of PF_6^- ions within the polymer film after characterization was not observed with SIMS analysis. Furthermore, the timing effect was not always observed even if there was no delay between placing the electrolyte and making the first measurement. Some samples showed maximum coverage in the first scan itself. Also, the number of scans required to achieve the maximum coverage showed a large variation over different samples. These results are preliminary and a detailed study of **Por-m** on Si is required to understand the exact behavior of the polymeric system. Also, care must be taken to minimize the exposure of molecules to moisture in order to ensure that the coverage does not start to decrease.

3.4.2.4 Thickness (Non-)Uniformity

The SEM image in Fig. 3.11(b) shows a 20 nm thick polymer film for a single drop attachment. However, it has been observed that this thickness is not always the same over different samples that were subjected to the same attachment procedure. Electrical characteristics have also shown that the coverage for a single drop attachment of **Por-m** on p-Si can be anywhere within the range 1.5×10^{14} to 1.5×10^{15} molecules/cm². This large variation in thickness is due to the variations in the volume of the molecule solution placed on the sample and the area on the sample the solution covers during attachment. If a 1 mM solution is used during the attachment procedure, then, for coverage of 1.5×10^{14} cm⁻² on a $100 \times 100 \mu\text{m}^2$ area, the amount of solution required would be approximately 25 μl (assuming that all the molecules polymerize and attach to the active area only). Since it is impossible to accurately measure such small volumes and to confine the solution within the active area, 2 to 3 μl of the molecule solution is placed on the sample during attachment. Since the polymer film adheres to both Si and SiO₂ surfaces, the density of molecules (and therefore the thickness of the polymer film) will depend on the area on the sample over which the solution is placed. However, this area cannot be accurately controlled, which results in large variations in the density of molecules in the polymer film. This is not a problem for real devices, where the areas can be accurately defined using a spectrometer.

3.4.3 Conclusions

Three states in a single cell were achieved by incorporating monolayers and multi-layers (polymers) of zinc-porphyrins on Si surfaces. The redox voltages and extent of oxidation were observed to depend on the doping type and availability of holes, as for the ferrocenes. Monolayers of **Por-BzOH** on p-Si had densities of 4.5×10^{13} molecules/cm², which is less than half of that of **Fc-BzOH**. Higher densities, up to 1.5×10^{15} molecules/cm² were achieved by employing **Por-m** on Si, which forms a polymer film. The polymeric film did not behave like a bulk material, but preserved the distinct nature of the energy levels of individual molecules. However, the electron transfer rate for the

polymer was found to be slower than that for the monolayer. Furthermore, timing effect and thickness non-uniformity were observed for the polymeric system. Therefore, further detailed study is required for redox-active polymers in order to understand these effects and variations. The very high density and three state properties of these redox-active polymers make them very attractive for nanoscale, low power memory applications.

3.5 A Note on Stability

Stability and endurance of the organic molecules used in this study are of paramount importance for transforming this technology from research to development and production. Both ferrocenes and porphyrins are known to be very stable compounds at room temperature and ambient conditions. However, when these compounds are immobilized on Si or SiO₂ surfaces, it is not the stability of molecules by themselves which is important, but that of the entire device consisting of the redox-active unit, the covalent bond that binds it to the surface and the electrolyte solution. Furthermore, these molecules have to endure a large number of write/erase cycles for this technology to compete against existing memory technologies. Another important requirement is the thermal budget. In order to seamlessly integrate these organic molecules with current fabrication processes, they must be able to withstand high temperatures (> 400 °C) for extended periods of time (> 30 min.).

In this study, both **Fc-BzOH** and **Por-BzOH** on Si surfaces were found to be susceptible to moisture. Samples exposed to air before electrical characterization showed much less coverage than the ones that were measured immediately after attachment. On samples that were characterized in air, the molecular densities were found to degrade with repeated cycling. After approximately 100 CyV cycles, the coverage degraded by 10% for ferrocene monolayers and 20% for porphyrin monolayers. Slower scan rates and CV, GV measurements resulted in more rapid degradation. However, if the samples were not exposed to air and were characterized in an inert environment (nitrogen purged in a glove box), then no such degradation was observed even after cycling for days together. A detailed study has shown that porphyrin monolayers can withstand up to 10¹¹ square-pulse cycles without any appreciable degradation [23]. In addition, porphyrins can also withstand exposure to 450 °C for 30 minutes, whereas ferrocenes were found to dissociate beyond 200 °C [23]. This makes the porphyrin molecule more attractive for real-world applications. However, ferrocene based devices are still useful tools to understand the physics of hybrid Si-molecular devices. The understanding can then be extended to systems with more complex molecules with multiple charge states.

The stability of porphyrin polymers on Si was inconclusive. Some samples, particularly the ones which showed timing effect and very high densities, were found to endure many more CyV and CV cycles than the monolayers, even when characterized in ambient conditions. Possible reasons for the extended stability and endurance might be the presence of a thick film and the carbosilane covalent linkages between molecules and Si. In monolayers, it is believed that moisture can lead to

the breaking of the covalent O-Si bond between the redox-active unit and Si, thereby resulting in degraded coverages. Since polymers on Si are covalently bonded via carboxilane linkages, moisture might not play such a role in degradation. Also, top layers of porphyrin in the polymer film might be protecting the layers closer to Si surface, thereby preserving their redox behavior for longer periods of cycling. However, the disadvantages of polymers are their slow charge transfer kinetics.

In order to increase the stability and endurance of these hybrid devices, the molecular layers can be capped with a protective film immediately after attachment. However, the thermal budget remains a constraint for real-world applications.

3.6 Need for SiO₂

3.6.1 Passivate Si surface

The density of molecules in monolayers of **Fc-BzOH** and **Por-BzOH** on Si are 1.5×10^{14} and 4.5×10^{13} molecules/cm², respectively. The density of Si atoms on (100) plane is approximately 6.8×10^{14} cm⁻². Therefore, even with a monolayer of 2-state molecules ferrocenes, more than 77% of the Si atoms are not covalently bonded to any molecules within the monolayer. This number becomes even larger for molecules with higher number of states because of a larger footprint per molecule. Due to the absence of any intentionally grown thermal SiO₂, the non-bonded Si atoms would either be left dangling or will lead to the formation of native SiO₂. In either case, the Si surface is not fully passivated, which may result in a large number of interface states. When monolayers of redox-active compounds on Si are used as FLASH memory devices, the resulting MoleFET device will exhibit unwanted characteristics due to the presence of this large interface states. Therefore, in order to passivate the Si surfaces before attachment on molecules, it is necessary to grow thermal oxides to obtain high quality Si/SiO₂ interfaces. Molecules, specifically synthesized for attachment to SiO₂ could then be used to create monolayers on oxide surfaces.

3.6.2 Longer retention times

One of the important criteria for any memory technology is its retention time. Current DRAM technology has a retention time in the tens of milliseconds. One of the main advantages of hybrid molecular memories is the longer retention times of the hybrid devices with monolayers of molecules immobilized on different surfaces. Ferrocene and porphyrin monolayers on Au electrodes have shown charge retention times in the range of minutes [24-26]. Also, the charge retention times for ferrocenes on p-Si, measured using the OCPA technique described in [25], is about 90 s (details in next chapter). However, for non-volatile memory applications, longer retention times – of the order of 10 years – are required. One of the main routes for charge leakage in these devices is tunneling of electrons from Si surfaces. Therefore, longer retention times can be achieved by increasing the tunnel barrier between molecules and Si, which can be realized using SiO₂. As will be discussed in the next chapter, introducing even a thin SiO₂ layer of 12 Å increases the retention times to more than

200 s. This increases further (and the increase is almost exponential) as the SiO₂ thickness is increased. Hence, to achieve longer retention times and for non-volatility, a tunnel barrier between molecules and Si in the form of SiO₂, is absolutely essential. However, it should be noted that the tunnel barrier also negatively impacts the write and erase speeds of these devices.

3.7 Summary

Monolayers of ferrocenes (**Fc-BzOH**) and porphyrins (**Por-BzOH**) were formed on Si surfaces via self-assembly. Both n-Si and p-Si substrates with varying doping densities were used. Charging and discharging of molecules in the monolayers were confirmed by the presence of distinct peaks in CyV, CV and GV characteristics. The densities of molecules in the monolayers were found to be 1.5×10^{14} ferrocenes/cm² and 4.5×10^{13} porphyrins/cm².

The redox voltages of capacitor devices with monolayers of molecules on Si were observed to be dependent on the Si doping type and density. This is due to the differences in Fermi levels and the region of operation – and hence the surface potential – of Si. Negative gate voltages are required to raise the electron energies in the molecules in order to initiate the charging process. This pushes p-Si surface to into accumulation and n-Si surface into depletion/inversion. For p-Si, the redox process is independent of the doping density. But, for n-Si, the redox process depends on the doping density. Peak positions in CyV, CV and GV occur at less negative voltages for low doped n-Si. Also, the extent of oxidation of molecules is greater for lightly doped n-Si than for heavily doped substrates, due to the presence of more number of holes (minority carriers), which are essential for the oxidation process to occur. The generation rate of holes can be increased by using steady state optical excitation, which then increases the extent of oxidation of molecules on n-Si substrates.

Higher densities of porphyrins were achieved by forming redox-active polymer films on Si surfaces. The discrete electronic states of individual molecules were maintained in the polymer films. However, the rate of electron transfer for polymers was found to be less than that for monolayers. Further, sample-to-sample variations were observed in electron transfer rates, polymer thickness and density. Detailed and thorough studies are required in order to fully understand the behavior of these polymeric systems.

In general, ferrocene monolayers were observed to be more stable than porphyrin monolayers at ambient conditions. But, in inert environment, both ferrocene and porphyrin monolayers were stable under repeated cycling. However, porphyrins are capable of withstanding temperatures as high as 450 °C, whereas ferrocenes dissociate at lower temperatures. Hence, porphyrins may be more attractive for real-world applications. Furthermore, very high densities of porphyrins can be achieved by creating polymer films wherein the porphyrins are covalently bonded to one another and the base layer is covalently attached to the surface via carbosilane linkages. The carbosilane linkages may be more stable than O-Si linkages.

The interaction between redox-active molecules and Si substrate has been studied and analyzed. Co-engineering of molecules and Si can lead to interesting properties and new functionalities. The need for SiO₂ to passivate Si surface and to increase retention times has been recognized. The next chapter discusses the electrical properties of molecules on SiO₂, focusing on the role of SiO₂ in memory properties of these hybrid devices.

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4. MOLECULES ON SILICON DIOXIDE

4.1 Introduction

As discussed in the previous chapter, a silicon dioxide (SiO_2) layer between the molecules and silicon substrate is necessary for multiple reasons – passivate the Si surface; create a high quality SiO_2 -Si interface; achieve longer charge retention times. In order to attach molecules to SiO_2 surfaces, redox-active compounds functionalized with a phosphonic acid group ($\text{PO}[\text{OH}]_2$) have been employed. Two-state molecules ferrocenes, three-state porphyrins and higher number of states molecules have been synthesized with this functional group [1-3]. These molecules have been incorporated on SiO_2 surfaces, with thickness (t_{ox}) varying from 0 to 3 nm ($t_{\text{ox}} = 0$ nm corresponds to Si surface). Monolayers, with densities as high as that on Si, were observed to be formed on SiO_2 surfaces. Electrical characterization revealed that the molecules in these monolayers can be oxidized and reduced by tunneling electrons between molecules and Si through the SiO_2 tunnel barrier. The presence of a barrier introduces significant dependence of device properties (charging, discharging voltages, retention times etc.) on SiO_2 thickness. Write voltages (oxidation) became more negative and erase voltages (reduction) became more positive with increasing t_{ox} . Charge retention times were observed to increase with increasing barrier thickness. However, this was at the expense of slower write and erase speeds.

After a brief recollection of the experimental procedure from chapter 2, this chapter proceeds to discuss the electrical properties of devices with two-state ferrocene molecules on SiO_2 . The physics behind the observed characteristics are identified and explained. Charge retention measurements, performed to quantify the gain in retention times by the introduction of barrier SiO_2 , are presented. The device properties and their dependences on tunneling current through SiO_2 , charge carriers at Si surface and threshold voltage (V_T) are analyzed through experiments in the presence and absence of an external light source. Although most of the chapter involves analysis of devices with p-Si substrates, device properties with n-Si substrates and varying t_{ox} are also introduced. Attachments of molecules with 3 and higher number of states on SiO_2 are discussed towards the end. Finally, stability and endurance of these molecules on SiO_2 are presented and possible mechanisms for the observations are recognized.

4.2 Experimental

Both p-Si and n-Si, with (100) orientation, were used as the substrates. A thin gate SiO_2 of thickness 15 nm was grown via dry oxidation on active areas of varying sizes defined using photolithography. These active areas were isolated from each other by a thick field SiO_2 of thickness greater than 300 nm. Prior to molecular attachment, samples were etched in 1% HF solution in a

controlled fashion to obtain gate SiO₂ thickness varying from 0 to 3 nm. The final thickness was confirmed using ellipsometry. The samples were immediately transferred to inert Argon ambient. The gate SiO₂ thickness after etch was estimated from ellipsometry measurements made on samples with blanket SiO₂ (no field oxide) that had the same starting thickness and were etched alongside the attachment samples. The attachment conditions for **Fc-P**, **Por-P** and **Por-m** are listed in Table 2.2. Monolayers of **Fc-P** and **Por-P** are created SiO₂ surfaces via the formation of P-O-Si covalent bonds. **Por-m**, on the other hand, forms a polymer film and may not be bound to SiO₂ surfaces via covalent bonds. Other porphyrin molecules were also employed in this study. The attachment procedures for these will be presented as and when their electrical properties are discussed. Electrolyte and silver wire were used for electrical characterization as discussed in earlier chapters. The resulting electrolyte-molecule-oxide-silicon (EMOS) capacitor test structures were characterized using cyclic voltammetry (CyV), impedance spectroscopy (CV and GV) and charge retention measurement techniques.

4.3 Ferrocenes on SiO₂ on p-Si

4.3.1 Charging and discharging through SiO₂

Fig. 4.1 shows the chemical structure of **Fc-P**. It is a compound with two-state ferrocene as the redox-active unit, functionalized with phosphonic acid group in order for attachment to SiO₂. Typical CyV characteristics of EMOS capacitors with **Fc-P** on SiO₂ on p-Si are shown in Fig. 4.2. In this figure, the SiO₂ thickness is 1.5 nm and the scan rates are varying between 0.1 and 10 V/s. Peaks associated with oxidation and reduction of molecules are observed in negative and positive currents, respectively. These peaks are similar to the ones observed for EMS capacitors with **Fc-BzOH** on p-Si. However, there are significant differences. The separation between charging and discharging peaks starts to increase at much lower scan rates for **Fc-P** on SiO₂. For an SiO₂ thickness of 1.5 nm (Fig. 4.2), this separation (ΔV_P) changes from 50 to 197 mV as the scan rate is increased from 0.1 to 10 V/s. In comparison, change in ΔV_P for ferrocenes on Si is only 1.5 mV for the same range of scan rates (27.5 mV @ 0.1 V/s, 29 mV @ 10 V/s; see Fig. 3.2). This increased peak separation is due to the presence of SiO₂ barrier. For oxidation and reduction to take place, electrons have to tunnel through the SiO₂ layer. For thickness less than 3.5 nm, tunneling through SiO₂ is dominated by direct tunneling mechanism [4]. In this regime, the tunneling current is dependent on the electric field across the oxide. If the measurement scan rate is faster than the electron transfer rate through SiO₂ (tunneling current and electron transfer rate are directly related), then it results in oxidation peak voltage (V_{PO}) becoming more negative and reduction peak voltage (V_{PR}) becoming more positive, thereby causing an increased peak splitting ($\Delta V_P = V_{PR} - V_{PO}$). For molecules directly on Si, charging and discharging are not limited by tunneling current hence the electron transfer rates are faster compared to the measurement scan rates. The density of molecules on SiO₂, obtained from the area under the peaks in CyV, is 1.5×10^{14} , indicating that **Fc-BzOH** forms a saturated monolayer on SiO₂.

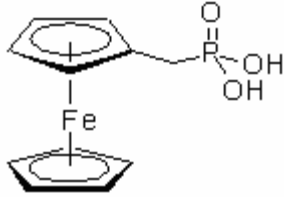


Figure 4.1 Chemical structure of **Fc-P**

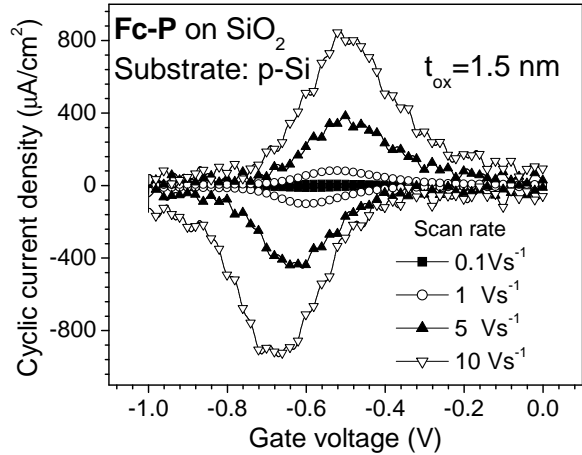


Figure 4.2 CyV characteristics of EMOS capacitor with **Fc-P** on 1.5 nm SiO_2 at scan rates varying from 0.1 to 10 V/s.

CV and GV characteristics for the EMOS capacitor for Fig. 4.2 are depicted in Fig. 4.3. Peaks in capacitance and conductance are observed both in forward and reverse scans, corresponding to charging and discharging of molecules, respectively. The oxidation and reduction peaks occur at the same gate voltage and, unlike in CyV, there exists no peak separation at all frequencies of measurement. The reason behind the absence of any peak separation in impedance spectroscopy measurement is due to the very slow dc ramp rate in this measurement technique. The small signal frequency is not equivalent to the scan rate in CyV. Instead, the dc ramp rate is, which, for the HP4284A LCR meter, is a combination of the voltage step size, measurement frequency and integration mode. This dc ramp rate is much slower compared to even the slowest scan rate in CyV. Hence, the electron transfer rate is comparable or faster than the dc scan rate. Therefore, no separation between the oxidation and reduction peaks is expected or observed. The voltage at which CV and GV peaks occur is mid-way between V_{PO} and V_{PR} . From electrochemical theories [5, 6], this is the voltage at which the charging and discharging rates of electron transfer are equal to one another (V^0). This will be discussed in depth later in this chapter.

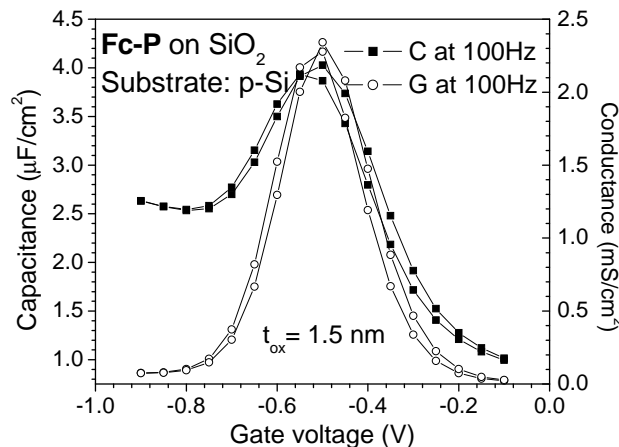


Figure 4.3 CV and GV characteristics of EMOS capacitor with **Fc-P** on 1.5 nm SiO_2 at 100 Hz. Both oxidation and reduction peaks are observed in CV and GV at -0.5 V.

4.3.2 Tunneling current limited electron-transfer

For monolayers directly on Si, there is minimal energy barrier between the energy levels of molecules and the energy bands of Si. Hence, electron-transfer readily takes place as long as the discrete molecular energy levels are lined up with the conduction band edge of Si (E_C). The electron-transfer rate, therefore, depends only on the molecules themselves (Note: this is not strictly true for molecules on n-Si, where oxidation is limited by the availability of holes at the Si surface). In the presence of SiO_2 , oxidation of molecules requires electrons to tunnel across the SiO_2 barrier. Tunneling currents through an insulating barrier are via two main mechanisms – (i) Direct tunneling and (ii) Fowler-Nordheim (FN) tunneling. These two mechanisms are depicted in Figs. 4.4 (a) and (b), respectively. For $t_{\text{ox}} \leq 3.5$ nm and low gate voltages, direct tunneling dominates [4].

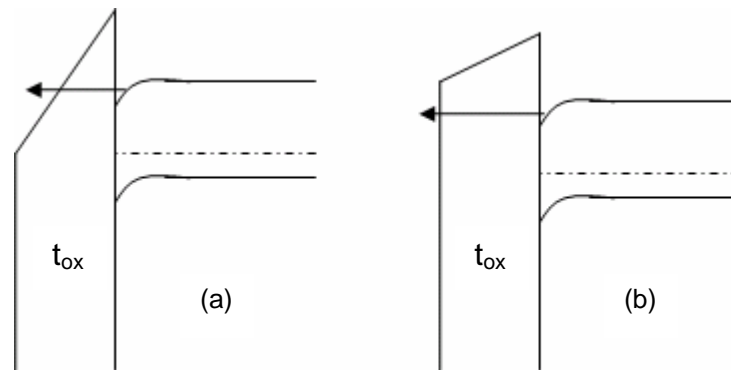


Figure 4.4 Energy diagrams depicting (a) FN tunneling and (b) direct tunneling across SiO_2 . FN tunneling occurs through a triangular barrier, whereas direct tunneling is through the entire barrier thickness.

For the oxidation process, the direct tunneling current depends on the electron energies in the molecules and the electric field across SiO_2 (E_{ox}). Therefore, it is not sufficient for the discrete molecular energy states line up with the conduction band edge of Si. The electron-transfer process becomes limited by the tunneling current through SiO_2 . Hence, the electron energy levels need to be raised further and E_{ox} need to be increased for oxidation to take place. Consequently, the gate voltage at which oxidation occurs is more negative for molecules on SiO_2 than for molecules directly on Si.

On the other hand, for the reduction process, the tunneling current depends on the electron energies at the surface of Si. More precisely, it depends on the difference between the discrete molecular energy levels and the conduction band of Si. Lower the molecular energy levels relative to E_C , greater the tunneling current. The tunneling current also depends on the field across SiO_2 . Therefore, the gate voltage at which reduction of molecules occurs is more positive (or less negative) for molecules on SiO_2 than for molecules on Si.

4.3.3 SiO_2 thickness dependence

EMOS capacitors with SiO_2 thickness varying from 1 to 3 nm were fabricated and characterized in order to observe the dependence of electrical properties on t_{ox} . Fig. 4.5 shows the CyV

characteristics of EMOS capacitors with varying t_{ox} at a scan rate of 0.1 V/s. As t_{ox} increases, the tunneling current through SiO_2 decreases due to increased barrier thickness. This is observed in Fig. 4.5, where the CyV currents decrease with increasing t_{ox} . The presence of SiO_2 and the decreasing tunneling current affects the charging and discharging voltages of the EMOS capacitors. As discussed in the previous section, the oxidation potential becomes more negative and the reduction potential becomes more positive than those for molecules on Si, thereby creating a separation between the oxidation and reduction peak voltages. Furthermore, this peak separation increases with increasing t_{ox} ; higher electron energies and E_{ox} are required for electron-transfer with increasing t_{ox} . Not only does the tunneling current decrease with increasing t_{ox} , but the voltage drop across SiO_2 (V_{ox}) required to achieve the same E_{ox} ($E_{\text{ox}} = \frac{V_{\text{ox}}}{t_{\text{ox}}}$) also increases. Combined together, these result in

an increasing peak separation. This can be observed in Fig. 4.5, where the peak separation ($\Delta V_{\text{P}} = V_{\text{PR}} - V_{\text{PO}}$) increases from 0.05 V to 1.31 V as t_{ox} increases from 1.5 to 2.6 nm at a scan rate of 0.1 V/s.

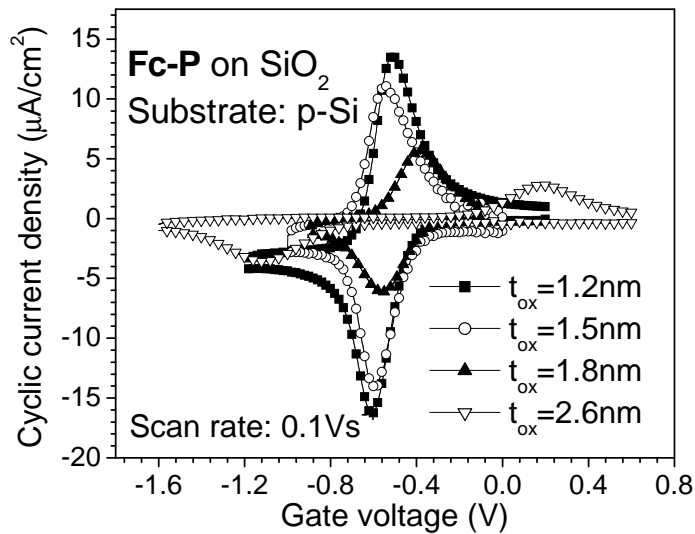


Figure 4.5 CyV characteristics of EMOS capacitors with t_{ox} varying from 1.2 to 2.6 nm. The scan rate is 100 mV/s.

Figs. 4.6 (a) and (b) show the dependence of V_{PO} , V_{PR} and ΔV_{P} on t_{ox} and scan rate. V_{PO} becomes more negative, V_{PR} becomes more positive and ΔV_{P} increases with increasing t_{ox} . The peak separation increases even further at faster measurement scan rates. Again, this is due to the SiO_2 barrier that limits the electron-transfer rate (tunneling current). The dependence of peak CyV current on scan rate, which is expected to be linear for surface attached redox active species, deviates from linearity with increasing t_{ox} , as shown in Fig. 4.7. The linearly increasing peak current starts to “roll-off” at higher scan rates. The scan rate at which roll-off begins decreases with increasing t_{ox} . This further indicates that the electron tunneling current through the oxide layer is the rate limiting step for charging and discharging in EMOS capacitors.

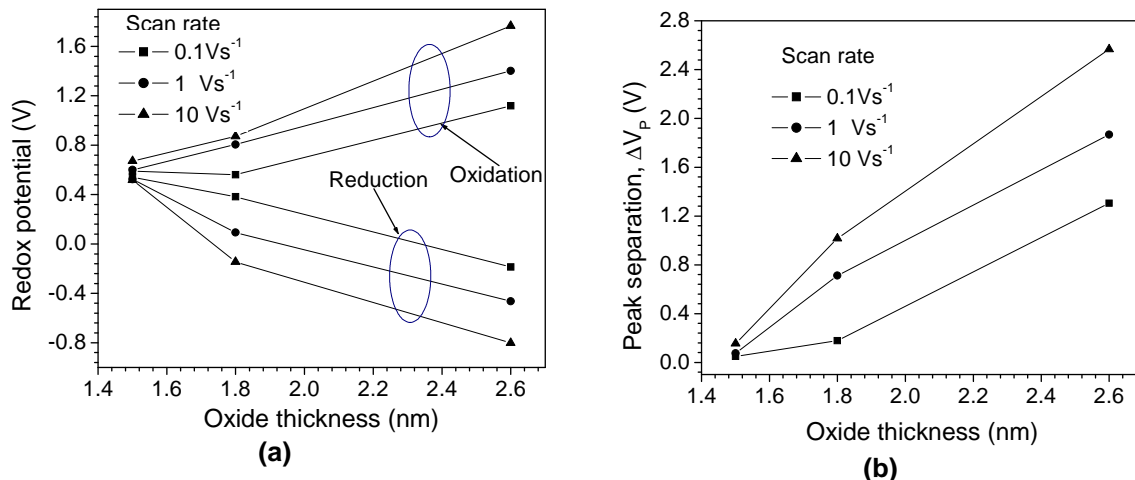


Figure 4.6 (a) Oxidation and reduction potentials for electrolyte-molecule-oxide-Si capacitor as a function of the oxide thickness at scan rates: 0.1, 1, and 10 V/s. The three curves at the bottom represent reduction and the ones at the top represent oxidation. (b) Peak separation, the difference between oxidation and reduction potentials, as a function of the oxide thickness at scan rates: 0.1, 1 and 10 V/s. The peak separation increases with increasing oxide thickness and increasing scan rates.

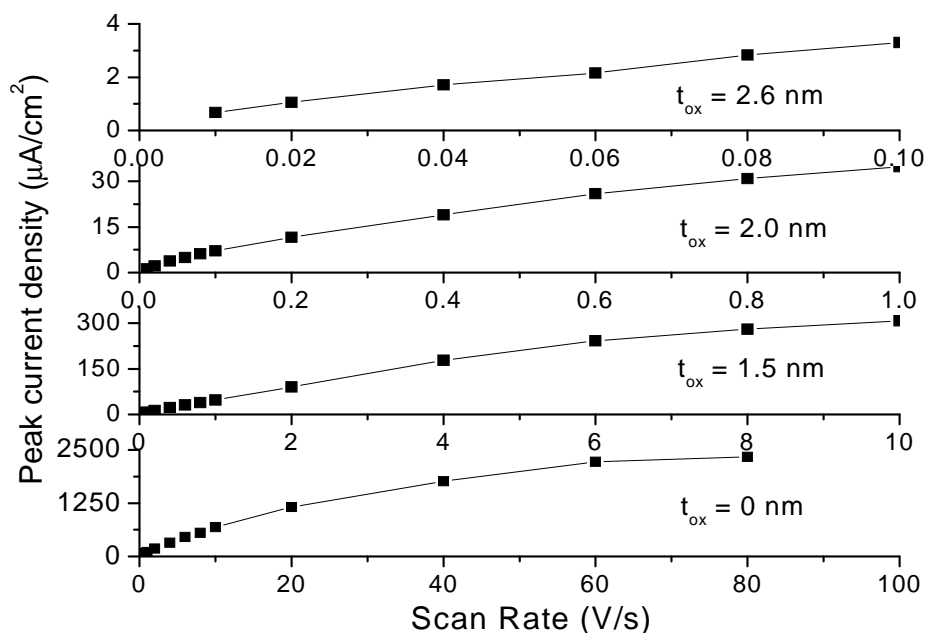


Figure 4.7 Peak current density versus scan rate for EMOS capacitors with 0, 1.5, 2.0 and 2.6 nm SiO_2 . The curves deviate from linearity at higher scan rates. Scan rate at which deviation starts decreases with increasing t_{ox} .

4.3.4 Conductance measurements

As mentioned in section 4.3.1, CV and GV measurements on EMOS capacitors showed peaks corresponding to oxidation and reduction of molecules. These impedance measurements, particularly GV, were also measured at varying small signal frequencies (f_{ac}) and small signal amplitudes (v_{ac}). The occurrence of redox peaks and the conductance peak amplitudes were observed to be strongly dependent on t_{ox} , f_{ac} and v_{ac} .

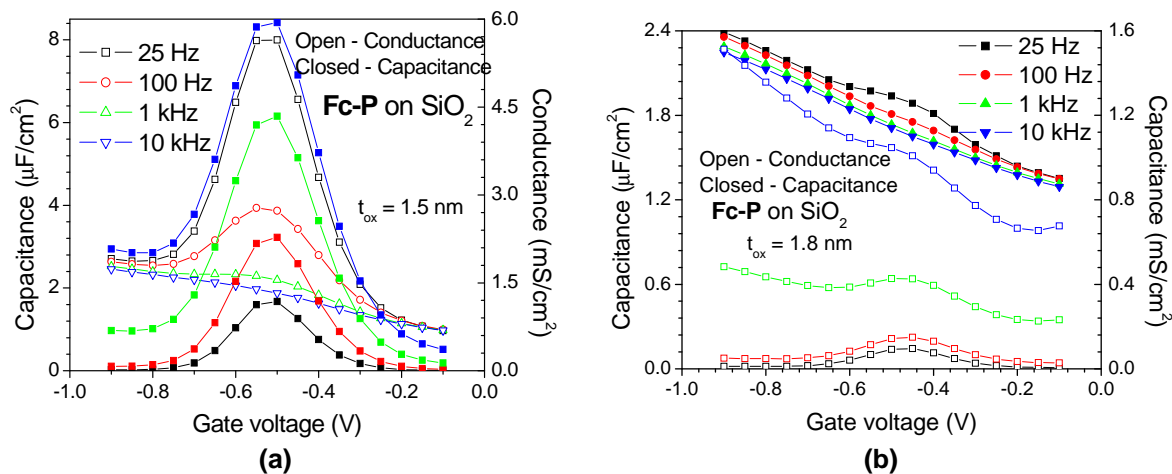


Figure 4.8 CV and GV characteristics of EMOS capacitors with **Fc-P** 1.5 nm **(a)** and 1.8 nm **(b)** SiO₂ at frequencies ranging from 25 Hz to 10 kHz. Only oxidation scans are shown. Capacitance peaks decrease and conductance peaks decrease with increasing frequency. Peaks in GV are not observed beyond a certain frequency (cut-off frequency). This frequency decreases with increasing t_{ox} .

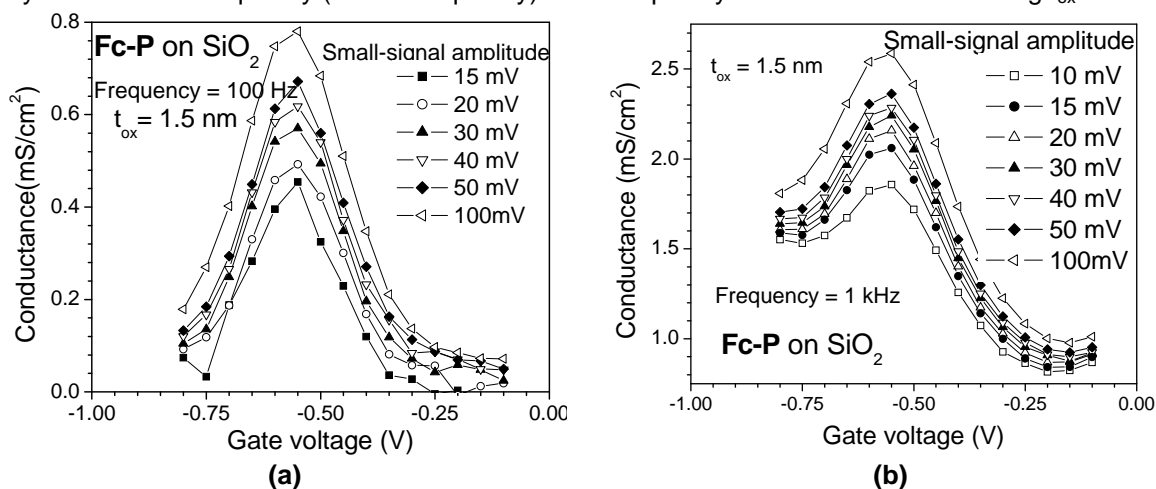


Figure 4.9 GV characteristics with **(a)** varying small-signal amplitude (v_{ac}) and **(b)** varying small-signal frequency (f_{ac}) for an EMOS capacitor with **Fc-P** on 1.5 nm SiO₂. Peak conductance increases with increasing v_{ac} and/or f_{ac} .

Figs. 4.8 (a) and (b) show CV and GV characteristics of EMOS capacitors for two different t_{ox} at varying frequencies. The peak capacitance decreases and the peak conductance increases with increasing f_{ac} . In GV measurements, the base conductance is also observed to increase with increasing f_{ac} . The impedance spectroscopy measurements were made in the parallel mode. Hence, at higher frequencies, the measured capacitance decreases due to increased contribution from the series resistance (R_s) [4]. However, since the measured conductance is not affected as much by the series resistance even at higher frequencies [4], the conductance due to redox increases with increasing f_{ac} . This is because, as long as the electron-transfer rate is faster than f_{ac} , the number of molecules participating in redox at any dc gate voltage will increase with increasing f_{ac} . Consequently, the small-signal conductance will increase with increasing f_{ac} , as observed in Figs. 4.8 (a) and (b). However, this is true only till a particular frequency, above which no conductance peaks were observed. This is due to f_{ac} exceeding the overall electron-transfer rate. This cut-off frequency

decreases with increasing t_{ox} , as expected, since the electron-transfer rate through the SiO_2 decreases as t_{ox} increases. This is a function of the tunneling distance (t_{ox}), the density of charges and f_{ac} . In other words, the maximum frequency up to which tunneling can be observed (cut-off frequency) decreases as the tunneling distance (t_{ox}) increases and the charge density decreases. Similar kind of behavior is also seen with deliberately placed near-interface oxide traps in MOS capacitors [7].

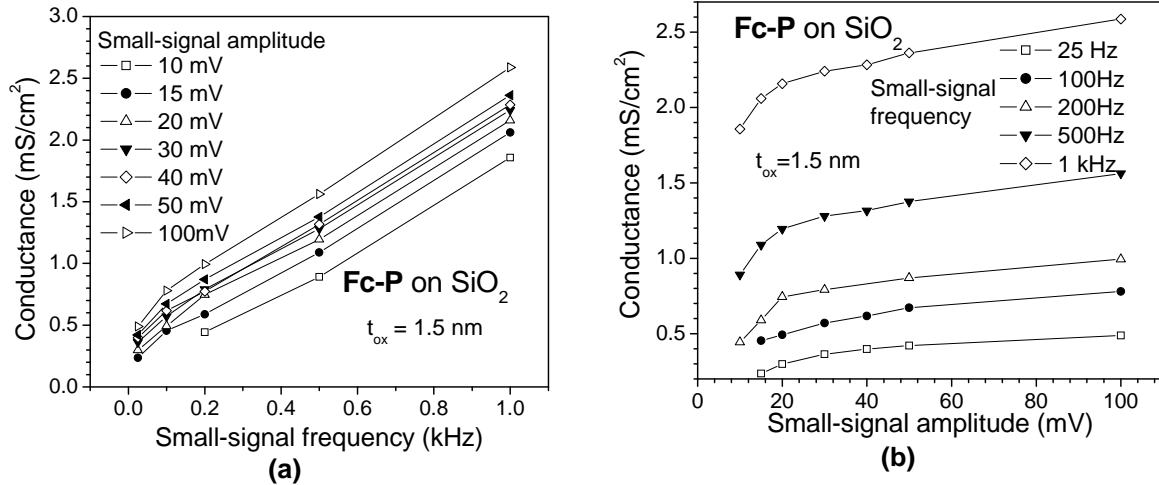


Figure 4.10 Peak conductance versus (a) small-signal frequency (f_{ac}) and (b) small-signal amplitude (v_{ac}) for an EMOS capacitor with **Fc-P** on 1.5 nm SiO_2 . Conductance increases linearly with f_{ac} and small v_{ac} . At large v_{ac} , the behavior deviates from linearity.

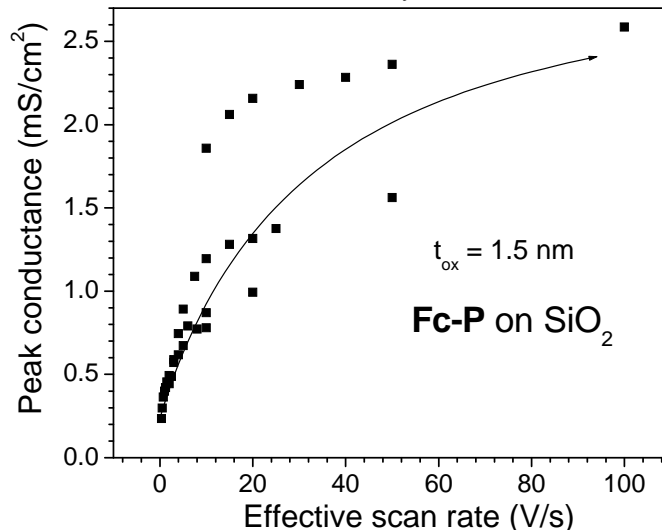


Figure 4.11 Peak conductance versus effective scan rate ($f_{ac} \times v_{ac}$) for an EMOS capacitor with **Fc-P** on 1.5 nm SiO_2 . Points are experimental data. Line is an approximate fit to the data points.

The frequency and amplitude dependences of GV measurements are very similar to those of ac voltammetric measurements from electrochemistry [8-10]. A theoretical model has been developed and reported for the average ac current as a function of f_{ac} and v_{ac} [8]. This model assumes that the redox process is reversible, i.e., f_{ac} is lower than the electron-transfer rate. In this frequency range, $f_{ac} \leq f_{cut-off}$, the peak average ac current increases with f_{ac} and v_{ac} . The small-signal conductance, which is directly related to the peak average ac current, was observed to follow the same trend, as shown in

Figs. 4.9 (a) and (b). The dependence of the peak conductance on f_{ac} is linear (Fig. 4.10 a), whereas that on v_{ac} is linear when v_{ac} is small and saturates at higher amplitudes (Fig. 4.10 b). These observations are in excellent agreement with the Nernstian electron source model for ac voltammetric response [8]. Another way to look at this dependence on f_{ac} and v_{ac} is to estimate an “effective scan rate” at any dc voltage as a function of f_{ac} and v_{ac} . An effective scan rate, v_{eff} , can be defined as $f_{ac} \times v_{ac}$. A plot of peak conductance versus v_{eff} (Fig. 4.11) shows a linear dependence for small v_{eff} and deviation from non-linearity for higher v_{eff} . This behavior is similar to the dependence of CyV peak current on scan rate.

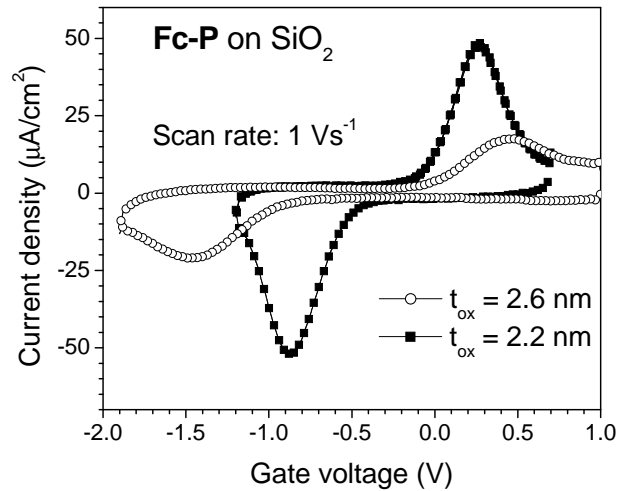


Figure 4.12 CyV of EMOS capacitors with 2.2 and 2.6 nm oxide, showing that the voltage ranges in which the oxidation and reduction processes occur are completely separated from each other.

4.3.5 Separation of charging and discharging processes

As discussed in the previous sections, the SiO_2 layer acts as a tunneling barrier to electrons and, as the thickness is increased, the gate voltage needed for transfer of electrons between the molecules and substrate increases. For oxides thicker than approximately 1.8 nm, the voltage ranges in which oxidation and reduction processes occur are completely separated from each other. This can be seen in Fig. 4.12, which shows CyV characteristics of EMOS capacitors with 2.2 and 2.6 nm SiO_2 at a scan rate of 1 V/s. For instance, in the CyV of 2.2-nm SiO_2 capacitor, the peaks can be defined from -0.30 to -1.25 V for oxidation (oxidizing range) and from -0.20 to 0.75 V for reduction (reducing range). Hence, there exists a range of voltage (stable range) in between the oxidizing and reducing ranges (in this case, from -0.2 to -0.3 V), where the molecules remain at the same state as they were previously. In other words, if the molecules were neutral, then application of any voltage in the stable range will not oxidize the molecules. On the other hand, if the molecules were oxidized and positively charged, then only the application of a voltage in the reducing range will result in bringing the molecules back to the neutral state. The retention time of the molecules in the stable range will depend on the retention properties of the molecules, tether [11], and oxide thickness, as will be discussed later in the chapter. The stable range for EMOS capacitors increases with increasing t_{ox} .

increasing from 100 mV (from -0.2 to -0.3 V) for 2.2 nm to 400 mV (from -0.2 to -0.6 V) for 2.6 nm (Fig. 4.12). This stable voltage range is essential for nondestructively “reading” memory cells based on this hybrid silicon-molecular technology. When molecules are incorporated in FET-type structures for FLASH applications, the drain current of the resulting device can be read at a gate voltage in the stable range, thereby not affecting the state of the molecules. Details about this structure and electrical characteristics are discussed in chapter 6.

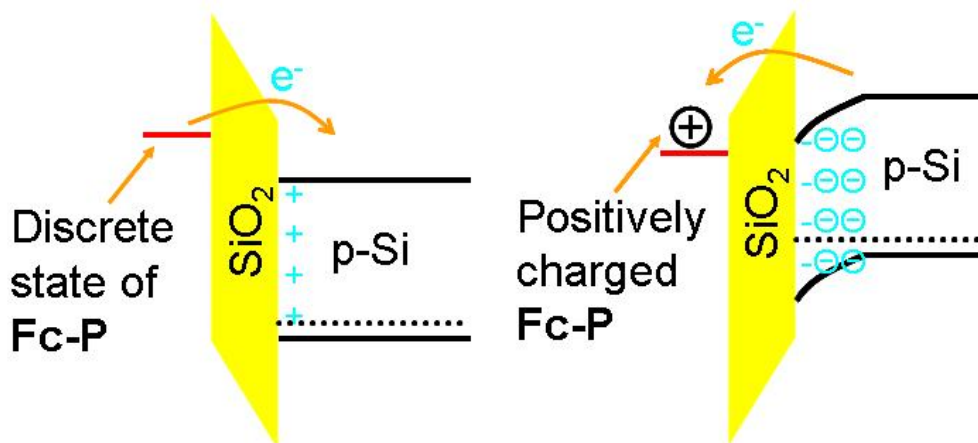


Figure 4.13 Energy band diagrams depicting the oxidation and reduction processes of **Fc-P** attached to SiO₂ on p-Si substrate.

This increasing peak separation with increasing t_{ox} can also be explained using energy band diagrams. Fig. 4.13 shows the energy diagrams for molecules on SiO₂. The discrete molecular orbitals are characteristic of molecules in the monolayer. As a negative gate voltage ramp is applied, the discrete molecular energy levels are raised. The Si surface would be in the accumulation region. Oxidation occurs when electrons tunnel from the HOMO of the molecules to the conduction band of Si. For this process to occur, not only does the HOMO have to be higher than the conduction band edge (E_C) of Si, but the electric field across SiO₂ also needs to be high enough. As the tunneling distance (t_{ox}) increases, the difference between HOMO and E_C , and the electric field across SiO₂ need to increase for tunneling to take place. As a result, the negative gate voltage required for oxidation increases with increasing t_{ox} . For the reduction process, electrons need to tunnel from the Si conduction band to the discrete molecular orbitals through SiO₂. The electric field across SiO₂ needs to be in the opposite direction to that during oxidation. Again, thicker oxides would require larger voltage drops across SiO₂ for the tunneling process to occur. Therefore, the voltage at which reduction occurs becomes more positive as t_{ox} is increased. The behavior of electron-tunneling current during the reduction process is discussed in more detail in section 4.3.7.

4.3.6 Butler-Volmer theory for electron-transfer rates

Butler-Volmer theory, from electrochemistry, is the simplest theory used to describe electron transfer of surface attached redox-active species [6]. According to this theory, the rates of electron transfer from and to the molecules, k_{ox} and k_{red} , respectively, are given by the following equations:

$$k_{ox} = k^0 \exp[\alpha(V - V^0)] \quad (1)$$

$$k_{red} = k^0 \exp[\alpha(V - V^0)] \quad (2)$$

Here, k^0 is the charge-transfer rate constant at V^0 , V is the applied potential (in this case, the gate voltage) and α is the charge transfer coefficient, which is a measure of the symmetry of the energy barrier for electron transfer from and to the molecules. For a perfectly symmetrical barrier, α takes a value of 0.5 [5].

The presence of the stable range for EMOS capacitors and its increase with increasing t_{ox} can be explained using the above equations. It can be seen from these equations that the oxidation and reduction rates are equal at V^0 . Hence, V^0 can be approximated as the average of V_{PO} and V_{PR} (a voltage that is equally away from both the oxidation and reduction peak potentials). As the gate voltage becomes more negative than V^0 , k_{ox} increases and k_{red} decreases exponentially, and vice versa. Since the peak separation at a given scan rate from CyV increases with increasing t_{ox} (Fig. 4.6), it can be concluded that the k^0 values decrease with increasing t_{ox} . Due to significant decrease in k^0 with increasing t_{ox} , the over-potential ($|V - V^0|$) required to increase the electron-transfer rates to significant values also increases significantly. Thus, there exists a range of voltages on either sides of V^0 where both k_{ox} and k_{red} are very low. This is the stable range, and electron exchange between molecules and the substrate happens at a very slow rate in this voltage range. Hence, application of a voltage in this range, after oxidizing the molecules, will preserve the charged state. However, positive charges will eventually leak off, depending on the oxide leakage, which will depend on t_{ox} .

4.3.7 Electron tunneling current from Si

For EMOS capacitors, discharging of molecules occurs when electrons tunnel from the Si surface to the molecules through the SiO_2 layer. As discussed earlier, direct tunneling mechanism dominates the electron tunneling current for $t_{ox} \leq 3.5$ nm and small gate voltages; Fowler-Nordheim (FN) tunneling mechanism dominates otherwise. The current I_{dir} and I_{FN} are given by the following expressions [4].

$$I_{dir} = A_G A x_{ox}^2 \exp \left(\frac{-B \left[1 - \left(1 - qV_{ox} / \Phi_B \right)^{1.5} \right]}{x_{ox}} \right) \quad (3)$$

$$I_{FN} = A_G A x_{ox}^2 \exp\left(\frac{-B}{x_{ox}}\right) \quad (4)$$

In these expressions, V_{ox} is the voltage drop across SiO_2 , ξ_{ox} is the electric field across SiO_2 given by $\frac{V_{ox}}{t_{ox}}$, A_G is the gate area of the device, Φ_B is the barrier height at Si-oxide interface, and A and B are usually considered constants. In both these cases, the current increases exponentially as V_{ox} increases. In an EMOS capacitor, the gate voltage distributes across different layers such that

$$V_G = f_{ms} + V_{dl} + V_{ox} + y_{Si} \quad (5)$$

In this expression, ϕ_{ms} is a constant for a given EMOS capacitor, whereas V_{dl} , V_{ox} and ψ_{Si} vary with V_G . V_{ox} and V_{dl} are both voltage drops across dielectrics and their relative magnitudes depend on their dielectric constants, k_{ox} and k_{dl} . Since, k_{dl} (~ 60) is much greater than k_{ox} (3.9), V_{dl} is negligible compared to V_{ox} . ψ_{Si} , the Si surface potential, depends on the region of operation of the Si surface. There can be 4 possible regions of operation;

1. Accumulation: $\psi_{Si} \approx 0$; Density of electrons at Si surface is low $n = \frac{n_i^2}{p}$.
2. Depletion & Weak inversion: $\psi_{Si} > 0$; $y_{Si} = \frac{qN_A d_B^2}{2e_{Si}}$, where d_B is the depletion width which increases with increasing V_G ; Density of electrons at Si surface is low.
3. Deep-depletion: Same as "depletion"
4. Strong Inversion: $\psi_{Si} > 0$; $\psi_{Si} \approx 2\phi_F = \text{constant}$; ψ_{Si} does not increase with further increase in V_G . Density of electrons is high.

The drop across SiO_2 , V_{ox} , depends on V_G and ψ_{Si} and is given as

$$V_{ox} = V_G - f_{ms} - V_{dl} - y_{Si} \quad (6)$$

As V_G increases in the positive direction, Si surface goes from accumulation to depletion. In the depletion region, most of the gate voltage is dropped across the Si surface in order to accommodate the depletion charges (that compensate the gate charges). Hence, V_{ox} is small. Also, the electrons necessary for the tunneling current through SiO_2 must be provided by thermal generation of minority carriers at the Si surface.

As V_G is increased further, the density of electrons at the Si surface increases. At the threshold voltage, V_T , of the capacitor, an inversion layer is created at the surface, and the density of electrons at the surface is as high as that of holes in the bulk p-Si substrate. Any further increase in V_G will

have negligible impact on ψ_{Si} since there're a large number of available electrons to balance the positive gate charges. Consequently, any gate voltage beyond V_T almost completely drops across SiO_2 and the electrolytic double layer capacitor. Since k_{dl} is much greater than k_{ox} , most of the voltage will drop as V_{ox} . Therefore, increasing V_G beyond V_T results in an exponential increase in the tunneling current (I_{dir} or I_{FN}).

In a capacitor structure, inversion layer is created at the surface via thermal generation of minority carriers (electrons). If the input voltage ramp rate is faster than the thermal generation rate, then an inversion layer will not be created even if V_G is greater than V_T . In such cases, ψ_{Si} will increase even after V_T in order to provide the necessary negative charges to balance the positive charges on the gate. The surface of Si is said to be in deep-depletion as the depletion regions extends deep into the substrate. Therefore, most of the applied gate voltage drops across this depletion region, and V_{ox} does not increase as it would in the presence of an inversion layer. As a result, the tunneling current remains saturated and does not increase even for large gate voltages [12-14]. The limited availability of electrons (minority carriers) also limits the electron tunneling current.

The minority carrier generation rate can be increased by introducing an external light source. In the presence of light, it is possible to create an inversion layer even at fast voltage ramp rates. Therefore, V_{ox} , density of surface electrons and the tunneling current will increase with increasing V_G beyond V_T .

The electron tunneling current from Si through SiO_2 heavily is responsible for the reduction of molecules in EMOS capacitors with p-Si substrates. The reduction properties of these devices were studied as a function of t_{ox} and scan rate. Very low scan rate measurements were included in order to be able to create inversion layers in the p-Si substrates. An external light source was also incorporated in order to observe the effect of light. These results are discussed in the next section and correlated with the electron tunneling current.

4.3.8 V_T – assisted reduction

4.3.8.1 Two-step reduction

In order to investigate the kinetics of reduction of molecules in EMOS capacitors, CyV measurements at very small scan rates were performed. Fig. 4.14 shows CyV characteristics of capacitors with **Fc-P** on 2.0 and 2.6 nm SiO_2 at a very low scan rate of 10 mV/s. The reduction process appears as two distinct peaks in the positive current. No peaks were observed in capacitors without molecules. The sum of the areas under the two peaks equals the area under the single oxidation peak, indicating that both positive current peaks are indeed associated with the reduction of oxidized molecules. These observations can be understood by considering that the reduction process involves the tunneling of electrons from the Si substrate to the molecules through the oxide barrier.

The first peak occurs at the reduction voltage of the device at that scan rate. At low scan rates, Si substrate is still in accumulation when this voltage is reached. Therefore, as discussed in the previous section, the tunneling current through SiO₂ is limited due to the limited availability of electrons in the p-Si substrate. Consequently, this limited current results in only a limited number of molecules getting reduced. As the gate voltage is made more positive and reaches the threshold voltage (V_T) of the capacitor, an inversion layer is formed at the Si surface. These measurements were made in the presence of light. Due to the low scan rate and presence of light, the electron generation rate is high enough to create an inversion layer. This exponentially increases the number of electrons available at the Si surface. Furthermore, as V_G is increased beyond V_T, almost all of the gate voltage drops across SiO₂ since ψ_{Si} remains constant. The creation of an inversion layer and the increase in V_{ox} results in an increase in the tunneling current, thereby enabling the reduction of the remaining charged molecules. This results in the occurrence of the second peak at the onset of inversion. These results show that the reduction process in EMOS capacitors takes place in two steps – one that is limited by electron-tunneling current and another that is V_T-assisted.

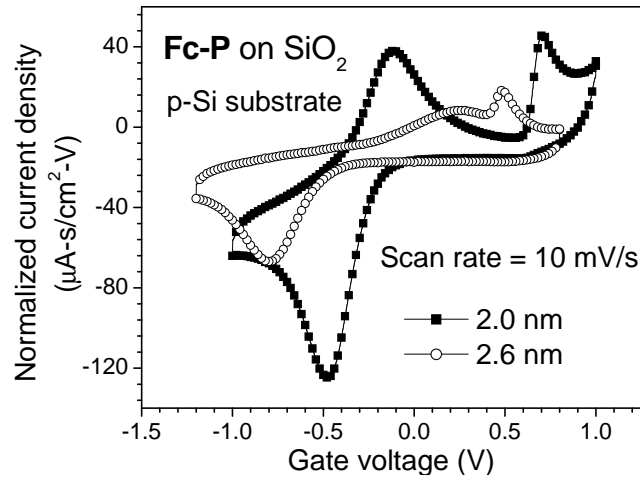


Figure 4.14 CyV characteristics of EMOS capacitors with **Fc-P** on 2.0 and 2.6 nm SiO₂ at a scan rate of 10 mV/s, showing the reduction process occurring in two steps.

4.3.8.2 Effect of scan rate

Figs. 4.15 (a) and (b) show the CyV characteristics of EMOS capacitors with 2.0 and 2.6 nm SiO₂ at varying scan rates. As the measurement scan rate is increased, the reduction voltage becomes more positive, but V_T remains the same (Fig. 4.16). The threshold voltage of a capacitor is independent of the scan rate and is usually given by

$$V_T = V_{FB} + 2f_F + \frac{\sqrt{2qe_{Si}N_A(2f_F)}}{C_{ox}} \quad (7)$$

As long as the generation rate of electrons is higher than the input scan rate (the generation rate can be increased by using an external light source), the Si surface will be inverted at V_T irrespective of the scan rate. As shown in Fig. 4.15, the first reduction peak voltage becomes more positive with

increasing scan rate, whereas the voltage at which the second peak occurs remains the same. Hence, as the scan rate increases, the first reduction peak moves closer and eventually merges with the second peak. The 2 peaks are found to merge at 100 and 1000 mV/s for EMOS capacitors with 2.0 and 2.2 nm, respectively. For a given scan rate, the reduction voltage is more positive for a thicker oxide due to the increased barrier thickness. Hence, the scan rate at which the peaks merge decreases with increasing oxide thickness. Once the peaks merge, any increase in the measurement scan rate results in only a single peak that occurs beyond V_T .

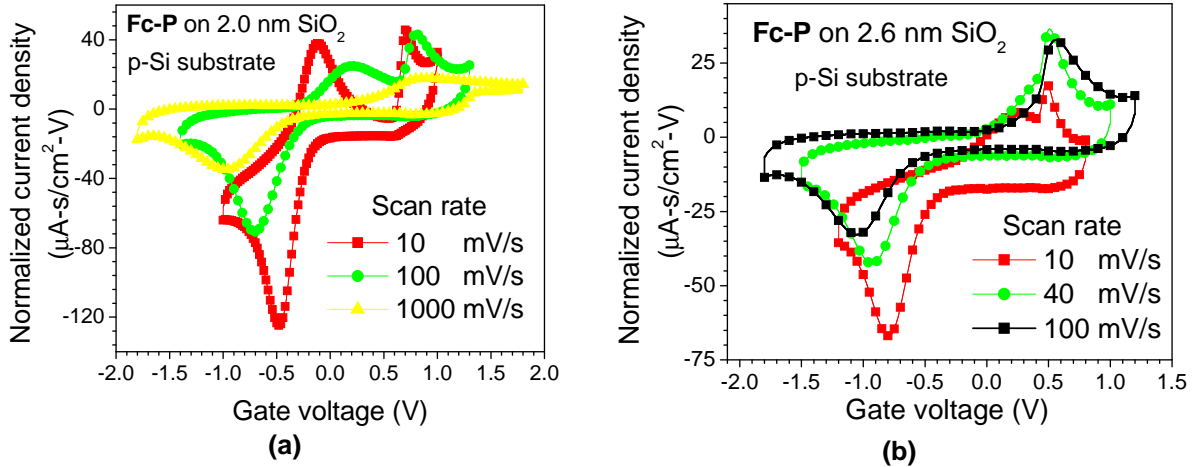


Figure 4.15 CyV characteristics of EMOS capacitors with **Fc-P** on (a) 2.0 nm and (b) 2.6 nm SiO_2 at low scan rates. At very low scan rates, two reduction peaks are observed, which merge into one at higher scan rates. The scan rate at which peaks merge decreases with increasing t_{ox} .

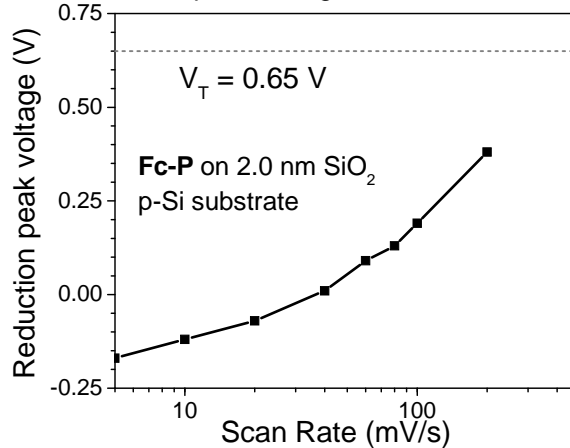


Figure 4.16 Reduction peak voltage versus scan rate for an EMOS capacitor with **Fc-P** on 2.0 nm SiO_2 . The reduction peak voltage increases and approaches V_T as the scan rate is increased.

4.3.8.3 Effect of SiO_2 thickness

The electron-tunneling current also strongly depends on the SiO_2 thickness. Thinner oxides have higher currents for the same V_{ox} due to the larger electric field. Fig. 4.17 shows the CyV behavior of an EMOS capacitor with a thinner SiO_2 (1.8 nm). Since this device has higher electron-tunneling currents, the extent to which the reduction process is limited at the first step is lesser. This is evident from Fig. 4.17, where at a low scan rate of 10 mV/s, the contribution from the second V_T -

assisted reduction peak is much less compared to that from the first peak. This indicates that most of the molecules are reduced when the reduction voltage is reached. However, as the scan rate is increased to 500 mV/s, the amount of molecules getting reduced at the first step decreases, which is seen as an increased contribution to the reduction current from the V_T -assisted peak.

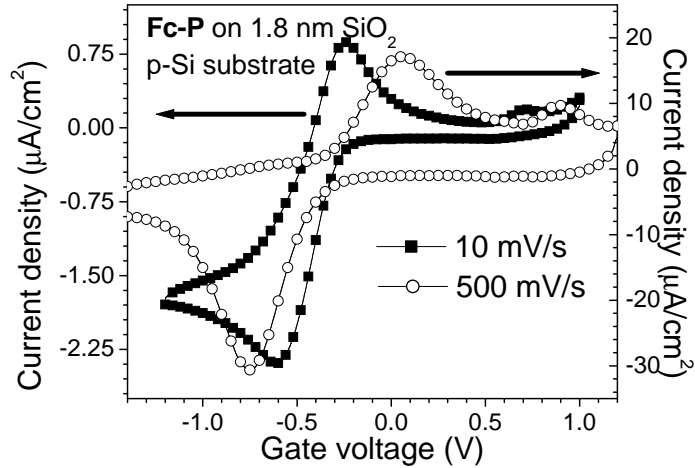


Figure 4.17 CyV characteristics of EMOS capacitor with **Fc-P** on 1.8 nm SiO_2 : contribution from V_T -assisted peak increases with increasing scan rate.

4.3.8.4 Effect of light

As mentioned previously, if measurement scan rates are faster than the thermal generation rate of electrons, then an inversion layer will not be created even if V_G is greater than V_T . As a result, the Si surface will go into deep-depletion and the tunneling current does not increase. However, in the presence of an external light source, the generation rate of electrons is increased and inversion layer is created.

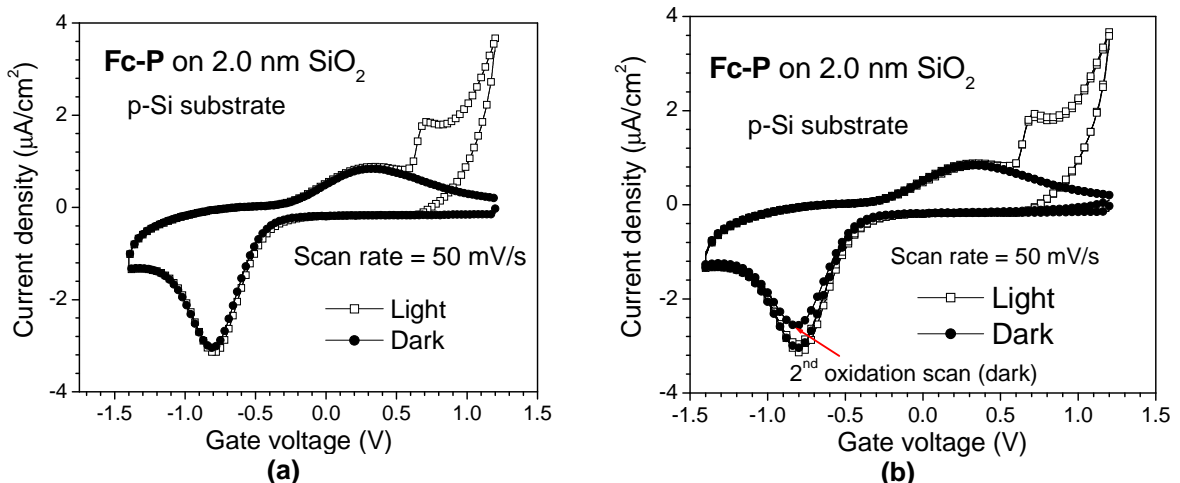


Figure 4.18 (a) CyV characteristics of an EMOS capacitor with **Fc-P** on 2.0 nm SiO_2 in the presence and absence of an external light source. Scan rate is 50 mV/s. Second reduction peak is observed only in the presence of light. **(b)** Same as **(a)** with two cycles each. The oxidation peak in the 2nd cycle is lower than that in the 1st one in the absence of light. With light, currents from 1st and 2nd cycles overlap each other.

Fig. 4.18 (a) shows CyV characteristics of an EMOS capacitor with 2.0 nm SiO₂ with and without an external light source at a scan rate of 100 mV/s. A second reduction peak is observed only in the presence of light. Fig. 4.18 (b) shows two successive CyV scans of the same capacitor at 100 mV/s. In the absence of light, second reduction peak is not observed and not all the oxidized molecules are discharged in the first scan. Therefore, in the subsequent scan, only the molecules that got discharged under the first reduction peak get oxidized. This can be clearly seen as a reduction in the oxidation current. On the other hand, in the presence of light, the second reduction peak is observed and both the CyV scans overlap one another. This indicates that all molecules are reduced only after the occurrence of the second reduction peak.

4.3.9 Charge retention measurements

The presence of a stable range for EMOS capacitors with t_{ox} greater than 1.8 nm, as discussed in section 4.3.5, enabled the study of charge retention properties of these structures and their dependence on t_{ox} . Oxidizing voltages were applied during two successive CyV scans, with a wait time between the two scans. The wait time was varied between 0 and 300 s. No reducing voltage was applied in between the two scans. Therefore, any positive charges lost during the wait time would be due to leakage rather than due to intentional reduction. The starting voltage in each oxidizing scan was in the stable range. Since the area under the peak gives the number of charges, the difference in the areas between the two scans would give the number of charges remaining after the wait time. A plot of the fraction of charges remaining versus the wait time can then be used to calculate the retention times of these structures. Another variation of this technique is to apply a reducing voltage in the second scans. The area under the peak will then directly give the number of charges remaining after the wait time.

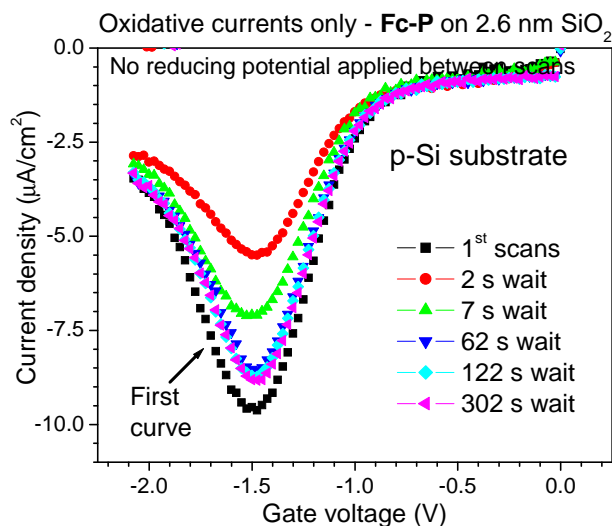


Figure 4.19 CyV scans of an EMOS capacitor with **Fc-P** on 2.6 nm oxide. First curve (black) represents the oxidation of the molecular monolayer from its neutral state. The subsequent curves are scans after initial oxidizing scan with a wait time in between the two scans. The wait time was varied from 0 to 300 s. The voltage applied during the wait time, i.e., V_w , was 0 V.

Fig. 4.19 shows the oxidizing scans of an EMOS capacitor with 2.6 nm oxide. The first curve represents the oxidation of molecules from their neutral state. The subsequent scans represent the second oxidizing scans after wait times varying from 0 to 300 s. As can be seen from this figure, the area under the peak increases with increasing wait time between the two oxidizing scans. This indicates that the number of molecules that lost their positive charge during the wait time increased with increasing wait time. Electrons from the substrate tunnel through the oxide barrier and neutralize the positively charged molecules. Though a reducing voltage is required for this reduction process to occur completely and at a significant rate, some of the molecules lose their positive charges due to oxide leakage. Figs. 4.20 (a) and (b) show the behavior of an EMOS capacitor with 2.0 nm oxide. The peak separation ΔV_P is smaller for this structure due to a thinner SiO_2 . As seen from these figures, the number of charges remaining decreases with increasing wait time. The area under the oxidation peak, which is a measure of the number of molecules that had been neutralized, increases with increasing wait time [see Fig. 4.20 (a)], whereas, the area under the reduction peak, decreases with increasing wait time [see Fig. 4.20 (b)]. The sum of the number of charges neutralized and the number of charges remaining should be equal to the number of molecules in the monolayer. This was indeed true, as it was observed that the sum of the areas under the oxidation and reduction peaks after a given wait time was equal to the area under the oxidation peak in the initial scan.

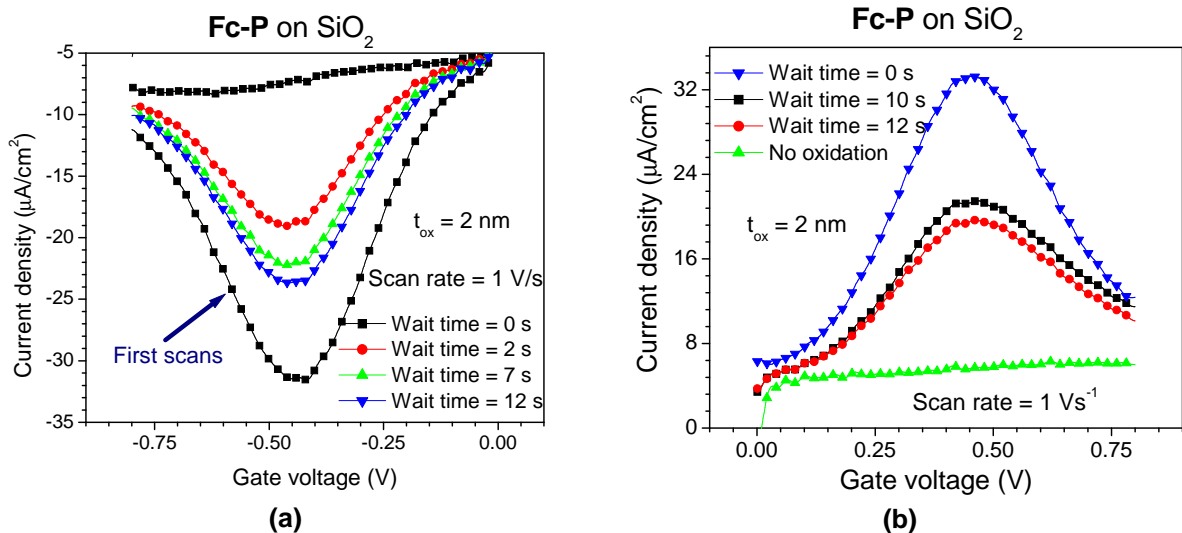


Figure 4.20 (a) CyV scans of an EMOS capacitor with **Fc-P** on 2.0 nm oxide. The first curve represents the oxidation of the molecular monolayer from its neutral state. The subsequent curves are scans after the initial oxidizing scan with a wait time in between the two scans. The wait time was varied from 0 to 12 s. The voltage applied during the wait time (V_w) was 0 V. **(b)** CyV scans of the same capacitor with the voltage in the reducing range. Oxidizing scans, with a wait time between the oxidizing and reducing scans, preceded all the curves, except the one without a peak. The wait time was varied between 0 and 12 s. The voltage applied during the wait time (V_w) was 0 V.

Fig. 4.21 shows the plot of the fraction of charges remaining versus the wait time for EMOS capacitors with two different t_{ox} (2.0 and 2.6 nm). It can be seen from this figure than the number of charges decays exponentially with time. Since the electron-tunneling rate across SiO_2 depends exponentially on the field across it, the number of charges remaining in the monolayer also decreases

exponentially with time. Thicker oxides are expected to have lower electron-tunneling rate between the substrate and molecules. Thus, the charge retention times are expected to be longer for EMOS capacitors with thicker oxides. However, the data in Fig. 4.21 suggest that the fraction charges remaining in the monolayer is similar for both 2.0 and 2.6 nm oxides. The starting voltages in the oxidizing scans are the same (0 V) for both EMOS capacitors. However, the oxidizing range for the EMOS capacitor with 2.6 nm is from -0.9 to -2.1 V and that for the capacitor with 2.0 nm oxide is from -0.3 to -1.2 V. The application of voltages much further away from the oxidizing range and the longer duration of time before the actual application of the oxidizing voltage cause the reduction of additional numbers of molecules than expected in the capacitor with 2.6 nm oxide. Had the over-potential during the wait time been 0 V ($k_{ox} = k_{red}$) for both capacitors, then the fraction of charge remaining would have depended solely on the oxide thickness. However, since the voltage during the wait time (V_w) was 0 V, the over-potential for the capacitor with 2.6 nm oxide was more positive than that for the capacitor with 2.0 nm oxide. The difference between V_w and V_0 , $\Delta V_w = V_w - V_0$, was 0.7 and 0 V for the two capacitors. Though V_w was not in the reducing range, the over-potentials (ΔV_w) were such that the reduction rate was slightly higher for the capacitor with 2.6 nm oxide than for the one with 2.0 nm oxide.

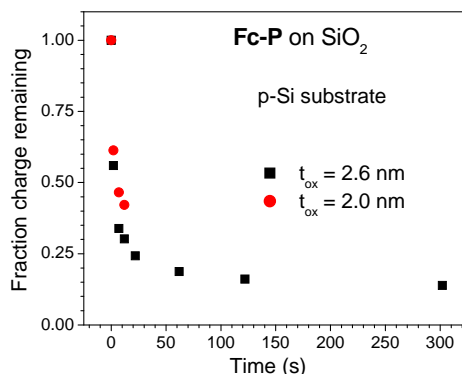


Figure 4.21 Fraction of charges remaining versus wait time for EMOS capacitors with **Fc-P** on 2.0 and 2.6 nm SiO_2

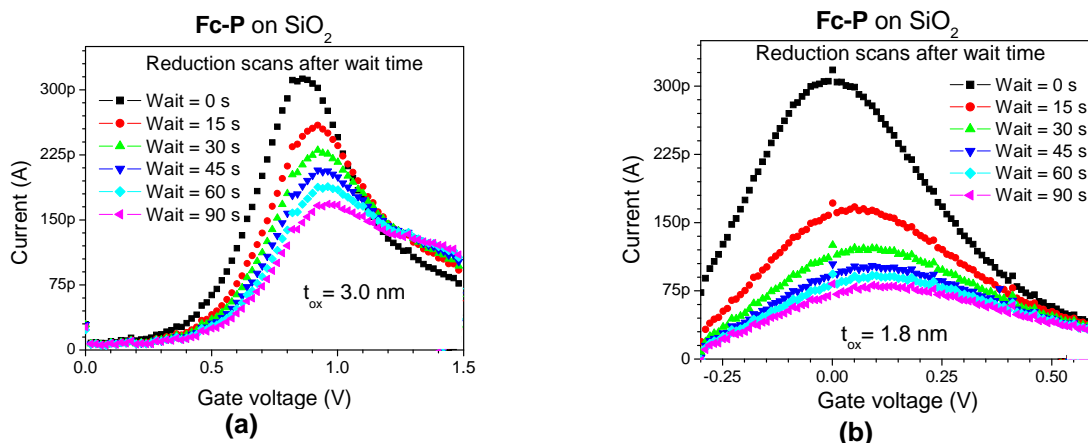


Figure 4.22 Reduction scans of an EMOS capacitor with **Fc-P** on (a) 3.0 nm and (b) 1.8 nm oxide. All scans were after an initial oxidation scan and a wait time, which was varied from 0 to 90 s. The voltage applied during the wait time (V_w) was 0 V for (a) and -0.3 V for (b).

When the applied V_w was such that ΔV_w was closer to 0 V, it was observed that, for a given wait time, the number of charges retained was more for a capacitor with thicker oxide than for one with a thinner oxide. Figs. 4.22 (a) and (b) show the reduction scans after oxidation with wait times varying from 0 to 90 s for two capacitors with 3.0 and 1.8 nm oxide, respectively. The voltages applied during the wait times were 0 and -0.3 V for the two capacitors, respectively (ΔV_w were 0.4 and 0 V). As can be seen from the figures, the fraction of charges remaining (area under the reduction peak) decreased more for the sample with 1.8 nm oxide than for the one with 3.0 nm oxide.

4.3.10 Pulse measurements

Charge retention properties of EMOS capacitors can also be measured using pulse measurement techniques or Open Circuit Potential Amperometry (OCPA) [15]. In these techniques, a negative voltage pulse is applied to oxidize the molecules. The amplitude and duration of the pulse depend on the SiO_2 thickness, and are such that all the molecules in the monolayer get oxidized. Thicker oxides require greater amplitudes and longer pulse durations. The external circuit is disconnected and the device is left in the open-circuit state after the duration of the pulse. A voltage more positive than the reduction potential is applied after varying disconnect times and the current through the device is monitored. At the application of this voltage, all the molecules that remain in the oxidized state would get discharged, resulting in a transient discharge current. The amount of charges that remained in the monolayer can be obtained from the area under the current-time plot. Charge retention times can then be derived from a plot of charges remaining versus wait time. In the OCPA technique, the voltage applied after the disconnect is the OCP (Open Circuit Potential), which is the voltage that the device attains after all the charging currents have decayed. The time taken for half the number of charges in the monolayer to decay ($t_{1/2}$) was observed to be 90 s for **Fc-P** directly on Si and a few hundred seconds for **Fc-P** attached to SiO_2 on Si. This $t_{1/2}$ was found to increase with increasing t_{ox} . Detailed discussions and results will be provided in another student's dissertation.

4.3.11 Summary

Monolayers of **Fc-P** have been formed on SiO_2 surfaces via the formation of P-O-Si covalent bonds. The charging and discharging voltages of molecules on SiO_2 have been tuned by varying the oxide thickness. The write voltage (oxidation) becomes more negative and the erase voltage (reduction) becomes more positive with increasing t_{ox} , thereby increasing the separation between the oxidizing and reducing voltage ranges. The charge transfer rates between the molecules and the Si substrate were strongly dependent upon the tunneling currents through the SiO_2 barrier. This was illustrated by scan rate dependence in CyV characteristics, and small-signal frequency & amplitude dependence in GV characteristics.

The reduction process was limited by the electron tunneling current from Si through the SiO_2 barrier. Consequently, reduction was found to occur at two steps – one at the reduction voltage and

the other at the threshold voltage of the capacitor. Experiments were performed without any external light source, which prevented the creation of an inversion layer. This resulted in deep depletion of the Si surface and saturation of the electron tunneling current. In such situations, the second reduction process was not observed and not all molecules were discharged. This limited reduction also resulted in enhance charge retention times for molecules on SiO₂. Charge retention times were observed to increase with increasing t_{ox}.

The mechanisms involved in charging and discharging of molecules in monolayers of **Fc-P** attached to SiO₂ surfaces on p-Si substrates have been understood. This understanding can be extended to three-state porphyrin molecules and molecules with higher number of states.

After developing an understanding of the mechanisms involved in writing, erasing and storing of charges in EMOS capacitor with monolayers of **Fc-P** on SiO₂, these molecules were incorporated in FET structures in order to modulate their device characteristics by charging and discharging the molecules. The next section describes the working of such a “moleFET” and discussed their current-voltage characteristics.

4.4 MoleFET Device

Fig. 4.23 shows the schematic of a “moleFET” device, where molecular monolayers are incorporated on SiO₂ in the channel regions of FET devices. The FET structures were fabricated using replacement gate technology, as explained in chapter 2. Low temperature oxidation process was used to grow the gate oxides. Monolayers of **Fc-P** were formed on the gate oxides via the attachment procedure listed in Table 2.2. Electrolyte gate was used to perform electrical characterization. Both p-FET and n-FET devices were employed. FET current-voltage characteristics were performed using HP 4155B Semiconductor Parameter Analyzer.

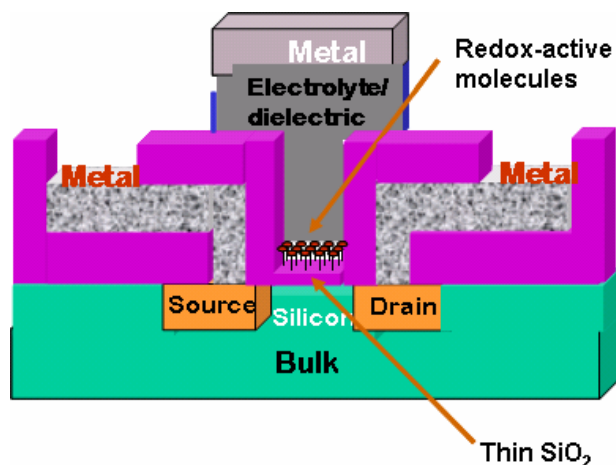


Figure 4.23 Schematic of a moleFET incorporating redox-active molecules on SiO₂ surfaces in the channel region of an FET structure.

The motivation behind fabrication and characterization of the moleFET device is to investigate the possibilities of modulating the threshold voltage and current-voltage characteristics of the device

by charging and discharging the molecules for FLASH memory applications. The threshold voltage of an FET device is given by the following expression.

$$V_T = V_{FB} + \psi_{Si} \pm \frac{\sqrt{2qe_{Si}N_{A/D}|\psi_{Si}|}}{C_{ox}} - \frac{Q_{ex}}{C_{ab}} \quad (8)$$

Here, + is for n-FETs and – is for p-FETs; ψ_{Si} is the Si surface potential at inversion, which is positive for n-FETs and negative for p-FETs; V_{FB} is the flat-band voltage; C_{ox} is the capacitance between the gate and channel; Q_{ex} is the density of any external sheet charges between the gate and the channel; C_{ab} is the capacitance above the location of the sheet charges. For moleFETs, C_{ab} is C_{dl} ; C_{ox} is the series combination of SiO_2 capacitance and double layer capacitance; Q_{ex} is zero when the molecules are neutral and $+Q_m$ when the molecules are positively charged. Therefore, the change in threshold voltage, ΔV_T , with charging and discharging of molecules is –

$$\Delta V_T = -\frac{Q_m}{C_{dl}} \quad (9)$$

The threshold voltage is more negative when the molecules are oxidized than when they are neutral.

For n-FET devices, V_T with the molecules neutral is positive. However, the redox processes occur at negative gate voltages. Consequently, the charging and discharging of molecules occurred when the transistor was off. Therefore, it was not possible to characterize the modulation of V_T and current-voltage characteristics for n-moleFETs.

The threshold voltages of p-FET devices are negative. Therefore, it is possible to increase V_T (more negative) of a p-moleFET by charging the molecules. Monolayers of **Fc-P** were attached to varying thickness of SiO_2 on n-Si substrate and characterized using an electrolyte gate. Fig. 4.24 shows CyV characteristics of EMOS capacitors with **Fc-P** on 1.5 and 2.3 nm. Current peaks are observed indicating charging and discharging of molecules through the SiO_2 barrier on n-Si.

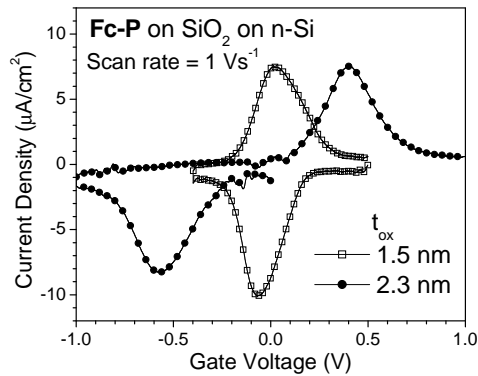


Figure 4.24 CyV characteristics of EMOS capacitors with **Fc-P** on 1.5 and 2.3 nm SiO_2 on n-Si.

Fig. 4.25 shows the I_d - V_{ds} characteristics of a p-moleFET with **Fc-P** on 2.8 nm SiO_2 at three different gate voltages. The gate voltages are negative and large enough to oxidize the molecules in

the channel region. Also, at $V_{ds} = 0$, the gate-to-drain voltage is large enough to oxidize the molecules on the gate-drain overlap region. With the molecules oxidized, the threshold voltage of this device was observed to be -1.8 V. Therefore, at $V_{gs} = -1.7$ V, the channel is not inverted and the transistor's sub-threshold current is observed in the I_d - V_{ds} characteristics. As V_{ds} increases (more negative), molecules in the overlap region will get reduced when $V_{gs} - V_{ds}$ becomes more positive than the reduction voltage. This is seen as a peak in the sub-threshold current. The molecules on the channel are unaffected because the channel is not inverted and is hence at a lower potential than the drain. Since molecules on the overlap region do not impact V_T of the device, the current levels remain the same after the peak. However, at V_{gs} greater (more negative) than the threshold voltage, the channel is inverted. As V_{ds} is increased with the channel inverted, not only do the molecules on the gate-drain overlap region get reduced, but so do some molecules on the channel near the drain end of the device. This results in a reduction in the threshold voltage causing the drain current to increase in the saturation region of the device. This increase in drain current can be observed in Fig. 4.25 at $V_{gs} = -1.8$ and -1.9 V.

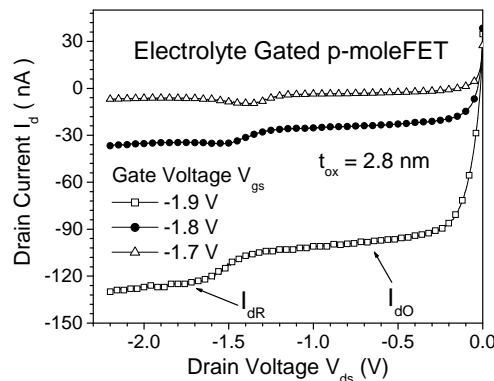


Figure 4.25 I_d - V_{ds} characteristics of a p-moleFET device with **Fc-P** on 2.8 nm SiO_2 . Molecules are oxidized at $V_{ds} = 0$ V. I_{dO} and I_{dR} refer to drain currents with molecules oxidized and reduced, respectively.

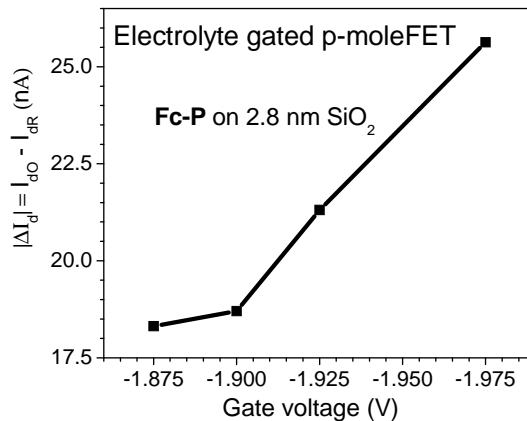


Figure 4.26 ΔI_d ($I_{dO} - I_{dR}$) versus V_{gs} from the I_{ds} - V_{ds} characteristics shown in Fig. 4.25, showing linear dependence.

The saturation current, I_{ds} , of an FET device is given by the following equation.

$$I_{ds} = k_p (V_{gs} - V_T)^2 \quad (10)$$

When the threshold voltage decreased by ΔV_T , the current equation changes to –

$$I_{ds} = k_p (V_{gs} - V_T + \Delta V_T)^2 \quad (11)$$

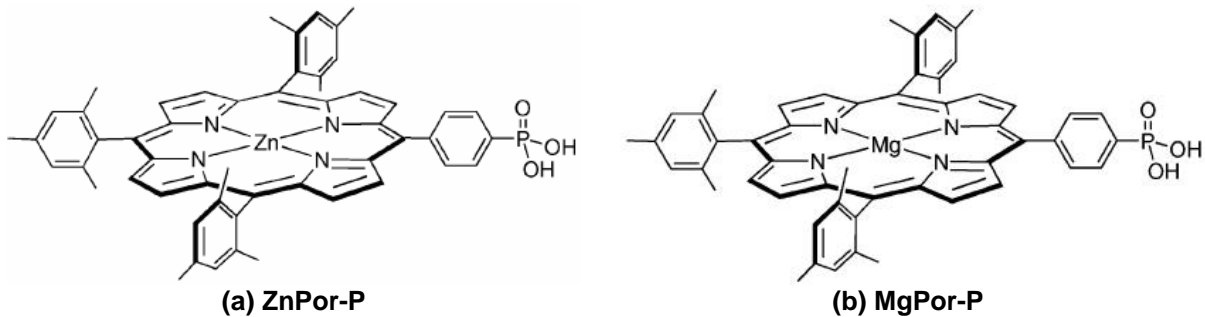
The difference in I_{ds} with the molecules charged and discharged is (11) – (10) and is given by

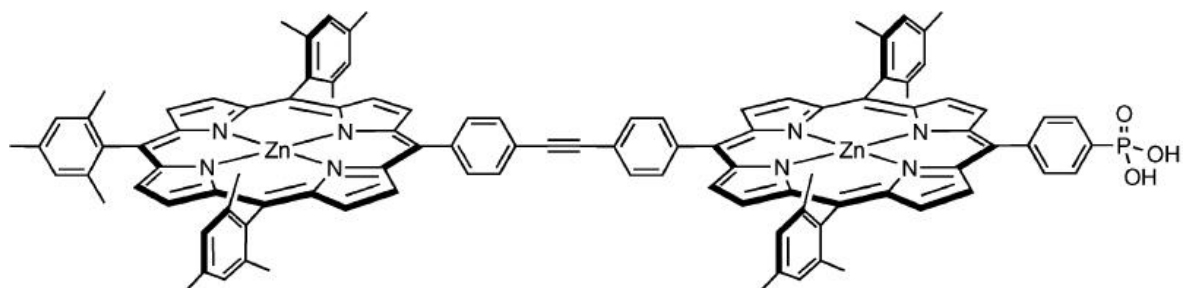
$$\Delta I_{ds} = k_p (2V_{gs} - 2V_T + \Delta V_T) \Delta V_T \quad (12)$$

From (12), it is clear that the difference in current has a linear dependence on V_{gs} for a constant ΔV_T . Fig. 4.26 is a plot of ΔI_{ds} versus V_{gs} from I_{ds} - V_{ds} characteristics of Fig. 4.25. As predicted by (12), ΔI_{ds} increases linearly with V_{gs} for V_{gs} greater than V_T .

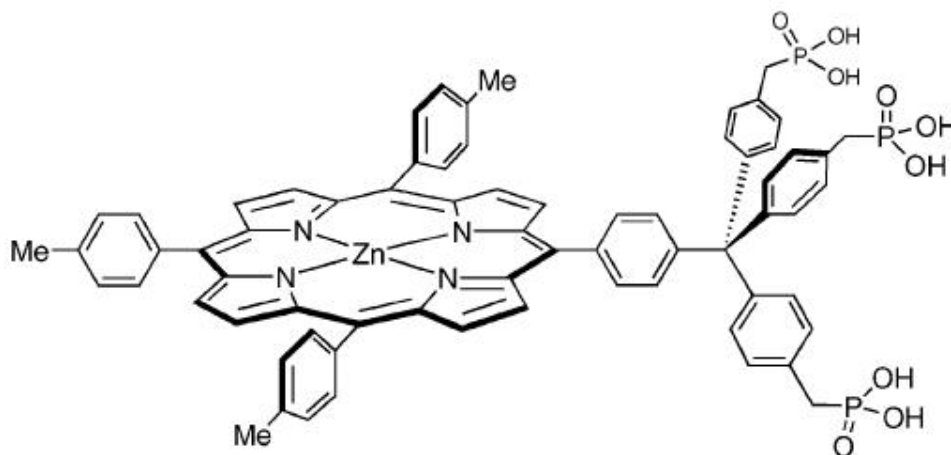
4.5 Porphyrin monolayers on SiO₂ on p-Si

Variety of metal containing porphyrin molecules functionalized with phosphonic acid linkers has been synthesized for attachment to SiO₂ surfaces [2, 3]. These molecules possess multiple number of stable redox states and, therefore, provide multiple bits in a single memory cell. Monolayers of these redox compounds have been formed on SiO₂ and the resulting EMOS capacitors have been characterized using CyV, CV and GV techniques. Fig. 4.27 shows the chemical structures of multi-state molecules employed in this study. **ZnPor-P** (or **Por-P**) is analogous to **Por-BzOH**, which is the zinc-containing porphyrin molecule used for attachment to Si (chapter 3). **MgPor-P** contains magnesium instead of zinc and is expected to have slightly higher redox potentials than **ZnPor-P**. **Tripod-P** has three phosphonic acid groups attached to one end of zinc-porphyrin. All three groups are expected to react with SiO₂ to form P-O-Si covalent bonds during attachment. Due to the presence of “three legs”, this porphyrin molecule is expected to form a physically stable monolayer with the individual molecules aligned vertically. However, the rate of electron transfer from these molecules might be slower due to the longer tether between the redox-active unit and SiO₂ [2]. **Dyad-P** has two zinc-porphyrin units coupled with one another. In a monolayer of this compound, the two porphyrins may be electrically inequivalent if there is a voltage drop across the long axis of the dyad. This electrical inequivalence could afford the possibility of doubling the number of accessible redox states [3].





(c) Dyad-P



(d) Tripod-P

Figure 4.27 Chemical structures of metal-porphyrins with phosphonic acid linkers for attachment to SiO_2 surfaces.

4.5.1 Attachment procedures

The attachment procedures for these porphyrin compounds, as outlined previously, involve placing solution of molecules on the samples in an inert environment at elevated temperatures. Dimethyl formamide (DMF) was used as the solvent for making the molecular solutions. Typically, the concentration of the solutions is approximately 1 mM. Temperatures in the range of 165 – 180 °C were found to produce the best electrical results. Maximum densities were obtained when 8 to 10 drops were employed, with 10 minutes between each drop. Samples with varying SiO_2 thickness were prepared by etching a 140 Å thick SiO_2 film to the desired thickness in a 1 % hydrogen fluoride (HF) solution. After the attachment procedure, the samples were rinsed in DMF in order to get rid of unattached molecules.

4.5.2 Electrical characterization

Fig. 4.28 shows typical CyV, CV and GV characteristics of EMOS capacitors with **ZnPor-P** attached to SiO_2 . The oxide thickness is 1.5 nm. Two distinct peaks, associated with the formation and neutralization of monocation and dication, are observed in current, capacitance and conductance. The maximum densities obtained in a monolayer were 3.5×10^{13} molecules/cm². Conductance peaks associated with depletion of Si can also be observed at positive gate voltages. **MgPor-P** was also found to form monolayers on SiO_2 with densities similar to that of **ZnPor-P**. CyV at

varying scan rates are shown in Fig. 4.29. The peak voltages for **MgPor-P** are slightly higher than those for **ZnPor-P**. Increased peak splitting is observed with increasing scan rates, similar to **Fc-P** monolayers on SiO_2 , indicating that the tunneling current through SiO_2 is rate limiting in the electron transfer processes.

Monolayers of **Dyad-P** and **Tripod-P** were also formed on SiO_2 surfaces. Representative CyV scans of EMOS capacitors with **Dyad-P** on SiO_2 are shown in Figs. 4.30 (a) and (b). As can be seen in Fig. 4.30 (a), three distinct peaks are observed indicating the presence of 4 distinct redox states. However, at higher scan rates [Fig. 4.30 (b)], the third peak disappears and only two peaks are observed. A plausible explanation is that the third peak is associated with slower electron transfer rates due to the longer distance from the SiO_2 surface. Higher scan rates, therefore, affect the slower rates of the third peak, but not the faster rates of the first two peaks. Fig. 4.31 shows CyV, CV and GV characteristics of an EMOS capacitor with **Tripod-P** on 1.5 nm SiO_2 . Two peaks indicate that these molecules form robust monolayers as well. The coverage obtained from the CyV peaks is approximately 2.25×10^{13} molecules/ cm^2 .

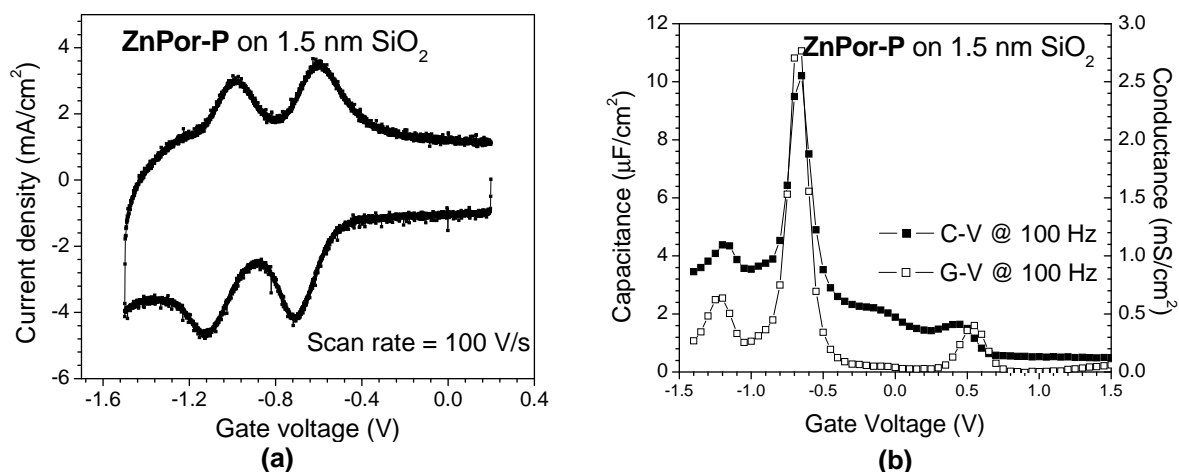


Figure 4.28 (a) CyV and **(b)** CV, GV characteristics of EMOS capacitor with **ZnPor-P** on 1.5 nm SiO_2

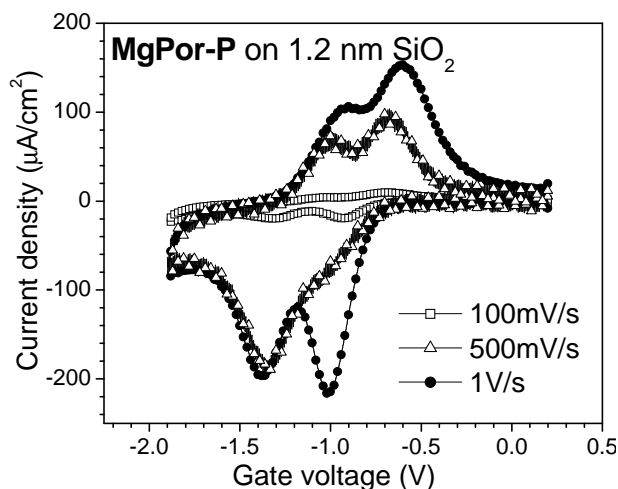


Figure 4.29 CyV characteristics of an EMOS capacitor with **MgPor-P** on 1.2 nm SiO_2 .

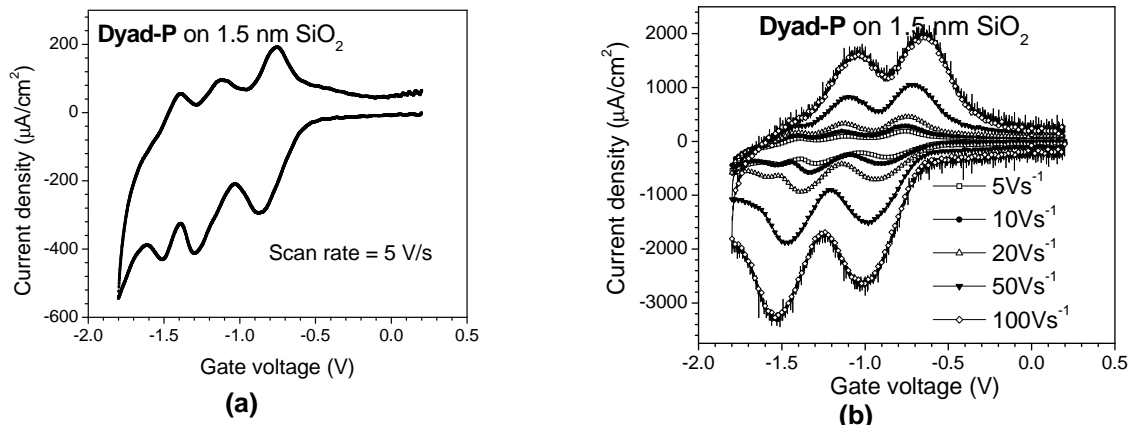


Figure 4.30 CyV characteristics of an EMOS capacitor with **Dyad-P** on 1.5 nm SiO₂ (a) at low scan rate of 5 V/s, showing 3 peaks and (b) at varying scan rates, showing disappearance of the 3rd peak at higher scan rates.

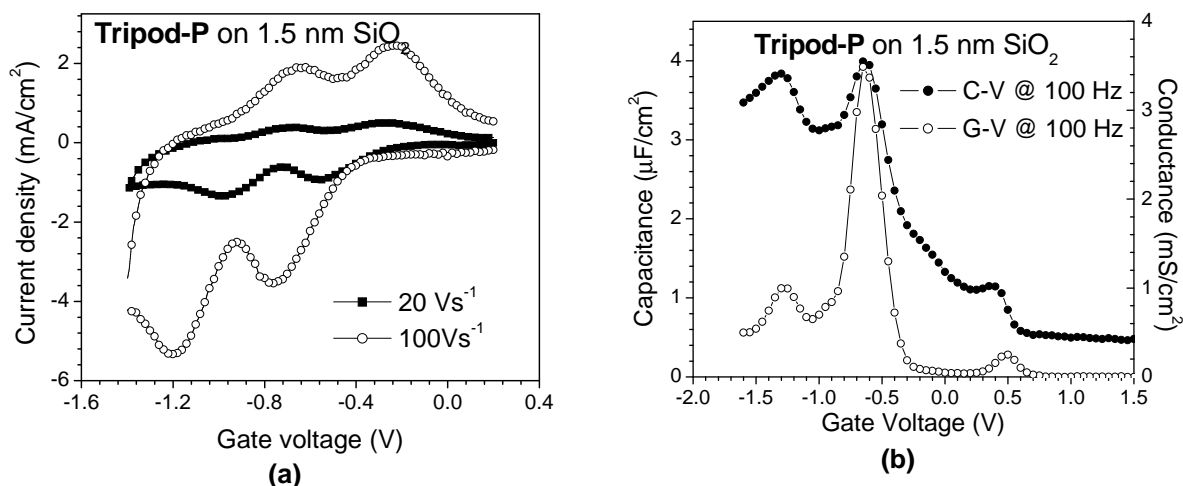


Figure 4.31 (a) CyV and (b) CV, GV characteristics of an EMOS capacitor with **Tripod-P** on 1.5 nm SiO₂.

4.6 Porphyrin polymers on SiO₂ on p-Si

In order to achieve higher densities of porphyrins on SiO₂, polymer films were formed using **Por-m**, whose chemical structure is shown in Fig. 4.32 (a). The technique used to create these monolayers on SiO₂ involves the formation of a covalently bonded monolayer of porphyrins on SiO₂ first and subsequent polymerization. The monolayer was formed using a 1 mM solution of **Por-Pm**, which has a phosphonic acid functional group at one end for attachment to SiO₂ surfaces, and an ethylene functional group at the other end for polymerization [see Fig. 4.32 (b)]. The solvent used was DMF. The attachment was carried out at 200 °C by placing the solution on the samples for 4 minutes. Immediately after this, a 1 mM solution of **Por-m** in DMF was placed on the samples and the temperature was raised to 400 °C. This facilitates the polymerization of the molecule and results in the formation of a polymer film, which is covalently bonded to the underlying SiO₂ via the phosphonate linker of **Por-Pm**.

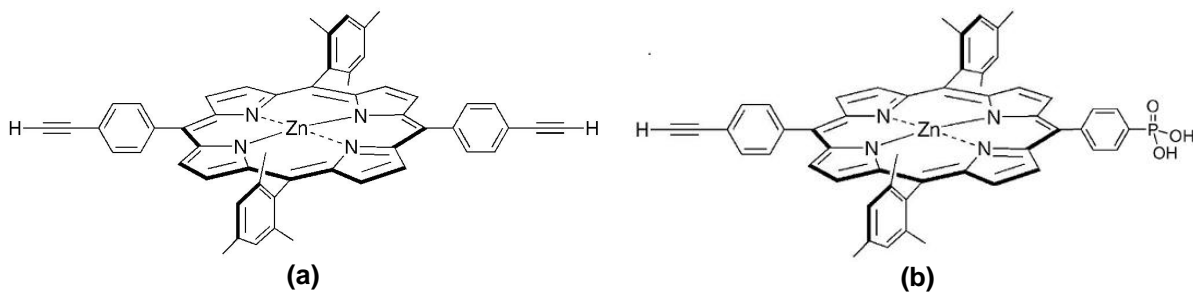


Figure 4.32 Chemical structures of (a) Por-m and (b) Por-Pm molecules.

Fig. 4.33 shows the CyV characteristics of EMOS capacitors with porphyrin polymers on SiO₂ at 100 and 500 mV/s. The maximum densities obtained from the CyV peaks are approximately 10¹⁶ molecules/cm². The densities are higher than that from **Por-m** directly on Si. However, the separation between oxidation and reduction peaks is much higher even at low scan rates. The peak separation is even larger than that for monolayer of porphyrin on SiO₂, for the same t_{ox} . This clearly indicates that the electron transfer rates for polymer porphyrins are slower than that for monolayer porphyrins.

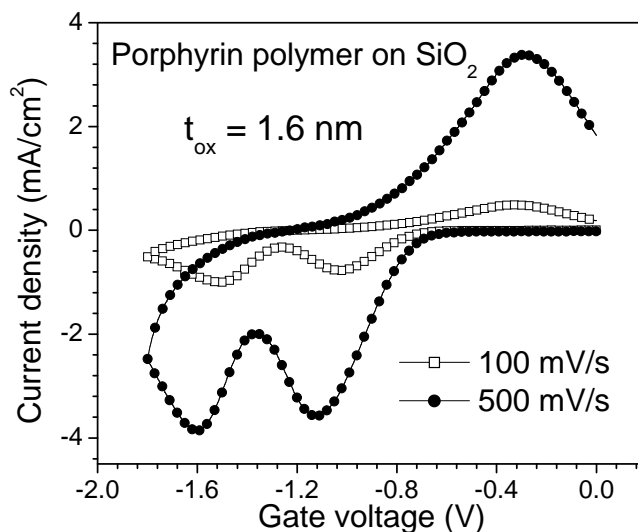


Figure 4.33 CyV characteristics of an EMOS capacitor with porphyrin polymer on 1.6 nm SiO₂.

4.7 Stability of molecules on SiO₂

The stabilities of monolayers of ferrocenes and porphyrins on SiO₂ under electrical stressing were studied. Electrical measurements were performed in ambient conditions as well as in inert environments to study the effect of moisture and oxygen on stability.

Fc-P monolayers on SiO₂ showed negligible degradation in density after electrical characterization in an inert environment over 3 hours. CyV at very low scan rates and impedance spectroscopy at different frequencies – measurements that usually result in rapid degradation in ambient conditions – resulted in no degradation in molecular densities in the monolayer, as shown in Fig. 4.34. Furthermore, samples remained stable and exhibited same high densities even after two days, so long as they stay in a controlled nitrogen purged environment. However, repeated application of large positive voltages resulted in increased splitting between oxidation and reduction

peaks [see Fig. 4.35]. Nevertheless, the molecular coverage, obtained from the area under CyV peaks, remained the same. One plausible reason for this increased peak splitting could be an increase in the SiO₂ thickness due to electrochemical growth of oxide at high voltages.

Porphyrim monolayers on SiO₂ exhibited very poor stabilities compared to the ferrocenes, even if characterized in inert conditions. Fig. 4.36 shows CyV characteristics of an EMOS capacitor with a monolayer of **ZnPor-P** on 1.5 nm SiO₂. The molecular densities degraded by as much as 90% within the first 100 CyV scans even at scan rates of 1 V/s. CV and GV measurements made the degradation more rapid. CV and GV peaks usually disappeared after the first 5 scans, if not earlier. A possible reason for this faster degradation of porphyrin monolayers on SiO₂ compared to their ferrocene counterparts could be due to the difference in temperature during attachment. The temperatures for ferrocene and porphyrin attachments are approximately 80 and 170 °C, respectively. It is possible that the phosphonic acid linkers are susceptible to higher temperatures and become less stable when exposed to temperatures of 170 °C.

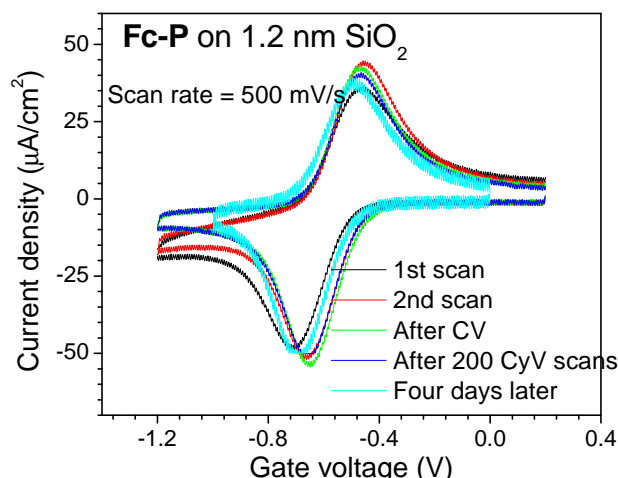


Figure 4.34 CyV characteristics of an EMOS capacitor with **Fc-P** on 1.2 nm SiO₂ over a period of 4 days. Negligible degradation was observed after many CV, GV and CyV measurements. Sample was characterized in an inert environment.

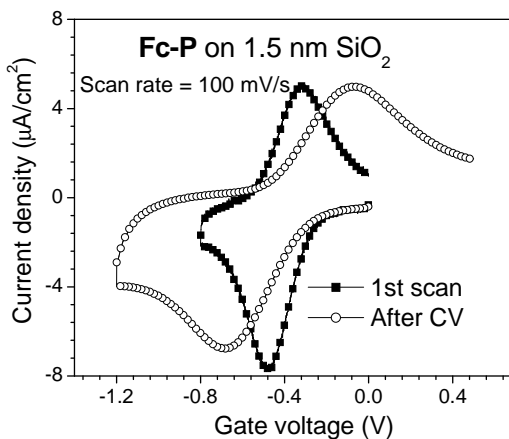


Figure 4.35 CyV characteristics of an EMOS capacitor with **Fc-P** on 1.5 nm SiO₂, showing increasing peak separation after many CV and CyV scans.

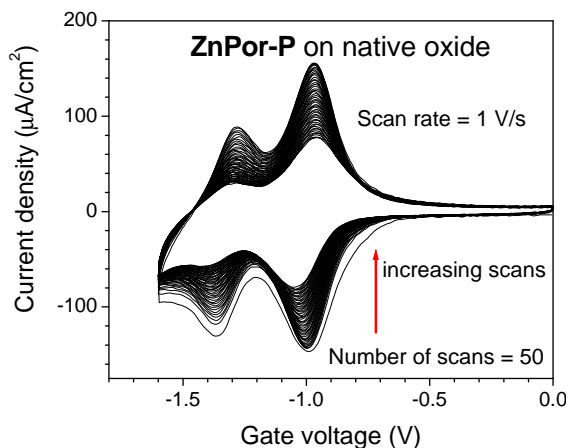


Figure 4.36 CyV characteristics of an EMOS capacitor with **ZnPor-P** on native SiO₂. 50 scans at 1 V/s results in a 90% degradation.

One way to overcome this stability problem with porphyrins would be to employ polymer films of **Por-m** without an underlying monolayer. Since **Por-m** does not have any functional groups for attachment to SiO₂ surfaces, the resulting film might not exhibit degradation due to instability of any covalent bonds between molecules and the surface. The **Por-m** molecules indeed form a strongly adsorbed polymer film on SiO₂ surfaces. However, the absence of covalent bonds would mean that the contact between molecules and the underlying surface is physical in nature. Consequently, achieving the same repeatable electrical behavior from sample to sample and from attachment to attachment might become a considerable challenge. Also, the polymers exhibit slower electron transfer rates than the monolayers. However, since the tunneling current through SiO₂ is rate limiting for molecules on SiO₂, the inherent speed of the polymers may no longer be an issue.

4.8 Summary and Conclusions

Monolayers of ferrocenes have been attached to SiO₂ surfaces and their write, erase and charge storage properties have been tuned by varying the oxide thickness. The physics of these hybrid devices and the mechanisms of charge transport have been studied. Ferrocene monolayers have also been incorporated in FET structures to create moleFETs. The threshold voltage and current-voltage characteristics of p-moleFETs were modulated by charging and discharging of molecules in the channel region. This work has demonstrated the ability to modulate transistor characteristics via charge storage in redox-active molecules employed within the transistor.

It was not possible to modulate the characteristics of n-moleFETs because the redox processes were taking place at negative gate voltages, whereas the transistors operation was in positive gate voltages. However, it might be possible to overcome this difficulty by employing molecules on a thicker gate SiO₂. As observed in this study, the discharging voltages become more positive as t_{ox} increases. The threshold voltage of the device decreases when the molecules are positively charged. Therefore, by increasing t_{ox} , the “written V_T ” could be made less positive than the discharging voltages. This would result in the presence of a voltage range where the device

characteristics would be different with the molecules charged and discharged. In any case, to achieve non-volatility for FLASH applications, thicker SiO₂ layers have to be employed for both n-moleFETs and p-moleFETs.

Ferrocene-based devices have been important tools for demonstration of concept and understanding of device mechanisms. However, since these molecules are not stable beyond 200 °C. Therefore, for real-world applications, molecules that are stable at high temperatures need to be explored. Porphyrins have proven to be stable up to 450 °C. A variety of porphyrin molecules have been employed on SiO₂ surfaces as monolayers as well as polymers. These devices exhibited multiple state behaviors. However, the porphyrin monolayers were found to be unstable and degraded much quicker than the ferrocene monolayer, which were stable for long durations of electrical measurements. A possible reason for this could be the exposure of the phosphonate linkers to temperatures greater than 170 °C during the attachment of porphyrins. Further investigations are necessary to understand the exact mechanisms responsible for degradation. Incorporation of high density porphyrin polymers on SiO₂ without any covalent bonding between the molecules and SiO₂ need to be explored for multiple bit FLASH applications.

4.9 References

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5. TOWARDS SOLID-STATE: ROLE OF ELECTROLYTE AND ITS REPLACEMENT

5.1 Introduction

So far, all the discussions about hybrid Si-molecular devices have involved the use of a liquid electrolyte as gate contact. Although this is a very useful tool in characterization that circumvents the problem of making efficient contacts to the molecules, it may not be ideal for real-world applications. Particularly, if this technology were to be integrated with existing CMOS technology for DRAM and/or FLASH memory applications, it is imperative to have a solid-state approach. Some of the advantages of a solid-state approach are –

1. Ease of integration and feasibility of large scale manufacturing
2. Lower resistance and faster operation compared to liquid electrolyte gate
3. Potential “all-electronic” operation, unlike with the electrolyte where conduction is ionic

However, achieving a complete solid-state molecular device has a lot of challenges: (a) Since the molecular film is typically just a monolayer to few layers thick, deposition of materials on top of the molecules without affecting the molecular layer is the biggest challenge; (b) The solid-state gate material has to replicate the role played by the electrolyte in charging and discharging the molecular layer.

This chapter analyzes the role played by the electrolyte and the electrolytic double layer in hybrid silicon-molecular devices before proposing a solid-state approach to replace the liquid electrolyte. One such approach utilizing a combination of aluminum and aluminum nitride is presented and characterization results of solid-state molecular devices with both redox and non-redox compounds are discussed. Finally, the potential drawbacks involved in a solid-state approach for this technology are examined.

5.2 Role of Electrolyte

Most approaches to molecular electronics involve metal-molecule-metal sandwich structures that utilize conductivity changes of molecules under applied voltages for memory and logic applications [1-3]. Unlike these approaches, the hybrid silicon-molecular technology discussed here utilizes charge storage properties of redox-active molecules for memory applications [4-8]. The electrolyte gate, employed to characterize devices in this technology, is not only used as a conducting medium, but is also involved in the molecular charging/discharging processes by forming an electrolytic double layer capacitor at the interface between electrolyte and molecules. Structures with metal directly on molecules may not be able to store charges due to the absence of any barrier

between the metal and the molecules. Therefore, the electrolyte plays a very critical role in these hybrid silicon-molecular charge storage devices.

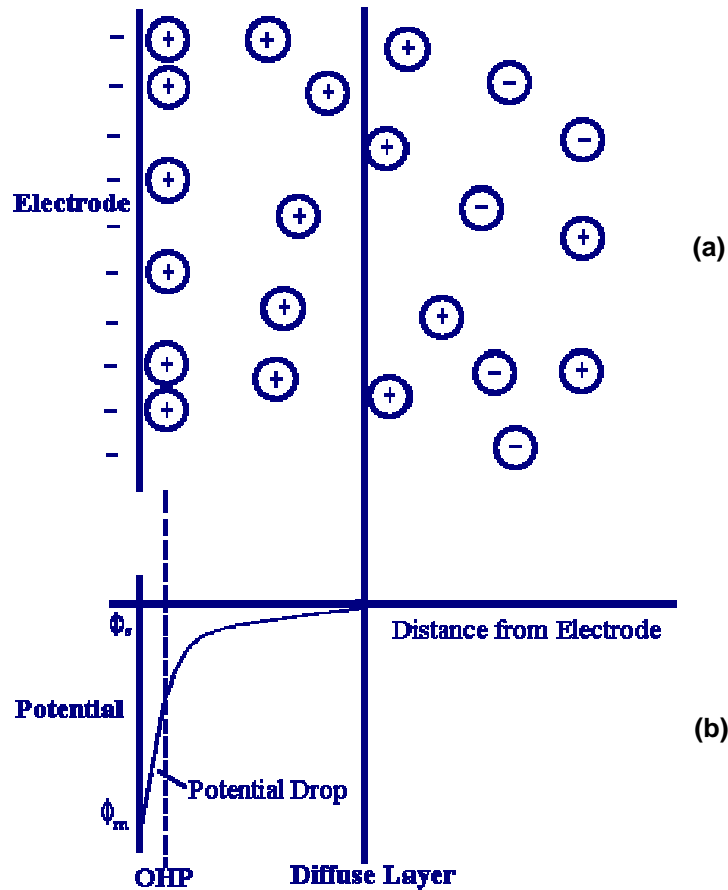


Figure 5.1 (a) Schematic structure and (b) potential distribution of a double layer created at the interface between electrolyte and an electrode

5.2.1 The electrolytic double layer

When an electrolyte is in contact with a solid, redistribution of ions in the electrolyte occurs at the electrolyte-solid interface due to charges at the surface of the solid. For instance, suppose that the solid is a metal with an excess of electrons at the surface. When electrolyte is in contact with this metal, positive ions in the electrolyte will get attracted to the surface and negative ions will get repelled, due to the presence of negatively charged electrons at the metal surface. The attracted ions form a layer of positive ions at the electrolyte-solid interface. The distance of approach is limited to the radius of the ion and a single sphere of solvation around each ion (solvent molecules surrounding the ion). As a result, a sheet of positively charged ions, separated from the metal surface by a distance equal to the size of the ions and solvent molecules, is formed. Away from this sheet of positive ions, there will be a gradual decrease in the concentration of positive ions and an increase in the concentration of negative ions until the concentrations become equal in the bulk electrolyte. The sheet of positive ions is called the Outer Helmholtz Plane (OHP) and the region adjacent to it is called the diffuse layer. Together, they constitute the “double layer”. Fig. 5.1 (a) shows the schematic

representation of the double layer structure, showing the OHP and the diffuse layer when there is an excess of electrons at the solid surface [9, 10]. The same argument holds good for positive charges at the solid surface as well, with the role played by positive and negative ions in the electrolyte interchanged.

The distance between OHP and the interface has only the solvent molecules and, therefore, no free charges or ions. The diffuse layer also consists of these ions-free solvent molecules in between the positive and negative ions. Due to the presence of the solvent, the double layer is capacitive in nature. The OHP is analogous to a parallel plate electrical capacitor, whereas the diffuse layer is similar to the depletion region in semiconductors. Fig. 5.1 (b) shows the potential drop within the electrolyte. There exists a potential drop between the solid surface and the electrolyte that occurs only within the double layer. This double layer is modeled in terms of capacitive elements in the field of electrochemistry.

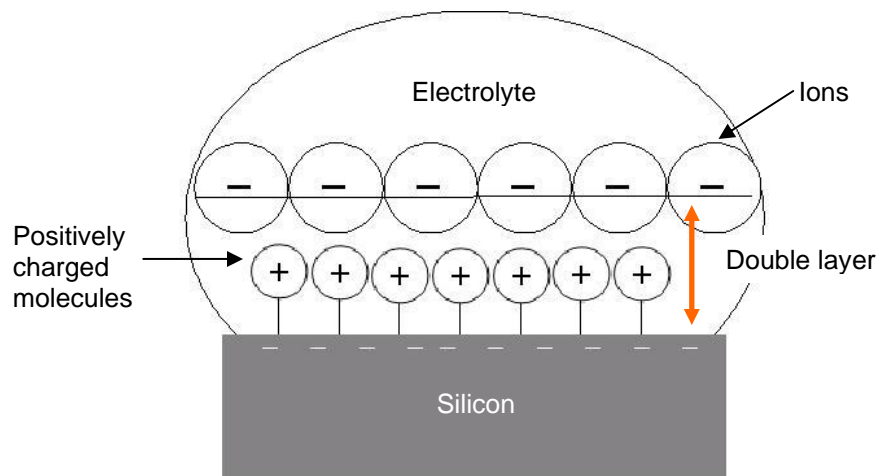


Figure 5.2 Schematic of an EMS capacitor showing positive charges in the molecular layer and ions in the electrolyte across the double layer screening those charges

5.2.2 Electrolyte in EMS/EMOS capacitors

The electrolyte in EMS and EMOS capacitors plays a dual role.

1. Formation of a double layer around the molecules at the interface between the electrolyte and the molecular layer:

Fig. 5.2 shows the schematic of an EMS capacitor depicting the charge distribution in the device when the molecular layer is oxidized (charged positive). As the gate voltage is increased in the negative direction, the molecular energy levels are raised causing the molecules to lose electrons to the Si substrate (write process) leaving behind positively charged molecules. These positive charges will be balanced by negatively charged ions in the electrolyte, electrons at the silicon surface and negatively charged ionized impurity atoms at the silicon surface, if it is p-doped. Negatively charged ions in the electrolyte will get attracted to the positively charged molecular layer and will result in the formation of a double layer, as discussed in the previous section (Note: A double layer will exist even

when the molecules are in the neutral state due to charges at the silicon surface). Since the molecules are completely surrounded by electrolyte, the double layer can potentially shield individual molecules from one another. In effect, the double layer is in parallel to the molecules.

The proportion of molecular charges balanced by the electrolyte and the Si surface will depend on the relative capacitances of the double layer (C_{dl}) and the combination of linker/SiO₂ (C_{ox}) underneath the molecules. If C_{dl} ($= e_{dl}/t_{dl}$) is greater than C_{ox} ($= e_{ox}/t_{ox}$), then more molecular charges will be balanced by ions in the electrolyte than charges/electrons at the Si surface and vice versa. The dielectric constant of the double layer, which depends on the solvent used in the electrolyte, is usually very high. For instance, ϵ_{dl} for propylene carbonate (PC), which is the solvent used in this study, is 60. The double layer thickness (t_{dl}) depends on the ionic concentration in the electrolyte. For a concentration of 0.1 M, t_{dl} is less than 100 Å, and can be as thin as 10 Å for a 1 M electrolyte solution [10]. Consequently, C_{dl} is at least 5 $\mu\text{F}/\text{cm}^2$ or greater. On the other hand, the dielectric constant of the organic molecule (linker) is approximately 2.5 and that of SiO₂ is 3.9, resulting in a C_{ox} of at most 1 $\mu\text{F}/\text{cm}^2$. Consequently, since C_{dl} is greater than C_{ox} , most of the molecular charges will be balanced by ions in the electrolyte rather than ionized impurity atoms or electrons at the Si surface.

The higher capacitance of the double layer also enables most of the molecules to get written within a small voltage range. As the oxidation process begins, molecules lose their electrons and become positively charged. These charges will mostly be balanced by negative ions in the electrolyte, thereby ensuring that the electric field across the linker/SiO₂ combination does not decrease. Had the positive charges been balanced by charges at the Si surface, then the electric field across the linker/SiO₂ would have decreased. Consequently, further oxidation of molecules would have required a larger negative gate voltage. However, since the double layer effectively screens the charged molecules, charge densities as high as 10^{14} cm^{-2} for the monolayer and 10^{15} cm^{-2} for the polymer have been achieved.

The double layer also has a significant impact on the charge retention properties of these devices. Once the device is written, i.e., the molecules have been positively charged, the electric field across the linker/SiO₂ combination is low because most of the charges are screened by ions across the double layer. This results in longer retention times that are useful in DRAM applications. Memory cells would have to be refreshed at smaller frequencies, thereby decreasing the power consumption. However, for non-volatile memory applications like FLASH, the longer retention time achieved by double layer charge screening is not advantageous. The principle behind FLASH memory device is that the positive charges in the molecular layer changes the conductivity of the Si channel. For this purpose, most of the charges need to be screened by opposite charges at the Si surface. Also, the change in threshold voltage, ΔV_T , depends on the capacitance between the gate and the location of positive charges. In this case, this capacitance is equal to the double layer capacitance, C_{dl} . ΔV_T is

given by $\left(\Delta V_T = -\frac{Q_m}{C_{dl}} \right)$. Therefore, a small C_{dl} is required to effect a large change in V_T for a given density of charges.

The double layer also efficiently blocks any DC leakage current, thereby limiting the leakage currents in the device. Since the conduction within electrolyte is ionic, there are no leakage currents due to tunneling of electrons or holes from Si to electrolyte across the double layer. The only DC currents that are measured in the device are that related to the transient charging of the double layer

capacitance, given by $I = \frac{dQ_{dl}}{dt}$. The low leakage currents across the double layer have enabled field effect transistors with just a native oxide to turn on by using an electrolyte gate [7].

2. Conducting medium between the substrate and the gate

The second role played by the electrolyte is that of a conducting medium between the substrate and the gate. Bulk electrolyte is an ionic conductor, enabling conduction through the movement of ions. Ions, due to their bigger sizes, are slower to respond to an electric field compared to electrons and holes. Hence, the conductivities of electrolytes are lower than that of metals. However, this lower conductivity enables impedance measurements at low frequencies. Nevertheless, if this technology were to compete with conventional solid-state memory technologies, then the speed of the device has to be comparable, if not faster than that of existing technologies. Therefore, a faster conducting medium would be necessary.

5.3 Solid-State Approaches

5.3.1 Metal on molecules

The most common approach in this field to date has been the metal-molecule-metal approach [1-3]. The molecules that are sandwiched between 2 metal layers change their conductivities at applied voltage biases, which are then used for memory and logic applications. The molecules may be covalently bonded to the substrate underneath. However, the top metal layers are deposited on top of the molecules and typically do not form covalent bonds. Covalent bonds are necessary to form repeatable good contacts from device to device and from deposition to deposition. In the absence of covalent bonds, the interface between metal and molecules becomes unknown and might lead to unacceptable variations from device to device, especially since the molecular film is just a monolayer to a few layers in thickness. Nevertheless, reversible switching in devices with metal on molecules have been observed and attributed to structural changes and/or metastable states of the molecules. However, the yield of these devices has been fairly low, sometimes less than 20-30% [11]. Recent reports also indicate that some of the switching behaviors are molecule-independent and can be

hugely dependent on the top metal electrode [12, 13]. Consequently, the knowledge base of these devices needs further work [14].

Previous efforts to create metal-molecule-silicon hybrid devices employing redox-active molecules for memory applications via charge storage in the molecules resulted in molecule-independent behavior [15]. Metal deposited directly on monolayers resulted in a Schottky diode type behavior due to shorts formed between metal and underlying Si substrate. Metal deposited on multilayer films of **Fc-P** [chemical structure shown in Fig. 5.3 (a)] on Si substrates resulted in a reversible non-volatile switching behavior. However, similar behavior was also observed for multilayers of non-redox active **BiP-P**, whose chemical structure is shown in Fig. 5.3 (b). Multilayers are formed when molecular attachment is carried out at temperatures greater than 175 °C using more number of drops and longer periods of time than those used for forming monolayers. Although the mechanisms responsible for the creation of multilayers are unclear, electrical characterization has revealed that more than a monolayer of redox-active molecules is deposited on the Si surface [15]. It is believed that the reversible switching behavior exhibited by metal-multilayer-silicon devices are due to formation and destruction of metal filaments through the multilayer film, connecting the top metal layer and the Si substrate. Details about multilayer characteristics and metal-multilayer-silicon structures can be found in [15].

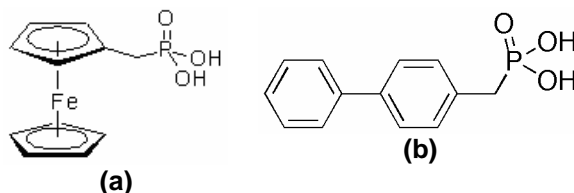


Figure 5.3 Chemical structures of (a) redox-active **Fc-P** and (b) non-redox active **BiP-P**

Although it might be possible to deposit metal layers on top of monolayers or multilayers of molecules without creating shorts or destroying the molecular films, metal-molecule-substrate structures are not viable for charge storage devices. Due to the absence of any barrier between the top metal layer and the molecules, any molecular energy level losing an electron to silicon will be immediately filled by an electron from the metal, resulting in a resonant tunneling behavior. Molecular resonant tunneling devices might have applications in logic devices; however, for the purposes of this study, metal directly on molecules may not be useful for memory applications.

5.3.2 Metal-insulator on molecules

In EMS and EMOS capacitors, as discussed previously, a double layer capacitor is formed around the molecules at the interface between the electrolyte and the molecular layer. The resulting structure is a stack of conducting electrolyte and insulating double layer on top of the molecules, which are either on SiO₂ or directly on Si. Fig. 5.4 (a) shows the schematic of such a structure. However, this schematic is only an approximate representation of the actual structure, where the double layer is in parallel with the molecules, especially for a monolayer. The conducting electrolyte

and the double layer can be replaced by a metal and a dielectric, respectively, to create a complete solid-state hybrid silicon-molecular memory device. In this solid state device, the dielectric plays the role played by the double layer in the electrolytic capacitors. Fig. 5.4 (b) shows the schematic of this solid state structure. The dielectric used in this figure is aluminum nitride (AlN), which is the material used in this study. Properties of AlN and devices made using AlN will be discussed later in this chapter.

Fig. 5.4 also depicts the differences between the two structures – electrolytic and solid-state capacitors. The positive charges in the molecules are screened by electrons in the metal across the dielectric in the solid-state device. On the other hand, it's the negatively charged ions in the electrolyte which screens the charges in the electrolytic capacitor. The other difference between the two structures is the type of conduction in the conducting medium between the gate and the substrate – ionic in the electrolyte; electronic in the metal.

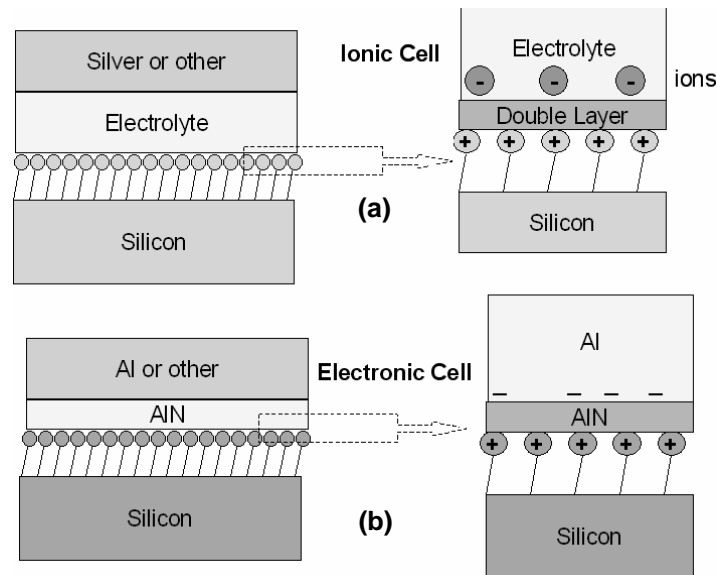


Figure 5.4 Structure of (a) electrolytic capacitor and (b) solid-state capacitor depicting the primary differences between the two. The electrolytic capacitor forms an ionic cell whereas the solid-state capacitor forms an electronic cell.

The salient advantages of this solid-state approach are: (a) the all electronic conduction, which increases the maximum operating speed of the device; and (b) the presence of insulating barriers both above and below the molecules, which enables charging of the molecules and storage of charges. However, there are many considerations that need to be taken into account in the choice of the dielectric material and thickness.

Firstly, the dielectric constant and thickness of the insulating material need to be chosen according to the application. DRAM applications require the capacitance of the dielectric to be as high as possible. A high capacitance of the layer above the molecules (C_{ab}) will ensure that most of the positive charges are screened by electrons in the metal above the dielectric, thereby enabling the maximum number of molecules to be charged within a small voltage range. This requires a very thin

high-k (high dielectric constant) material. The electrolytic double layer is an ideal match for these requirements! For FLASH applications, however, C_{ab} needs to be low in order to achieve the maximum ΔV_T for a given density of charges. Also, the dielectric layer has to be thick enough to ensure that electrons do not tunnel across the insulating barrier from the metal to neutralize positively charged molecules. This is a critical requirement to achieve non-volatility. Therefore, DRAM and FLASH applications have contrasting requirements for the choice of dielectric material above the molecules.

Secondly, C_{ab} also impacts the voltage distribution in the capacitor. Suppose that the capacitance of the linker/SiO₂ combination is C_{ox} ($= e_{ox}/t_{ox}$). The voltage at which the molecules are charged depends on the voltage drop across this combination, as discussed in the previous chapter. This voltage drop varies with the applied gate voltage as:

$$V_{ox} = \frac{C_{ab}}{C_{ab} + C_{ox}} V_G$$

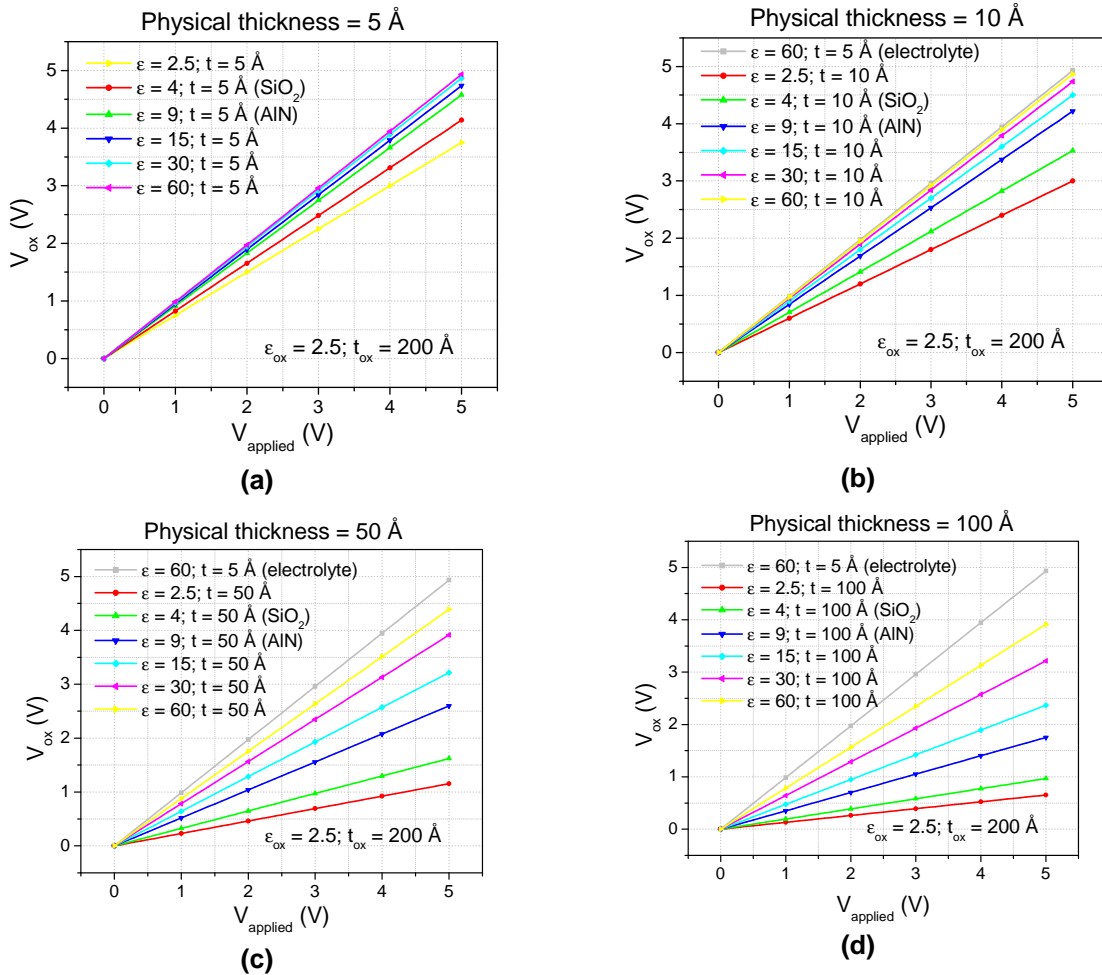


Figure 5.5 V_{ox} versus applied gate voltage for varying thickness and dielectric constant of the dielectric layer on top of the molecules. Comparisons made with the electrolyte double layer.

This expression ignores any capacitance of the Si substrate. It is essential to maximize V_{ox} in order to keep the oxidizing gate voltage as low as possible. According to this expression, in order to maximize V_{ox} for a given V_G , $\frac{C_{ox}}{C_{ab}}$ has to be much less than 1. Fig. 5.5 shows the variation of V_{ox} versus V_G for various combinations of ϵ_{ab} and t_{ab} , the dielectric constant and thickness, respectively, of the insulating material above the molecules. In these curves, ϵ_{ox} and t_{ox} are assumed to be 2.5 and 1.5 nm, respectively. Although the dielectric constant of SiO_2 is 3.9, ϵ_{ox} is taken as 2.5 in order to accommodate for the linker, which has a low dielectric constant. The plots in Fig. 5.5 compares V_{ox} for ϵ_{ab} varying from 3.9 (SiO_2) and 60 (double layer) and t_{ab} varying from 5 Å (double layer) to 100 Å. Clearly, it is very difficult to match the double layer's V_{ox} vs. V_G using a solid-state dielectric. Nevertheless, a very thin high-k dielectric material is required in order to maximize V_{ox} so as not to increase the write (oxidizing) voltages. This requirement is especially important for DRAM applications and become irrelevant for FLASH applications, where the oxidizing voltages are already large due to the thick SiO_2 layer underneath the molecules required for longer retention times.

High densities of charges ($\sim 10^{14} \text{ cm}^{-2}$) have been achieved in a monolayer of molecules in EMS and EMOS capacitors. Such high densities are made possible by the effective screening of charges by the double layer. Since the electrolyte surrounds the molecules completely, individual molecules, and hence charges, maybe electrostatically isolated from one another, thereby enabling high densities of sheet charges. In the solid-state system discussed above, the dielectric is on top of the molecules. As a result, it may not be possible to achieve similar densities of charges in the molecular monolayer. Nevertheless, in order to effectively screen charges, a very high-k material is required. The proportion of molecular charges screened by the dielectric above the molecules increases with increasing dielectric constant of the material.

From the above discussions, it is clear that a very thin high-k dielectric material is desirable to replicate the functions of the electrolytic double layer. However, such a material has still not been employed in the CMOS industry, which has been investigating on high-k dielectric materials for more than a decade now. Lastly, the deposition process of the dielectric material should not destroy the molecules and their charge storing redox properties.

5.3.3 Solid Electrolytes

Another solid-state approach to hybrid silicon-molecular memories is to use solid electrolytes [15]. There have been many research activities in developing solid polymer electrolytes and enhancing their conductivities [16-18]. These materials, while providing a solid-state device, would also lead to the formation of an electrolytic double layer that will satisfy most of the requirements of the dielectric material on top of the molecules. However, the conduction in the system would still be ionic, which would make the maximum operating speed of the device slower. Processing feasibility

and temperature stability are two other concerns with regards to solid electrolytes and solid polymer electrolytes.

5.4 Aluminum/aluminum nitride as replacement for electrolyte/double layer

In an effort to replicate the role played by electrolyte and the double layer in the operation of hybrid silicon-molecular memory devices, a stack of aluminum nitride (AlN) and aluminum (Al) was deposited on top of molecular layers. This section discusses the reasons behind choosing these materials, fabrication of solid-state molecular devices, and the physical and electrical characterization of these devices. Electrical measurements and Infrared spectroscopy reveal that molecular layers survive the deposition of AlN and retain their redox properties.

5.4.1 Choice of materials

The primary reason for choosing AlN as the dielectric material on top of molecules is the ease of fabrication of AlN layers at the NCSU cleanroom. It is the easiest high-k dielectric material that can be deposited with the tools available in the fabrication facilities. Table 5.1 lists the properties of AlN and their advantages when incorporated in devices with redox-active molecules used in this study. AlN is a high bandgap semiconductor with a bandgap of 6 eV [19]. In its undoped state, it behaves like an insulator with a high dielectric constant of 8.5 to 9 [20]. Deposition of AlN does not involve any oxygen, which may be critical for use with the redox-active molecules used in this study, which are susceptible to oxygen and moisture. Even though the dielectric constant of AlN is approximately 9, it would still require a very thin layer in order to effectively replicate the role played by double layer, as shown in Fig. 5.5. However, due to the other advantages that AlN offers, it was used to study the behavior of solid-state molecular devices. The knowledge base developed for AlN can always be transformed to other higher-k dielectric materials in order to meet all the requirements discussed in previous sections.

Table 5.1 Properties of AlN and their advantages when used with molecules

Property	Advantages
High bandgap (> 6 eV)	Insulator in its undoped state, potential dielectric for SiC devices
No oxygen involved	Critical to preserve molecules
Wide bandgap	Low leakage currents
High dielectric constant (8.5 – 9)	Minimizes voltage drop
Oxygen diffusion barrier	Increases stability of molecules

5.4.2 Fabrication process

Table 5.2 outlines the steps involved in the fabrication of solid-state hybrid molecular devices. The molecules used for these purposes are the redox-active **Por-m** and the non-redox active **BiP-m**. Both these molecules, whose chemical structures are shown in Fig. 5.6, have two acetylene

functional groups, and are capable of forming polymer films at elevated temperatures. The attachment procedures for the formation of polymer films are as mentioned in chapter 2. The molecule solutions were typically 0.1 to 1 mM of the compounds in tetrahydrofuran. The attachment temperatures were 400 °C for **Por-m**, and 250 °C and 400 °C for **BiP-m**. The attachment time was 2 minutes at 400 °C and 4 minutes at 250 °C. Redox-active polymer films were employed for this study so that the molecular layers close to the Si surface can be prevented from being affected by the AlN deposition procedure. Non-redox active polymer films were used as controls. Aluminum nitride was deposited using reactive sputtering of Al in N₂. A 150 nm thick Al layer was deposited as the gate electrode using a resistive-heated evaporator. The resulting structures were metal-AlN-Si (MIS) and metal-AlN-molecule-Si (MIMS) capacitors. Electrical characterization was performed using CHI 600 electrochemical analyzer, HP 4284A LCR meter and HP 4155B semiconductor parameter analyzer. For CyV measurements, a 1 M solution of tetrabutyl ammonium hexafluorophosphate in propylene carbonate was used as the electrolyte and silver wire was used as the gate electrode.

Table 5.2 Steps involved in fabricating Al/AlN/polymer/SiO₂/Si capacitors. * indicates optional steps

Step #	Fabrication process
1	Grow thin sacrificial oxide on (100) n- or p- Si substrates
2a*	Etch back the thin oxide using 1% HF solution to desired thickness
2	Etch sacrificial oxide using 1% HF solution
3	Expose to ambient to grow thin native SiO ₂
4*	Attachment of molecules (a) Place molecule solution on sample in Ar ambient (b) Place sample at elevated temperature for 2-4 min (c) Allow sample to cool down and rinse using THF
5	Deposition of AlN by reactive sputtering Al in Ar and N ₂ ambient
6	Evaporation of Al using Resistive-Heated evaporator and shadow mask

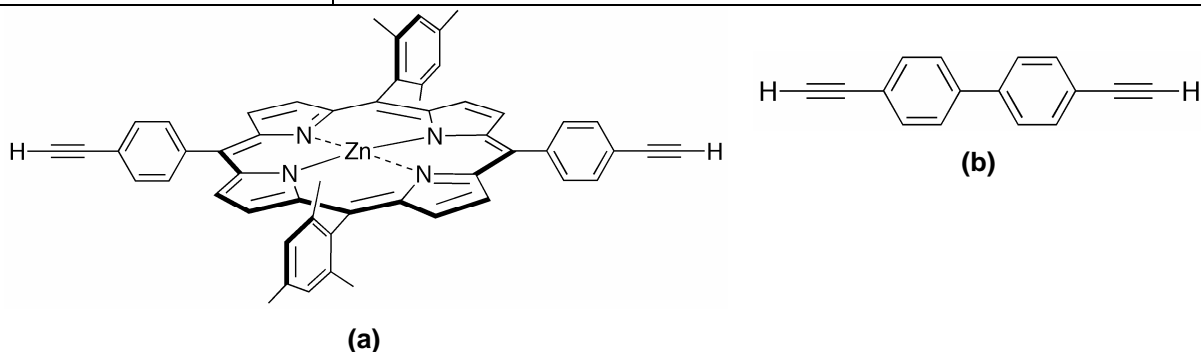


Figure 5.6 Chemical structures of (a) redox-active **Por-m** and (b) non-redox active **BiP-m**

5.4.3 Characterization of AlN layers

Aluminum nitride layers were deposited using reactive sputtering of Al in N_2 for varying durations of time and partial pressures of N_2 in Argon. Both p-Si and n-Si substrates were used to deposit AlN. CV characteristics at varying frequencies were performed on the MIS capacitors in order to estimate the thickness of AlN layers from the accumulation capacitance (C_{acc}). These capacitors exhibited good “MOS-CV” characteristics without much hysteresis between the forward and reverse CV scans. A representative CV characteristic of an MIS capacitor with AlN on n-Si is displayed in Fig. 5.7 (a). The measurement frequency was 1 kHz. The capacitors exhibited large frequency dispersions and shifts in flat-band voltage as the frequency of measurement was increased. One plausible reason for this behavior might be presence of interface states at the AlN-Si interface. The capacitors did not go through any kind of high temperature annealing steps after the deposition of AlN. Therefore, they are expected to have large densities of interface states. An argon-to-nitrogen ratio of 40 : 20 sccm was found to produce the best CV characteristics with minimum hysteresis and frequency dispersion.

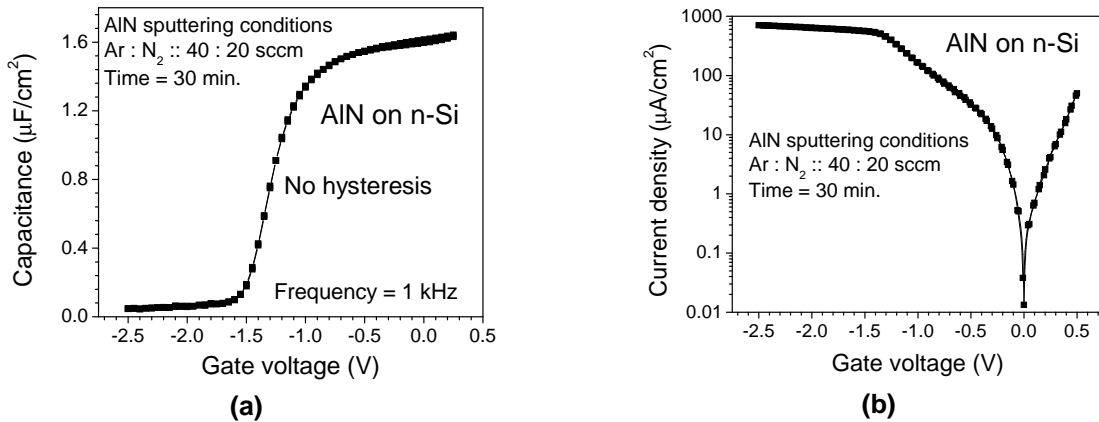


Figure 5.7 (a) CV and **(b)** IV characteristics of an MIS capacitor with AlN on n-Si substrate. AlN was deposited for 30 minutes with an Ar- N_2 ratio of 40:20. Al was the gate electrode.

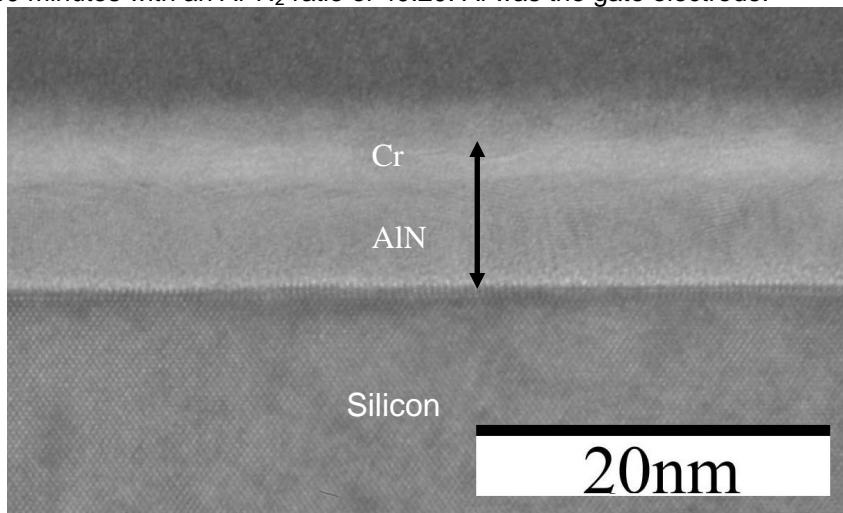


Figure 5.8 High resolution image of AlN layer on silicon obtained using a Transmission Electron Microscope. The AlN was deposited at an Ar- N_2 ratio of 40:20 sccm for 60 minutes.

AlN depositions for durations of times varying from 15 to 60 minutes resulted in thicknesses from 50 to 120 Å. These thicknesses were estimated from the accumulation capacitance of the CV curves, using the equation $C_{acc} = \frac{e_{AlN}}{t_{AlN}}$ and a dielectric constant of 8.9 for AlN. However, these estimates might not be accurate because the effective dielectric constant of AlN on Si may not be 8.9. AlN thicknesses measured using ellipsometry were 118 Å and 70 Å for deposition times of 60 and 30 minutes, respectively. Fig. 5.8 shows an image of an AlN-Si capacitor capped with a layer of chromium (Cr) obtained using a Transmission Electron Microscope (TEM). The AlN deposition time for this capacitor was 60 minutes. The image shows a very uniform layer of AlN on Si. The AlN thickness obtained from this image is approximately 90 Å. Gate leakage characteristics of MIS capacitors were also measured for varying AlN thickness. Fig. 5.7 (b) shows the IV characteristics of an MIS capacitor with 30 minutes AlN on n-Si. As can be seen from the figure, the leakage currents at negative gate voltages are approximately 0.75 mA/cm², which indicate that AlN layers behave like insulators. However, the conductance becomes very high in the accumulation region of the capacitor. Therefore, for the MIMS capacitors, n-Si substrates were employed since charging and discharging of molecules take place at negative gate voltages (accumulation for p-Si; depletion/inversion for n-Si).

5.4.4 Characterization of MIMS capacitors

Fig. 5.9 shows the CyV characteristics of **Por-m** attached to p-Si and n-Si substrates. A 1 mM solution was used during the attachment procedure. The charge densities obtained are 10¹⁵ and 2×10¹⁴ cm⁻² on p-Si and n-Si, respectively. The availability of holes at the surface of n-Si and the slow generation rate of minority carriers limit the extent of oxidation of molecules on n-Si. The densities obtained using a 0.1 mM solution was approximately 4×10¹³ cm⁻², indicating that concentrations as low as 0.1 mM lead to the formation of just a monolayer of **Por-m** rather than a thick polymer film.

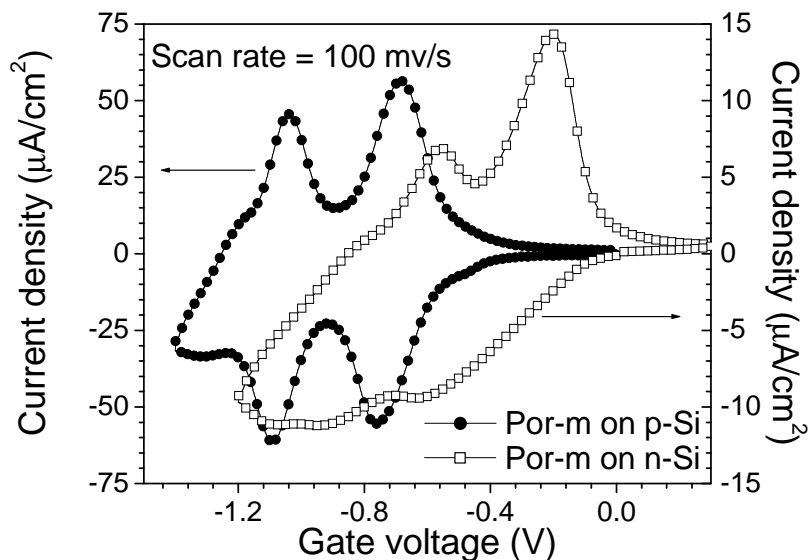


Figure 5.9 CyV characteristics of **Por-m** on p-Si and n-Si substrates. Scan rate is 100 mV/s.

Fig. 5.10 (a) shows CV characteristics of an MIMS capacitor with AlN deposited on a polymer film of **Por-m** on n-Si. The concentration of the solution used for attachment was 0.1 mM. AlN was deposited for 30 minutes at an Ar-N₂ ratio of 40:20 sccm. As can be seen from Fig. 5.10 (a), peaks in CV are observed in both the forward and reverse scans. There's also hysteresis between the forward and reverse CV scans. For a capacitor with no AlN (Al directly on **Por-m**), the peaks in CV were not as prominent and no clear hysteresis was seen [inset in Fig. 5.10 (a)]. Also, no peaks or hysteresis were observed for capacitors with no molecules or with polymer film of non-redox active **BiP-m**, as shown in Fig. 5.10 (b). The concentrations of solution used for attachment of **BiP-m** were 0.1 to 2 mM and the attachment temperature was 250 °C. However, when the concentration was increased to 10 mM and the attachment temperature was raised to 400 °C, the resulting MIMS capacitor with AlN on polymer film of **BiP-m** exhibited peaks and hysteresis in CV, as shown in Fig. 5.11. These peaks and hysteresis are similar to those seen for MIMS capacitors with **Por-m**.

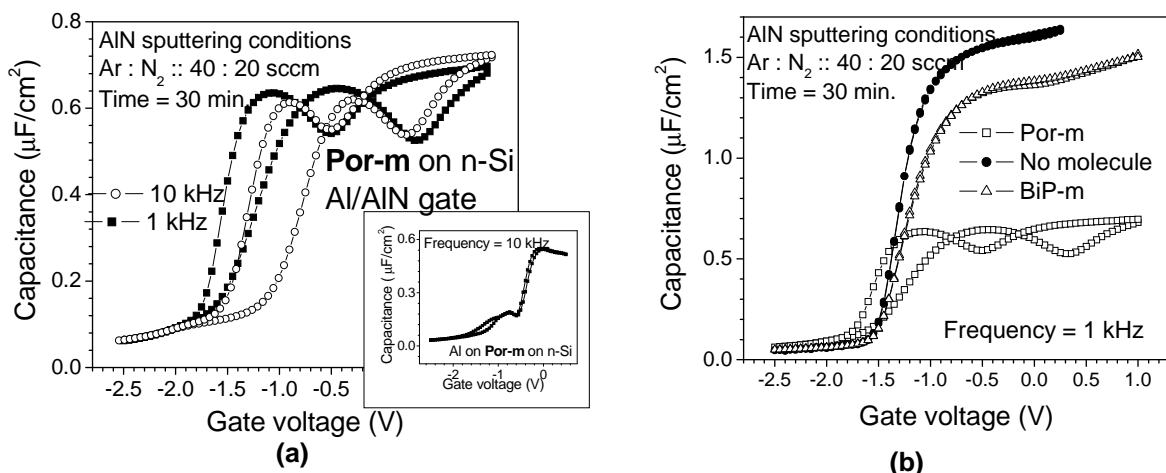


Figure 5.10 (a) CV characteristics of a MIMS capacitor with AlN deposited on **Por-m** on n-Si. The gate is evaporated Al. AlN was deposited for 30 minutes at an Ar-N₂ ratio of 40:20 sccm. Inset shows CV of a capacitor with no AlN. (b) CV characteristics of MIMS capacitors with **Por-m** and **BiP-m**, and an MIS capacitor. AlN conditions are same as in (a)

One plausible explanation for the presence of peaks and hysteresis in the CV characteristics of MIMS capacitors with **Por-m** is charging and discharging of molecules in the polymer film. As the gate voltage is swept from negative to positive, the surface of n-Si goes from accumulation to depletion. As the gate voltage reaches the redox voltage of the molecules, the molecules become oxidized and positively charged, thereby resulting in an increase in the capacitance. Once the molecules are oxidized, the Si surface goes further into depletion. Furthermore, the presence of positive charges between the dielectric (AlN) and Si causes the flatband voltage to shift towards more negative values, which can be observed as hysteresis in the CV. This explanation would be valid had the peaks and hysteresis been observed only for capacitors with redox-active molecules. However, since capacitors with non-redox active **BiP-m** also revealed peaks and hysteresis in the CV characteristics, redox charging and discharging is probably not responsible for this behavior. For MIMS capacitors with AlN on **BiP-m**, this behavior was observed only when the attachment

temperature was 400 °C. When the attachment was carried out at lower temperatures (250 °C), no peaks or hysteresis were observed, as shown in Fig. 5.10 (b). Attachment at high temperatures may have introduced high densities of interface states at the molecule-Si interface that might be responsible for the CV behavior shown in Fig. 5.10 (a) and Fig. 5.11. Nevertheless, these CV measurements do not provide any information about redox related charging and discharging of molecules in the polymer films.

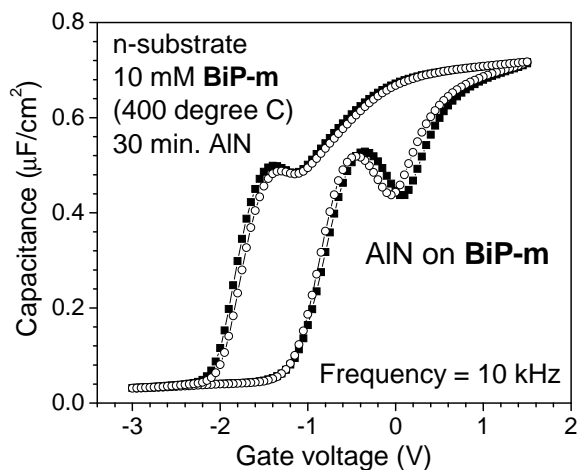


Figure 5.11 CV characteristics of a MIMS capacitor with AlN on a polymer film of **BiP-m**. The concentration of molecular solution was 10 mM. The attachment temperature was 400 °C.

Current-voltage measurements were performed on MIMS capacitors with AlN on polymer films on **Por-m** and **BiP-m**. Fig. 5.12 shows representative IV characteristics of these MIMS capacitors and also an MIS capacitor without any molecules. The AlN was deposited for 30 minutes at an Ar-N₂ ratio of 40:20 sccm. The DC currents were lowered due to the presence of molecular layers. However, no peaks associated with redox states were observed. This is due to the increased current levels compared to those with electrolyte gate (Fig. 5.9). Again, these measurements do not reveal any characteristic redox related charging and discharging either.

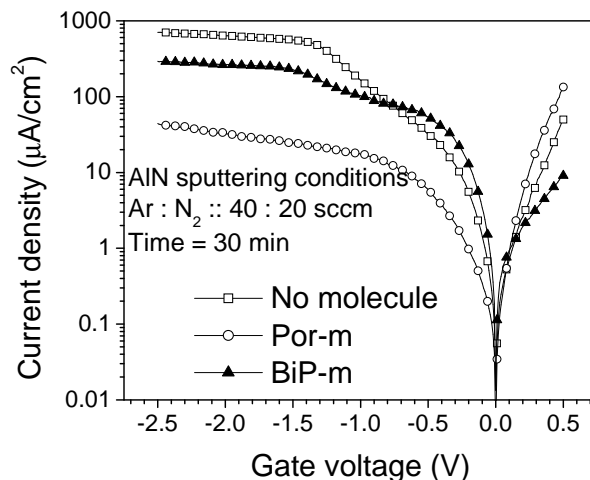


Figure 5.12 IV characteristics of capacitors with **Por-m**, **BiP-m** and without any polymer

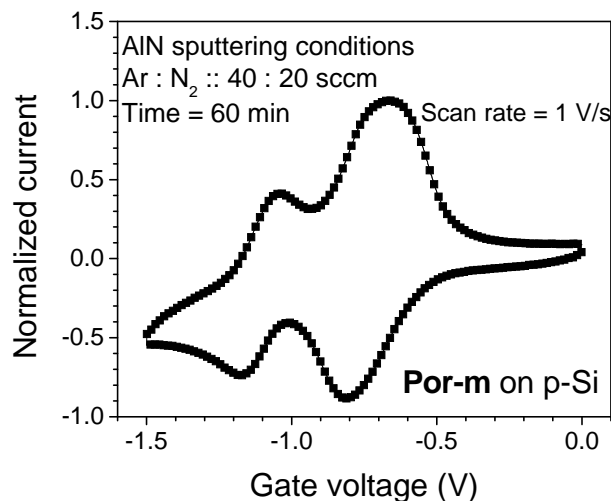


Figure 5.13 CyV characteristics measured using an electrolyte gate on AIN deposited on a polymer film of **Por-m**. The substrate is p-Si. Concentration of molecular solution was 1 mM. AIN was deposited for 60 minutes at an Ar-N₂ ratio of 40:20 sccm.

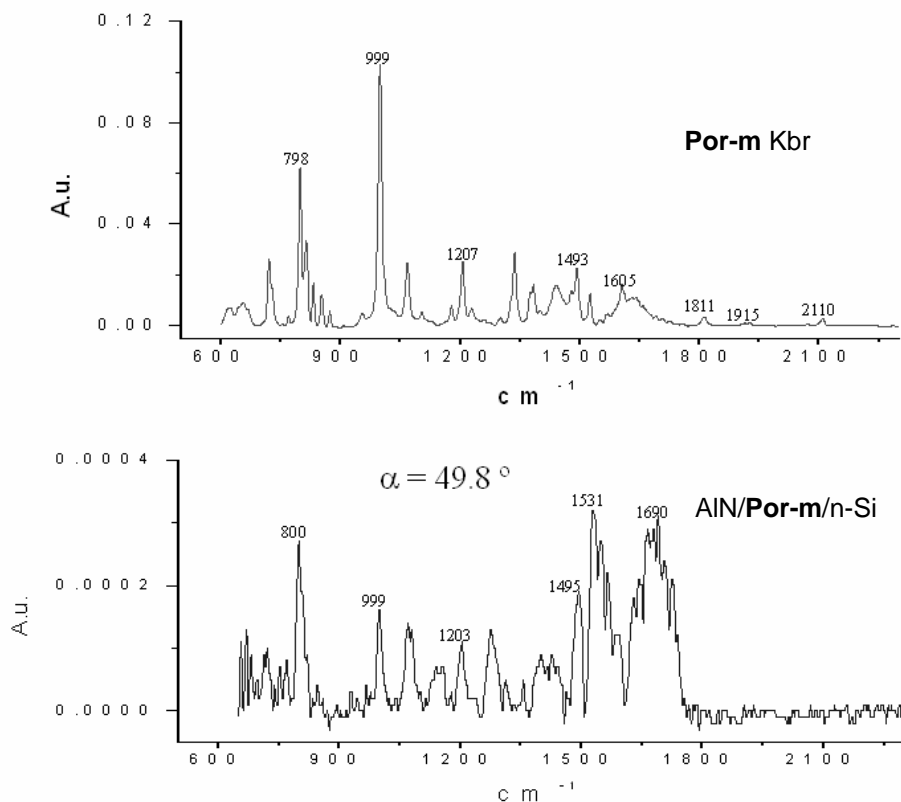


Figure 5.14 IR spectroscopy of AIN/**Por-m**/n-Si (bottom) vs. solid KBr (top). Out-of-plane and in-plane molecular bands are observable for the AIN case indicating the presence of porphyrin molecule after AIN deposition.

In order to verify that the redox properties of molecules were preserved after the deposition of AIN layers on top of the polymer films, electrolyte was used as a gate on top of AIN to perform electrical characterization. Fig. 5.13 shows CyV characteristics of a capacitor with an electrolyte gate on AIN deposited on top of a polymer film of **Por-m**. As can be seen from this figure, two peaks

associated with redox are observed both in negative and positive currents. These peaks correspond to charging and discharging of the redox-active **Por-m** molecules in the polymer film. The AlN deposition was carried out for 60 minutes at an Ar-N₂ ratio of 40:20 sccm. The presence of distinct current peaks in the CyV characteristics indicates that the redox properties of molecules were preserved after the deposition of AlN layers. The reason for observing peaks with electrolyte gate and not with Al gate on AlN is unclear. Firstly, the electrolytic double layer that is formed at the interface between electrolyte and AlN could be providing additional insulating barrier within the capacitor structure, thereby decreasing the DC leakage currents. Consequently, the charging and discharging currents would be revealed due to lower total current. Another possible reason for observing peaks with electrolyte is the slow conduction. Unlike with Al gate where the conduction is all-electronic, the conduction in the electrolytic capacitor is partly ionic. This might be limiting the overall speed of electron transfer, and hence allowing it to be captured in the CyV characteristics. A third possibility is that the electrolyte might be seeping through the AlN layers and be directly in contact with the molecules. This would result in a double layer around the molecules, which would effectively screen positive charges within the molecules via ions in the electrolyte. As a result, more number of molecules might be getting charged and discharged than in the solid-state cell, thereby increasing the redox related currents. Infrared spectroscopy data shown in Fig. 5.14 further illustrates that the molecules in the polymer film remain unaffected by the AlN deposition process.

5.5 Summary

The roles of electrolyte and double layer in EMS and EMOS capacitors were studied. The double layer, which surrounds the molecules, effectively screens the charges thereby allowing high densities of molecules to be written. A combination of metal and insulator has been proposed to replace the electrolyte to create complete solid-state hybrid silicon-molecular devices.

A stack of aluminum and aluminum nitride has been deposited on polymer films of porphyrin molecules. Electrical characterization with electrolyte on AlN layers deposited on porphyrin polymers revealed that the redox properties of the molecules were unaffected after the deposition of AlN layers. However, charging and discharging characteristics were not observed in electrical measurements performed on complete solid-state cells.

For DRAM applications, high densities of charges are desirable in the molecular layers. In order to be able to attain such high densities, the charges in the molecules have to be screened by the dielectric layer above them. This would ensure that the electric field across the barrier between the molecules and the underlying substrate remains high enough for oxidation of all the molecules. For this purpose, the dielectric material above the molecules has to have a high dielectric constant. Furthermore, this layer also needs to be thin in order to increase the capacitance of the layer so that most of the gate voltage appears across the barrier underneath the molecules.

It has been demonstrated that redox-active molecules can survive the deposition of materials on top of them. The need for a high-k material on top of the molecules has been recognized and further investigations on suitable high-k materials are necessary. Direct current-voltage measurements may not reveal charging and discharging of molecules in solid-state molecular devices. CV measurements, pulsed IV measurements and FET structures may be required in order to reveal the molecular signature in solid-state devices.

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6. SUMMARY AND FUTURE OUTLOOK

6.1 Goals of this study

The focus of this work has been on studying the properties of devices created by incorporating redox-active organic molecules on a silicon platform. The motivation was to examine the possibility of using charge storage properties of redox compounds for memory applications by creating a class of hybrid silicon-molecular devices. The particular goals of this study were –

- i. To fabricate capacitor structures with redox molecules on silicon surfaces and to study the interactions between the discrete molecular energy levels and the energy bands of Si.
- ii. To attach molecules to SiO₂ surfaces to introduce a tunnel barrier for electrons between the molecules and Si; to study the dependence of oxidation & reduction voltages and charge retention properties on oxide thickness.
- iii. To incorporate redox-active molecules on Si and SiO₂ surfaces in an FET-type structure in order to modulate the threshold voltage and current-voltage characteristics of the device by charging and discharging the molecules for FLASH memory applications.
- iv. To understand the role of electrolyte in charging and discharging of molecules in hybrid silicon-molecular devices and to investigate solid-state replacements for the liquid electrolyte.

6.2 Conclusions and specific findings

Many significant findings have been made while working towards achieving the above mentioned goals. The conclusions of this work along with the major contributions are summarized below.

- i. Monolayers of two-state ferrocene and three-state porphyrin molecules have been formed on Si surfaces. The charge densities achieved in these monolayers were 1.5×10^{14} and $4.5 \times 10^{13} \text{ cm}^{-2}$, respectively. Electrical characterization of these monolayers immobilized on Si surfaces was performed using cyclic voltammetry and impedance spectroscopy techniques.
- ii. Both p-Si and n-Si substrates, with varying doping densities, were used to attach molecules. The oxidation and reduction voltages of the molecules were found to depend on the Si doping type. Furthermore, for n-Si, the redox voltages were also dependent on the doping density. No such dependence was observed for p-Si. These differences have been explained using differences in work functions and Si surface potentials (p-Si: accumulation; n-Si: depletion/inversion).

- iii. The oxidation process was found to be limited by the availability/generation rate of holes, which are minority carriers in n-Si. An external source of light was used to increase the generation rate of holes to further illustrate this limitation.
- iv. Porphyrin polymer films, exhibiting very high charge densities ($\sim 10^{15} \text{ cm}^{-2}$), were formed on n-Si and p-Si substrates. However, the oxidation and reduction processes were found to occur at slower speeds compared to monolayers. Also, the uniformities of thickness and charge density were not well controlled.
- v. Ferrocene monolayers were formed on SiO_2 surfaces, with varying thickness of SiO_2 on p-Si. The separation between oxidation and reduction voltages increased with increasing t_{ox} due to the oxide barrier. The two processes were completely separated from each other for t_{ox} greater than 1.8 nm, resulting in a voltage range where both the charging and discharging rates were negligibly low. Charge retention times increased with increasing t_{ox} .
- vi. The reduction process was limited by electron tunneling current from Si through SiO_2 , which is dependent on the amount of electrons available at the Si surface and the voltage drop across the oxide barrier. Threshold voltage assisted reduction was found to occur following the creation of an inversion layer.
- vii. Molecules were incorporated on Si and SiO_2 surfaces in the channel regions of n-FET structures. It was not possible to modulate transistor characteristics by charging and discharging the molecules because the regions of redox were at negative gate voltages, whereas the transistor operation was in positive gate voltages.
- viii. Threshold voltage and current-voltage characteristics of p-FET devices were modulated by charging and discharging ferrocene molecules that were incorporated on the channel regions of the device. These results showed that redox molecules can indeed be used as charge storage elements to create future generation nanoFLASH memory devices.
- ix. The role of electrolyte and the electrolytic double layer were studied and it was concluded that the high-k, ultra-thin double layer surrounding the molecules was responsible for high densities of charges in monolayers. A solid-state replacement of the electrolyte in the form of a metal-insulator stack was proposed. Requirements for the insulator material were identified.
- x. Aluminum and aluminum nitride were employed as candidate replacements for the electrolyte. AlN layers were deposited on polymer films of porphyrin molecules by sputtering Al in a nitrogen environment. Redox properties of the molecules in the polymer film were preserved after the deposition of AlN layers. However, charging and discharging characteristics were not evident in electrical characteristics of a complete solid-state cell.

6.3 Future outlook

Significant developments have been made in the development and understanding of hybrid silicon-molecular devices incorporating redox-active molecules on a silicon platform. The future in this field looks interesting and many areas require attention in order to transfer this technology from the research phase to real-world applications. Some of these areas are listed below.

6.3.1 DRAM applications

The major advantages of this hybrid technology over existing DRAM technology are (i) the ability to achieve very high charge densities at very low applied voltages, and (ii) long charge retention times that require lesser number of refresh cycles. In order to achieve a solid-state memory cell that retains these advantages, alternative high-k materials for the dielectric on top of molecules need to be investigated. Fast read, write and erase can only be achieved using an all-electronic device and the primary. The most important future goal is to replace the electrolytic double layer using a solid-state dielectric material.

6.3.2 FLASH applications

The important criterion for FLASH memory devices is non-volatility. It has been established that the retention times of these molecules increase with increasing barrier thickness (SiO_2). In order to achieve non-volatility, SiO_2 thickness in the range of 6.5 nm needs to be explored. At such thickness values, the write/erase voltages would further increase. The impact of this increase on the separation between adjacent states in multi-state molecules has to be studied. The discrete multiple state properties of redox-active molecules are the most attractive components for FLASH applications – future work requires ensuring that these properties are maintained while achieving non-volatility.

6.3.3 Solid-State approach

A solid-state approach is imperative for this technology to be able to compete with other emerging technologies and to integrate it with existing CMOS technology. As mentioned before, high-k materials need to be investigated as candidate replacements for the double layer. The vast knowledge base established from research on high-k dielectrics over the past decade can be utilized for this purpose. The important question that needs to be addressed is if it will be possible to achieve charge densities of the order of 10^{14} cm^{-2} and higher without the dielectric surrounding the molecules, thereby electrostatically isolating individual molecules from one other. Theoretical calculations based on electrostatics need to be performed to better define the thickness and dielectric constant requirements of the insulating materials both above and below the molecules. The deposition technique for the new material and the material properties have to be compatible with the molecules and should not adversely affect their charge storage properties.

6.3.4 Monolayer vs. Polymer

It has been shown that very high charge densities can be achieved by using polymer films. However, the polymer films are inherently slower than monolayers. Further examination is required to understand the exact mechanism of charge transport in the polymer films. Also, the slowness might not be an impeding factor for FLASH applications since the SiO₂ barrier is rate limiting. Therefore, polymer films need to be incorporated in moleFET devices and the differences between monolayers and polymers have to be identified.

6.3.5 Molecules, their stability and endurance

Endurance and stability are key issues that need to be addressed before this technology heads into the development and manufacturing stages. Reasons for degradation of coverage with electrical stressing have to be recognized. Studied related to the strength and endurance of covalent bonds formed between molecules and the substrate have to be performed. A thorough understanding of the pros and cons of different types of covalent bonds – O-Si, P-O-Si, C-Si etc. – is required in order to choose between the two. Thermal stability of molecules is another important aspect that needs to be dealt with. In order to be able to integrate this technology with existing fabrication processes, molecules need to be able to withstand high temperatures for extended periods of time (450 °C for back-end and ~ 900 °C for front-end processing). These stability issues will be important parameters to be considered while incorporating molecules with three and higher number of states.

6.3.6 Test structures and characterization techniques

New test structures and characterization techniques may need to be developed in order to verify that charging and discharging processes take place in the solid-state memory cells. These processes may be occurring at high rates and hence may not be captured in transient current-voltage measurements. Furthermore, in order to investigate lateral conductivity between molecules within a monolayer and to understand the scaling behavior of these molecules, they have to be incorporated in nano-sized test structures.

6.3.7 Physics of devices

The concepts that have been developed for two-state ferrocene molecules have to be extended to three-state porphyrins and other molecules with higher number of states. Simulation models for these molecular devices need to be developed in order to accurately simulate the working of individual devices as well as large density memory arrays.

6.3.8 Novel structures and applications

Novel structures incorporating molecules within a dielectric layer can be explored for charge storage memory devices. Applications of redox-active molecules in areas other than memories can also be investigated. Molecules on different substrates (n-Si, p-Si, SiO₂ with varying thickness, metal

and other insulating substrates) have different redox voltages and rates of electron transfer. This property can be utilized to create molecules on devices with varying substrates so that selective smaller areas can be accessed at different applied voltages. Metal directly on molecules attached to metallic or semiconducting substrates can be used as resonant tunneling diodes that have varying conductivities at different applied voltages. These structures have potential applications in the field of logic devices.

6.4 Closing remarks

This technology has evolved from its incipient stage over the past 6 years. Many ideas that were formed back then have been proven experimentally. Redox-active molecules on a silicon platform have indeed shown to possess charge storage properties. Lots of interesting challenges lie ahead before this field matures into an advanced technology. This hybrid technology can lead to the conceptualization and development of “molecule-only” electronics, where individual molecules may be synthesized with separate charge storage, insulating, metallic and semiconducting units. As Feynman said in his famous speech in 1959, “*There’s plenty of room at the bottom*” and we are on our way to occupy!