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(54) **METHOD FOR FABRICATING TRANSISTOR GATE STRUCTURES AND GATE DIELECTRICS THEREOF**

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See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,352,623 A	10/1994	Kamiyama
5,891,809 A	4/1999	Chau et al.
6,013,553 A	1/2000	Wallace et al.
6,015,739 A	1/2000	Gardner et al.
6,020,243 A	2/2000	Wallace et al.
6,136,654 A	10/2000	Kraft et al.
6,251,761 B1	6/2001	Rodder et al.

6,291,866 B1	9/2001	Wallace et al.
6,291,867 B1	9/2001	Wallace et al.
6,436,801 B1	8/2002	Wilk et al.
6,544,906 B1	4/2003	Rotondaro et al.
6,624,090 B1	9/2003	Yu et al.
6,642,131 B1 *	11/2003	Harada 438/591
6,809,370 B1 *	10/2004	Colombo et al. 257/310
6,875,678 B1 *	4/2005	Jung et al. 438/591
2003/0045080 A1 *	3/2003	Visokay et al. 438/591
2003/0052358 A1	3/2003	Weimer
2003/0080389 A1	5/2003	Hu et al.
2003/0129817 A1 *	7/2003	Visokay et al. 438/591

OTHER PUBLICATIONS

“Fabrication of HfSiON Gate Dielectrics by Plasma Oxidation and Nitridation, Optimized for 65nm node Low Power CMOS Applications”, Seiji Inumiya, Katsuyuki Sekine, Shoko Niwa, Akio Kaneko, Motoyuki Sato, Takeshi Watanabe, Hironobu Fukui, Yoshiki Kamata, Masato Koyama, Akira Nishiyama, Mariko Takayanagi, Kazuhiro Eguchi and Yoshitaka Tsunashima, 2003 Symposium on VLSI Technology Digest of Technical Papers, 2 pgs.

* cited by examiner

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(57) **ABSTRACT**

Methods are disclosed for treating deposited gate dielectric materials, in which the deposited dielectric is subjected to one or more non-oxidizing anneals to densify the material, one or more oxidizing anneals to mitigate material defects, and to a nitridation process to introduce nitrogen into the gate dielectric. The annealing may be performed before and/or after the nitridation to mitigate deposition and/or nitridation defects and to densify the material while mitigating formation of unwanted low dielectric constant oxides at the interface between the gate dielectric and the semiconductor substrate.

40 Claims, 5 Drawing Sheets

